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DESIGN OF A LOW POWER FLIP-FLOP USING CMOS DEEP SUBMICRON TECHNOLOGY

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Abstract— This paper enumerates low power, high speed design of flip-flop having less number of transistors and only one transistor being clocked by short pulse train which is true single phase clocking (TSPC) flip-flop. Compared to Conventional flip-flop, it has 5 Transistors and one transistor clocked, thus has lesser size and lesser power consumption. It can be used in various applications like digital VLSI clocking system, buffers, registers, microprocessors etc.

The analysis for various flip flops and latches for power dissipation and propagation delays at 0.13µm and 0.35µm technologies is carried out. The leakage power increases as technology is scaled down. The leakage power is reduced by using best technique among all run time techniques viz. MTCMOS. Thereby comparison of different conventional flip-flops, latches and TSPC flip-flop in terms of power consumption, propagation delays and product of power dissipation and propagation delay with SPICE simulation results is presented.

Keywords— *CMOS, figure of merit, leakage current, power, delay, TSPC flip-flop.*

I. INTRODUCTION

Flip-Flop is an electronic circuit that stores a logical state of one or more data input signals in response to a clock pulse. Flip-flops are often used in computational circuits to operate in selected sequences receive and maintain data for a limited time period sufficient for other circuits within a system to further process data [1].

At each rising or falling edge of a clock signal, the data stored in a set of flip-flops is readily available so that it can be applied as inputs to other combinational or sequential circuitry. Such flip-flops that store data on both the leading edge and the trailing edge of a clock pulse are referred to as double-edge triggered flip-flops otherwise it is called as single edge triggered flip-flops.When technology scales down, total power dissipation will decrease and at the same time delay varies depends upon supply voltage, threshold voltage, aspect ratio, oxide thickness, load capacitance.
CMOS devices have scaled downward aggressively in each technology generation to achieve higher integration density and performance. However leakage current has increased drastically with technology scaling and become a major contributor to the total IC power.

II. BRIEF LITERATURE REVIEW

A. 8 Transistor T flip-flop and 6 transistor latch circuit
8 during recurring clock intervals to Transistors flip-flop the pioneer CMOS traditional flip-flop circuit is reported in Ref [1]. 6 transistor latch is built using 4 NMOS and 2 PMOS transistors [1-3].

B. 5 Transistors proposed TSPC flip-flop

The schematic of proposed TSPC flip-flop is shown in Fig

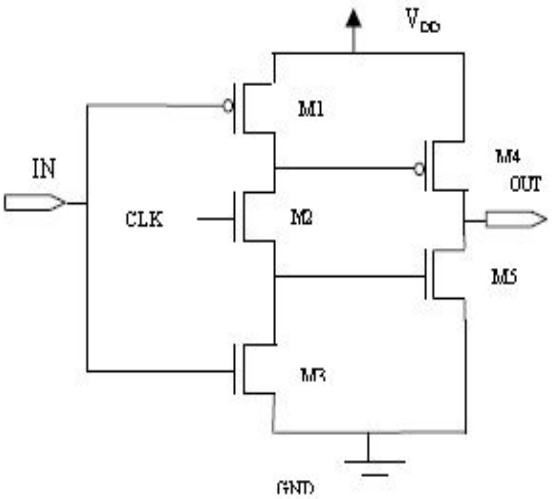

Fig. 1. 5 transistor TSPC FF

1. This flip-flop is built using transistors [1-3].

Fig. 1 shows positive edge triggered 5 Transistor D latch. When CLK and input IN are high then the transistors M1, M5 are OFF and remaining transistors M2, M3, M4 are ON. The output becomes high. During ON clock period whatever is the values of input it becomes output. It also acts as a flip-flop when the input IN has less pulse width.

IV. LEAKAGE POWER ANALYSIS

Minimization power consumption is essential for high performance VLSI systems. In digital CMOS circuits there are three sources of power dissipation, the first is due to signal transition, the second comes from short circuit current which flows directly from supply to ground terminal and the last is due to leakage currents. As technology scales down the short circuit power becomes comparable to dynamic power dissipation [4-5]. Furthermore, the leakage power also becomes highly significant. High leakage current is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length and gate oxide thickness are reduced [6-8]. Consequently, the identification and modeling of different leakage components is very important for estimation and reduction of leakage power especially for low-power applications. Multivariable Threshold voltage CMOS (MTCMOS) and voltage scaling are two of the methods to reduce power.

V. MTCMOS TECHNIQUE

MTCMOS is one of the important low power techniques and is used to reduce the leakage. Fig. 2 shows TSPC FF with this technique.

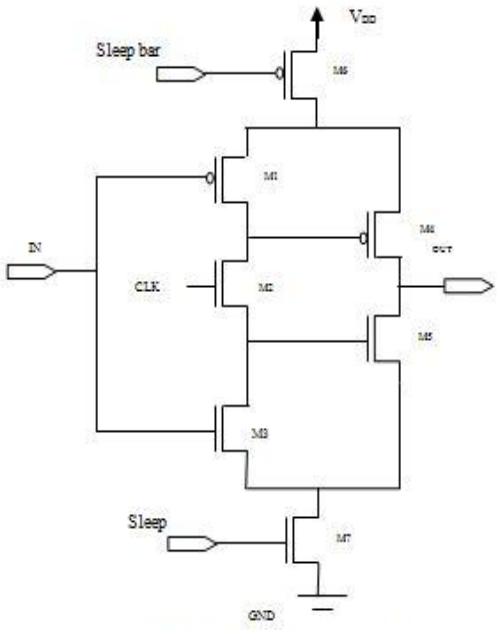

Fig. 2. TSPC FF with MTCMOS technique

To reduce leakage power in MTCMOS circuits, sleep and

sleep bar transistors are high threshold voltages. When sleep input is OFF and sleep bar input is ON, there is no current flow in the low threshold voltage main circuit. When sleep is ON and sleep bar is OFF then the circuit works in normal mode.

VI. RESULTS AND DISCUSSION

Performance analysis of Various FFs and latches is presented in this section. TSPICE is used to carry out the present work [9]. 0.13µm, 0.35µm, 0.8µm technology nodes have been considered. TABLES I to IV shows power dissipation, delays and figure of merit in terms of power delay product (PDP) for various latches and flip-flops for different technologies for scaled supply voltages

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TABLE I
0.13µm TECHNOLOGY DELAY, POWER DISSIPATION AND FIGURE OF MERIT WITH VDD=1.8V

Circuit	Delay (ns)	Power Dissipation (µW)	Figure of Merit (fJ)
5T Latch	46.80	11.15	521.82
6T Latch	47.07	11.62	546.95
5T FF	47.54	10.848	515.75
8T FF	3.62	16.38	60.31

From Table I it is clear that 5T LATCH is having 1.5% lesser delay when compared with the 5T FF, but the power dissipation of 5T Latch transistor is 2.78µW higher and figure of merit of 5T LATCH transistor is 1.176 % higher. Compared to 6 Transistor D Latch the 8 Transistor T FF, is having higher power dissipation but delay is 92.26% lesser. 8T FF shows least PDP compared to all circuits. Compared to 5T latch, 5T flip-flop has lesser PDP which represents better performance at maximum supply voltage.

TABLE II

0.13µm TECHNOLOGY DELAY, POWER DISSIPATION AND FIGURE OF MERIT WITH SCALED VDD=1.2V

Circuit	Delay (ns)	Power Dissipation (µW)	Figure of Merit(fj)
5T Latch	48.44	4.06	196.66
6T Latch	47.95	4.59	220.09
5T FF	51.01	3.83	195.36
8T FF	4.62	6.65	30.72

TABLE II, shows that 5T Latch is having 5.03% lesser delay when compared with the 5T FF, but the power dissipation of 5T Latch is higher and PDP of 5T Latch is 1.3fj higher. This shows that the over all performance of 5T FF is better. Compared to 8T FF, 6T Latch is having 2.06µW lesser power dissipation but delay of 8T FF is 92.26% lesser than T Latch. 8T FF has lowest PDP thereby highest figure of merit as compared to all circuits. Compared to 5T latch, 5T FF shows lesser PDP even for highly scaled V_{DD} of 1.2V, which is advantageous.

TABLE III

0.35µm TECHNOLOGY DELAY, POWER DISSIPATION AND FIGURE OF MERIT FOR VDD=5V

Circuit	Delay (ns)	Power Dissipation (µW)	Figure of Merit(fj)
5T Latch	43.51	72.29	3145.33
6T Latch	44.03	88.69	3905.02
5T FF	44.54	68.60	3055.44
8T FF	3.173	140.30	445.17

In TABLE III, 5T Latch is having 2.3% lesser delay when compared with the 5T FF, but the power dissipation of 5T Latch is 5.78µW higher and figure of merit of 5T Latch is 2.94% lesser as PDP is higher. Compared to 8T FF, 6T Latch is having 0.36µW lesser power dissipation and the delay 92.79% lesser. 8T FF is having least PDP thus highest figure of merit as compared to all circuits. Compared to 5 Transistor latch, 5 Transistor flip-flop has less PDP and represents better performance at a supply voltage of 5V for 0.35µm technology node as well.

TABLE IV

0.35µm TECHNOLOGY DELAY, POWER DISSIPATION AND FIGURE OF MERIT FOR A SCALED VDD=3.3V

Circuit	Delay (ns)	Power Dissipation(µW)	Figure of Merit(fj)
5T Latch	44.11	33.87	1494.60
6T Latch	47.23	40.13	1895.50
5T FF	45.29	30.96	1402.42
8T FF	3.56	60.35	215.38

From TABLE IV, 5T Latch is having 2.6% lesser delay when compared with the 5T FF, but the power dissipation of 5T Latch transistor is 9.39µW higher and figure of merit of 5T Latch is 6.57 higher. Compared to 8T FF, 6T D Latch is having 0.33µW lesser power dissipation and the delay 92.46% lesser. Compared to 5T latch, 5T flip-flop has lower PDP and therefore has better performance even for a scaled supply voltage of 3.3V.

A. Variation of power and delay

Variation of power and delay with supply voltage for various flip-flops is presented in Fig. 3 to Fig. 6. The performance of 5-transistor latch for 0.13µm Technology is shown in Fig. 3. From Fig. 3 it is seen that the propagation delay decreases with increasing supply voltage and vice versa. As supply voltage increases, power dissipation also increases. The minimum value of supply voltage at 1.5V that would allow delay and power dissipation for normal operation of the circuit. The minimum propagation delay for 5 transistor latch gives a change of 3.13%. Performance of 5-transistor FF for 0.13µm Technology shown in Fig. 4.

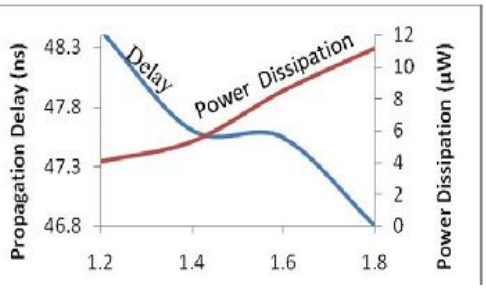

Fig. 3. Variation of power and delay with VDD for 5T latch.

Fig. 4. Variation of power & delay with VDD for 5 T TSPC FF. Fig. 4 shows propagation delay decreases with increasing supply voltage and vice versa. As supply voltage increases, power dissipation also increases. The percentage change in minimum

propagation delay for 5T TSP CFF is 7.83.

Characteristics of 6-transistors FF for 0.13µm Technology
shown in Fig. 5.

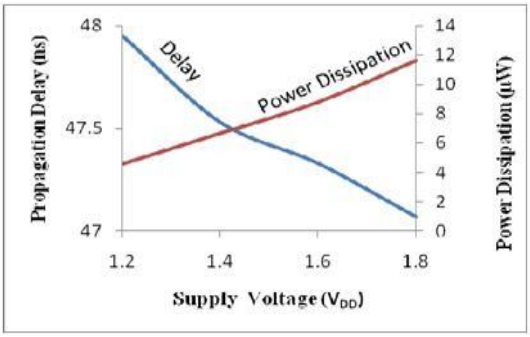

Fig. 5 shows propagation delay decreases with increasing
supply voltage and vice versa. As supply voltage increases,
power dissipation also increases. The minimum propagation
delay for 6-transistor latch shows a change of 2.03%.
Performance of 8-transistors FF for 0.13µm Technology is shown in Fig. 6.

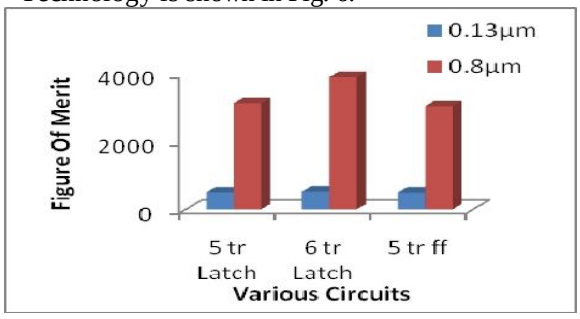

Fig. 6 shows propagation delay decreases with increasing supply voltage and vice versa. As supply voltage increases, power dissipation also increases. The percentage change for minimum power dissipation for 8-transistor FF is 66.6

B. Figure of Merit from 0.13µm and 0.8µm Technology
PDP is considered figure of merit is shown in Fig. 7. In the present analysis the minimum PDP corresponds to the best performance of the circuit.

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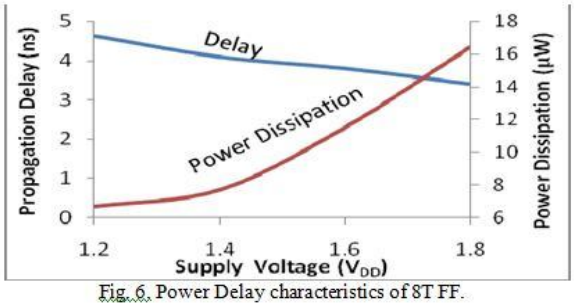


Fig. 6. Power Delay characteristics of 8T FF.

Fig. 7 shows that when power supply increases, delay decreases and the power dissipation increases. Amongst all the FFs and Latches, TSPC 5-Transistor FF is having least power dissipation and least Figure of merit or PDP for 0.13µm Technology. Compared to 0.35µm technology, 0.13µm technology is giving lesser power consumption and also less PDP therefore showing better performance.

C. Leakage Power

Leakage power with MTCMOS Technique and without it (i.e. general) for proposed 5T FF is considered. Leakage power decreases with MTCMOS technique as compared to without this technique for 0.13µm technology by 83.62%. Comparison of power dissipation from 0.13µm to 0.8µm Technologies as shown in Fig. 8. For higher technology the overall power is significantly high as compared to 0.13µm technology. Comparison of leakage power with and without MTCMOS technique is shown in Fig. 9. It shows that when technology scaled down from 0.8µm technology to 0.13µm technology, leakage power increases by 10pW. Furthermore, leakage is reduced by nearly 85% as compared with the original circuit with out MTCMOS technique.

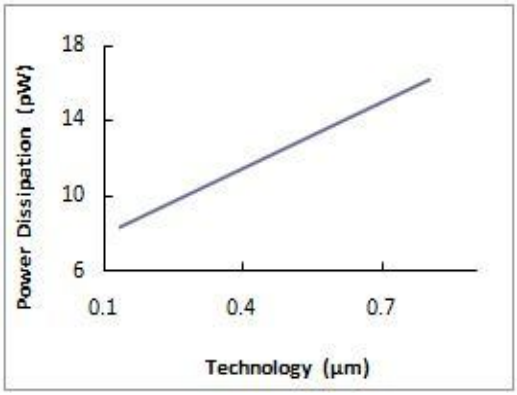
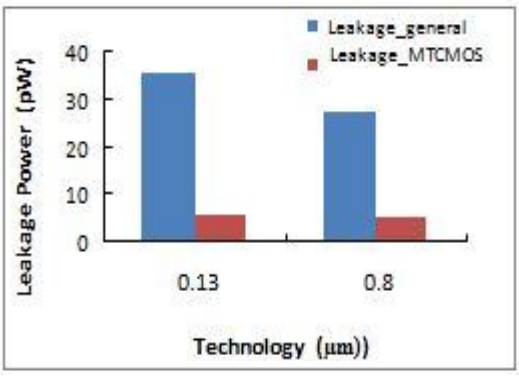


Fig. 8. Comparisons of two technologies in terms of power dissipation.



VII. CONCLUSIONS

From simulation results it is concluded that TSPC Flip-Flop is having less power consumption. This is because it is having only 5 transistors, only one transistor being clocked and that clock is having short pulse train. By applying MTCMOS leakage power minimization technique, the leakage power is minimized when technology scales down.

The flip-flops and latches are simulated for 0.13µm and

0.35µm technology nodes using TSPICE. When technology is

scaled down power dissipation increases and propagation

delay decreases. Figure of merit i.e. PDP is calculated for all circuits. Among these TSPC FF is having least power delay product; therefore its performance is the best. Furthermore, it can be used in various applications like level converters, microprocessors, clocking systems counters and others.

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