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DESIGN APPROACHES FOR LOW POWER- LOW AREA D FLIP FLOP S IN NANO TECHNOLOGY

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Abstract – This paper enumerates design of D flip flop with low power and low area for low power applications, for that analysis of various D-flip flops for low power dissipation ,area and delays is carried out at 0.12um to achieve low power, low-area the technology is scaled down to nanometer ranges, due to shrinking process, the leakage power tends to play a vital role in total power consumption at nano meter technology. In this paper, different D flip flop circuits are designed using Berkeley Short Channel Insulated Gate MOSFET (BSIM4) model equations.. in this paper to reduce leakage power at 90nm 70nm and 50nm we implement leakage power reduction techniques six techniques are considered they are namely Sleep transistor, sleepy stack, Dual sleep ,Dual stack Forced Transistor sleep (FTS) and Sleepy keeper From the results, it is observed that SLEEP TRANSISTOR, and SLEEPY KEEPER.FORCED TRANSISTOR SLEEP techniques produces lower power dissipation than the other techniques , in this paper a qualitative comparison is done with the help of Dsch,, Micro wind Simulation tools, this paper concludes that a leakage reduction technique produce different power optimization levels for different architectures and employing a suitable technique for a particular architecture will be an effective way of reducing the leakage current and thereby static power.

Keywords - *D Flip Flop, Leakage power, Forced Transistor Sleep, sleep transistor, sleepy keeper.*

I. INTRODUCTION

Flip-Flop is an electronic circuit that stores a logical state of one or more data input signals in response to a clock pulse. Flip-flops are often used in Computational circuits to operate in selected sequences during recurring clock intervals to receive and maintain data for a limited time period .At each rising or falling edge of a clock signal, the data stored in a set of flip-flops is readily available so that it can be applied as inputs to other combinational or sequential Circuitry. Delay Flip-Flop (DFF) has been the integral part of any digital system to construct the sequential part of it. to achieve low power low area we have design various D flip flop to analyze the performance of various architectures of DFF with respect to performance metrics such as power, delay, area and Power Delay Product(PDP) at . But as technologies scales down to the nanometer regime (Deep Sub-Micron (DSM)), the static power dissipation becomes more dominant than the dynamic power consumption.

With technology downscaling, interconnect resistance and capacitance increase the propagation delay. Leakage power optimization will be a key design objective in future CMOS circuits. power will continue to be a limiting factor in future technologies. Two major factors for the increase in power dissipation are the speed and the number of gates on the silicon. The two main effects that contribute to the total power dissipation on a chip are the active and static power dissipation. The expression to compute the total power is as follows

$$P_{total} = P_{dynamic} + P_{static} + P_{sc} \quad (1)$$

Dynamic dissipation power occurs when a transistor switches state and is due to capacitive charging and discharging associated with the output wiring. A small proportion of dynamic power arises from the short-circuit current that flows momentarily while the complementary devices (push/pull) in a circuit are simultaneously conducting during a change in the output state. This dynamic power is considerable during normal mode of operation, especially at high operating frequencies. The dynamic power consumption (P_{dyn}) is given by

$$P_{dynamic} = KCV_{dd}^{2} f_{sw} \quad (2)$$

Where k is the technology factor, C is the capacitance of switching nodes, Vdd is the supply voltage and f_{sw} is the effective switching frequency. During the transition of signals from 0 to 1 (or) from 1 to 0both nmos and pmos network of CMOS circuits will be on for a while which leads to short-circuit power dissipation (Psc) and given by

$$P_{SC} = Isc.V_{dd}.ts.fsw \quad (3)$$

Where Isc is the short circuit current, Ts is the switching delay. Both sources of power dissipation (P_{dyn} and P_{sc}) in CMOS circuits are related to transitions at gate outputs and are therefore collectively referred to as active dissipation. In contrast, the third source of power dissipation () is due to leakage current, which flows when the inputs and outputs are changing their state and is called static dissipation (P_{static}). In standard CMOS circuits, only static dissipation is due to

leakage current, usually small in magnitude and will be computed by

$$P_{leak}= I_{leak} \cdot V_{dd} \quad (4)$$

But as the supply voltage is being scaled down to reduce dynamic power, lower threshold transistors have to be used to maintain performance, yet the lower the threshold voltage, greater the standby leakage current. Due to the substantial increase in leakage current, the static power consumption is expected to exceed switching portion of power consumption unless effective measures are taken to reduce leakage power. ,leakage power plays a vital role in deciding the overall power consumption.

II. LEAKAGE POWER ANALYSIS

We have different types of leakage components. They are

1. Sub-threshold leakage (weak inversion current)
2. Gate oxide leakage (Tunneling current)
3. Channel punch through
4. Drain induced barrier lowering

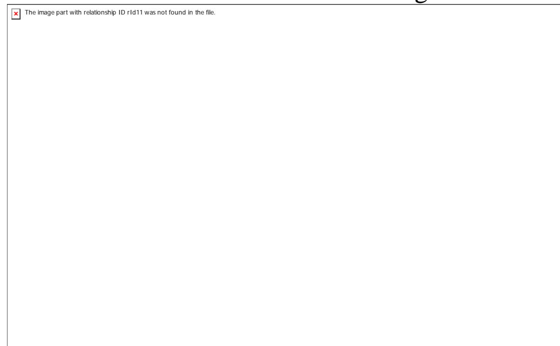

Fig. 1: Leakage power components in CMOS

Figure 1: Schematic Diagram of shunt active power line conditioners

A. Sub Threshold Leakage:

One of the main reasons causing the leakage power increase is increase of sub-threshold leakage power. The Sub-threshold conduction or the sub-threshold leakage or the sub threshold drain current is the current that flows between the source and drain of a MOSFET when the transistor is in sub-threshold region, or weak-inversion region, that is, for gate-to source voltages below the threshold voltage. The sub-threshold region is often referred to as the weak inversion region. When technology feature size scales down, supply voltage and threshold voltage also scale down. Sub-threshold leakage power increases exponentially a sub threshold voltage decreases which increases the sub-threshold leakage power Sub threshold or weak inversion conduction current between source and drain in a MOS transistor occurs when gate voltage is below the transistor threshold voltage (Vt). The Sub threshold or weak inversion current (Ids) can be expressed as

$$I_{ds}=\mu_0 C_{ox}\frac{W}{L}\,(m-1)\,(V_t)^2\; e^{\frac{(V_g-V_{th})}{mv_t}}\;\left(1-e^{\frac{-v_{ds}}{v_t}}\right)$$

$$\text{Where}\quad m=1+\frac{C_{dm}}{C_{ox}}=1+\frac{\frac{\varepsilon_{si}}{W_{dm}}}{\frac{\varepsilon_{ox}}{t_{ox}}} \quad (5)$$

and is threshold voltage and is the thermal voltage. is the gate oxide capacitance, is the zero bias mobility and is the body effect coefficient. is the maximum depiction layer width and is the gate oxide thickness is the capacitance of the depletion layer. Reverse biasing well to source junction of a MOSFET widens the bulk depletion region and increases the threshold voltage. The effect of body bias can be considered in the threshold voltage equation.

B. The Gate Oxide Leakage:

The gate oxide, which serves as insulator between the gate and channel, should be made as thin as possible to increase the channel conductivity and performance. But as the gate oxide is made thinner the barrier voltage of the oxide changes. For the positive gate voltage thus some positive charges get stuck in the oxide. Therefore, current flows through the oxide. This is also known as tunneling current.

C. Channel Punch Through:

Punch through in a MOSFET is an extreme case of channel length modulation where the depletion layers around the drain and source regions merge into a single depletion region. The field underneath the gate then becomes strongly dependent on the drain-source voltage, as is the drain current. Punch through causes a rapidly increasing current with increasing drain-source voltage. This effect is undesirable as it increases the output conductance and limits the maximum operating voltage of the device.

III. REVIEW OF LEAKAGE CURRENT REDUCTION TECHNIQUES

For a CMOS circuit, the total power dissipation includes dynamic and static components during the active mode of operation. In the standby mode, the power dissipation is due to the standby leakage current. Dynamic power dissipation consists of two components. One is the switching power due to charging and discharging of load capacitance. The other is short circuit power due to the nonzero rise and fall time of input waveforms. The static power of a CMOS circuit is determined by the leakage at the circuit level,

A. Existing Approaches:(Sleep Transistor Approach)

In previous MTCMOS approach, sleep and sleep bar transistors of high threshold voltages are inserted in series between the circuit and. V_{DD} and ground due to this high threshold voltage the additional delay will add to the main circuit so in

sleep transistor approach we use same threshold voltage to sleep transistors When sleep input is OFF and sleep bar input is ON, there is no current flow in the low threshold voltage main circuit. When sleep is ON and sleep bar is OFF then the circuit works in normal mode, the sleep transistor technique dramatically reduces leakage power during sleep mode. , the additional sleep transistors increase area and delay but it is low compare to MTCMOS.

B. Sleepy Stack Approach:

The sleepy stack approach uses sleep transistor and the stacked transistor in each network are made parallel. Here the width of the sleep transistors is reduced. . The activity of the sleep transistors in sleepy stack is same as the activity of the sleep transistors in the sleep transistor technique. The sleep transistors are turned on during active mode and turned off during sleep mode. . The high V_{th} transistors are used for the sleep transistor and the transistors parallel to the sleep transistor without incurring large delay increase. The delay time is increase sing here but it gives low leakage. During sleep mode both the sleep transistors are turned off. But the sleepy stack structure maintains exact logic state.

C. Dual Sleep Approach:

In dual sleep method two sleep transistors in each NMOS or PMOS block are used. One sleep transistor is used to turn on in ON state and the other one is used to turn on in OFF state. . Dual sleep approach uses the advantage of using the two extra pull-up and two extra pull- down transistors in sleep mode either in OFF state or in ON state. It uses two pull-up sleep transistors and two pull-down sleep transistors. When S=1 the pull down NMOS transistor is ON and the pull-up PMOS transistor is ON since S‟=0. So the arrangement works as a normal device in ON state. During OFF state S is forced to 0 and hence the pull down NMOS transistor is OFF and PMOS transistor is ON and the pull-up PMOS transistor is OFF while NMOS transistor is ON. So in OFF state a PMOS is in series with an NMOS both in pull-up and pull-down circuits which is liable to reduce power.

D. Dual Stacked Sleep Approach:

This technique uses two stacked sleep transistor in Vdd and two stacked sleep transistor in ground. So, leakage reduction in this technique occurs in two ways. First, the stack effect of sleep transistors and second, the sleep transistor effect. It is well known that pmos transistors are not efficient at passing GND; similarly, it is well known that nmos transistors are not efficient at passing Vdd. But this stacked sleep technique uses pmos transistor in GND and nmos transistor in Vdd for maintaining the exact logic state during sleep mode The extra two transistors of the design for maintaining the logic state during sleep mode.

E. Advance Approaches:

1. Sleepy Keeper Approach:

The sleepy keeper circuit maintains output value of „1‟ and an NMOS transistor continue this value during sleep mode. An additional NMOS transistor is added in parallel to the pull up sleep transistor connected to Vdd. In sleep mode this NMOS transistor is the only source of Vdd to the pull-up network since the sleep transistor is off. Similarly, to maintain a „0‟ value, The sleepy keeper approach maintain output value of „0‟ and a PMOS transistor maintains the value during sleep mode .An additional PMOS transistor is added in parallel to the pull down sleep transistor connected to GND. At sleep mode this PMOS transistor is only source of GND the pull down network since the sleep transistor is off. The draw backs of sleepy keeper is that it consumes 31% more dynamic power than the sleepy stack.

2. *Forced Sleepy Approach:*

The forced sleep method has a structure merging the forced stack technique and the sleep transistor technique, uses W/L = 3 for the pmos transistors and W/L = 1.5 for the nmos transistors, ld use W/L = 6 for the pull-up transistor and W/L = 3 for the pull-down transistor (assuming $\mu n = 2\mu p$). Then sleep transistors are added in series to each set of two stacked transistors. We use two sleep transistors here, the nmos sleep transistor with Vdd and the pmos sleep transistor with ground. Conventionally the nmos transistor is connected to ground because it is very efficient passing ground voltage and the pmos transistor is connected to Vdd because it is efficient passing Vdd In forced sleep method we just reverse the connection. That‟s why we have some delay penalty in our method. We use same W/L for all the pmos and nmos transistors.

IV. EXPERIMENT SET UP AND RESULTS

This paper aims at analyzing the performance of different architectures of DFF with respect to performance metrics such as power, area , delay and Power Delay Product(PDP). Four D flip flop architectures with True Single Phase Clocking(TSPC) has been considered with 12, 8 and 5 transistors Figures 1,2,3,4) respectively and observe the simulated results and for low area, design the DFF which has low power dissipation, at nano meter technology 90nm,70nm,50nm and apply the different leakage power reduction techniques and comparison of the above performance metrics .for different leakage reduction techniques is carried out ,the Simulation results of average 20ns are observed. Since all the parameters are derived using Berkley Short Channel Insulated Gate FET simulation model, the simulated results are expected to be very close to actual results.

From the results, it is observed from Table (1) that the proposed 5T-TSPC circuit produceslow power dissipation(4.23uw), compare to other 12,8,5 transistor D flip flop andin

nano meter technology when leakage reduction techniques were applied on this type of D flip flop the Sleepy transistor technique produces best result of pavg (30%) power reduction when compared to base case, and sleep transistor Technique reports(99.9%)reduction of the leakage power and Power Delay Product is also minimum for sleepy transistor technique.

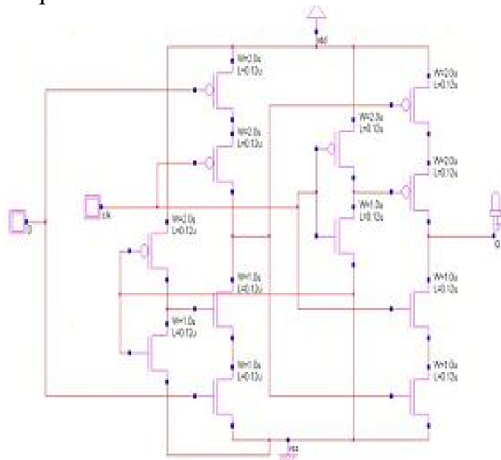

Fig. 1: Shows the Model Diagram of 12t DFF

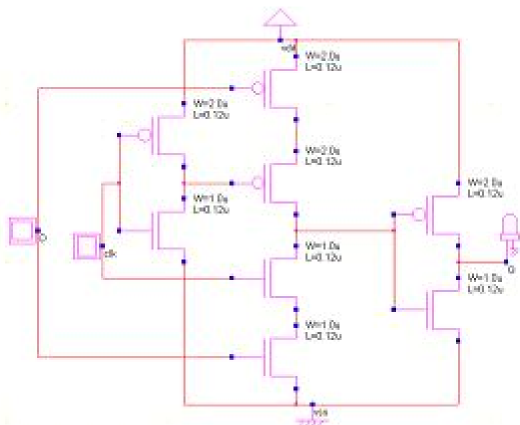

Fig. 2: Shows the Model Diagram of 8t DFF

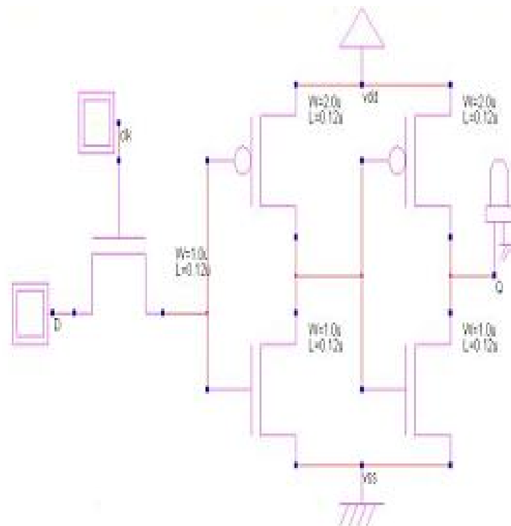

Fig. 3: Shows the Model Diagram of 5tConventional DFF

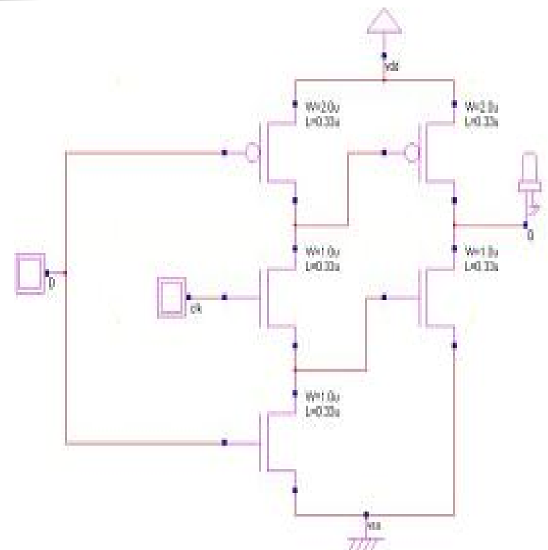

Fig.4: Shows the Model Diagram of 5t proposed DFF

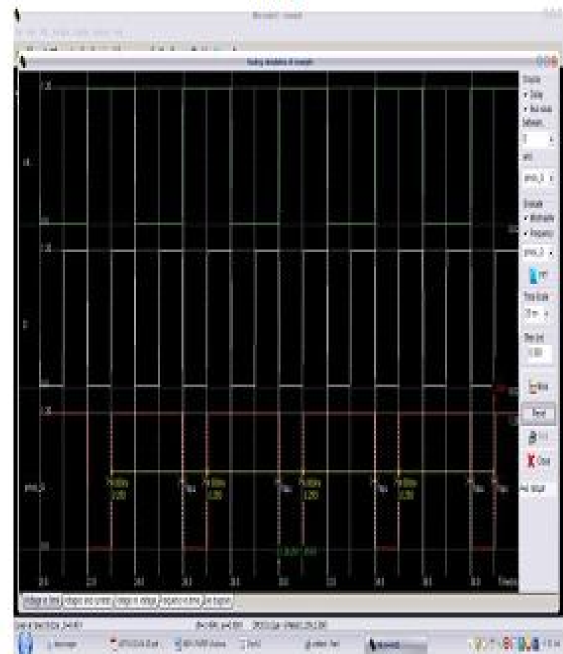

Fig. 5: Shows the Simulated wave form1 of 12tDFF

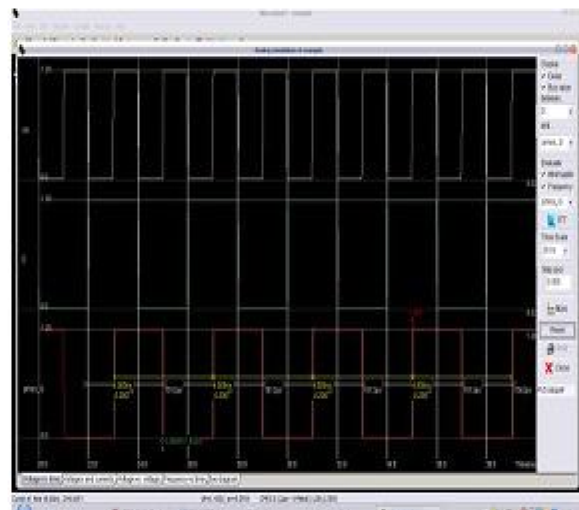

Fig.6: Shows the Simulated wave form2 of 8t DFF

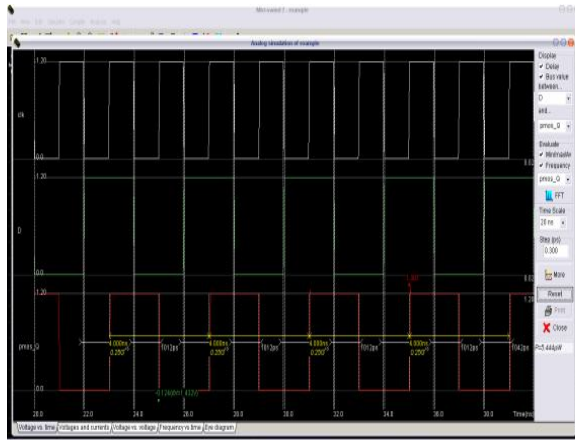
Fig. 7: Shows the Simulated wave form3 of 5t DFF

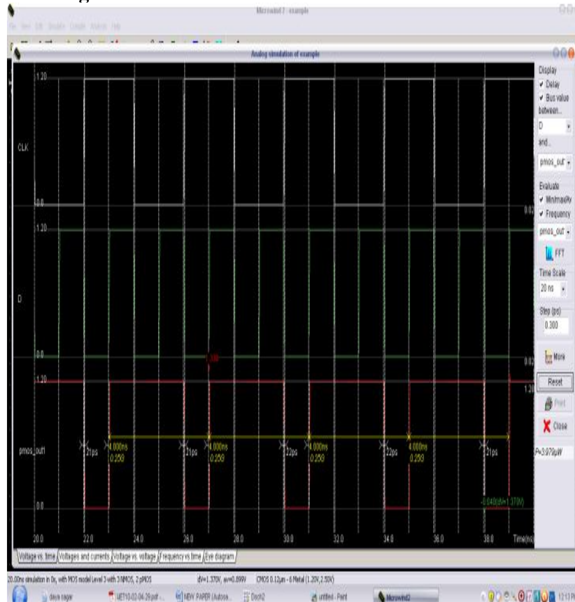
Fig.8: Shows simulated wave form 4 of proposed 5t DFF

From table (2) observe that sleepy keeper and forced sleep techniques also reports the better power reduction From the results, it is observed that, proposed 5T-TSPC D- flip flop architecture has the better percentage of average power reduction for 3 cases (ST(30%), FTS (28%)and SK(23%)) and also in the case of leakage power reduction, 5T-DFF has better results for 3 techniques.

V. CONCLUSION

In this Paper performance analyses of different D-Flip-flop Circuits are presented. proposed 5t DFF has low power consumption compare to all other DFF, the Efficiency of Power reduction varies with different topology with different leakage reduction technique. Best average power reduction p_{avg} (30%) and p_{leak}(99.90%) is reported with sleep transistor technique, due to its power gating ability. Lowest Power (0.301uw)) is reported ,and sleepy keeper and forced sleep also gives better results.
the election of leakage power reduction technique is depends upon topology and designing technology of DFF

TABLE 1
Performance analysis of different D flip flop Architectures

CIRCUIT TYPE	POWER (uw)	DELAY (ns)	PDP (fj)	AREA (um)
12t DFF	9.909	1.000	9.909	336
8t DFF	6.709	0.047	0.307	228
Con. DFF	5.329	0.053	0.291	144
Pro. DFF	4.230	0.055	0.230	132

TABLE 2
Performance Analsys of Different Leakage Reduction Techniques on 5tDFF at 50nm Technology

circuit	Power(uw)	Delay(ns)	pdp(fj)	Area(um)
base case	0.418	0.052	0.021	40
sleep transistor	0.301	4.028	1.513	60
sleepy stcack	0.420	1.028	0.438	72
dual sleep	0.375	1.425	0.605	72
dual stack	0.378	1.029	1.019	105
sleepy keeper	0.322	4.017	1.293	72
forced sleep	0.304	4.018	1.221	84

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