International Journal of Power System Operation and Energy Management

Volume 1 | Issue 4 Article 1

October 2012

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Recommended Citation

Chaudhari, Madhuri Avinash (2012) "Implementation of Digital Signal Processor to Control Three-Phase Voltage-Source Inverter," *International Journal of Power System Operation and Energy Management*: Vol. 1 : Iss. 4 , Article 1.
DOI: 10.47893/IJPSOEM.2012.1037
Available at: https://www.interscience.in/ijpsoem/vol1/iss4/1

Implementation of Digital Signal Processor to Control Three-Phase Voltage-Source Inverter

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Abstract **-** This paper explores the advantages and implementation of Digital Signal Processing (DSP) *TMS* 320*F*2812 to generate gate pulses. The main features of this DSP are elaborated. The technique to obtain gate pulses in different pulse width modulation methods in order to control three-phase voltage source inverter is explained systematically. The steps needed to develop the program are highlighted in detail to control frequency and the duty cycle of PWM waveform. Further Fabrication of gate driver circuit is presented. Experimental results of three-phase voltage source inverter controlling ac drive in variable voltage-variable frequency mode are also given.

Key words **-** *DSP; gate pulse; PWM; duty cycle; ac drive.*

I. INTRODUCTION

Pulse Width Modulated (PWM) converters are used to overcome the problem of low order harmonics associated with input line current rectifier circuit. PWM converter shift the frequency of the dominant harmonics to a higher value so that, these harmonics can be eliminated by employing a small passive filter [1]. Furthermore, the PWM rectifier can markedly cut down the devices' bulk and weight, and get dynamic response faster remarkably [2]. The PWM converters can be operated in variable frequency mode and duty ratio control mode. The analog circuits used for variable frequency control consists of voltage-controlled oscillator, logic circuits, dead-band circuits, frequency limiter circuit and overload protection circuits [3]. The analog control systems can experience performance degradation due to aging, component tolerances and drift. They lack in the flexibility to adoption of different control strategies and precision adjustment of the equal dead-bands is difficult. Hence, digital circuit is built. The digital control using a digital signal processor (DSP) provides precision and improvement in the system performance. The DSP controller offers reliability, programmability and the flexibility to adapt to the different control strategies with the same hardware. Moreover, the high-speed central processing unit allows the designer to process the control algorithms in real time. Owing to these reasons the digital control of the three-phase voltage source converter to control output three-phase ac voltage is realized using a digital signal processor *TMS* 320*F*2812. A three-phase voltage source converter feeding three-phase inverter is shown in Fig. 1. View of DSP is shown in Fig. 2. In this paper the algorithm development methodology to build DSP program to control the output voltage is explored. In addition to this control circuit, the high performance gate drive circuit using MOSFETs for driving the IGBTs in the three-phase HF inverter is elaborated. The experimental results three-phase VSI are also discussed.

II. PWM CONTROL USING DIGITAL TECHNIQUE

The analog control systems have drawbacks of performance degradation due to aging, component tolerances and drift. The equal and precise adjustment of dead-bands in the gate signals of the two IGBTs on the same leg was difficult. Hence, Digital signal processor (DSP) has been used to generate switching signals for inverter. Salient features of DSP *TMS* 320*F*2812 [4] are as follows,

- 150 MHz operating frequency.
- 18 K words on chip RAM.
- 128 K words on chip Flash memory.
- Using C2000 tools code composer studio code can be developed in assembly language, C or C++.
- Two Event Managers.
- 12 bit ADC module with 16 channels.
- Up to 56 general purpose input output pins.

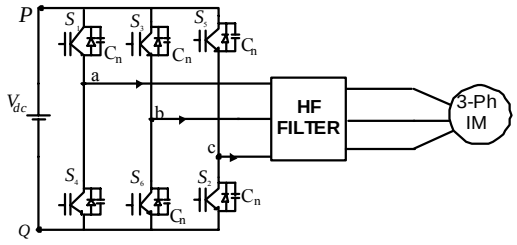


Fig. 1 : Three-phase Voltage Source Inverter feeding three-phase Induction Motor.

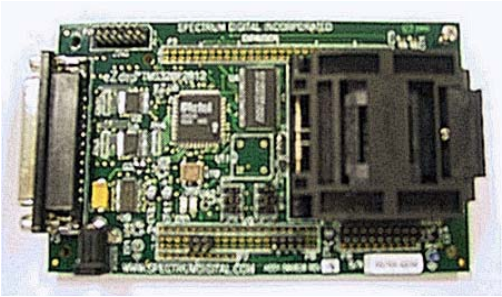


Fig. 2 : View of DSP TMS 320F2812.

The event manager (EV) modules provide a broad range of functions and features that are particularly useful in power electronics converters and motor control applications. The event-manager modules include general-purpose (GP) timers, full compare/ PWM units, capture units, and quadrature-encoder pulse (QEP) circuits. The two EV modules, EVA and EVB, are identical peripherals, intended for multi-axis/motion-control applications. The pulse-width modulation (PWM) circuits associated with compare units make it possible to generate six PWM output channels (per EV) with programmable dead-band and with desired output polarity.

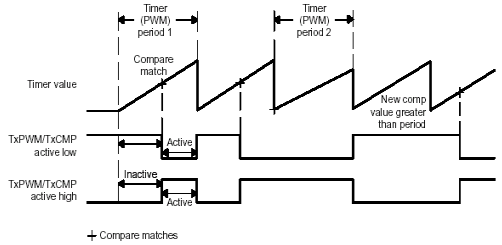
A. PWM circuits associated with compare units

This includes the following functional units:

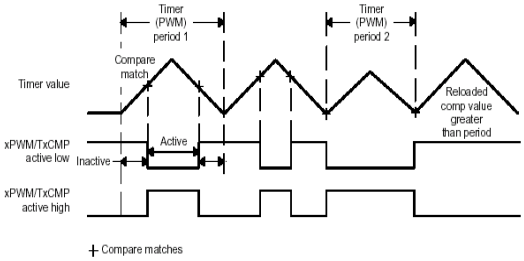
- Asymmetric/Symmetric Waveform Generators
- Programmable Dead-Band Unit (DBU)
- Output Logic
- Space Vector (SV) PWM State Machine

PWM generation with compare units and associated PWM circuits are controlled by the following control registers: T1CON (Timer 1 control register), COMCONA (Compare control register), ACTRA (action control register), and DBTCONA (dead-band control register) in case of EVA; and T3CON, COMCONB, ACTRB, and DBTCONB in case of EVB. The PWM circuits are designed to minimize CPU overhead and user intervention when generating pulse width modulated waveforms used in motor control and motion control applications.

The bits in the control register COMCONX determine the operation mode of the compare units. The value of the GP timer 1 counter is continuously compared with that of the compare register. When a match is made, a transition appears on the two outputs of the compare unit according to the bits in the action control register ACTR. The bits in ACTR can individually specify each output to be toggle active high or toggle active low on a compare match. An asymmetric and symmetric waveform generator and the associated output logic decide the transition on the PWM output. The asymmetric/symmetric waveform generator generates an asymmetric or symmetric PWM waveform based on the counting mode of the GP timer. An asymmetric waveforms are shown in Fig. 3(a). This wave form is generated virtually when the GP timer is in continuous up-counting mode. When the GP timer is in this mode,



(a)



(b)

Fig. 3 (a) A symmetric waveform

(b) An asymmetric waveform

the output of the waveform generator changes according to the following sequence:

(i) Zero before the counting operation starts.

(ii) Remains unchanged until the compare match happens.

(iii) Toggles on compare match.

(iv) Remains unchanged until the end of the period.

(v) Resets to zero at the end of a period on period match, if the new compare value for the following period is not zero.

One characteristic of asymmetric PWM waveforms is that a change in the value of the compare register only affects one side of the PWM pulse.

A symmetric waveform (Fig. 3(b)) is generated when the GP timer is in continuous up/down-counting modes. When the GP timer is in this mode, the state of the output of the waveform generator is determined by the following:

(i) Zero before the counting operation starts.

(ii) Remains unchanged until first compare match.

(iii) Toggles on the first compare match.

(iv) Remains unchanged until the second compare match.

(v) Toggles on the second compare match.

(vi) Remains unchanged until the end of the period.

B. Programmable dead-band unit

The dead-band unit is designed to prevent an overlap under any operating situation between the turn-on period of the upper and lower devices controlled by the two PWM outputs associated with each compare unit. The turn-on periods of the two devices must not overlap with each other in order to avoid a shoot-through fault [5, 6]. Thus, a pair of non-overlapping PWM outputs is often required to properly turn on and off the two devices. A dead-time (dead-band) is often inserted between the turning-off of one switching device and the turning-on of the other switching device. This delay allows complete turning-off of one switching device before the turning-on of the other switching device. The event manager has a programmable dead-band unit for inserting such dead-times. The operation of the dead-band unit is controlled by the dead-band timer control register (DBTCON). Minimum dead-band duration of one device can be equal to a clock cycle of event manager and it should not be less than a clock cycle of event manager.

C. Algorithm for PWM waveform generation

Steps for PWM generation are: To set up the GP timer for the PWM operation, the following steps need to be done:

1. Pre-scaling of system clock frequency for this DSP can be done by putting proper count in registers PCLKCR (Peripheral Clock Control Register), PLLCR (PLL control register), HISPCP (High Speed peripheral clock Pre-scaler).
2. The DSP *TMS* 320*F*2812 has 56 general purpose input-output pins. These pins can be set in peripheral modes. This is done by using registers GPxMUX (general purpose mux control register), GAxDIR (general purpose direction control register). In order to use PWM circuit associated with compare register the port pins have be set in peripheral modes. GPIO The general purpose Data Register GPxDAT is set to pull the pin high or low.
3. Set up Timer period register (TxPR) which is 16 bit register, as per the count required PWM switching period.
4. Set up timer control register (TxCON) to specify the counting mode and clock source, and start the operation. This register can also be used for pre-scaling of clock frequency.
5. The count in Compare Register (CMPRx) is set to achieve the required duty cycle. This is shown in Fig 3. For sinusoidal PWM (SPWM) of three-phase inverter the three compare registers are loaded with the counts obtained by using sinusoidal function. The outputs of the output Logic for the compare units which are: PWMx, x = 1−6 (for EVA) and PWMy, y = 7−12 (for EVB) go high and low corresponding to that sinusoidally varying count period.
6. GPTCONx: General Purpose Timer Control Register is used to control polarity of timer compare output.
7. The compare action control registers (ACTRA and ACTRB) control the action that takes place on each of the six compare output pins (PWMx, where x = 1−6 for ACTRA, and x = 7−12 for ACTRB) on a compare event, if the compare operation is enabled by setting 15th bit of COMCON register. ACTRA and ACTRB are double buffered. The condition on which ACTRA and ACTRB is reloaded is defined by bits in COMCON register.

The frequency of the output signals shown in Fig. 3 depends on the carrier frequency. This in turn depends on the content of the period register T1PR. The pulse widths of these signals depend on the compare match points, which are decided by the contents of the three compare registers. A software program is developed in code composer studio of the DSP. Fig. 4 shows example of generation of gate pulses required to operate three-phase inverter in square wave mode. Since no clock pre-scalers are used in the DSP controller, the CPU and all the peripherals operate on 150 MHz clock. To generate the gating signals for the three-phase HF inverter operating at 300 kHz on full load condition, a carrier signal of (3*300 kHz) 900 kHz is generated. To generate this carrier signal the content of T1PR is set to ratio of clock frequency to the carrier frequency i. e. at 167 decimal. The counter is set in the continuous up counting mode. This makes the counter to reset and

restart the counting after the end of every period interval i.e. after every 167-clock cycles. A set of three signals displaced by 120^0 from each other is generated on PWM pins 1-3 by properly adjusting the contents of the three compare registers for each period interval. This is shown in Fig. 4.5. The PWM outputs 1, 2 and 3 are set to active low. The other three signals, generated on the PWM output pins 4-6, are inverted to those on the PWM pins 1-3. This is done by setting these outputs to active high using ACTR (0-11) bits. Setting an output to active low means that the output will be high until the corresponding compare match is found. On the compare match the output toggles to low and remains low until the beginning of the next period interval. The output 1 is required to be high for the period interval 0^0 to 180^0, whereas the outputs 2 and 3 are required to be high for the period intervals 120^0 to 300^0 and 240^0 to 60^0 respectively. The OUTPUTx (x = 1, 2 or 3) remains in the high state through-out the period interval if the content of the register CMPRx (x = 1, 2 or 3) is greater than the content of period register (i.e. if no compare match is found during the period interval). The output remains in the low state if the content of CMPRx is zero (i.e. if the compare match is found at the beginning of the period interval). The contents of the three compare registers for the three period intervals are also shown in the Fig. 4. It is seen that these contents are required to be updated for every period interval. Since the three compare registers are shadowed (double buffered), the contents required for the next period interval are loaded in the shadow registers in the current period interval. As soon as the period register resets, these contents are transferred automatically to the actual CMPRx registers.

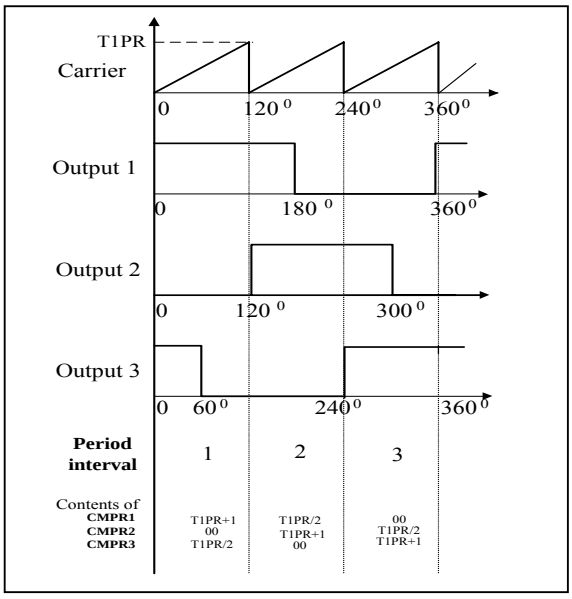


Fig.4 : Generation of PWM gating signals for three-phase inverter.

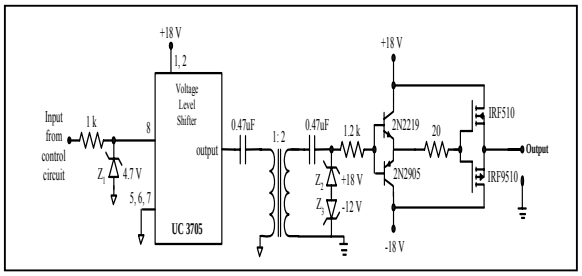


Fig. 5 : Bipolar Gate driver circuit

The above logic is extended to generate gate pulses for three-phase voltage source inverter to drive ac motor in variable voltage-variable frequency control mode.

III. BIPOLAR GATE DRIVER CIRCUIT

The SPWM switching signals are generated by using DSP TMS320F2812. The carrier frequency for the SPWM of the VSI is $f_s = 33\,kHz$ and reference frequency is 50 Hz. To avoid false triggering of the IGBTs during their off state, high performance bipolar gate driving circuits are needed. Such a bipolar high performance gate driver circuit is fabricated that uses the ultra-high speed MOSFETs *IRF* 510 and *IRF* 9510. This is shown in Fig. 5.

The voltage level of the gating control signals generated by a DSP (3.3 V) is increased to 18 V using an integrated circuit UC3705. The isolation is provided using a pulse transformer. To avoid the core saturation in the pulse transformer, the capacitive coupling is used in the primary circuit. A controlled dc restoration circuit using a capacitor and two back-to-back connected zener diodes is used in the secondary circuit. An intermediate totem pole bipolar transistorized circuit drives the ultra-high speed MOSFETs *IRF* 510 and *IRF* 9510. These in turn drive the main IGBTs of the three-phase HF inverter of the proposed converter circuits.

IV. EXPERIMENTAL RESULTS

An experimental prototype is built in the laboratory to control ac drive using DSP (TMS320F2812). . The three-phase VSI is built using IGBTs $HGTG\ 20N60A4D$. The sinusoidal PWM (SPWM) voltage sourced inverter is used to drive Induction Motor of 4 pole, 5 hp, 1435 rpm, 400 V, 50Hz. To reduce HF ripple, a HF filter is connected in the IM input. Fig. 6 shows the performance of the converter when it is controlled in square wave operation by DSP. Fig. 6(a) presents output phase voltages and phase currents of the three-phase voltage source converter (VSI). Three-phase line voltages are shown in Fig. 6(b). To show that proposed scheme works for various output speed of IM, it is operated in constant torque region with variable speed. To obtain various output speeds of

operation v/f control method is used. The three-phase IM speed is controlled by varying reference frequency and modulation index in SPWM gate control scheme of VSI. The SPWM switching signals are generated by using DSP (TMS320F2812). The carrier frequency for the SPWM of the VSI is $f_s = 33\,kHz$. To control IM in v/f mode carrier frequency is kept constant and reference frequency is varied. Fig. 7 shows the performance of the converter under v/f control.

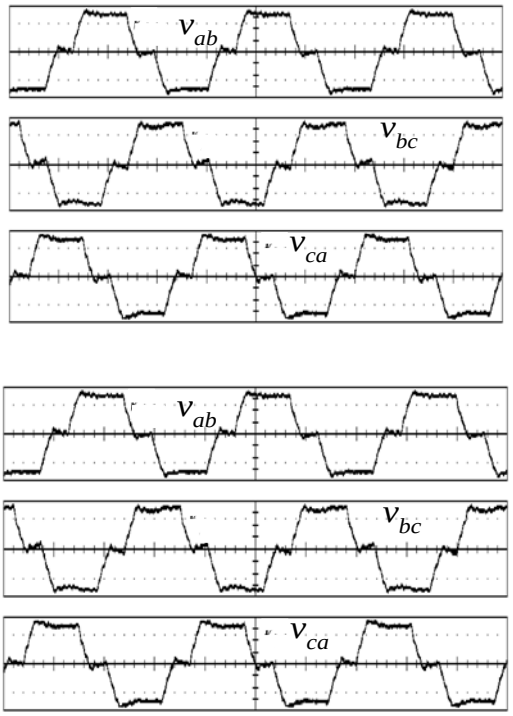
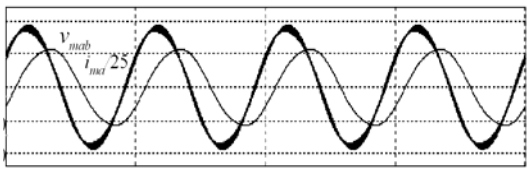
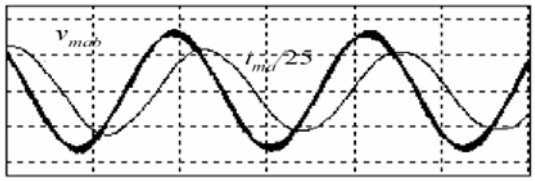


Fig. 6 : Waveforms of Three-phase voltage source inverter (a) output phase voltages and phase currents (b) Output line voltages Scales: time 1μS/div., voltage 100 V/div., current 10 A/div.

Fig. 7(a) shows input voltage and input current of 'a' phase of induction motor at 1435 rpm. The input line voltage and stator current of IM running at 1285 rpm (45 Hz) and 1135 rpm (40 Hz) are shown in Fig. 7(b) and 7(c). Table I shows the performance of the converter for ac drive in variable frequency-variable voltage control mode.



(a)



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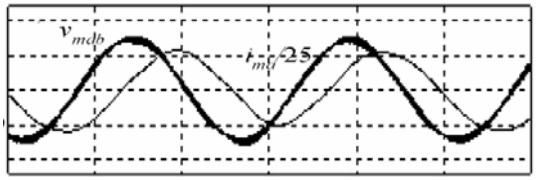

(c)

Fig. 7 : Induction motor input line voltage (v_{mab}) and phase current (i_{ma}) (a) while running at 1435 rpm. Scale: X axis: 20 ms/ div., Y axis: 200 V/ div. (b) while running at 1285 rpm. Scale: X axis: 10 ms/ div., Y axis: 200 V/ div. (c) while running at 1135 rpm. Scale: X axis: 10 ms/ div., Y axis: 200 V/ div.

Table 1 Performance of converter

v_{ab} of VSI (V)	Freq. (Hz)	Speed (rpm)
400	50	1435
360	45	1285
320	40	1135

V. CONCLUSION

In this paper the digital control circuit used to control three-phase voltage-source converter is presented. The PWM waveform generation using DSP *TMS* 320*F*2812 is discussed step-by-step. The algorithm to develop DSP program is discussed in simplified way. The variable frequency control strategy under 180^0 wide gate control (square wave operation) is explained using an example. The control circuit is also used to operate ac drive in variable voltage-variable frequency mode. Finally a high performance, bipolar gate driver scheme using ultra-high speed MOSFETs *IRF* 510 and *IRF* 9510 is given. The experimental results on the laboratory prototype of the three-phase VSI controlling three-phase induction motor are also presented. The digital techniques are flexible to adopt different control strategies and do not sacrifice the precision as well as system performance.

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