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Abstract- In this paper a low-power current-mode RMS-to-DC converter is proposed. The converter includes two-quadrant squarer/divider and the first-order low-pass filter cell, both of them use MOS translinear loops. The RMS-to-DC converter has low power consumption (< 0.75µW), low supply voltage (0.8 V), wide input range (from 40 nA to 500 nA), low relative error (< 3 %), and low circuit complexity. Comparing the proposed circuit with two other current-mode circuits shows that the former outperforms the latters in terms of power dissipation, supply voltage, and complexity. Simulation results by HSPICE show high performance of the circuit and confirm the validity of the proposed design technique.

Keywords- *current-mode; squarer/divider; RMS-to-DC converter, weak inversion; low power; low voltage.*

I. INTRODUCTION

True RMS-to-DC converter is a circuit for calculating of the average energy content in a signal. The converter is widely used in instrumentation devices, biomedical ICs, and syllabic companding systems. The two approaches exist for designing RMS-to-DC converter: 1) current-mode approach, 2) voltage-mode approach. A current-mode circuit enables current processing and has certain important advantages against a voltage-mode circuit, such as, wide bandwidth, high slew rate, low power consumption, and simple circuitry [1,2]. A squarer cell is the most important component of a current-mode RMS-to-DC converter. The input range of two-quadrant squarer is wider than a one-quadrant one's [2]. The principle of MOS translinear loops (MTL) are expressed by Seevinck and Wiegerink for the first time [3]. MTL principle used in analyzing and evaluating analog signal processing functions [4]. CMOS current-mode circuits has been developed because of the increasing demand for low-voltage/low-power integrated circuits.

In this paper, a current-mode RMS-to-DC converter which has low-power consumption and two-quadrant squarer with MOS transistors operating in weak inversion region is presented. The proposed RMS-to-DC converter has less power consumption and simpler circuitry than the one's of voltage-mode converters because of the special characteristics of current-mode and circuitry structure. The two-quadrant squarer cell causes wide input range. There is no additional power supply. Combining all these techniques allows circuitry reduction compared to the proposed circuits in [5,6], results in a simple and compact design, and lowers power dissipation and consumption area. The simulation results indicate that the circuit achieves lower power and lower voltage compared to the proposal current-mode circuits in [5,6]. The remaining of the paper is organized as follows; Basic principle is explained in section 2 for the better conception of the proposed RMS-to-DC converter, section 3 analyses operation of the squarer circuit and the low-pass filter. The simulation results are presented and compared with the ones' of two other current-mode converters in section 4. The paper is concluded in section 5.

II. BASIC PRINCIPLE

One of the most notable instances of nonlinear dynamic operation from a practical viewpoint is the RMS-to-DC conversion. In its basic form, and assuming input and output currents, such operation can be described by the equation :

$$I_{out} = \sqrt{\langle I_{in}^2 \rangle} \qquad (1)$$

Where I_{in} and I_{out} are the input and output currents of the RMS-to-DC converter, respectively, and the operator $\langle ... \rangle$ represents a time averaging. A (mathematically equivalent) approach, better in terms of offset [7], is given by

$$I_{out} = \left\langle \frac{I_{in}^2}{I_{out}} \right\rangle \qquad (2)$$

Hence, two operations have to be performed: squaring/division and subsequently, averaging. Fig. 1 shows the block diagram of the current-mode true RMS-to-DC converter which consists these two operations.

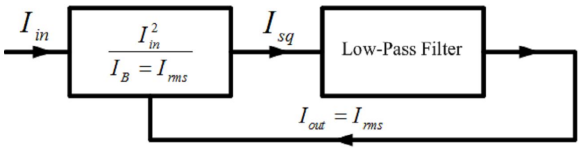

Figure 1. Block diagram of RMS-to-DC converter

III. PRINCIPLE OPERATION OF THE PROPOSED RMS-TO-DC CONVERTER

The ratio of V/I for MOSFETs transistors operating in weak inversion region can be obtained from equation (3) [8]:

$$V_{GS} = \xi\ V_T\ \ln\left(\frac{I}{(W/L).I_{0n,p}}\right) \qquad (2)$$

Where $I_0 = I_S e\wedge(V_{th-n,p}/\xi V_T)$, $V_T = kT/q$, $\xi > 1$ and $I_S = 2\xi\ \mu_{n,p}\ C_{ox}(V_T\wedge 2)$. Except for ξ , equation (3) is similar to the exponential I_C/V_{BE} relationship in a bipolar transistor. Principle of operation for squarer circuit is based on translinear loops. The translinear cell which uses two NMOS and two PMOS transistors with inward input is shown in Figure 2. I_{in} the input current which enters into sources of M2 and M4 (node x). Considering Figure 2, M1-M4 form a translinear loop. The relationship between these four transistors can be described as [3]:

$$\sum_{CW} V_{GS} = \sum_{CCW} V_{GS} \rightarrow$$

$$\xi V_T\ \ln\left(\frac{I_1}{\left(\frac{W}{L}\right)_1 I_{0n}}\right) + \xi V_T\ \ln\left(\frac{I_3}{\left(\frac{W}{L}\right)_3 I_{0p}}\right) =$$

$$\xi V_T\ \ln\left(\frac{I_2}{\left(\frac{W}{L}\right)_2 I_{0n}}\right) + \xi V_T\ \ln\left(\frac{I_4}{\left(\frac{W}{L}\right)_4 I_{0p}}\right) \qquad (4)$$

$$\frac{I_1}{\left(\frac{W}{L}\right)_1 I_{0n}}\ \ \frac{I_3}{\left(\frac{W}{L}\right)_3 I_{0p}} =$$

$$\frac{I_2}{\left(\frac{W}{L}\right)_2 I_{0n}}\ \ \frac{I_4}{\left(\frac{W}{L}\right)_4 I_{0p}} \qquad (5)$$

According to equation (5) and Figure 2, the advantage of the translinear loop is that there are I_{0p} and I_{0n} in both side of the equation. Therefore, they can be eliminated. Considering $(W/L)_1 = (W/L)_2$ and $(W/L)_3 = (W/L)_4$, The final equation for this translinear loop is shown below:

$$I_1\ I_3 = I_2\ I_4 \qquad (6)$$

The analysis of Figure 2 indicates $I_1 = I_3 = I_B$ and $I_4 = I_{in} + I_2$. Thus, equation (6) can be written as:

$$I_2^2 + I_{in}.I_2 - I_B^2 = 0 \qquad (7)$$

I_2 is obtained by solving quadratic equation (7):

$$I_2 = -(1/2)I_{in} + (1/2)(I_{in}^2 + 4I_B^2)^{0.5} \qquad (8)$$

Using power series of equation (9)

$$(1+x)^a = 1 + \sum_{n=1}^{\infty} C_n^a x^n, -1 < x < 1,$$

$$C_n^a = \frac{a(a-1)(a-2)...(a-n+1)}{n!} \qquad (9)$$

and applying it to equation (8),

$$I_2 = -(1/2)I_{in} + I_B + (I_{in}^2/8I_B) \qquad (10)$$

For a good approximation, the value of the input current should be restricted to:

$$-2I_B \le I_{in} \le 2I_B \qquad (11)$$

Figure 3 shows the translinear cell with outward input. Operation of this cell is like the translinear circuit in Figure 2. The final equation for the translinear cell in Figure 3 is shown below :

$$I_5\ I_7 = I_6\ I_8 \qquad (12)$$

The analysis of Figure 3 indicates $I_6 = I_8 = I_B$ and $I_5 = I_{in} + I_7$. Thus, equation (12) can be written as:

$$I_5^2 - I_{in}.I_5 - I_B^2 = 0 \qquad (13)$$

By solving quadratic equation (13):

$$I_5 = +(1/2)I_{in} + (1/2)(I_{in}^2 + 4I_B^2)^{0.5} \qquad (14)$$

Using power series of equation (9) and applying it to equation (14), I_5 is equal to:

$$I_5 = +(1/2)I_{in} + I_B + (I_{in}^2/8I_B) \qquad (15)$$

By summing two currents I_2 and I_5 and also eliminating bias current, the proposed squarer is formed. This is shown in equation (16).

$$I_2 + I_5 = 2I_B + (I_{in}^2/4I_B) \rightarrow$$

$$I_2 + I_5 - 2I_B = I_{in}^2/4I_B = I_{sq} \qquad (16)$$

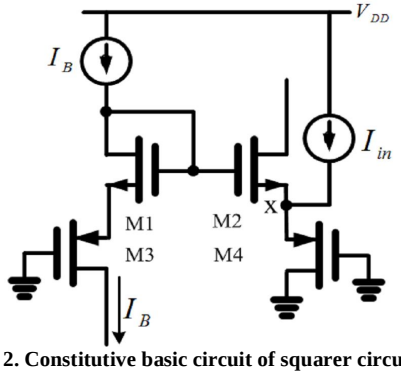

Figure 2. Constitutive basic circuit of squarer circuit with inward input.

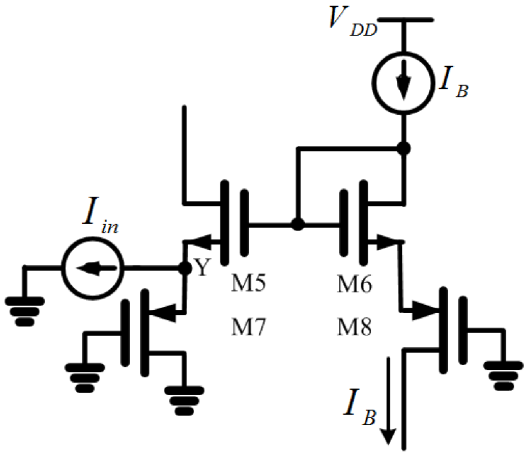

Figure 3. Constitutive basic circuit of squarer circuit with outward input.

The proposed squarer circuit is shown in Figure 4. If the direction of input current changes, I_2 and I_5 are equal to:

$$I_2 = +(1/2)I_{in} + I_B + (I_{in}^2/8I_B) \quad (17)$$

$$I_5 = -(1/2)I_{in} + I_B + (I_{in}^2/8I_B) \quad (18)$$

Again by summing I_2 and I_5 and also eliminating bias current, output current of squarer circuit (I_{sq}) is equal to:

$$I_2 + I_5 = 2I_B + (I_{in}^2/4I_B) \rightarrow$$
$$I_2 + I_5 - 2I_B = I_{in}^2/4I_B = I_{sq} \quad (19)$$

By changing the direction of input current, output current of the squarer circuit doesn't change. It means that the squarer acts as a two-quadrant circuit.

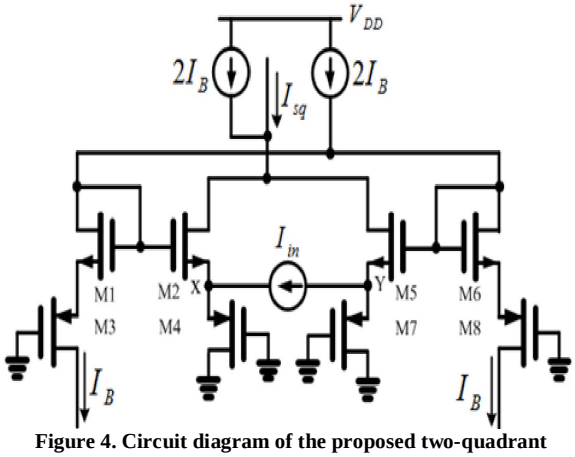

Figure 4. Circuit diagram of the proposed two-quadrant squarer.

For a current-mode first order low-pass filter, output current I_{out} and input current I_{sq} in laplace domain are related as :

$$\frac{I_{out(s)}}{I_{sq(s)}} = \frac{1}{1+\frac{s}{\omega_c}} \rightarrow I_{out(s)} + \frac{s}{\omega_c} I_{out(s)} = I_{sq(s)} \quad (11)$$

Time domain of equation (11) is equal to :

$$\frac{1}{\omega_c}\frac{dI_{out(t)}}{dt} = I_{sq(t)} - I_{out(t)} \quad (12)$$

In which, $\omega_c = 1/\tau$ is the cutoff frequency of filter. Fig. 3 shows the circuit of the proposed low-pass filter. For the I-V relationships of transistor Mf1 in weak inversion region and its derivation can be expressed by:

$$I_{out} = (W/L)I_0 e^{\frac{V_C}{\xi V_T}} \rightarrow \frac{dI_{out}}{dt} = \frac{1}{\xi V_T}(W/L)I_0 e^{\frac{V_C}{\xi V_T}}\frac{dV_C}{dt}$$

$$\rightarrow \frac{dI_{out}}{dt} = \frac{I_{out}}{\xi V_T}\frac{dV_C}{dt} \quad (13)$$

In which, V_{gs} is the voltage of capacitor C ($V_{gs} = V_C$).

Using (13) and also $I_C = C(dV_C/dt)$, it results :

$$\frac{dI_{out}}{dt} = \frac{I_{out}}{\xi V_T}\frac{I_C}{C} \quad (14)$$

And then, substituting (14) into (12) gives :

$$\frac{1}{\omega_c}\frac{I_{out}}{\xi V_T}\frac{I_C}{C} = I_{sq(t)} - I_{out(t)} \quad (15)$$

Considering $I_{C(t)} = I_{sq(t)} - I_{out(t)}$ and equation (15), $(1/C\omega_c)(I_{out}/\xi V_T) = 1$. Therefore, cutoff frequency of the filter is equal to :

$$\omega_C = I_{out}/\xi V_T C \quad (16)$$

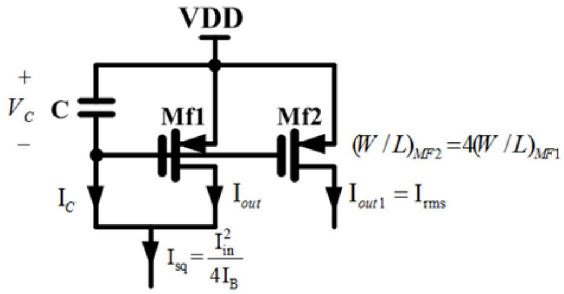

Figure 5. The proposed first-order low-pass filter.

It can be shown that, for the input signal whose frequency is more than five times the cutoff frequency of the filter, output ripple will be less than 1% [9]. In such case, the output current of the RMS-to-DC converter is a DC current (I_{rms}) with an ac

ripple on it. The amplitude of this ripple is small compared to I_{rms} , i.e., $I_{out1} \cong I_{rms}$. Considering these conditions and also using (16) it results that the values of the capacitor to ac9hieve the accuracy of more than 1% is :

$$C \geq \frac{5I_{rms,MAX}}{\xi V_T (2\pi f_{\min})} \qquad (17)$$

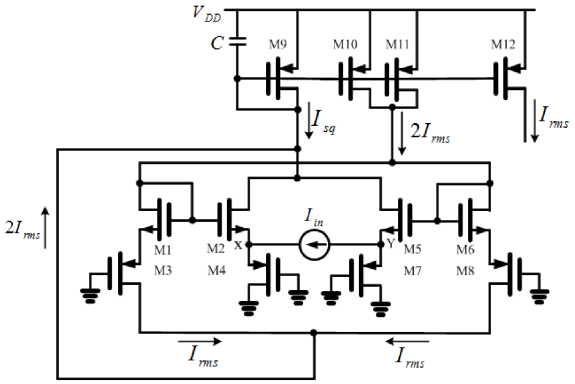

Figure 6. Complete circuit diagram of the proposed RMS-to-DC converter.

Where $f_{\min}$ is the lowest frequency of the interested frequency range. For example, if the amplitude of the sinusoidal input current $I_M = 400nA$, $f_{\min} = 100Hz$ and ripple error of 1%, then the averaging capacitance of $C = 15nF$ must be chosen. Considering equation (17), it's obvious if frequency increases then the capacitance of C decreases. Therefore, the ripple error diminishes by increasing of frequency. Completed circuit of the proposed RMS-to-DC converter is shown in Figure 6.

IV. SIMULATION RESULTS

The performance of the converter has been analyzed using HSPICE by level 49 parameters (BSIM3v3.2) in 0.18 µm standard CMOS technology. $V_{DD} = 0.8$ V and $C = 20$ nF were employed. The aspect ratio of the transistors is shown in Table 1.

TABLE I. SIMULATION RESULTS

	M1-M2,M5-M6	M3-M4,M7-M8	M9	M10-M12
L(µm)	0.5	1	1	1
W(µm)	1	3	1	4

I_{rms} is shown in Figure 7 and Figure 8 for the sinusoidal and triangular input signals with peak amplitude of 200 nA at frequency of 100 Hz. It's important to note that the restriction of Eq. (9) doesn't make problems, the reason is given in equation (27) ($I_{rms} = I_B = 0.7I_{in}$):

$$-2 \times 0.7I_{in} \leq I_{in} \leq 2 \times 0.7I_{in} \qquad (27)$$

The relative error, calculated by equation (28), is depicted for sinusoidal and triangular waveforms in Figure 9 for different amplitudes of input currents. A less than 3% error is achieved for amplitudes between 40 nA and 500 nA.

$$\text{Relative error} = \frac{I_{rms}(theoretical) - I_{rms}(simulated)}{I_{rms}(theoretical)} \qquad (28)$$

Simulation results show that the power consumption of the circuit for the maximum accepted input current (500 nA) is less than 750 nW. The comparison results, shown in Table 2, indicate that the proposed converter has better performance than two other current-mode converters in terms of power dissipation, supply voltage, and complexity.

The comparison results, shown in Table 2, indicate that the proposed converter has better performance than the two other current-mode converters in terms of power dissipation, supply voltage, and complexity.

V. CONCLUSION

In this paper, a very low-power, low-voltage two-quadrant current-mode RMS-to-DC converter based on MOS translinear principles operating in weak inversion region is presented. Simulation results have been given to confirm the validity of the theoretical analysis. According to results, the converter has low power consumption (750 nW), low power supply voltage (0.8 V), and wide input range (40 nA to 500 nA).

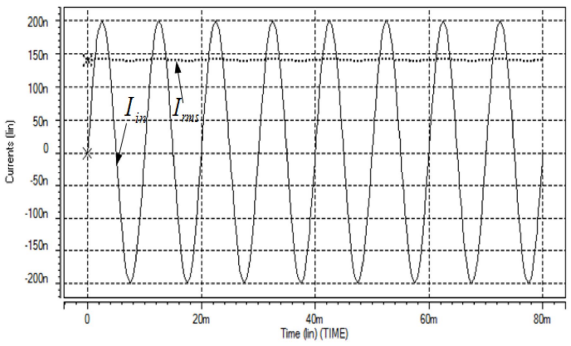

Figure 7. Time response of a sinusoidal input current (solid) and output current (dotted) of converter.

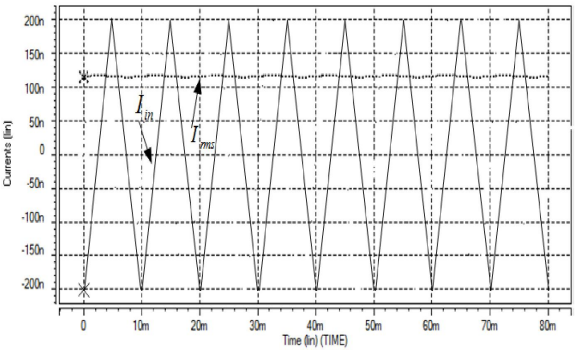

Figure 8. Time response of a triangular input current (solid) and output current (dotted) of the converter.

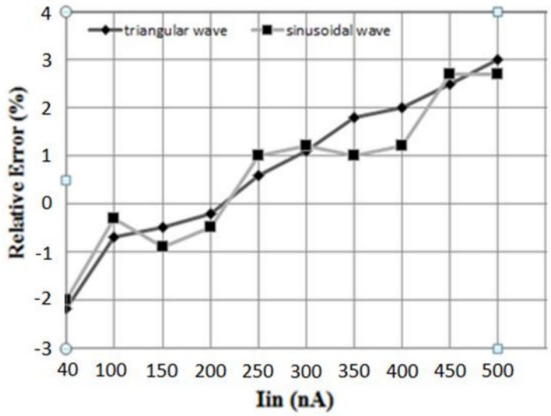

Figure 9. Relative error versus input current of the converter.

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