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EFFECTS OF A BARRIER LAYER IN INGAAS CHANNEL MOSFETS FOR ANALOG/ MIXED SIGNAL SYSTEM-ON-CHIP APPLICATIONS

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Abstract- Addition of a barrier layer in an InGaAs MOSFET, which shows promise for high performance logic applications due to enhanced electron mobility, further improves the electron mobility. We report, for the first time, a detailed investigation of the impact of different barrier layers on the analog performance of an InGaAs MOSFET. The device parameters for analog applications, such as transconductance (g_m), transconductance-to-drive current ratio (g_m/I_{DS}), drain conductance (g_d), intrinsic gain, and unity-gain cutoff frequency (f_T) are studied with the help of a device simulator. A barrier layer is found to improve the analog performance of such a device in general; with a double-barrier layer showing the best performance.

Keywords*-Analog performance, InGaAs n-MOSFETs, transconductance, unity-gain cut-off frequency*

I. INTRODUCTION

In recent years, InGaAs-channel MOSFETs have attracted a lot of interest amongst the researchers for high performance logic applications due to its enhanced electron mobility [1-6]. Recent investigations reveal that the buried-channel InGaAs MOSFETs can achieve much higher effective electron mobility (> 5000 cm^2/V.s) [2] than that in the surface channel devices, in which the effective electron mobility is usually less than 2000 cm^2/V.s.

On the other hand, a barrier-layer reduces the gate control over the channel. As a result, surface-channel devices, as compared with the buried-channel devices, exhibit lower subthreshold swing (SS) and better immunity to short channel effects (SCEs), such as drain-induced barrier lowering (DIBL).

In the past one decade or so, the analog performance of the scaled CMOS devices has also received considerable attention particularly for mixed-signal system-on-chip (SoC) applications where the analog circuits are realized together with the digital circuits and memories in the same integrated circuit in order to reduce the cost and improve the performance.

In this letter, we report, for the first time, an investigation of the impact of different barrier layers on the analog performance of an InGaAs MOSFET.

The analog performance of such a device with a channel length of 40 nm is investigated in terms of transconductance (g_m), output conductance (g_d), intrinsic voltage gain (g_m/g_d),transconductance-to-drain current ratio (g_m/I_{DS}), and the unity-gain cut-off frequency (f_T).

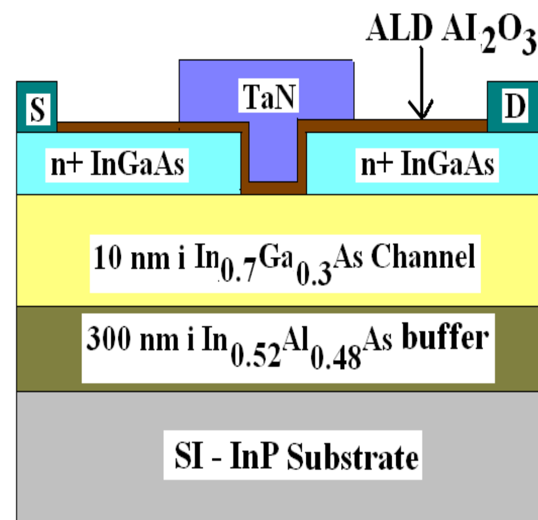

Figure 1 (a) Schematic no barrier device structure of buried InGaAs channel n-MOSFET with L_g= 40 nm.

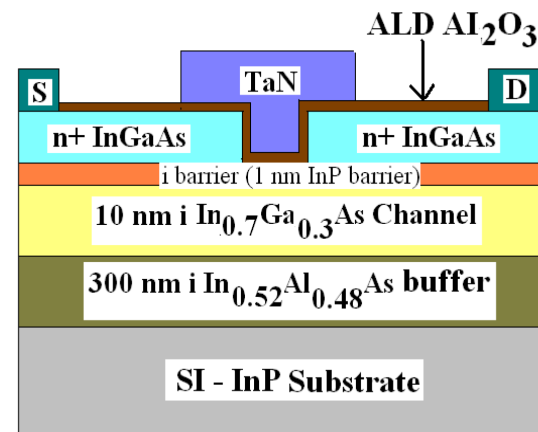

Figure 1 (b) Schematic single barrier device structure of buried InGaAs channel n-MOSFET with L_g= 40 nm

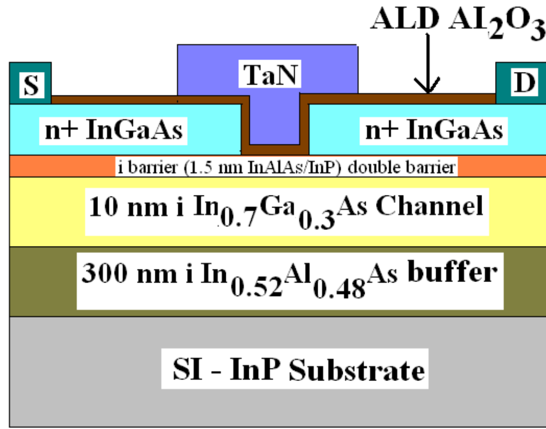

Figure 1(c) Schematic double barrier device structure of buried InGaAs channel n-MOSFET with L_g= 40 nm.

II. DEVICE STRUCTURE AND SIMULATION

The cross sections of different inversion-type enhancement-mode InGaAs channel n-MOSFETs, considered in our study, are shown in Figs. 1(a), (b) and (c). The details of the process flow for fabrication of such a device is reported in [3]. The device structure comprises a 300 nm $In_{0.52}Al_{0.48}As$ buffer layer, a 10 nm quantum well $In_{0.7}Ga_{0.3}As$ and a thin barrier layer. Sample 1 and sample 2 consist of 1 nm InP layer and 1.5-nm- $In_{0.52}Al_{0.48}As$/2-nm-InP double barrier, respectively and a 20 nm $In_{0.53}Ga_{0.47}As$ cap layer. All the layes are undoped except the top $In_{0.53}Ga_{0.47}As$ layer, which is heavily. doped n^+ layer intended for the source/drain (S/D). TaN is used as a gate material and Au is used for formation of ohmic source and drain contacts We have carried out 2D numerical device simulation using SILVACOATLAS [7] to obtain terminal characteristics of buried InGaAs channel inversion type nMOSFETs with three different configurations as depicted in Figs. 1(a), (b) and (c). Since the channel material InGaAs is an alloy, its dielectric constant and bandgap are computed using linear interpolation among the corresponding reported parameters of the constituents that include GaAs and InAs [8, 9]. The intrinsic carrier concentration of 9×10^{11} cm^{-3} for InGaAs [9] has been used in our study. Also the reported values of the dielectric constant and band gap of the barrier materials InP and InAlAs [11] are used in our studies. Earlier experimental findings revealed that the high–k/InGaAs interface contained appreciable amount of D_{it} in the range 1×10^{12} to 4×10^{12} $eV^{-1}cm^{-2}$ [3]. CVT Lombardi model for carrier mobility of InGaAs has been used to model electron mobility in InGaAs channel. The reported experimental results [12] for effective electron mobility at different electric fields are utilized to extract simulation parameters appeared in Lombardi model pertaining InGaAs channel. The interface trap charge density and fixed charge density have been incorporated in the device simulator. Newton and Block numerical techniques are used to obtain solutions of a set of coupled equations – such as continuity equations for electrons and holes, current equations for electrons and holes, etc. – employed in ATLAS.

III. RESULTS AND DISCUSSIONS

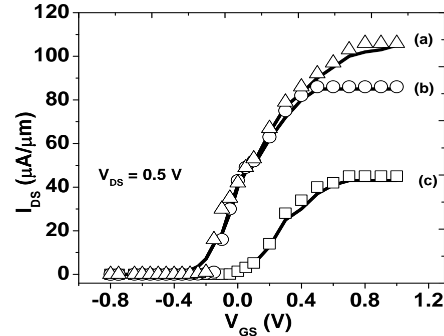

Figure 2. Comparison of transfer characteristics between the experimental (symbols) and the simulation (lines) results for the InGaAs devices with (a) InP/InAlAs double barrier, (b) InP single barrier and (c) no barrier.

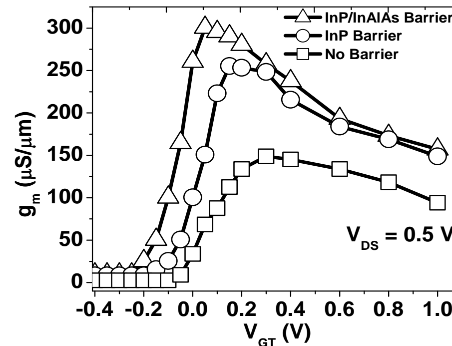

Figure 3. Comparison of g_m as a function of gate overdrive voltage V_{GT} for the three types of InGaAs MOSFETs.

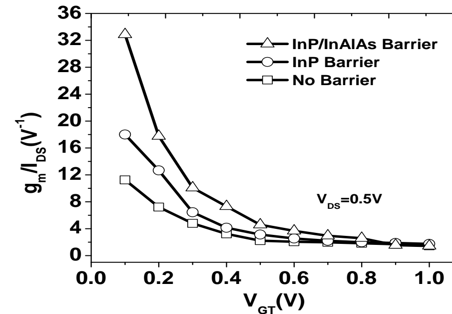

Figure 4. Dependence of g_m/I_{DS} at V_{DS}= 0.5 V as a function of V_{GT} between the three types of InGaAs MOSFETs.

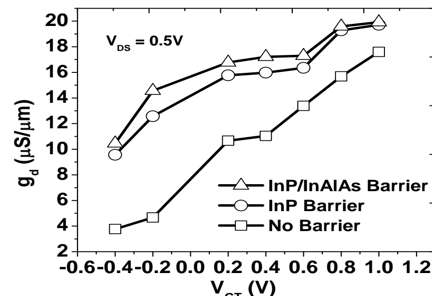

Figure 5. Variation of g_d as a function of V_{GT} at V_{DS}=0.5 V for three types of InGaAs MOSFETs.

Fig. 2 shows a comparison of the simulated device characteristics with the experimental curves as reported in [2] for InGaAs channel n-MOSFETs with different architectures – no barrier, single barrier and double barriers. One can easily observe a good agreement between the simulated and experimental curves from Fig. 2. This feature certainly ensures the validity of our simulation techniques. Fig. 3 shows the variation of g_m as a function of gate overdrive voltage V_{GT} (= $V_{GS} - V_T$, where V_T is the threshold voltage) at V_{DS} = 0.5V. The value of V_T is extracted as per the constant current definition (10^{-7} A/μm) and found be -0.01, -0.26, and -0.3V for no barrier, single-barrier, and double-barrier devices, respectively, which are in consistence with the reported values in [3]. Significant improvement in g_m is observed in Fig. 3 for a device with a barrier layer in general; with a double barrier showing the best results. A barrier layer enhances the electron mobility in the channel as it keeps the channel away from the insulator-semiconductor interface resulting in improvement in both I_{DS} and g_m, as evident in Figs. 2 and 3. The g_m/I_{DS} is an important device parameter for analog circuit performance, since g_m represents the amplification delivered by the device and I_{DS} represents the power dissipation to obtain the amplification. Therefore, higher the g_m/I_{DS} ratio, more suitable is the device for analog applications. Fig. 4 shows a comparison of g_m/I_{DS} as the function of V_{GT} for the above mentioned three devices. It is observed in Fig. 4 that, although a single-barrier device shows marginal improvement in g_m/I_{DS}, the same is significant for a double-barrier device. A comparison of g_d as a function of V_{GT} between the above three devices is shown in Fig.5. It is observed in Fig. 5 that the device with no barrier shows the smallest value of g_d as compared with the devices with a single barrier or a double barrier. The gate control over the channel increases as one moves from the double barrier device to the no barrier device through the single barrier device, the impact of SCEs, such as DIBL, is also reduced accordingly, thereby reducing the value of g_d. A decrease in g_d is expected by adopting SCE reduction techniques such as dual material gate [13-15].

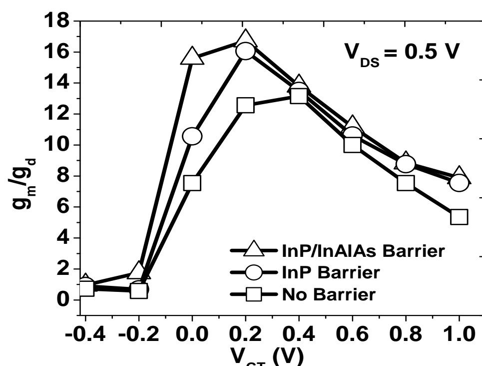

Figure 6. Plot of intrinsic voltage gain g_m/g_d as a function of V_{GT} for the three types of InGaAs MOSFETs.

Fig. 6 shows a comparison of the intrinsic voltage gain g_m/g_d as a function of V_{GT} between the three different device structures. It is evident in Fig.6 that a barrier layer helps improve the device gain; with a double barrier layer producing the highest gain. This is due to the significant improvement in g_m when a barrier layer is used in the device, as observed in Fig.3, in spite of the fact that the improvement in g_m is partially compensated by the higher value of g_d, as observed in Fig.5.

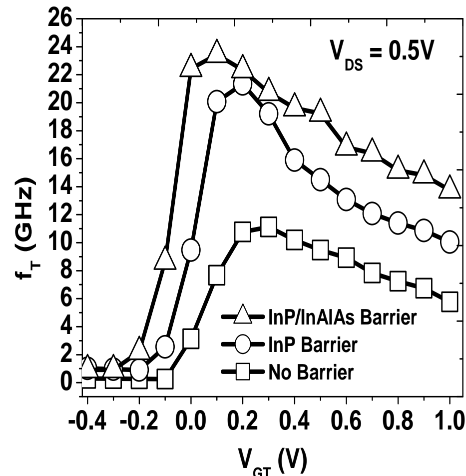

Figure 7. Comparison of unity-gain cut-off frequency f_T as a function of V_{GT} for the three types of InGaAs MOSFETs.

Fig. 7 shows a comparison of f_T as a function of V_{GT} among the three different device structures. The device with double barrier exhibits the highest value of f_T as compared to other devices, which is again due the improvement in g_m for such devices.

III. CONCLUSION

The impact of a barrier layer on the analog circuit performance of an InGaAs MOSFET has been performed in detail. It is found that, although a barrier layer improves the analog performance parameters, except g_d, of the device in general, the improvement is significant for the device with a double-barrier layer. Weaker control of the channel by the gate results in deterioration in g_d for such devices. Therefore, further improvement in the analog performance of such devices may be possible by reducing g_d with the use of some SCE reduction techniques.

IV. ACKNOWLEDGEMENT

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