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# SINGLE STAGE LOW FREQUENCY ELECTRONIC BALLAST FOR HID LAMPS

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**Abstract -** The paper presents a single-stage high-power-factor electronic ballast for metal halide lamps. The proposed ballast integrates a buck-boost converter, a buck converter and a full-bridge inverter into a single power conversion circuit. The buck-boost converter served as a power factor corrector (PFC) is designed to operate at discontinuous conduction mode (DCM) to achieve nearly a unity power factor at the input line. By adjusting the duty-ratio of the active switches of the PFC, the lamp power is remained at rated value for universal input voltage ranged from 90 Vrms to 264 Vrms. The four active switches of the full-bridge inverter, an inductor and a capacitor form a bidirectional buck converter which supplies a low frequency square-wave currentfor the lamp at to avoid the lamp from happing acoustic resonance. The circuit operation is analyzed in detail to derive the design equations. A prototype electronic ballast for a 70 W metal halide lamp is built and tested.

## I. INTRODUCTION

Among various kinds of high intensity discharge (HID) lamps, metal halide (MH) lamps have the advantages of long lamp life, high luminous efficacy, good color rendition, and have been widely used in many lighting applications . Since MH lamps have the characteristics of negative incremental impendence, ballasts are required to stabilize the lamp current. With the rapid development of power electronics, high frequency electronic ballasts have numerously replaced the traditional electromagnetic ones to reduce the size and weight and improve the efficiency of the ballast circuit and light performance in recent years. However, MH lamps driven by a high frequency electronic ballast may suffer from problematic acoustic resonance which may lead to arc instability, light fluctuation or extinguishment, and even cracking the arc tube. Many approaches have been proposed to solve the acoustic resonance. Among them, driving MH lamps with a low-frequency square-wave voltage has been considered the most effective method. Besides, in order to comply with the more stringent regulations on current harmonics, such as IEC61000-3-2 standards, and to improve the power factor, electronic ballasts require an additional ac/dc conversion stage to perform as a power-factor corrector (PFC). Hence, the most common used electronic ballasts in light market are usually of a three-stage circuit topology. The first stage is a PFC and the second stage is a buck converter which regulates the dc-link voltage for the third stage and thereby controls the lamp power. Both the first and the second stages operate at high switching frequency to enable the use of small magnetic components. The final stage is a full-bridge inverter of which the active switches operate at low switching frequency to drive the MH lamp with a low-frequency square-wave voltage. Although such three-stage electronic ballasts can achieve a high

power and drive the MH lamp with a low-frequency square-wave voltage to avoid the acoustic resonance, they are not cost-effective products.

Some literatures have successfully developed two-stage electronic ballasts by integrating the buck converter stage and the full-bridge inverter stage.These two-stage approaches can effectively achieve a high power factor and eliminate the occurrence of acoustic resonance by driving the MH lamp with a low-frequency square-wave voltage. In order to further reduce the component count and hence lower the product cost, this paper proposes a novel single-stage electronic ballast which are derived by integrating the PFC, the buck converter and the full-bridge inverter into a single power conversion circuit. A prototype circuit designed for a 70W MH lamp was built and tested to verify the analytical predictions

## II. CIRCUIT CONFIGURATION AND OPERATION

Fig. 1 shows the proposed single-stage electronic ballast which is derived by integrating a buck-boost converter, a buck converter and a full-bridge inverter. MOSFETs $S1\sim S4$ serve as the active switches of a full-bridge inverter. Diodes $D1\sim D4$ represent their intrinsic body diodes. $S1\sim S4$ are controlled by four gated signals $vGS1 \sim vGS4$, respectively.
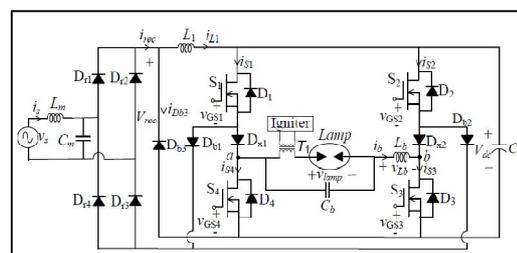


**Fig. 2.1 : The proposed single-stage electronic ballast.**

Figure 2.2 illustrates their time sequence. As shown, $vGS3$ and $vGS4$ are low-frequency rectangular-wave voltages with a short dead time between them. On the contrary, $vGS1$ and $vGS2$ are high-frequency rectangular wave voltages which happen when $vGS3$ and $vGS4$ are at high voltage level, respectively.

The full-bridge rectifier ($Dr1~Dr4$) is followed by a buck-boost converter which consists of active switch $S1$ and $S2$, diodes $Db1$, $Db2$ and $Db3$, inductor $L1$ and dc-link capacitor $C1$. The buck boost converter performs the function of PFC by operating at discontinuous current mode (DCM) at a fixed switching frequency to make the input line current be sinusoidal and in phase with the input line voltage. The four switches $S1~S4$, inductor $Lb$, capacitors $Cb$, $C1$ and diodes $Dx1$, $Dx2$ form a bidirectional buck converter. $S1$ and $S2$ are switched at high frequency and the high-frequency components of the inverter voltage $vab$ are filter out by $Cb$ and $Lb$. Hence, the voltage across $Cb$ will be a low-frequency square waveform. An igniter and the transformer $T1$ generate a high voltage to start-up the lamp. A small low-pass filter, $Lm$ and $Cm$, is used to remove the high frequency current harmonics at the input line.
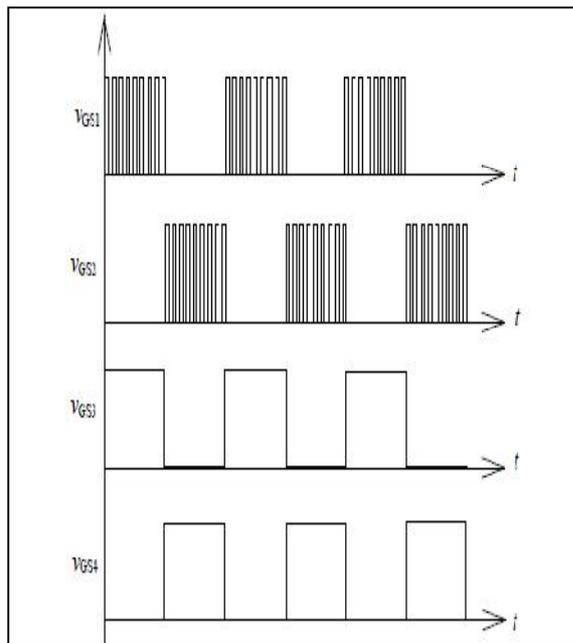


**Fig. 2.2 : Time sequence of gated voltages**

The operation modes for the sequence when either $vGS3$ or $vGS4$ is at high voltage level are similar. Therefore, the following circuit analysis only illustrates the operation modes when $vGS3$ is at high level. The buck-boost converter and the buck converter are both designed to operate at DCM. At steady-state, the circuit operation can be divided into four modes in each high frequency cycle. For simplifying the circuit analysis, the low-pass filter, the lamp igniter circuit and transformer $T1$ are omitted and the MH lamp is represented by its equivalent resistance, $R$ $lamp$. Fig.3 shows the

operation modes and Fig. 4 illustrates the theoretical waveforms for each mode. The circuit operation is described as follows:

**Mode I ($t_0 < t < t_1$) :** $Mode$ $I$ begins at the instant of turning on switch $S1$. The rectified input voltage $vrec$ is imposed on the inductor $L1$. Since the buck-boost converter is designed to operate at DCM, the Inductor current $iL1$ increases linearly from zero with a rising slope which is proportional to the rectified line voltage .Mean while, $S3$ operates at low frequency and keeps on in this mode. The voltage across the inductor $Lb$ is equal to $Vdc - Vlamp$. Since the buck converter is also operated at DCM, the buck inductor current $ib$ rises from zero linearly. Capacitors $C1$ supplies current through $S1$, $Dx1$ and $S3$ to charge $Lb$.

**Mode II ($t_1 < t < t_2$) :** The circuit enters Mode II at the instant of turning off $S1$ while $S3$ r emains on. Current $iL1$ will freewheel through diode $Db3$ to charge $C1$. Meanwhile, current $ib$ flows through $S3$ and diode $D$ 4 to supply current to $Cb$ and the lamp. The voltages across $L1$ and $Lb$ are equal to $–Vdc$ and $–Vlamp$, respectively. Therefore, both currents decrease linearly. Because $S1$ operates at a constant duty ratio within the period of the input voltage, the peak of $iL1$ is proportional to $vrec$. The duration for $iL1$ declining to zero is not a constant but varies with $vrec$, while that for $ib$ declining to zero is a constant. Thus, there could be two possible modes following Mode II, depending on which current of $iL1$ or $ib$ reaches zero first.

**Mode III-A ($t_2 < t < t_3$) :** When the rectified input voltage is low, so does the peak value of $iL1$. On this condition, $iL1$ declines to zero before $ib$ does. When $iL1$ declines to zero, the circuit operation enters Mode III-A. During this mode, only $ib$ and lamp current keep flowing and $ib$ decreases continuously. When $ib$ reaches zero, Mode III-A ends and the circuit operation enters Mode IV.

**Mode III-B ($t'_2 < t < t'_3$) :** On the contrary, when $vrec$ is high, the peak of $iL1$ is also high. It takes a longer time for $iL1$ declining to zero. Therefore, $iL1$ may decline to zero later than $ib$ does. The circuit operation will enter Mode III-B when $ib$ reaches zero. In this mode, current $iL1$ keeps flowing through $Db3$ to charge $C1$ while $Cb$ supplies current for the lamp. This mode ends at the time when $iL1$ reaches zero and the circuit operation enter Mode IV.
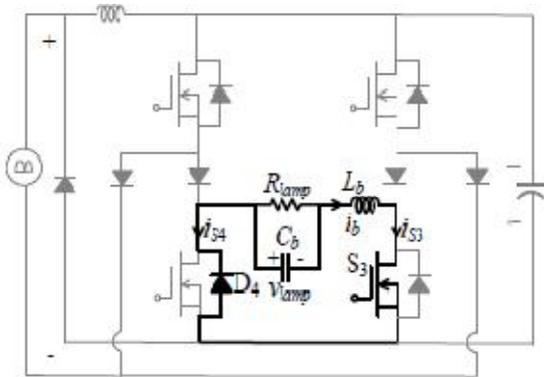
**Mode IV ($t_3 < t < t_4$) :** During this mode, both $iL1$ and $ib$ are zero. Only the lamp current supplied from $Cb$ exists. When $vGS1$ goes back to high level to turn on $S1$, the circuit operation returns to Mode I of the next high-frequency cycle.
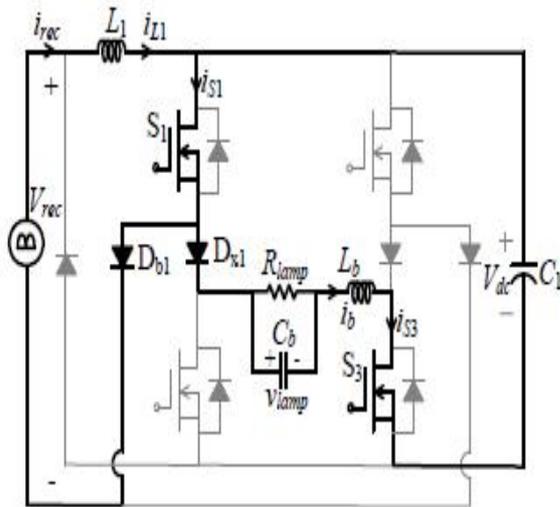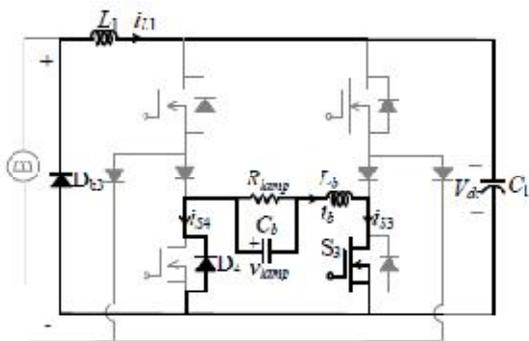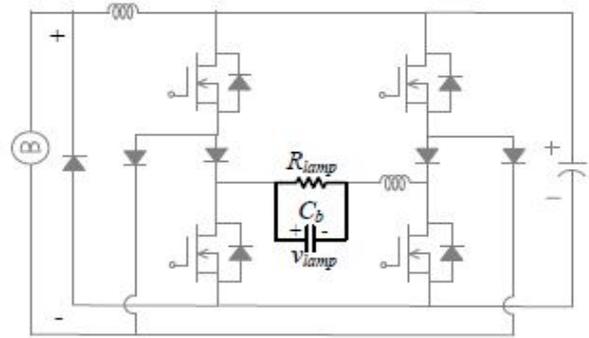
Mode I
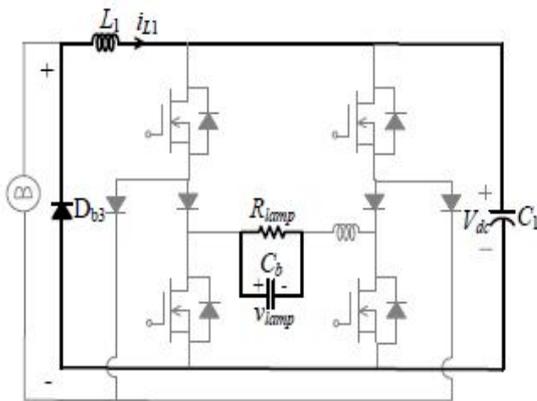


Mode II



Mode IIIA



Mode IIIB



Mode IV
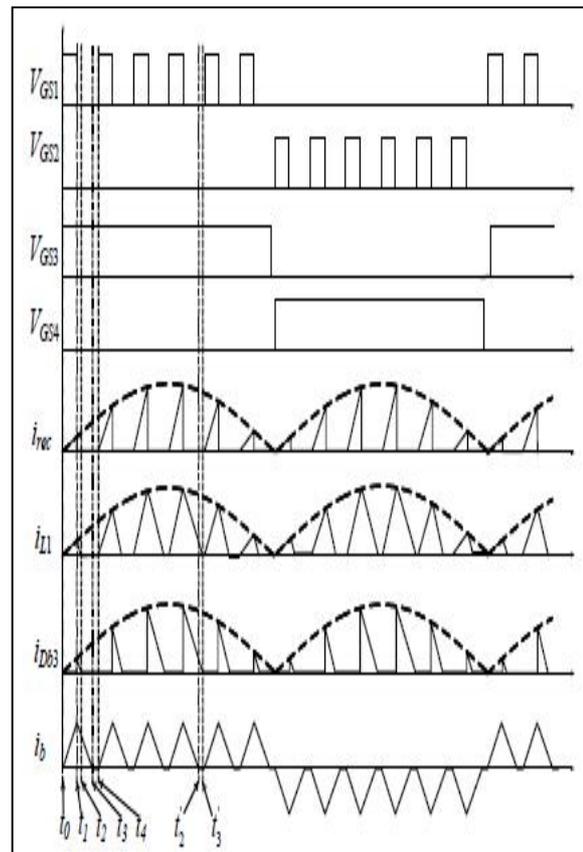
**Fig. 2.3. Operation modes.**



**Fig. 2.4 : Theoretical waveforms.**

## III. CIRCUIT ANALYSIS

For simplifying the circuit analysis, the following assumptions are made:
1) All the circuit components are ideal.
2) The capacitances of $C1$ is large enough, thus the dc-link voltage $Vdc$ can be regarded as a voltage source.
3) The capacitance $Cb$ is large enough so that the voltage $Vlamp$ across it remains constant during the high-frequency switching cycle.
4) The lam p is regarded as an open circuit before ignition, and a pure resister at the steady state.

Based on the circuit operation described above, the features of the buck-boost converter and the buck

converter remain the same, even though they share some switches. Therefore, the buck-boost PFC and the buck converter can be analyzed, separately.

## A. Buck-Boost Power Factor Corrector

The ac/dc converter is supplied from the ac line voltage source.

$$V_s(t) = V_m \sin(2\pi f_L t) \tag{1}$$

Where $fL$ and $Vm$ are frequency and amplitude of the line voltage source, respectively. In practice, $fL$ is much lower than the high switching frequency, $fs$, of $S1$ and $S2$. It is reasonable to consider the rectified input voltage as a constant over a high frequency cycle. Since the buck-boost converts are operated at DCM over an entire line frequency cycle, $iL1$ rises from zero at the beginning of Mode I and reaches its peak at the end of Mode I. The waveform of $irec$ and $iL1$ are conceptually shown in Fig. 5. Their peaks follow a sinusoidal envelope and can be expressed as:

$$i_{L1,peak}(t) = \frac{V_m \sin(2\pi f_L t) D_1 T_s}{L_1} \tag{2}$$

Where $Ts$ is the high-frequency switching period and $D1$ is the duty ratio of the high switched active switches. The high-frequency contents of $iL1$ can be removed by $Lm$ and $Cm$. Therefore, the input current $is$ is equal to the average of $iL1$ over a high-frequency cycle.

$$i_s(t) = \frac{1}{T_s} \int_0^{T_s} i_{L1}(t) \cdot d(t) = \frac{V_m T_s D_1^2}{2L_1} \sin(2\pi f_L t) \tag{3}$$

Equation (3) reveals that the input current is sinusoidal and in phase with the input line voltage if the duty ratio remains constant over an entire line cycle. As a result, a high power factor can be achieved. The input power can be obtained by taking average of its instantaneous value over one line-frequency cycle.

$$P_{in} = \frac{1}{2\pi} \int_0^{2\pi} v_s(t) \cdot i_s(t) d(2\pi f_L t) = \frac{V_m^2 D_1^2}{4L_1 f_s} \tag{4}$$
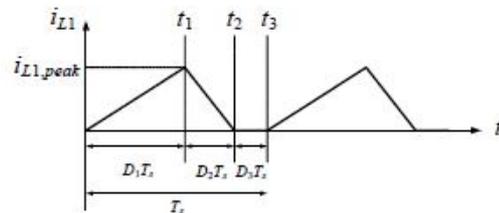
Then, the lamp power can be calculated.

$$P_o = \eta \cdot P_{in} = \frac{\eta V_m^2 D_1^2}{4L_1 f_s} \tag{5}$$

Where $\acute{\eta}$ represents the circuit conversion efficiency.
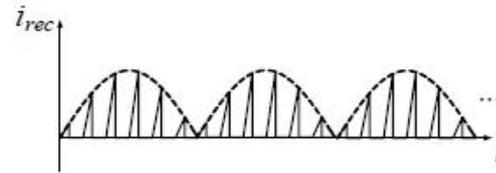


(a) $i_{rec}$ in low-frequency cycles



(b) $i_{L1}$ in high-frequency cycles

**Fig. 3.1 : The theoretical waveforms of *irec* and *iL1*.**

## B. Bidirectional Buck Converter

Based on operation modes in section II, $S1{\sim}S4$, $Lb$ and $Cb$ form a bidirectional buck converter operating at DCM. The inductor $Lb$ and capacitor $Cb$ can filter out the high frequency components of the inverter voltage $Vab$. Then, the voltage across $Cb$ is low-frequency square waveform. Fig. 3.2 shows the equivalent circuits of the bidirectional buck converter. In Fig. 3.2(a) $S2$ and $S4$ are off; $S3$ is kept on and $S1$ is turned on and off at high frequency. In Fig. 3.2(b), $S1$ and $S3$ are off; $S4$ is kept on and $S2$ is turned on and off at high frequency. Since the operations in Fig. (a) and Fig. (b) are similar except that the polarities of $ib$ and $Vlamp$ are reversed. Here, only the circuit operation in Fig. 3.2(a) is discussed.

When $S1$ and $S3$ are on, the voltage across inductor $Lb$ is

$$v_{Lb} = V_{dc} - V_{lamp} . \tag{6}$$

The inductor current $ib$ rises from zero and will reach a peak value at the instant of turning off $S1$. Its peak value is equal to

$$i_{b,peak} = \frac{(V_{dc} - V_{lamp}) D_1 T_s}{L_b} \tag{7}$$

When $S1$ is turned off, $ib$ freewheels through diode $D4$. The voltage across $Lb$ is

$$v_{Lb} = -V_{lamp} \tag{8}$$

This negative voltage causes $ib$ to decrease. The duration for $ib$ decreases from the peak value to zero is

$$T_{off} = \frac{(V_{dc} - V_{lamp}) D_1 T_s}{V_{lamp}} \tag{9}$$

For fulfilling DCM operation, $Toff$ should be shorter than $(1-D1)Ts$. It leads to

$$V_{dc} \leq \frac{V_{lamp}}{D_1} . \tag{10}$$

As can be seen in Fig. 2.4, *ib* is a triangular waveform in the high-frequency cycle. At steady state, its average is equal to lamp current.

$$\overline{i_b} = \frac{(V_{dc} - V_{lamp})V_{dc}D_1^2 T_S}{2L_b V_{lamp}} = \frac{V_{lamp}}{R_{lamp}} \quad (11)$$

Where *Rlamp* is the equivalent lamp resistance. From (11), *Lb* can be expressed as:

$$L_b = \frac{(V_{dc} - V_{lamp})V_{dc}D_1^2 T_S R_{lamp}}{2V_{lamp}^2} \quad (12)$$
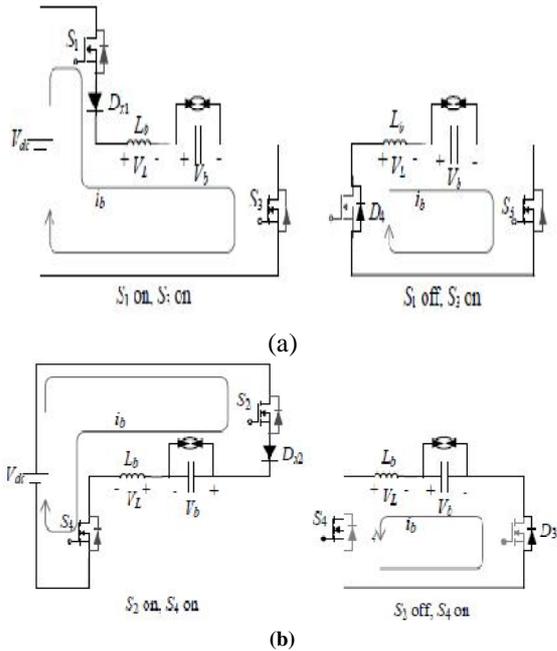


(a)



(b)

**Fig. 3.2 : Equivalent circuit of buck converter. (a) in the positive half-cycle, (b) in the negative half-cycle of the input voltage**

## IV. PARAMETERS DESIGN

An electronic ballast for a 70 W MH lamp is illustrated as a design example. Table I lists the circuit specifications. The switching frequency of *S*1 and *S*2 is 30 kHz while that of *S*3 and *S*4 is 60Hz. The lamp voltage and current at rated power are 85 V and 0.82 A, respectively. For fulfilling the buck-boost converter to operate in DCM, the dc-link voltage, *Vdc*, should be large enough to meet

$$V_{dc} \geq \frac{V_m D_1}{(1-D_1)} \quad (13)$$

Form (10) and (13), the relation curves of *Vdc* versus *D*1 is plotted and shown in Fig. 7 when the input voltage is 90 Vrms and the lamp voltage is 85 V. For operating both the buck-boost converter and the buck converter at DCM, the duty ratio *D*1 should be less than 0.54. Based on (5), the duty ratio is inverse proportional to the input voltage at a constant lamp power. Here, the duty ratio is regulated from 0.54 to 0.184 for the input voltage from 90 Vrms to 264

Vrms. In this design example, *Vdc* of 155 V is chosen to meet the DCM operation at an input voltage of 90 Vrms.

Assuming 85% circuit efficiency, *L1* and *Lb* are calculated to be 0.48 mH and 1.19 mH by using (5) and (12), respectively. To avoid the lamp from acoustic resonance, the energy caused by the lamp current ripple should be small. It requires *Cb* be high enough to reduce the voltage ripple, thereby, reduce the current ripple. The voltage ripple of the lamp voltage is expressed as [17]:

$$\frac{\wedge V_{lamp}}{V_{lamp}} = \frac{(1-D)T_S^2}{8I_b C_b} \times 100\% \quad (14)$$

In order to have a voltage ripple lower than 10% *Cb* is calculated to be larger than 0.54 uF.

## V. CONCLUSION

A novel single-stage electronic ballast for driving MH lamp with a low-frequency square-wave voltage is presented. It is suitable for the universal input voltage ranged from 90 Vrms to 264 Vrms. The proposed circuit is derived by integrating a buck-boost converters, a buck converter and a full-bridge inverter. The buck-boost converter performs as a power-factor corrector and operates at DCM to achieve high power factor and low total current harmonic distortion. The circuit operations are described and the design equations are derived. A prototype circuit designed for a 70-W MH lamp was built and measured to verify the theoretical analyses. Experimental results show that the electronic ballast performs satisfactorily. A nearly unity power factor and low THD can be achieved. The lamp is driven by a low-frequency square-wave current to avoid the occurrence of acoustic resonance.

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