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PERFORMANCE EVALUTION OF CNTFET-BASED SRAM CELL DESIGN

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Abstract - Carbon Nanotube Field-Effect Transistor (CNTFET) technology with their excellent current capabilities, ballistic transport operation and superior thermal conductivities has proved to be a very promising and superior alternative to the conventional CMOS technology. A detailed analysis and simulation based assessment of circuit performance of this technology is presented here. As figures of merit speed, power consumption and stability are considered to evaluate the performance parameters of CNTFET-Based SRAM Cells with different chiral vectors for the optimum performance. A novel performance metric, presented as "SPR," is used to assess these figures of merit. This comprehensive metric includes a metric of low power delay product (PDP) for write operation and high stability in the operation of a memory cell. It is shown that an 8T SRAM cell provides 73% higher SPR than Dual-Chiral based 6T SRAM cell for CNT technology and 124% higher SPR than its CMOS counterpart, thus attaining superior performance. The CNTFET-based 8T SRAM cell demonstrates that it provides high stability, low delay and low power, which is better than CNTFET-based 6T SRAM cell as well as CMOS SRAM cell.

Keywords*-CNTFET; CNT;SNM; SINM; SPR; SRAM;PDP.*

I. INTRODUCTION

Scaling down the physical gate length (feature size) of current CMOS technology deeper in nanoscales results in various critical challenges and reliability issues, which will reduce its potential for energy-efficient applications in near future. To handle these difficulties in terms of physical phenomena and technological limitations, such as increased short-channel effects, reduced gate control, exponentially rising leakage current, larger process variations and high power dissipation, scientists and researchers are working towards new alternative technologies to replace conventional CMOS technology [1]. Nanoscaled alternatives, such as ultrathin body devices FinFETs [2], Carbon nanotube field-effect transistor (CNTFET) [3] could be the possible alternatives to bulk silicon transistors. CNTFETs are very promising and superior alternative to the conventional CMOS, due to their unique 1-D band structure that provides ballistic transport operation by suppressing backscattering, superior thermal conductivities and excellent current capabilities [4-8].

In a billion-transistor superscalar microprocessor, approximately 70% of the transistors are estimated to be used for memory arrays such as larger L2 and L3 SRAM data caches. Therefore, it is highest priority to design a fast and power-efficient memory structures to increase the performance of overall system. The unique properties of CNTFETs such as ballistic transport operation and low current under OFF condition makes them very attractive for the high performance and increased integration complexity of SRAM arrays design.

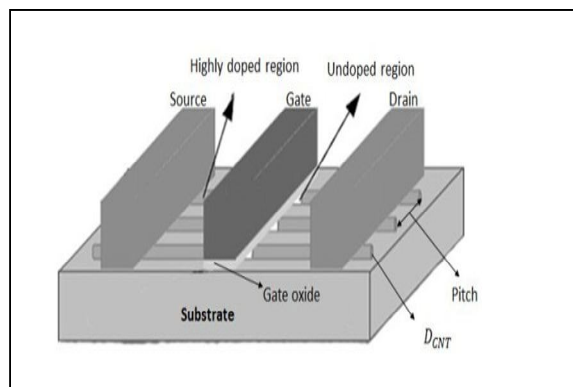
In this paper, the performance parameters of 8T Static RAM (SRAM) cell as well as 6T SRAM cell based CNTFETs are evaluated and compared in various simulation conditions and test benches by using novel efficient performance matrices. For 6T SRAM cell similar qualitative behavior has been observed as found in Ref. [16]. Hereafter, a common simulation environment has been adopted to perform a comparative analysis between 6T SRAM cell and 8T SRAM cell. At a circuit level design of CNTFET, the analysis and simulation for selection of optimum diameters for optimized threshold voltages of the two types (i.e. N or P) of CNTFETs are also performed to achieve the best overall performance in terms of power consumption, write time and stability of the CNT-based SRAM cell. Experimental results demonstrate that 8T SRAM cell outperforms 6T SRAM cell in terms of high stability, low delay and low power.

In Section II of this paper, a brief review of the characteristics and physical features of CNTFET devices is presented. The designs of 6T and 8T CNTFET SRAM cell are explained in Section III. Section IV includes the simulation result and finally, Section V concludes this paper.

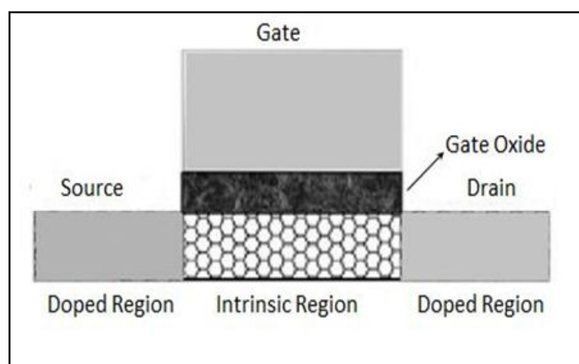
II. CARBON NANO TUBE FIELD EFFECT TRANSISTOR (CNTFET)

A carbon nanotube (CNT) is a graphene sheet (with carbon atoms appearing in a hexagonal pattern) rolled up to form a hollow cylinder. CNTs have extremely low electrical resistance because electrons can travel for large distances without scattering (ballistic transport). This is partly due to their very small diameter and huge ratio of length to diameter. Also, because of their low resistance, CNTs dissipate very little energy. This will prove useful in solving

the power consumption problems that are plaguing Silicon circuits. In the generic CNTFET which could be single wall (SWCNTs) or multi wall (MWCNTs), a carbon nanotube is placed between two electrodes while a separate gate electrode controls the flow of current in the channel, as presented in Figure1(a) [9-11].



(a)



(b)

Figure 1 (a).Carbon Nano Tube Field Effect Transistor, (b). Cross-section of MOSFET like CNTFET

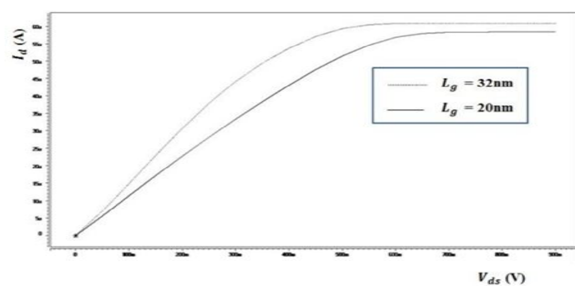


Figure 2. Current-Voltage characteristics for MOSFET like CNTFET

A typical CNTFET and the cross section of MOSFET like CNTFET is shown in Figure 1(a) and (b), respectively [9-11]. In SWCNTs, the arrangement of carbon atoms along the tube is determined by its chiral vector which is specified by (n, m) indices [9-11]. Based on a chiral vector, a SWCNT could be conducting or semiconducting. The current-voltage (I-V) characteristics of the CNTFET with different channel lengths, is shown in Figure 2, and they are similar to those of MOSFET which makes CNTFET a good candidate for ultra-low power applications. CNTFETs have the capability of setting the required threshold voltages by choosing proper diameter for the nanotubes [12], which makes them very suitable for implementing high-performance multiple-V_{th} structures. The threshold voltage of CNTFET can be approximated to the first order as the half bandgap and can be calculated by the following equation [9-11]:

$$V_{th} \approx \frac{E_g}{2e} = \frac{1}{\sqrt{3}} \frac{aV_\pi}{eD_{CNT}} \approx \frac{0.43}{D_{CNT}(nm)}$$

Where, $V\pi$ (≈ 3.033 eV) is the carbon π–π bond energy in the tight bonding model, e is the unit electron charge, parameter a (= 0.249 nm) is the carbon to carbon atom distance, and D_{CNT} is the diameter of CNTs, which is a function of chiral vector (n,m) and can be calculated by the following equation [9-11]:

$$D_{CNT} = \frac{a \times \sqrt{n^2+m^2+nm}}{\pi} \approx 0.0783 \times \sqrt{n^2+m^2+nm}$$

For example, the threshold voltage of the CNTFET having (19, 0) CNTs is 0.289 V because the D_{CNT} of (19, 0) CNT is 1.49 nm. Simulation results have corrected this threshold voltage. Figure 3 shows the threshold voltage of NCNTFET with different chiral vectors. Extensive research has been reported on manufacturing well-controlled CNTs [13-14]. In this paper, CNTFETs with different diameters are utilized and channel length of 20nm is selected for area efficient SRAM design.

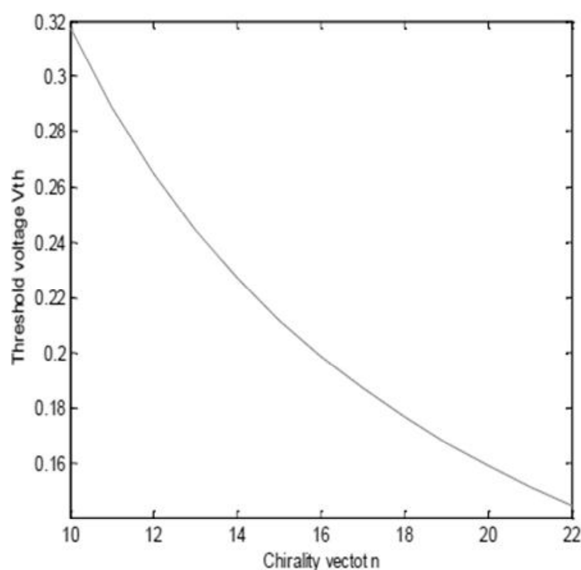


Figure 3. Threshold voltage of NCNTFET with different chiral vectors

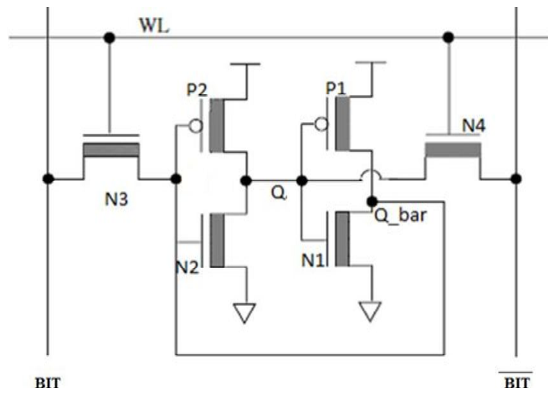


Figure 4. CNTFETs based 6T- SRAM

III. 6T & 8T SRAM CELL DESIGN

A. 6T SRAM Cell Design

The conventional [six-transistor (6T)] SRAM cell structure based on CNTFETs which is the core storage element of most register file and cache designs, is shown in Figure 4. It has four transistors P1, P2, N1 and N2 form two cross-coupled inverters for storage and two pass transistors N3 and N4 form as a combination of read/write port. With the aggressive scaling in CMOS technology, at ultra-low power supply ,the use of 6T SRAM cell leads to numerous critical problems like poor stability, high power consumption etc. In this case CNTFETs could be a good alternative with high stability and high density for high density memories.

The BIT and $\overline{\text{BIT}}$ lines in Figure 4 are pre-charged before any read operation. During read operation, the WL bit is "high" which makes both the transistor N3 and N4 to be turned ON and the stored data in SRAM cell is read. But this stored data may change due to a read-upset problem which is as follows. Suppose that the SRAM cell is currently storing a "1" so that Q is "1" and Q_bar is "0". When WL bit is high and transistor N3 and N4 are ON, then voltage level at node Q_bar will rise. In this case, an appropriate device sizing ratio between N1 and N3 is desired to limit the voltage at node Q_bar to be less than threshold voltage (V_{th}) so that the stored data will not differ during the read operation. For the appropriate selection of sizing ratio between N1 and N3, simulation has been done, which is shown in Figure 5, at the gate length of 20nm. As mentioned earlier, the threshold voltage of the (19, 0) CNTFET is 0.289V, so the sizing ratio of the N1 and N3 should not be less than 0.5. However, in this designing, sizing ratio between N1 and N3 is chosen as 1.5 for fair comparison with 8T SRAM cell as well as CMOS SRAM cell which has threshold voltage of 0.18V at gate length of 32 nm [15].

For the reliable write operation, the pull-up transistor of SRAM cell should not be very conducting. Suppose that the WL bit is high, SRAM cell is currently holding "1" and system is going to write "0" into SRAM cell. In this case the voltage level at node Q2 in Figure 4 will decrease only when the pass transistor N4 is stronger than the pull up transistor P2. Therefore, for the proper selection of sizing ratio between P2 and N4, simulations have been performed and the results are shown in Figure 6, at the gate length of 20nm. As described before, the threshold voltage of the CNTFET (19, 0) is 0.289V, so the sizing ratio between P2 and N4 should not be greater than 1.6. In this design, device sizing ratio between P2 and N4 is taken as 0.5 for proper comparison with CMOS which has threshold voltage of 0.18V at gate length of 32 nm.

The transistor width of CNTFET is defined in terms of the number of the tubes and the distance from one tube to adjacent tube is 20nm in a device [9-11]. The channel length chosen in this paper is also 20 nm. Therefore, in the presented CNTFET-based 6T SRAM cell, two NCNTFETs having device dimension of 80/20 nm, two PCNTFETs having device dimension of 40/20 nm and two NCNTFETs having device dimension of 60/20 nm are utilized. For a CMOS based.

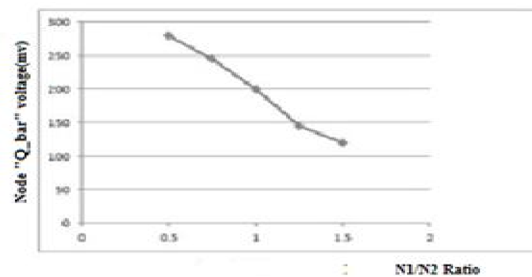


Figure 5.node "Q_bar" voltage v/s N1/N2 ratio

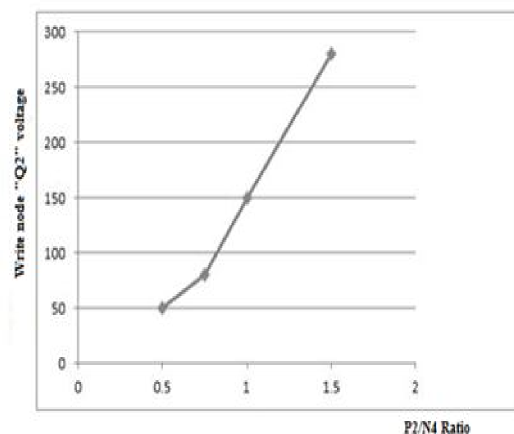


Figure 6. Write node "Q2" voltage v/s P2/N4 ratio

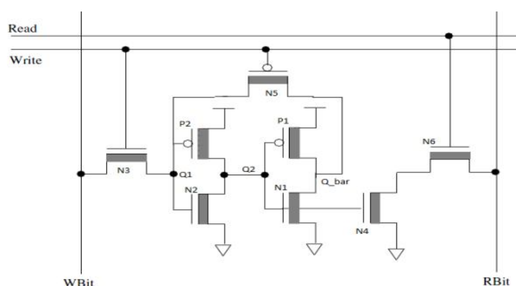
SRAM cell with a channel length of 32nm and similar circuit performance to the proposed CNTFET SRAM cell, the dimensions (width to length ratio) of the pull-up transistors, the pull-down transistors and

the pass gate transistors are found to be 2/1, 4/1, and 3/1, respectively.

B. 8T SRAM Cell Design

The need of 8T-SRAM has originated from the fact that the 6T SRAM has more power consumption and less immunity to noise voltage during read operation as a small noise voltage is enough to flip the data. Designing an efficient cache system with 8 transistors in basic SRAM cell provides increased stability and good effective memory speed. Figure 7 shows the 8T SRAM cell configuration based on CNTFETs, where the write and read bits are separated to improve read cycle. In 8T SRAM only the Write bit is used to write for both "0" and "1" data, while BIT and $\overline{\text{BIT}}$ lines are utilized for writing data in the conventional 6T SRAM.

The writing operation starts by breaking the feedback loop of the cross-coupled inverter. During read operation, the feedback loop is maintained. The feedback loop is disconnected by setting Write bit to"1".In this case, SRAM memory cell has just two cascaded inverters. The Wbit line voltage decides the data that is going to be written into SRAM cell. The Wbit line transfers the inversion of the input data to Q2 (cell data), which drives the other cascaded inverter to get Q_bar. The Wbit line has to be pre-charged before and after each write operation. When writing "0" data, there is no. discharging at WBit line so negligible power is consumed. But writing '1' data at Q2, the dynamic power consumption is same as 6T SRAM cell because the WBit line has to be discharged to ground level. The proposed 8T SRAM cell is more power efficient in comparison with conventional ones because during write operation, the circuit does not require discharging for every write operation but discharges only when writing "1" data, and the discharging activity factor of the WBit line is less than 1.



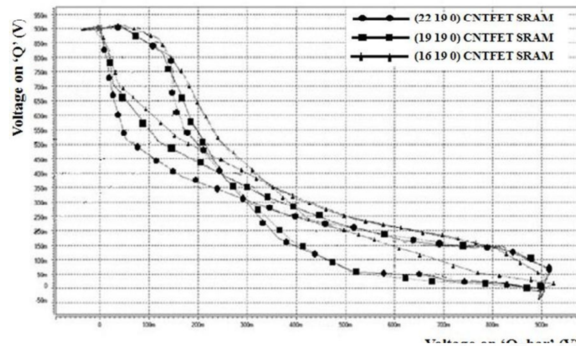
The Rbit line has to be pre-charged before any read operation. During read operation, Read bit is "high" and Write bit is low, which set turning ON condition for N5 & N6. When Q2="0", the transistor N4 is OFF maintaining the Rbit line at the pre-charged value, which shows the cell data Q2 holds "0". On the other side, when cell data Q2= "1", both the transistors N4 and N6 are ON which makes the Rbit line to be dropped at few milivolts, which is quite enough for detection in the sense amplifier. In the proposed 8T SRAM cell design, the device sizing of the read zero path with pull down transistor N4 and N6 is made 8 and 6 times larger to get a quicker discharge path to ground. In this design, two PCNTFET (P1,N5) with one tube, two NCNTFETs (N2,N3) with two tubes, one P-type CNTFET (P2) with two tube, one NCNTFET (N1) with one tube, are utilized for proper functionality and shorter delay at the minimal cost of the chip area overhead. Compared to CMOS SRAM cell with a transistor length of 32nm, a CNTFET SRAM cell offers a significant saving in chip area.

IV. SIMULATION RESULTS

In this paper, NCNTFETs and PCNTFETs with different chiral vectors are utilized for the optimized circuit performance. Therefore, a triplet index (*np*, *nn*, *m*) as shown in Ref. [16], where *np* and *nn* indicate the first chiral vector "*n*" of the PCNTFETs and NCNTFETs, respectively, and *m* is the common second chiral vector "*m*" of the two types of CNTFETs, is used. It has been shown in Ref. [16] that a comprehensive metric, SPR must be used to assess the circuit performance in terms of power dissipation, stability with respect to noise and delay. The SPR (in sec^{-1}) is defined as the ratio of product of static noise margin (SNM) and static current noise margin (SINM): (SNM X SINM) to the product of write power and write delay (write power X write delay). The SNM of SRAM cell is demonstrated as the maximum noise magnitude that does not disturb the stored bit of the SRAM cell [17]). The SINM is defined as the maximum DC noise current that can be injected in the SRAM cell without changing its content [18].Therefore, the combined SNM and SINM is used in SPR, to define the static stability criteria for the SRAM cell [18]. To measure the SNM of the SRAM cell, simulations have been performed on CNTFET SRAM cells with index triplets of (16, 19, 0), (19, 19, 0), and (22, 19, 0) for the CNTFETs. Simulation results for SNM of the 6T SRAM cell as well as 8T SRAM cell at 0.9V power supply and room temperature are shown in Figure8 (a) and 8(b), respectively. As shown in Figure 8, the SNM of SRAM cell is increased as the chiral vector of P-type CNTFET changes from (19, 0) to (22,0). Simulation has shown that the SNM of the CMOS SRAM at 32nm channel length [15], is smaller than CNTFET SRAM cell. The PDP can be used as an important metric to compare the performance of circuits. The power dissipation of SRAM cell is high during write operation in comparison with read operation. Therefore, in this paper, write power and write delay is used to estimate PDP.

In this paper circuit simulation uses the Stanford CNTFET model [9-11] the 32nm BSIM PTM (predictive technology model) [15] for CMOS to evaluate the performance of CNTFET and CMOS

SRAM cells. Table I & II show the SNM, SINM, Write Power, Write Delay



(a)

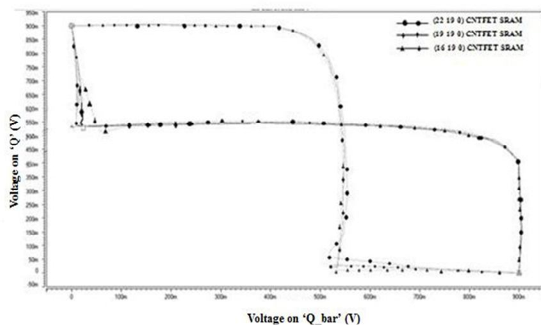


Figure.8 SNM of the (a) 6T SRAM cell (b) 8T SRAM cell

and SPR of the CNTFET SRAM cell and CMOS SRAM cell for 6T and 8T respectively, with different chiral vectors, at 0.9V power supply and room temperature. Simulation results confirm that (19,19,0) 8T SRAM cell occupies higher SPR in comparison with all specified CNTFET SRAM cells as well as CMOS SRAM cell. They also show that 8T SRAM cell provides 73% higher SPR than 6T SRAM cell in CNT technology and 124% higher SPR than 8T SRAM cell in CMOS technology.

TABLE I. ALL PERFORMANCE PARAMETERS OF THE 6T-SRAM CELL (CHANNEL LENGTH = 20 NM)

SRAM Cell (6T-SRAM)	SNM (mV)	Write time (ps)	Write Power (µW)	SINM (µA)	SPR (1/s)	SNM/ Write Delay (mV/ps)
(16,19,0)	176.00	26	24.4	70	1.94e+10	6.76
(19,19,0)	204.00	31	26.34	80	1.99e+10	6.58
(22,19,0)	225.00	35	30.10	85	1.81e+10	6.42
32nm CMOS SRAM cell	120.25	25	50.00	50	4.8e+9	4.82

TABLE II. ALL PERFORMANCE PARAMETERS OF THE 8T-SRAM CELL (CHANNEL LENGTH = 20NM)

SRAM Cell (8T-SRAM)	SNM (mV)	Write time (ps)	Write Power (µW)	SINM (µA)	SPR (1/s)	SNM/ Write Delay (mV/ps)
(16,19,0)	239.00	11	6.59	9.10	3e+10	21.70
(19,19,0)	392.00	13	7.10	7.91	3.35e+10	30.15
(22,19,0)	410.00	15	7.74	7.00	2.47e+10	27.33
32nm CMOS SRAM cell	268.56	18	20.40	28.00	2.05e+10	14.92

V. CONCLUSION

This paper has contemplated the use of CNTFETs in 8T SRAM and 6T SRAM cell designs. The extensive simulation and analysis have been done for selection of best chiral vector for the transistors used in 8T SRAM and 6T SRAM cell to attain high stability, low PDP during write operation. The performance parameters of an SRAM cell have been investigated based on a novel comprehensive metric which is known as SPR. This comprehensive metric provides versatile performance measurement of stability, access time, and power consumption in the operation of a memory cell.

It has been shown that 8T CNTFET SRAM cell has 124% higher SPR than its CMOS counterpart. In comparison with dual-chiral based 6T SRAM cell in Ref.[16], our simulation results have confirmed the superiority of the 8T SRAM cell in terms of 122% higher SNM, 50% less access time and 73% higher SPR. Thus, 8T CNTFET SRAM cell achieves superior performance in terms of high stability, low delay and low power in CNT as well as in CMOS Technology.

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