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COMPARATIVE STUDY ON CARRIER OVERLAPPING PWM STRATEGIES FOR THREE PHASE FIVE LEVEL DIODE CLAMPED AND CASCADED INVERTERS

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Abstract: This paper proposes three Carrier Overlapping PWM (COPWM) methods that utilize the (CFD) control freedom degree of vertical offsets among carriers. They are: COPWM-A, COPWM-B, COPWM-C these three methods are simulated . This paper presents a comparative study of diode clamped and cascaded three phase five-level inverters based on sinusoidal PWM& modified space vector PWM control techniques. Performance analysis is based on the results of simulation study conducted on the operation of the multilevel inverters using MATLAB/ SIMULINK. For comparison purposes, non-overlapping phase disposition PWM (PD PWM) using SPWM and modified space vector PWM is also presented. The performance parameters chosen the work included fundamental output voltage and total harmonic distortion. . A hardware set up was developed for a single-phase 5-level cascaded inverter topology using constant pulses.

Index Terms*- Multilevel concept, Diode clamped and Cascaded Multi level inverters, Multi level carrier signals, Pulse width modulation, Total Harmonic Distortion.*

I. INTRODUCTION

Multilevel power conversion technology is a very rapidly growing area of power electronics with good potential for further development. The most attractive application of this technology is in the medium-to-high-voltage range, motor drives, power distribution, and power conditioning applications. In recent years, industry demands power in the megawatt level. Controlled ac drives in the megawatt range are usually connected to medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels [4].

In general multilevel inverter can be viewed as voltage synthesizers, in which the high output voltage is synthesized from many discrete smaller voltage levels. The main advantages of this approach are summarized as follows:

- They can generate output voltages with extremely low distortion and lower (dv/dt).
- They can operate with a lower switching frequency.
- Their efficiency is high (>98%) because of the minimum switching frequency.
- They are suitable for medium to high power applications.

The selection of the best multilevel topology for each application is often not clear and is subject to various engineering tradeoffs. By narrowing this study to the DC/AC multilevel power conversion technologies that do not require power generation.

Multilevel inversion is a power conversion strategy in which the output voltage is obtained in steps thus bringing the output closer to a sine wave and reduces the total harmonic distortion (THD). Various circuit configurations namely diode clamped, flying capacitor and cascaded, etc., have been proposed [5].

II. SYSTEM CONFIGURATION

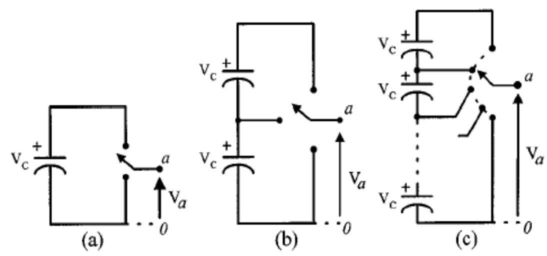


Fig. 1 Multilevel concept for (a) two level (b) three level and (c) n- level

Multilevel inverter structures have been developed to overcome shortcomings in solid-state switching device ratings so they can be applied to higher voltage systems. The multilevel voltage source inverters [10] unique structure allows them to reach high voltages with low harmonics without the use of transformers. The general function of the multilevel inverter is to synthesize a desired ac voltage from several levels of dc voltages as shown in Fig.1.

Compares the power component requirement per phase leg among the two multilevel voltage source inverters mentioned above. The table 1 shows that the number of main switches and main diodes needed by the inverters to achieve the same number of voltage levels is the same.

Devices	Diode clamped Inverter	Cascaded Inverter
Main switching Devices	2(m-1)	2(m-1)
Main diodes	2(m-1)	2(m-1)
Clamping diodes	(m-1)*(m-2)	0
Dc Balancing Capacitors	m-1	m-1/2
Balancing Capacitors	0	0

Table.1. Component requirements per phase of diode clamped &cascaded Multilevel inverters

III. DIODE CLAMPED FIVE LEVEL INVERTER

Fig. 2 shows a five-level diode-clamped converter in which the dc bus consists of four capacitors,C_1 ,C_2 ,C3 , and C_4 . For dc-bus voltage V_{dc} , the voltage across each capacitor is$V_{dc/4}$,and each device voltage stress will be limited to one capacitor voltage level through clamping diodes.

To explain how the staircase voltage is synthesized, the neutral point *n* is considered as the output phase voltage reference point. There are five switch combinations to synthesize five level voltages across *a* and *n*.

Output Voltage	Switching sequence							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a1}^1	S_{a2}^1	S_{a3}^1	S_{a4}^1
0	1	1	0	0	1	1	0	0
Vdc/4	0	1	1	1	1	0	0	0
Vdc/2	1	1	1	1	0	0	0	0
-Vdc/4	0	0	0	1	1	1	1	0
-Vdc/2	0	0	0	0	1	1	1	1

Table.2 Switching states for diode clamped 5 level inverter

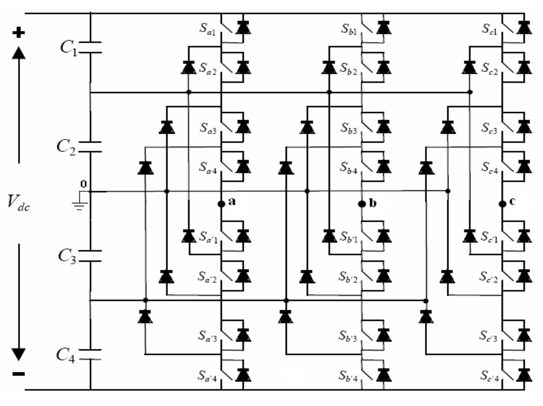


Fig. 2. Configuration of three-phase diode clamped Five Level Inverter (C 5LI)

IV. CASCADED FIVE LEVEL INVERTER

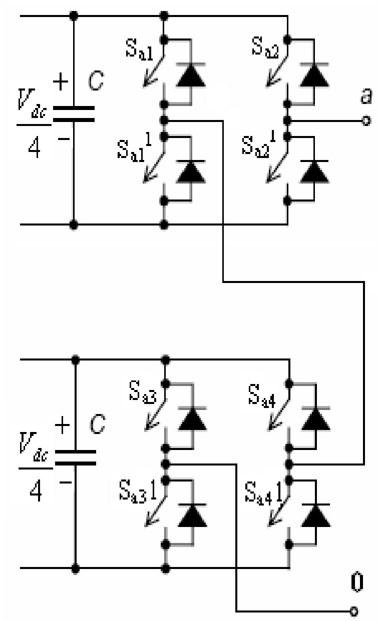


Fig.3. Configuration of single-phase Cascaded Five Level Inverter (C 5LI)

Output Voltage	Switching sequence							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a1}^1	S_{a2}^1	S_{a3}^1	S_{a4}^1
0	1	1	0	0	0	0	1	1
Vdc	1	0	0	0	0	1	1	1
2Vdc	1	0	1	0	0	1	0	1
-Vdc	0	1	1	1	1	0	0	0
-2Vdc	0	1	0	1	1	0	1	0

Table.3. Switching states for Cascaded 5 level inverter

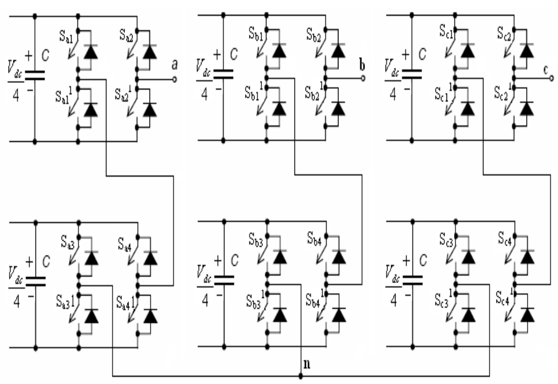


Fig. 4. Configuration of three-phase Cascaded Five Level Inverter (C 5LI)

The advantages and disadvantages of cascaded H-bridge inverter is as follows:

V. MODULATION STRATEGIES FOR MULTILEVEL INVERTERS

A number of modulation strategies are used in multilevel power conversion applications. They can generally be classified into three categories:

- fundamental Frequency switching strategies
- Space Vector PWM strategies
- Carrier based PWM strategies

Of all the PWM methods for cascaded multilevel inverter, carrier based PWM methods and space vector methods are often used but when the number of output level is more than five, the space vector method will be very complicated with the increase of switching states. So the carrier based PWM method is preferred under this condition in multilevel inverters. This paper focuses on carrier based PWM techniques which have been extended for use in multilevel inverter topologies by using multiple carriers.

VI. CARRIER BASED PWM METHODS BASED ON CFD COMBINATION USING SPWM

This paper presents three COPWM methods that utilize the CFD of vertical offsets among carriers. They are: COPWM-A, COPWM-B, COPWM-C. The above three methods are simulated in this work. For comparison purposes, a non overlapping Sub Harmonic PWM(SHPWM) method is also presented in this work.

A. COPWM-A strategy using SPWM

The vertical offset of carriers for five level inverter with COPWM-A method is illustrated in Fig.5. It can be seen that the four carriers are overlapped with other and the reference sine wave is placed at the middle of the four carriers.

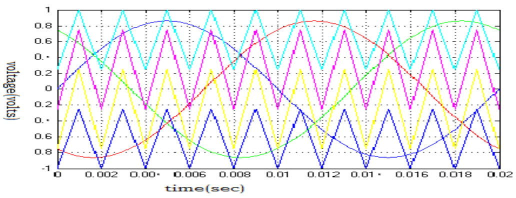


Fig.5. Carrier arrangement for COPWM-A using SPWM strategy

B.COPWM-B strategy using SPWM

Carriers for five level inverter with COPWM-B method are shown in Fig.6.

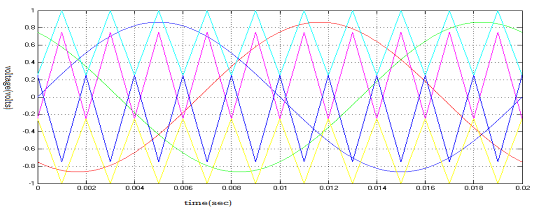


Fig.6.Carrier arrangement for COPWM-B SPWM strategy

C. COPWM-C strategy using SPWM

Carriers for five level inverter with COPWM-C method are shown in Fig.7.

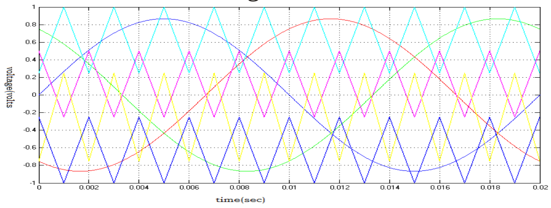


Fig.7. Carrier arrangement for COPWM-C using SPWM strategy

D. **Phase Disposition** *strategy using SPWM*

In phase disposition PWM method all the carriers are in phase. In this method all the carriers are displaced without overlapping. Fig.9. demonstrates the sine-triangle method for a three-level inverter.

m = A /(2 A) (3)*

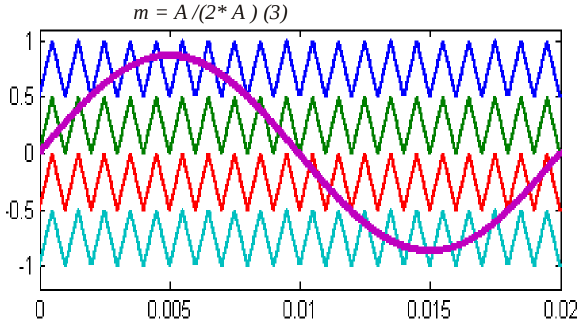


Fig.8. Carrier arrangement for PD using SPWM strategy

VII. Carrier based PWM methods based on CFD combination using Modified SVPWM

In the SPWM scheme for two-level inverters, each reference phase voltage is compared with the triangular carrier and the individual pole voltages are generated, independent of each other [6]. To obtain the maximum possible peak amplitude of the fun common mode voltage, Voffset1, is added to the reference phase voltages [9, 1], where the magnitude of Voffset1 is given by

$$V_{offset1} = \frac{-(V_{\max} + V_{\min})}{2} \quad \text{--(1)}$$

A. COPWM-A strategy using modified SVPWM

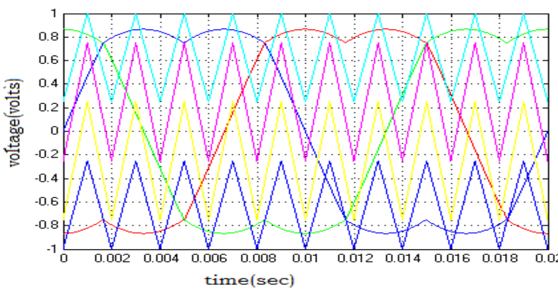


Fig.9.Modified reference voltages for a 3-phase five-level COPWM-B SVPWM scheme

B. COPWM-B strategy using modified SVPWM

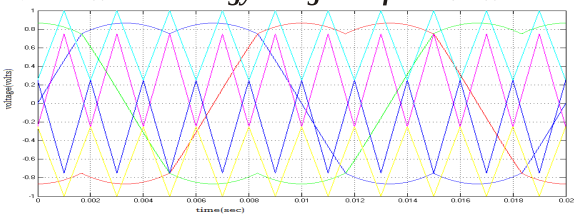
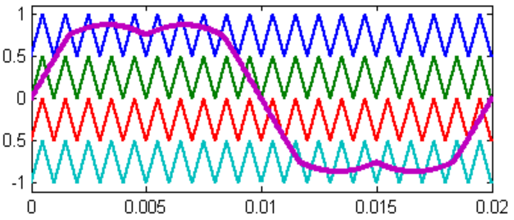


Fig.10.Modified reference voltages for a 3-phase five-level COPWM-B SVPWM scheme



C. COPWM-C strategy using modified SVPWM

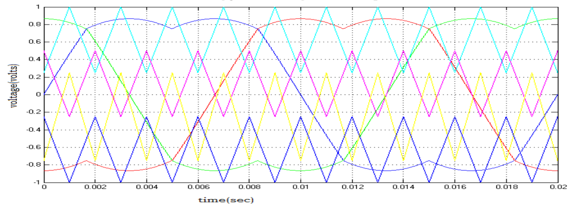


Fig.11.Modified reference voltages for a 3-phase five-level COPWM –C SVPWM scheme

D. **Phase Disposition** *strategy using modified*

Fig.12. Modified reference voltages for a 3-phase five-level PD –SVPPWM scheme

VIII. SIMULATION RESULTS FOR SPWM AND MODIFIED SVPWM STRATEGIES FOR BOTH DIODE CLAMPED AND CASCADED INVERTERS

The diode clamped and cascaded three phase five level inverter is modeled in SIMULINK using power system block set. Switching signals for cascaded multilevel inverter are generated using SPWM and modified SVPWM techniques.

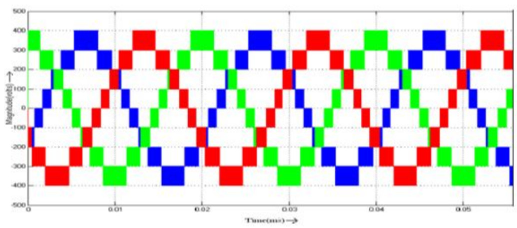


Fig.13.Output voltage generated by COPWM-A,B,C & PD SPWM strategy for diode clamped 5LI

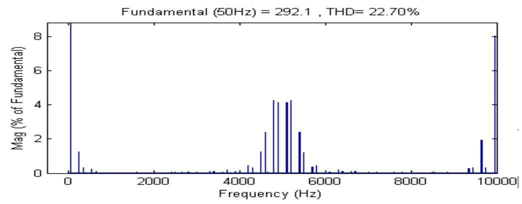


Fig.14.FFT plot for COPWM-A SPWM strategy

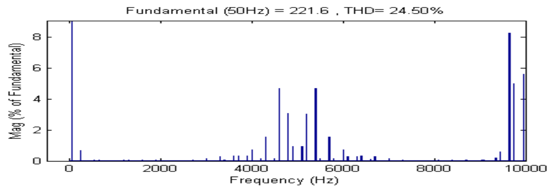


Fig.15. FFT plot for COPWM-B SPWM strategy

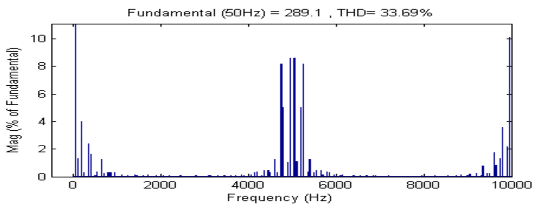


Fig.16. FFT plot for COPWM-C SPWM strategy

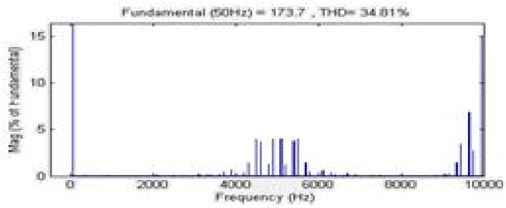


Fig. 17.FFT plot for PD SPWM strategy

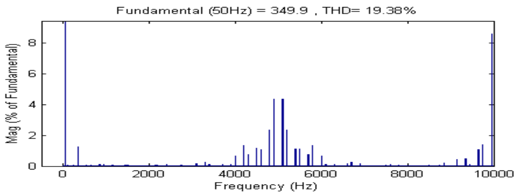


Fig.18. FFT plot for COPWM-A SVPWM strategy

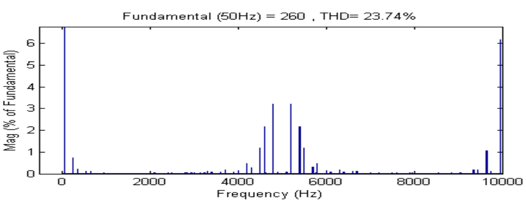


Fig.19. FFT plot for COPWM-B SVPWM strategy

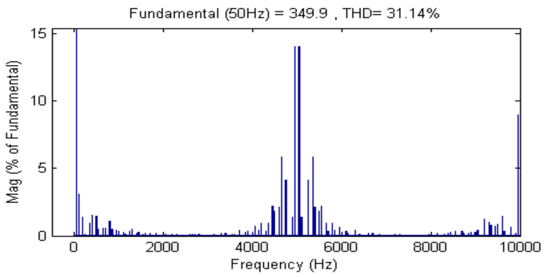


Fig20. FFT plot for COPWM-C SVPWM strategy

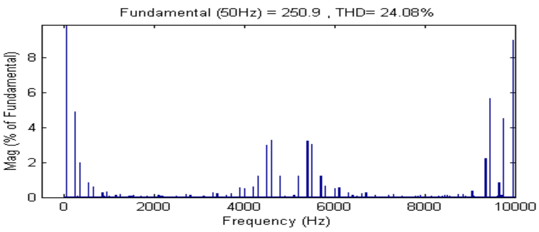


Fig.21. FFT plot for PD SVPWM strategy

IX. SIMULATION RESULTS FOR CASCADE 5LI

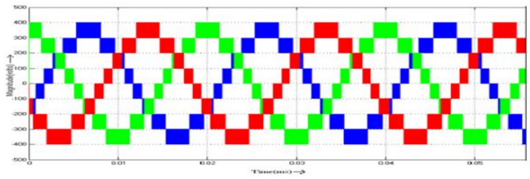


Fig.22. Output voltage generated by COPWM-A,B,C & PD SPWM strategy for Cascaded 5LI

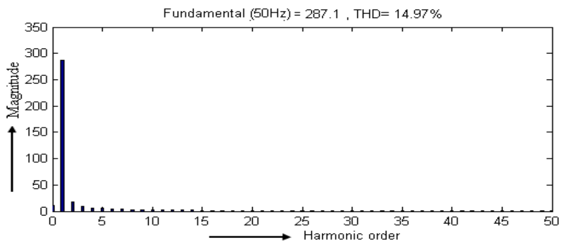


Fig. 23.FFT plot for COPWM-A SPWM strategy

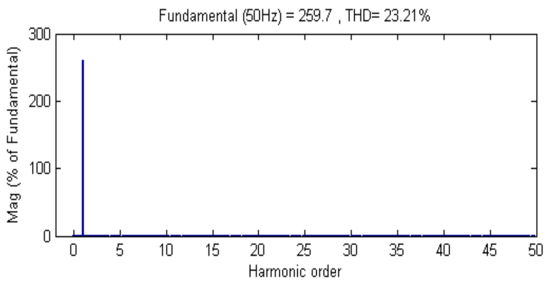


Fig. 24. FFT plot for COPWM-B SPWM strategy

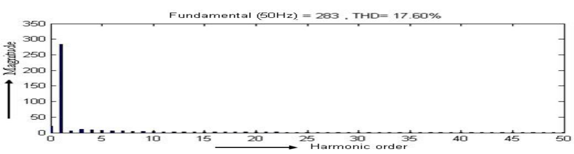


Fig. 25. FFT plot for COPWM-C SPWM strategy

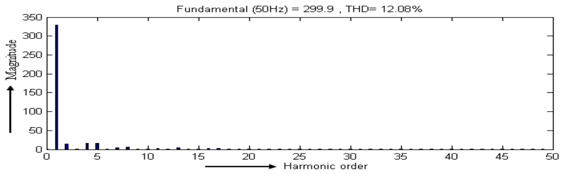


Fig. 26.FFT plot for PD SPWM strategy

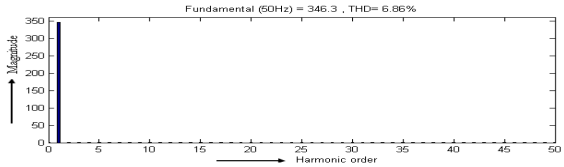


Fig.27. FFT plot for COPWM-A SVPWM strategy

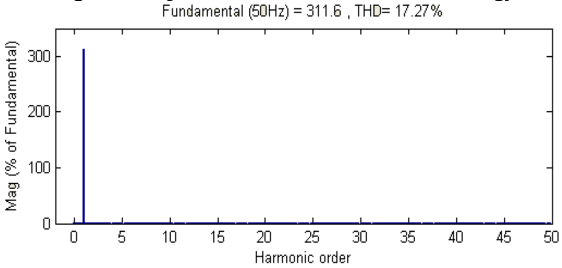


Fig.28. FFT plot for COPWM-B SVPWM strategy

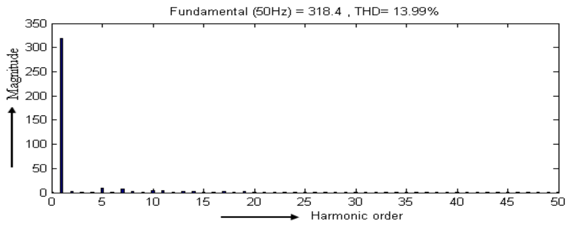


Fig.29. FFT plot for COPWM-C SVPWM strategy

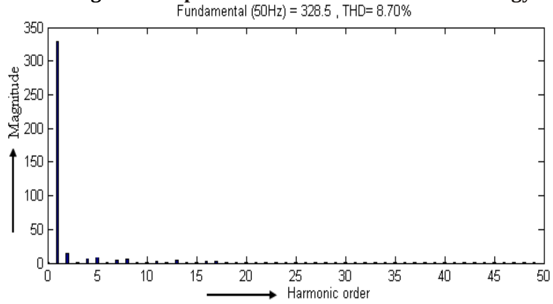


Fig.30. FFT plot for PD SVPWM strategy

X. COMPARISON OF THD FOR DIFFERENT PWM TECHNIQUES OF CASCADED 5LI

Input voltage = 400v
Switching frequency = 10 KHz
Modulation index = 0.866

PWM Techinque	**SPWM**		**Modified SVPWM**	
	Funda mental voltage	%THD	Funda mental voltage	%TH
COPWM-A	292.1	22.70	349.9	19.38
COPWM-B	221.6	24.50	264.8	23.74

COPWM-C	289.1	33.69	349.9	31.14
PD	245.8	34.81	250.9	24.08

Table .4. Summary of simulation results for three-phase diode clamped 5LI

PWM Tenchinque	**SPWM**		**Modified SVPWM**	
	Funda mental voltage	%THD	Funda mental voltage	%THD
COPWM-A	287.1	14.97	346.3	6.86
COPWM-B	259.7	23.21	311.6	17.27
COPWM-C	283	17.60	318.4	13.99
PD	299.9	12.09	328.5	8.70

Table .5. Summary of simulation results for three-phase cascaded 5LI

XI. HARDWARE DESCRIPTION

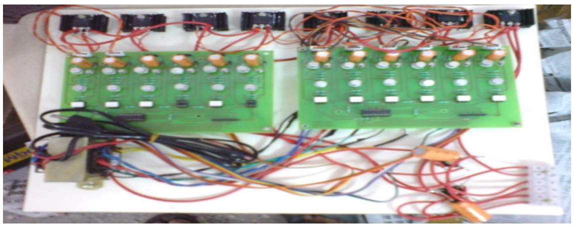


Fig.31 Cascaded single-phase 5-level Inverter Hardware Kit

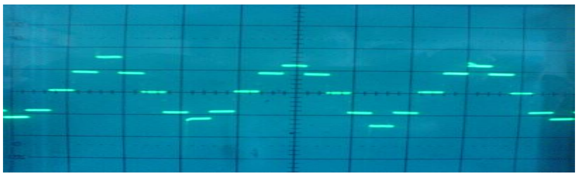


Fig .32 Output voltage for single-phase cascade 5 level inverter

XII. CONCLUSION

The diode clamped and Cascaded 3-phase 5LI are simulated for sinusoidal PWM technique and modified space vector PWM technique with COPWM-A, COPWM-B, COPWM-C and PD PWM strategies. The simulation results with harmonic spectrum are presented, and in this paper it is concluded that modified reference SVPWM using COPWM-C technique has given good harmonic spectrum with fundamental (346.3) and THD (6.86%) when compared with other techniques. Compared with diode clamped and cascade inverters cascaded inverter has given good fundamental output voltage with reduced THD.

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