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Editorial

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EDITORIAL

Editor- in-Chief
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I am happy to announce the publication of the inaugural issue of International Journal of Electronics and Electrical Engineering (IJEEE) which provides the latest industry findings useful to academicians, researchers, and practitioners regarding the latest developments in the areas of science and technology of machines, imaging, and their related applications, systems, and tools. This journal contains unique articles of original, innovative research in the area of computer science, education, security, government, engineering disciplines, software industry, vehicle industry, medical industry, and other fields. IJEEE is intended as an effective medium to spread the results of high quality applied research and fundamental, theoretical, particularly in the domain of computer vision and image interpretation. For this issue, a number of good quality articles have been received from various authors. Out of more than fifty papers, we have accepted selected papers after peer review process, for publication in this inaugural issue of IJEEE.

The first paper entitled "A High Performance DDR3 SDRAM Controller" by Shabana Aqueel and Kavita Khare has presented the implementation of compliant DDR3 memory controller. It discusses the overall architecture of the DDR3 controller along with the detailed design and operation of its individual sub blocks, the pipelining implemented in the design to increase the design throughput.

In the second paper entitled "EARM: An Efficient and Adaptive File Replication with Consistency" by K. V. K. Chaitanya and Smt. S.Vasundra have presented an Efficient and Adaptive file Replication and consistency Maintenance (EARM) that combines file replication and consistency maintenance mechanism that achieves higher query efficiency in file replication and consistency maintenance at a low cost. Instead of accepting passively file replicas and updates, each node determines file replication and update polling by adapting to time-varying file query and update rates.

The next paper entitled "Dynamic Voltage Scaling with Reduced Frequency Switching and Preemptions" by Arya Lekshmi Mohan and Anju S.Pillai investigates the main challenges of Dynamic Voltage Scaling

are increased number of preemptions and frequency switching. A part of dynamic energy as well as CPU time is lost due to these processes. To limit such processes, an algorithm is proposed which reduces both unwanted frequency switching and preemptions.

The fourth paper entitled “Syncing and Integrating Windows and Mac OS in the Solitary Macintel, Power PC and x86 Intel Environments” by C. Infant Louis Richards and T. Yuva presents a simple but effective solution to use various operating systems without hardware being a hindrance in developing the solution.

The next paper entitled “Audio Retrieval Using Multiple Feature Vectors” by Vaishali Nandedkar have presented a quick search method can quickly detect known sound in a long audio stream. They have used four features for extracting the audio from the database, use of this multiple features increase the accuracy of the audio file which we are retrieving from the audio database.

The sixth paper entitled “Determination of Characteristic Frequency for Identification of Hot Spots in Proteins” by Yashpal Yadav and Sulochana Wadhwani have proposed an alternative approach for determination of characteristic frequency for hot spot identification is proposed using power spectral density (PSD).

The next paper entitled “Proposed design for circular antenna and half ring antenna for UWB Application” by Minal Kimmatkar et. al. have proposed the circular patch antenna and half ring patch antenna are simulated using HFSS. The proposed antennas have the advantages of small size, easy fabrication and simple construction.

Shambhavi S et. al in their paper entitled “Multiplier Based On Add And Shift Method ByPassing Zero” have proposed a low-power structure for shift-and-add multipliers is proposed. The architecture considerably lowers the switching activity of conventional multipliers. The modification to the multiplier which multiplies A by B include the removal of the shifting register, direct feeding of A to the adder, bypassing the adder whenever possible, using a ring counter instead of a binary counter and removal of the partial product shift. The architecture makes use of a low-power ring counter proposed in this work. The proposed multiplier can be used for low-power applications where the speed is not a primary design parameter.

The ninth paper entitled “VLSI Architecture OF Parallel Multiplier– Accumulator based on RADIX-2 Modified Booth Algorithm” by M.V.Sathish and Sailaja have presented proposing method CSA tree uses

1's-complement-based radix-2 modified Booth's algorithm (MBA) and has the modified array for the sign extension in order to increase the bit density of the operands.

The next paper entitled "MBER Space Time Equalization assisted Multiuser Detection" by Yogeshwary. B. H. and et. al. have proposed a novel minimum bit-error rate (MBER) space–time-equalization (STE)-based multiuser detector (MUD) is proposed for multiple-receive-antenna-assisted space-division multiple-access systems.

The eleventh paper , "A Strategic Review on Growth of InP on Silicon Substrate for Applications in High Frequency RF Devices", written by S Umesh. P. Gomes et.al has presented a review on the advances in InAlAs/InGaAs High Electron Mobility transistors (HEMT) over silicon substrates used in high frequency and low noise applications.

The next paper entitled "Study of Optimal Design of Low Pass Block Digital Filter" by Neha Gupta and Lillie Dewan have compared the design of low pass optimal block digital filter is compared with traditional low pass overlap-save block digital filter.

The next paper entitled "Bit-Level Systolic Architecture for a Matrix-Matrix Multiplier" by M.N. Murty et. al. have proposed a serial-parallel multiplier designed to achieve precision with 4 bits. This multiplier is configured to accept and produce unsigned or signed two's complement numbers.

The last paper in this issue entitled "Study on Performance Analysis of CMOS RF front-end circuits for 2.4GHz Wireless Applications" by M.Sumathi and S.Malarvizhi have presented a low voltage design concepts and new CMOS front-end circuits for 2.4GHz wireless applications. The performances of these circuits are analysed and compared with other existing structures using TSMC 0.18-μm CMOS technology scale. They also highlight the design trade-offs between impedance matching, power gain and noise figure of low-noise amplifiers.

I wish the reader shall get immense benefit out of the research publication. I welcome the author to contribute more articles in the future issues of IJEEE.

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