Summer 6-30-2012

Proceeding of International Conference on Electronics and Communication Engineering ICECE- 2012

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Editorial

Innovation in Communication Engineering is happening at an incredible pace. Network technologies are multiplying faster than ever; subscribers are demanding more and forgiving less. As people use mobile broadband wherever they are and whenever they want, demand for services fluctuates throughout the day, creating wildly changing traffic patterns. To meet these dynamic market demands takes a new way of looking at communications technology and end-user expectations. Mobile communications is one of the fastest growing industries in history. It continues to deliver new ways to stay in touch, from basic mobility to the social networking and video-based services of today and tomorrow. Innovation has driven the industry's success. As an industry, communications has shown fantastic innovation, most recently in developing higher bit rates and greater efficiency in the air interface as we move from 3G to 4G and beyond. The industry has done a good job in building networks that can support the new communications experience. But operator revenue has not grown in line with the explosion in smartphone-generated traffic. We need to pick up the pace of innovation. We need to find new ways to help operators better serve their customers and realize the value of their investments, not leaving it all to the over-the-top players such as Skype.

The wireless communications industry is highly standardized, making innovation more challenging. Infrastructure vendors can find it very challenging to differentiate their products. However, with those challenges come opportunities. One is to build the portfolio of patents that is deemed essential for all vendors. Two is to differentiate around vendor-specific areas not covered by the standard. Three is to be in a leadership position to evolve and re-invent the communications industry to better serve operators and their customers.

There is also a strong and growing commitment to cooperating with small and start-up companies, which are also expected to bring a stream of innovation into Nokia Siemens Networks. Such projects are complemented by collaborative research initiatives with operators around the world. Emerging markets have been leading the charge in raising awareness of the potential of TD-LTE, especially in China, where China Mobile sees it as a natural evolution from its existing TDD-based networks. The operator currently has large scale trials in many cities, with In India, where fixed broadband penetration is below 1%, operators aim to complement 3G with TD-LTE. New operators, such as RIL, may also provide TD-LTE in India. Commercial network launches are expected as early as the end of 2011 in countries spanning all continents. There is further operator interest in using TD-LTE as an additional carrier to augment capacity in existing networks, including FDD-LTE, and also as an alternative for rural fixed line broadband.

The conference designed to stimulate the young minds including Research Scholars, Academicians, and Practitioners to contribute their ideas, thoughts and nobility in these disciplines of engineering. It's my pleasure to welcome all the participants, delegates and organizer to this

international conference on behalf of IOAJ family members. We received a great response from all parts of country and abroad for the presentation and publication in the proceeding of the conference. I sincerely thank all the authors for their invaluable contribution to this conference. I am indebted towards the reviewers and Board of Editors for their generous gifts of time, energy and effort.

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Image Compression – Overview of Various Techniques and their VLSI Architectures

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Abstract **-** Image compression is a key image processing technique pervasively used in area of communication, archives satellite imagery, medicine, digital library etc. This paper aims to glimpse through the various techniques adopted for compression and real-time constraints of the VLSI architectures when implemented in hardware with speed, power, area and other optimizations. The strengths and the shortcomings of them are briefed. Other issues like scan methods, border processing and metrics are also dealt.

Keywords **-** *image compression; real time constraints; optimization; VLSI architecture; border processing; metrics*

I. INTRODUCTION

Storage of voluminous data base like digital photography, medical records, legal documents and transmitting them with high fidelity in an unprocessed manner is an preposterous process because of the pervasive use of interactive multimedia applications like videoconferencing, telemetry etc. The panacea to these challenges - channel bandwidth, transmission of high quality image over fading channel, optimizing rate distortion over complete range of rate is image compression. It also allows for incorporating robust coding techniques to withstand transmission error and security of data through encryption. It enables hardware implementations to meet real time VLSI constraints like low power, less area and high speed. Progressive transmission provides quality and resolution scalability to the communication system. Region of Interest (ROI) coding in image compression system enables faster perusal of data by compressing and encoding certain regions of image and remaining part of image to be dealt at a slower pace.

Compression is reducing the amount of data to represent an image by removing the redundancies in the data. When an information is represented by two different lengths of data,-one very shorter, say B_0 than the other say B_1, then

$$\text{Compression ratio (CR)} = B_0 / B_1 \qquad (1)$$

$$\text{Data Redundancy} = 1 - \frac{1}{CR} \qquad (2)$$

Compression may of two types (a) information preserving one called Lossless and (b) Lossy. In digital images basically three types of redundancies occur – coding redundancy, inter pixel redundancy and psycho visual redundancy. Once image is compressed the communication channel should represent the information as compactly as possible. The minimum length of code is given by Shannon's First theorem that states that nth extension of a zero memory source can be coded with fewer average bits than the unextended source itself [1].

II. IMAGE COMPRESSION MODEL

The Image compression for still images is standardized by ISO and CCITT as Joint Photographic Experts Group (JPEG) and the JPEG2000 with better performance. Both standards have the same basic modules – transform, quantization and entropy coding with rate distortion control. Using JPEG image is divided into

- Smaller 8X8 sub images (depending on the transformer's size) then
- DC level shifted by subtracting $2n^{-1}$ from coefficients (Pixels). 2^n is the maximum gray levels

- Color images undergo Intra component transform from RGB to YC_bC_r .
- Intercomponent transform is done using DCT which have good information packing property when compared to Haar, Hadamard-Walsh and Discrete Fourier Transform (DFT).
- Scalar quantization
- Entropy coding using run length coding.

Using JPEG2000 image is divided into

- DC level shifted color images undergo Intra component transform from RGB to YC_bC_r .
- Divide into smaller tiles (facilitates ROI coding and reduces hardware)
- Intercomponent transform is done using Lifting based Discrete Wavelet Transform which deco relate data without blocking artifacts that happen with DCT
- Scalar quantization
- Entropy coding using Embedded Block coding with optimized truncation (EBCOT) [2].

Both standards have bit stream layering and packetising before putting data to channel. Reconstruction is a reverse process.

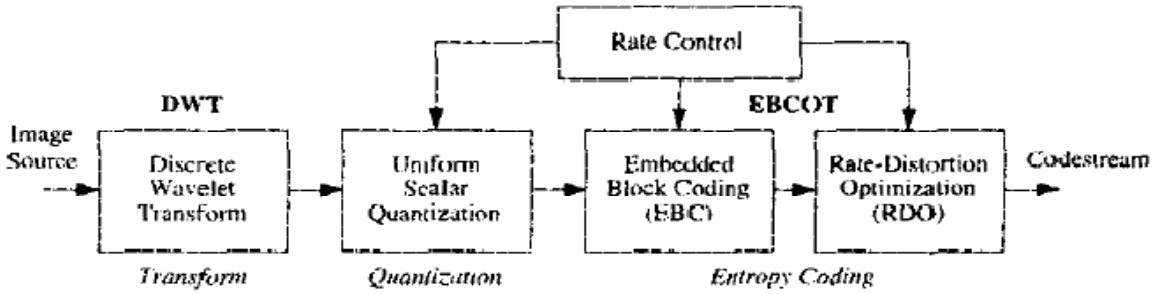


Fig.1 : JPEG2000 standard compression model

III. LOSSLESS COMPRESSION TECHNIQUES

Lossless compression is used for high fidelity applications like medical documents where minute details form the pathological features, legal documents , satellite imagery and so on. It produces a low compression rate from 2:1 to 10:1.Following are some of the techniques:

A. Run length coding

In a sequential data if a pixel(X) is repeated several times it is represented as (X, run length) where run length is the no. of times X is repeated consecutively in the data

Eg. If input data stream is XXXXXYYYYZZZZZZZ it is encoded as (X,5), (Y,4),(Z,7). If 8 bit data and 8 bit code for run length used compression rate is $13*8/6*8 \approx 2:1$

B. Variable length coding

Depending on the probability of the pixel occurrence, highly probable pixel is encoded using shorter code than lower probable ones. This method is used in JPEG for entropy coding.

C. Huffman Coding

This method uniquely codes each pixel with a code. It does not need any dictionary. It is data dependent. This coder iteratively combines two lower probabilities of pixels arranged in descending order. Encoding is done in a back tracking manner. It is used for luminance imagery In JPEG.

D. LZW-Lempel Ziv Welch coding

Following Shannon's I coding theory, it codes a group of data using a growing dictionary. It does not require a piori knowledge of source symbols.

E. Bit-plane coding

It reduces interpixel redundancy of binary images. M- bit pixels are arranged into M bit planes . Each bit plane represents a bit position. Compression may be

achieved by truncating the least significant biplanes and gray coded bit plane helps in low power compressions . Other coding techniques are predictive coding , area coding .

IV. LOSSY COMPRESSION TECHNIQUES

Lossy techniques provide considerable compression rate of the order 100:1 because quantization is part of it. Image is first transformed and then quantized.

Transforms are used to change the properties of the image into desirable one for further stages. Some of the transforms are

A. *Discrete Fourier transform and Discrete Fourier transform*

Discrete Fourier Transform(DFT) and Discrete cosine Transform transforms image pixels in spatial domain(x,y) to frequency domain(u,v)

$$F(u,v) = \frac{1}{MN}\sum_{u=0}^{M-1}\sum_{v=0}^{N-1} f(x,y)e^{j2\pi(ux/M+vy/N)} \qquad (3)$$

DCT is computed as

$$F(u,v) = \alpha(u)\,\alpha(v)\cos\left[\frac{(2x+1)u\pi}{2N}\right]\cos\left[\frac{(2y+1)v\pi}{2N}\right] \qquad (4)$$

Where $\alpha(u) = \begin{cases} 1/\sqrt{n} & \text{FOR=0} \\ \sqrt{(2/N)} & \text{for u=1 to N-1} \end{cases}$

and image dimension is MxN.

DFT cannot have frequency localization along with time localization. Another shortcoming is the blocking artifacts present in DCT due boundary between sub images and ringing artifacts in Quantized DFT coefficients due to Gibb's Phenomenon.

B. *Discrete Wavelet transform*

Discrete Wavelet Transform maps image from spatial domain into time frequency domain using small oscillatory waves called wavelets. They decorrelate image by separable or non separable transform to get wavelet coefficients and scaling coefficients [1].

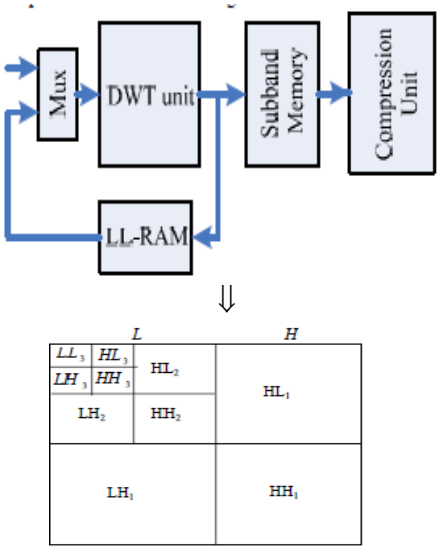


Fig. 2 : 3-level sub band decomposition using DWT in a compressor

Wavelet coefficients:

$$W_{\psi}^{i}(j,m,n) = \frac{1}{MN}\sum_{x=0}^{M-1}\sum_{y=0}^{N-1} f(x,y)\psi^{i}_{j,m,n}(x,y) \qquad (5)$$

where i={Horizontal, Vertical , Diagonal}, j-scale and Ψ is wavelet function φ is scaling function

Scaling coefficients by

$$W_{\phi}(j,m,n) = \frac{1}{MN}\sum_{x=0}^{M-1}\sum_{y=0}^{N-1} f(x,y)\phi_{j,m,n}(x,y) \qquad (6)$$

The first decomposition, which consist of sub bands HL1(horizontal), HH1(diagonal) and LH1(vertical), are stored in the memory blocks labeled *HL1*, *HH1*, and *LH1*, respectively. Then, the compression unit is informed to read these memory blocks. The compression unit can read each sub band memory block code-block by code-block for EBCOT. The compression unit applies compression algorithm on each code-block independently. The compression unit first reads contents of *HL1*, then *HH1*, and last *LH1*. While, the LL1 sub band coefficients, which are stored in the RAM, are scanned by the DWT unit for further decomposition.

Sub bands of the second decomposition HL2, HH2, and LH2, are stored in the sub band memory blocks labeled *HL2*, *HH2*, and *LH2* and higher sub bands on the indicated memory blocks *HL3*, *HH2*, and *LH3* [3].

C. Other transforms

Apart from the above other transforms like Walsh Hadamard transform, Haar and Karneuhen-Loevue transform (KLT) may also be used. KLT has the most optimal information packing property but computation of Eigen vector and covariance matrix for large real time image data is cumbersome. So DWT is the most preferred in its recent version of Lifting scheme.

D. Quantisation

The considerable reduction in redundant data is due this step. It maybe scalar if it act on single pixel or Vector if it act on a group of pixels.[4]

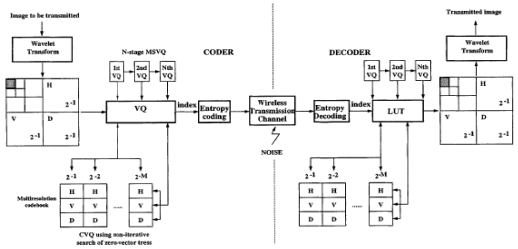


Fig. 3 : Wavelet Vector quantization in compression model

V. CODEC ALGORITHMS

Aiming to increase performance of compressor and expander several algorithms like Embedded Zero tree wavelet coding (EZW), Set partitioning in hierarchical Tree (SPHIT), Embedded Block coding with optimized Truncation (EBCOT) evolved.

A. EZW

This algorithm developed by Shapiro involves identifying zero quad trees using threshold.

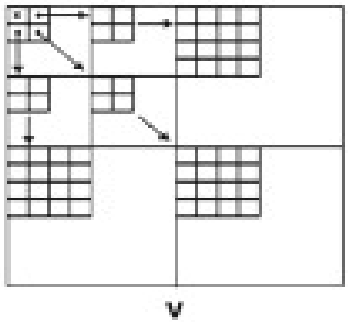


Fig. 4 : Tree structure

Zero tree is a tree arrangement of coefficients in which every parent pixel has 4 children pixels in lower scales. EZW uses several dominant passes and subordinate passes in dominant pass by iteratively reducing the threshold and zero trees are identified. In subordinate pass encoding only non-zero trees is done. This enables progressive transmission for better quality of reconstruction.

B. SPHIT

SPHIT is based on quad tree formation in image blocks and transmitting the information about significant pixels that above a threshold. It uses three lists List of insignificant pixels(LIP), List of insignificant sets(LIS), list of significant pixels(LSP)[7].

C. EBCOT

EBCOT process image as bit planes in two phases - context formation and arithmetic coding. Each bit of the plane is checked for its context pairs using surrounding pixels for the arithmetic coder to encode in next [8].

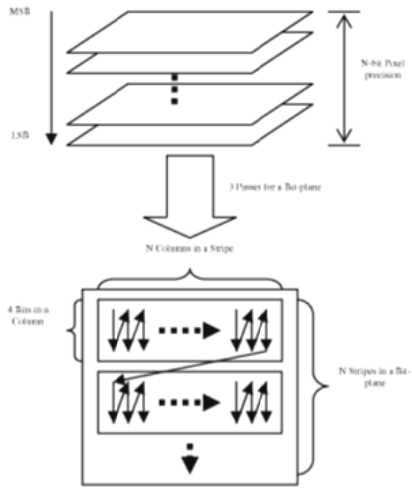


Fig. 5 : bit plane structure and scanning for EBCOT

D. Scan methods

For ease of processing Zig-zag and Mortan scan are used. Other scan method is raster scan [5].

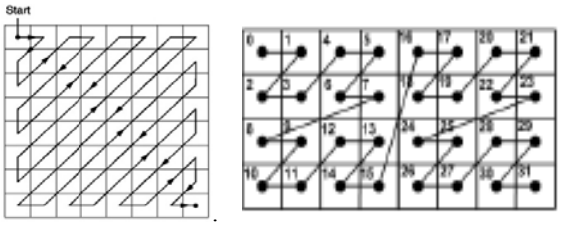


Fig. 4 : Zigzag scan and Morton scan of quantized coefficients

E. Borderprocessing

At boundaries of images to have perfect reconstruction

- Periodic extension
- symmetric extension and
- zero padding methods are used

F. Pretreatment

By denoising using fuzzy C-means and Kohonen's network the compression ratio and reconstructed quality is improved [6].

VI. VLSI ARCHITECTURES

This section addresses the hardware requirements and techniques that may be applied for its implementation when the key concern is reducing power and resources, thereby the die area and cost of the chip. Several circuit level and system level design are explored in brief.

A. VLSI architecture of codec algorithms

a) SPHIT:

It requires many FIFOs for LIS, LIP AND LSP in addition to memory, control logic and address generator. The FIFO operate in a parallel manner. Fixed order architectures are available.

b) EBCOT:

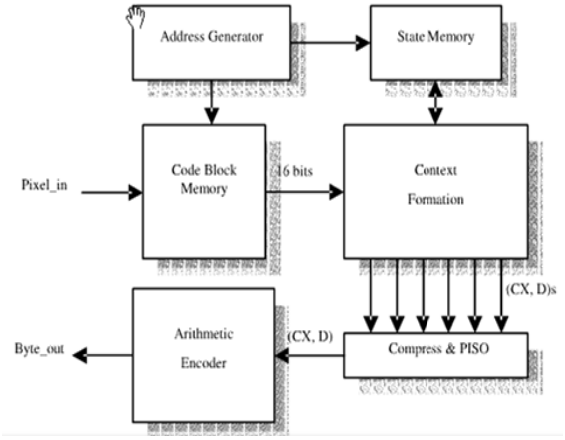


Fig. 6 : Architecture of EBCOT

Input pixels are stored in code block memory. Upon the addressing from address generator biplane of 16 bits are passed to context formation to produce context pairs (CX, D). (CX, D) are compressed in parallel manner and serially sent out to arithmetic encoder for bit stream out. Other skipping methods and memory saving methods are available but this architecture has lesser storage requirements.

B. Transform architectures

a) DCTQ architecture:

quantisation with DCT architecture uses DCT arithmetic module that basically multiplies by shifting [10].

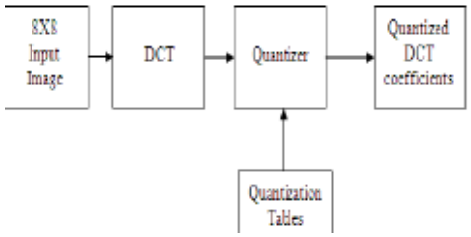
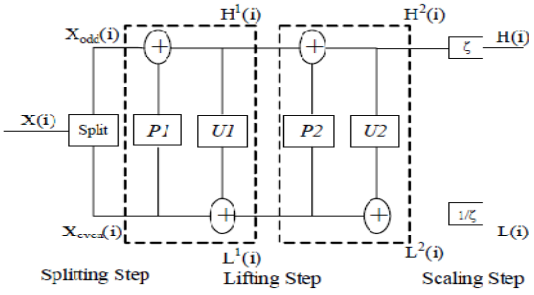


Fig. 7 : DCTQ architecture

b) DWT architecture:

Lifting DWT consists of basic steps:

- Split
- Lifting step
- Scaling step



$$P2=\gamma(1+z) \text{ and } U2=\delta(1+z^{-1})) \quad (P1=\alpha(1+z),\ U1=\beta(1+z^{-1}), \qquad (7)$$

Fig. 8 : DWT architecture.

Various architectures involve parallel, pipelining, folding, flipping and canonic signed digit representation.

C. Circuit-level and device level optimisations:

Multipliers may be implemented using Carry save adders, Ripple carry adders or carry look-ahead adders. Integer multiplications may be simply done by shift left operations. Wallace tree, Booth multipliers and radix multipliers may be used. Of all circuits ripple carry has longer delay than others. Tree adders have high speed but occupy large area. Radix multipliers have complex logic, occupy much area using more power but they

operate faster.Power delay is an important metric for VLSI circuits:

Power delay product=Max delay*Average power dissipation. (8)

Dynamic power dissipation = CV^2f (9)

Where C - load capacitance, V- supply voltage , f- switching frequency.

Low power is achieved by scaling supply voltage, reduction in energy of clock distribution using advanced clocking techniques like Wave pipelining, glitch reduction [12]. Switching activities are reduced in shift and add radix multipliers [11].

Other device level measures to reduce power are using pass transistors to implement basic logic functions resulting in lower gate capacitance and low power dissipation.

Other major component affecting VLSI design is memory. Restricting number of external memory access and using small cache may help in lower design [13].

VII. METRICS

Performance of various coding techniques and algorithms are evaluated using metrics given below

Peak signal to noise ratio (PSNR) PSNR= $20\log_{10}\left[\frac{\max\ pixelvalue}{rmserror}\right]$ db. (10)

Root mean square error (Rmserror):

Rmserror= $\sqrt{\frac{1}{MN}\sum_{i=0}^{m-1}\sum_{j=0}^{N-1}p(i,j)}$ for MxN image.

(11)

Signal to Noise Ratio (SNR):

SNR= $10\ \log\left[\frac{\sum_{i=0}^{M-1}\sum_{j=0}^{N-1}y'^{@}}{\sum\sum(y_{ij}-y'_{ij})2}\right]$ db

Y' is the reconstructed pixel from an expander. Y –input pixel.

(12)

VIII. CONCLUSION

This paper has tried to give the salient features of widely used compression techniques. In reality depending upon the application hybrids of the various transforms and techniques like neural network and MIMO are used for denoising, compression and reconstruction. Often there is a tradeoff made between the area, speed and power optimizations to achieve the target of the application design.

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Dynamic Power Reduction in Hybrid Adders using Transistor Sizing based on Modified Genetic Algorithm

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Abstract **-** A new power reduction method for hybrid adders, using modified genetic algorithm for transistor sizing, has been described in this paper. Transistor sizing plays a crucial role in determining the circuit performance for low power applications. An optimal size of transistor is necessary for providing a better power delay product performance in low power data path circuits. In this work, Hybrid adders are designed with the help of mixed logic structure and their performances analyzed. Further reduction in power and delay in the adders is achieved by optimizing the size of transistor. The modified genetic algorithm is proposed for determining the optimal value of transistor width in Hybrid adders and its power, delay and PDP parameters are compared with the existing work. All simulations are carried out using HSPICE at 90nm technology with BSIM Models.

Keywords **-** *Transistor sizing, power delay product, genetic algorithm, full adders.*

I. INTRODUCTION

Present development in VLSI technology has increased the quantity of transistors in one chip to around two billion. In this complicate production, a main design objective is to limit the power utilization of the chip. Transistor sizing is a significant way for evaluating the performances of the circuits. For fair evaluation, an appropriate size of transistor is required for low power applications. The intention of the optimization is to reduce the power-delay product or the energy utilization. The power and delay based on the transistor size which in turn is proportional to R^n ($w \in R^n$), where n is the transistor count.

As per the literature survey several techniques have been proposed for transistor sizing, like Hybrid Tree Structure, MDE (Minimum Delay Estimation) [5-6], TILOS [7] and ADC (Area-Delay Curve) [8-11]. Because few of the techniques only look a part of space and they are starting size dependent, they cannot assure a global optimization. Thus, this paper attempts to find out a technique assuring the global optimum achievement as well as the short runtime of optimization [4]. Genetic algorithm (GA) is used to resolve this difficulty, which is a power optimization technique. Genetic algorithm has the capability of directing the arbitrary search for a global optimum solution. This technique minimizes the density of exploration for an optimal solution. It is functional in transistor sizing which is a search problem in the huge space. An added advantage of this is parallel implementation in multiprocessors [12].

A technique called Modified Genetic Algorithm (MGA) based on power optimization is proposed in this paper, in which chooses a higher starting group by means of preprocessing for solving the local solution in a genetic algorithm. The presented technique determines the optimized energy needed by modified genetic algorithm.

The reminder of the paper is organized as follows. In section II the literature survey of the power minimization in VLSI based circuits is presented. Section III presents the existing methodology which explains Hybrid Tree Structure and its properties with Genetic Transistor Sizing Algorithm and proposed methodology. Experimental results are given in section IV and Section V concludes the paper with some discussions.

II. PREVIOUS WORK

This section presents the literature survey on the minimization of power consumption in low power VLSI. The power consumption can be reduced in the different abstraction levels.

Massoud Pedram [1] explained the cause for the power indulgence in VLSI processors. Power indulgence in CMOS circuits originates by the following three sources: 1) the leakage current that is

found in the stand- by mode 2) the short-circuit current that is because of the DC path between the provided rails through output transitions and 3) the charging and discharging of capacitive loads throughout logic changes, which is the dominant one.

Jui-Ming Chang *et al.,* [2] presented a novel technique for energy minimization using multiple supply voltages in the integrated circuits. A dynamic programming method is proposed for solving the multiple supply voltage scheduling difficulties in both non pipelined and functionally pipelined data-paths. The scheduling difficulty refers the assignment of a supply voltage level to every operation in a data flow graph so as to reduce the average energy needed for given computation time or throughput constraints or both and it required level converter.

A very valuable method to decrease power consumption is to reduce the supply voltage level for a circuit. If supply voltage is decreased, the circuit delay is increased due to threshold voltage reduction. Chandraskan *et al.,* [3] describes that the balance for the increased delay by shortening critical paths in the data-path with the help of behavioral transformations like parallelization or pipelining. The obtained circuit requires lower average power and meets the total throughput limitation at the cost of enlarged circuit area. Currently, the utilization of multiple supply voltages on the chip is very conspicuous. This has the merits of permitting modules on critical paths to utilize the highest voltage level and permitting modules on noncritical paths to use lower voltage. This technique tends to result in smaller area overhead compared to parallel architectures.

III. METHODOLOGY

In the conventional technique the power reduction in data path circuits is achieved by building the Hybrid tree and the optimization is carried on with the support of genetic algorithm. Initially the Hybrid tree structure is explained and then the genetic algorithm approach for power minimization is provided.

A. Hybrid Tree Structure

Hybrid Tree Structure is a secure and normal technique for the transistor sizing of circuit and the optimization of the power-delay product. The algorithm is presented by Chang e*t* al. [12-13].This algorithm starts with the primary value set of transistor sizes. Then the scaling procedure is performed transistor by transistor for a number of iterations. In this method, θ_k represents the circuit energy consumed in kth iteration and w_j (T_i) represents the width of the ith transistor at step j. For each optimization iteration, single transistor is tuned on for minimal power-delay product in 2×m steps with a step resolution of $\pm\Psi$[15].

The scaling procedure is carried on until the difference in two consecutive iterations is lesser than the provided error ε.

Greater than single iterations may be required since every time a new transistor is sized in the current run. The further transistor sized in the earlier run may no longer continue their optimality. Two factors are taken into account in the process to speed up the operation as follows.

Initially, the equivalent PMOS and NMOS in a corresponding pair are optimized in consecutive runs since the output transitions of the node determined by one transistor depends on the driving capability of its complementary counterpart. Next, the series transistors or parallel transistors of the identical type that source current to, or sink current from the related nodes have identical size and can be optimized in tandem **[**14,15].

B. Transistor sizing Optimization using Genetic Algorithm

An adaptive heuristic search method is Genetic algorithm for optimization problem. The fundamental attitude of this technique has been described by Charles Darwin in his survival of the fittest theory. The evolution generally begins from a population of randomly created individuals and occurs in generations. In every generation the fitness of each person in the population is estimated, multiple individuals are stochastically chosen from the present population, and adapted to form a new population. The new population is then applied in the subsequent run of the procedure. Usually, the algorithm ends when either a maximum number of generations have been reached, or an acceptable fitness level has been occurred for the population [15].

Initially, circuit transistors are grouped by rules which proposed in [4]. As represented, this technique uses the similar position transistor regulation for combination in symmetric circuits. This rule provides that, transistors that have similar position in the circuit, not series and parallel, can be optimized with the same size since two paths will have identical resistance and similar drivability. Thus delay of both the paths are necessary to be similar, or two identical paths having dissimilar operations in which one of them acts as a critical path that limits circuit process. This technique minimizes the grouping count in addition to the transistor sizing runtime [4]. After combining, the circuit structure has been considered as in Figure 1. and the sizes of transistor or the k_i coefficients comprises the chromosome genes. Finally the values of transistor sizes are considered as a real number.

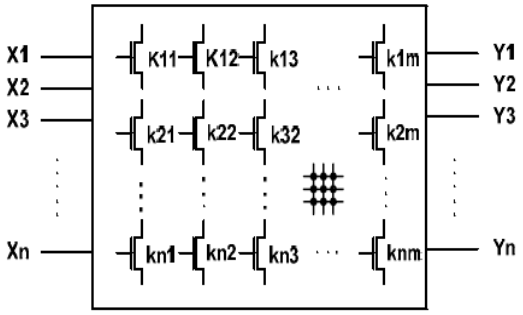


Fig. 1 : Two dimensional structures of circuits. [17]

The fitness function can consider every optimization attribute or a mixture of them. The energy utilization was optimized in [16]. In the starting population, the k_i values have been created at random and a new population has been altered by crossover and mutation process.

III. PROPOSED METHOD

In the proposed technique the modified genetic algorithm is used for the power reduction. The power reduction in data path circuits will be efficient when the modified genetic algorithm is used.

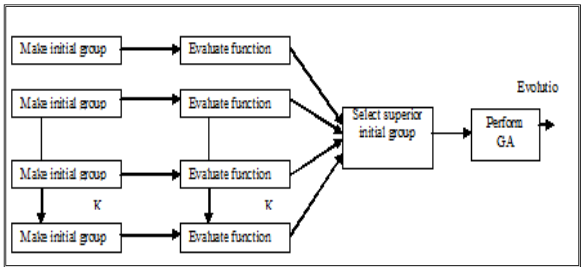
A. Modified Genetic Algorithm

The local minima problem of genetic algorithm is obtained from the choice of the starting generation. For solving this difficulty, Modified genetic algorithm preprocesses starting generations which are dependent on a master / slave technique. Modified genetic algorithm uses k - slave generation and each slave generation is estimated appropriately. The master processor places the most superior group to starting generation and picks over the other group. The master processor executes genetic algorithm by choosing a better starting group.

A master processor that saves whole slave group in its individual memory is in accusation of choosing the starting group. And k - slave processors are responsible for estimating the purpose of starting groups.

In the genetic algorithm procedure, a bubble sort technique is utilized for reproduction. It chooses according to the ranking of each individual. The superior half ranks of the individuals are reproduced and new individuals are created by crossover of the earlier individuals. So, the reproduction results in new individuals with the help of crossover and upper alive individuals together make the new generation. Figure 2 a & b. shows the flow chart of modified genetic algorithm technique.

The proposed technique is replacing modified genetic algorithm (MGA) instead of the Genetic Algorithm (GA), which chooses a better starting group by means of preprocessing for solving the local result in a genetic algorithm(refer figure 2).



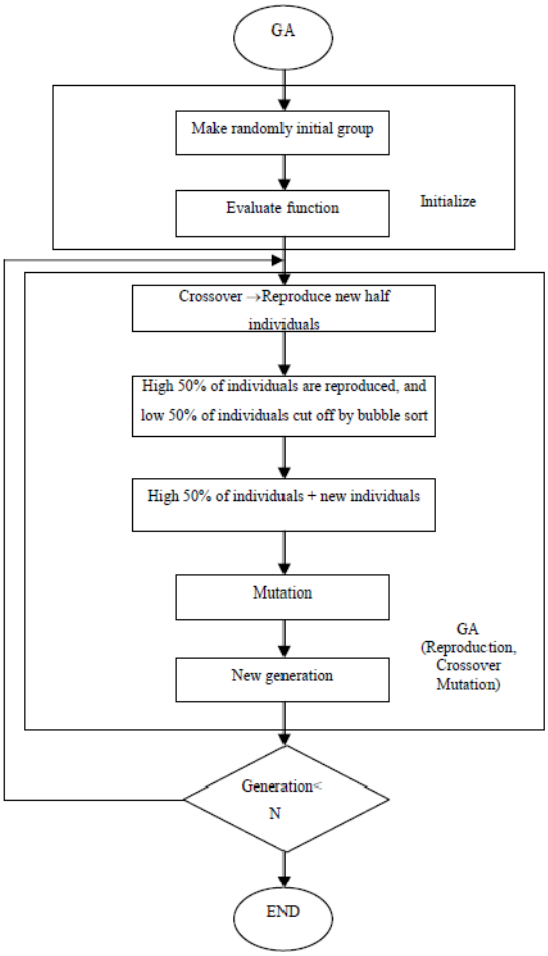


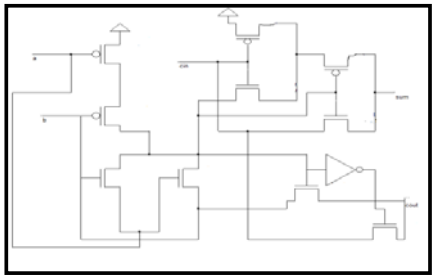
Fig. 2 a. Modified genetic algorithm. b. Flow chart of GA

The proposed MGA method determines the optimized value of the needed power and the extra power usage is minimized. This rule targets transistors that are not series and parallel but having similar location in the circuit which can be optimized with same

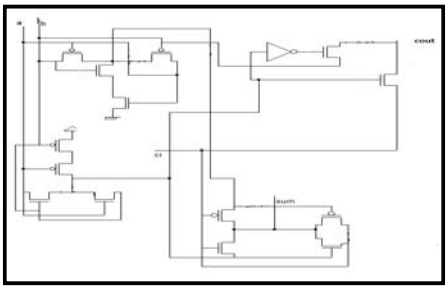
size since two paths will have similar resistance and similar drivability.

B. Hybrid adders

Full adder cell is the basic component for all digital signal processing unit. Based on the merits and demerits of the existing adder's features, the new Hybrid Full adders are designed [16-17]. The combination of 14T's Sum and Modified Shannon's carry is implemented, called as Hybrid-I[16] .In order to improve the power, delay and driving capability, Hybrid –A and Hybrid-B Full adders are designed[17],which are shown in Fifure.5. Hybrid-A Full adder is designed with 10T Sum and modified Shannon carry which consist of 12 transistors. Hybrid -B Full adder is designed with low power XOR and XNOR for sum implementation and carry is designed with modified Shannon .It requires 16 transistor using pass transistor logic and NMOS transistors. The Figure 3. shows the Hybrid- A and Hybrid- B adder. The optimal value of power is obtained by changing the size of the transistor (W/L) using modified genetic algorithm and the operating supply voltage V_{dd}. The width of the PMOS and NMOS transistors are alerted from 2.0 µm to 0.1 µm for optimizing Power Delay Product (PDP). The optimization of the width is carried out by modified genetic algorithm, which is proposed in this paper.



a. Hybrid A Full adder



b. Hybrid B Full adder

Fig. 3 : Transistor Schematic for Hybrid Full Adders [18]

IV. RESULTS AND DISCUSSION

Hybrid adders are designed and simulated in the HSPICE simulator at 90nm technology. The proposed modified genetic algorithm for width optimization is carried out with the help of MATLAB. This begins with 30 individuals and termination after 200-500 generation. The transistors adjusted with these size-values are induced in the circuit and the PDP is determined with the help of HSPICE circuit simulator. Table I shows the power consumption for the Hybrid A and Hybrid B adder with and without optimization. Delay performance of the Hybrid A and Hybrid B adders are given in the Table II. The comparison analysis of the power, delay and power delay product are shown in the Figure .4. The power consumption in the hybrid adders is reduced up to 9-11% with modified genetic algorithm at 1V (V_{dd}) with width optimization. Delay performance is improved up to 14-29 % at 1V (V_{dd}) in the adders using new optimization method. The power delay product reduction is achieved (24-39%) for the proposed adders with modified genetic optimization.

Table. I Power, Delay and PDP Analysis of the Hybrid adders

Sl.no	**One bit Adders**	**Power (µw) 1V**		**Power (µw) 0.8V**	
		Before optimization [18]	**After Optimization**	**Before optimization [18]**	**After optimization**
1	HYBRID–A	1.61	1.46	1.20	1.11
2	HYBRID –B	0.67	0.59	0.53	0.43
Sl.no	**One bit Adders**	**Delay (ps)-1V**		**Delay (ps)-0.8V**	
		Before optimization [18]	**after optimization**	**Before optimization [18]**	**After optimization**
1	HYBRID–A	0.37	0.26	0.95	0.79
2	HYBRID–B	6	5.12	9	7.68
Sl.no	**One bit Adders**	**PDP(e-18)-1V**		**PDP(e-18)--0.8V**	
		Before optimization [18]	**after optimization**	**Before optimization [18]**	**After optimization**
1	HYBRID–A	0.61	0.37	1.14	0.87
2	HYBRID–B	4.02	3.02	4.77	3.30

V. CONCLUSION

Transistor sizing is an important technique for determination of the power delay product in low power

circuits. This technique is applicable for all arithmetic low power circuits. In this paper modified genetic algorithm is proposed for transistor sizing through which power delay product optimization is achieved. In this work the Hybrid one bit adders are implemented in 90nm technology operated 1 GHZ frequency. The performances are analyzed using BSIM library files at 1V and 0.8V V_{dd}. Then the Power Delay product is reduced by width optimization using modified genetic algorithm. The performances of the proposed method is compared with existing adder .A better power delay product (24-39% reduction) has been achieved in the Hybrid Adders.

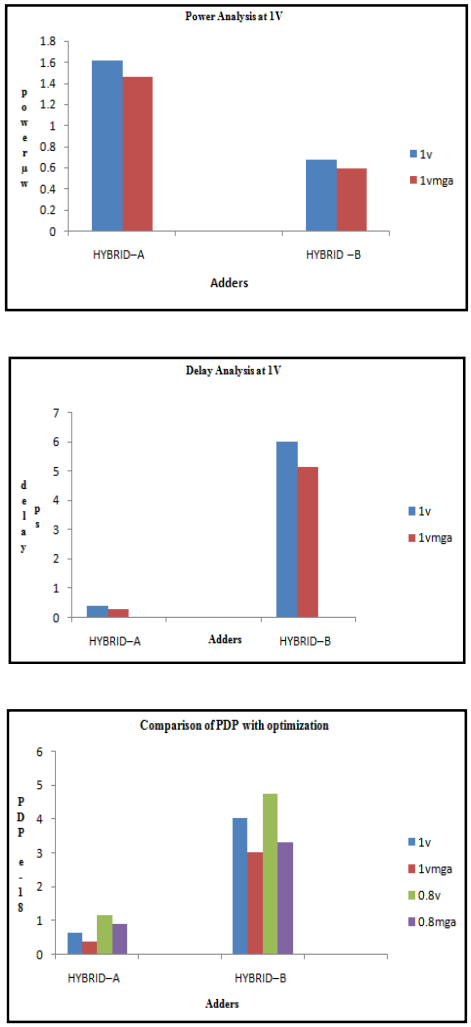


Fig. 4 : Comparison of the power, Delay and PDP of the Hybrid Adders

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Non Standard Size Image Compression with Reversible Embedded Wavelets

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Abstract **-** The rapid growth of digital imaging applications, including desktop publishing, multimedia, teleconferencing and high definition television, (HDTV) has increased the need of effective image processing. While processing any data, it requires large memory space for storage, which ultimately increases the transmission time. In order to save memory space and speed up the rate of transmission of data over networks, data compression is essential. Technically all image data Compressed into two groups as lossless and lossy. Some information is lost in the lossy compression, especially for radiological images. In this paper Non standard size still images are compressed by CREW using MATLAB. It uses a new form of wavelet transform technology. It is pyramidal (similar to hierarchical) and progressive by nature. From results it is observed that CREW provides higher compression ratio as compared to JPEG compression with same quality of image. The PSNR is also in acceptable range.

The features make CREW an ideal choice for applications that require high quality and flexibility for multiple input and output environments, such as, medical imagery, fixed-rate and fixed-size applications.

Key words **-** *CREW, JPEG, Image Compression, JPEG2000.*

I. INTRODUCTION

Uncompressed multimedia data (graphics, audio and video) requires considerable storage capacity and transmission bandwidth. Despite of rapid progress in mass storage density, processor speeds, and digital communication system performance, demand for data storage capacity and data-transmission bandwidth continues to outstrip the capabilities of available technologies. The recent growth of data intensive multimedia based applications have not only sustained the need for more efficient ways to encode signals and images but have made compression of such signals central to storage and communication technology [1].

For still image compression, the JPEG [2] standard has been established. The JPEG compression encoding is based on Discrete Cosine Transform [3] scheme. First the image is divided into 8 x 8 block size and then DCT is applied. Due to this block based DCT scheme, the performance of these encoders generally degrades at low bit rates.

Over the past few years, a variety of powerful and sophisticated scheme for image compression with high compression ratio and good image quality have been developed and implemented. More recently, the wavelet transform has emerged as a cutting edge technology. Wavelet based coding [4] provides substantial improvements in picture quality at higher compression ratios. This paper introduces some basic concepts on image compression and the more popular wavelet based image-coding schemes. Further the performance of wavelet-based compression is compared with JPEG compression.

In this paper section (II) describes image compression techniques using CREW. In section (III) the algorithm implemented is described. In section (IV) experimental results of wavelet transform are given. The performance comparison is briefed in section (V) and section (VI) concludes the paper.

II. COMPRESSION WITH REVERSIBLE EMBEDDED WAVELETS

CREW is a completely new type of image compression system. CREW is the first lossless and lossy continuous-tone still image compression system. It is based on a lossless reversible wavelet transform and has embedded quantization before storing and transmitting the mage. To reconstruct the compressed image, it is decoded, dequantized and inverse transformed.

A. Reversible wavelets

A reversible transform is an implementation of an exact reconstruction transform in integer arithmetic, such that a signal with integer coefficients can be losslessly recovered. An efficient reversible transform is one with transform matrix [5] of determinant≈ 1[6].There are two reversible wavelet transforms are employed. The first one, the so-called S-transform is introduced in and used by and [6] among others. The second one, the TS-transform was introduced in [7].

Let x(0),x(1),x(2),….. be the input signal, and let s(0),s(1),…..and d(0),d(1),……. be the smooth and the detail outputs respectively. The smooth output and the detail output are the results of the applications of the low-pass and the high-pass filters respectively.

The S-transform: The S-transform is defined by the outputs at a given index, n, is given in equ. (a).

$$s(n)= \left\lfloor \frac{x(2n)+x(2n+1)}{2} \right\rfloor \qquad (a)$$

$$d(n)= \frac{x(2n)-x(2n+1)}{2}$$

The factor of two in the transform coefficients addressing is the result of an implied subsampling by two. This transform is reversible and the inverse is given in equ. (b).

$$x(2n) = s(n) + \left\lfloor \frac{d(n)+1}{2} \right\rfloor \qquad (b)$$

$$x(2n+1)= s(n)- \left\lfloor \frac{d(n)}{2} \right\rfloor$$

The TS-transform: Similar to the S-transform, the TS-transform or two-six transform named after the number of taps in the low and high pass respectively

B. Embedded quantization

Lossy compression is achieved by embedded quantization. Embedded is used here to indicate that the codestream includes the quantization. The actual quantization (or visual importance) levels can be a function of the decoder or the transmission channel, not necessarily the encoder.

C. Pyramidal and progressive transmission

The CREW wavelet is pyramidal. Here pyramidal refers to a decomposition by a factor of two of the image without difference images. Here progressive refers specifically to progressive by bit-plane, i.e. MSB followed by lessor bits. Both the spatial and wavelet domains can be decomposed progressively, although CREW is progressive in the wavelet domain specifically.

D. Tree structure of wavelet decomposition

Figure.(1) shows a diagram of a wavelet decomposed image. The first level of coefficients is in the bottom and right most quadrants. These are denoted by LL, HL, HH, LH corresponding to high pass horizontal and low pass vertical, high pass horizontal and high pass vertical, low pass horizontal and high pass vertical respectively. The LL part of the first level is again decomposed, and so on. There is a natural and useful tree structure to wavelet coefficients in a pyramidal decomposition. Note that, there is a single LL subblock corresponding to the last level of decomposition. On the other hand there are as many HL, LH, and HH bands as the number of levels. The tree structure first introduced by Lewis and Knowles [8] and shown in figure (2), the coefficient at A is the direct parent to B, C and D and all their decedents. Specifically B is the parent to the four coefficients around E and the sixteen coefficients around H, etc

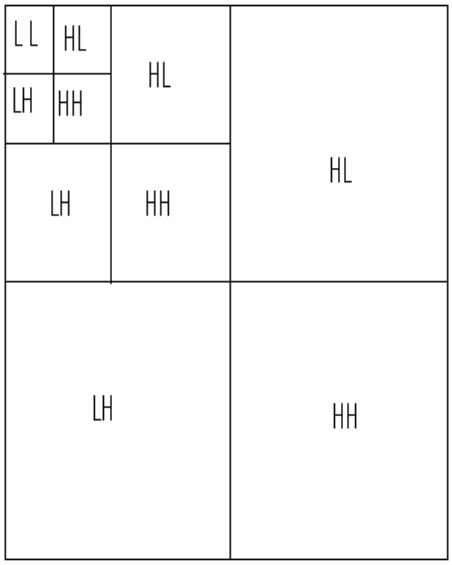


Fig. 1 : Relationship between the coefficients

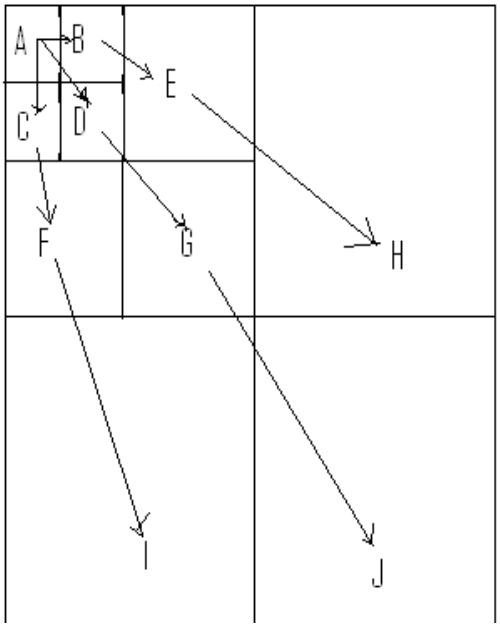


Fig. 2 : Tree Structure

E. Ordering of the coefficients and bit planes

The ordering of the data is important to realize the embedded quantization of the codestream. Two ordering systems are required: one for ordering the coefficients and the second for ordering the binary values within a coefficient. This order leads to a bitstream that is coded with a binary entropy coder.

All the coefficients within a coding unit are available in the random access memory, the embedding order between the coefficients within a coding unit can be any arbitrary order, known to both the encoder and the decoder. But since the entropy coder must be causal with respect to this ordering, it has a significant impact on the compression.

The embedded order used within a coefficient is bit-significance in the transform domain which is similar to but more general than the system used in [9]. The largest possible coefficient is used as a reference, and the coefficients are aligned with respect to it. This alignment is near-optimal in terms of statistical error metric such as MSE. Other alignments could correspond to coefficient specific quantization.

The binary entropy coder uses a Horizon context model in order to encode the coefficients. The model uses bits within a coding unit based on the spatial and spectral dependencies of the coefficients. The available binary values of the neighboring coefficients and parent coefficients can be used to create contexts. The contexts however must be causal for decidability and in small numbers for efficient adaptation.

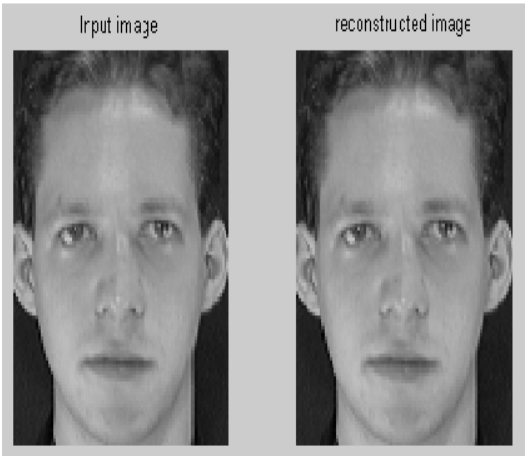
F. Entropy coding

The bit stream is encoded with a binary entropy coder. For this implementation Q-coder is used.

III. ALGORITHM

1) Digitize the source image into a signal s, which is a string of numbers.
2) Decompose the signal into a sequence of wavelet coefficients w.
3) Use thresholding to modify the wavelet coefficients
4) Use quantization to convert w' to a sequence q.
5) Apply entropy coding to compress q into a sequence

IV. EXPERIMENTAL RESULTS



V. PERFORMANCE COMPARISON CREW

Table 1: Compression Ratios and PSNR using CREW

Images	Level	MSE	PSNR dB	C R%	En-tropy
face1	3	7.95	39.13	87.50	7.03
dog	3	0.89.	48.64	75	7.17
flower	3	1.27	37.25	87.5	6.76
egret	3	0.13	57.07	75	6.92
bird	3	1.48	46.44	75	7.74

From the images of the experimental results it is seen that in JPEG method the effects of artifacts are due the correlation between boundaries of the blocks of the DCT

VI. CONCLUSION

Over the past several years, the wavelet transform has gained widespread acceptance in signal processing in general, and in image compression research in particular. In many applications wavelet-based schemes (also referred as subband coding) outperform other coding schemes like the one based on DCT. Since there is no need to block the input image and its basis functions have variable length, wavelet coding schemes at higher compression avoid blocking artifacts. Wavelet-based coding is more robust under transmission and decoding errors, and also facilitates progressive transmission of images. In addition, they are better matched to the HVS characteristics. Because of their inherent multiresolution nature[4], wavelet coding schemes are especially suitable for applications where scalability and tolerable degradation are important.

The CREW based image compression techniques provide higher compression ratios with moderate PSNR. The picture quality is also good for the intended application. The upcoming JPEG- 2000 standard incorporates the inherent multiresolution nature of wavelet transform. Many methods like EZW [6], SPIHT [7], EBCOT [8], SR [9] utilizes the wavelet image coding using decomposition techniques. There are few outstanding challenges facing the data compression community like interaction of harmonic analysis with data compression, joint source channel coding, image coding based on models of human perception, scalability, robustness, error resilience, and complexity. The challenges after fully resolved may enhance image data compression performance in the years to come.

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Design and Implementation of IEEE-754 Addition and Subtraction for Floating Point Arithmetic Logic Unit

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Abstract – This paper describes the FPGA implementation of a Decimal Floating Point (DFP) adder/subtractor using IEEE 754-2008 format. In this paper we describe an efficient implementation of an IEEE 754 single precision Standard for Binary Floating-Point Arithmetic to include specifications for decimal floating-point arithmetic. As processor support for decimal floating-point arithmetic emerges, it is important to investigate efficient algorithms and hardware designs for common decimal floating-point arithmetic algorithms. This paper presents novel designs for a decimal floating-point addition and subtraction. They are fully synthesizable hardware descriptions in VERILOG. Each one is presented for high speed computing.

Key words – *IEEE-754 Floating Point Standard; Addition and Subtraction Algorithm.*

I. INTRODUCTION

Floating point numbers are one possible way of representing real numbers in binary format; the IEEE 754 [1] standard presents two different floating point formats, Binary interchange format and Decimal interchange format. Multiplying floating point numbers is a critical requirement for DSP applications involving large dynamic range. This paper focuses only on single precision normalized binary interchange format. Fig. 1 shows the IEEE 754 single precision binary format representation; it consists of a one bit sign (S), an eight bit exponent (E), and a twenty three bit fraction (M or Mantissa). An extra bit is added to the fraction to form what is called the significand[1]. If the exponent is greater than 0 and smaller than 255, and there is 1 in the MSB of the significand then the number is said to be a normalized number; in this case the real number is represented by (1)

The IEEE-754 standard specifies six numerical operations: addition, subtraction, multiplication, division, remainder, and square root. The standard also specifies rules for converting to and from the different floating-point formats (e.g short/integer/ long to /from single/double/quad-precision), and conversion between the different floating-point formats.

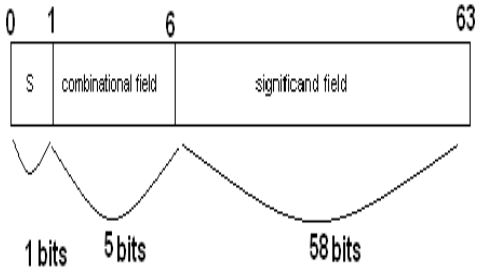


Fig. 1 : IEEE floating point format

$$Z = (-1^{S}) * 2^{(E - \underline{Bias})} * (1.M) \qquad (1)$$

Where $M = m_{22}\ 2^{-1} + m_{21}\ 2^{-2} + m_{20}\ 2^{-3} + \ldots + m_1\ 2^{-22} + m_0\ 2^{-23}$; $\underline{Bias} = 127$.

Fig : 1

a) 1-bit sign s.

b) A w + 5 bit combination field G encoding

classification and, if the encoded datum is a finite number,the exponent q and four significand bits (1 or 3 of which are implied). The biased exponent E is a w + 2 bit quantity q + bias, where the value of the first two bits of the biased exponent taken together is either 0, 1, or 2.

c) A t-bit trailing significand field T that contains J ×

10bits and contains the bulk of the significand. J represents the number of depletes.

When this field is combined with the leading significand bits from the combination field, the format encodes a total of p = 3 × J + 1 decimal digits. The values of k, p, t, w, and bias for decimal64 interchange formats are 16, 50, 12, and 398 respectively. That means that number has p=16 decimal digits of precision in the significand, an unbiased exponent range of [383, 384], and a bias of 398.

The IEEE-754 standard specifies six numerical operations: addition, subtraction, multiplication, division, remainder, and square root. The standard also specifies rules for converting to and from the different floating-point formats (e.g short/integer /long to/from single/double/quad-precision), and conversion between the different floating-point formats.

AX and BX are the significands and EAX, EBX and EX are the exponents respectively. X is a digit that denotes the outputs of different units. The symbol $(N)_Z^T$ refers to T^{th} bit of the Z^{th} digit in a number N, where the least significant bit and the least significant digit have index 0. For example, (A1)2

II. DECIMAL FLOATING POINT IN IEEE 754-2008:-

The primary difference between two formats, besides the radix, is the normalization of the significands (coefficient or mantissa). BFP significands are normalized with the radix point to the right of the most significant bit (MSB), while DFP mantissa are not required to be normalized and are represented as integers. The mantissa is encoded in densely packed decimal,

The exponent must be in the range [emin, emax], when biased by bias. Representations for infinity and not-a number (NaN) are also provided.

$$D = -1^{s} \times C \times 10^{q}, \quad q = E - \text{bias}$$

Where s is the sign bit, C is the non-negative integer Significand and q the exponent. The exponent q is obtained as a function of biased non-negative integer exponent E.

The mantissa is encoded in densely packed decimal [3], the exponent must be in the range [emin, emax], when biased by bias. Representations for infinity and not-a-number (NaN) are also provided. Representations of floating-point numbers in the decimal interchange formats are encoded in k bits in the following three fields (Fig1):

III. DECIMAL FLOATING-POINT ADDER /SUBTRACTOR IMPLEMENTATION

A general overview of proposed adder/subtractor is described below. For the best performance, the design presents eight pipelined stages as is exhibited in the Fig. 2. Arrows are used to show the direction of data flow, the dashed blocks indicate the main stages of the design, and the dotted line indicates the pipeline.

This architecture was proposed for the IEEE 754-2008 decimal64 format and can be extended for the decimal128 format. The adder/subtractor on decimal64 is carried out as follows: The decoder unit takes the two 64-bit IEEE 754-2008 operands (OP1, OP2) to generate the sign bits (SA, SB), 16-digit BCD significant (A0, B0), 10-bit biased exponents (EA, EB), the effective operation (EOP) and flags for specials values of NaN or infinity. The signal EOP defines the effective operation (EOP = 0 for effective addition and EOP = 1 for effective subtraction), this signal is calculated as:

$$EOP = SA \text{ xor } SB \text{ xor } OP \qquad (2)$$

As soon as possible the decoded significant become available, the leading zero detection unit (LZD) takes these results and computes the temporary exponents (EA1, EB1) and the normalized coefficients (A1, B1). The swapping unit swaps the operands (A1, B1) if EA1 < EB1 and Generates the BCD coefficients A2 (with higher exponent,max(EA1, EB1)) and B2 (with lower exponent, min(EA1,EB1)). In parallel with the above mentioned, this unit generates an exponent difference (Ed = |EA1 - EB1|), the exponent E2 = max(EA1, EB1), the SWAP flag if a swapping process is carried out, and the right shift amount (RSA) which indicates how many digits B2 should be right shifted in order to guarantee that both coefficients (A2, B2) have the same exponent.

The RSA is computed as follows:

if (Ed <= p_max)

RSA = Ed

else RSA = p_max

The value p_max = 18 digits, RSA is limited to this value since B2 contains 16 digits plus two digits which will be processed to compute the guard and round digit.

Next, the Shifting unit receives as inputs the RSA, and the significand B2 generating a shifted B2 (B3) and a 2-bit signal called predicted sticky-bit (PSB) that will predict two initials sticky bits. PSB and B3 will be

utilized as inputs in the decimal addition, control signals generation and post-correction units, respectively.

The outputs above mentioned plus two signals, significand A2 and EOP, are taken as inputs in the control signals generation unit and generates the signals necessary to perform an addition or subtraction operation, these signals are described in the Sub-section 3.4 and are made up of a prior guard digit (RD2), the final partial sum (S2) and the corrected exponent (E3). digit (GD1), a prior round digit (RD1), an extra digit (ED), a signal which verifies if A2 > B3(AGTB) and a carry into (CIN).

The significant BCD (A2, B3) and the CIN are inputs the decimal addition unit generating the partial sum of magnitude |S1| = |A2 + (-1) EOP B3| and a carry out (COUT), respectively.

At once, the 16-digit decimal addition unit takes the A2, B3, EOP and CIN and computes S1 as follows:

S1 = A2 + B3 if EOP = 0, S1 = A2 + cmp9 (B3)

if EOP = 1 and A2 >= B3, and

S1 = cmp9 A2+cmp9(B3)) if EOP = 1 and A2 < B3.

The symbol cmp9 means the 9`s complement.

The post-correction unit uses as inputs the PSB, the Exponent E2, GD1, RD1, ED, the partial sum S1 and COUT to verify, correct and compute the inputs signals if only the following two cases occur: 1) COUT=1 and EOP=0 and 2) (S1)15=0 and (GD1 > 0) and (EOP=1).

The analysis is explained in the Sub-section 3.5.

This unit generates the final sticky bit (FSB), the corrected guard digit (GD2) and round Next, the Rounding unit takes the outputs of the prior unit and rounds S2 to produce the result´s significand S3 and adjusts the exponent E3 to calculate the final exponent E4. Simultaneously the overflow, underflow and sign bit signals

The final sign bit is computed as:

FS = (SA ^ ~EOP) V (EOP ^ (AGTB ⊕ SA ⊕ SWAP))

IV. PROBLEMS ASSOCIATED WITH FLOATING POINT ADDITION & SUBTRACTION

For the input the exponent of the number may be dissimilar. And dissimilar exponent can't be added directly. So the first problem is equalizing the exponent. To equalize the exponent the smaller number must be increased until it equals to that of the larger number. Then significant are added. Because of fixed size of mantissa and exponent of the floating-point number cause many problems to arise during addition and subtraction. The second problem associated with overflow of mantissa. It can be solved by using the rounding of the result. The third problem is associated with overflow and underflow of the exponent. The former occurs when mantissa overflow and an adjustment in the exponent is attempted the underflow can occur while normalizing a small result. Unlike the case in the fixed-point addition, an overflow in the mantissa is not disabling; simply shifting the mantissa and increasing the exponent can compensate for such an overflow. Another problem is associated with normalization of addition and subtraction. The sum or difference of two significant may be a number, which is not in normalized form. So it should be normalized before returning results

V. ADDITION AND SUBTRACRION ALGORITHM

Let a1 and a2 be the two numbers to be added. The notations ei and si are used for the exponent and significant of the addends ai. This means that the floating-point inputs have been unpacked and that si has an explicit leading bit. To add a1 and a2, perform these eight steps:

1. If e1 < e2, swap the operands. This ensures that the difference of the exponents satisfies d = e1–e2 0. Tentatively set the exponent of the result to e1.

2. If the sign of a1 and a2 differ, replace s2 by its two's complement.

3. Place s2 in a p-bit register and shift it d = e1-e2 places to the right (shifting in 1's if the s2 was complemented in previous step). From the bits shifted out, set g to the most- significant bit, r to the next most-significant bit, and set sticky bit s to the OR of the rest.

4. Compute a preliminary significant S = s1+s2 by adding s1 to the p-bit register containing s2. If the signs of a1

Abstract", will require you to apply a style (in this case, italic) in addition to the style provided by the drop down menu to differentiate the head from the text.

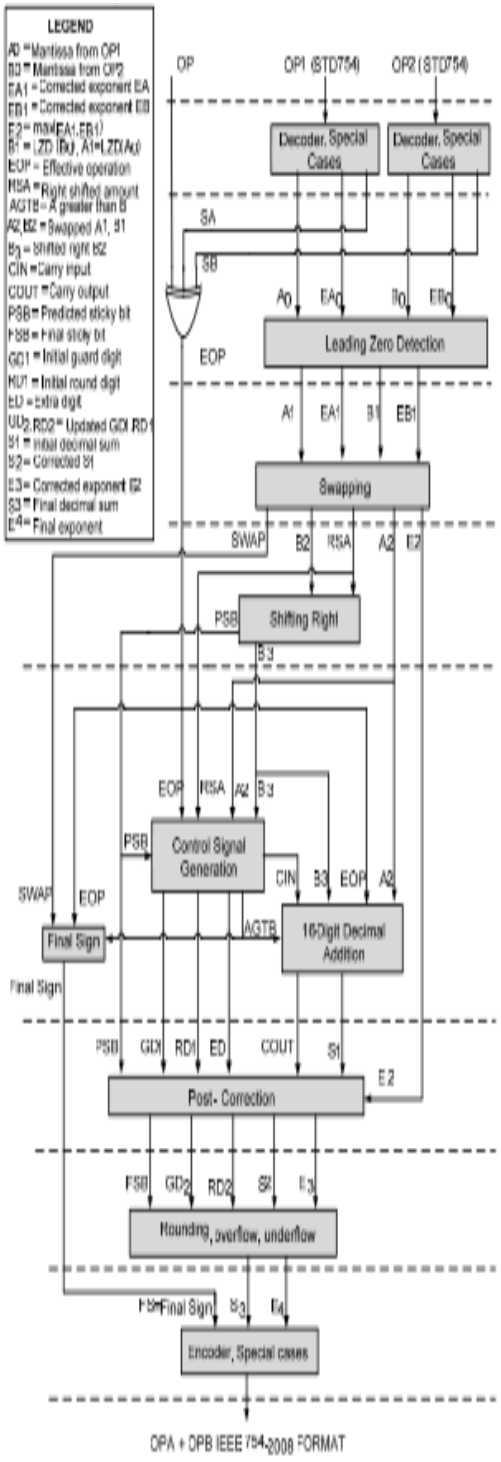


Fig. 2: implementation diagram are generated.

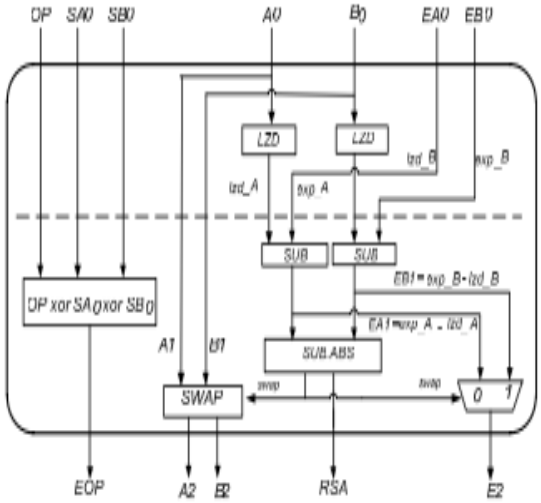


Fig. 3. Alignment and swapping unit

and a2 are different, the most-significant bit of S is 1, and there was no carry out then S is negative. Replace S with its two's complement. This can only happen when d = 0.

5. Shift S as follows. If the signs of a1 and a2 are same and there was a carry out in step 4, shift S right by one, filling the high order position with one (the carry out). Otherwise shift it left until it is normalized. When left shifting, on the first shift fill in the low order position with the g bit. After that, shift in zeros. Adjust the exponent of the result accordingly.

6. Adjust r and s. If S was shifted right in step 5, set r: = low order bit of S before shifting and s: = g or r or s. If there was no shift, set r: = g, s: = r. If there was a single left shift, don't change r and s. If there were two or more left shifts, set r: = 0, s: = 0. (In the last case, two or more shifts can only happen when a1 and a2 have opposite signs and the same exponent, in which case the computation s1 + s2 in step 4 will be exact.)

7. Round S using following rounding rules as in Table ;

Rounding	*Sign of result ≥0*	*Sign of result <0*
$-\infty$		+1 if r ∨ s
$+\infty$	∨ s	
0		
Nearest	+1 if r ∧ p_0 or r	+1 if r ∧ p_0 or r

If a table entry is non empty, add 1 to the low order bit of S. If rounding causes carry out, shift S right and adjust the exponent. This is the significant of the result.

8. Compute the sign of the result. If a1 and a2 have the same sign, this is the sign of the result.If a1 and a2 have different signs, then the sign of the result depends on which of a1, a2 is negative, whether there was a swap in the step 1 and whether S was replaced by its two's complement in step 4. As in table below

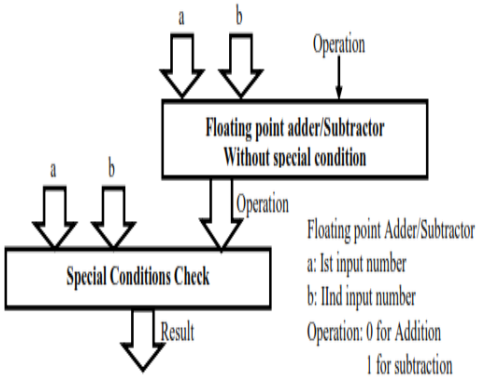
Swap	*Compleme*	*Sign (a_1)*	*Sign*	*Sign*
Y	∅	+	-	-
es	∅	-	+	+
Y		+	-	+
es	N	-	+	-
N	o	+	-	-

VI. SPECIAL CONDITIONS

Some special conditions are checked before processing. If any condition is met then we have no need to calculate the result by normal procedure. Results are directly calculated. So all the operations are bypassed when any such condition is met.

1. If a1 = 0 and a2 = 0 then result will be zero.
2. If a1 = a2 and sign of a1 sign of a2 then result will be again zero.
3. If a1 = 0 and a2 0 then result will be equal to a2.
4. If a2 = 0 and a1 0 then result will be equal to a1.
5. If d = |e1 – e2| > 24 then result will be equal to larger of a1 and a2.

VII. HARDWARE APPROACH



The block diagrams of the architecture used for combinational adder is shown above in Figure 4, step by step from the lower abstract level to the higher abstract level.

B. Unsigned Adder (for exponent addition)

This unsigned adder is responsible for adding the exponent of the first input to the exponent of the second input and subtracting the Bias (127) from the addition result (i.e. A_exponent + B_exponent - Bias). The result of this stage is called the intermediate exponent. The add operation is done on 8 bits, and there is no need for a quick result because most of the calculation time is spent in the significand multiplication process (multiplying 24 bits by 24 bits); thus we need a moderate exponent adder and a fast significand multiplier.

An 8-bit ripple carry adder is used to add the two input exponents. As shown in Fig. 3 a ripple carry adder is a chain of cascaded full adders and one half adder; each full adder has three inputs (A, B, C_i) and two outputs (S, C_o). The carry out (C_o) of each adder is fed to the next full adder (i.e each carry bit "ripples" to the next full adder).

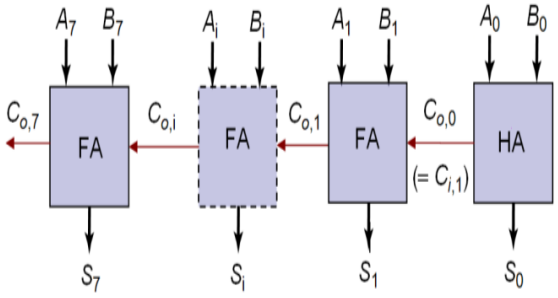


Fig. 5 : Rripple carry adder

The addition process produces an 8 bit sum (S_7 to S_0) and a carry bit ($C_{o,7}$). These bits are concatenated to form a 9 bit addition result (S_8 to S_0) from which the Bias is subtracted. The Bias is subtracted using an array of ripple borrow subtractors.

A normal subtractor has three inputs (minuend(S), subtrahend (T), Borrow out (B_o)).The subtractor logic can be optimized if one of its inputs is a constant value which is our case, where the Bias is constant ($127|_{10}$ = $001111111|_2$).

S	T	B_i	Difference(R)	B_o
0	1	0	1	1
1	1	0	0	0
0	1	1	0	1
1	1	1	1	1

The above table shows one bit subtractor

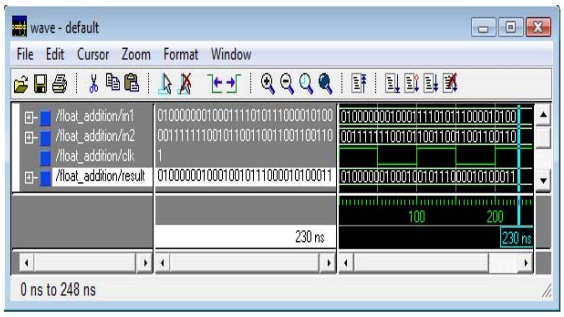
VIII. SIMULATION RESULTS FLOATING POINT ADDER

Input 1 = 01000000010001111010111000010100
(3.120 10)

Input 2 = 00111111100101100110011001100110
(1.175 10)

Required Result =
01000000100010010111000010100011
(4.295 10)

Obtained Result =
01000000100010010111000010100011 (4.295 10)

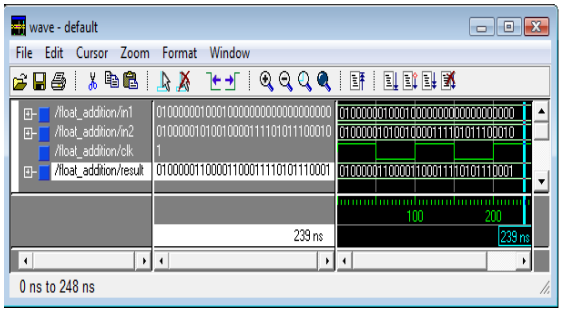


Input 1 = 01000000100010000000000000000000
(4.25 10)

Input 2 = 01000001010010000111101011100010
(12.53 10)

Required Result =
01000001100001100011110101110000 (16.78 10)

Obtained Result =
01000001100001100011110101110001 (16.78 10)



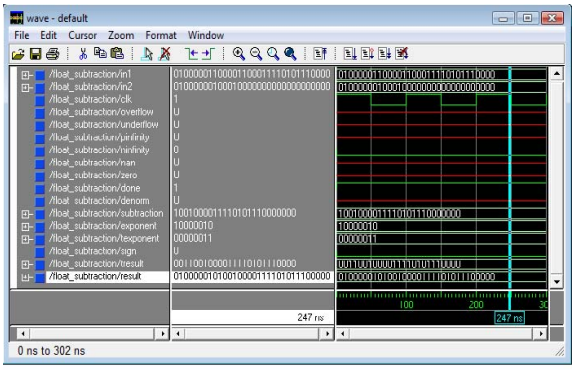
FLOATING POINT SUBTRACTOR

Input 1 = 01000001100001100011110101110000
(16.78 10)

Input 2 = 01000000100010000000000000000000
(4.25 10)

Required Result =
01000001010010000111101011100010 (12.53 10)

Obtained Result =
01000001010010000111101011100010 (12.53 10)

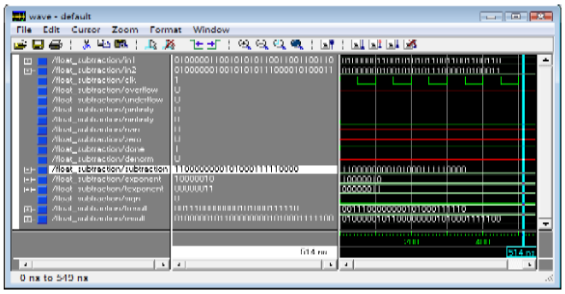


Input 1 = 01000001100101010110011001100110
(18.675 10)

Input 2 = 01000000100101010111000010100011
(4.670 10)

Required Result =
01000001011000000000101000111101 (14.005 10)

Obtained Result =
01000001011000000000101000111101 (14.005 10)



IX. IMPLEMENTATION AND TESTING

The whole adder (top unit) was tested against the Xilinx floating point adder core generated by Xilinx coregen. Xilinx core was customized to have two flags to indicate overflow and underflow, and to have a maximum latency of three cycles. Xilinx core implements the "round to nearest" rounding mode.

A testbench is used to generate the stimulus and applies it to the implemented floating point adder and to the Xilinx core then compares the results. The floating point multiplier code was also checked using DesignChecker [7]. DesignChecker is a linting tool which helps in filtering design issues like gated clocks, unused/undriven logic, and combinational loops. The design was synthesized using Precision synthesis tool [8] targeting Xilinx Virtex-5 ,5VFX200TFF1738 with a timing constraint of 300MHz.

Post synthesis and place and route simulations were made to ensure the design functionality after synthesis and place and route. shows the resources and frequency of the implemented floating point multiplier and Xilinx core

	Technology	Clk	Cycle	Dela	Mop
SW	**Itanium2 [18]**	1.4	219	156.4	6.4
	Xeon5100 [19]	3.0	133	44.3	22.6
	Xeon [18]	3.2	249	77.8	12.9
	Pentium M [21]	1.5	848	565.3	1.8
HW	**Power6 [22]**	5.0	17	3.4	294.1
	Z10 [23]	4.4	12	2.7	366.7
	BID 65nm [10]	1.3	3-13	10.0	100.0
	BID Virtex 5 [9]	0.16	13-18	109.8	9.1
	Proposed	0.2	8	40	200.0

The area of Xilinx core is less than the implemented floating point adder because the latter doesn t truncate/ round the 48 bits result of the mantissa multiplier which is reflected in the amount of function generators and registers used to perform operations on the extra bits; also the speed of Xilinx core is affected by the fact that it implements the round to nearest rounding mode.

X. CONCLUSIONS AND FUTURE WORK

This paper deals with development of a Floating Point adder and subtractor for ALU in VHDL and verilog with the help of ModelSim and synthesized with Xilinx tools. Simulation results of all the designed programs have been carried out for various inputs with the help of ModelSim tool. Both are available in single cycle and pipeline architectures and fully synthesizable with performance comparable to other available high speed implementations. The design is described as graphical schematics and VHDL code. This dual representation is very valuable as allows for easy navigation over all the components of the units, which allows for a faster understanding of their interrelationships and the different aspects of a Floating Point operation.

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Intelligent Lighting By Fuzzy Logic Using PSS

(An innovative approach towards energy conservation)

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Abstract **-** This paper presents an insight into the energy conservation by the automation of electronic appliances using proximity switch sensors (PSS). The proposed system conserves energy efficiently in the lighting of building which is scalable to computers, TV, air-conditioners, fans etc. The lighting of the room depends not only on the exterior environment light but also on the presence of human. The present system available can only dim the lighting of the room according to external lighting. The most advanced system can just sense only whether there s a human in room.[1]But it is more possible to manage energy more efficiently by providing the required lighting only to the place occupied and dimming all the other lights in addition to the existing system. This differential lighting system is a new innovation. The proposed control system can dim or brighten the LED lights automatically not alone according to the environmental light but also by the occupancy. This proposed system is realized using fuzzy logic providing a clean, environment friendly day lighting system. It can be applied to many fields such as control of streetlights, control rooms etc. Therefore a tremendous potential energy saving of well over to 80% was achieved in a residential or commercial building due to automated control of fan, light and air conditioners.

Key words **-** *pss, Fuzzy logic, potential savings.*

I. INTRODUCTION

In the current scenario, energy crisis is the burning problem in all developing nations. A huge deal of energy is wasted due to major electrical loadings like machineries, lighting, air-conditioning etc. In our work we have focused on optimizing power consumption by detecting the parameters such as occupancy, light intensity using an automated fuzzy control system.

Moreover it is a general fact that only a 30% of the room is most often say 80% of the time is used but the whole room is lighted to the required lux level resulting in a huge deal of power going for nothing. Energy in large magnitude can be saved if the illumination is given where ever necessary, also maintaining a threshold value in other areas. This is highly applicable in control rooms in industries where a high degree of lux level is maintained always. Hence a new fuzzy based lighting system is introduced to optimize power consumption.

II. PRINCIPLE OF PROXIMITY SENSOR:

The electric field is generated around and between two electrodes. For the sensor to function, the body being sensed must intersect the field generated between the two electrodes. Electrodes are positioned such that whatever it is you are trying to detect, will move into that field. When a hand, body or any other conductive object is placed in the field, an electric current will be induced in it. If that object is grounded, a portion of the radiated field will be shunted to ground. In Shunt Mode, the sensor is adjusted so that when there is no object in the field, the signal strength arriving at the receive electrode is just enough to cause a relay on the board to close.

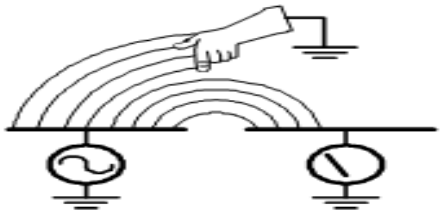

Fig. 1

When an object enters the field, the signal strength is reduced, and the power to the relay is no longer enough to hold it closed. It opens and will remain open until the object exits the field. An important consideration for the use of Shunt Mode is that the object entering the field be grounded. If the object is not grounded, it is unlikely that it will draw off enough of the radiated signal to cause the relay to open.

III. GENERAL CONTROL STRUCTURE FOR SYSTEMS:

It must be possible for the user to switch off or bypass the proposed system under some conditions or in case of failures. Hence for all the proposed systems below the following provisions (switch sw1 and sw2) are made. (Fig-2)

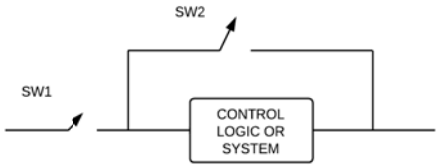

Fig. 2

Here sw2 is used to bypass the system and sw1 is used to switch on or switch off the appliance.

IV. LIGHT:

When the whole scenario is set for superior energy utilization, it is known fact that the lights is tuned to work based on occupancy and the exterior lighting.. To make it more efficient the LED lights are used instead of CFL or incandescent lights.

The proposed algorithm is: (Fig-3)

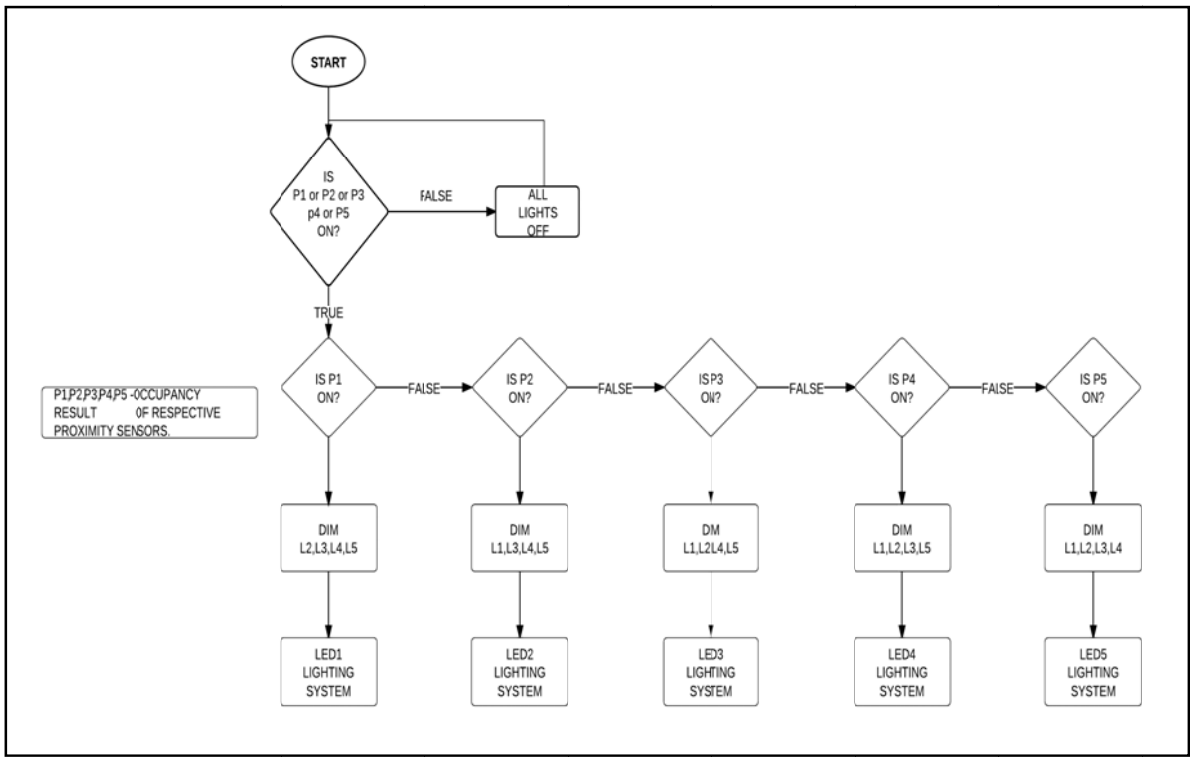

Fig. 3

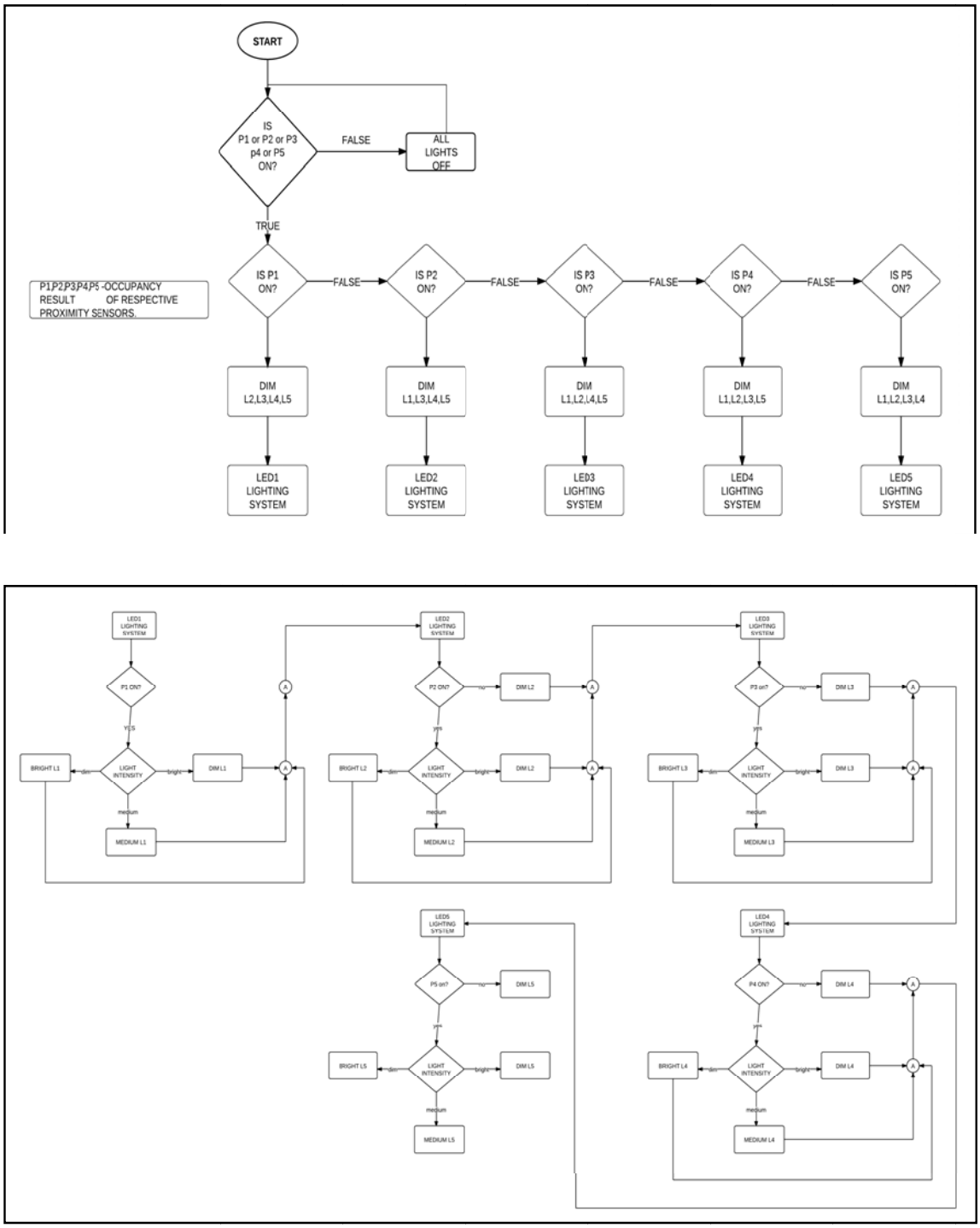

Fig. 4

Rule Block

Each rule block confines all rules for the same context. A context is defined by the same input and output variables of the rules. The degree of support (DoS) is used to weigh each rule according to its importance. As example when the Intensity is "Poor" and the Occupancy is "High" then the Light Intensity will trigger the certain pulse so that the dimmer light will be "Bright".

- If the occupancy is low, Intensity is high, Light intensity and the duty cycle will be low
- If the occupancy is zero, Intensity is high, Light intensity and the duty cycle will be zero
- If the occupancy is high, Intensity is low, Light intensity and the duty cycle will be high
- If the occupancy is high, Intensity is medium, light intensity and the duty cycle will be medium.
- If the occupancy is high, Intensity is high, Light intensity and the duty cycle will be medium

Likewise a rule list is obtained by fuzzification and defuzzification. Fuzzification and defuzzification is done using MATLAB.

V. INPUT VARIABLE INTENSITY:

This is an input variable due to the variation of luminance (Lux) of the surrounding. The Figure shows a value of intensity that is set t, that is 0, 110, 200, 350. It has four-membership functions, which are off, dim, medium, Bright. The figure below shows the value of luminance that is set.

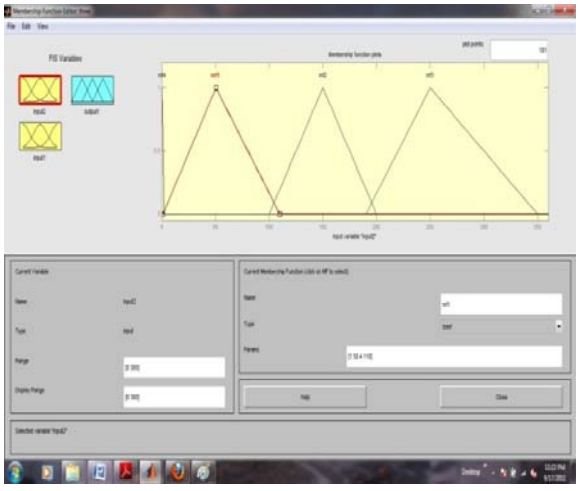

Fig. 5

VI. INPUT VARIABLE OCCUPANCY:

This value is a change of existence of user in the modeled area. It has two membership functions, on and off. In The Figure shows the value of occupancy that is set.

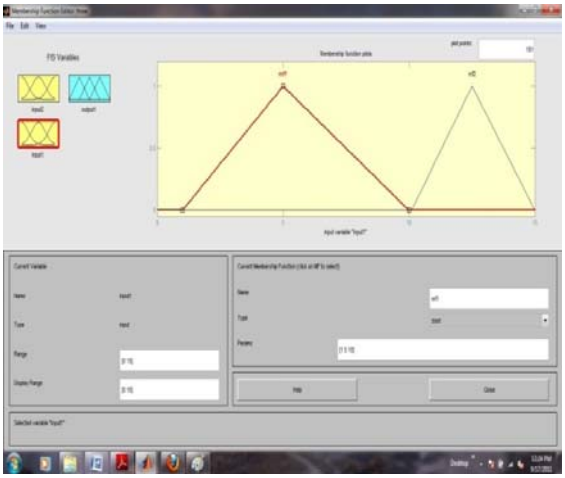

Fig. 6

VII. OUTPUT VARIABLE LIGHT INTENSITY:

It has five-membership function that is off, Dim, Medium and Bright. The modeled area shows the output of the light intensity. This output is controlled by Centroid Defuzzification method.

The Figure shows a value of duty cycle that is set in this paper, that is 0, 30, 70, 100

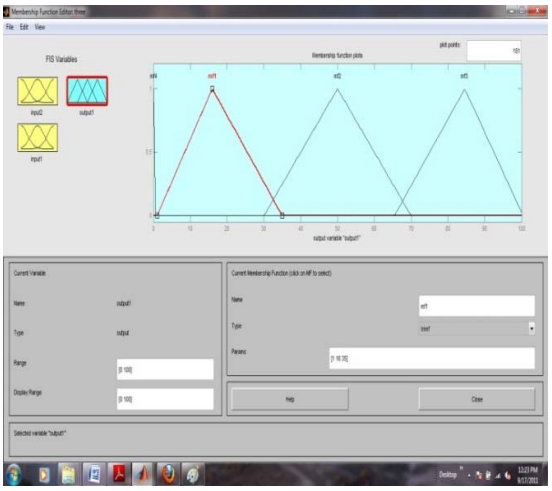

Fig-7

From the defuzzification results, the hereby surface graph is obtained as output:

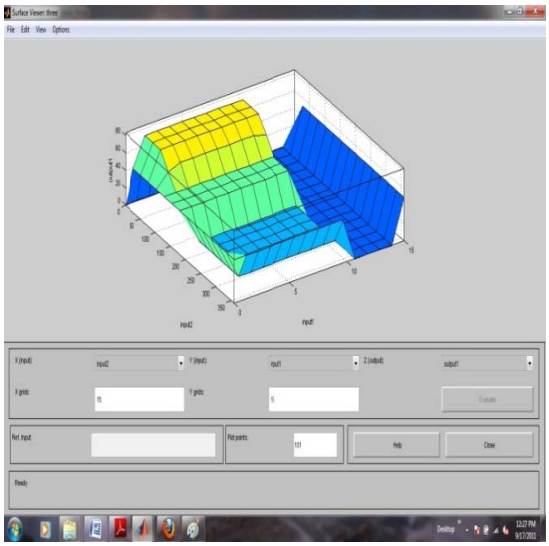

Fig. 8

VIII. IMPLEMENTATION:

The implementation of the given by the following block diagram

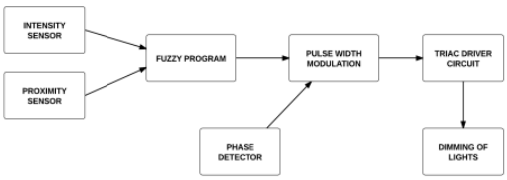

Fig. 9

LIGHT INTENSITY AND PROXIMITY SENSOR:

Photo sensors can be used to detect the available lighting in a closed loop system and the occupancy can be detected by proximity sensors as mentioned.

PULSE WIDTH MODULATION:

A far superior method of dimming LEDs is to use Pulse Width Modulation (PWM). With PWM strings of LED bulbs can all be driven with the recommended forward current, with the dimming achieved by turning the LEDs on and off at high frequency.

PHASE DETECTOR:

The function of Phase Detector circuit is to convert AC Voltage sine signal into square wave signal so that the Pulse Width Modulation (PWM) can be synchronized with the 8-bit (digital signal) to trigger light intensity by using Triac Driver Circuit

PWM with a Microcontroller

- This powerful CMOS FLASH-based 8-bit microcontroller comes with an 40pins
- .The PIC16F887 features 256 bytes of EEPROM data memory, self programming, an ICD, 2 Comparators, 14 channels of 10-bit Analog-to-Digital (A/D) converter, 1 capture/compare/PWM and 1 Enhanced capture/compare/PWM functions.[2]
- This makes it ideal for our application.

TRIAC DRIVER CIRCUIT:

Once triggered, the device continues to conduct until the current through it drops below a certain threshold value, the holding current, such as at the end of a half-cycle of alternating current (AC) mains power. This makes the TRIAC a very convenient switch for AC circuits, allowing the control of very large power flows with milli-ampere-scale control currents. In addition, applying a trigger pulse at a controllable point in an AC cycle allows one to control the percentage of current that flows through the TRIAC to the load (phase control). Hence it can be used to efficiently dim or brighten the lights.[courtesy:Wikipedia.com]

IX. COMPARISAN OF POWER CONSUMPTION IN AND CONTROL ROOMS:

CONTROL ROOM:

It is generally known fact, a lot of lux is focussed even when there is no man. To proceed further with the effectiveness of the proposed system, a typical control room in industry is studied and calculations are done with the both existing and proposed system.

Only 30% of the either part of room is only occupied most of the times in the typical example taken. Hence by evaluating it,

When cfl is used without the proposed system:Let us assume that 7500 lumens is required

EXISTING SYSTEM:

Five 1600lumens bulbs are required.

=5*25w(each 25 w tube light gives 1600lumens)

=125w

It is operated all over the day when assumed as the room is closed.

=24*125*365(total power for a year)

=1095 kwh

Similarly when incandescent bulb is used,

100w bulb gives 1600 lumens

By similar calculations,

Total energy consumed for a year is=4380 kwh.

PROPOSED SYTEM:

5*16w led bulbs are sufficient. Suppose the light intensity outside is bright from 8 am – evening 4pm,light will glow dim. On an average of 25% power consumed,

=16*0.25*8

=32Wh

Suppose the light intensity outside is medium from 6am – 8am and evening 4pm-6pm ,light will glow medium brightness. On an average of 50% power consumed,

=16*0.5*4

=32Wh

Suppose the light intensity outside is dim or no light in the remaining hours, light will glow bright. On an average of 80% power consumed,

=16*0.8*12

=153.6Wh

Total energy consumed in a day per led light=153.6+32+32=217.6Wh. Only 30% of the room is occupied for 80% of the time and remaining full load hence,

=(0.3*217.6*5*0.8)+(0.2*217.6*5)

=261.12 + 217.6

=478.72Wh

When operated for 365 days,

=174.73 KWh

Hence the potential savings close to:

TYPE OF LIGHTING	Potential Savings When fluorescent lights are used(%)	Potential Savings When Incandescent lights are used(%)
PROPOSED SYSTEM WITH LED LIGHTS	84.1	96.1

Table 1

TOTAL POWER CONSUMED IN PERIOD OF 6 YEARS:

Specifications	LIGHT IN EXISTING SYS.	LIGHT IN PROPOSED SYS
Cost per unit in HT connection(Rs)	8.5	**8.5**
Total energy consumed(Kwhr) in 6 years	1095	174.73
Total cost(Rs)	9308	1485.2
No of hours of operation needed for lights(hours)	52560	52560
No. of replacement of lights needed	7	nil
Cost of replacement(Rs)	5250	nil
Grand total of running cost (Rs)	14558	1485

Table 2

X. CONCLUSION:

Energy is a global necessity and the world's burgeoning population has increased the demand for energy to levels that we simply cannot continue meet. It is, therefore, imperative that we implement more effective conservation measures, as the supply of fossil fuels is not infinite and its use is exceedingly harmful to the environment. For the present generation and future generations, we need to find ways to conserve energy. Now from the above result, it is seen that by just investing 16440 once we can save nearly 85% of the electricity bill in lighting to operate more efficiently. This is nearly 0.016% of the total profit from this implementation. Moreover a great deal of energy is also conserved meeting the energy demands. This system when implemented in large scale promises to add more carbon credits to the country enabling to grow more. Hence let us progress towards greener efficient environment.

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Design & Analysis of Fly back Converter for Grid & Filament Power Supplies of Travelling Wave Tube

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Abstract **-** In High Power Pulsed Radar Transmitters the gridded TWT are used and consists of floating deck modulator unit which houses the Grid and Filament power supplies. The Grid Control includes the Grid Positive & Grid Negative Power Supplies. The Positive voltage is used to turn on the TWT & Negative voltage is used to operate the TWT in off state. The Filament power supply heats the cathode to required temperature to emit electrons. The aim of the project is to design the Grid power supplies and Filament Power supply based on the Fly back Converter topology which is operated at 100 KHz in DCM mode and CCM mode respectively. The Pulse width modulation technique is used to maintain the voltage at desired value using an IC UC1526.The switching device is protected against over currents by pulse to pulse current limiting using current transformer and current limit comparator of uc1526.

Keywords *- RADAR, TWT, FLYBACK Converter, pulse width modulator, Grid filament, DCM (Discontinuous current mode),CCM(Continuous current mode).*

I. INTRODUCTION

Transmitter in radar applications, use microwave tubes for the purpose of amplifying RF signals from few milliwatts to several kilowatts. This amplification is performed by the microwave tubes like Crossfield amplifiers, Klystrons, TWT's etc. All these microwave tubes amplify the RF signal by proper interaction between electron beam and RF field, in such a way that electron beam energy is converted into RF field energy to generate necessary electron beam energy high/low voltage floating supplies are used. These supplies include high frequency converter topologies to get improved performance and to realize in compact size, also these power supplies needed to be regulated precisely to meet requirements of spectral purity. Filament, grid bias for cut-off, grid pulse supply and focus supply. It is essential to design these supplies using high frequency converter topologies to get improved performance and to realize in compact size, also these power supplies needed to be regulated precisely to meet requirements of spectral purity.

II. RADAR

The term RADAR stands for *RA*dio *D*etecting *A*nd *R*anging. Radar is the primary sensor on nearly all military aircraft. Radar radiates electromagnetic energy from an antenna to propagate in space. Some of the radiated energy is intercepted by a reflecting object usually called a target, located at a distance from the Radar. The energy intercepted by the target is reradiated in many directions. Some of the re-radiated which called an echo is retuned and received by the Radar antenna. Thus Radio waves were utilized to detect the presence of a target and determine its distance or range. Other roles include airborne early warning, target acquisition, target tracking, target illumination, ground mapping, collision avoidance, altimeter, weather warning. Practical frequency range 100MHz-100GHz. The velocity of the electromagnetic waves radiated from the Radar in free space is approximately 1000ft/µsec. Therefore if the object is on nautical mile away (6080ft) it will take slightly more than 12 µsec for the transmitted energy to reach the target and return. The radar transmitter subsystem uses a microwave tubes for the purpose of amplifying the signal from few milliWatts to several kilowatts. This amplification is performed by the microwave tubes like Cross field amplifier, Klystrons and TWT (Traveling Wave tube).

III. TRAVELING WAVE TUBE

A traveling wave tube (TWT) which is shown in Fig 1.1 is a device that is used to create high power radio frequency (RF) signals. The injected RF signal into a TWT travels along a helical transmission line inside vacuum tube waveguide, which allows the

signal's electromagnetic fields to interact with an electron beam that passes through the center of the coil. This interaction amplifies the input signal. TWTs have been designed to operate for frequencies as low as 500MHz and as high as 300 GHz. They are used extensively in satellite communication and airborne radar systems.

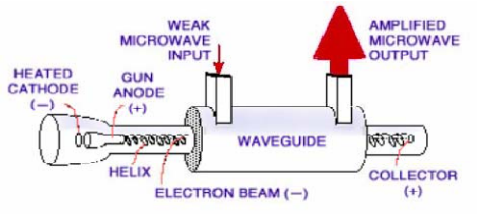

Fig. 1 : Structure of Traveling Wave Tube

IV. FLYBACK CONVETER

A flyback converter is a switching power supply topology widely used in applications that require power below IOOW.

A basic flyback converter, comprising of a power MOSFET, diode, capacitor, and transformer, is shown in Fig. **2. A** gapped transformer provides electrical isolation between input and output as well as store energy (in the air-gap). When the MOSFET is turned on, the primary current flows, while the diode is reverse biased preventing a flow of secondary current. During this MOSFET's turn on period, energy is stored in the transformer with a load current being supplied by the output capacitor. When the MOSFET is tuned off, the primary current ceases to conduct. The collapsing magnetic field in the transformer causes a polarity of the secondary voltage to reverse. The diode is now forward biased enabling a flow of secondary current. During this turn off period, energy stored in the transformer is released to the output capacitor and load.

Various aspects of the flyback converter and design are mentioned in [1]. A flyback converter can be designed to operate in CCM or DCM.

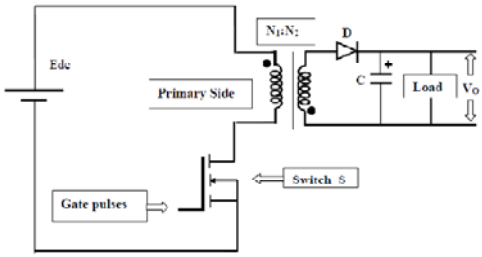

Fig. 2 : Flyback Converter

GRID & FILAMENT POWER SUPPLIES

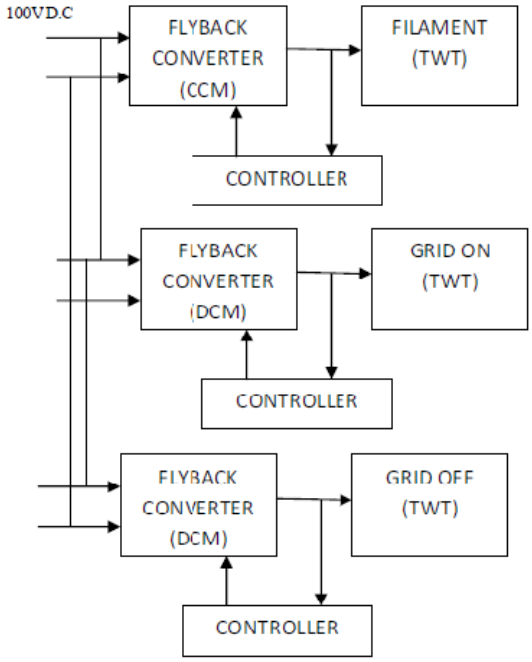

Fig. 3 : Block diagram of Grid & filament power supplies

The Grid power supplies includes Positive Grid & Negative Grid supplies which are used to control the output of the TWT.The Positive Grid Supply is used to switch on the TWT & Negative Grid supply is used to switch of the TWT.In Fig.3. An input of 100V is fed to Flyback Converter that uses the MOSFET switch, operating at 100 KHz. The duty cycle of switch is varied to obtain the required output voltage.The Fly back converter is operated in DCM mode.The fly back transformer provides the adjustment output voltage as required by the TWT .

The filament power supply is realized using a flyback converter topology which operates in CCM Mode . The continuous power supply is maintained at filament which heats the cathode to required temperature to emit electrons.

V. POWER SUPPLY DESIGN

A. Transformer Design

Positive Grid supply design :

Output voltage - V_o = 400V-700V (adjustable)

Switching freq, f = 100 kHz

Supply voltage – V_{in} = 100 ± 5%

Power rating = 14 W

Core used – Pot core.

Negative Grid supply design :

Output voltage - V_o = 450V-550V (adjustable)

Switching freq, f = 100 kHz

Supply voltage – V_{in} = 100 ± 5%

Power rating = 5.5 W

Core used – Pot core

Filament supply design :

Output voltage - V_o = 8V-10V (adjustable)

Switching freq, f = 100 kHz

Supply voltage – V_{in} = 100 ± 5%

Power rating = 90 W

Core used – Pot core

B. PWM Controllers

The selection of PWM controller IC is based on outputs required and the maximum duty cycle operation, switching frequency ,the peak current of the output based on this the UC1526 is selected.The UC1526 is a high performance pulse width modulator integrated circuit intended for fixed frequency switching regulators and other power control applications.

C. Features of UC1526

- *To 35V Operation*
- *V Reference Trimmed To 1%*
- *1Hz To 400kHz Oscillator Range*
- *Dual 100mA Source/Sink Outputs*
- *Digital Current Limiting*
- *Double Pulse Suppression*
- *Programmable Deadtime*
- *Under-Voltage Lockout*
- *Programmable Soft-Start*
- *Wide Current Limit Common Mode Range*

VI. SIMULATIONS AND RESULTS

SPICE is a general purpose circuit program that simulates electronic circuits.In this project, OrCAD PSpice 9 and 16.3 versions are used and Matlab software is used to design compensation circuit.

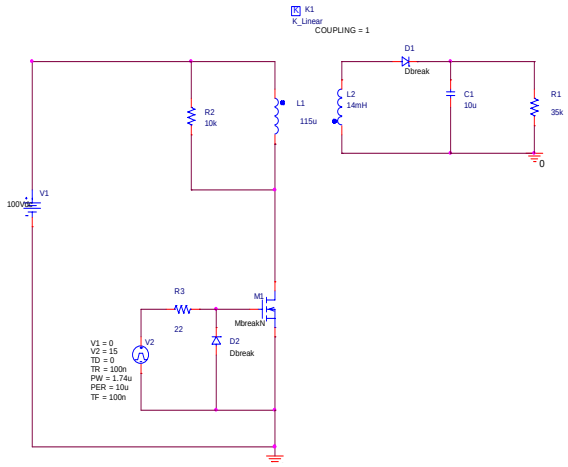

Fig. 5: Circuit diagram for Positive Grid supply

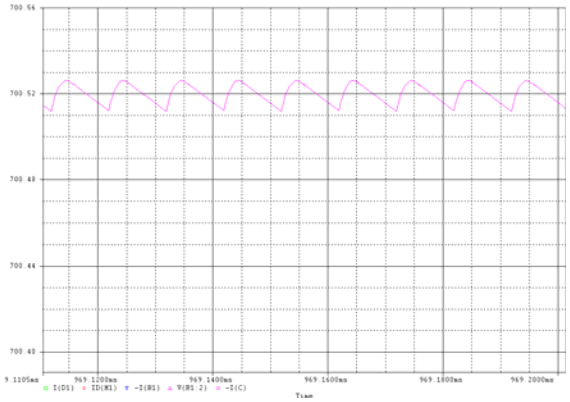

Fig. 5.a. Output voltage V_o=700V

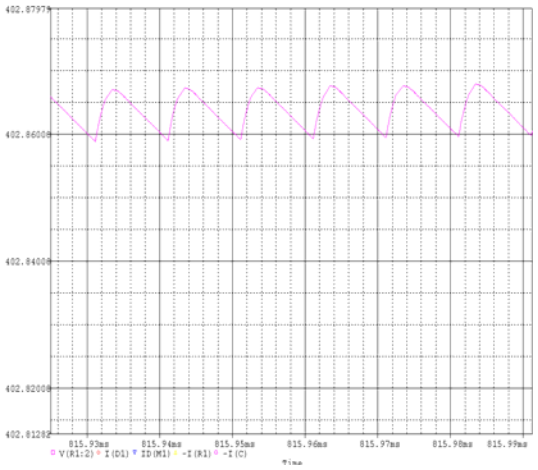

Fig. 5.b : Output voltage V_o=400V

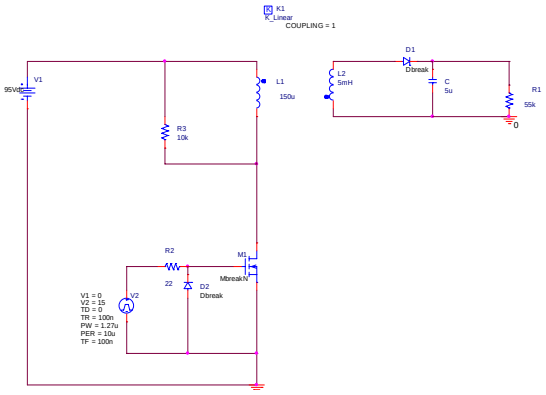

Fig. 6 : Circuit diagram for Negative Grid supply

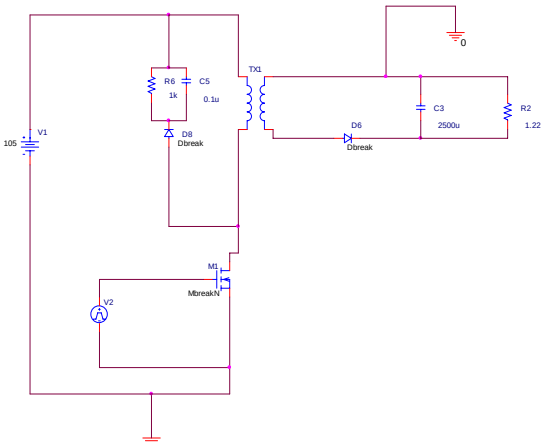

Fig. 7 : Circuit diagram for filament supply

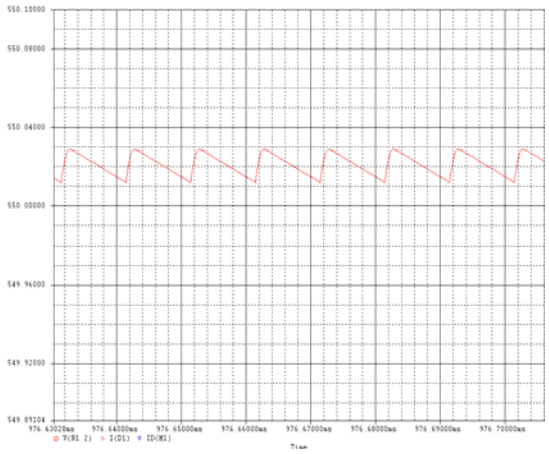

Fig. 6.a : Output voltage V_o=550V

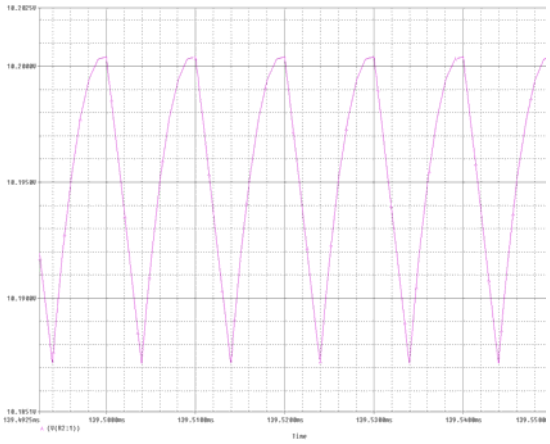

Fig. 7.a. output voltage V_o=10V

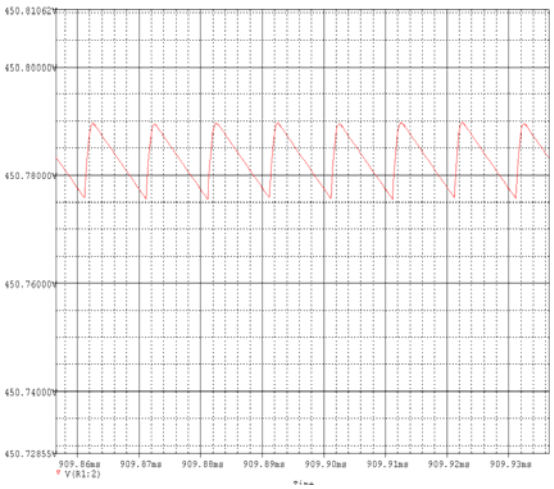

Fig. 6.b. Output voltage V_o=450V

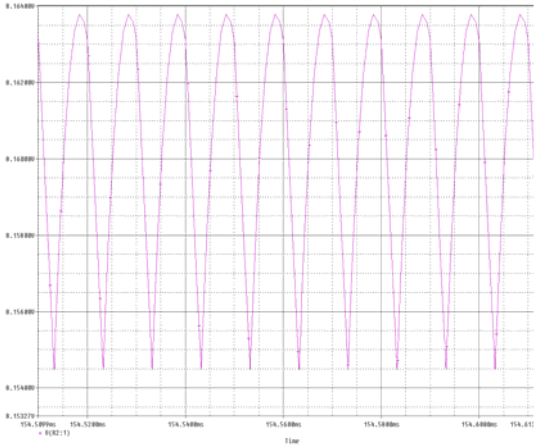

Fig. 7.b : Output voltage V_o=8 V

A. *FEEDBACK LOOP COMPENSATION*

Bode plot for Positive Grid system

The T.F of Flyback Converter [2] in DCM

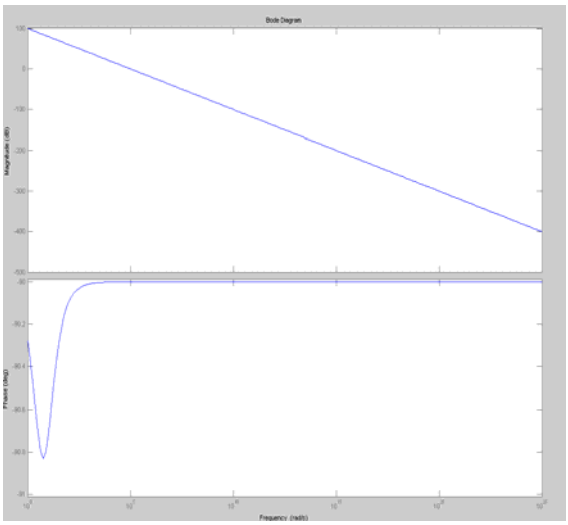

Fig. 8 : Bode plot for Positive Grid system

Results:

PM=INF , BW=15Khz,GM=90

Bode plot for Negative Grid system

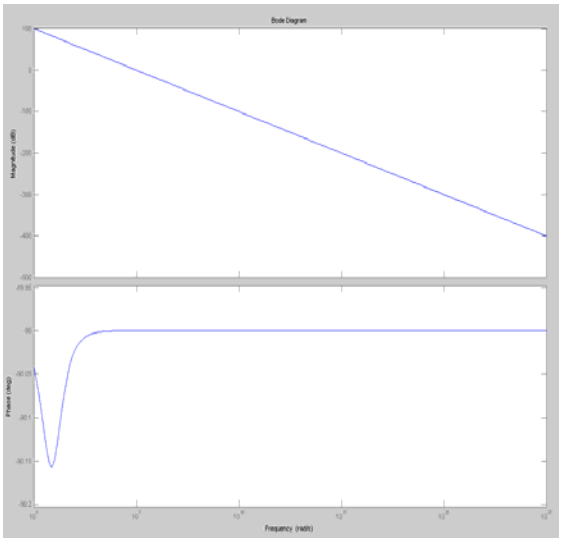

Fig. 9 : Bode plot for Negative Grid system

Results:

PM=INF , BW=15Khz,GM=90

Bode plot for filament Power supply

The T.F of Flyback Converter [2] in CCM

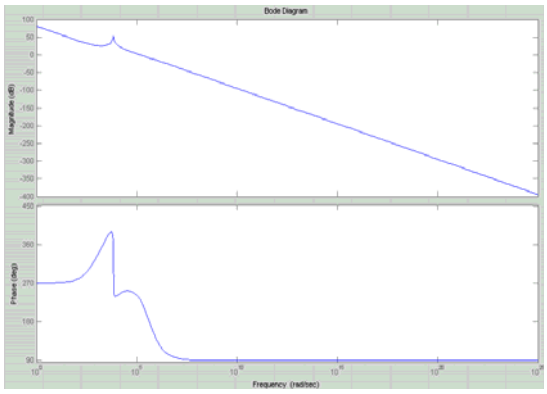

Fig.10 : Bode plot for filament Power supply

Results:

GM=2.7993 PM =52.4276 BW = 21Khz

VII. CONCLUSION

The fly back converter topology is best suited for application less than 100W. The TWT requirements are meet with the selected topology. The increase in switching frequency and use of pot core has resulted in the reduction in size and weight of SMPS.

ACKNOWLEDGEMENTS

First of all,I would like to thank Dr.R.Jayapal , HOD, EEE Dept.RVCE, Bangalore, providing right academic environment and valuable guide lines.

It is a matter of immense pleasure to express sincere thanks to Mr. Venkatesh Prabhu Scientist 'D', B-Radar,LRDE, DRDO,for accepting me as a project trainee under his supervision and guidance.

I thank Mrs. Dr.S.G.Srivani, Associate Professor,EEE Dept. RVCE, for her continuous support and guidance.

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