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CRITICAL ANALYSIS OF SiC SIT DESIGN AND PERFORMANCE BASED UPON MATERIAL AND DEVICE PROPERTIES

By

YunMo Sung

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Submitted to the Faculty of
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Recently, the need for high power, high frequency devices continues to grow with the increase in wireless communication, radar systems, HDTV, digital communication, and other military application of the RF spectrum. Traditionally when higher power is needed, one needs to either combine the output power of multiple devices or use vacuum tubes, which are still uncontested at very high power levels, capable of up to a few hundred kilowatts at 5*GHz* [11]. But wide band gap semiconductor devices capable of competing in this application. Moreover, the static induction transistor(SIT) in silicon carbide can provide very high total power at microwave frequency. This is due to the vertical structure of the SIT which consists of a vertical channel that is defined by a mesa with gate electrodes of the Schottky type to control the current between a top side source contact and a drain contact on the backside of the wafer.

This thesis demonstrates that through careful modeling by means of simulations and inclusion of all significant device physics, good agreement is reached

between theoretical prediction and simulation results. It is shown in particular that by careful choice of the device critical parameters, such as mesa width, gate length, and contact resistance, SIT should be able to obtain cut-off frequency up to 42*GHz* and shown temperature simulation results of SIT.

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TABLE OF CONTENTS

Page

ACKNOWLEDGMENTS ii

LIST OF TABLES v

LIST OF FIGURES vi

CHAPTER

I. INTRODUCTION 1

1. Background :Review 1
2. Properties of SiC 3
    2.1 Crystal Structure 3
    2.2 Energy Band Structure 5
    2.3 Intrinsic carrier concentration 5
    2.4 Low field mobility 6
    2.5 Thermal conductivity 8

    References 10

II. STATIC INDUCTION TRANSISTOR 12

1. Device Structure 12
2. Operation 15
    2.1 Ohmic region region 18
    2.2 Exponential region 19
    2.3 Space Charge Limited Conduction region 19
3. Limitations for Design 20
    3.1 Thermal Limit on Total Power 20
    3.2 Impedance and Area Limit on Total Power 21
4. Qualification of the simulation 23
    4.1 Thermal Equilibrium condition 23
    4.2 Compare to measured data for parameter fitting 27

    References 30

CHAPTER Page

III. STATIC CHARATERISTICS 31

1. Device Physics 31
2. Voltage Gain and Maximum Current Physics 32
3. Basic Dimension parameters for SIT Design 33
4. Drain and Source Resistance 40
5. Basic considerations of Power and frequency performance 41

References 42

IV. HIGH FREQUENCY CHARATERISTICS 43

1. Small Signal Equivalent Circuit of SIT 43
2. Effect of contact Resistance 49
3. Effect of Mobility 58
   3.1 Analytic Mobility 58
   3.2 Perpendicular Electric Mobility Model 58
   3.3 Surface Mobility Model 59
   3.4 Hewlett-Packard Mobility Model 59
4. Effect of Saturation Drift velocity 62
5. Considerations for high frequency SIT Design 65

References 67

V. TEMPERATURE SIMULATIONS 69

1. Theoretical Considerations 69
2. Gate-Drain Breakdown Voltage 70
3. Temperature Dependent DC performances 79
4. Temperature Dependent Frequency performances 84

References 96

VI. CONCLUSION AND FUTURE WORK 97

1. Conclusion 97
2. Future Works 100

References 101

APPENDICES

A. Reported gain of SiC SIT's over the past 5 years 102
B. Simulation Results for I-V Characteristics 104
C. Conversion from Y-parameter to S-parameter 129
D. Simulation Results for Frequency and Transconductance Characteristics 131

LIST OF TABLES

TABLE Page

1.1 Properties of SiC polytypes 4

LIST OF FIGURES

FIGURE Page

1.1 Intrinsic carrier concentrations *vs* temperature of 4H-Sic, Si and GaAs ···· 6

1.2 Low field electron and hole mobility of 4H-SiC, Si, and GaAs at room temperature ··· 7

1.3 Mobility *vs* doping and temperature for electron and holes 4H-SiC, GaAs, Si ··· 9

2.1 Structure of recessed gate static induction transistor ··· 13

2.2 Structure of well-suited recessed gate static induction transistor ··· 14

2.3 Structure of surface gate static induction transistor ··· 14

2.4 SIT's three regions of current flow ··· 16

2.5 Conduction Band Energy of one half drift channel ··· 16

2.6 Conduction Band Energy in some bias ··· 17

2.7 Conduction Band Energy in the center of channel (X=0) for different drain voltages ··· 17

2.8 Electron current densities inside the SIT ··· 24

2.9 Current densities inside the SIT ··· 25

2.10 The simulation result of electron quasi-Fermi potential under thermal equilibrium ··· 26

2.11 The simulation result of hole quasi-Fermi potential under thermal equilibrium. ··· 26

2.12 Output I-V curve for a 0~50 [*V*] drain voltage scales. The "+" symbols are measured data and the solid line are the results obtained from Medici Simulations. ··· 27

FIGURE Page

2.13 Output I-V curve for a 0~130 [V] drain voltage scales. The "+" symbols are measured data and the solid line are the results obtained from Medici Simulations. 28

3.1 On resistance, voltage gain, maximum current and knee voltage 32

3.2 I-V curves for various gate length and mesa widths with $N_D = 5\cdot10^{15}\ cm^{-3}$, L_{sg}=0.5 μm and $t=2a$. Curve start at a gate voltage Vg=0 and progress in -2V steps 36

3.3 Maximum Current for various gate lengths and mesa widths on the IV curves. 37

3.4 Maximum Current for various gate lengths and mesa widths. 38

3.5 Blocking gain as a function of gate lengths and mesa widths 39

3.6 Cut-off Frequency as function of gate lengths and mesa widths for fixed voltage gain 10 dB 41

4.1 Pi-equivalent circuit for small signal modeling 45

4.2 General Hybrid-Pi equivalent circuit 46

4.3 Magnitude of Y_f and Y_o as function of frequency at bias point $V_d = 10V$, $V_g = 0V$. 47

4.4 Gate-Drain and Gate-Source Capacitance as function of frequency at bias point $V_d = 10V$, $V_g = 0\ V$. 48

4.5 Cut-off Frequency as a function of gate length and mesa width with drain contact resistivity $1\cdot10^{-5}$ [$\Omega\ cm^2$] 50

4.6 Transconductance as a function of gate length and mesa width at drain contact resistivity $1\cdot10^{-5}$ [$\Omega\ cm^2$], source contact resistivity $0.5\cdot10^{-5}$, $1\cdot10^{-5}$, $5\cdot10^{-5}$, $10\cdot10^{-5}$, $50\cdot10^{-5}$ [$\Omega\ cm^2$], from top to bottom, respectively 51

4.7 Gate-source capacitance as a function of gate length and mesa width with drain contact resistivity $1\cdot10^{-5}$ [$\Omega\cdot cm^2$], source contact resistivity $0.5\cdot10^{-5}$, $1\cdot10^{-5}$, $5\cdot10^{-5}$, $10\cdot10^{-5}$, $50\cdot10^{-5}$ [$\Omega\ cm^2$], from top to bottom, respectively 52

4.8 Gate-drain capacitance as a function of gate length and mesa width at drain contact resistivity $1\cdot10^{-5}$ [$\Omega\cdot cm^2$], source contact resistivity $50\cdot10^{-5}$, $10\cdot10^{-5}$, $5\cdot10^{-5}$, $1\cdot10^{-5}$, $0.5\cdot10^{-5}$ [$\Omega\ cm^2$], from top to bottom, respectively. 53

4.9 Cut-off Frequency as a function of gate length and mesa width with source contact resistivity $1.0 \cdot 10^{-5}$ [Ω cm^2], drain contact resistivity $0.5 \cdot 10^{-5}$, $1 \cdot 10^{-5}$, $5 \cdot 10^{-5}$, $10 \cdot 10^{-5}$, $50 \cdot 10^{-5}$ [Ω cm^2], from top to bottom, respectively ········· 54

4.10 Transconductance as a function of gate length and mesa width at source contact resistivity $1 \cdot 10^{-5}$ [Ω cm^2], from top drain contact resistivity $0.5 \cdot 10^{-5}$, $1 \cdot 10^{-5}$, $5 \cdot 10^{-5}$, $10 \cdot 10^{-5}$, $50 \cdot 10^{-5}$ [Ω cm^2], respectively. ········· 55

4.11 Gate-source Capacitance as a function of gate length and mesa width with source contact resistivity $1 \cdot 10^{-5}$ [Ω cm^2], from top drain contact resistivity $50 \cdot 10^{-5}$, $10 \cdot 10^{-5}$, $5 \cdot 10^{-5}$, $1 \cdot 10^{-5}$, $0.5 \cdot 10^{-5}$ [Ω cm^2], respectively ········· 56

4.12 Gate-Drain Capacitance as a function of gate length and mesa width at source contact resistivity $1 \cdot 10^{-5}$ [Ω cm^2], from top drain contact resistivity $50 \cdot 10^{-5}$, $10 \cdot 10^{-5}$, $5 \cdot 10^{-5}$, $1 \cdot 10^{-5}$, $0.5 \cdot 10^{-5}$ [Ω cm^2], respectively 57

4.13 Cut-off Frequency depend on mobility model ········· 61

4.14 Cut-off Frequency in several mobility models, LSSMMOB : Analytic Mobility model, HPMOB : Hewlett Parkard mobility, SRFMOB : Surface mobility model, PRPMOB : Perpendicular Electric Mobility········· 61

4.15 Cut-off Frequency depend on Saturation Drift velocity ········· 62

4.16 Transconductors depend on Saturation Drift velocity, from top to bottom, $2.5 \cdot 10^7$, $2.2 \cdot 10^7$, $2.0 \cdot 10^7$ and $1.5 \cdot 10^7$[cm/s], respectively ········· 63

4.17 Gate-drain capacitances in other saturation drift velocity, from top to bottom, v_{sat} : $2.5 \cdot 10^7$, $2.2 \cdot 10^7$, $2.0 \cdot 10^7$, and $1.5 \cdot 10^7$[cm/s] ····· 64

4.18 Gate-source capacitances in other saturation drift velocity, from top to bottom, v_{sat} : $1.5 \cdot 10^7$, $2.0 \cdot 10^7$, $2.2 \cdot 10^7$, and $2.5 \cdot 10^7$[cm/s] ········· 65

4.19 Cut-off Frequency as a function Doping N_D and Gate length with source contact resistivity $1.0 \cdot 10^{-5}$ [$\Omega \cdot cm^2$] ········· 66

5.1 Avalanche Breakdown voltage and Electric Field at Impact Ionization integral reaches unity for a) 300K, b) 400K, c) 500K, d) 600K, e) 700K, d) 800K ········· 72

5.2 Avalanche breakdown voltage as a function of mesa width and gate length with doping $5 \cdot 10^{16}$ [cm^{-3}] for temperature increase ········· 76

FIGURE Page

5.3 Avalanche Breakdown voltage as a function of mesa width and gate length with the doping $2\cdot10^{17}$ [cm^{-3}] for temperature increase 77

5.4 Avalanche Breakdown voltage with doping $5\cdot10^{16}$ [cm^{-3}] for temperature increase, from top to bottom, 300*K*, 400*K*, 500*K*, 600*K*, 700*K*, 800K 78

5.5 Avalanche Breakdown voltage with temperature increasing for the doping $2\cdot10^{17}$ [cm^{-3}] from top to bottom 300*K*, 400*K*, 500*K*, 600*K*, 700*K*, 800*K* 78

5.6 I-V Curves at (a) T=300*K*, (b) T=400*K*, (c) T=500*K*, (d) T=600*K*, (e) T=700*K*, (f) T=800*K*, respectively. The ten curves in each figures correspond to V_g=0*V*, -2*V*, -4*V*, -6*V*, -8*V*, -10*V*, -12*V*, -14*V*, -16*V*, -18*V*, from the top to the bottom. 80

5.7 I-V Curves at T=300*K*, 400*K*, 500*K*, 600*K*, 700*K*, 800*K* for $V_g = -8V$, -10*V*, from the top to the bottom, respectively 83

5.8 Maximum Current at T=300*K*, 400*K*, 500*K*, 600*K*, 700*K*, 800*K* for $2\cdot10^{17}$ cm^{-3}, from top to bottom, respectively 84

5.9 h_{21} parameter from simulated Y-parameter showing the bandwidth-gain product (f_T) of 9.6 *GHz* at 600 [K]. Bias point is $V_d = 50$ *V*, $V_g = -4$ *V* 86

5.10 h_{21} parameter from simulated Y-parameter with bais point is $V_d = 50$ *V*, $V_g = -4$ *V*, Doping *5.0e+16* cm^{-3}, from top to bottom, 300, 400 500, 600, 700, 800 [K], respectively 87

5.11 Cut-off frequency as a function of gate length and mesa width for a bias point of $V_d = 50$ *V*, $V_g = -4$ *V*, Doping *5.0e+16* cm^{-3}, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively 88

5.12 Transconductance plotted as a function of gate length and mesa width for a bias point of $V_d = 50$ *V*, $V_g = -4$ *V*, Doping value *5.0e+16* cm^{-3}, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively. 89

5.13 Gate-Source capacitance plotted as a function of gate length and mesa width for a bias point of $V_d = 50$ *V*, $V_g = -4$ *V*, Doping value *5.0e+16* cm^{-3}, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively 90

5.14 Gate-Drain capacitance as a function of gate length and mesa width for a bias point of $V_d = 50\ V,\ V_g = -4\ V$, Doping value $5.0e+16\ cm^{-3}$, from top to bottom, 800, 700, 600, 500, 400, 300 [K], respectively 91

5.15 Cut-off frequency plotted as a function of gate length and mesa width for a bias point of $V_d = 25\ V,\ V_g = 0\ V$, Doping value $5.0e+16\ cm^{-3}$, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively 92

5.16 Transconductance plotted as a function of gate length and mesa width for a bias point of $V_d = 25$ V, $V_g = 0$ V, Doping value 5.0e+16 cm^{-3}, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively 93

5.17 Gate-Source capacitance plotted as a function of gate length and mesa width for a bias point of $V_d = 25\ V,\ V_g = 0\ V$, Doping value $5.0e+16\ cm^{-3}$, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively 94

5.18 Gate-Drain capacitance plotted as a function of gate length and mesa width for a bias point of $V_d = 25\ V,\ V_g = 0\ V$, Doping value $5.0e+16\ cm^{-3}$, from top to bottom curves, 800, 700, 600, 500, 400, 300 [K], respectively 95

B.1 I-V curves for different values of L_g and $2a$, with $N_D = 5\cdot10^{15}\ [cm^{-3}]$ and 300 [K]. 105

B.2 I-V curves for different values of L_g and $2a$, with $N_D = 5\cdot10^{15}\ [cm^{-3}]$ and 400 [K]. 106

B.3 I-V curves for different values of L_g and $2a$, with $N_D = 5\cdot10^{15}\ [cm^{-3}]$ and 500 [K] 107

B.4 I-V curves for different values of L_g and $2a$, with $N_D = 5\cdot10^{15}\ [cm^{-3}]$ and 600 [K]. 108

B.5 I-V curves for different values of L_g and $2a$, with $N_D = 5\cdot10^{15}\ [cm^{-3}]$ and 700 [K]. 109

B.6 I-V curves for different values of L_g and $2a$, with $N_D = 5\cdot10^{15}\ [cm^{-3}]$ and 800 [K]. 110

B.7 I-V curves for different values of L_g and $2a$, with $N_D = 1\cdot10^{16}\ [cm^{-3}]$ and 300 [K]. 111

FIGURE Page

B.8 I-V curves for different values of L_g and $2a$, with $N_D = 1 \cdot 10^{16}$ [cm^{-3}] and 400 [K]. 112

B.9 I-V curves for different values of L_g and $2a$, with $N_D = 1 \cdot 10^{16}$ [cm^{-3}] and 500 [K]. 113

B.10 I-V curves for different values of L_g and $2a$, with $N_D = 1 \cdot 10^{16}$ [cm^{-3}] and 600 [K]. 114

B.11 I-V curves for different values of L_g and $2a$, with $N_D = 1 \cdot 10^{16}$ [cm^{-3}] and 700 [K]. 115

B.12 I-V curves for different values of L_g and $2a$, with $N_D = 1 \cdot 10^{16}$ [cm^{-3}] and 800 [K]. 116

B.13 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{16}$ [cm^{-3}] and 300 [K]. 117

B.14 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{16}$ [cm^{-3}] and 400 [K]. 118

B.15 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{16}$ [cm^{-3}] and 500 [K]. 119

B.16 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{16}$ [cm^{-3}] and 600 [K]. 120

B.17 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{16}$ [cm^{-3}] and 700 [K]. 121

B.18 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{16}$ [cm^{-3}] and 800 [K]. 122

B.19 I-V curves for different values of L_g and $2a$, with $N_D = 2 \cdot 10^{17}$ [cm^{-3}] and 300 [K]. 123

B.20 I-V curves for different values of L_g and $2a$, with $N_D = 2 \cdot 10^{17}$ [cm^{-3}] and 400 [K]. 124

B.21 I-V curves for different values of L_g and $2a$, with $N_D = 2 \cdot 10^{17}$ [cm^{-3}] and 500 [K]. 125

B.22 I-V curves for different values of L_g and $2a$, with $N_D = 2 \cdot 10^{17}$ [cm^{-3}] and 600 [K]. 126

FIGURE Page

B.23 I-V curves for different values of L_g and $2a$, with $N_D = 2 \cdot 10^{17}$ [cm^{-3}] and 700 [K]. 127

B.24 I-V curves for different values of L_g and $2a$, with $N_D = 2 \cdot 10^{17}$ [cm^{-3}] and 800 [K]. 128

D.1 Cut-off frequency for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{15}$ [cm^{-3}], from top to bottom, 300, 400, 500, 600, 700, 800 [K], respectively. 132

D.2 Cut-off frequency for different values of L_g and $2a$, with $N_D = 1 \cdot 10^{16}$ [cm^{-3}], from top to bottom, 300, 400, 500, 600, 700, 800 [K], respectively. 132

D.3 Cut-off frequency for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{16}$ [cm^{-3}], from top to bottom, 300, 400, 500, 600, 700, 800 [K], respectively. 133

D.4 Cut-off frequency for different values of L_g and $2a$, with $N_D = 2 \cdot 10^{17}$ [cm^{-3}], from top to bottom, 300, 400, 500, 600, 700, 800 [K], respectively. 133

D.5 Transconductance for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{15}$ [cm^{-3}], from top to bottom, 300, 400, 500, 600, 700, 800 [K], respectively. 134

D.6 Transconductance for different values of L_g and $2a$, with $N_D = 1 \cdot 10^{16}$ [cm^{-3}], from top to bottom, 300, 400, 500, 600, 700, 800 [K], respectively. 134

D.7 Transconductance for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{16}$ [cm^{-3}], from top to bottom, 300, 400, 500, 600, 700, 800 [K], respectively. 135

D.8 Transconductance for different values of L_g and $2a$, with $N_D = 2 \cdot 10^{17}$ [cm^{-3}], from top to bottom, 300, 400, 500, 600, 700, 800 [K], respectively. 135

CHAPTER I

INTRODUCTION

1 Background :Review

Silicon Carbide (SiC) as a semiconductor material is provided with several special properties. The primary research areas for SiC have been high power RF devices, high temperature electronics and radiation hard electronics (space electronics and nuclear reactor). This can be attributed to special material properties of SiC. The large bandgap of SiC (3.2 *eV* for 4H polytype) and high electron field strength (3.0 *MV/cm*) allows for high voltage applications and reduces series resistance in the lightly-doped drift region. The high saturated drift velocity of SiC is also advantageous in the development of high speed devices such as high frequency amplifiers [1]. Table 1-1 shows a comparison of material parameters for various semiconductors.

SiC's Static Induction Transistor (SIT) is well-suited for high power and high frequency (71 *Kw* demonstrated at UHF). The leading parameters for design are developed through careful modeling by means of simulations and inclusion of all significant device physics, this thesis demonstrates that good agreement is reached between theoretical prediction and results of various simulations, such as temperature, saturation drift velocity, and contact resistance.

The SiC Static Induction Transistor is based on the original SIT concepts developed in 1950 [2] by Nishizawa, which have received continued development for

the past five decades [3-5]. As compared to a Si Bipolar Junction Transistor (BJT), the SIT has advantages in being a majority carrier device, voltage-controlled, and often higher breakdown voltage and input impedance. While most SIT development has occurred in Si, renewed interest in the use of SiC SIT's over the past 10 years has occurred because of SiC's ten-fold advantage (3 *MV/cm*) in critical field strength and nearly two-fold advantage in saturated electron velocity (1.6~2.2 x 10^7 *cm/s*) [6-10]. Additionally, SiC has an extremely high thermal conductivity (θ_k = 3 *W/cm·K*) which far surpasses that of Si and GaAs, and allows an increased junction operating temperature (T_j) to nearly 400 ℃ because of the high θ_k and dramatically reduced pn junction leakage currents resulting from its wide (E_g = 3.2 *eV* for the 4H-SiC polytype) bandgap. By use of SiC, it is thus possible to increase the voltage (power) rating of high-frequency amplifiers, and also increase the power density by a factor of 4 to 10 in UHF to S-band transistors. Parasitic capacitances are reduced by shrinking the device area while maintaining the power level and higher input/output impedance of the devices often requires little or no impedance matching. Limitations, which have slowed commercial insertion of SiC devices to date, include wafer size (75 *mm* maximum diameter available in 2002), wafer cost, device/epitaxy processing, and wafer defects. Currently, solid state devices are available provide a total power of tens of watts at 1 *GHz*, such as the silicon based bipolar transistor, and a few watts at 10 *GHz*, like the GaAs based MESFET [21]. When higher power is needed, one needs to either combine the output power of multiple devices or use vacuum tubes, which are still uncontested at very high power levels, capable of up to a few hundred kilowatts at 5 *GHz* [11]. High total power for a single device means that a smaller

number of devices is needed to build a high power amplifier. This should lead to higher reliability, easier circuit design and lower cost.

2 Properties of SiC

2.1 Crystal Structure

SiC exhibit a one-dimensional polymorphism called polytypism. An almost infinite number of SiC polytypes are possible, and approximately 200 polytypes have already been discovered.[12] SiC polytypes differentiated by the stacking sequence of each tetrahedrally bonded Si-C bilayer. With the exception of 2H and 3C, all of the polytypes form 1-D superlattice structure [13]. The polytypes are divided into three basic crystallographic categories; cubic (C), hexagonal (H), and rhombohedral (R). Cubic SiC has only one possible polytype, and is referred to as 3C-SiC or ß-SiC. Each SiC bilayer can be oriented into only three possible positions with respect to the lattice while the tetrahedral bonding is maintained. If these three layers are arbitrarily denoted *A, B,* and *C*, and the stacking sequence is *ABC/ABC*.... then the crystallographic structure is cubic zinc blende and referred to as 3C-SiC. It possesses the smallest bandgap (~2.4 *eV*) [14], and one of the largest electron mobility of all the SiC polytypes, and has been grown on 6H-SiC substrate. If the stacking of the bi-layers is *AB/AB….,* then referred to as 2H-SiC, stacking sequence with *ABCB/ABCB*.... and *ABCACB/ABCACB*…., is referred to as 4H-SiC and 6H-SiC. 4H-SiC consists of an equal number of cubic and hexagonal bonds. 6H-SiC is composed of two-thirds cubic bonds and one-third hexagonal bonds.

These SiC polytypes have substantially different thermal, optical, and electrical properties due to their different crystal structure. The properties of the commonly used SiC polytypes which are most important for device applications are comparing with the similar properties of silicon and gallium arsenide in Table 1.1[14, 20].

The properties of SiC, such as wide band gap, excellent thermal conductivity, high breakdown filed, high saturation drift velocity, provide a great deal of attractiveness in high speed, high power devices working at elevated temperature and radiation, such as high power switch and high power amplifier. Also, SiC's properties of high chemical stability and radiation tolerance have attraction for aviation, nuclear, and space applications.

Table 1.1 Properties of SiC polytypes

Property	**Si**	**GaAs**	**4H-SiC**	**6H-SiC**	**3C-SiC**
Band Gap(eV)	1.12	1.42	3.2	3	2.4
Breakdown Field (MV/cm)	0.6	0.6	3.0	3.0	3.0
Saturated Drift Velocity (cm/s)	10^7	10^7	$2.2x10^{7‡}$	$1.9x10^{7‡}$	$2.5x10^7$
Thermal Conductivity (w/cm °C)	1.5	0.5	4.9	4.9	5
Electron Mobility (cm^2/Vs)†	1100	6000	900	370	750
Hole Mobility (cm^2/Vs)†	420	320	115	90	40

†: at doped concentration of 10^{17} cm^{-3}
‡: [15]

2.2 *Energy Band Structure*

The energy band structure of SiC strongly depends on the polytypes. Both experimental and theoretical results show that the valence band maxima for all common polytypes are located at the center of the Brillouin zone (Γ point). For all polytypes but 2H-SiC the conduction band minimum of 4H-SiC is found to be at the M point of the Brillouin zone. The indirect energy band gap varies with the polytype reaching values between E_g=2.3 *eV* for 3C-SiC and E_g=3.2 *eV* for 4H-SiC. 4H-SiC has the largest energy band gap among all common SiC polytypes.

The temperature dependent energy band gap is not known for 4H-SiC. Experiment results in Ref. [16] show that the temperature coefficients of energy band gap for 6H-SiC and 3C-SiC are -3.3 x 10^{-4} *eV/K* and -5.8 x 10^{-4} *eV/K,* respectively, Since crystal structure of 4H-SiC is closer to 6H-SiC than to 3C-SiC, following the same approach as in Ref.[17] and using the temperature coefficient of the energy band gap of 4H-SiC, the following temperature dependent band gap of 4H-SiC is obtained

$$E_g(T) = 3.19 - 3.3 \times 10^{-4}(T - 300K)\ eV \tag{1.1}$$

2.3 *Intrinsic carrier concentration*

In semiconductor 4H-SiC, effective densities of states in the conduction and valence bands can be expressed as

$$N_c = (\frac{4\pi m_c kT}{h^2}) \tag{1.2}$$

$$N_v = (\frac{4\pi m_v kT}{h^2}) \tag{1.3}$$

where *k* is the Boltzman constant. For 4H-SiC m_c(300k) = 0.76m_0, m_v(300k) $\approx 1.2 m_0$, m_0(300K) = 9.11x10^{-31} *Kg* in room temperature.

The intrinsic carrier concentration at thermal equilibrium is given by

$$n_i = \sqrt{N_c N_v} \exp(\frac{-E_g(T)}{2kT}) \quad (1.4)$$

The temperature dependant intrinsic carrier concentrations of 4H-SiC, Si, and GaAs according to are shown Figure 1.1.

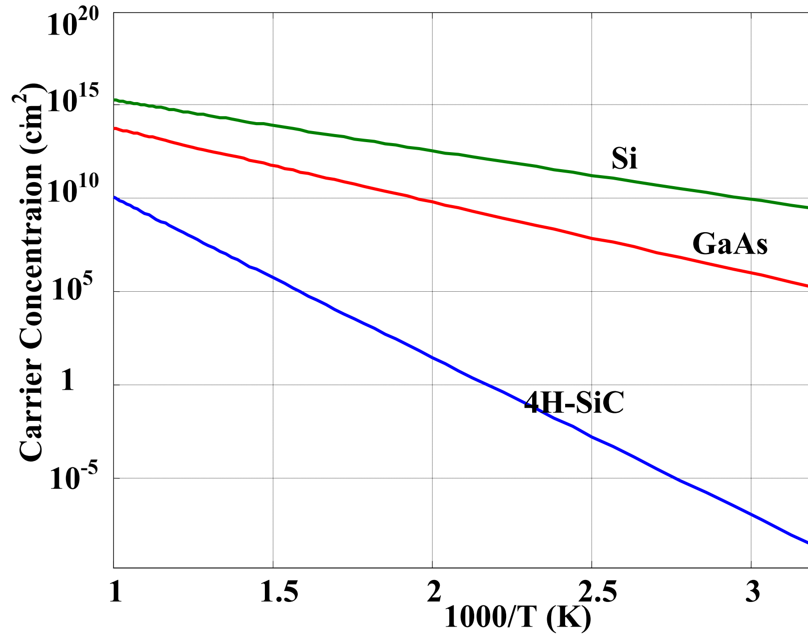

Figure 1.1 Intrinsic carrier concentrations *vs* temperature of 4H-Sic, Si and GaAs.

2.4 Low field mobility

The low field mobility model for 4H-SiC can be expressed as

$$\mu_{n,p} = \mu_{n,p}^{\min} + \frac{\mu_{n,p}^{delta}}{1 + (\frac{N_D + N_A}{N_{n,p}^{\mu}})^{\gamma_{n,p}}} (\frac{T}{300K})^{\alpha_{n,p}} \quad (1.2)$$

where the electron set of data are $\mu_n^{\min}$ =0 cm²/(V sec), μ_n^{delta} =947 cm²/(V sec), N_n^{μ} =1.94×10^{17} cm²/(V sec), γ_n =0.61 and $\alpha_n = -2.15$; the hole set of data are $\mu_p^{\min}$=15.9 cm²/(V sec), μ_p^{delta} =108.1 cm²/(V sec), N_p^{μ}=1.76×10^{19} cm²/(V sec), γ_p =0.34 and $\alpha_p = -2.15$. Note: this mobility model does not contain the effects of electron-hole scattering, which may be important in power devices operating under high-injection conditions [17].

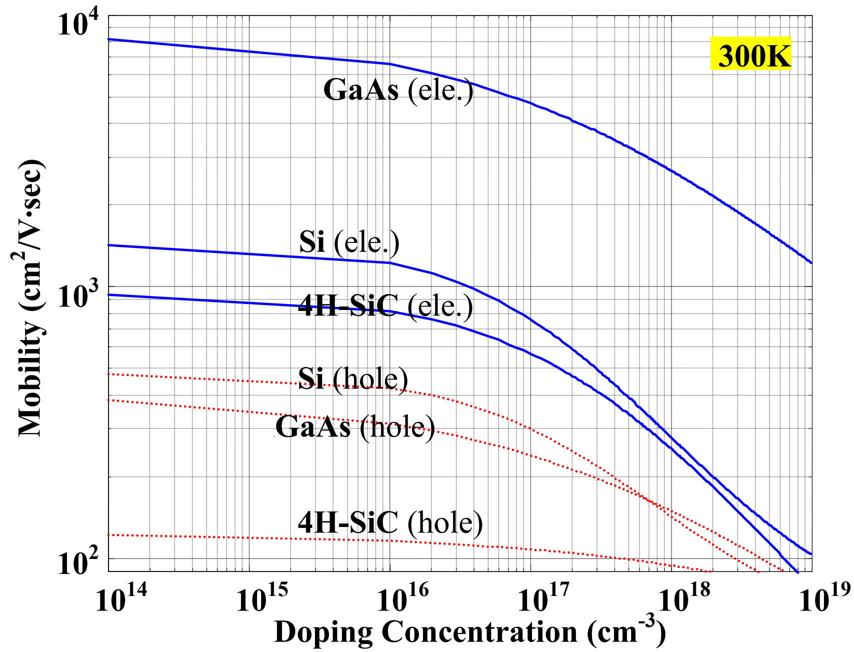

Figure 1.2 Low field electron and hole mobility of 4H-SiC, Si, and GaAs at room temperature

The low field mobility of 4H-SiC higher than those of 6H-SiC for both electrons and holes; the mobility of Si is high than that of 4H-SiC, and that of GaAs is highest. Thus GaAs has the tremendous advantage in high speed application field over both Si and 4H-SiC at low fields. The low field mobility of 4H-SiC, Si, and GaAs at room

temperature is shown in Figure 1.2. In the low doping case, as the temperature increases, the lattice atoms vibrate more about their mean position, thus effectively increasing in "size" and thereby increasing the chance of collisions. The mobility therefore decreases with increase *T*. The theoretical dependence is $\mu \propto T^{-\frac{3}{2}}$ [18] and it shown in Figure 1.3.

2.5 Thermal conductivity

The other important physical property of SiC is its high thermal conductivity. Typically, the thermal conductivity depends on polytypes and doping but the thermal conductivity of SiC exceeds that of copper (4.01$Wcm^{-1}K^{-1}$), silver ((4.29$Wcm^{-1}K^{-1}$), Al_2O_3 , and is about 5 times higher than that of Si. This is mainly due to the phonon dispersion relation distribution. Also, this property leads to a simple design of heat dissipation of the device and the circuit even in high temperature and high power field [19].

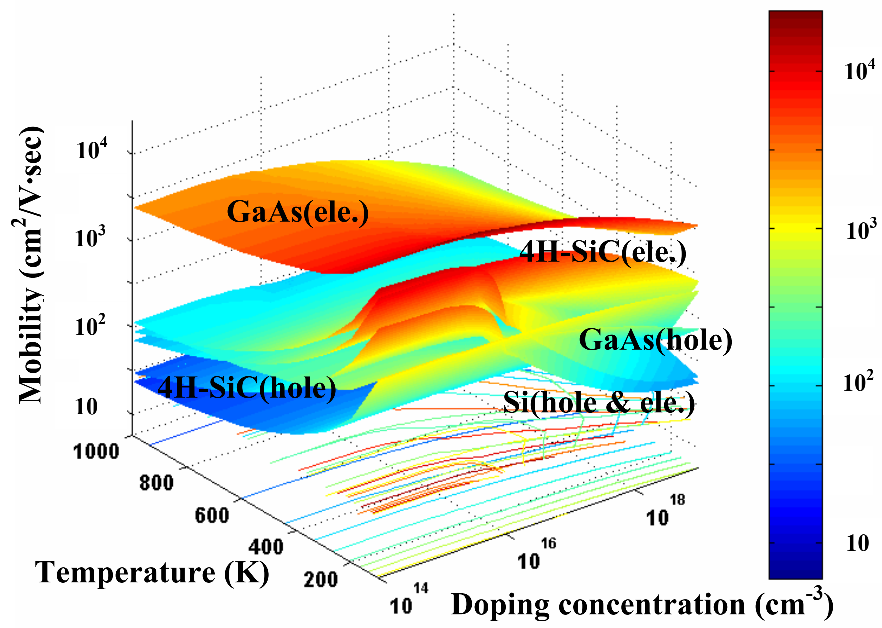

Figure 1.3 Mobility *vs* doping and temperature for electron and holes 4H-SiC, GaAS, Si.

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CHAPTER II

STATIC INDUCTION TRANSISTOR

1 Device Structure

Both recessed gate and planar gate SIT's have been fabricated in Si and SiC. However because of difficulty in deep ion implantation (p-type dopant Al implanted at energy of 380 keV has a peak range of only $0.42\mu m$ into SiC) and the lack of diffusion at temperatures below 1800 ℃, the recessed gate structure has been favored in SiC. Typical recessed gate SIT structures are shown in Fig. 2.1, with primary differences found in the gates. The gate may be a Recessed Gate - Bottom contact (RG-B), as shown in Fig. 2.1, or a RG with Sidewall and Bottom contact (RG-SB), as shown in Fig. 2.2 which provides a longer gate length (L_g). Increasing Lg improves gate control, voltage gain (μ), and transconductance (g_m), while reducing the output resistance (r_{DS}). The gate material may be formed from either a Schottky metal or a pn junction, and can be thought of as analogous to a vertical dual-gate MESFET or JFET structure, respectively. The gate depletes the channel from each side a distance (x_d) into the channel. The total channel thickness ($2a$), trench width (t), and drift region length (L_{gd}) are illustrated in Fig. 2.1. Planar gates can also be fashioned in SiC [1], but the recessed gate with a Schottky barrier offers the lowest parasitics and most efficient gating [2]. A PN junction gate can be used with higher gate resistance (R_g), but offers less gate-to-source leakage at a higher maximum junction temperature

(T_{jmax}) and potentially higher power density. The PN gate leakage at high temperatures in SiC devices is substantially reduced (proportional to the intrinsic carrier concentration of n_i or n_i^2) compared to Si or GaAs devices, and degradation of the Schottky contact is not limiting reliability if one uses a PN gate, as shown Fig. 2.3. PN gate also adds some cost to processing since additional p-type implant and activation anneal are required

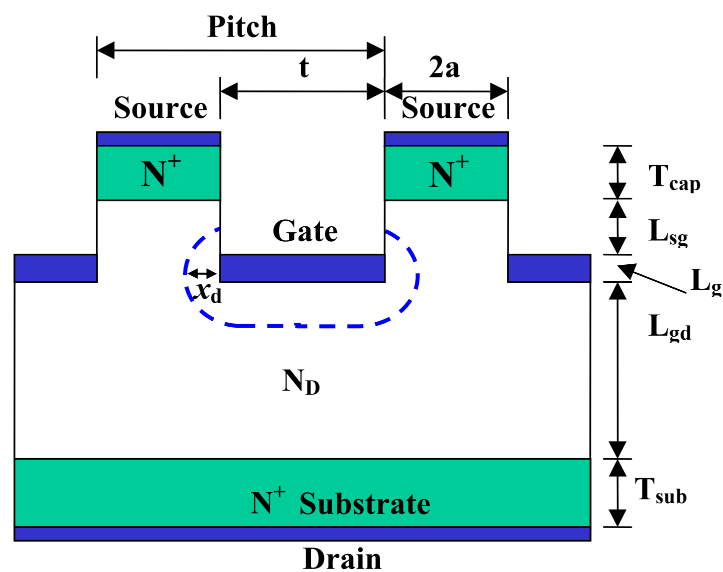

Figure 2.1 Structure of recessed gate static induction transistor.

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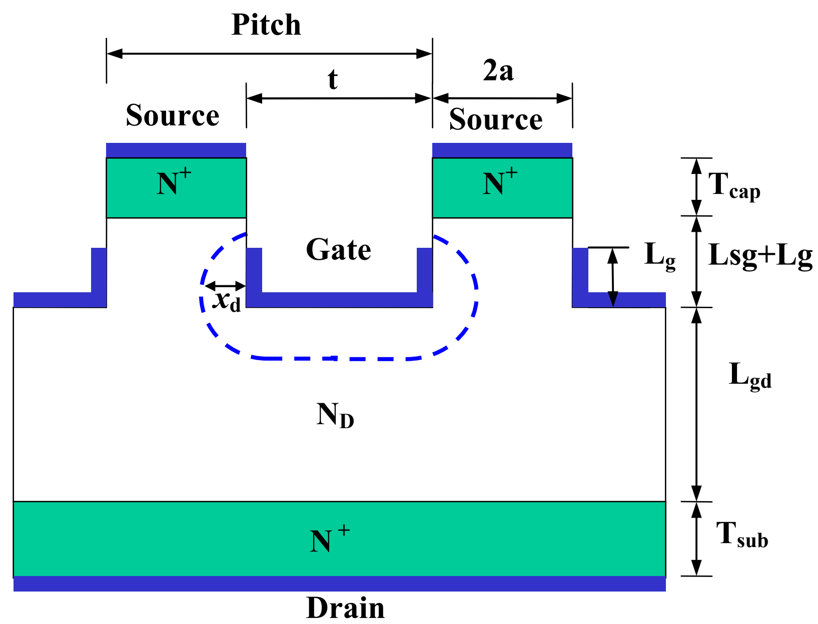


Figure 2.2 Structure of well-suited recessed gate static induction transistor

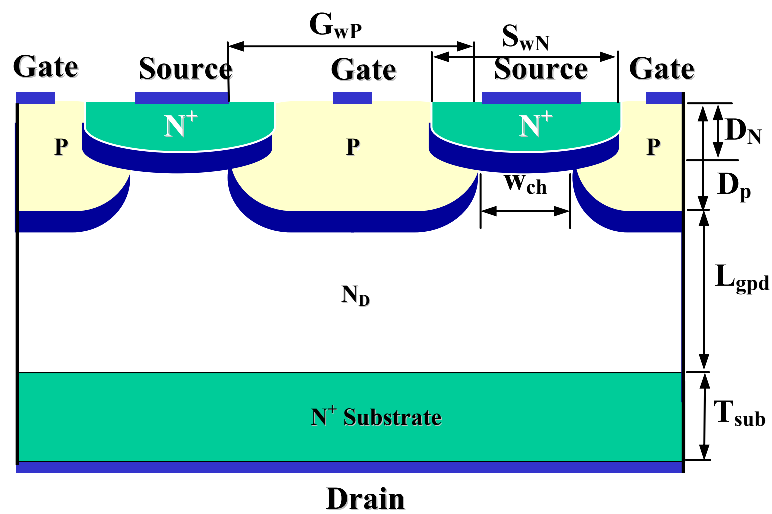


Figure 2.3 Structure of surface gate static induction transistor.

2 Operation

With $V_g = V_s = 0\ V$, the conventional SIT has its channel completely depleted ($x_d > a$). If $x_d < a$, which often done to increase maximum total current and power, then the SIT is referred to as mixed-mode [4]. Other terms for the SIT include gridstor, VFET (Vertical FET), or Permeable Base Transistor (PBT) [5]. PBT's often have extremely short gates ($L_g < a < x_d$). The VFET nomenclature is generally reserved for devices with saturated drain-source output curves, unlike the triode characteristics of the SIT. The SIT name itself refers to the fact that the output characteristics are modified by static induction and not just the input (gate) voltage as is the case for conventional FET's in the saturation mode. There are three basic conduction mechanisms possible when the SIT is on, known as the ohmic, exponential, and Space Charge Limited Current (SCLC) regions, which are identified in Fig. 2.4 for a typical RG-SB SIT in SiC with a channel and drift region doped at $5\times10^{15}\ cm^{-3}$. (One may increase the channel doping to increase the total maximum current.) The transistor conduction mechanisms are two-dimensional, and a short basic description of the various regimes is given. Current flow is modified by gate, drain, and source potentials, through saddle point minima between the gate electrodes, as shown in Fig. 2.5, where the minima is located at the mid-point of the channel.

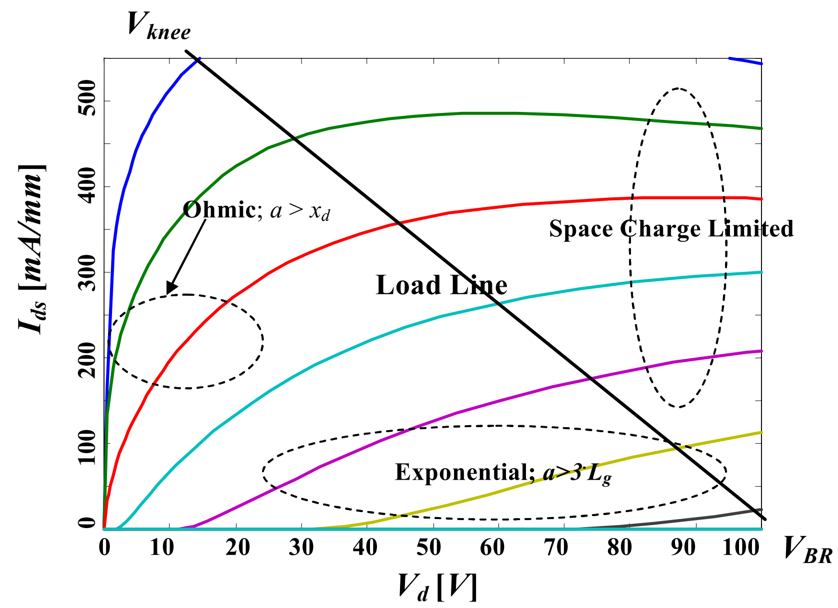


Figure 2.4 SIT's three regions of current flow.

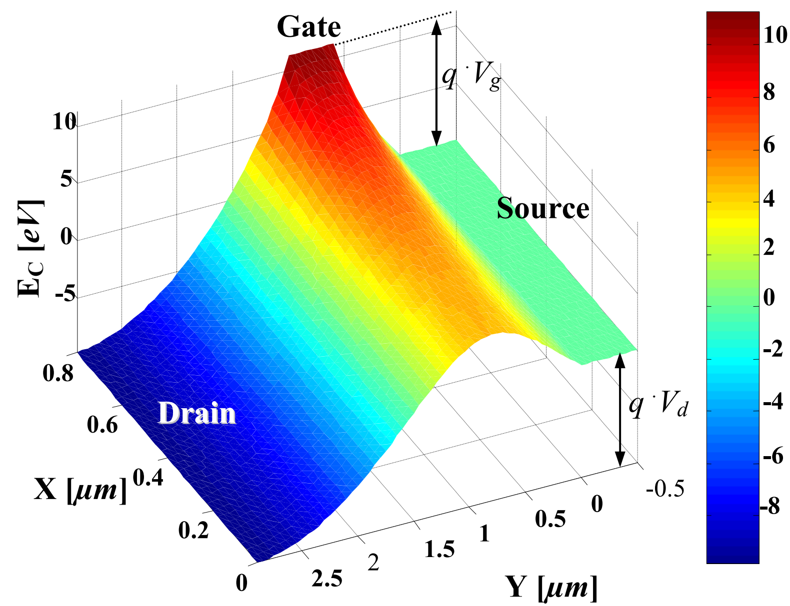
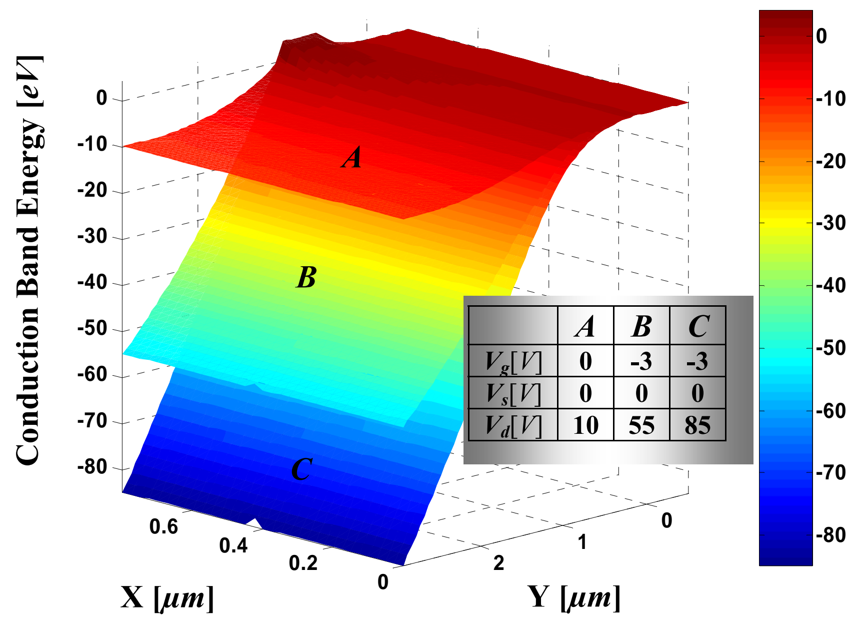


Figure 2.5 Conduction Band Energy of one half drift channel.



	A	B	C
$V_g[V]$	0	-3	-3
$V_s[V]$	0	0	0
$V_d[V]$	10	55	85

Figure 2.6 Conduction Band Energy in some bias.

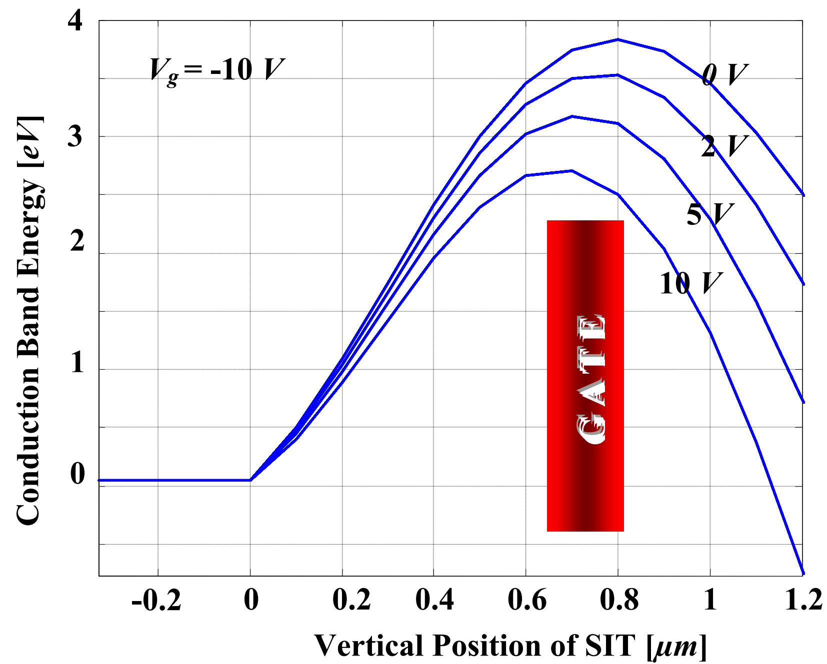


Figure 2.7 Conduction Band Energy in the center of channel (X=0) for different drain voltages.

2.1 Ohmic region

In the ohmic (linear) region, the channel is not completely pinched off by the depletion regions under fairly low gate and drain bias (see Fig. 2.5, Fig. 2.6, and Fig. 2.7). The current from drain-to-source (I_{ds}) is controlled by ohmic resistances found between the depletion regions under (beside) the gate, undepleted portions of the drift region, and the partially depleted portion of the channel immediately above the gate. The limiting portion is of course the region between gate depletion regions, which is often very narrow. Each channel is depleted from the gate on both sides by x_d which is given by *Eqn. (2.1),* where $\varepsilon_s = 10.0$ for SiC, $\varepsilon_0 = 8.854 \times 10^{-14}\ F/cm^2$, $q = 1.6 \times 10^{-19}\ C$ and N_D is the channel doping. V_{bi} and V_g represent the built-in potential and gate voltage, respectively.

$$x_d = \sqrt{\frac{2\varepsilon_s \varepsilon_0 (V_{bi} - V_g)}{qN_D}} \tag{2.1}$$

where: $V_{bi} = \phi_B - \frac{1}{q}[\frac{E_g}{2} - kT\ln(\frac{N_D}{n_i})]$.

The quantity ϕ_B is the Schottky barrier height (typically 1.1 eV for Ni on SiC) at the metal-SiC junction. The current density in this region can be given by $J_D = q\ .v_{nD}\ .N_D$, and the area is simply $A=2.A_{eff}\ .Z$ per finger. The quantities A_{eff} and Z are the undepleted channel width and channel depth, respectively. In this low-field region, the current is not limited by v_{sat}, but rather proportional to the effective open area, channel doping, and low-field electron velocity (v_{nD}). For this reason, the 4H polytype of SiC is the commercially-available preferred polytype because it has the highest electron mobility.

2.2 Exponential region

In the exponential region, even though the channel is depleted with a low gate bias, a high drain bias influences conduction over the potential barrier in the channel from drain to source. The potential barrier in the channel (as shown in Fig. 2.5 and 2.6 for half of a 1.2 μm channel thickness) between the two gate electrodes has barrier lowering in the mid-point region exponentially dependent upon the high drain bias. Since the exponential relationship exists, the current in this region can be described below in *Eqn. (2.2)* as exponentially dependent upon the amount of barrier lowering in the channel ($\Delta\Phi$), which is a function of the drain and gate bias [6].

$$I = I_0 e^{\frac{q\Delta\Phi}{kT}} \tag{2.2}$$

where, q is the electron charge, k is Boltzman's constant, T is the absolute temperature, and I_0 is a constant that depends on the channel geometry.

2.3 Space Charge Limited Conduction region

When the current density becomes high, a large drain voltage induces a large number of carriers into the gated and drift region. Also, when the carrier concentration becomes higher than the doping, the current becomes space charge limited. One can modify the treatment by Mott and Gurney [7, 8] and arrive at

$$J_D = 2\varepsilon_s \varepsilon_0 v_{SAT} \frac{V}{L^2} \tag{2.3}$$

where, V is the voltage drop from the contact (drain terminal) to the saddle point minima and L is the distance from the drain to the saddle point minima ($\approx L_{sg} + L_g + L_{gd}$). v_{sat} is the saturated electron drift velocity. *Eqn. (2.3)* can be expressed in terms of total current [2] as shown in *Eqn. (2.4).*

$$I_d = 2\varepsilon_s \varepsilon_0 v_{sat} \frac{V_d}{(L_{sg} + L_g + L_{gd})^2} A_{eff} \tag{2.4}$$

Note that total current for similar voltage and frequency rated Si and SiC devices will be quite different as L_{gd} would be an order of magnitude thinner and v_{sat} would be 1.5 to 2X higher in the case of SiC. However, in using these equations, there is an intrinsic assumption made regarding the SIT operation, which is explicitly that the electric field remains high enough ($\gg 1\times10^5$ V/cm in SiC) throughout the device, so that the electron velocity remains in saturation. While this is a simplifying assumption, which makes analysis easier, it can easily be violated, and can have significant impact on device operation (see discussion regarding temperature limits below for example).

3 Limitations for Design

3.1 Thermal Limit on Total Power

Most power devices have a heat sink that is usually attached to the backside of the wafer. The generated heat must be transferred to it. Assuming a 45° spreading angle, the associated thermal resistance can be computed by

$$R_{TH} = \frac{1}{\sigma_{TH} |W - Z|} \left| \ln \frac{\left(T_{sub} + W\right)Z\right)}{(T_{sub} + Z)W} \right| \tag{2.5}$$

where, W and Z are width and depth of device. and for a given power density per area $P^{''}$ we find the rise in device temperature ΔT for steady state conditions

$$\Delta T = R_{TH} P^{''} \tag{2.6}$$

The thermal resistance R_{TH} has a sizable spreading part that scales sublinearly with an increase of the device area, $A=W \cdot Z$. This means an increase in internal device temperature for larger area devices and a give temperature of the heat sink. Typically, the pitch between adjacent mesas, $t+2a$, affects the thermal resistance as well as the thermal power density generated on the top side of the wafer. A larger pitch makes it easier to dissipate the heat from the device. Additionally possibilities to improve the heat dissipation are a reduction of the generated thermal power by a high efficiency, and reducing the thermal resistance by thinning the substrate. However, a thinner substrate may in practice not improve the heat dissipation much because the thermal conductivity of the SiC substrate is comparable to the thermal conductivity of the metals that one would use for a heat sink attached to the backside of the wafer.

3.2 Impedance and Area Limit on Total Power

The output and input impedances can use in a microwave system have a lower limit that is fixed by circuit considerations and rarely be influence by the device designer. The impedance at the input and output of a device decreases with increasing device periphery, thus impedance imposes a limit on the total device size. The input impedance of a typical SIT is mainly capacitive. For example, the input capacitance with the output shorted is C_{in}^{S}, the input impedance with output connected to load is C_{in}^{L}, and the input inductance is L_{in}. For all cases of interest C_{in}^{L} is larger than C_{in}^{S} due to Miller effect [9]. In power microwave, the loaded input capacitance; C_{in}^{L} must be small enough so that the desired bandwidth can be achieved. The input impedance of the device is realized by synthesizing a transmission line such that the input

capacitance of each transistor stage is absorbed into the line impedance. This transmission line will have a cut-off frequency given by [10]

$$\omega_c = \frac{2}{\sqrt{C_{in}^L L_{in}}} \tag{2.7}$$

and, input impedance given by

$$Z_{in} = \sqrt{\frac{L_{in}}{C_{in}^L}} \tag{2.8}$$

Eqn. (2.7) and *Eqn. (2.8)* lead to the frequency limit for the amplifier given by [10]

$$f_c \langle \frac{1}{\pi Z_{in} C_{in}^L} \tag{2.9}$$

The load line is given in Fig. 2.4 between V_{BR} ($I_{ds} = 0$) to I_{max} ($V_{ds} = V_{knee}$), where V_{BR} is the static breakdown voltage between drain and source. I_{max} is the maximum total current in the ohmic region at $V_g = 0$ before conduction begins to be affected by SCLC and series resistance denoted at $V_{ds} = V_{knee}$. The very high V_{BR} of SiC SIT's (up to 450 V for S-band parts has been demonstrated) allows the theoretical power density (P_D) described in *Eqn. (2.10)* to be much higher than in Si. Since P_D is proportional to V_{BR}^2, and SiC's V_{BR} is nominally 10 times that of Si for similar-rated parts, this translates to a 100 times higher theoretical power density advantage for SiC SIT's over Si. Achieving those advantages will also require exceptional packaging technology to be implemented for SiC parts.

$$P_D = \frac{1}{8} I_{max} (V_{BR} - V_{knee}) = \frac{(V_{BR} - V_{knee})^2}{8 R_L} \tag{2.10}$$

Using SiC provides for another advantage in broadband amplifiers, which require minimum output impedance from the transistor. Since scaling the area up in a device

decreases both input and output impedance, the area of the device can be constrained by this requirement. SiC's ability to operate at higher voltages can increase the total output power while still maintaining some required output impedance.

4 Qualification of the simulation

Before using simulation software or tool to perform any serious simulation, the simulator must be tested to follow the basic physical principals. Basically, the simulator shall predict the thermal equilibrium condition and satisfy total current conservation. Only, after the simulator passes these tests, the simulation results for non equilibrium cases can be trusted in certain sense.

4.1 Thermal Equilibrium condition

It is well know that there is no current flowing inside the semiconductor device if the thermal equilibrium is imposed.

$$\vec{J}_{n,p} = -q\mu_{n,p} n, p \nabla \phi_{n,p} \equiv 0 \tag{2.11}$$

This lead to

$$\nabla \phi_{n,p} \equiv 0 \qquad \Rightarrow \qquad \phi_{n,p} = \text{constant}. \tag{2.12}$$

This means there is a single one Fermi level throughout the device. The choice of the constant is arbitrary. Mathematically the value of the Fermi level depends on the boundary conditions. The mathematical formulation of different boundary conditions must be self-consistent in this manner. Usually the constant is chosen to be equal to zero for sake of simplicity. Fig. 2.8 and Fig. 2.9 show the simulation results of electron and hole current densities inside the SIT. Except for a peak current in a small

region of the device, both electron and hole current densities are essentially zero everywhere inside the device. They are all in the order 10^{-8} [*A*].

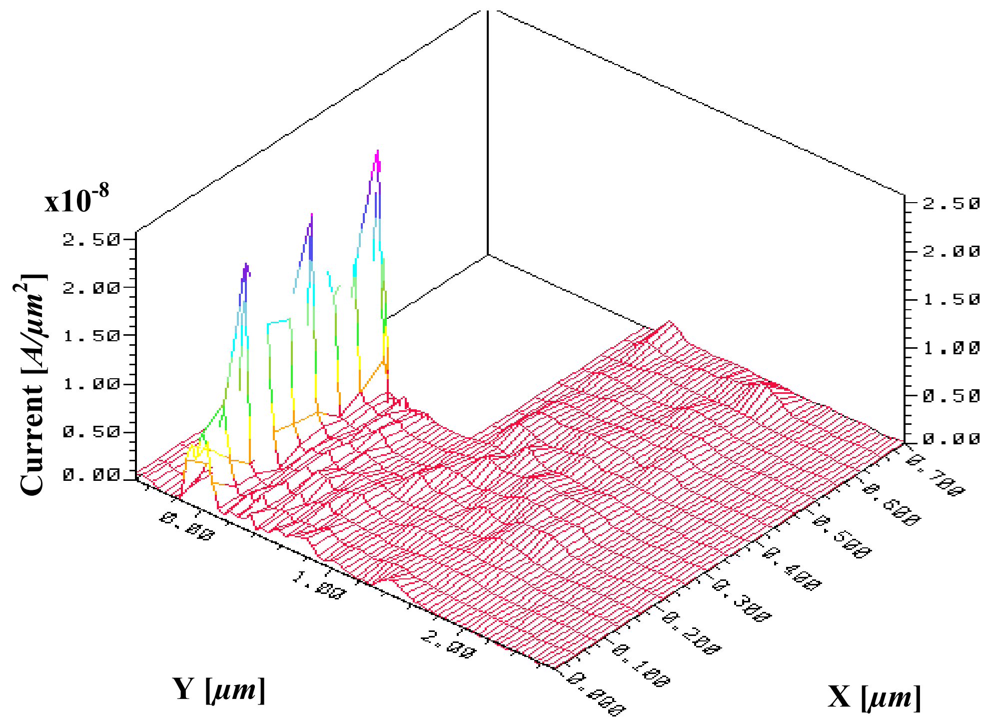


Fig. 2.8 Electron current densities inside the SIT

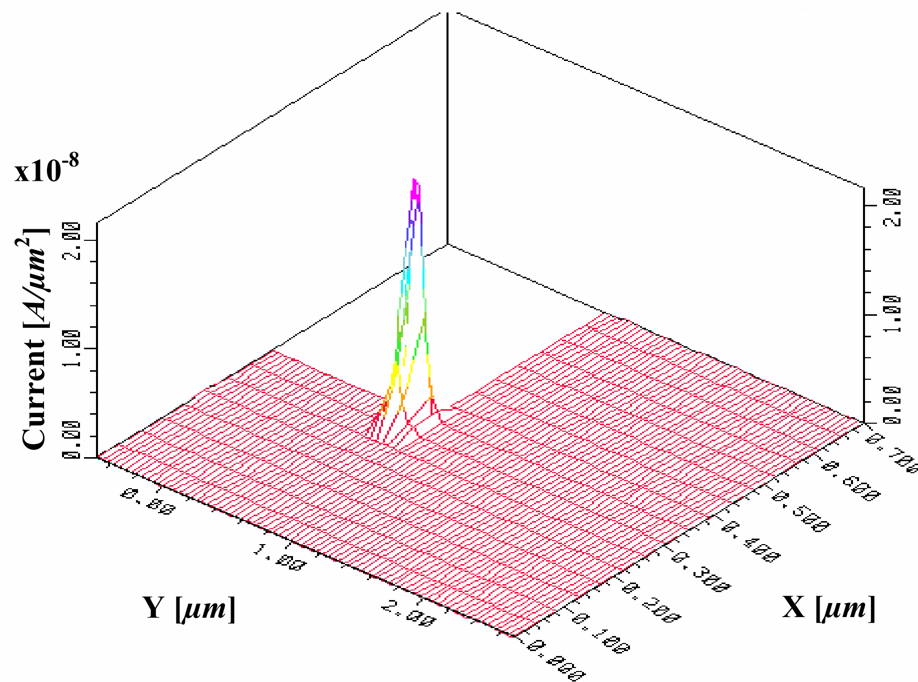


Fig. 2.9 current densities inside the SIT

The electron and hole quasi-Fermi potentials are shown in Fig. 2.10 and Fig. 2.11. The maximum amplitudes of electron and hole quasi-Fermi potential are all in the order of $10^{-12}[V]$. Considering the finite word length of computer, these can be essentially considered as zero. Hence the simulation results fulfill thermal equilibrium condition.

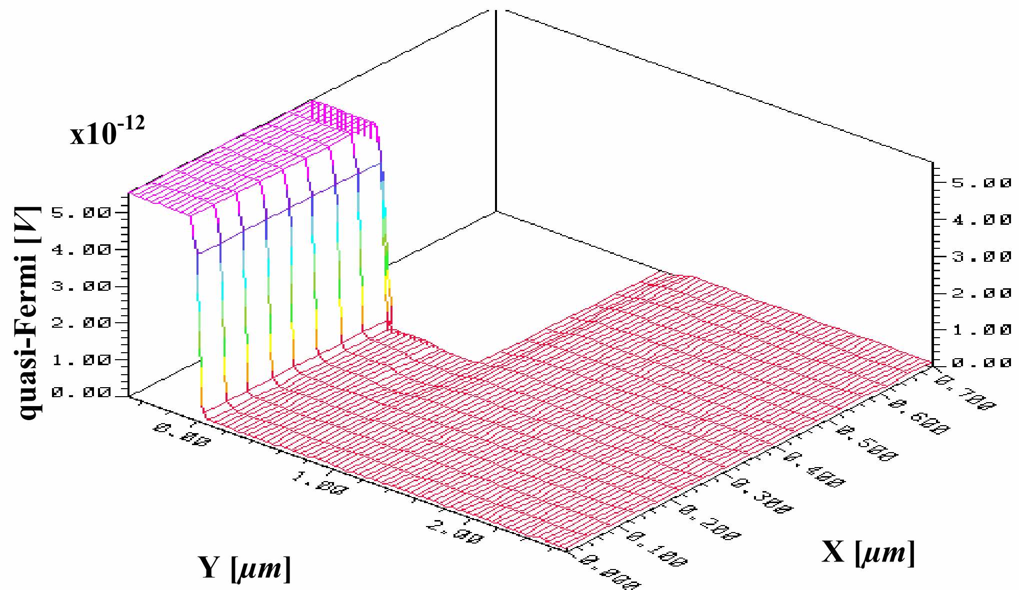


Fig 2.10 The simulation result of electron quasi-Fermi potential under thermal equilibrium.

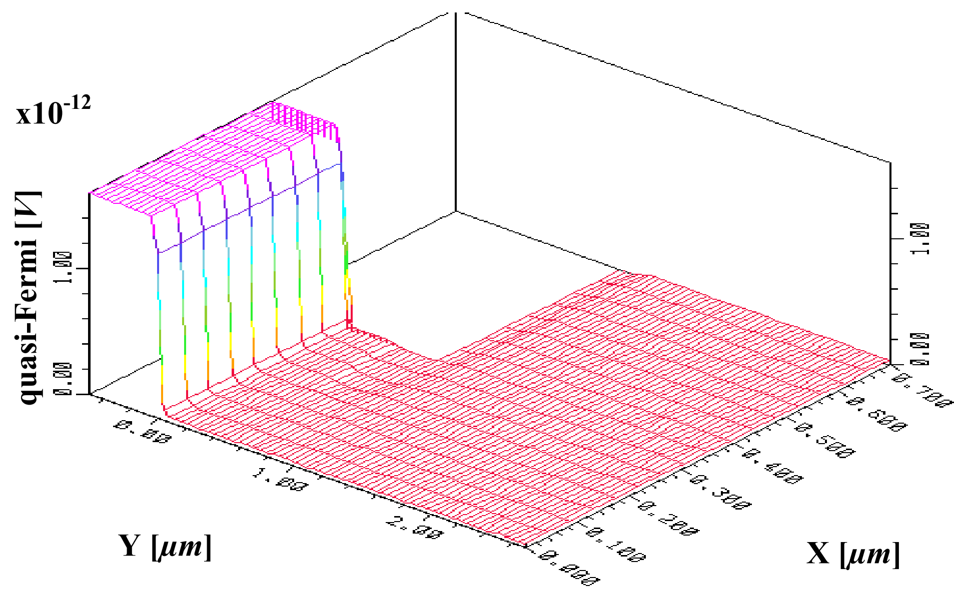


Fig 2.11 The simulation result of hole quasi-Fermi potential under thermal equilibrium.

4.2 Compare to measured data for parameter fitting.

In this chapter, we describe experimental results that were obtained from a device. Details of the fabrication can be found in [10, 11]. From the tests described in the previous section, it is evident that the simulation results are eligible to DC model steady state behaviors of semiconductor device. However, the simulated DC I-V curves are some different from the corresponding experimental results as shown in Figure 2.12 and Figure 2.13. The reason is that the material parameters used in the simulation are collected from literature. Since material parameter for SiC technology is still in its premature stage, these material parameters used in our simulator may not

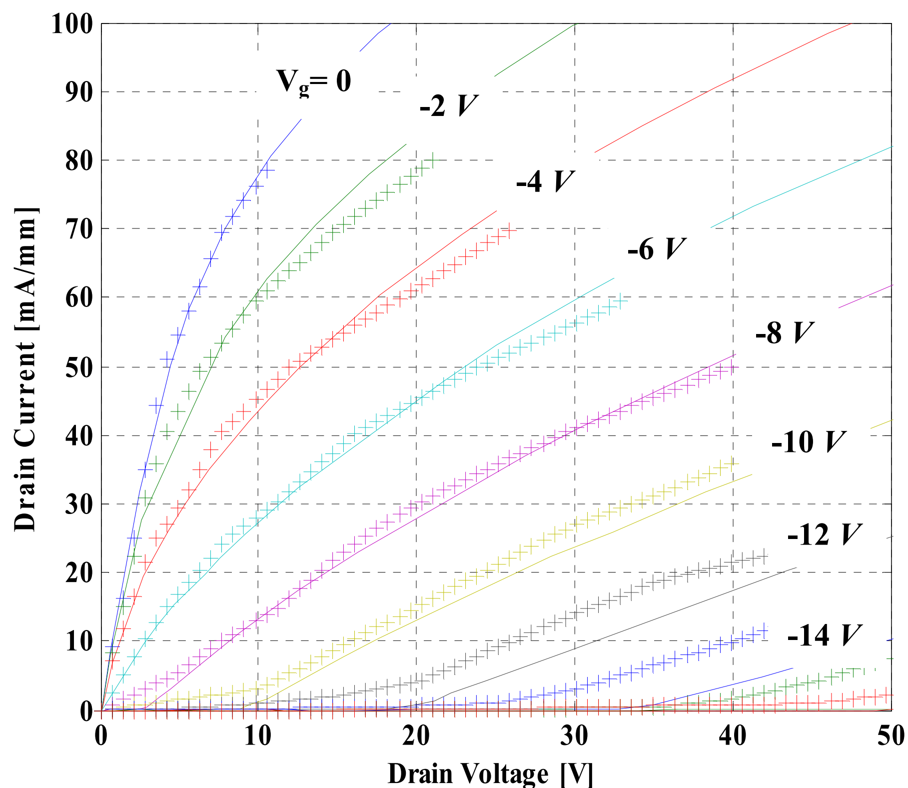


Fig 2.12 Output I-V curve for a 0~50 [*V*] drain voltage scales. The "+" symbols are measured data and the solid line are the results obtained from Medici Simulations.

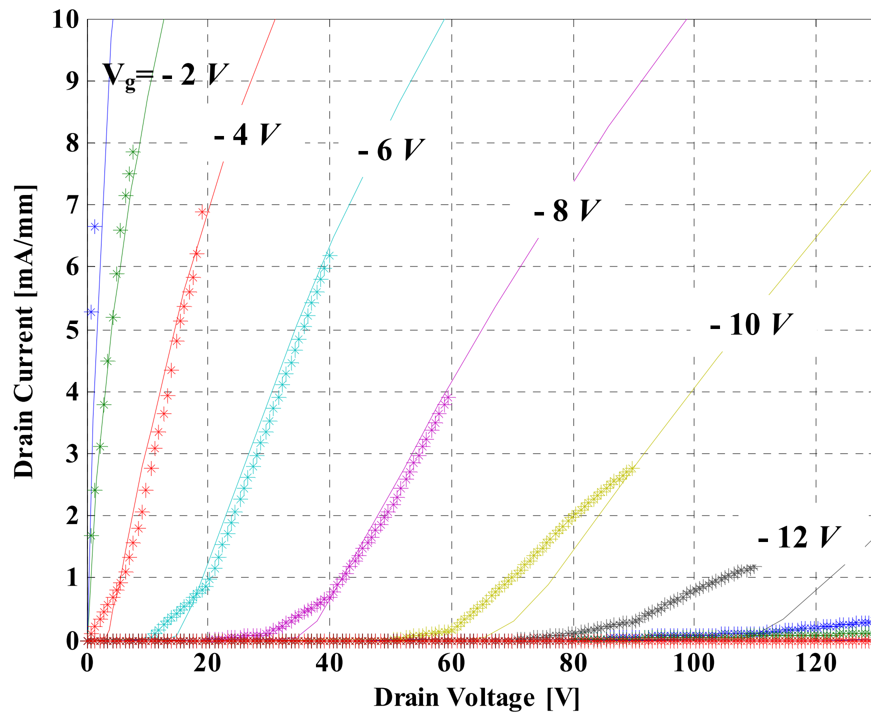


Fig 2.13 Output I-V curve for a 0~130 [*V*] drain voltage scales. The "+" symbols are measured data and the solid line are the results obtained from Medici Simulations.

correspond to the real data of the experimental device. These material parameters include low field mobility, high field mobility, saturation drift velocity for electron, and source resistance.

For the perfect fitting, the material parameters adjustment has to be repeated iteratively until the overall best fitting is reached. After all these fitting procedures, a good agreement is obtained in almost all regions of the available experimental data. In such a way, the material parameters may not correspond to the true values, but they can be quite close them. In this thesis, the material parameters in order to obtain good agreement with experimental data are changed to a saturation drift velocity of $2.2 \cdot 10^7$ [*cm/s*] [12], that is $2.0 \cdot 10^7$ [*cm/s*] in previously reported experimental values[2,10].

The drain resistance was accounted with the lumped 10 [Ω] resistance and a lumped source resistance was adjusted to obtain the best possible agreement with the measured data. The result was a value of 63 [Ω]. These detailed relationships are described in Figure 4.5, Figure 4.6, Figure 4.7, and Figure 4.8. The effects of mobility and saturation drift velocity were shown as Figure 4.14, Figure 4.15, Figure 4.16, Figure 4.17, and Figure 4.18 in the chapter 4.

The measured and simulated I-V curves are compared in Figure 2.11 and Figure 2.12. The agreement in the range of low voltages and high currents as shown in Figure 2.11 is quite good. The remaining deviation is probably due to not one particular material parameter factor but a consequence of the uncertainty of all material and device parameters involved. In the I_{MAX}, as shown in figure 2.12, the device behavior is particularly sensitive to changes in the channel geometry, but overall agreement between measured and simulated result is still acceptable. A better overall fitting could probably be enforced by adjusting some of the simulation parameters when the output I-V curve would be available for all drain currents. Unfortunately, most of measured data was limited to taking the I-V data for reasonably low static power levels in order to avoid destruction of the device during testing.

Reference

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CHAPTER III

STATIC CHARATERISTICS

1 Device Physics

The static I-V characteristics of the basic SIT were computed with the three partial differential equations (*Eqn. (3-1), (3-2)*, and *(3-3)*) self-consistently for the electrostatic potential ψ and for the electron concentrations n, respectively. In the SIT, the electrical behavior is governed by Poisson's equation.

$$\nabla^2\psi = -\frac{q}{\varepsilon}(-n + N_D^+) \tag{3-1}$$

and Continuity equation for electrons.

$$\nabla \cdot \vec{J} = U_n \tag{3-2}$$

where ψ, ε, and n are the electrostatic potential, dielectric constant, and electron density, respectively. N_D^+, $\vec{J}$, U_n are the concentration of ionized donors, current density, and net rate of electron recombination. Since the SIT is a majority carrier device and SiC is large bandgap material, the effect of holes has been omitted in this analysis. The hole concentration will be smaller than the numerical limit of the simulation tools. Carrier transport is given by the drift diffusion equation

$$\vec{J} = q\mu_n\vec{E}_n n + qD_n\vec{\nabla}n \tag{3-3}$$

where, μ_n, $\vec{E}_n$, and D_n are the electron mobility, the electric field, and electron diffusivities, respectively.

2 Voltage Gain and Maximum Current Physics

The voltage gain μ is a measure for the possible large signal gain. It changes considerably with drain voltage, but for the scope of this work μ is defined for a drain voltage of 100V. For practical devices the voltage gain should be at around 10, which would correspond to a device that required -10V on the gate terminal to keep the device off at 100V on the drain. A graphical interpretation of these parameters is shown Fig. 3.1.

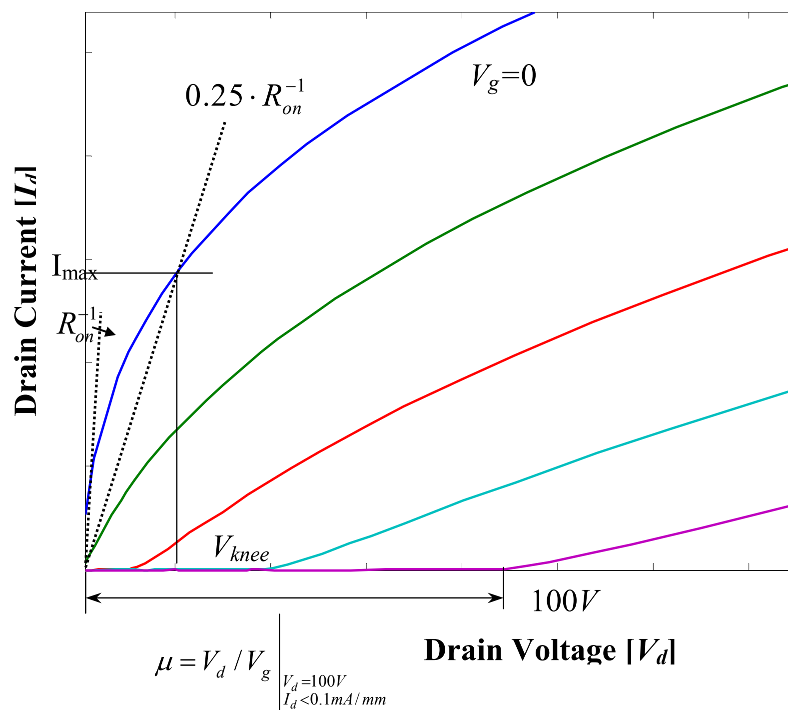

Figure 3.1 On resistance, voltage gain, maximum current and knee voltage.

The zero bias on-resistance, R_{on}, is simply the initial slope of the drain current versus drain voltage curve for zero gate voltage

$$R_{on} = \left(\frac{\partial V_d}{\partial I_d} \right) \Bigg|_{V_d=0,\ V_g=0} \tag{3-4}$$

In *Eqn.* (3-4), a small R_{on} is desirable for higher total current and smaller knee voltage. The definition illustrated in Fig. 3.1 places the point of maximum current where the straight line through the origin given by $I_{\max} = \frac{V_d}{4R_{on}}$ intersects with the drain current curve for V_g=0. Since the SIT shows non-saturating I-V curves, I_{max} is not as obvious as for a MESFET type device. Also, it should be mention that V_g can be up to +2.5V in wide bandgap(3.2 eV) SiC pn-gate SIT's without getting forward bias injection from the gate. But higher I_{max} will allow for a higher power density per unit width for a given breakdown voltage. The knee voltage V_{knee} is the drain voltage that corresponds to the point of maximum current. The knee voltage is important because it is the main factor that degrades the drain efficiency, which is given by [1]

$$\eta_D = \frac{P_{out}}{P_{DC}} = \frac{0.5}{1 + 2(\frac{V_{knee}}{I_{\max} R_L})} \tag{3-6}$$

where P_{DC} is the DC power dissipated in the device, P_{out} is AC output power which is given by $P_{out} = \frac{R_L V_{\max}^2}{8(R_{on} + R_L)^2}$, and R_L is a load impedance.

3 Basic Dimension parameters for SIT Design

We have seen the SIT in Fig. 2.1 and Fig. 2.2, it is defined by four geometry parameters (*2a*, L_g, L_{sg}, and L_{gd}) and one doping parameter (N_D). Theoretically, the source gate distance L_{sg} should be as small as possible to minimize the source resistance. However L_{sg} is limited by the requirement that a low leakage path with sufficient breakdown voltage must exist between the gate and source. A nominal distance of L_{sg}=0.5 μm works well and this value was also adopted for all simulations.

As a side note we mention that the voltage gain improves when L_{sg} increases for fixed L_g, because for increasing drain bias the saddle point tends to move toward and eventually reach the source, as was shown in Fig. 2.7. An increased L_{sg} allows the saddle point to move further behind the gate and increase the screening of the drain induced field by the gate, thereby increasing the blocking gain. The trench width (t) was fixed at one half of mesa width ($2a$), and except for a small change in spreading resistance of the drain drift region, it had relatively little effect on the static characteristic.

One of the most significant parameters for design is the doping value, N_D. In these simulations, we used four different values, $5 \cdot 10^{15}\ cm^{-3}$, $1 \cdot 10^{16}\ cm^{-3}$, $5 \cdot 10^{16}\ cm^{-3}$, and $2 \cdot 10^{17}\ cm^{-3}$, spanning a range of nearly two orders of magnitude. Two lower doping values correspond to devices used by Northrop Grumman for their pioneering work [2] whereas the two higher doping values were used by Purdue University [3]. The gate-drain length (L_{gd}) needs to be tailored to each doping, and is determined by the two conflicting requirements of low drain resistance and a large breakdown voltage. In lower doping levels, the gate-drain length (L_{gd}) is limited by the requirements for a low drain resistance, due to the low doping and resulting in high bulk resistivity. On the other hand, in high doping, the bulk resistivity is low enough that the gate-drain distance can be chosen to be comparable to the punch-through depletion depth for maximum drain voltage. We investigate the effect of varying two design parameters, gate length (L_g) and mesa width ($2a$) on the static I-V curve by keeping all other parameter constant. The computed static I-V curve for SIT with a doping value of $N_D = 5 \cdot 10^{16}\ cm^{-3}$ are shown in Fig. 3.2 for five different gate lengths (0.05, 0.1, 0.2, 0.3, and 0.5 μm) and five different mesa width (0.4, 0.5, 0.6, 0.7, and 0.8 μm). Other plots

for different doping values can be found in appendix B. For the case of a large mesa width and very short gate, as shown in the lower left hand corner in Fig. 3.2, it is difficult to pinch off the drain current at high gate voltages, which corresponds to a low voltage gain μ. The other extreme cases of a long gate length and a narrow mesa width, which the device characteristic is in the upper right hand corner on the Fig. 3.2. This device is pinched off for all drain voltage with a relatively small gate voltage at the expense of having only a very small maximum current I_{max}. Maximum current for above gate lengths and mesa widths is shown in Fig 3.3. For the case of a large mesa width and very short gate, as shown in the lower left hand corner in Fig. 3.3, maximum current is maximum and the other case of a long gate length and a narrow mesa width, which is the device characteristic in the upper right hand corner in Fig. 3.3, maximum current is minimum. For example, we will design highest current SIT with blocking gain 10 [dB] in doping value of $N_D = 5 \cdot 10^{16}\ cm^{-3}$, mesa width is 0.7 μm and gate length is 0.5 μm from simulation results on the Fig 3.3.

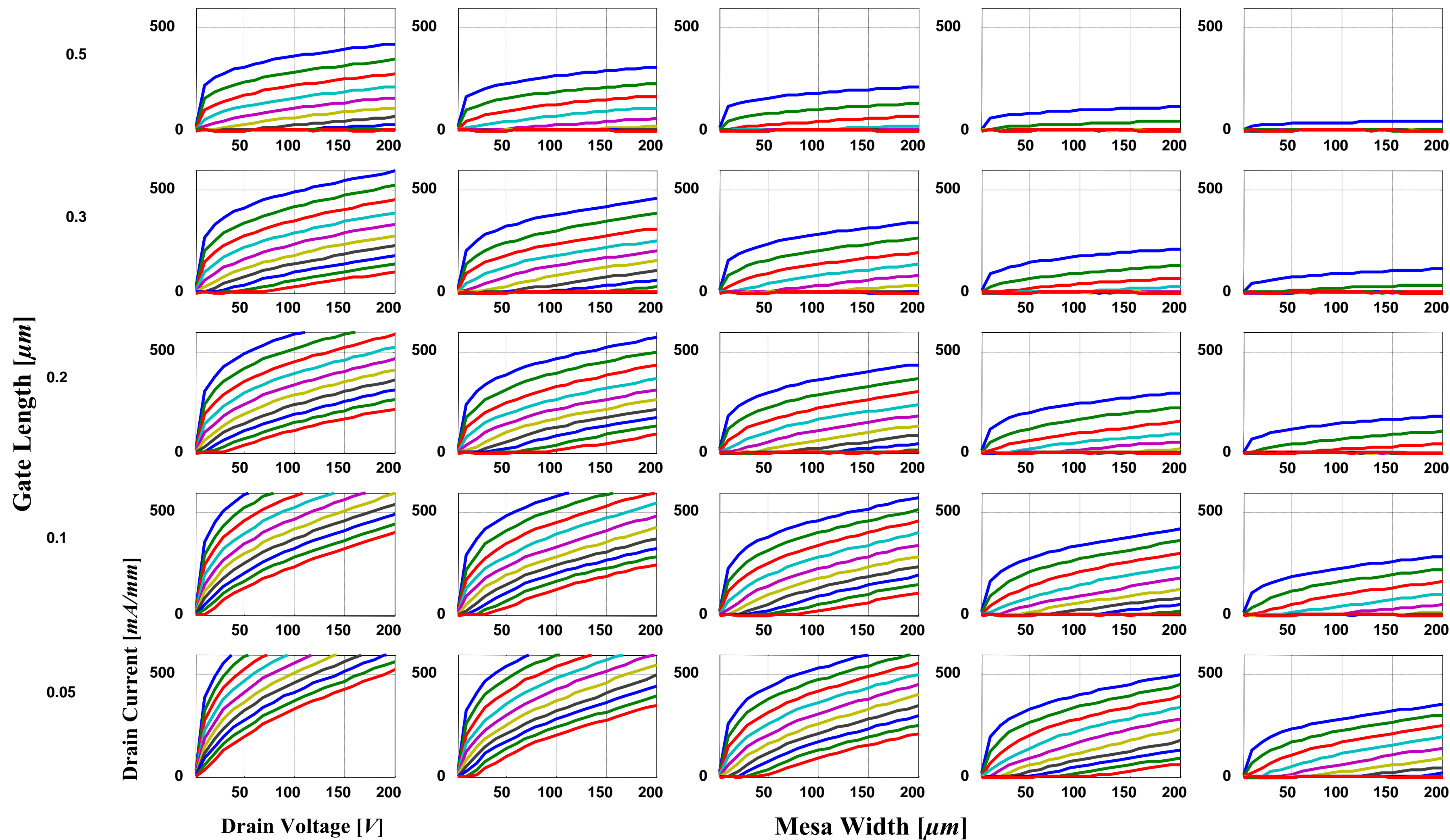

Figure 3.2. I-V curves for various gate length and mesa widths with $N_D = 5 \cdot 10^{16}\ cm^{-3}$, L_{sg}=0.5 μm and t=2a. Curve start at a gate voltage Vg=0 and progress in -2V steps.

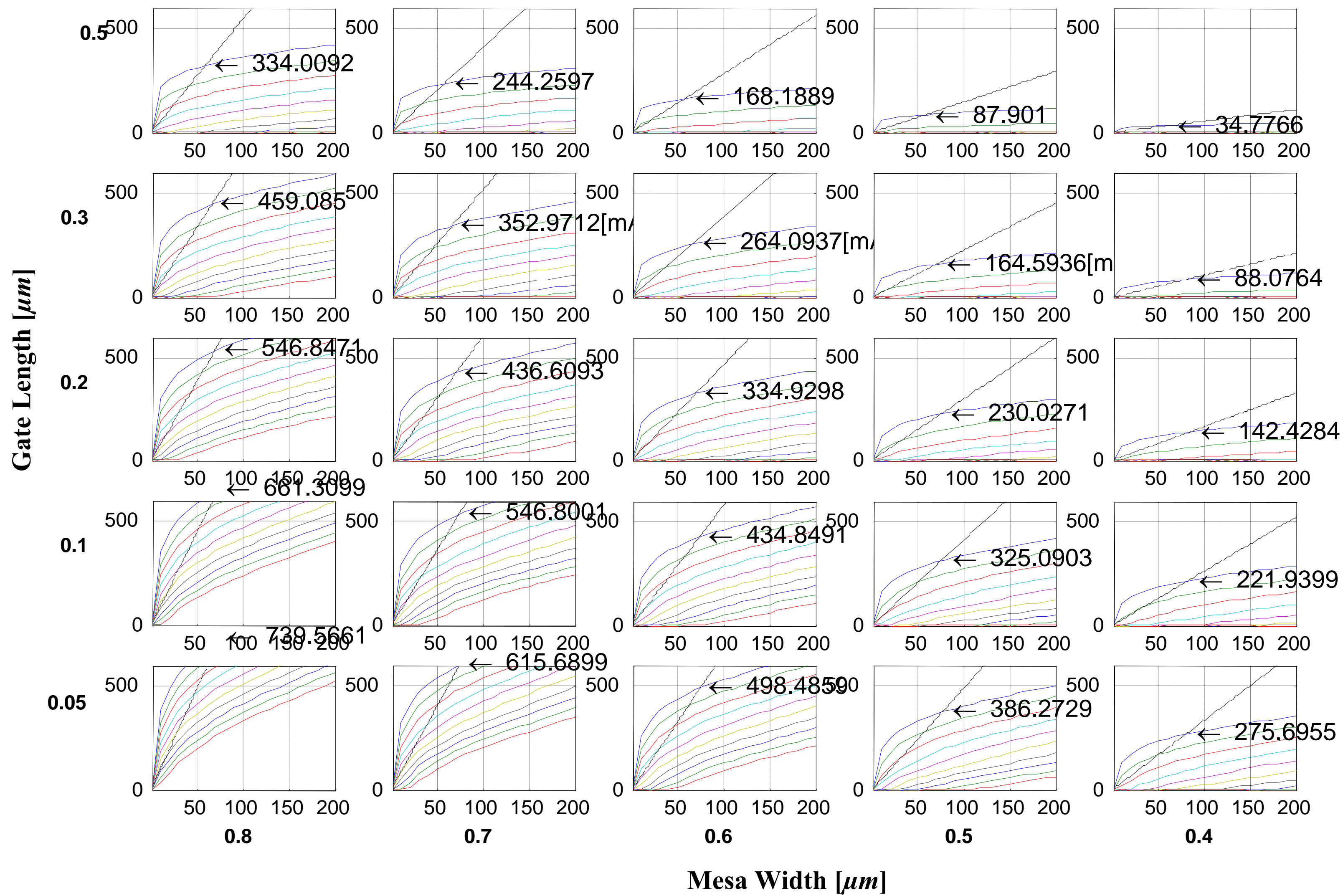

Figure 3.3 Maximum Current for various gate lengths and mesa widths on the IV curves.

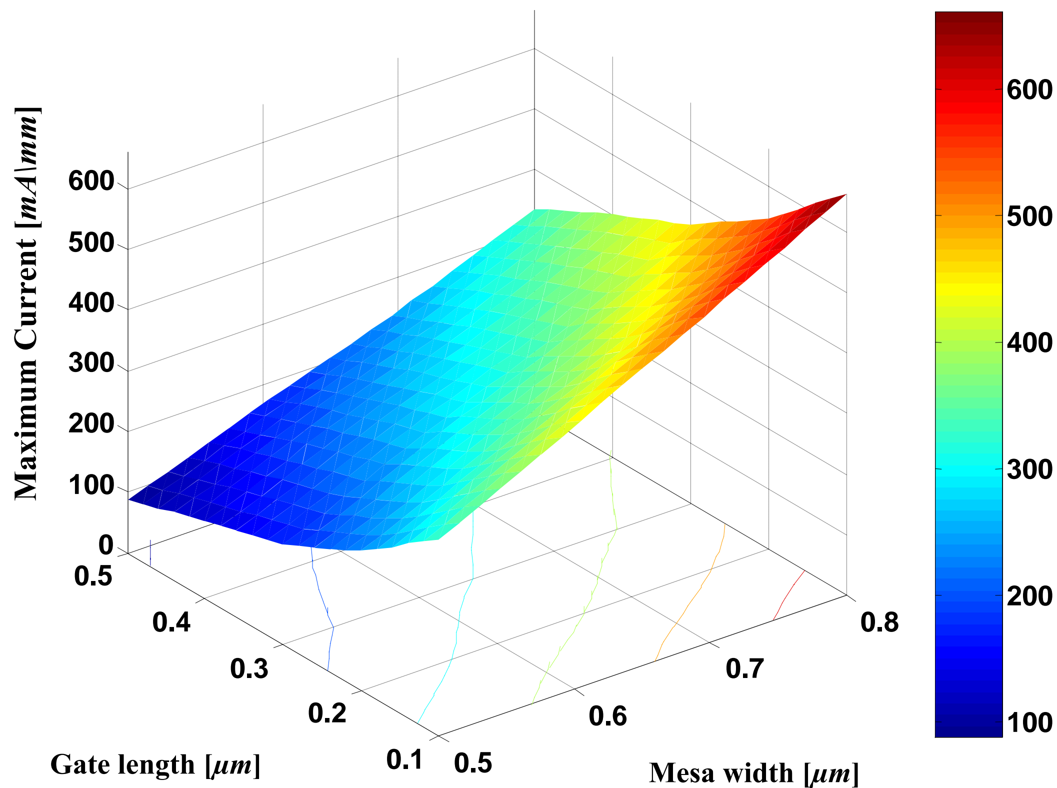

Figure 3.4 Maximum Current for various gate lengths and mesa widths.

Fig. 3.4 is shows maximum current, I_{max} depends on the gate length, L_g, along with mesa width *2a* as a parameter. In Fig. 3.4, the effect of an increased L_g is a reduction in I_{max} as a result of the increased channel resistance. The part of the channel between the gates that is partially depleted and which forms the bottleneck for current flow simply becomes longer. The increase of the channel resistance follows nearly linearly with L_g, and we can see an inverse proportional effect on the maximum current. On the other hand, maximum current is proportional to mesa width and it increases with mesa width in a nearly linear fashion, because the bottleneck between gate electrodes becomes wider. The blocking gain, μ, is a stronger function of mesa width and gate length than the maximum current, unless the mesa width becomes very

wide, as shown Fig. 3.5. The physical reason is that the current changes linearly with channel dimension whereas the blocking gain to first order depends exponentially on the channel dimensions [5], because of high voltages and low currents, the current is exponentially related to the saddle point potential. As a result, when the ratio between gate length and mesa width is increased, the blocking gain increases and the maximum current decreases.

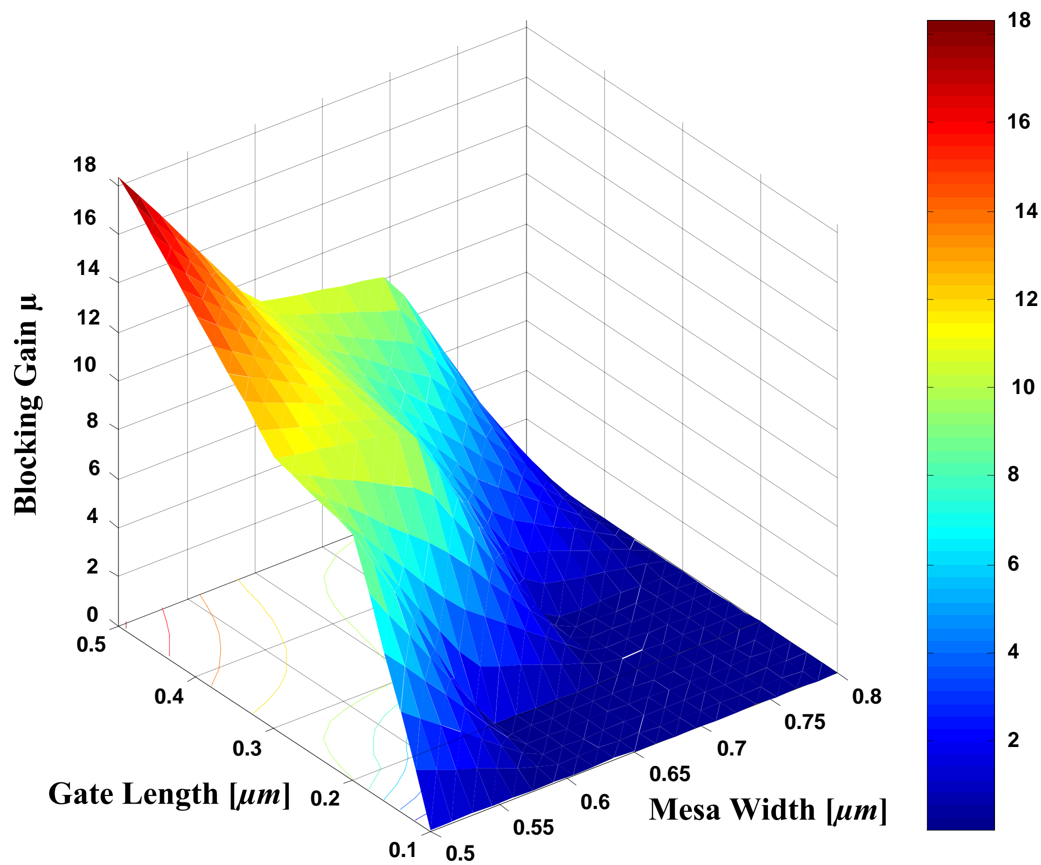

Figure 3.5 Blocking gain as a function of gate lengths and mesa widths.

4 Drain and Source Resistance

The parasitic resistances in the SIT are the resistance of the source (R_S), Drain (R_D) and the bulk resistance of the substrate (R_{sub}). The substrate resistance can only be meaningfully defined for a complete device, and by assuming current spreading angle of 45 degrees can be computed by [12]

$$R_{sub} = \rho_{sub} \frac{1}{|W-Z|} \left| \ln \frac{(T_{sub}+W)Z}{(T_{sub}+Z)W} \right| \tag{3.7}$$

which is similar to the equation for the thermal resistance (see *Eqn.* (2.5)), expect that now the resistivity of the substrate, ρ_{sub}, appears. The resistance of the drain and source contact for a complete device can be estimated by

$$R_D = \frac{\rho_D}{(W+2\cdot T_{sub})(Z+2\cdot T_{sub})} \tag{3.8}$$

$$R_S = \frac{\rho_S}{2a\cdot W\cdot N_m} \tag{3.9}$$

Typical values are T_{sub} =300 μm, ρ_{sub}=15 $m\Omega\cdot cm$, and $\rho_{D,S}$=$1\cdot 10^{-5}$ $\Omega\cdot cm^2$. when we assume a small area test device with 1*mm* periphery with 20 fingers, Z=40 μm and W=50 μm, the substrate contribution would be R_{sub}=2.9 $\Omega\cdot mm$ by *Eqn.* (3.7), nearly order of magnitude smaller than the large area limit. Similarly, we find R_D=0.5 $\Omega\cdot mm$ and R_S=0.024 $\Omega\cdot mm$ for the large area and small area device respectively. From this follows immediately that the resistance due to the drain contact can be neglected; this would still be true for even a poor contact of ρ=$1\cdot 10^{-4}$ $\Omega\cdot cm^2$. The source resistance depends on the particular design because the area of the contact is determined by the mesa width.

5. Basic considerations of Power and frequency performance

In previous definition (Fig. 3.1) of maximum current I_{max}, a large maximum current can be obtained for larger channel dimensions. We can show in Fig. 3.6 the effect of varying gate length on the frequency performance. it should be understood that f_T is a function of zero bias. The use of smaller dimension allows for higher frequency performance but comes at the expense of a slightly lower maximum current. Therefore, to maximize frequency performance, a short gate length should be selected.

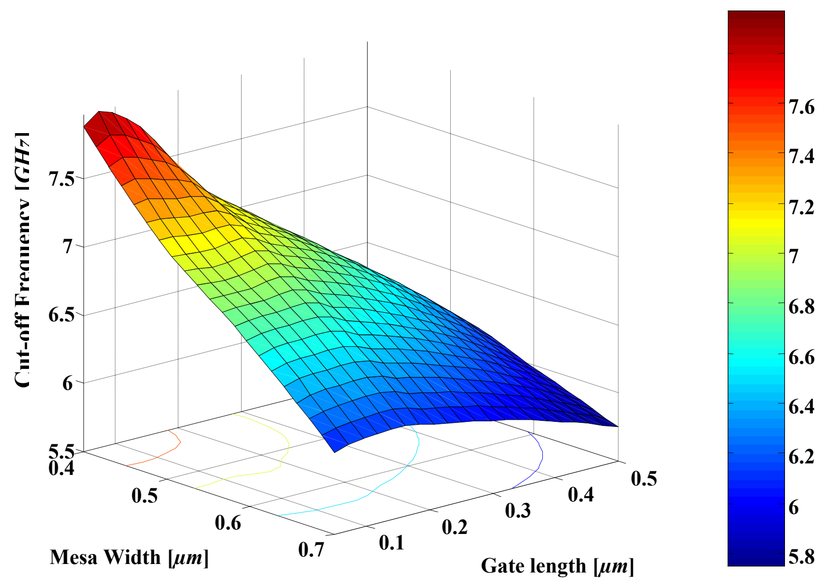

Figure 3.6 Cut-off Frequency as function of gate lengths and mesa widths for fixed voltage gain 10 dB

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CHAPTER IV

HIGH FREQUENCY CHARATERISTICS

1. Small Signal Equivalent Circuit of SIT

The SIT is usually used as a small signal amplifier. Small signal analysis is as important as DC analysis for semiconductor device, especially for high frequency operation of the SIT. There are three types of techniques for small signal analysis of a semiconductor device [1]. The first technique is transient excitation followed by Fourier decomposition, second one is incremental charge partitioning, and the third one is small-signal AC steady state frequency domain analysis. The small-signal AC steady state frequency domain analysis is superior approach compared to the other methods [1]. This technique is easy to be incorporated into a device simulator. In this chapter, the small-signal AC steady state frequency domain analysis technique is applied on the frequency performance of the SIT.

For an assessment of the frequency performance of the SIT, the small signals Y-parameters have been computed by MEDICI over the anticipated operation frequency range from 500 *MHz* to 10 *GHz*. The Y-parameters as a function of frequency, as obtained from MEDICI simulation, were fit to the pi-equivalent circuit shown on Fig. 4.1. The gate-drain capacitance is occasionally referred to as the feedback capacitance because it couples the output and input of the device. The model the frequency behavior of the input impedance the gate-source resistance R_{gs} is connected in series with C_{gs}. The gate-source resistance represents the resistance of the undepleted part of

the mesa on the source side of the gate. The magnitude of the transconductance, g_m, is equal to the DC transconductance. The transit time, τ, accounts for the delay due to the finite time that a carrier needs to travel from the source to the drain. The output conductance is denoted by g_{ds}. The procedure of finding the equivalent circuit elements from the simulated data is identical to determining these elements from a measured data set, with the exception that measured data are obscured by unwanted effects such as noise, imperfect calibration and unaccounted parasitics because the exact details of a physical structure are only known within certain limits, whereas the simulated structure is known precisely. At a circuit level, input current I_i is equal to the magnitude of ideal output current $g_m \cdot V_{gs}$ of the intrinsic transistor. When the output is short-circuit [2],

$$I_i = jw(C_{gs} + C_{gd})V_{gs} \tag{4-1}$$

if we let C_g=C_{gs}+C_{gd}, then at the cutoff frequency

$$|I_i| = 2\pi f_T C_g V_{gs} = g_m V_{gs} \tag{4-2}$$

in Egn.(4-2),

$$f_T = \frac{g_m}{2\pi C_g} \tag{4-3}$$

or,

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{4-4}$$

The four elements of the general pi-circuit, Y_i, Y_o, Y_r, and Y_f, can be obtained easily from the Y-parameters [3] that one has available either from simulations or from measured S-parameters that were transformed to Y-parameters (see App. D).

$$Y_i = Y_{11} - Y_{12} \tag{4-5}$$

$$Y_o = Y_{22} - Y_{12} \tag{4-6}$$

$$Y_r = -Y_{12} \tag{4-7}$$

$$Y_f = Y_{21} - Y_{12} \tag{4-8}$$

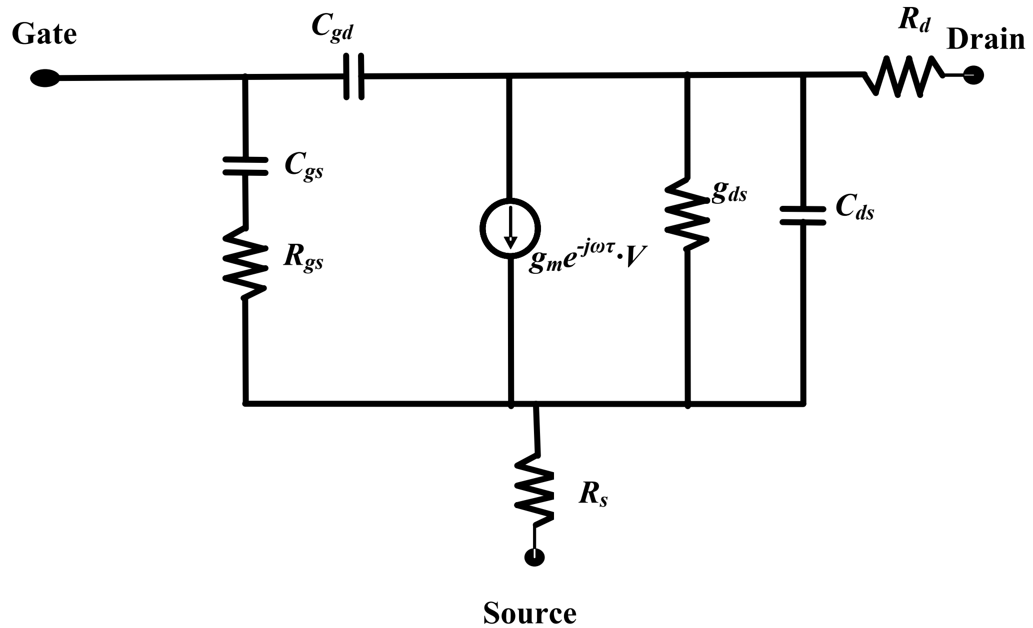


Figure 4.1 Pi-equivalent circuit for small signal modeling.

From these the reactive components of the intrinsic device may be determined. MEDICI will be able to create the Y-parameters directly from the small signal simulation. Using circuit model for the SIT, the value of the components can be determined by the simulations. Applying the small signal simulations to the circuit models, from Egn. (4-5) through (4-8) the Y-parameters are related by [3]:

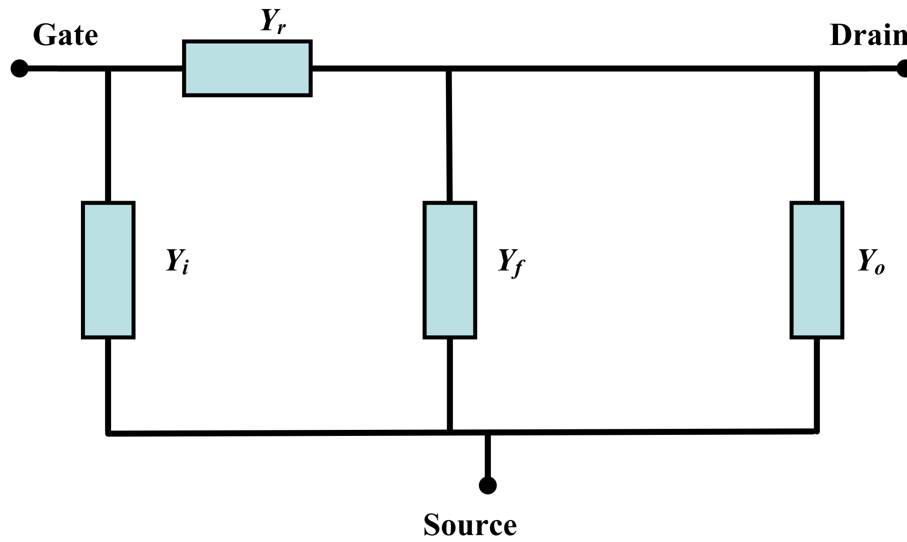


Figure 4.2 General Hybrid-Pi equivalent circuit.

$$Y_{11} = j\omega(C_{gs} + C_{gd}) \tag{4-9}$$

$$Y_{12} = -j\omega \cdot C_{gd} \tag{4-10}$$

$$Y_{21} = g_m \cdot e^{-jw\tau} - j\omega C_{gd} \tag{4-11}$$

$$Y_{22} = g_{ds} + j\omega(C_{ds} + C_{gd}) \tag{4-12}$$

The Y-parameters used for the following discussion are for a bias point with V_d = 10 V and V_g = 0. Plotting the magnitude of Y_f as a function of frequency, as show on Fig. 4.4, we can obtain values for g_m and τ. By *Eqn*. (4-8), (4-10), and (4-11) the magnitude of Y_f plot shows that $|Y_f|$ is almost independent of frequency, and we obtain g_m by forming the average over the lower frequency part of the plot. The phase plot linearly decreases over frequency, and τ can be obtained from the slope of the line by fitting the plot using the equation ΔY_f = 2πfτ. Also, in Fig. 4.4 shown the magnitude of Y_o that Gate-Drain and Gate-Source Capacitance from which we obtain a

value for g_{ds}. The feedback capacitance C_{gd} is obtained by averaging the data of a plot of $\Im(-Y_{12}/\omega)$ over frequency by Eqn. (4-10), which should be independent of frequency. Here $\Im(-Y_{12}/\omega)$ means that the imaginary part of $-Y_{12}/\omega$. Similarly, C_{gs} is found by averaging $\Im((Y_{11}+Y_{12})/\omega)$ over frequency by Eqn. (4-9), (4-10), as shown Fig. 4.3.

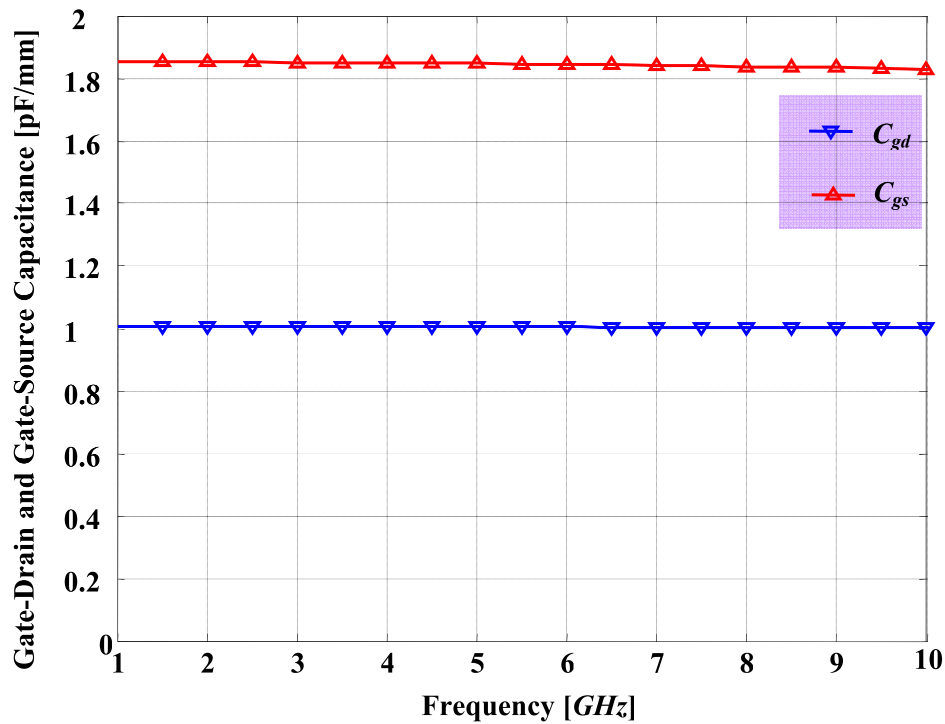


Figure 4.3 Magnitude of Y_f and Y_o as function of frequency at bias point V_d = 10V, V_g = 0V.

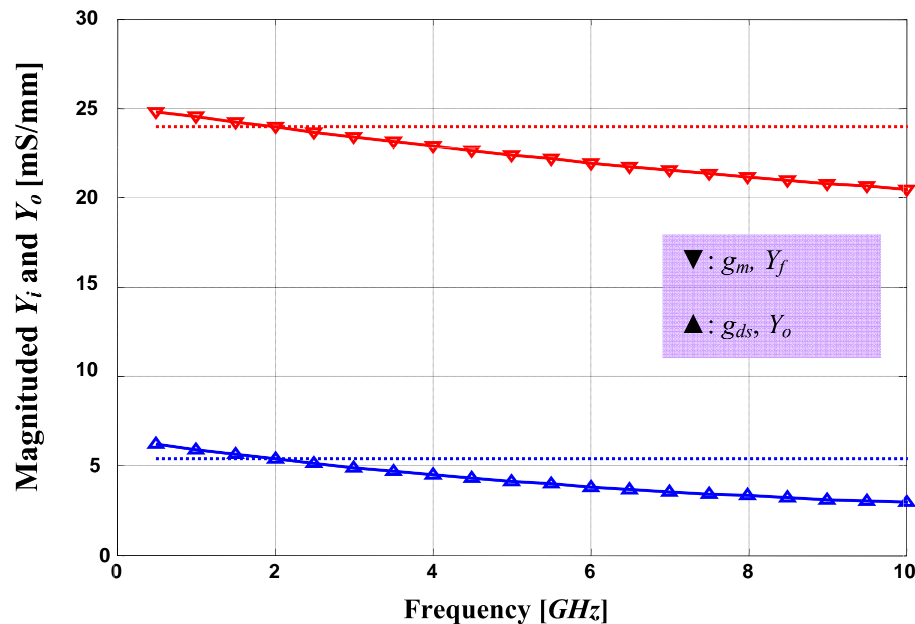


Figure 4.4 Gate-Drain and Gate-Source Capacitance as function of frequency at bias point $V_d = 10V$, $V_g = 0V$.

If one tried to find a value for C_{ds} by simulation from MEDICI, the resulting values seem to randomly jump between positive and negative numbers with an absolute value that is at least an order of magnitude smaller than either of the values found for C_{gs} or C_{gd}. Therefore, let $C_{ds} = 0$. This is physically meaningful if one considers the vertical arrangement of the device that essentially places the gate electrode as a grid between the drain and source electrode, electrostatically shielding the two from each other. This also agrees with the usual interpretation of the drain source capacitance in lateral devices, such as MESFET, where it is due to fringing effects between the source and drain electrode through the substrate under the active device [4]. There is no equivalent to the substrate fringing effect in a SIT due to the vertical channel, which is similar to two MESFET channel in a mirror-image like arrangement.

2. Effect of contact Resistance

The contact resistivity of the source, R_s, and drain contact, R_d, can be described by lumped resistances that are in series with the source and drain terminal, respectively. A finite source resistance R_s affects the transconductance as well as the short circuit input capacitance. For the special case that $R_d = 0$ we find for the transconductance [5]

$$g_{m,ext} \approx \frac{g_m}{1+g_m R_s} \qquad \text{when} \quad R_d = 0, \qquad (4\text{-}13)$$

and for the short circuit input capacitance

$$C_{in} \approx C_{gs}\frac{1}{1+g_m R_s} + C_{gd} \qquad \text{when} \quad R_d = 0, \qquad (4\text{-}14)$$

The drain resistance, R_d acts like a built in load resistance and therefore increase the input capacitance according to the Miller effect. When we assume the any special case that $R_s = 0$, the Miller effect can be theoretically expressed by the following approximation [5]

$$C_{in} \approx C_{gs} + C_{gd}(1+\frac{g_m}{g_{ds}+1/R_d}) \text{ assumed } R_s = 0 \qquad (4\text{-}15)$$

In the general case, when both R_s and R_d are unequal to zero, the expression for the input capacitance becomes more complicated. However, we conclude that an increase in R_d and R_s leads to an overall degradation in frequency performance, namely the cut-off frequency, because the contribution of C_{gd} is significant for the SIT and tends not to decrease when a source resistance is introduced, *Eqn*. (4-14). Note that for a device with a very small feedback capacitance, the cut-off frequency does not change notably with increasing source resistance. Such as MESFET, HEMT, where the overall contribution of C_{gd} to the total input capacitance is typically less than 10% [6]. The source resistance also increases the total resistance of the device between source and

drain, therefore the maximum current is reduced. Fig 4.5 shown Cut-off frequency as a function of gate length and mesa width with drain contact resistivity $1{\cdot}10^{-5}$ [Ω cm^2]. As source contact resistivity increase from $0.5{\cdot}10^{-5}$ to $5{\cdot}10^{-4}$ [Ω cm^2], cut-off frequency decrease. Cut-off frequency is limited by transconductance, gate-drain capacitance, and gate-source capacitance in *Eqn* (4-4). Therefore, we need to investigate these three factors.

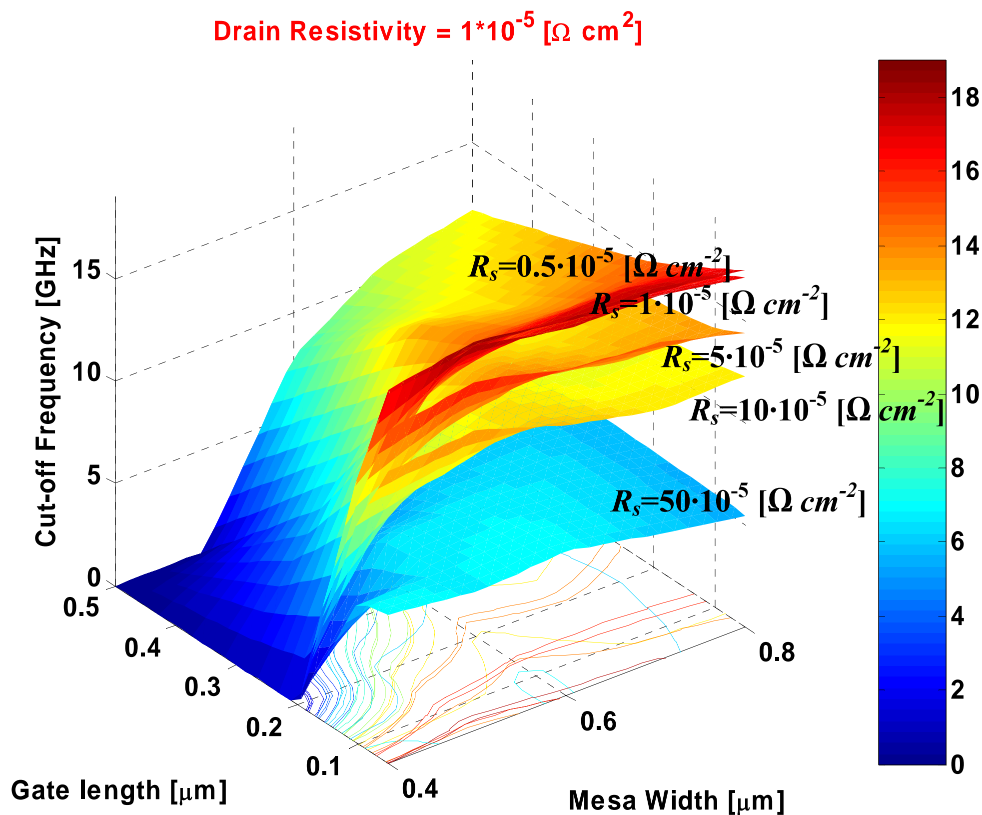
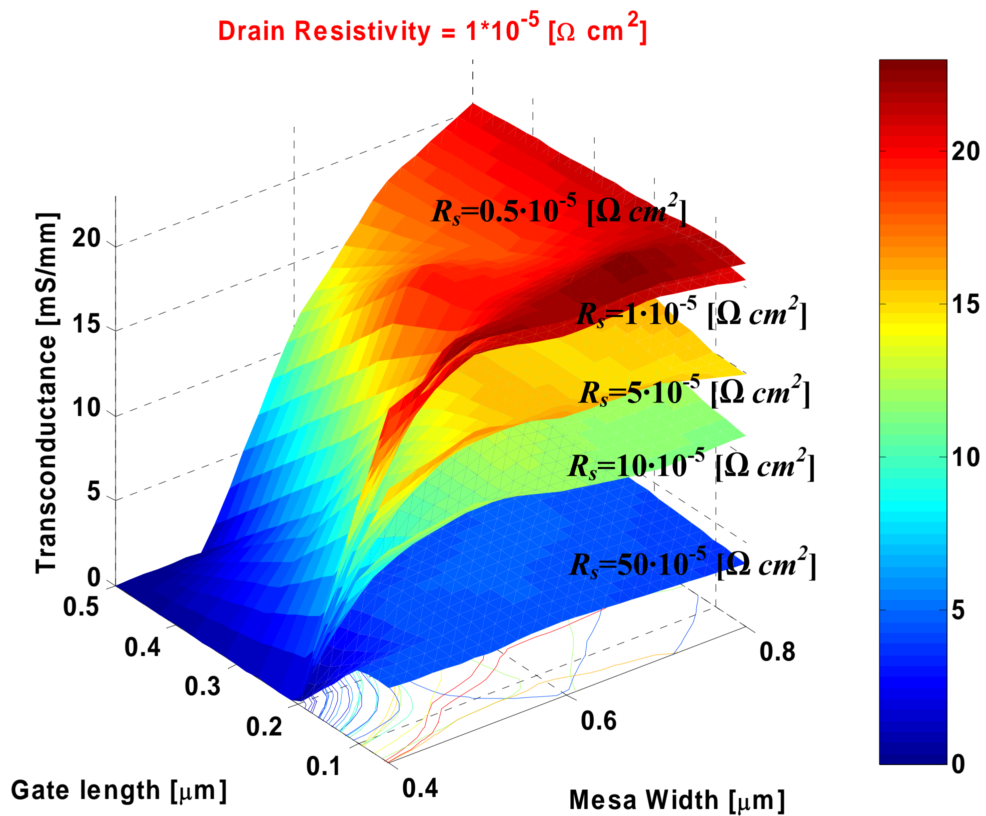


Figure 4.5 Cut-off Frequency as a function of gate length and mesa width with drain contact resistivity $1{\cdot}10^{-5}$ [Ω cm^2].

In the Fig 4.6, as source contact resistivity increase, transconductance decrease with drain contact resistivity $1{\cdot}10^{-5}$ [Ω cm^2]. Decrease rate of transconductance is

higher than that of cut-off frequency in Fig 4.5. The gate-drain capacitance and the gate-source capacitance diminish cut-off frequency decrease rate for source contact resistivity increase. It is very important to us because we look for higher frequency device.



ure 4.6 Transconductance as a function of gate length and mesa width at drain contact resistivity $1 \cdot 10^{-5}$ [Ω cm^2], source contact resistivity $0.5 \cdot 10^{-5}$, $1 \cdot 10^{-5}$, $5 \cdot 10^{-5}$, $10 \cdot 10^{-5}$, $50 \cdot 10^{-5}$ [Ω cm^2], from top to bottom, respectively.

The gate-source capacitance is shown in the Fig 4.7. As the source contact resistivity increases, the gate-source capacitance decreases. Contrary to our

expectation, the gate-source capacitance affects to reduce cut-off frequency decrease rate for the source contact resistivity increase. Unfortunately, it is a small rate. On the other hand, as the source contact resistivity increases, the gate-drain capacitance increases.

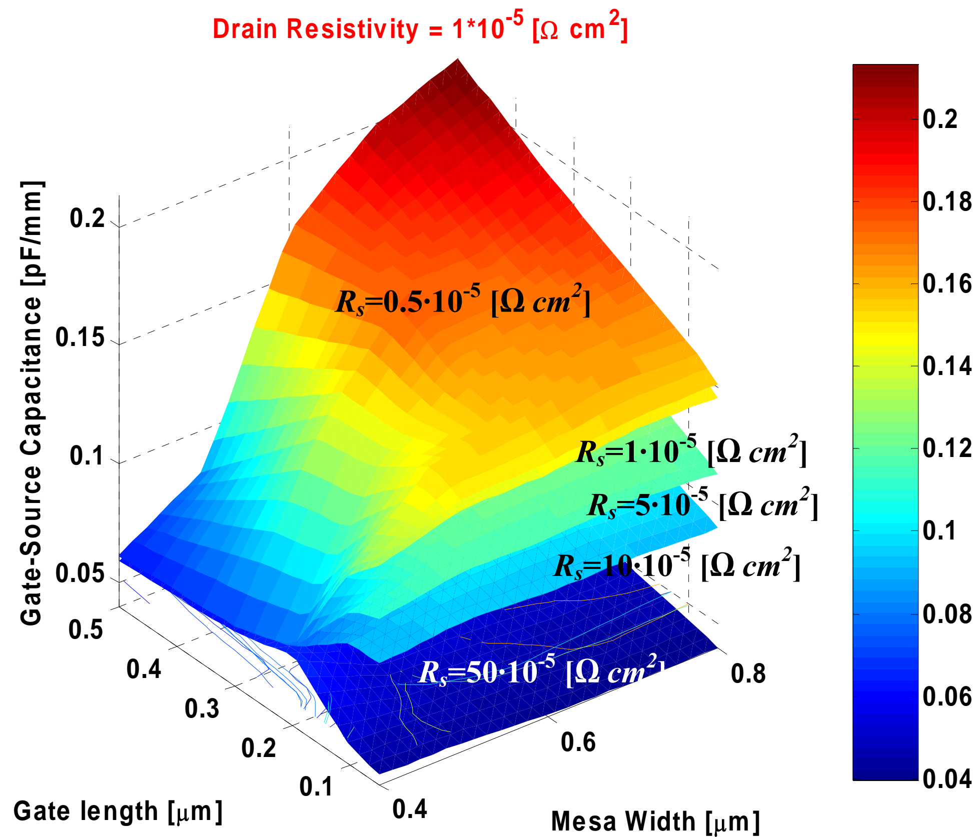


Figure 4.7 Gate-source capacitance as a function of gate length and mesa width with drain contact resistivity $1 \cdot 10^{-5}$ [Ω·cm^2], source contact resistivity $0.5 \cdot 10^{-5}$, $1 \cdot 10^{-5}$, $5 \cdot 10^{-5}$, $10 \cdot 10^{-5}$, $50 \cdot 10^{-5}$ [Ω cm^2], from top to bottom, respectively.

The gate-drain capacitance is shown in Fig. 4.8. The Gate-drain capacitance is a stronger function of mesa width than gate length, unless the source contact resistivity becomes less than $5 \cdot 10^{-5}$ [Ω cm^2]. If a SIT fabricate with the source contact resistivity less than $1 \cdot 10^{-5}$ [Ω cm^2], the gate-drain capacitance should be almost independent of mesa width and proportional to gate length.

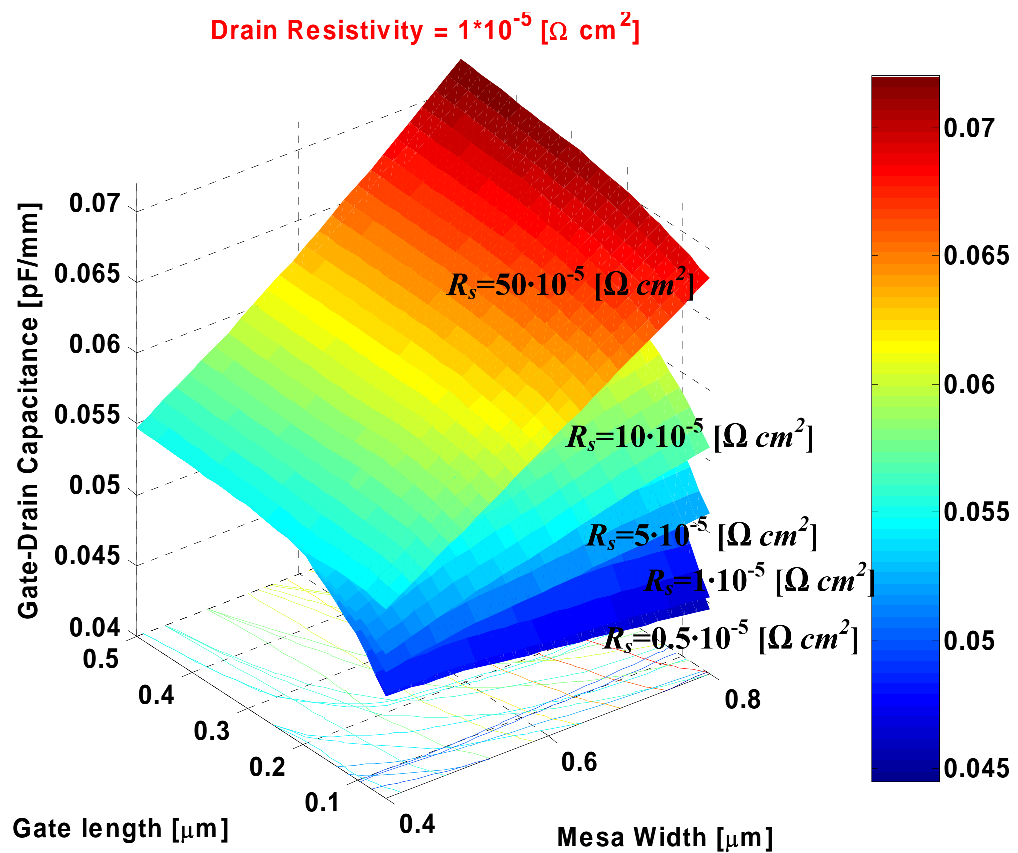


Figure 4.8 Gate-drain capacitance as a function of gate length and mesa width at drain contact resistivity $1 \cdot 10^{-5}$ [$\Omega \cdot cm^2$], source contact resistivity $50 \cdot 10^{-5}$, $10 \cdot 10^{-5}$, $5 \cdot 10^{-5}$, $1 \cdot 10^{-5}$, $0.5 \cdot 10^{-5}$ [Ω cm^2], from top to bottom, respectively.

Reversely, in Fig 4.9 the cut-off frequency shown as a function of mesa width and gate width with source contact resistivity $1.0 \cdot 10^{-5}$ [Ω cm^2] for drain contact resistivity

increase. The cut-off frequency decrease rate is less than that of drain contact resistivity $1.0 \cdot 10^{-5}$ [Ω cm^2] in Fig 4.5. Typically, the drain contact resistivity is slightly ignored. But there are the differences that the effects of the drain contact resistivity increase. When the drain contact resistivity increases to $5 \cdot 10^{-5}$ [Ω cm^2], the cut-off frequency decrease about 10%. It is shown in Fig. 4.9.

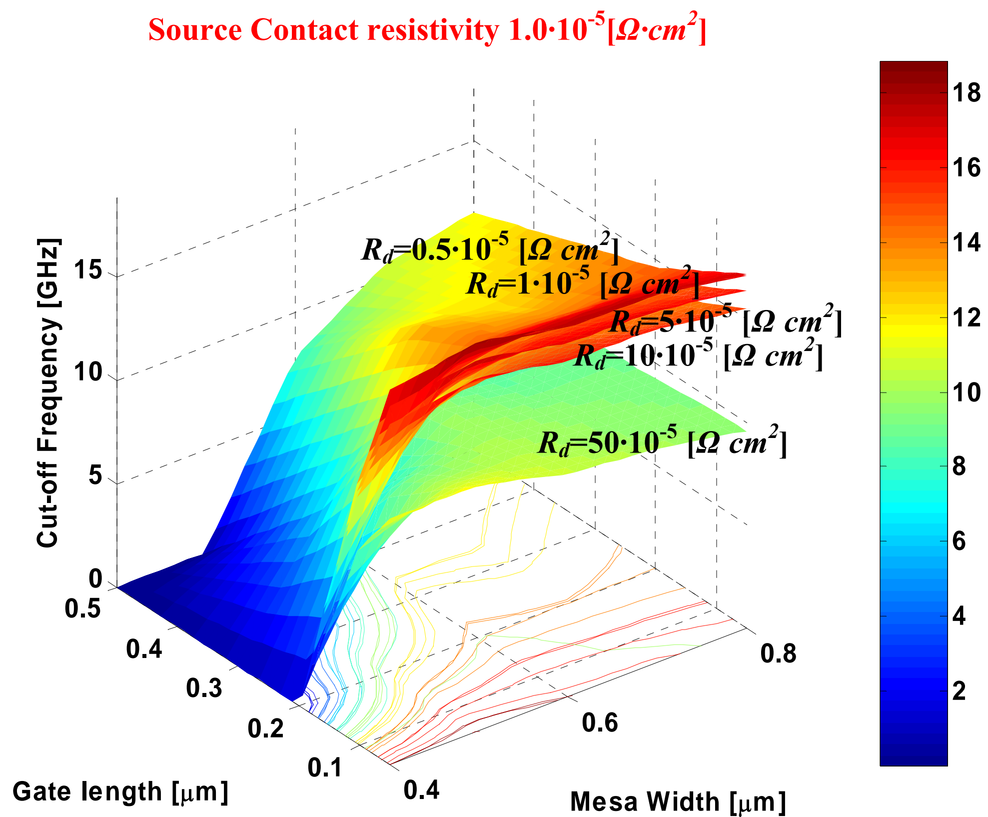


Figure 4.9 Cut-off Frequency as a function of gate length and mesa width with source contact resistivity $1.0 \cdot 10^{-5}$ [Ω cm^2], drain contact resistivity $0.5 \cdot 10^{-5}$, $1 \cdot 10^{-5}$, $5 \cdot 10^{-5}$, $10 \cdot 10^{-5}$, $50 \cdot 10^{-5}$ [Ω cm^2], from top to bottom, respectively.

The transconductance is shown in Fig. 4.10 with source contact resistivity $1\cdot10^{-5}$ [Ω cm^2] for drain contact resistivity increase. The transconductance decrease rate is relatively small compared with that of an increased source contact resistivity shown in the Fig. 4.6. The effect of an increased drain resistivity with source contact resistivity $1\cdot10^{-5}$ [Ω cm^2] is a reduction in the transconductance as a result of the increase channel resistance.

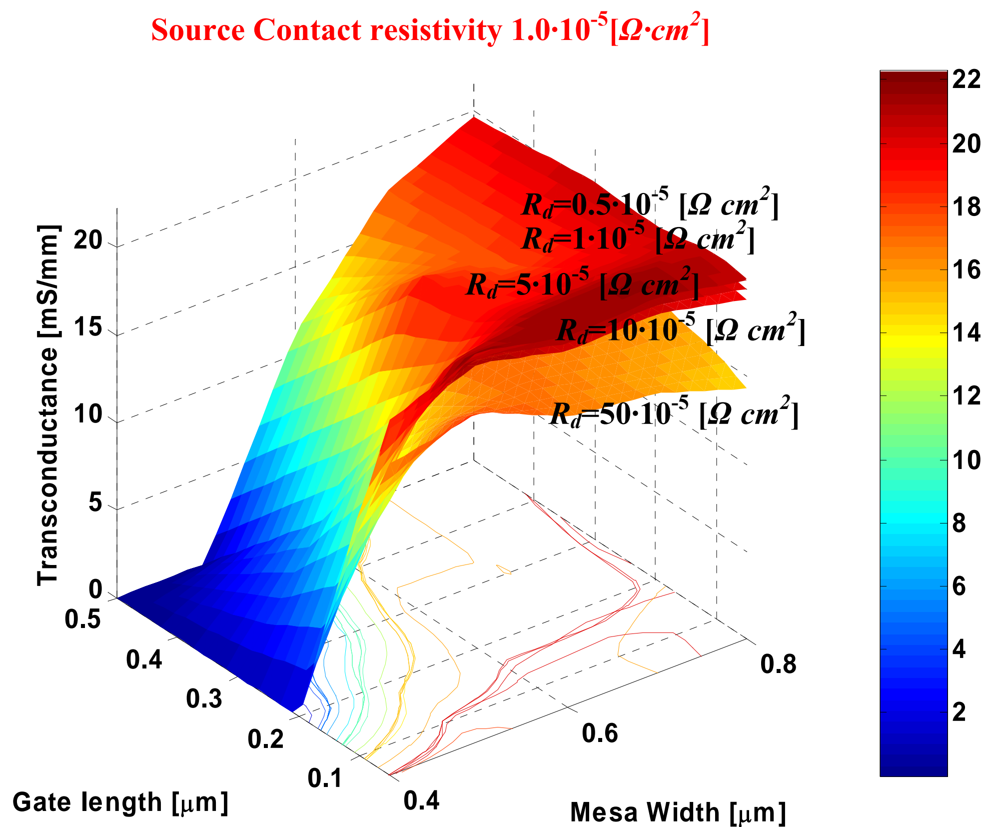


Figure 4.10 Transconductance as a function of gate length and mesa width at source contact resistivity $1\cdot10^{-5}$ [Ω cm^2], from top drain contact resistivity $0.5\cdot10^{-5}$, $1\cdot10^{-5}$, $5\cdot10^{-5}$, $10\cdot10^{-5}$, $50\cdot10^{-5}$ [Ω cm^2], respectively.

We can see that the reversed effect of an increased drain resistivity in related cut-off frequency and transconductance. In previous results (Fig 4.5 and Fig 4.6), as source contact resistivity increase, the transconductance decrease rate is higher than that of cut-off frequency. The gate-source capacitance is shown in Fig.4.11 as a function of gate length and mesa width at source contact resistivity $1 \cdot 10^{-5}$ [Ω cm^2], from top to bottom drain contact resistivity $50 \cdot 10^{-5}$, $10 \cdot 10^{-5}$, $5 \cdot 10^{-5}$, $1 \cdot 10^{-5}$, $0.5 \cdot 10^{-5}$ [Ω cm^2], respectively.

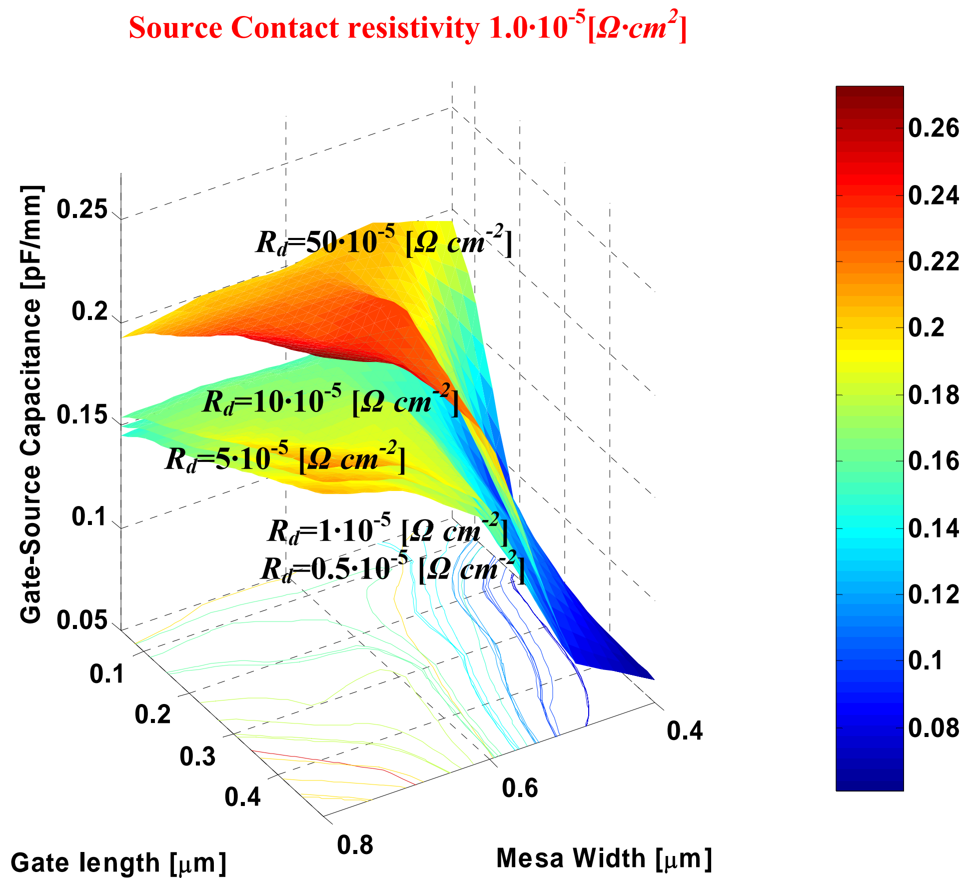


Figure 4.11 Gate-source Capacitance as a function of gate length and mesa width with source contact resistivity $1 \cdot 10^{-5}$ [Ω cm^2], from top drain contact resistivity $50 \cdot 10^{-5}$, $10 \cdot 10^{-5}$, $5 \cdot 10^{-5}$, $1 \cdot 10^{-5}$, $0.5 \cdot 10^{-5}$ [Ω cm^2], respectively

The gate-source capacitance increase rate is relatively small compared with that of an increased source contact resistivity shown in the Fig. 4.7. But it is that the reversed rate. Namely, in Fig. 4.7, as source contact resistivity increase, gate-source capacitance decrease. But, as drain contact resistivity increase, gate-source capacitance increase in Fig. 4.11. It is a significant result but its analysis turn to future work. The gate-drain capacitance is shown in Fig. 4.12 as a function mesa width and gate length with source contact resistivity $1 \cdot 10^{-5}$ [Ω cm^2], it is proportional to mesa width. As drain contact resistivity increase, the gate-drain capacitance increase with a small rate.

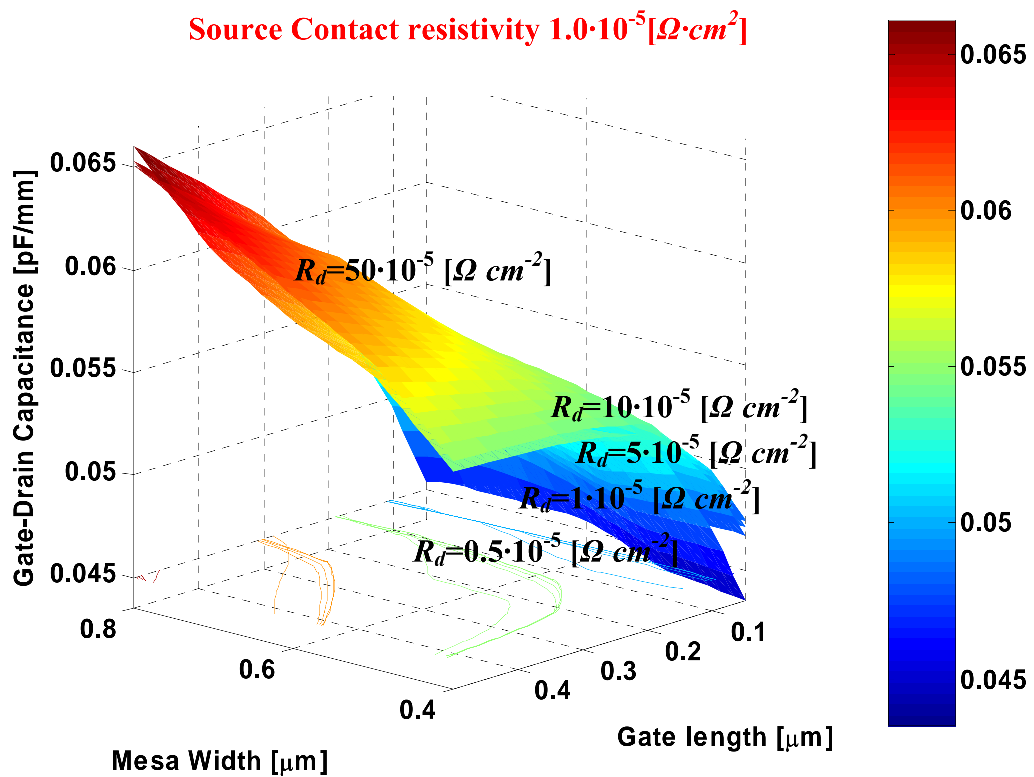


Figure 4.12 Gate-Drain Capacitance as a function of gate length and mesa width at source contact resistivity $1 \cdot 10^{-5}$ [Ω cm^2], from top drain contact resistivity $50 \cdot 10^{-5}$, $10 \cdot 10^{-5}$, $5 \cdot 10^{-5}$, $1 \cdot 10^{-5}$, $0.5 \cdot 10^{-5}$ [Ω cm^2], respectively.

3. Effect of Mobility

3.1. Analytic Mobility

The carrier mobilities μ_n and μ_p account for scattering mechanisms in electrical transport. MEDICI provides several mobility model choices.

As an alternative to the concentration-dependent mobility, the mobility is concentration- and temperature-dependent empirical mobility function. These are given by the expressions [7]

$$\mu_{n,p} = \mu_{\min} + \frac{\mu_{\max}\left(\frac{T}{300}\right)^{N^{\mu}_{n,p}} - \mu_{\min}}{1+(\frac{T}{300})^{xin,p}(\frac{N_{total}(x,y)}{N_{refn,p}})^{\alpha_{n,p}}} \tag{4-16}$$

where, $N_{total}(x,y)$ is the local total impurity concentration (in #/cm3) and T is the temperature (in K).

In most case, this mobility model is used in semiconductor device simulation.

3.2 Perpendicular Electric Mobility Model

This model is applied at every position in the device and not just at interfaces or in the inversion layer and is described by modified of Analytic Mobility *Eqn.* (4-16)

$$\mu_{S,n,p} = G_{surfacn,p} \cdot \frac{\mu_{n,p}}{\sqrt{1+\frac{E_{\perp,n,p}}{E^{\mu}_{cn,p}}}} \tag{4-17}$$

where $E_{\perp,n}$, and $E_{\perp,p}$ are the components of electric that are perpendicular to the side of an element (the default) or the components of electric perpendicular to the current

direction. The factors $G_{surfacn}$ and $G_{surfacp}$ are only applied at interfaces between semiconductor and insulator.

3.3 Surface Mobility Model

Along insulator-semiconductor interface, the carrier mobilities can be substantially lower than in the bulk of the semiconductor due to surface scattering. This model is only applied at the interface because it assumes that the carrier inversion layer width is smaller than the grid spacing used at the interface. With this assumption, all the inversion charge effectively occurs at the interface, and it is appropriate to use this model. This model calculates effective mobilities at the interfaces using the expressions

$$\mu_{S,n,p(Surface)} = G_{surfan,p}(\frac{E_{eff_{\perp},n,p}}{E_{refn,p}})^{-exn,p}\mu_{refn,p} \quad (4\text{-}18)$$

Also, an enhanced surface mobility model has been included in MEDICI that takes into account phonon scattering, surface roughness scattering, and charges impurity scattering.

3.4 Hewlett-Packard Mobility Model

The Hewlett-Packard Mobility model takes account dependence on electric fields both parallel and perpendicular to the direction of current flow. The expressions for mobility used by this model are

$$\mu_{n,p} = \frac{\mu_{\perp,n,p}}{\sqrt{1 + \dfrac{\left(\dfrac{\mu_{\perp,n,p} E_{\parallel,n,p}}{V_{cn}^{HP}}\right)^2}{\dfrac{\mu_{\perp,n,p} E_{\parallel,n,p}}{V_{cn}^{HP}} + G_{n,p}^{HP}} + \left(\dfrac{\mu_{\perp,n,p} E_{\parallel,n,p}}{V_{sn,p}^{HP}}\right)^2}} \tag{4-19}$$

The expressions for $\mu_{\perp,n,p}$ are given by

$$\mu_{\perp,n,p} = \frac{\mu_0^{HP}}{1 + \dfrac{E_{\perp,n,p}}{E_{cn,p}^{HP}}} \text{ if } N_{total}(x,y) < N_{ref}^{Hp} \tag{4-20}$$

Where, the default value for N_{ref}^{Hp} is $5 \cdot 10^{17}$. if above condition is not satisfied, then $\mu_{\perp,n,p} = \mu_{n,p}$, where $\mu_{\perp n,p}$ are low field mobility values described in 3.1 Analytic Mobility.

The cut-off frequency shown in Fig. 4.13 and Fig. 4.14 is calculated by above mobility models, respectively. The cut-off frequency calculated by Analytic Mobility is highest. This can be explained by the fact that the current flow for a device occurs primarily at the interface and is directed along the edges of elements that make up the interface; therefore, in two case (Hewlett-Packard Mobility, Perpendicular Electric Mobility Model) the components of electric field parallel and perpendicular to the sides of the interface elements are almost identical to the components of field parallel and perpendicular to the direction of current. This accounts for the nearly-identical results.

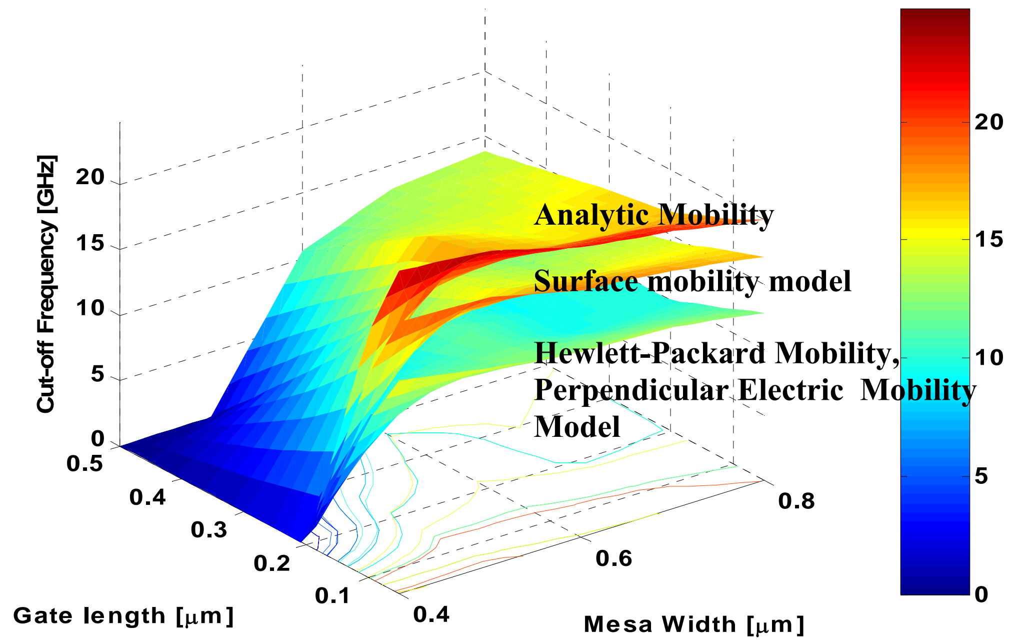


Figure 4.13 Cut-off Frequency depend on mobility model

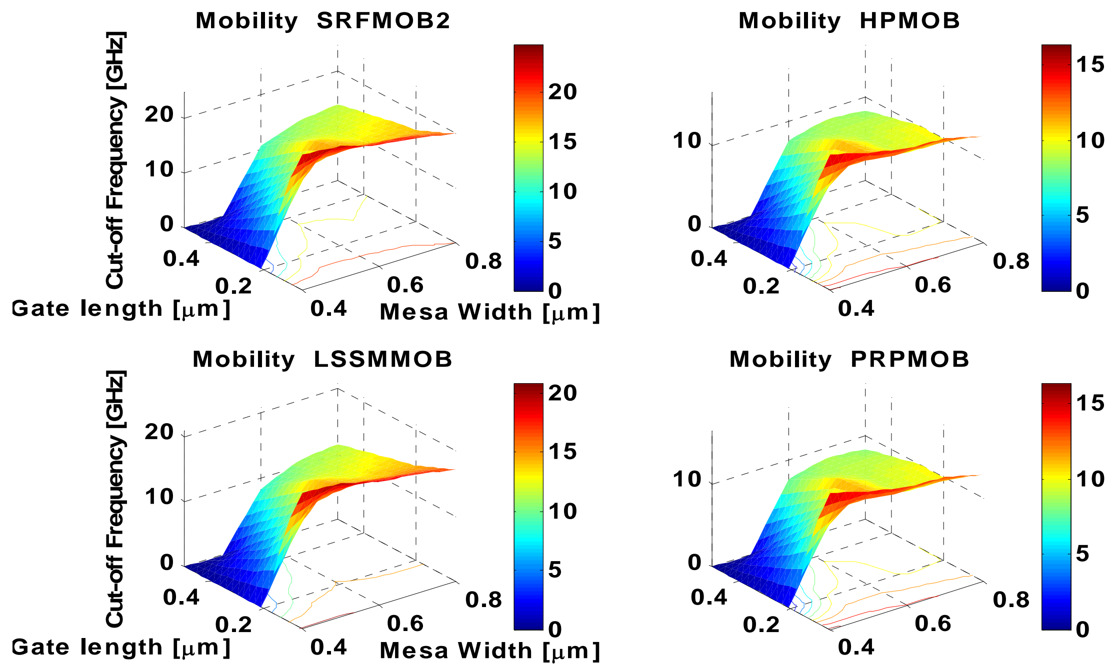


Figure 4.14 Cut-off Frequency in several mobility models, LSSMMOB : Analtic Mobility model, HPMOB : Hewlett Parkard mobility, SRFMOB : Surface mobility model, PRPMOB : Perpendicular Electric Mobility.

4. Effect of Saturation Drift velocity

In semiconductor device design, one of the most important parameters is a saturated drift velocity that the relationship between the drift velocity of electrons and applied electric filed. The first measurements of the high-filed drift velocity of electrons in SiC were performed by von Müench and Pettenpaul in 1977 on Lely crystals of 6H-SiC. They reported an electron saturation velocity of $2 \cdot 10^7$ cm/s parallel to the basal plane at room temperature. But recently, the drift saturation velocity is reported to reach $1.9 \cdot 10^7$ *cm/s* in 6H-SiC and $2.2 \cdot 10^7$ *cm/s* in 4H-SiC, measured at both room temperature [8]. Therefore, in this work, we simulated the device behavior with different saturated drift velocities, respectively.

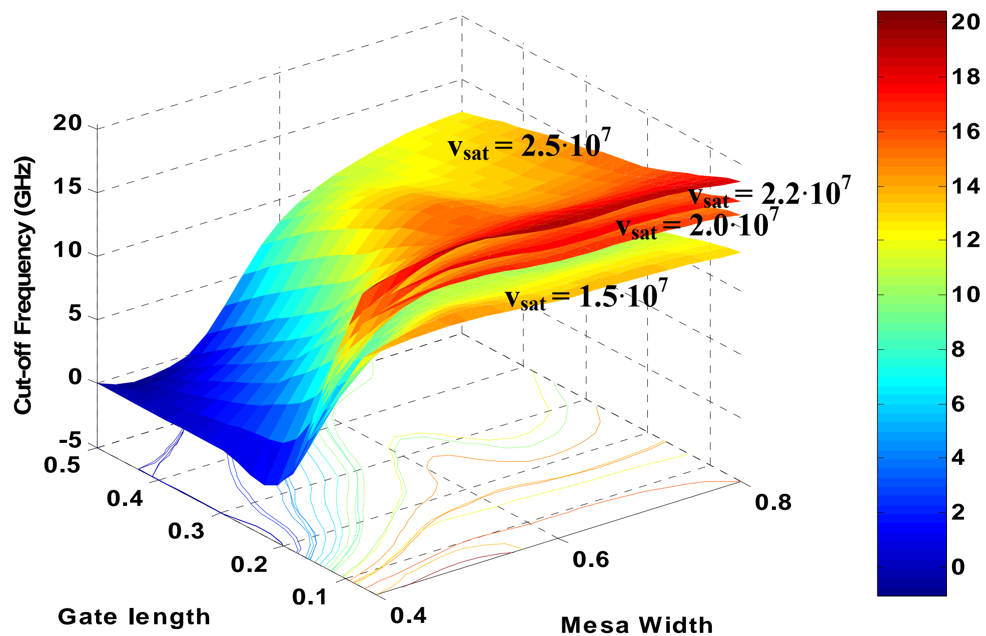


Figure 4.15 Cut-off Frequency depend on Saturation Drift velocity.

The cut-off frequency depended on saturation drift velocity is shown in Fig. 4.15. Also, it is shown that the saturation drift velocity is very critical parameter in device simulation. The cut-off frequency difference of a simulated result is about 10% compare with that of v_{sat}, $2.2{\cdot}10^7$ *cm/s,* and $2.0{\cdot}10^7$ *cm/s*. The transconductance is shown in Fig 4.16. As saturation drift velocity increase, transconductance increase. The increase rate is almost equal to that of cut-off frequency as shown in Fig 4.15. It is that the increased cut-off frequency is attributed to an increased transconductance for a high saturation drift velocity.

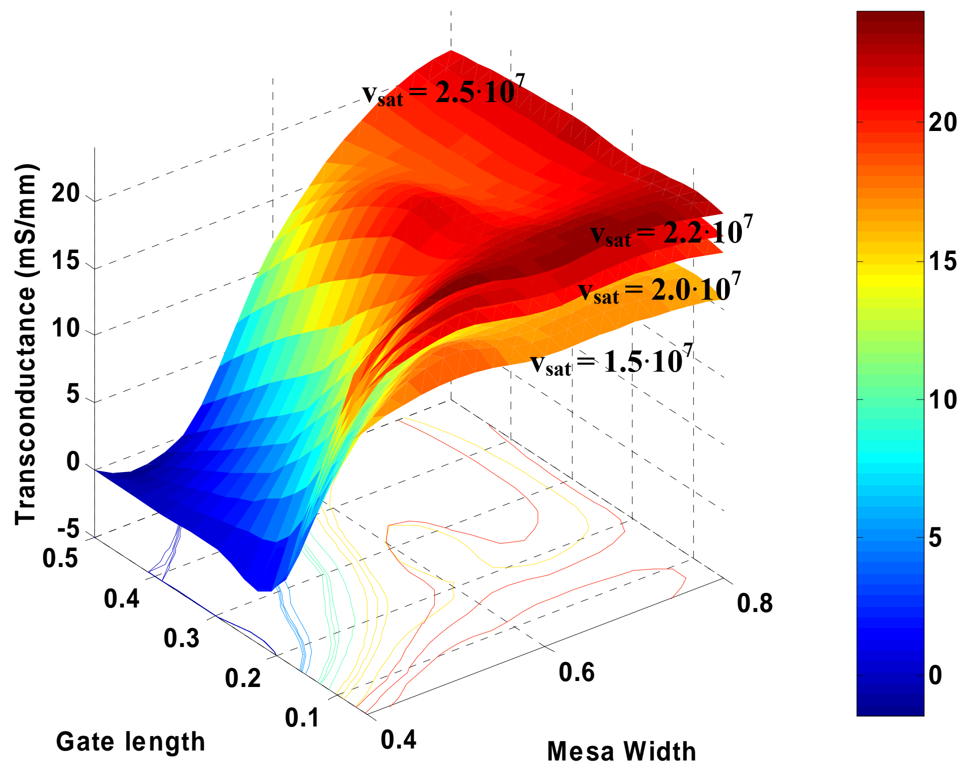


Figure 4.16 Transconductors depend on Saturation Drift velocity, from top to bottom, $2.5{\cdot}10^7$, $2.2{\cdot}10^7$, $2.0{\cdot}10^7$ and $1.5{\cdot}10^7$[*cm/s*], respectively.

The gate-drain capacitance is shown in Fig 4.17 with saturation drift velocity. : $1.5{\cdot}10^7, 2.0{\cdot}10^7, 2.2{\cdot}10^7$, and $2.5{\cdot}10^7$[*cm/s*]. As saturation drift velocity increase, gate-drain capacitance increase. On the other hand, as saturation drift velocity increase, gate-source capacitance decrease. It is shown in Fig. 4.18. However, this effect of an increased saturation drift velocity is similar to that of an increased source contact resistivity in Fig. 4.7, the rate is less than that of an increased source contact resistivity.

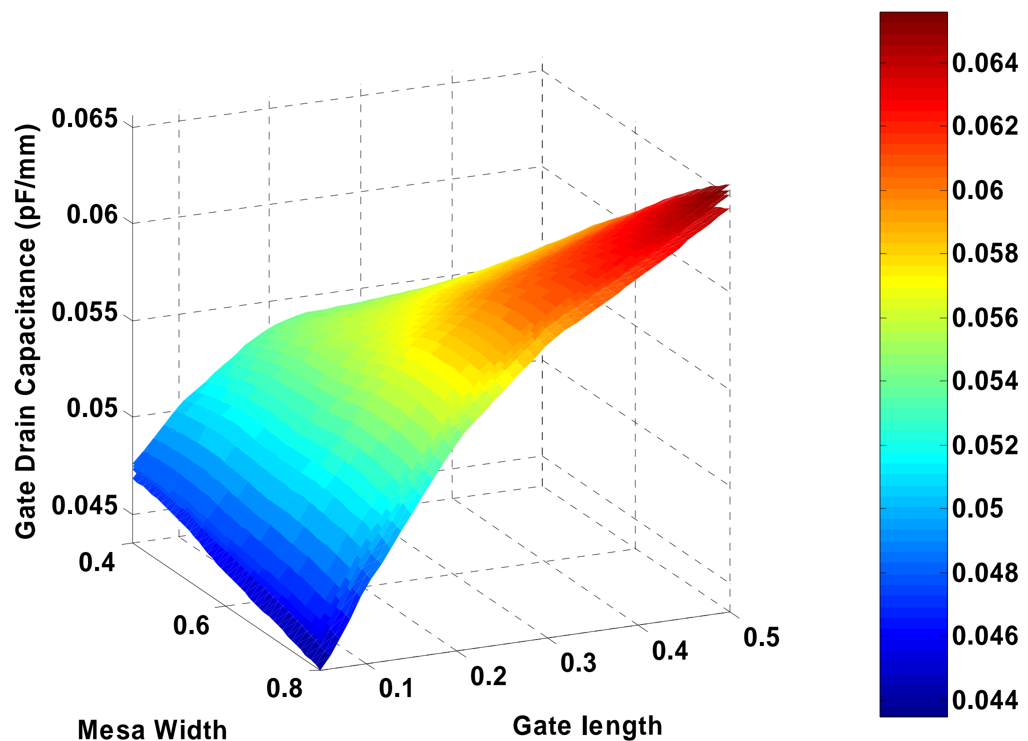


Figure 4.17 Gate-drain capacitances in other saturation drift velocity, from top to bottom, v_{sat} : $2.5 \cdot 10^7, 2.2 \cdot 10^7, 2.0 \cdot 10^7$, and $1.5 \cdot 10^7$[*cm/s*].

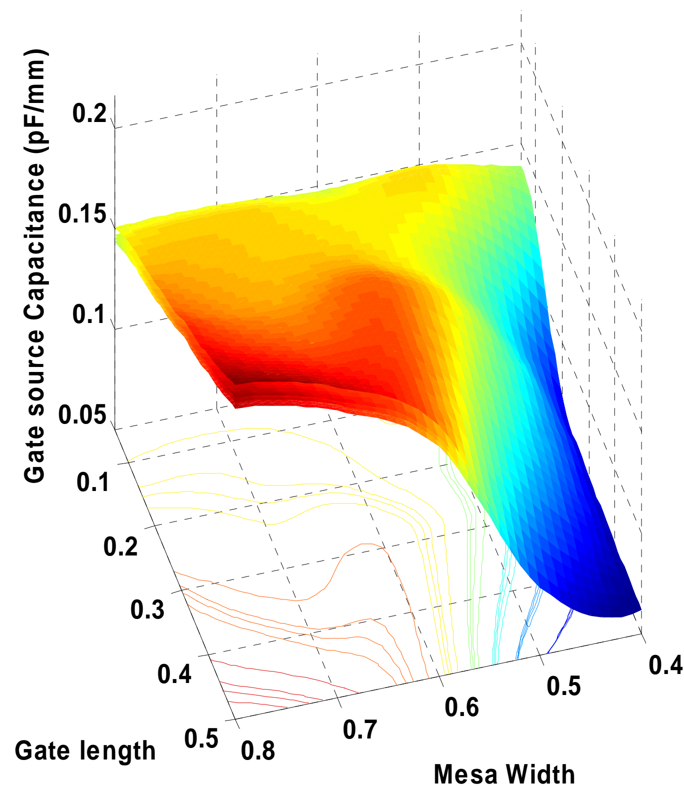


Figure 4.18 Gate-source capacitances in other saturation drift velocity, from top to bottom, v_{sat} : 1.5 · 10^7, 2.0 · 10^7, 2.2 · 10^7, and 2.5 · 10^7[*cm/s*].

5. Considerations for high frequency SIT Design

In order to SITs design with high frequencies, scaling of the device doping, gate length and mesa width have the biggest effect. The transconductance increases faster with doping, roughly linearly, than the input capacitance. The cut-off frequencies as a function of doping and for gate length, source contact resistivity $1.0 \cdot 10^{-5}[\Omega \cdot cm^2]$, shown in Fig 4.19, Cut-off frequencies in excess of 40 *GHz* can be obtained for doping $2 \cdot 10^7$ cm^{-3}. However, reduction of trench width is also important because the value of $C_{gd,}$ which contributes to the input capacitance $C_{in}=C_{gd}+C_{gs}$ of device, essentially scales with the trench width *t*. The effect of C_{gd} gains in importance when the doping is increases because C_{gd} can be approximated by the depletion capacitance

under the gate electrode [18]. Also, the reduction in depletion width with increasing doping for a given bias point results in an increase value for C_{gd}. For a scaled trench, the effect of C_{gd} eventually becomes so pronounced that the rise in cut-off frequency for increasing doping levels off. Therefore, it is import to scale the trench together with the mesa width. However, other considerations besides maximizing the frequency response affect the choice of the trench width, such as device heating due to excessive power density.

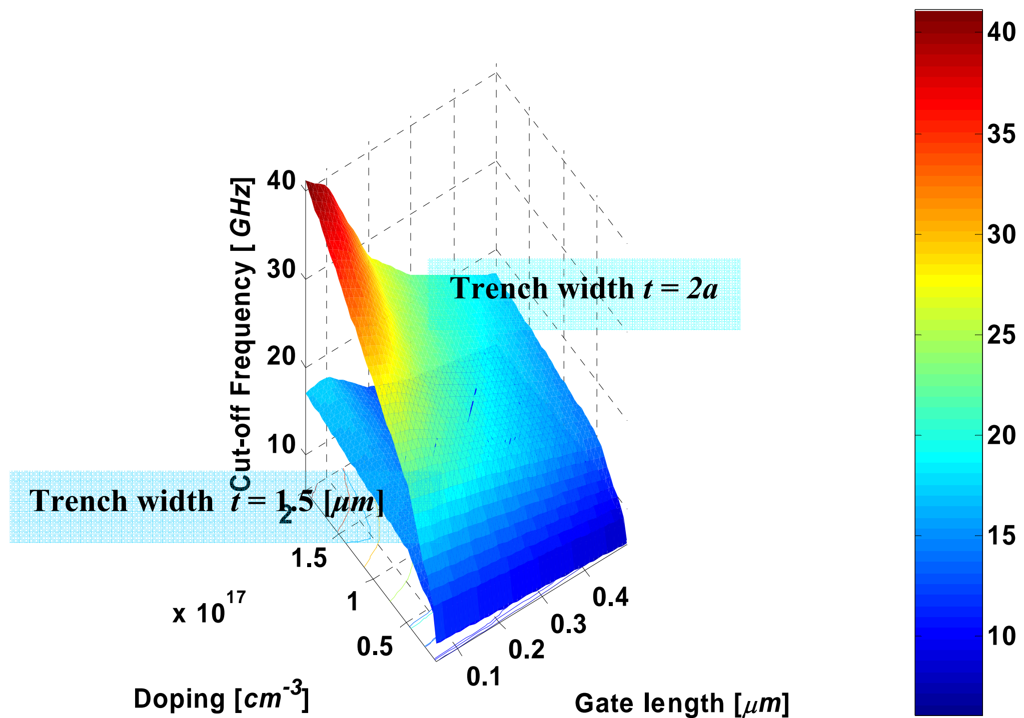


Figure 4.19 Cut-off Frequency as a function Doping N_D and Gate length with source contact resistivity $1.0{\cdot}10^{-5}$ [$\Omega{\cdot}cm^2$].

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CHAPTER V

TEMPERATURE SIMULATIONS

1 Theoretical Considerations

Silicon Carbide (SiC) is a semiconductor material combining several unique features such as high breakdown field, high electron saturation velocity, and high thermal conductivity. These properties make it a promising candidate for RF power transistors. RF Power transistors are commonly operated at high voltage and high current levels leading to considerable self heating. Thus, the operating temperature can be much higher than room temperature. To simulate power transistors under these conditions properly, the temperature dependence of the electron mobility in the both the low-field and high-field region must be also taken into account in the mobility models. Recently, the electron mobility in 4H, 6H, and, 3C SiC has been investigated both experimentally and theoretically by Monte Carlo(MC) simulations by several authors, and models for the electron mobility have been proposed. Unfortunately, none of these models includes detailed temperature dependence for both the low-field and high-field mobilities [1]. In this works, we will use the electron mobility model for SiC RF device simulation. The models are based on the reported mobility data and include the dependence of the mobility on doping concentration, temperature, and electric field. The following 4H-SiC temperature dependent parameters have been determined by [1]

$$\mu_{\max} = 950 \times (\frac{T}{300K})^{-2.4} \quad (5\text{-}1)$$

$$\mu_{\min} = 40 \times (\frac{T}{300K})^{-0.5} \quad (5\text{-}2)$$

$$N_{ref} = 2 \times 10^{17} \times (\frac{T}{300K}) \quad (5\text{-}3)$$

$$\alpha = 0.76 \quad (5\text{-}4)$$

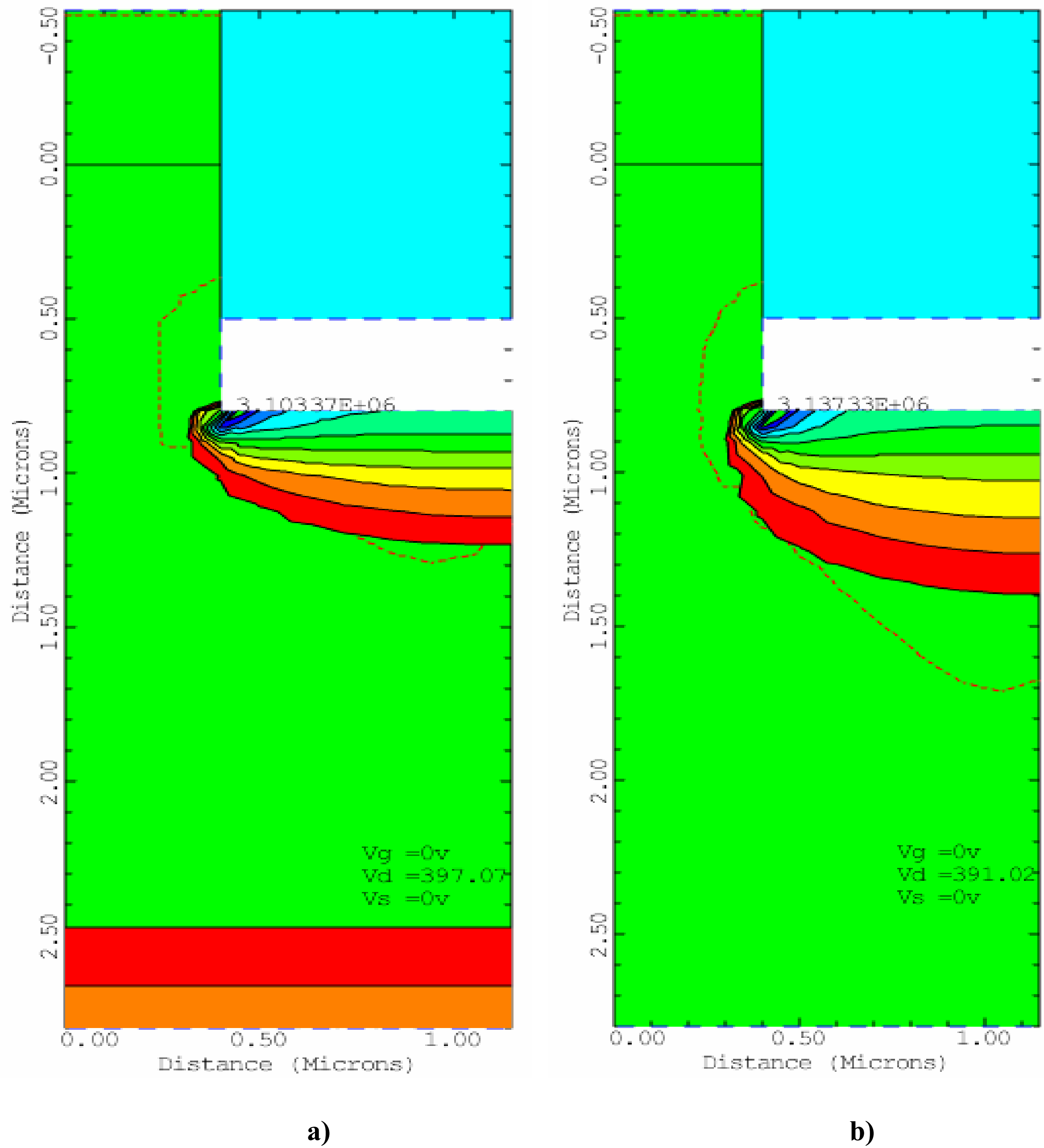
$$\beta = \beta_0 + a \times \exp(\frac{T - T_0}{b}) \quad (5\text{-}5)$$

where β_0, a, b, and T_0 are fitting parameters. a =4.27x10^{-2}, b =98.4 and T_0=327 K.

2 Gate-Drain Breakdown Voltage

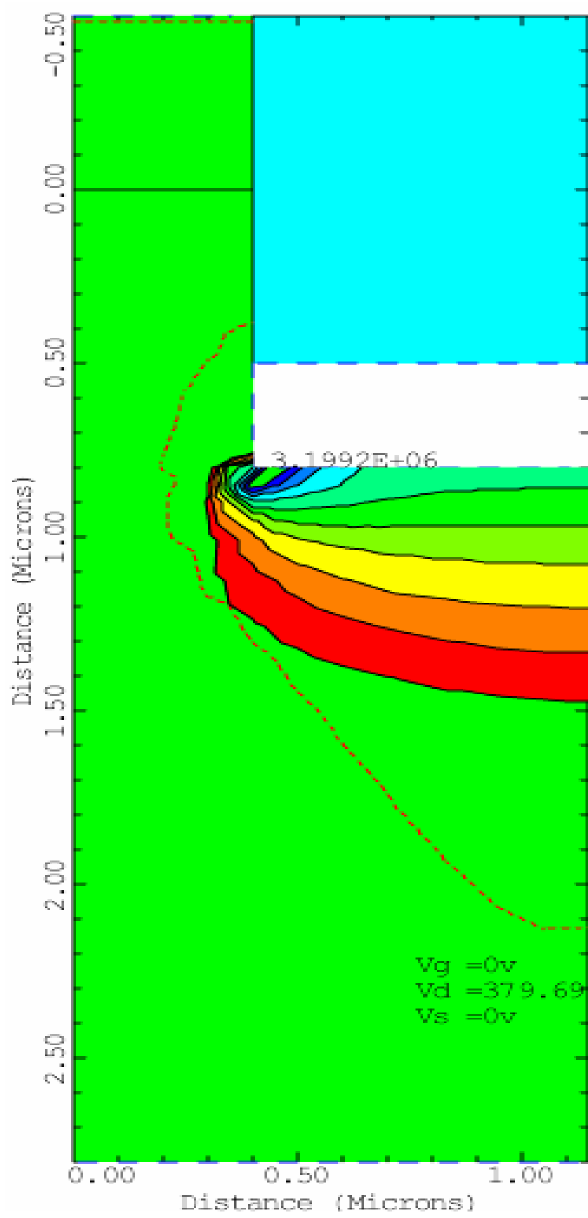
Silicon Carbide (SiC) has received increasing attention for power switching, microwave and high temperature applications due to its high breakdown electric field, thermal conductivity and electron saturation drift velocity. One of the most important parameters of SiC power device is its breakdown voltage. Also, one of the advantages of the static induction transistor is its high output impedance which results from the high breakdown voltage between the gate and drain terminals. This is expected because of the vertical arrangement of the device channels. The gate electrode, in effect, looks like a finely meshed grid such that the overall field distribution approaches that of a parallel plate capacitor. The local field at the very corner of gate is expected to approach arbitrarily high values, depending on how sharp the corner will be in practice, as shown Fig 5.1. However, this field spike does not mean that the breakdown due to avalanche will occur at much lower voltages than predicted by

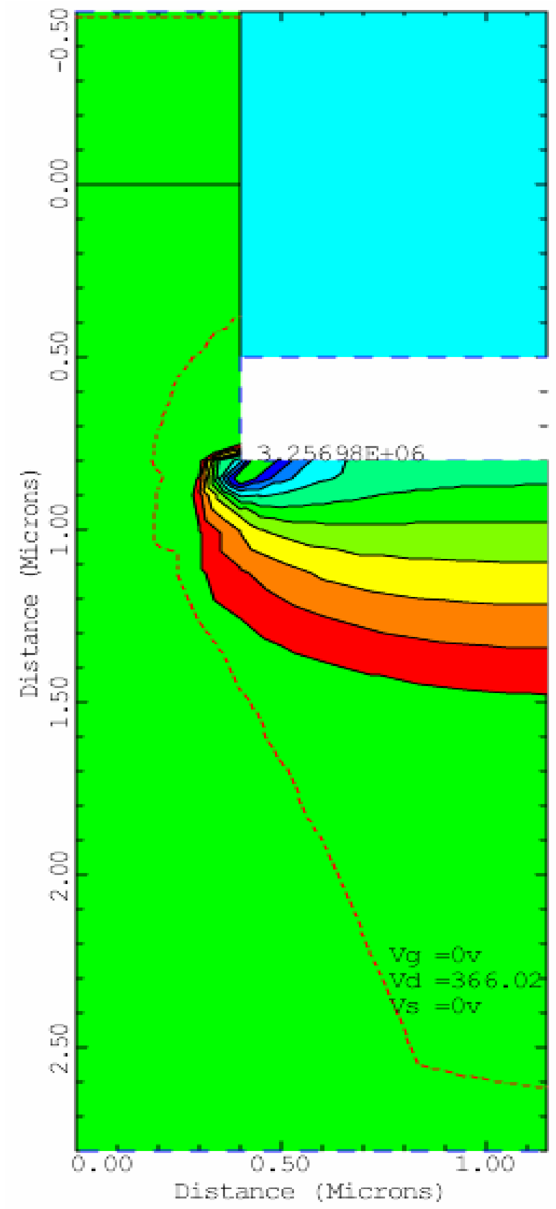
calculation. The avalanche breakdown process occurs when electrons and/or holes, moving across the space charge region, acquire sufficient energy from the electric field to create electron-hole pairs by colliding with atomic electrons within the depletion region. Thus, for avalanche to occur, a high enough electrical field must be supplied to the charge carriers in order to produce electron-hole pairs, and a certain extent of the avalanche region is needed to obtain a round trip gain of unity in order to sustain the avalanche. In this work, because of the importance of the gate-drain breakdown voltage, the maximum obtainable output voltage for a SIT was investigated by means of simulations with several temperatures and doping, respectively.



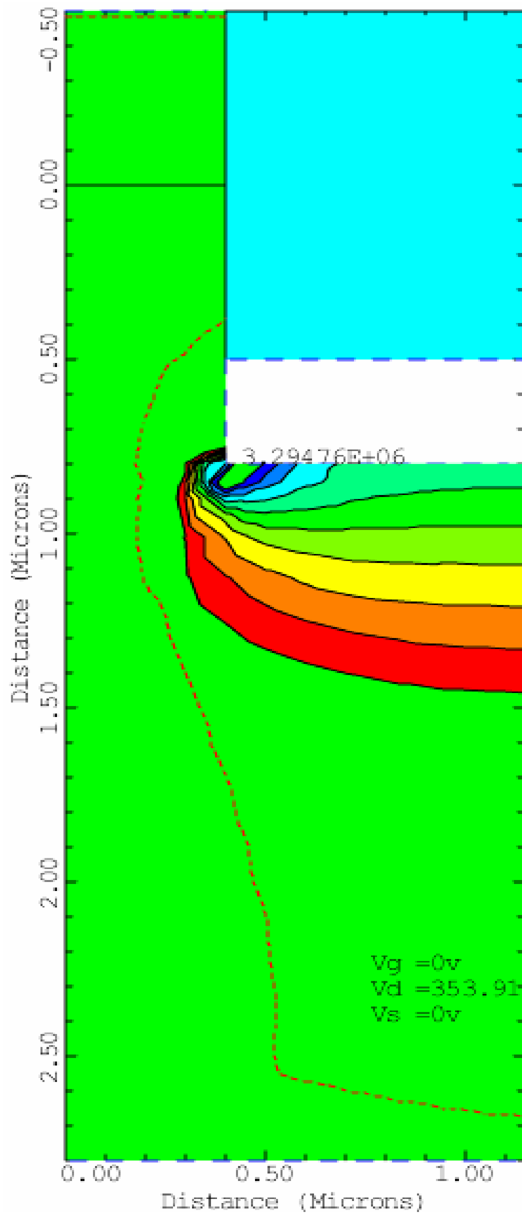
a) **b)**

Figure 5.1 Avalanche Breakdown voltage and Electric Field at Impact Ionization integral reaches unity for a) 300K b) 400K c) 500K d) 600L e)700K f) 800K.

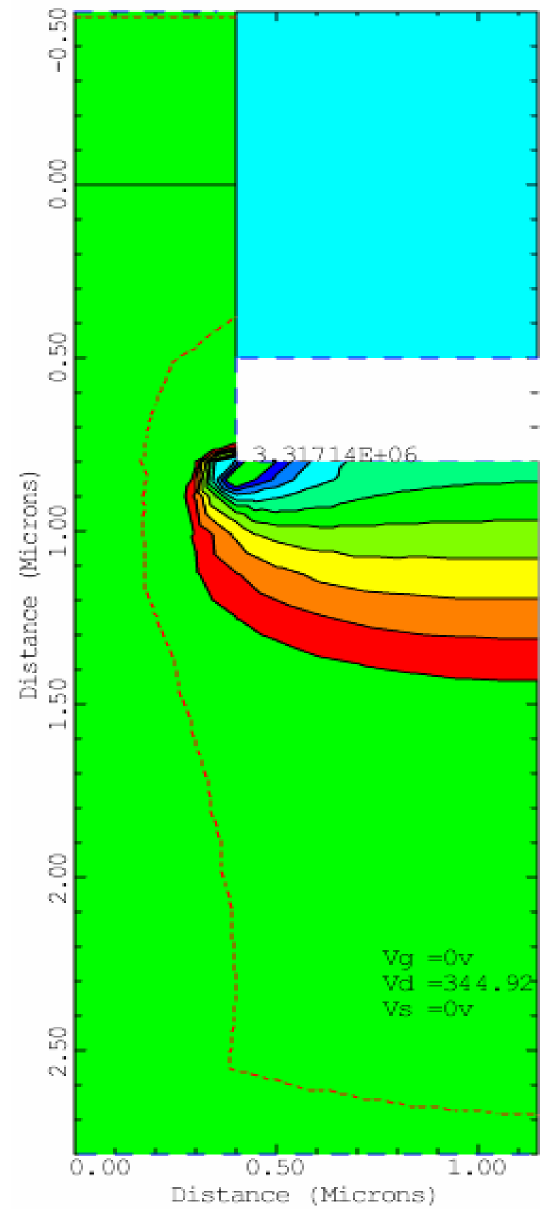




c) d)



e)



f)

In Fig. 5.1, as temperature increases, avalanche breakdown voltages decreases, maximum electric field increases and depletion region increases. The breakdown voltage decrease and depletion region decrease for temperature increase can be explained to more donors ionized. The breakdown voltage due to avalanche breakdown predicted by the impact ionization integral is usually lower for the SIT because it does not take into account that a carrier can escape from the path along the highest field either by diffusion or scattering due to the curvature of the electric field line, thereby decrease the multiplication factor of carriers in the avalanche region. In Fig. 5.1, the drain region is considered with doping concentration $5 \cdot 10^{16} cm^{-3}$ [7]. When the gate-drain voltage is not limited by the gate edge, the device will break down intrinsically at the corner of the gates facing the mesa center. The simulated avalanche breakdown of the device is 397V to 344V for an increased temperature in the drain region. But this avalanche breakdown voltage is roughly 25% lower than one would obtain from a parallel plate calculation. The avalanche breakdown voltage as a function of mesa width and gate length is shown in Fig. 5.2 and Fig. 5.4 for temperature increase with doping $5 \cdot 10^{16} cm^{-3}$. it is shown with $2 \cdot 10^{17} cm^{-3}$ in the Fig 5.3 and Fig 5.5. As temperature increase, breakdown voltage entirely decrease. But as temperature increase, the peak of avalanche breakdown moves to a smaller mesa width and longer gate length region. It is shown in Fig. 5.2 and Fig. 5.5. This effect that breakdown voltage is higher that of the smaller mesa width and longer gate length in the same doping region than that of the others in the same doping region can be explained to more donors ionized, too.

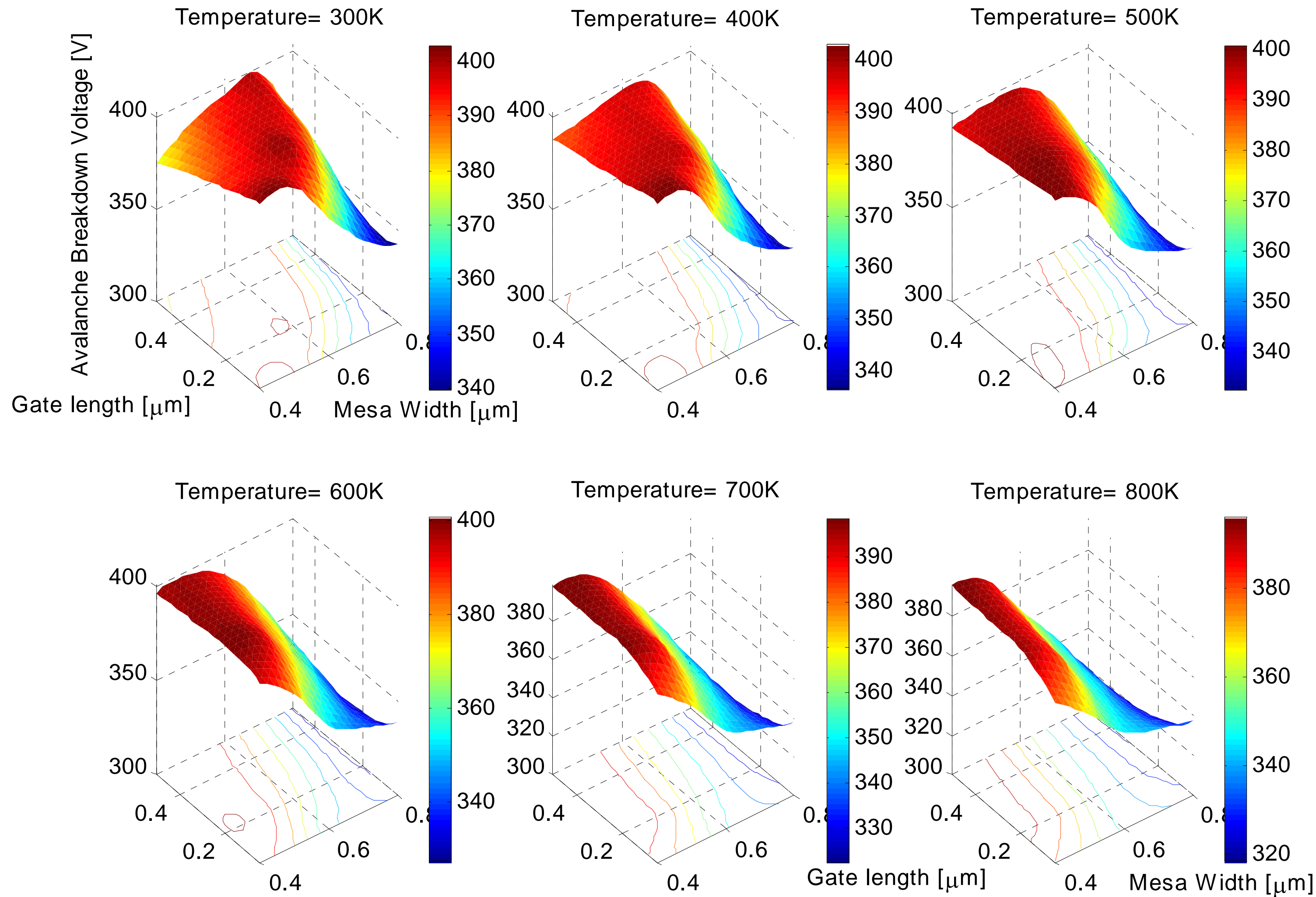


Figure 5.2 Avalanche breakdown voltage as a function of mesa width and gate length with doping 5·10^{16} [cm^{-3}] for temperature increase.

Figure 2.5

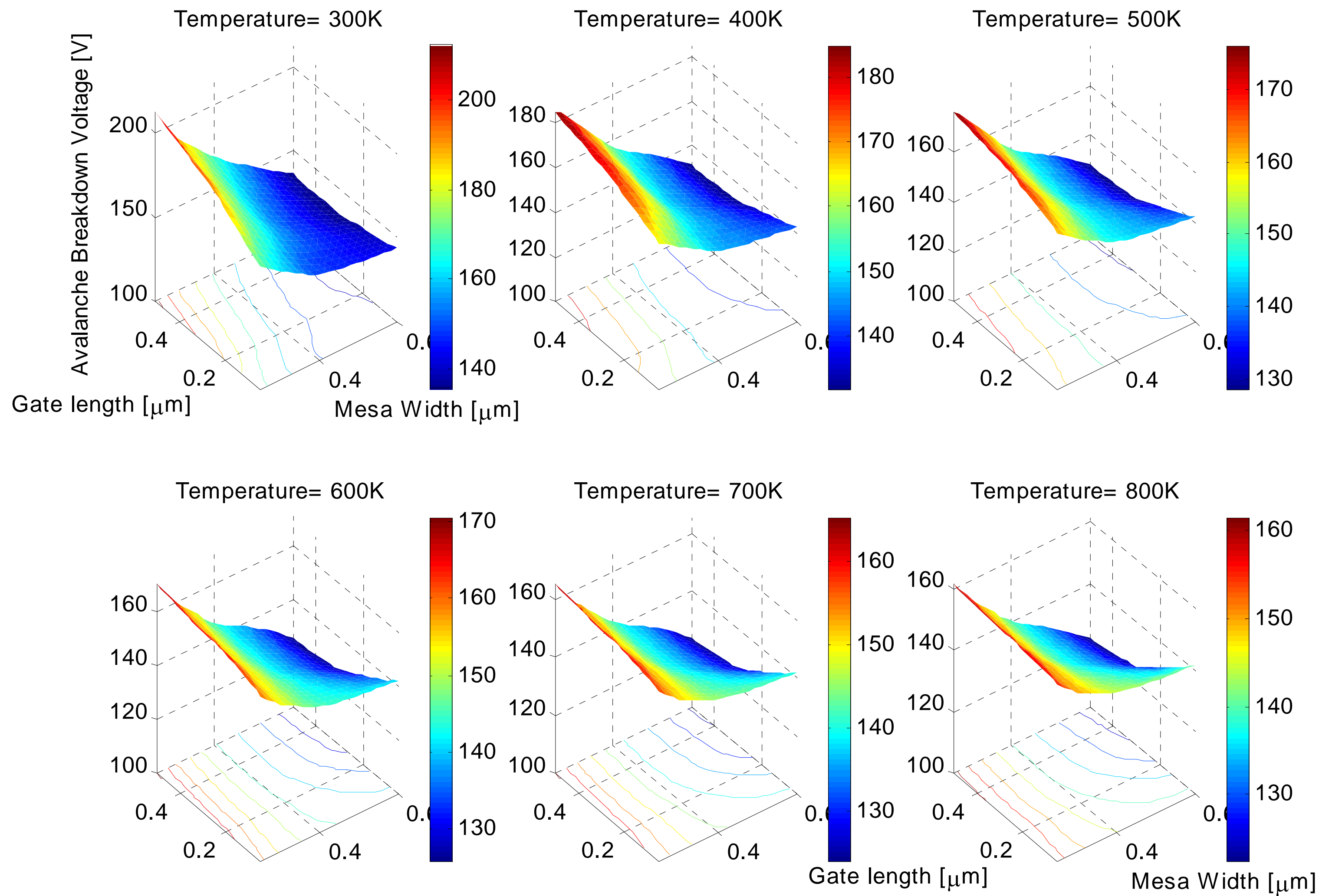


Figure 5.3 Avalanche Breakdown voltage as a function of mesa width and gate length with the doping $2{\cdot}10^{17}$ [cm^{-3}] for temperature increase

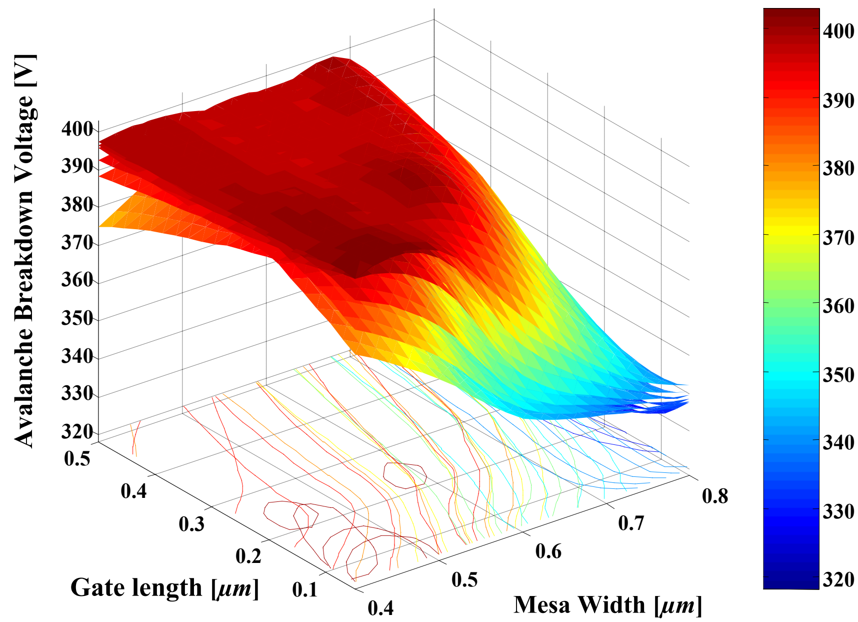


Figure 5.4 Avalanche Breakdown voltage with doping $5\cdot10^{16}$ [cm^{-3}] for temperature increase, from top to bottom, 300K, 400K, 500K 600K 700K, 800K.

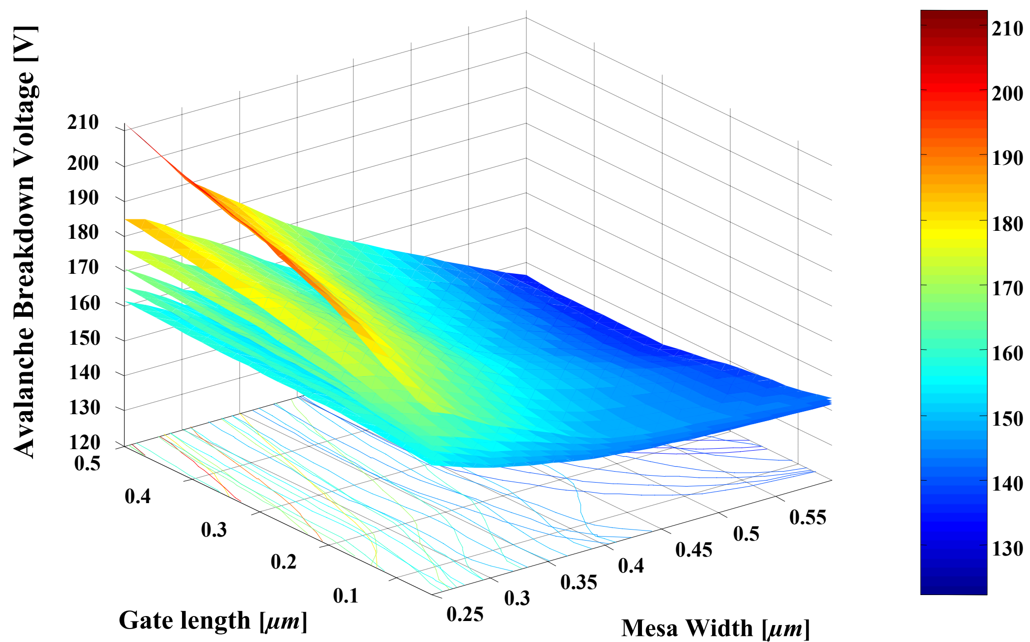
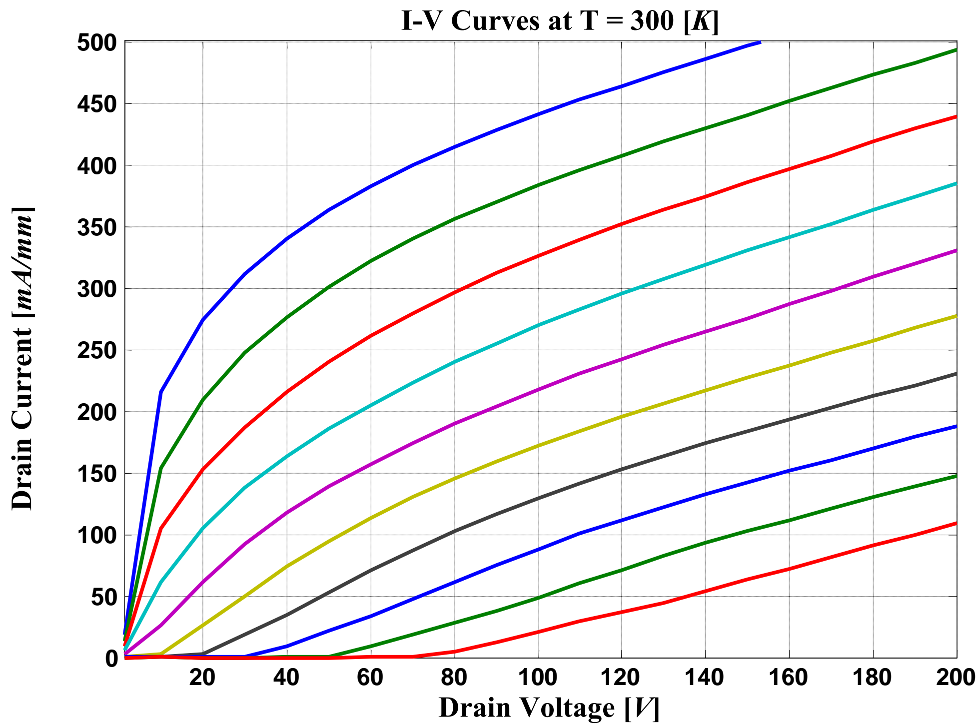


Figure 5.5 Avalanche Breakdown voltage with temperature increasing for the doping $2\cdot10^{17}$ [cm^{-3}], from top to bottom, 300K, 400K, 500K 600K 700K, 800K.

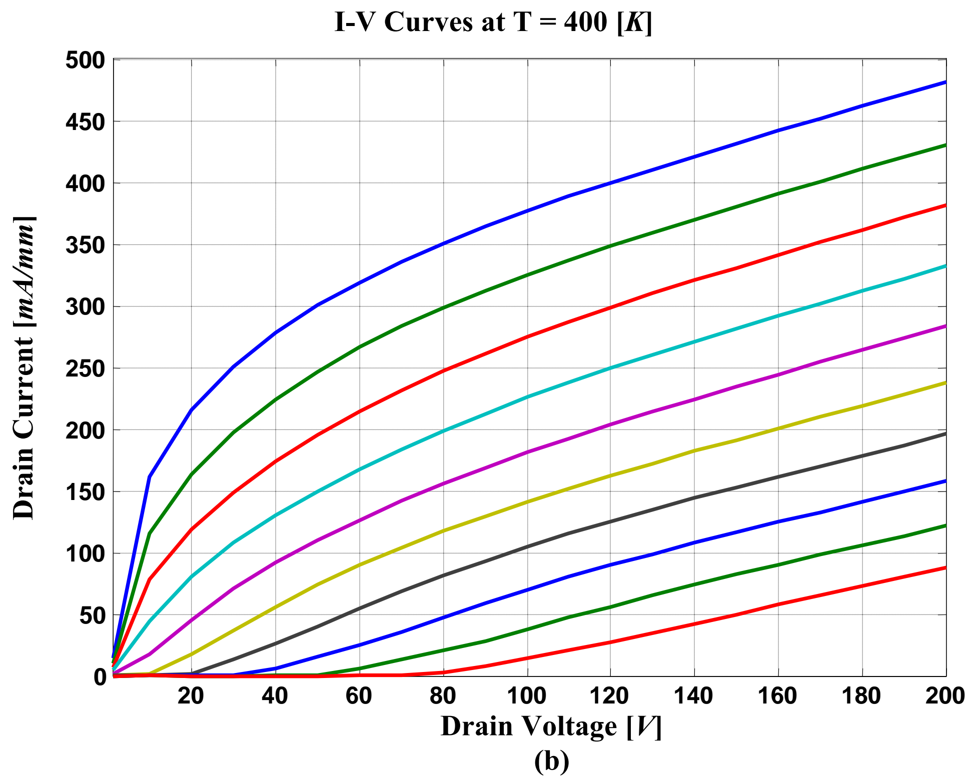
3 Temperature Dependent DC performances

DC performance at the room temperature has been described in chapter 3. The Fig. 5.6 show the I-V curves from 300K to 800K with mesa with 0.6 μm, gate length 0.1 μm, doping $5 \cdot 10^{16}$ cm^{-3}. As the operating temperature increases, the drain current I_{ds} decrease monotonically for $V_g = 0\ V$. At 700K, the saturation current is almost 50% of the 300*K*. This is a quite good comparison with Si device which is completely useless at such temperature. Experimental saturation drain currents show the same trend of temperature dependence. The temperature dependent characteristics can be explained as follows. As temperature increase, more donors are ionized, the depletion width increases, and the effective channel thickness decrease. Thus the total number of mobile carriers increases. On the other hand, the carrier mobilities decrease.

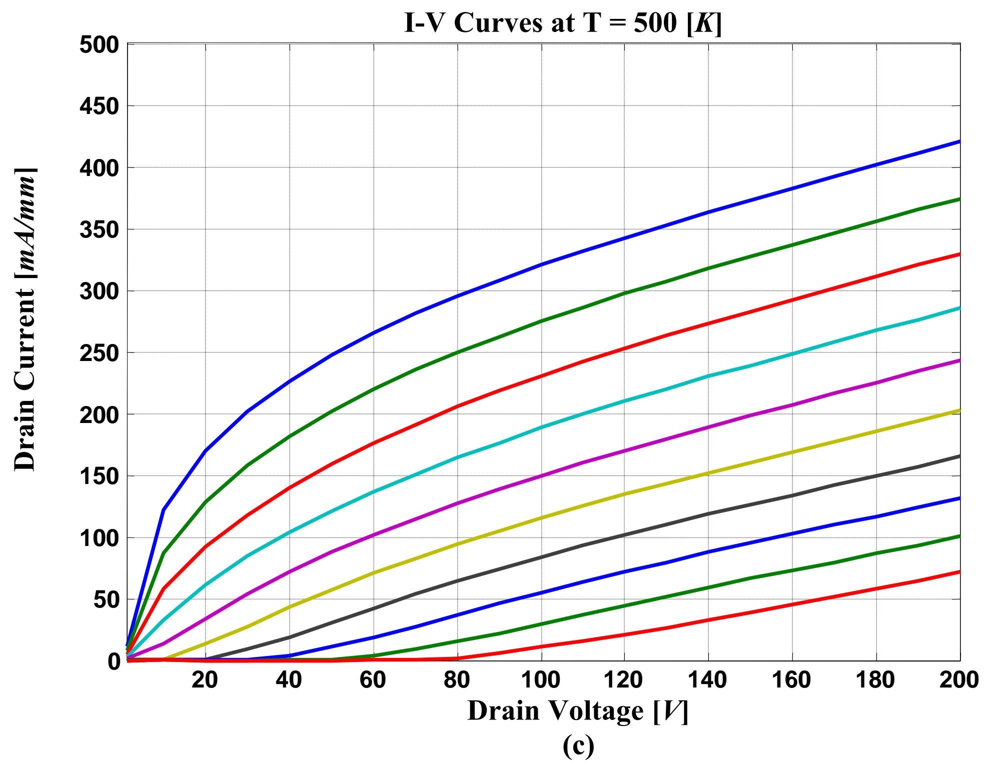


(a)

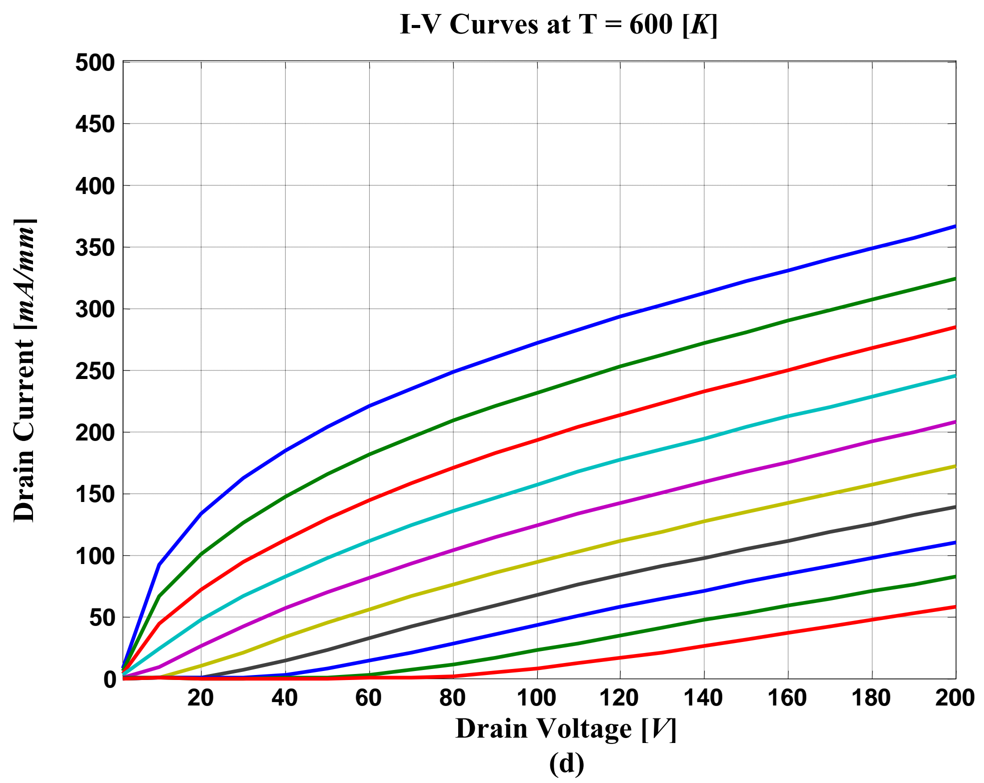
Figure 5.6 I-V Curves at (a) T=300*K*, (b) T=400*K*, (c) T=500*K*, (d) T=600*K*, (e) T=700*K*, (f) T=800*K*, respectively. The ten curves in each figures correspond to V_g=0*V*, -2*V*, -4*V*, -6*V*, -8*V*, -10*V*, -12*V*, -14*V*, -16*V*, -18*V*, from the top to the bottom.



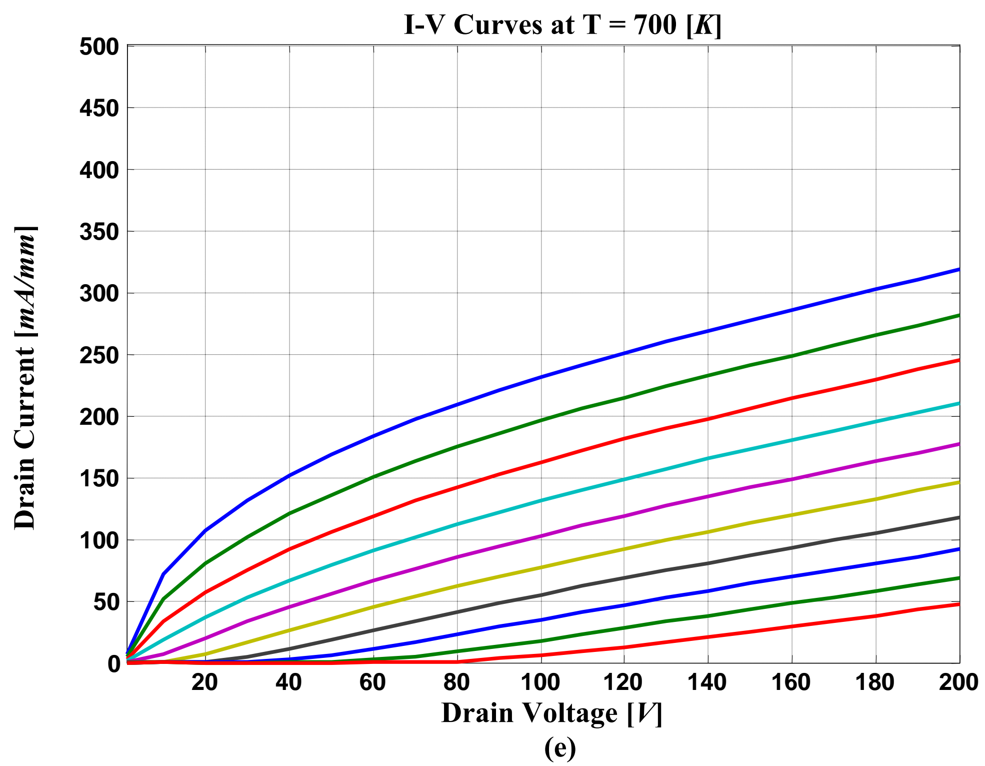
(b)



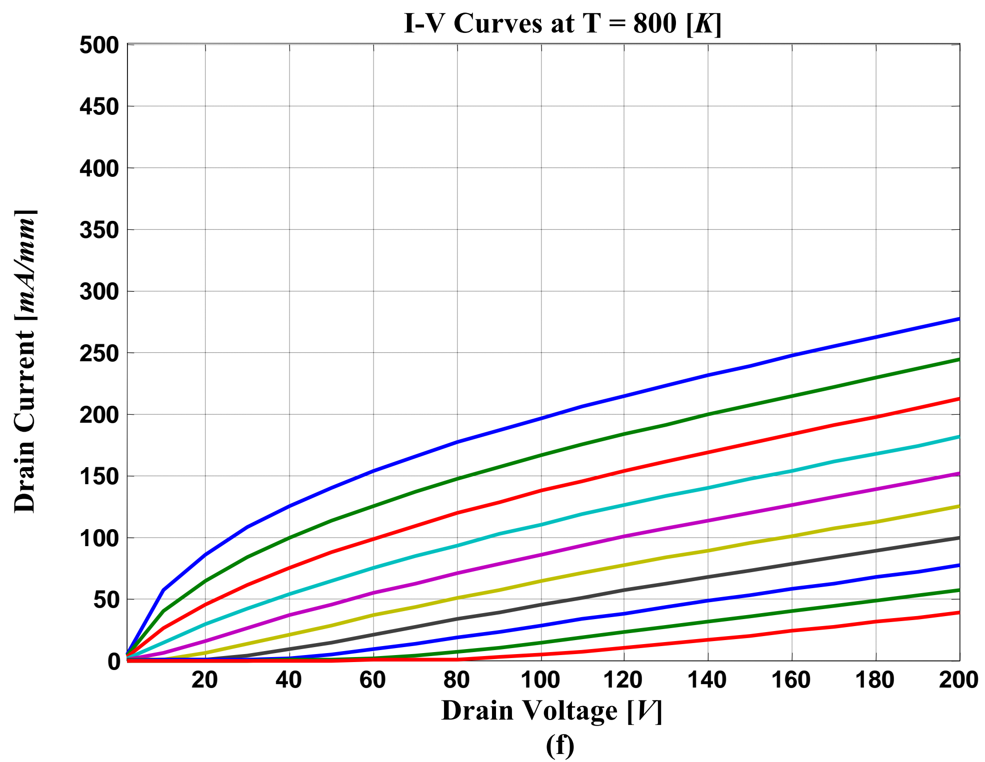
(c)



(d)



(e)



(f)

The Fig. 5.7 show the I-V curves from 300K to 800K with mesa width 0.6 *μm,* gate length 0.1 *μm*, doping $5{\cdot}10^{16}$ cm^{-3}, V_g= -8 *V*, and -10 *V*. As the operating temperature increases, the drain current I_{ds} decrease monotonically for V_g = -8 *V,* -10 *V*. At 800K, V_g = -8 *V,* the saturation current is almost 56% of the 300*K*. At 800K, V_g = -10 *V,* the saturation current is almost 55% of the 300*K*. The drain current I_{ds} decrease rate is a different between V_g = -8 *V* and V_g = -10 *V*. The gate voltage is electrons barrier, therefore, the high barrier induce that much more donors are ionized.

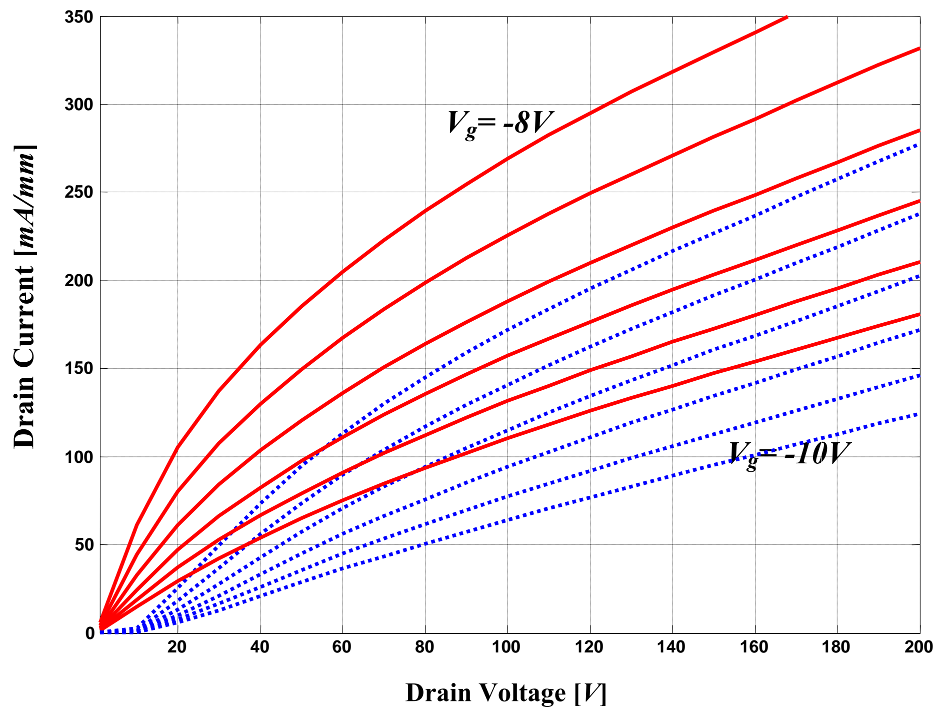


Figure 5.7 I-V Curves at T=300*K*, 400*K*, 500*K*, 600*K*, 700*K*, 800*K* for V_g = -8*V*, -10*V*, from the top to the bottom, respectively.

The maximum current is shown in Fig. 5.8. As temperature increase, the maximum current decreases. The decrease rate is different between a small mesa width and large mesa width. It can be explained that more donors are ionized.

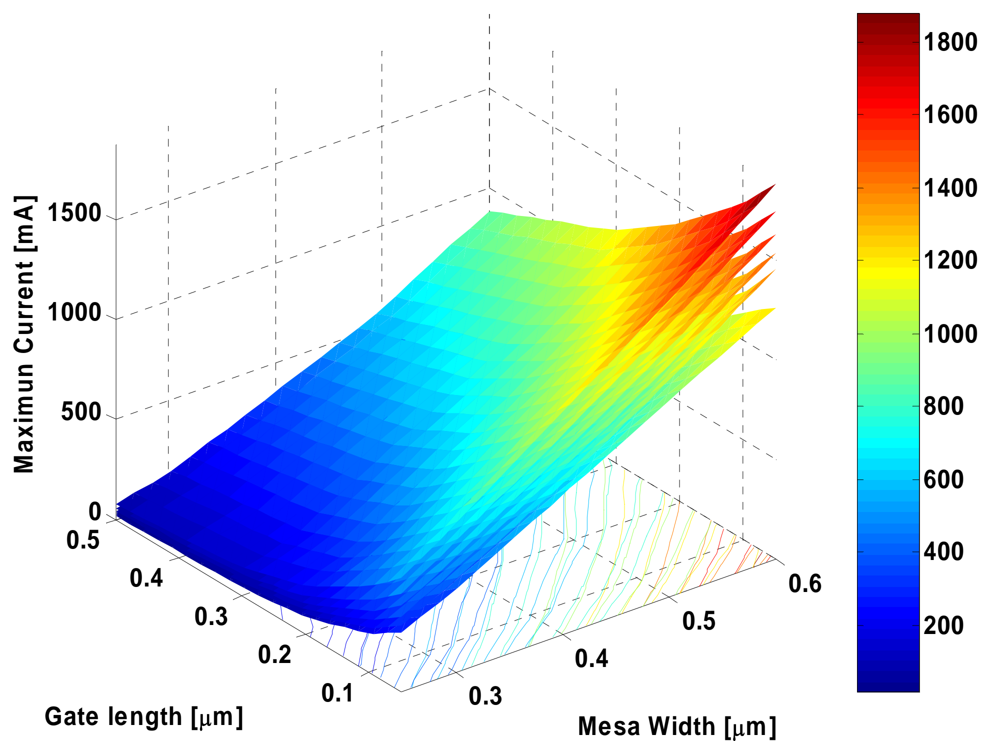


Figure 5.8 Maximum Current at T=300*K*, 400*K*, 500*K*, 600*K*, 700*K*, 800*K* for $2{\cdot}10^{17}$ *cm*$^{-3}$, from top to bottom, respectively.

4 Temperature Dependent Frequency performances

Since the system input and output impedance are variables, we are interested in the maximum frequency that the device can operate. The definition of this maximum frequency becomes ambiguous. There are two standard measures of this maximum frequency. These are f_T and f_{max}. The f_T, or frequency bandwidth, is the frequency that the transistor has unity current gain while driving a short circuit load. This is equal to the h_{21}=1 frequency. The f_{max} is the maximum frequency of oscillation. In order to have oscillation, the gain of the device must be equal to, or above unity. Therefore the f_{max} is the highest frequency that unity gain can be obtained for any load condition. This is obtained under the maximum available gain condition; (G_{max}) which occur when the device is conjugate matched.

Y or *S*-parameters can be extracted from MEDICI simulation and h_{21}, G_{max} can be obtained by calculation. The h_{21} can be calculated by

$$h_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{21}S_{12}} = \frac{Y_{21}}{Y_{11}} \tag{5-6}$$

The maximum available power gain can also be calculated from the *Y* or *S*-parameters.

$$\mathrm{G}_{\max} = \left|\frac{S_{21}}{S_{12}}\right|(K-\sqrt{K^2-1}) \tag{5-7}$$

Where, K is the stability factor which is given by

$$K = \frac{1+|S_{11}S_{21}-S_{12}S_{21}|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{12}||S_{21}|} \tag{5-8}$$

The stability factor will predict the stability of the device against oscillation. For a *K* greater than unity and positive, the device will be unconditionally stable for any

impedance presented to it. Oscillations are possible whenever the $|S_{11}|$ or $|S_{22}|$ greater than unity. The device is unconditionally stable if the input and output impedances are greater than zero for any source or load impedance presented. The calculation of G_{max} is only valid when the device is unconditionally stable. From Eqn. (5-6) the gain bandwidth f_T can be calculated directly from the simulated Y-parameters. Fig. 5.9 shows the h_{21} versus frequency. The extrapolated intercept of h_{21} = unity (0 dB) can be found f_T. For this SIT, 0.5 μm mesa width and gate length 0.3 μm with V_g = -4 V, V_d = 50 V, f_T is 9.6 GHz at 600 [K].

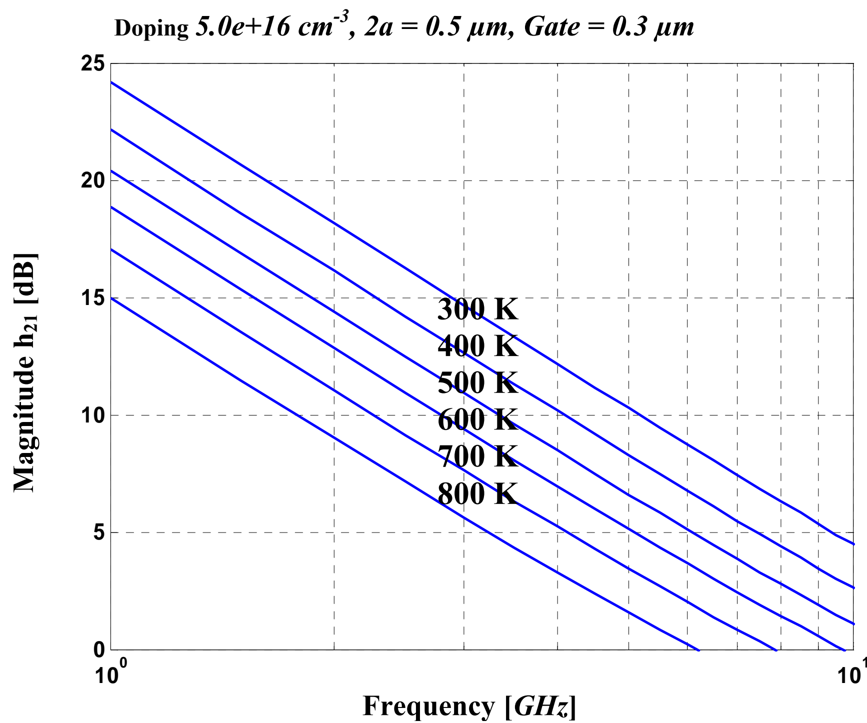


Figure 5.9 h_{21} parameter from simulated Y-parameter showing the bandwidth-gain product (f_T) of 9.6 *GHz* at 600 [*K*]. Bias point is V_d = 50 *V*, V_g = -4 *V*.

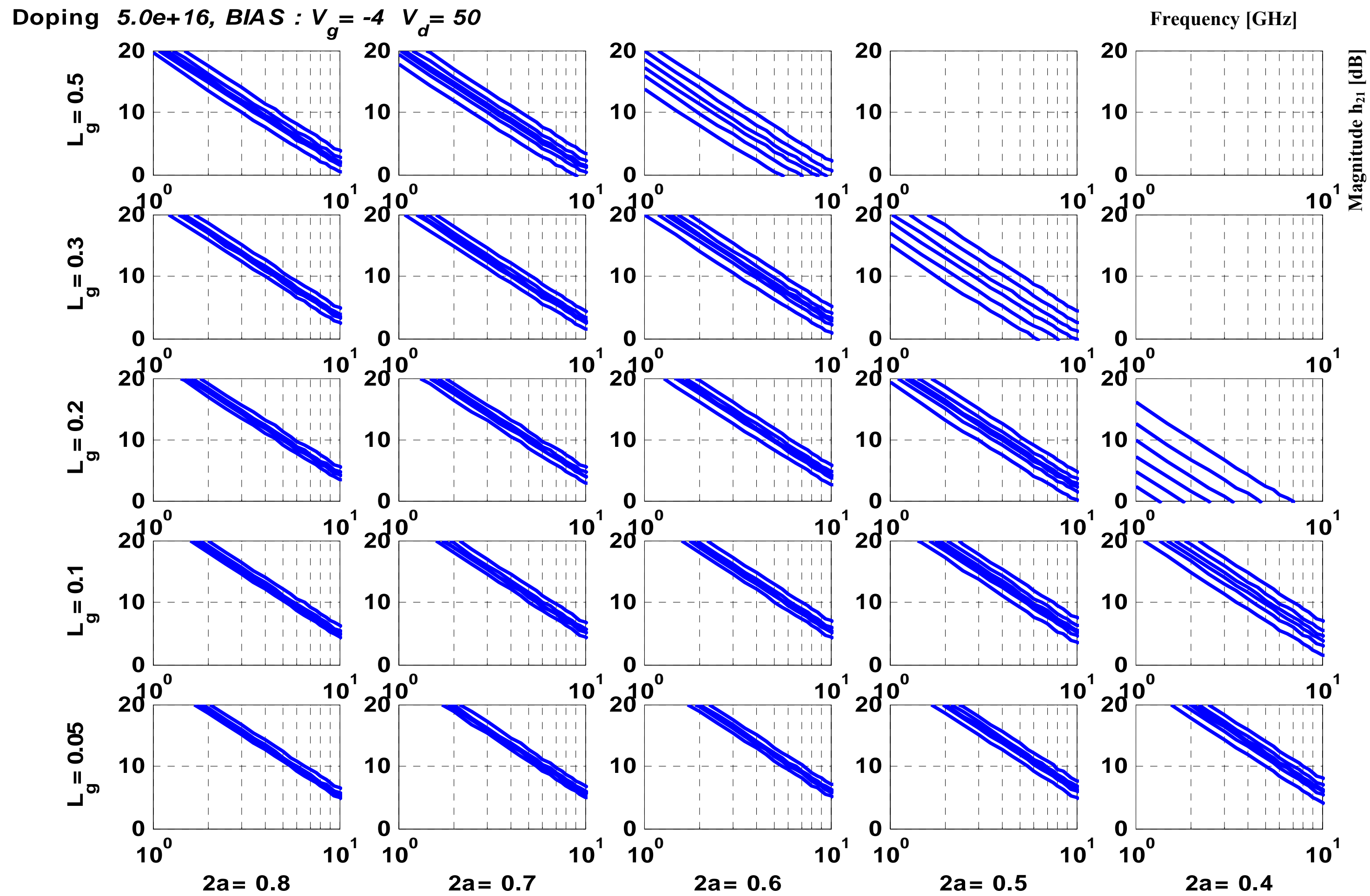


Figure 5.10 h_{21} **parameter from simulated Y-parameter with bais point is** $V_d = 50\ V$, $V_g = -4\ V$, **Doping** $5.0e+16\ cm^{-3}$, **from top to bottom, 300, 400 500, 600, 700, 800 [K], respectively.**

In the Fig.5.10, the cut-off frequency is obtained by the magnitude of h_{21} and its trends along with a increased mesa width and gate length, where, as gate length increase or mesa width decrease, cut-off frequency decrease. Also, as temperature increase, cut-off frequency decrease. The more mesa width is a wide, the more cut-off frequency decrease rate is a small. We will see in next figures, too.

Additionally, from the Y-parameters obtained by MEDICI simulations, the data can be converted into S-parameters, and using information from Eqn. (4-9) through (4-12), the circuit model capacitance can be determined. Also, we can obtain cut-off frequency from the capacitance.

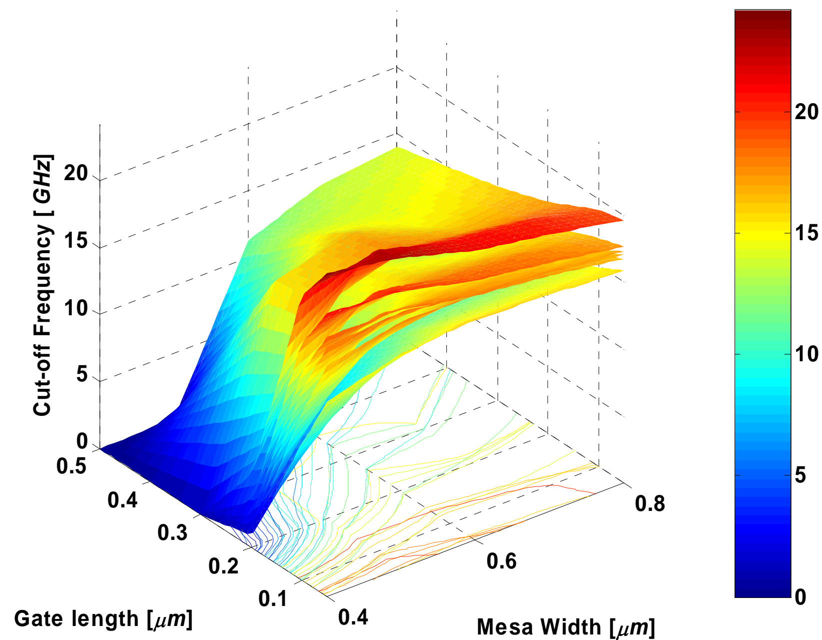


Figure 5.11 Cut-off frequency as a function of gate length and mesa width for a bias point of V_d = 50 V, V_g = -4 V, Doping $5.0e+16$ cm^{-3}, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively.

In Fig. 5.11, Cut-off frequency as a function of gate length and mesa width with a bias point $V_d = 50$ V, $V_g = -4$ V, Doping $5.0e+16$ cm^{-3}, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K]. We can see that the maximum cut-off frequency can obtain in the smallest mesa width and gate length. And as temperature increase, cut-off frequency decrease. Transconductance is shown in Fig. 5.12. The transconductance is maximum value in the smallest mesa width and gate length.

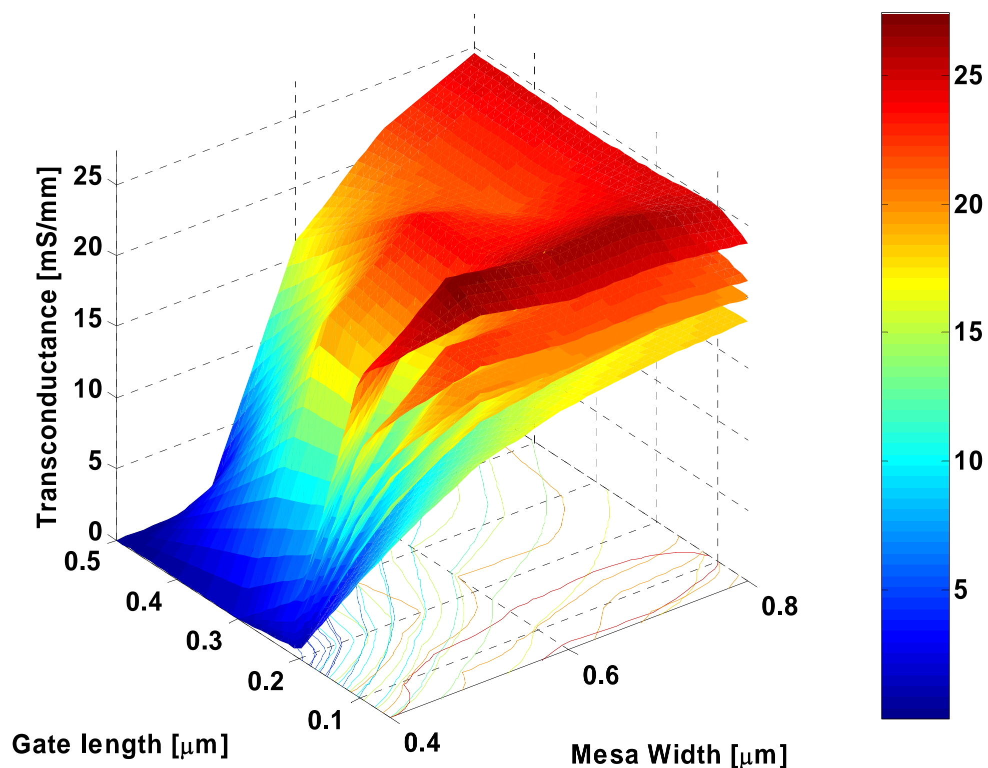


Figure 5.12 Transconductance plotted as a function of gate length and mesa width for a bias point of $V_d = 50$ V, $V_g = -4$ V, Doping value $5.0e+16$ cm^{-3}, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively.

In the narrow mesa width, transconductance is almost proportional to gate length, but, in the wide mesa width, the gate length doesn't affect to transconductance. It is that the increased enough channel. The Gate-source capacitance is shown Fig. 5.13. As temperature increases, gate-source capacitance decreases. On the other hand, gate-drain capacitance increases. It is shown in Fig. 5.14.

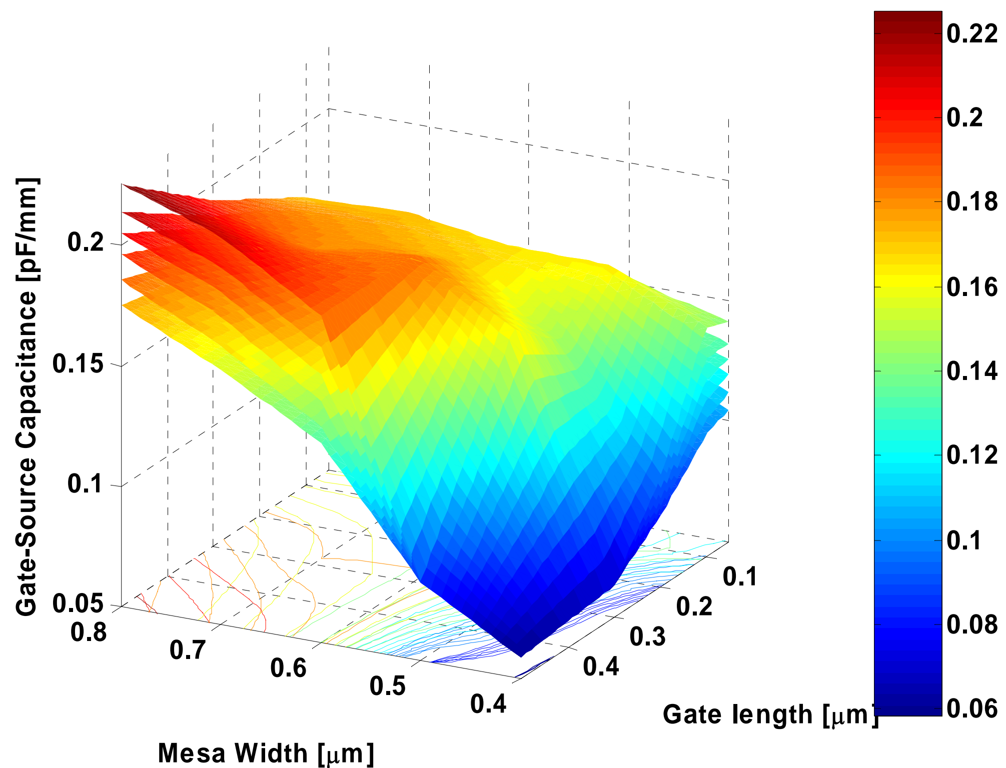


Figure 5.13 Gate-Source capacitance plotted as a function of gate length and mesa width for a bias point of V_d = 50 V, V_g = -4 V, Doping value $5.0e{+}16\ cm^{-3}$, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively.

The gate-drain capacitance is proportional to mesa width and gate length. It increases with gate-length and mesa width in a nearly linear fashion. Typically, cut-off frequency or bandwidth frequency is the frequency that the transistor has unity current gain while driving a short circuit load. But we simulated for research with the several bias points.

Fig. 5.15 shows the cut-off frequency as a function of gate length and mesa width for a bias point of $V_d = 25\ V$, $V_g = 0\ V$, Doping value $5.0e{+}16\ cm^{-3}$, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively.

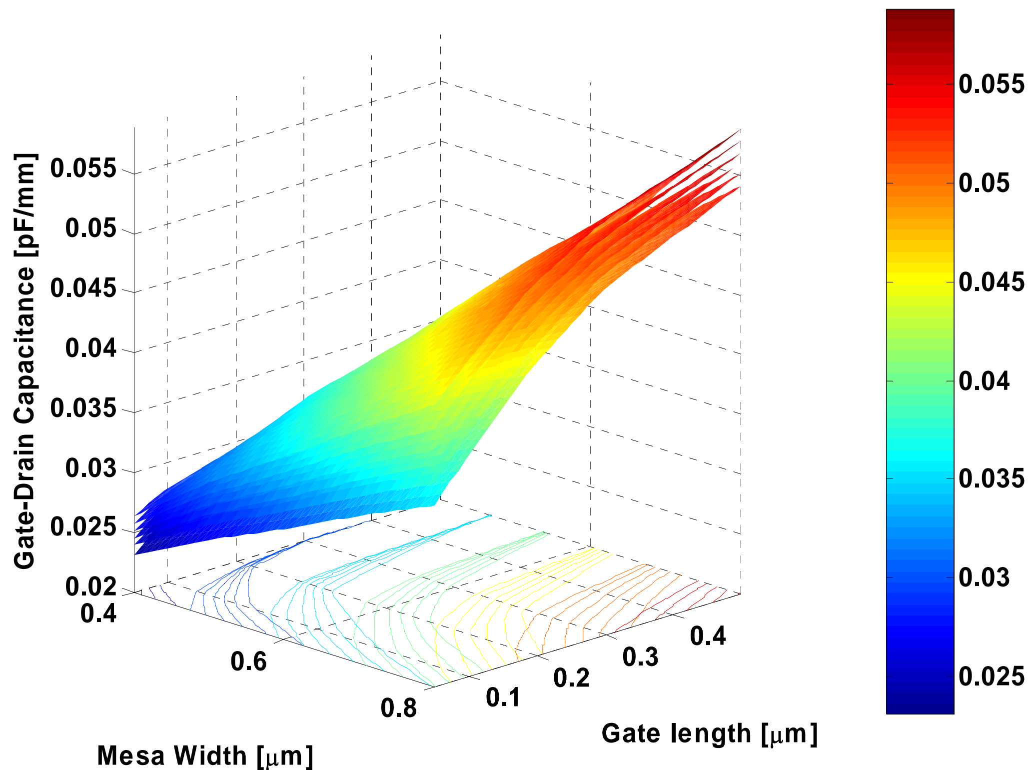


Figure 5.14 Gate-Drain capacitance as a function of gate length and mesa width for a bias point of $V_d = 50\ V$, $V_g = -4\ V$, Doping value $5.0e{+}16\ cm^{-3}$, from top to bottom, 800, 700, 600, 500, 400, 300 [K], respectively.

In the Fig 5.15, cut-off frequency is inversely proportional to gate length. As temperature increase, cut-off frequency decrease. It is like almost linear fashion. In the Fig. 5.11, we can see the pinch-off regions that it is a dark blue and bottom space. But in this Fig. 5.15, there is no it. It is that gate voltage. In I-V curves described previous chapter, there is no pinch-off with V_g=0 V in all the mesa width and gate length ranges.

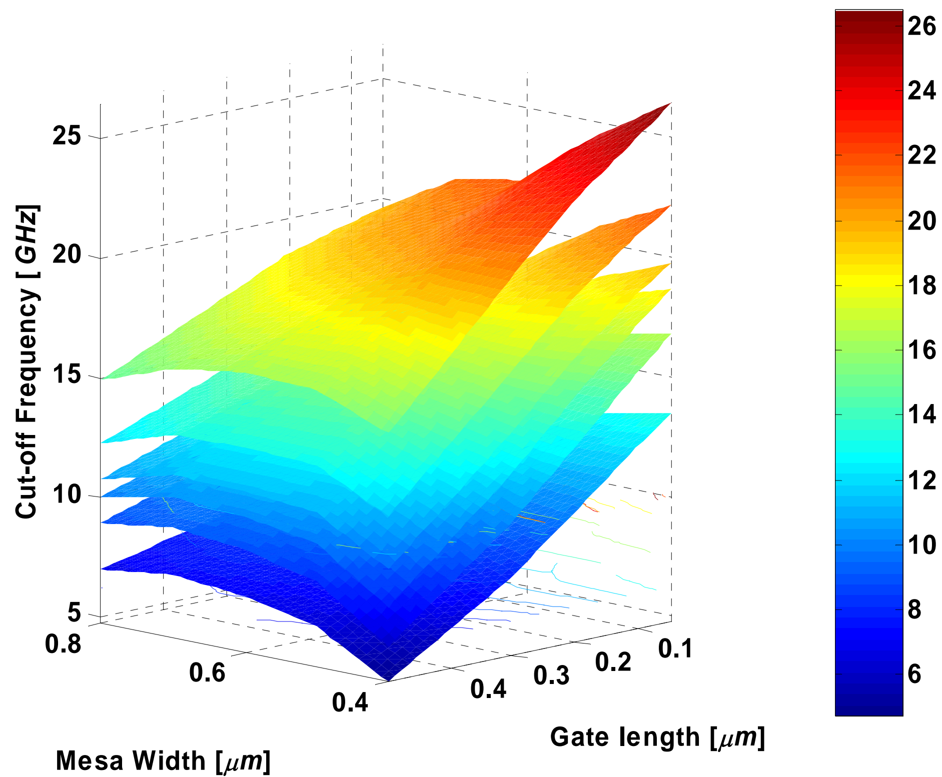


Figure 5.15 Cut-off frequency plotted as a function of gate length and mesa width for a bias point of V_d = 25 V, V_g = 0 V, Doping value $5.0e+16\ cm^{-3}$, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively.

In the Fig. 5.16, the transconductance is shown as a function of gate length and mesa width with bias point of $V_d = 25\ V,\ V_g = 0\ V$, Doping value $5.0e{+}16\ cm^{-3}$, for temperature increase. As temperature increase, transconductance decrease. The transconductance is inversely proportional to gate length in the high temperature. It can be explained to effect of the depletion region increased by temperature. The drift region is decreased by a increased depletion region in the channel. Therefore, the transconductance is decreased.

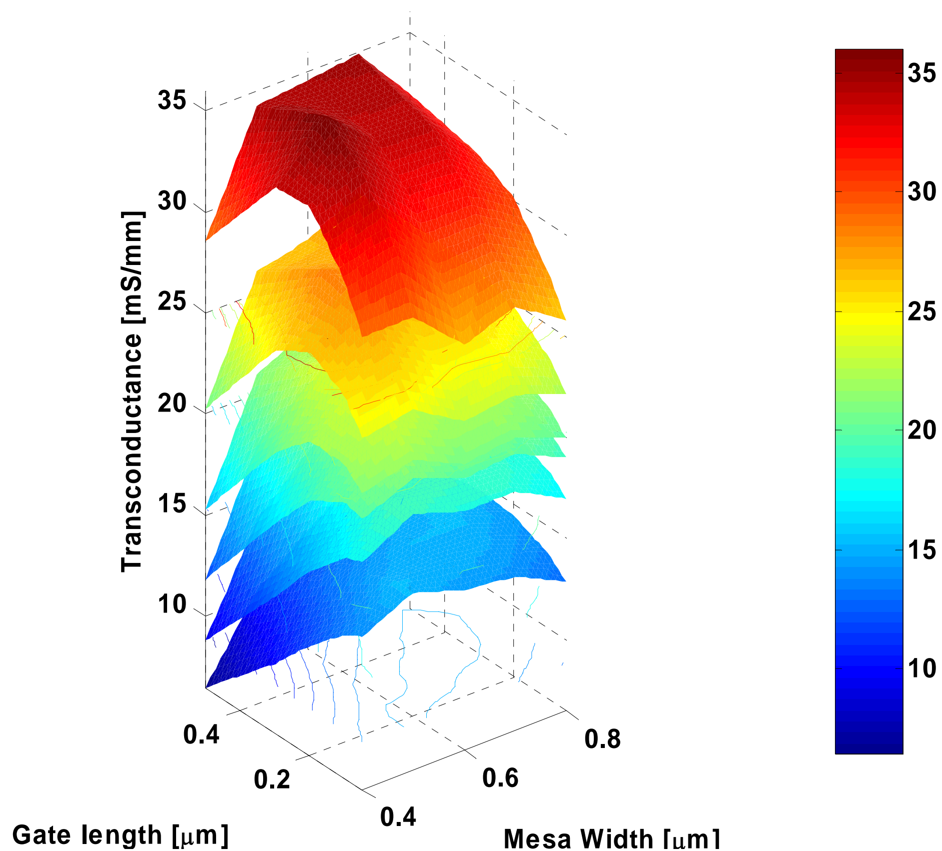


Figure 5.16 Transconductance plotted as a function of gate length and mesa width for a bias point of $V_d = 25\ V,\ V_g = 0\ V$, Doping value $5.0e{+}16\ cm^{-3}$, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively.

In the Fig. 5.17, the gate-source capacitance is shown as a function of gate length and mesa width with a bias point of $V_d = 25\ V,\ V_g = 0\ V$, Doping $5.0e+16\ cm^{-3}$. As temperature increase, the gate-source becomes a stronger function of gate length. The effect of temperature is deceased in a short gate length. It can be explained to effect of the depletion region increased by temperature, too.

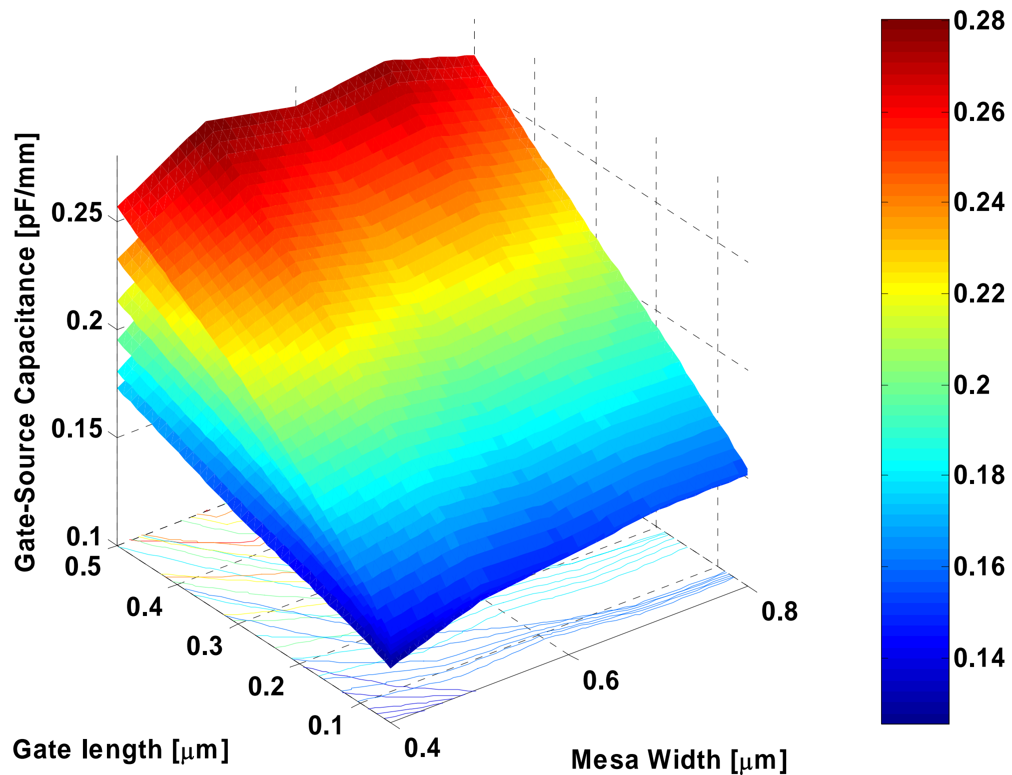


Figure 5.17 Gate-Source capacitance plotted as a function of gate length and mesa width for a bias point of $V_d = 25\ V,\ V_g = 0\ V$, Doping value $5.0e+16\ cm^{-3}$, from top to bottom curves, 300, 400, 500, 600, 700, 800 [K], respectively.

The gate-drain capacitance is shown as a function of gate length and mesa width with a bias point of $V_d = 25\ V,\ V_g = 0\ V$, Doping value $5.0e+16\ cm^{-3}$ in the Fig. 5.18. Where, as temperature increases, gate-drain capacitance increases. It is proportional to mesa width, an increased temperature and gate length.

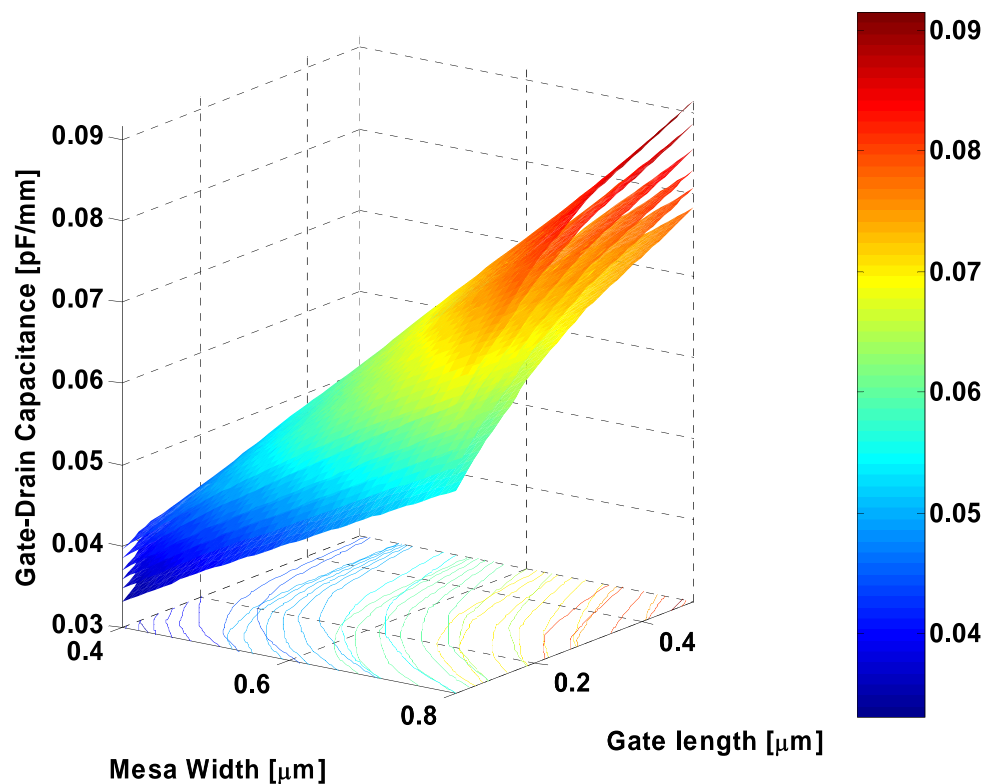


Figure 5.18 Gate-Drain capacitance plotted as a function of gate length and mesa width for a bias point of $V_d = 25\ V,\ V_g = 0\ V$, Doping value $5.0e+16\ cm^{-3}$, from top to bottom curves, 800, 700, 600, 500, 400, 300 [K], respectively.

In above results, as temperature increase, cut-off frequency f_T and transconductance g_m are decreased. At 800 K, g_m is about 20% of it at 300 K. The

monotonic decrease of transconductance is due to the decrease of the saturation current which is mainly a result of mobility degradation. At 800 K with doping *2.0e+17* cm^{-3}, f_T is about 13 *GHz* which is about 20% of it at 300 K. Thus, f_T and g_m decrease to almost same rate.

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CHAPTER VI

CONCLUSION AND FUTURE WORK

1 Conclusion

The superior physical properties of SiC, such as wide band gap, high saturation electron velocity, low impact ionization rates, and high thermal conductivity, provide very promising candidates for high temperature, high power, high frequency, and radiation resistant applications. The high blocking voltage, the low harmonics and the low internal modulation distortion (IMD) are the excellent features of SIT compared to those of BJT and FET. The current-voltage (I-V) transfer function (I_b to I_c) of BJT is the exponential, and the square law (V_g to I_d) of the conventional FET. In contrast to those of the BJT and FET, the low distortion amplifier was reported by virtue of its linear V_g-I_d characteristics of SIT. In this works, the static induction transistor (SIT) in SiC was investigated as a possible microwave device for high breakdown voltage and large bandwidth of operation. A large number of device structures were considered by means of simulations. Its properties of each parameter described as results of simulation.

It has been demonstrated that 4H-SiC SIT is capable of operating at high current and high voltage. For a doping $5 \cdot 10^{15}$cm^{-3} 4H-SiC SIT, the room temperature Avalanche breakdown voltage is as high as 668 V, and for a doping $2 \cdot 10^{17}$cm^{-3}

4H-SiC SIT, the room temperature maximum current is 1860 *mA*. Therefore, 4H-SiC SIT is a very attractive candidate for high voltage and high power applications.

In the frequency property simulations under small-signal condition, for a doping a doping $2 \cdot 10^{17}$cm^{-3}, mesa width 0.3 *μm*, gate length 0.05 *μm* 4H-SiC SIT, the cut-off frequency f_T is as high as 42 *GHz*. As operating temperature increases, cut-off frequency f_T degrades gracefully. However, even at such a high temperature ad 800 K the cut-off frequency is still as high as 18 *GHz*. On the other hand, at this temperature, both Si and GaAs devices are no longer working at all. Therefore, 4H-SiC SIT is a very promising device high temperature.

The key design parameters are the mesa width $2a$ and the gate length L_g when the channel doping is fixed. The simulated I-V curves are presented that allows one to find the appropriate combination of $2a$ and L_g while maintaining adequate blocking gain. It is also shown that short gate lengths are needed for a high cut-off frequency and that a trade-off exists between frequency performance and current density. Therefore, in this works, all curves extended to function of mesa width and gate length.

The main approach to get higher cut-off frequency is to increase the doping in channel, and adjust the mesa width and gate length accordingly. Also, trench width is made very narrow. For the highest doping values ($2 \cdot 10^{17} cm^{-3}$) and smallest trench width considered, a cut-off frequency of up to 42 *GHz* simulated in this works.

Actually, the high cut-off frequency devices do not reach theoretical best performance because of the source contact resistivity and the shrink source contact area with reduced mesa width. Contacts better than $1 \cdot 10^{-5}\ \Omega cm^2$ are needed to reduce the effect of the source resistance. The large gate-drain and gate-source capacitance of

the SIT affects not only the cut-off frequency but maximum current. The contact resistivity is very important in high performance device design. The input capacitance under realistic operating conditions is further increases due to the Miller effect. Therefore, in this works, it has been demonstrated that the effect of contact resistivity is simulated in detail.

The equivalent circuit was extracted from simulated Y-parameter as a function of bias, and it can expand to large signal equivalent circuit. This circuit model was imported into a circuit simulation program to simulate load-pull results, and can also be used for circuit design.

The drain-gate breakdown voltage is limited by breakdown at the edge of the gate metal, unless an edge termination is employed. The edge termination of the gate seems to be of limited use because the drain-gate breakdown merely shifts to the inner trench corners, and the ultimate breakdown voltage is only slightly higher than in the unterminated device. However, it is still useful to terminate the gate edge, because the added processing is minimal and easy to perform. In this works, the effect of breakdown voltage and temperature is shown in the last chapter.

The material parameters of SiC are not known well enough. The material parameters may even vary from lot to lot or vendor to vendor. Therefore, the SiC device simulation is not easy.

The two key advantages of the SIT are the high frequency and the high power density per area. But it is difficult to achieve both of these advantages in a same SIT, because a large mesa width for high power diminishes an advantage of a high frequency. A high doping for high frequency diminishes an advantage of a high power. Therefore, it is that a trade-off exists between high power and high frequency.

2. Future Works

The neural networks have recently been introduced to the microwave area as a fast and flexible vehicle to microwave modeling, simulation and optimization. Also, in recent years, a new CAD approach based on neural network models has been introduced for microwave device design. It has been applied to the efficient modeling of devices, circuit and device optimization.

Even if today's simulators are powerful tools, they can only be as accurate as the mathematical models that are used. As a consequence constructing good model for device used in circuits and for circuits used in systems is a basic task [4].

There are three main factors that make the SIT devices less attractive in RF mobile applications. First, it is on normally-on characteristics, second, the large on-state voltage drop and, third, the need of using relatively high gate bias voltage [1]. To overcome this problem, neural network can be used. We obtained much SiC SIT data of properties and can be use for training neural network to it.

In neural network, adequate modeling of nonlinear RF devices still remains a complex but an avoidable step toward the achievement of a good design. And simulation system boundary is very flexible.

Reference

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APPENDIX A

Reported gain of SiC SIT's over the past 5 years

A. Reported gain of SiC SIT's over the past 5 years

Gate Structure	Gain	Comments
RG-SB	8.7 dB at 600 MHz	packaged devices (1.5 cm parts with total periphery of 16.5 cm) – max. current, 1A/cm - max. blocking voltage, 200V - 47% PAE, 225W output power, and power density of 13.5 W/cm at 600 MHz – cut-off frequency 4 GHz – common-source mode
RG-SB	9.5 dB at 3 GHz	packaged devices (three unmatched 1 cm devices connected in parallel) – operated at 80V on the drain - 42% PAE, 36 W output power, and 9.5 dB gain at 3 GHz – common-gate mode packaged devices (23 cells connected in parallel with total periphery of 34.5 cm – shown in Fig. 5) – operated at 90V on the drain – power density was 165 kW/in^2 and good linearity observed in class AB operation from output power of 50 to 450 W at 600 MHz – common-source mode
RG-SB	15 dB at 3 GHz	single devices – drain bias of 40V – 80V resulted in 11.5 dB - 15 dB gain at 3 GHz
RG-SB	9.5 dB at 3-4 GHz	packaged devices (airbridged parts with total periphery of 3 cm) - 40% PAE, 38 W of output power, power density of 300 KW/cm^2 and 9.5 dB gain at S-band frequencies (3-4 GHz)– power levels up to 120 W have been observed from these S-band SIT packages
P-SB (pn gate)	9dB at 2 GHz	single device - max. channel current, 700 mA/cm – max. blocking voltage, 250 V
P-SB (pn gate)	7 dB at 1.3 GHz	packaged devices – Class AB operation - 80-90V on the drain - voltage swing of 200V - 52% drain efficiency, 35W of output power, and power density of 15.5 W/cm
RG-SB	7.7 dB at 1.3 GHz	Packaged devices (16 parts with 1.5 cm source periphery) - 55% PAE, power density of 16.7 W/cm and power of 400W
RG-SB	7 dB at 4 GHz	packaged devices (four 1.29 cm airbridged parts) - 30% drain efficiency and 47W of output power at 4 GHz 40% drain efficiency, 78W output power and power density of 15.5W/cm at 2.9 GHz
RG-SB	10 dB at 4 GHz	packaged devices (total periphery of 1 cm – approximately 200 fingers) – measurements taken on wafer at full channel current – drain bias of 40V - 40% drain efficiency and 16W output power at 1.3 GHz – common-gate mode

APPENDIX B

Simulation Results for I-V Characteristics

B. Simulation Results for I-V Characteristics

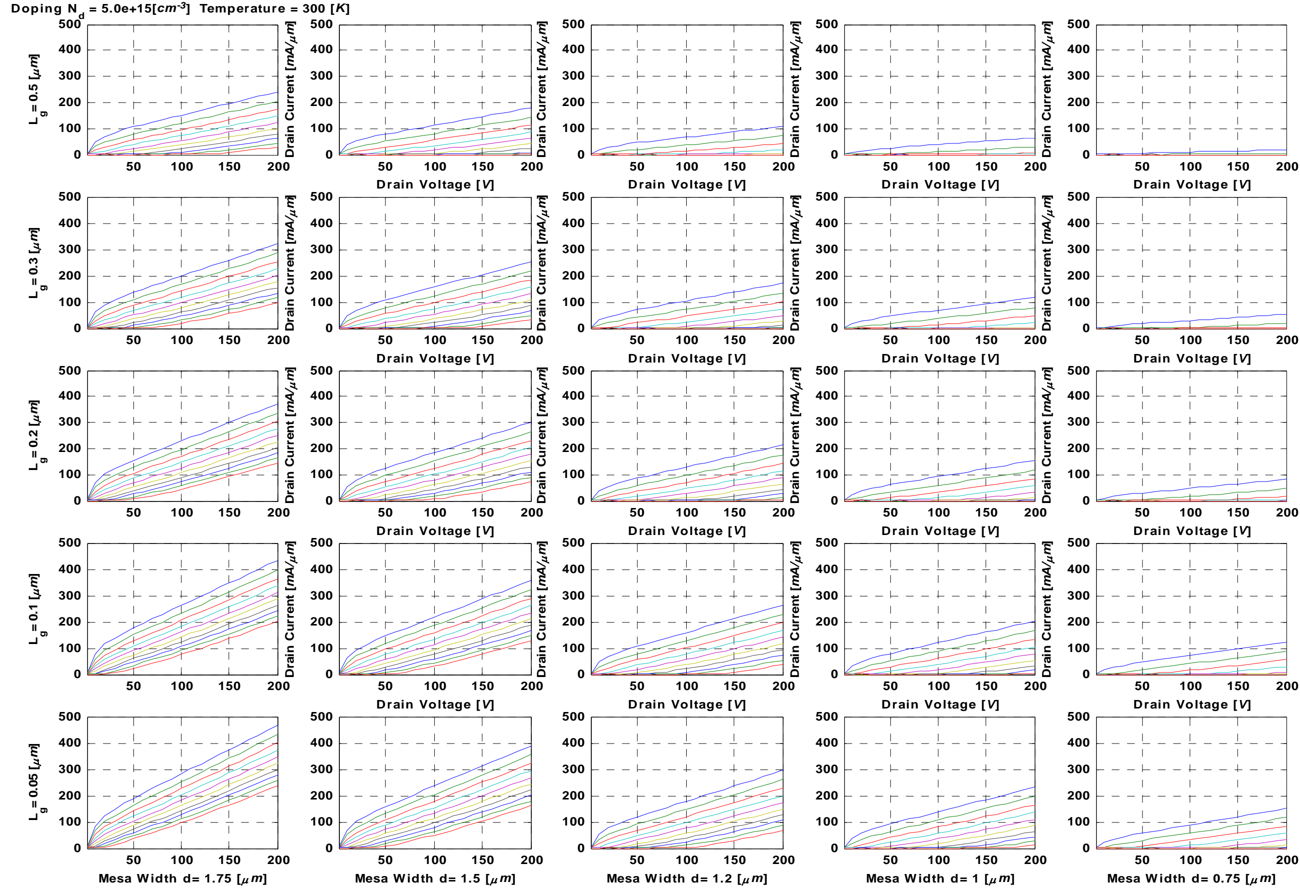

Figure B.1 I-V curves for different values of L_g and $2a$, with $N_D = 5{\cdot}10^{15}$ [cm^{-3}] and 300 [K].

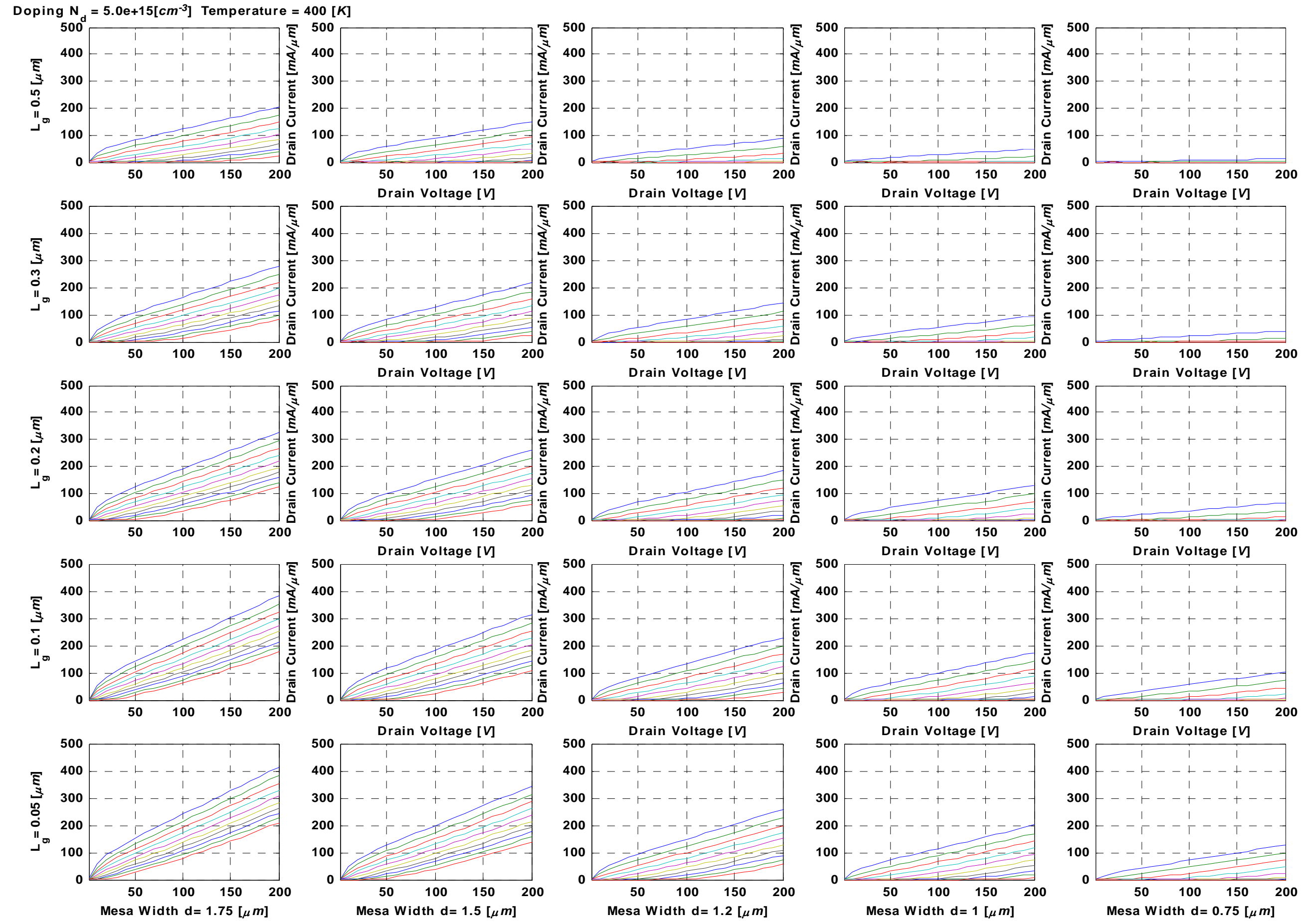

Figure B.2 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{15}$ [cm^{-3}] and 400 [K].

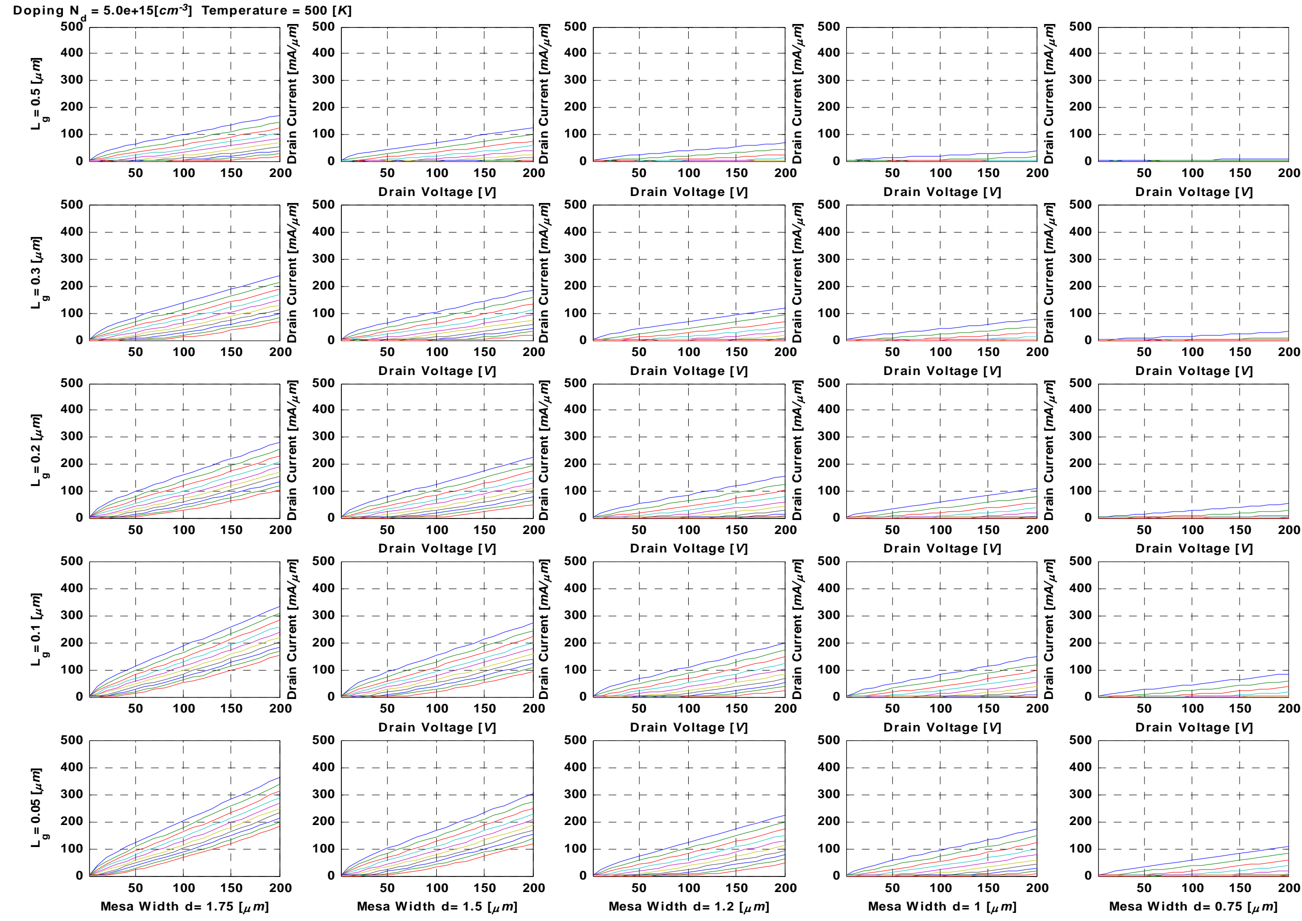

Figure B.3 I-V curves for different values of L_g and $2a$, with $N_D = 5{\cdot}10^{15}$ [cm^{-3}] and 500 [K].

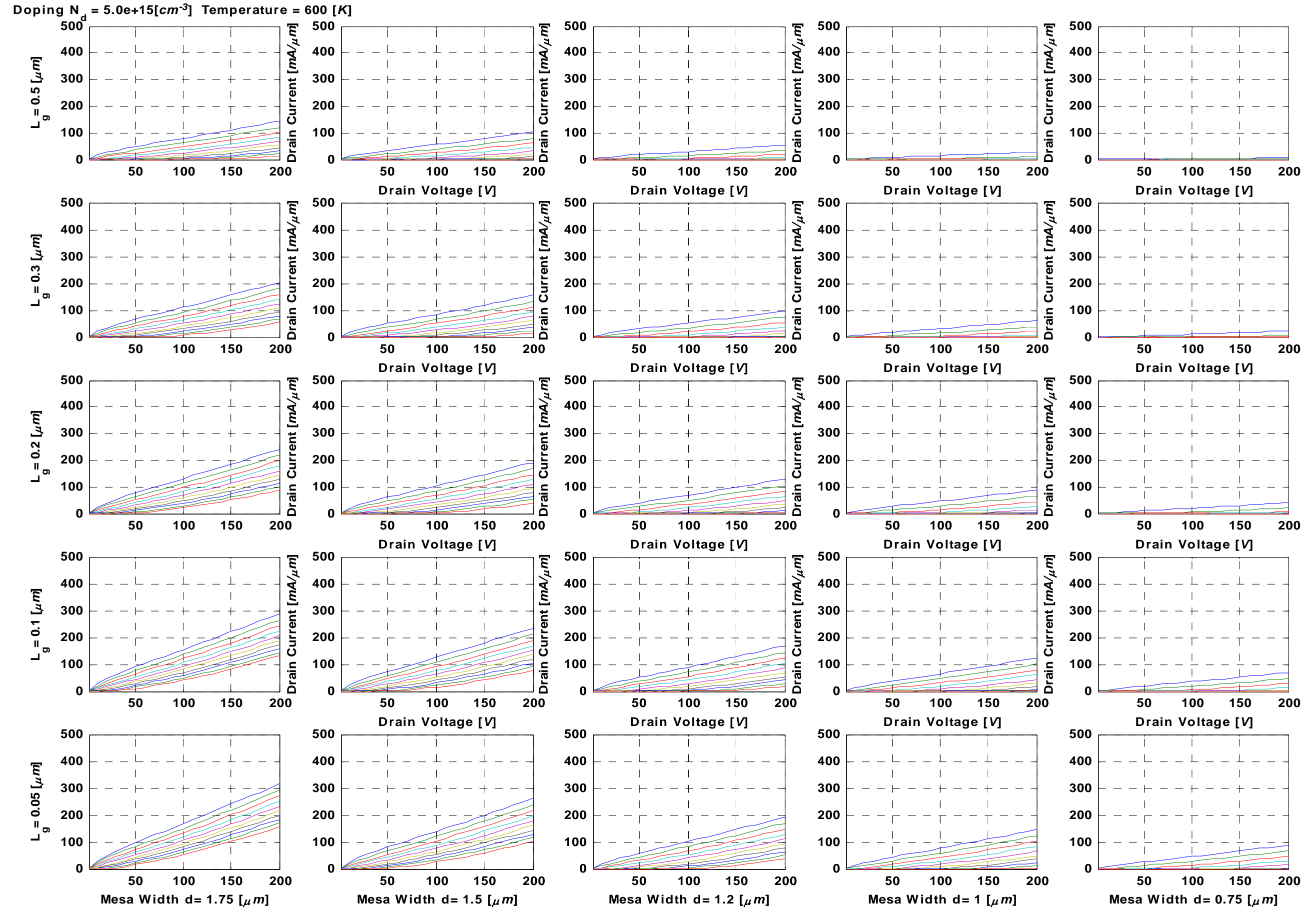

Figure B.4 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{15}$ [cm^{-3}] and 600 [K].

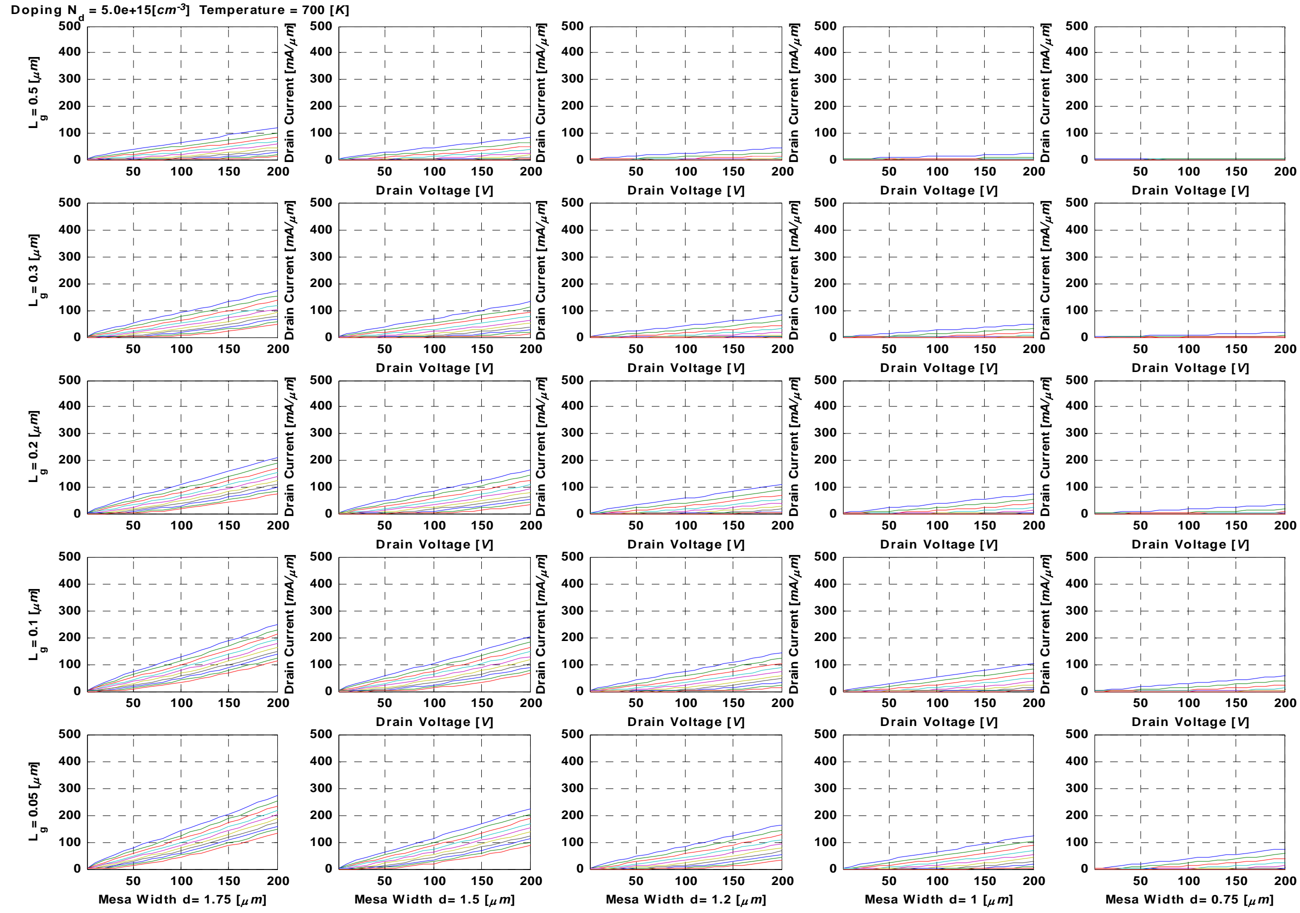

Figure B.5 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{15}$ [cm^{-3}] and 700 [K].

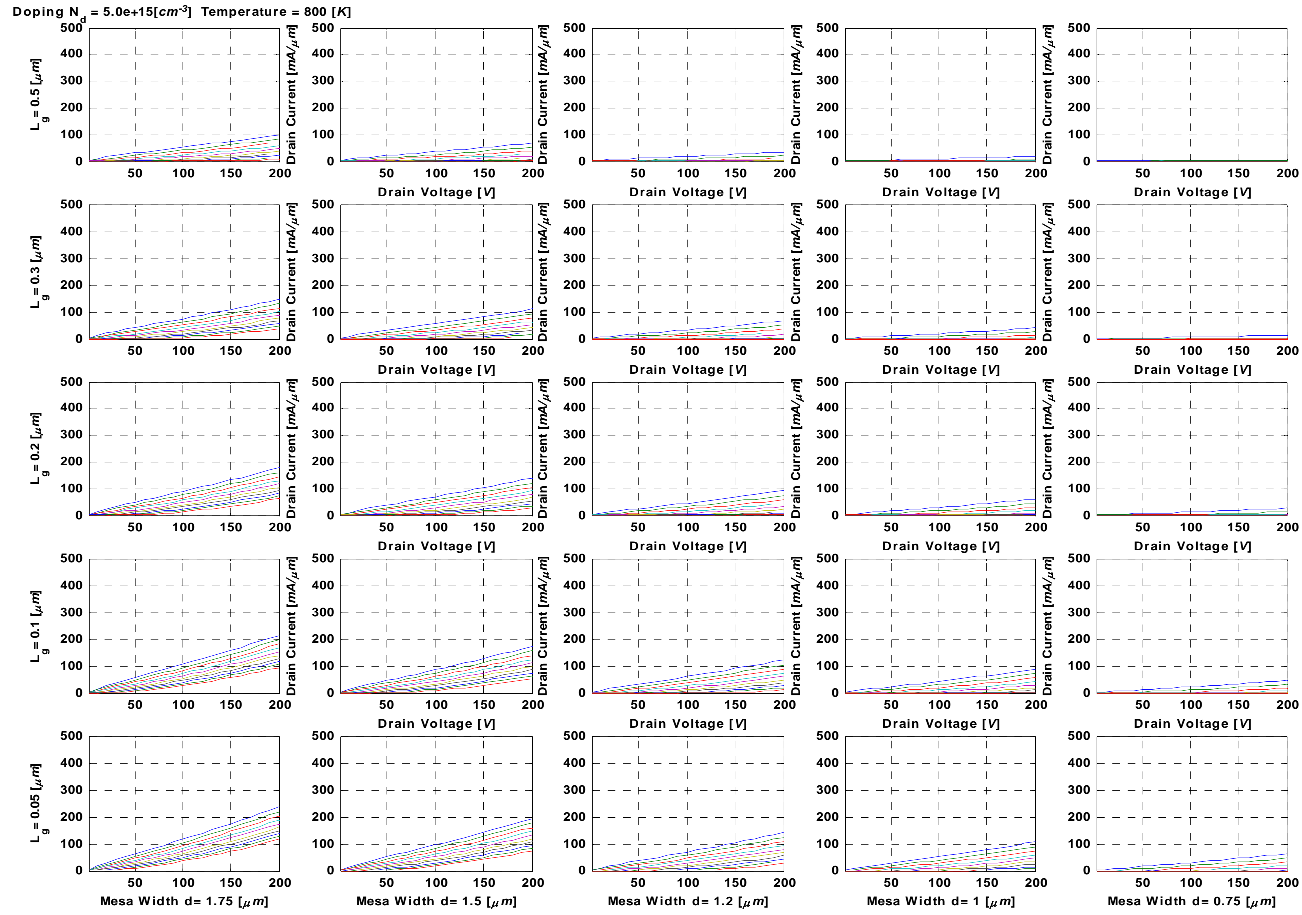

Figure B.6 I-V curves for different values of L_g and $2a$, with $N_D = 5{\cdot}10^{15}$ [cm^{-3}] and 800 [K].

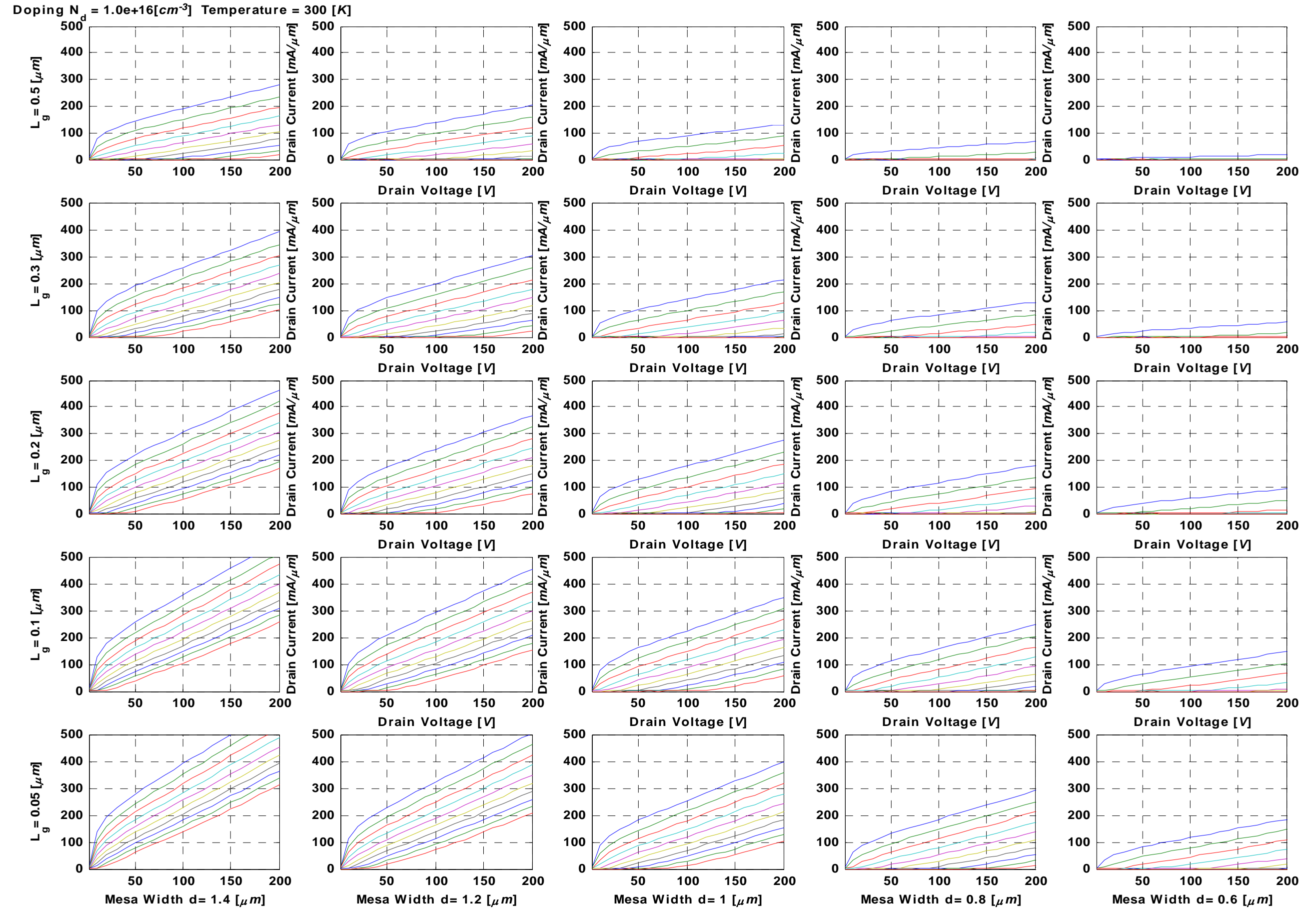

Figure B.7 I-V curves for different values of L_g and $2a$, with $N_D = 1 \cdot 10^{16}$ [cm^{-3}] and 300 [K].

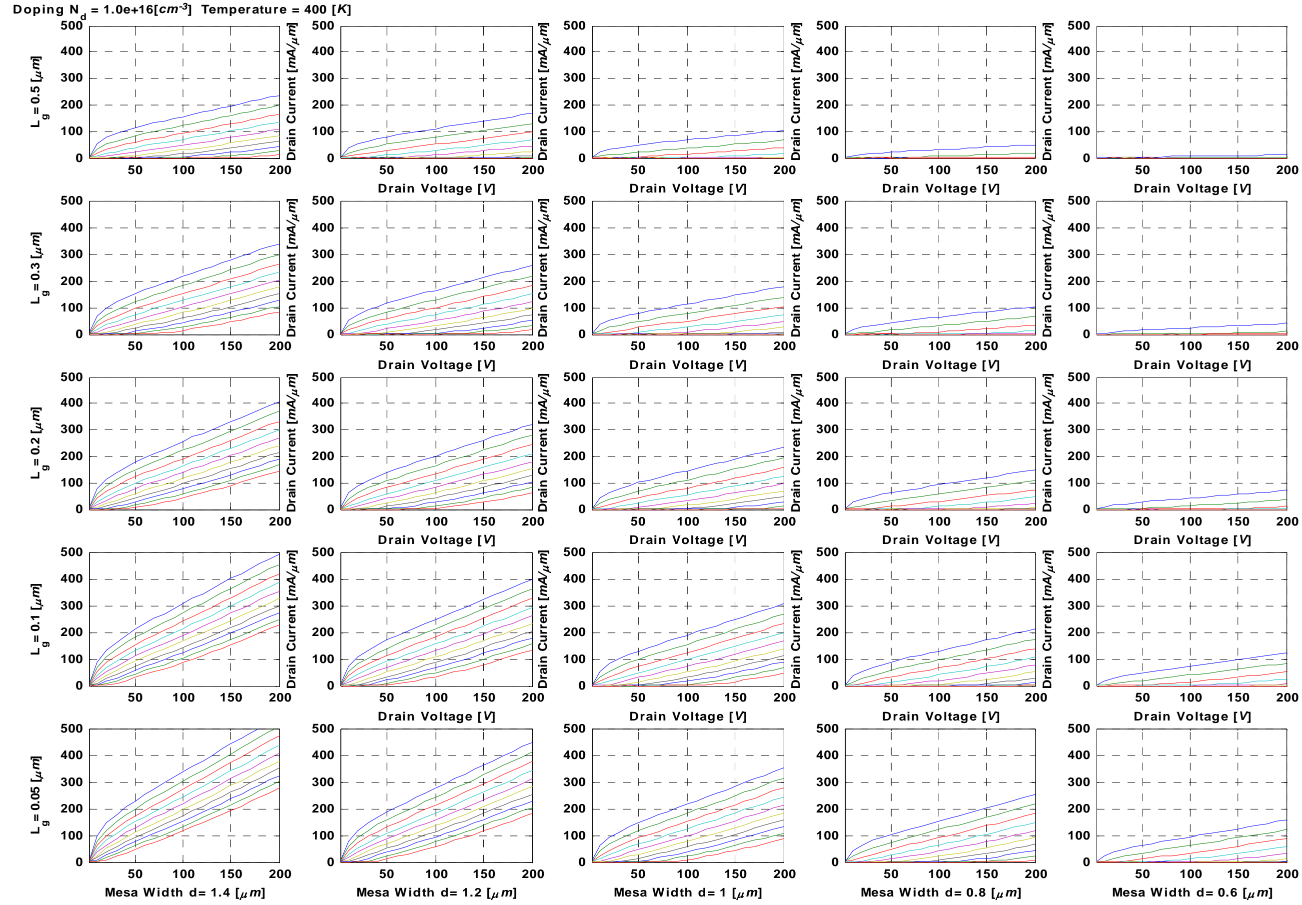

Figure B.8 I-V curves for different values of L_g and $2a$, with $N_D = 1{\cdot}10^{16}$ [cm^{-3}] and 400 [K].

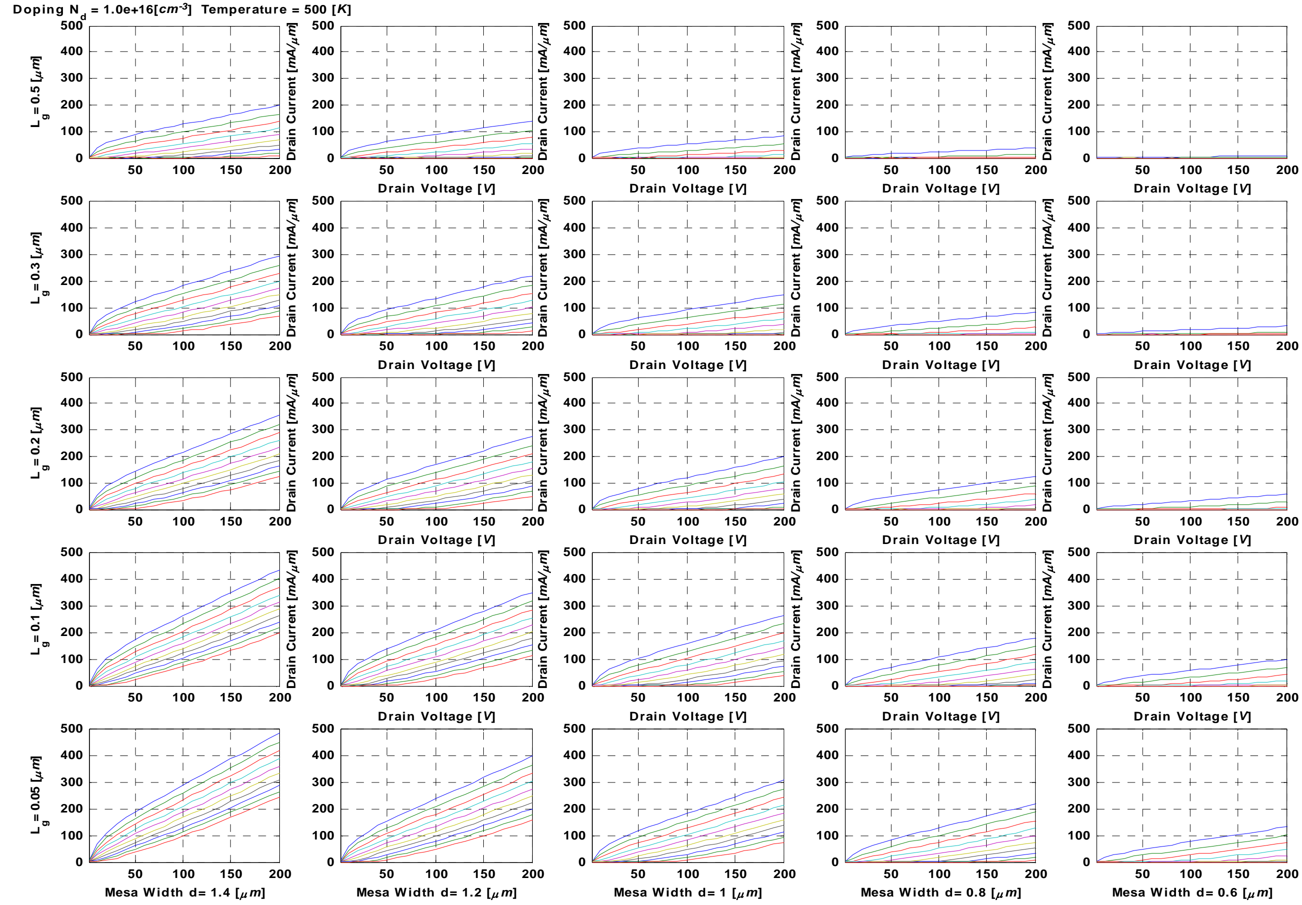

Figure B.9 I-V curves for different values of L_g and $2a$, with $N_D = 1 \cdot 10^{16}$ [cm^{-3}] and 500 [K].

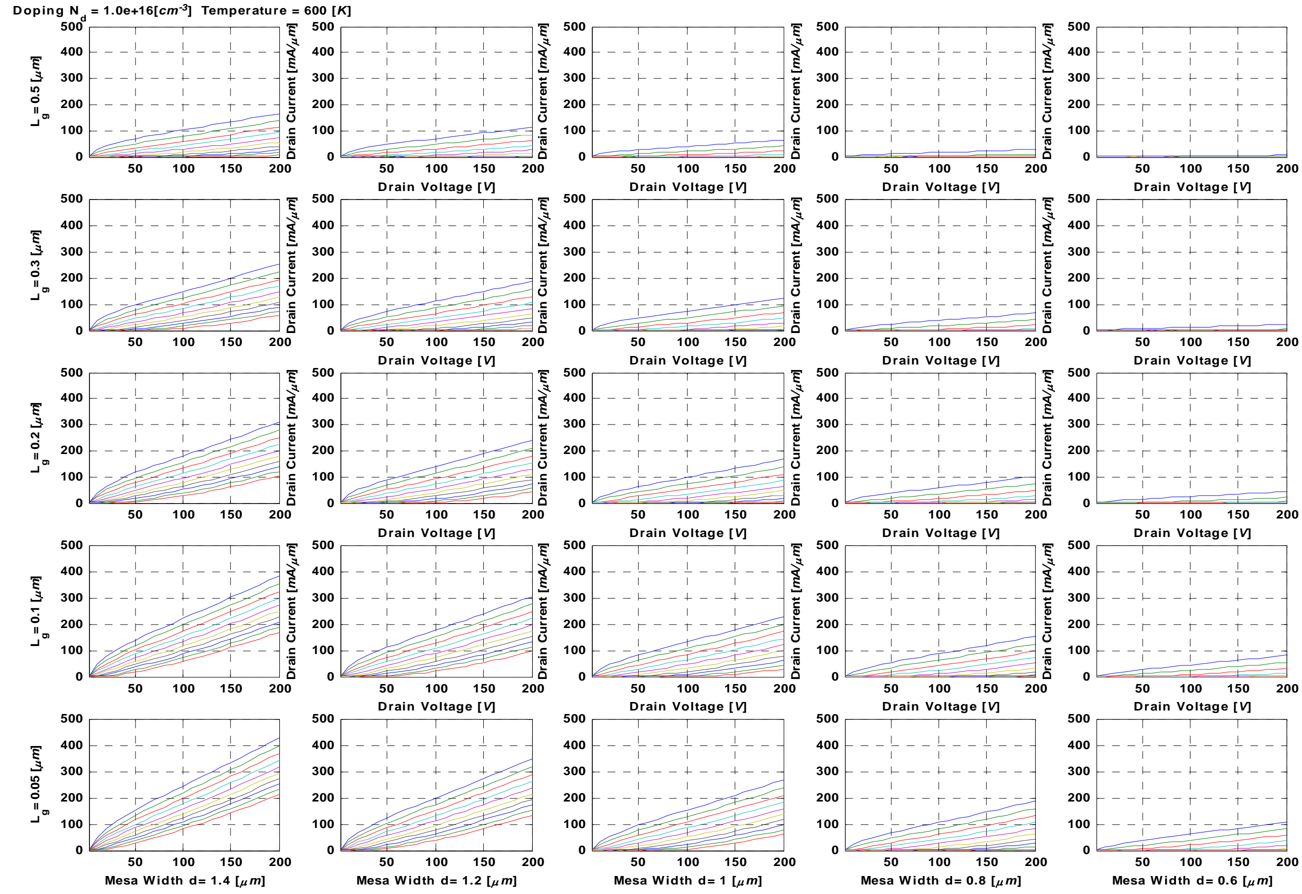

Figure B.10 I-V curves for different values of L_g and $2a$, with $N_D = 1 \cdot 10^{16}$ [cm^{-3}] and 600 [K].

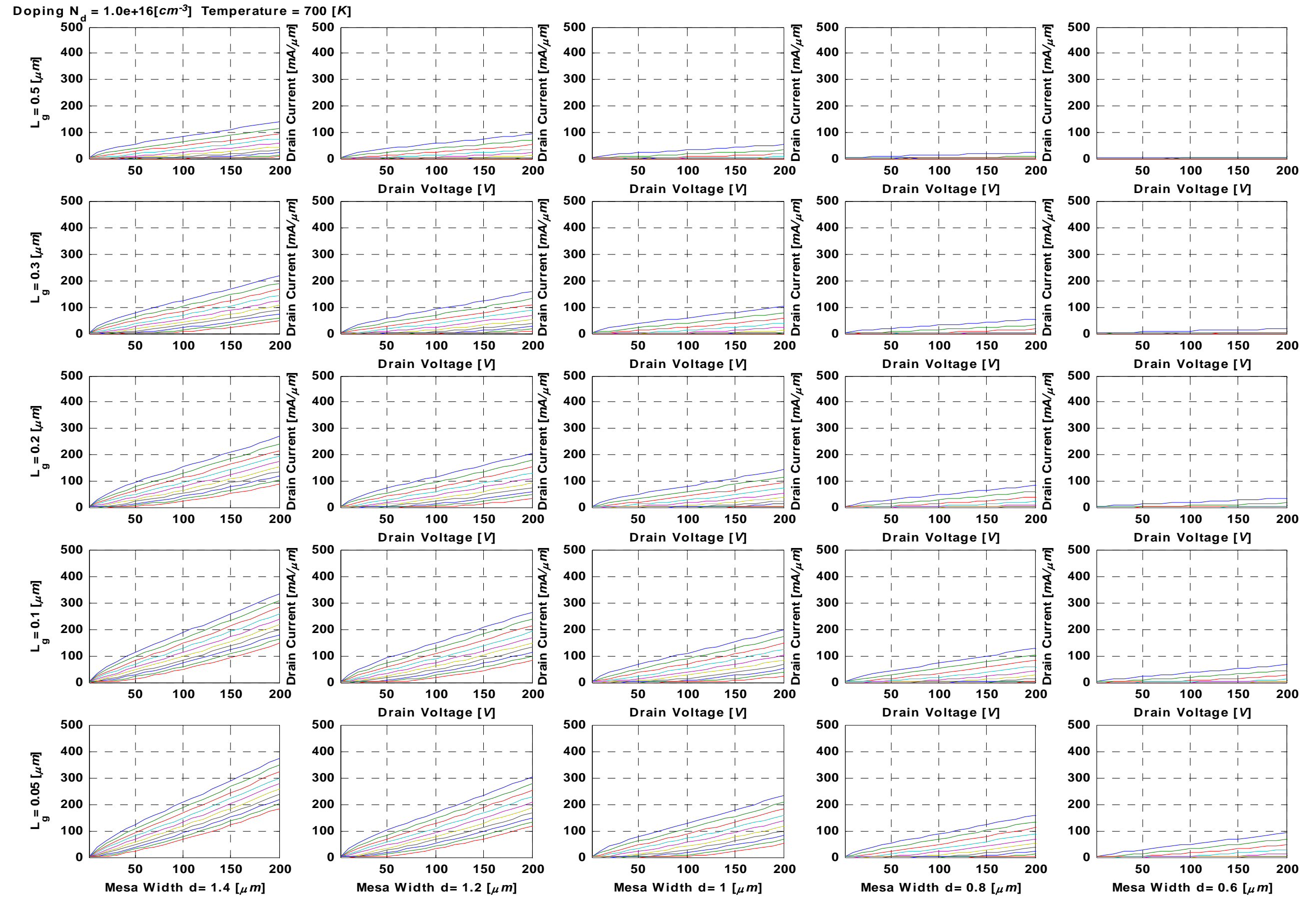

Figure B.11 I-V curves for different values of L_g and $2a$, with $N_D = 1 \cdot 10^{16}$ [cm^{-3}] and 700 [K].

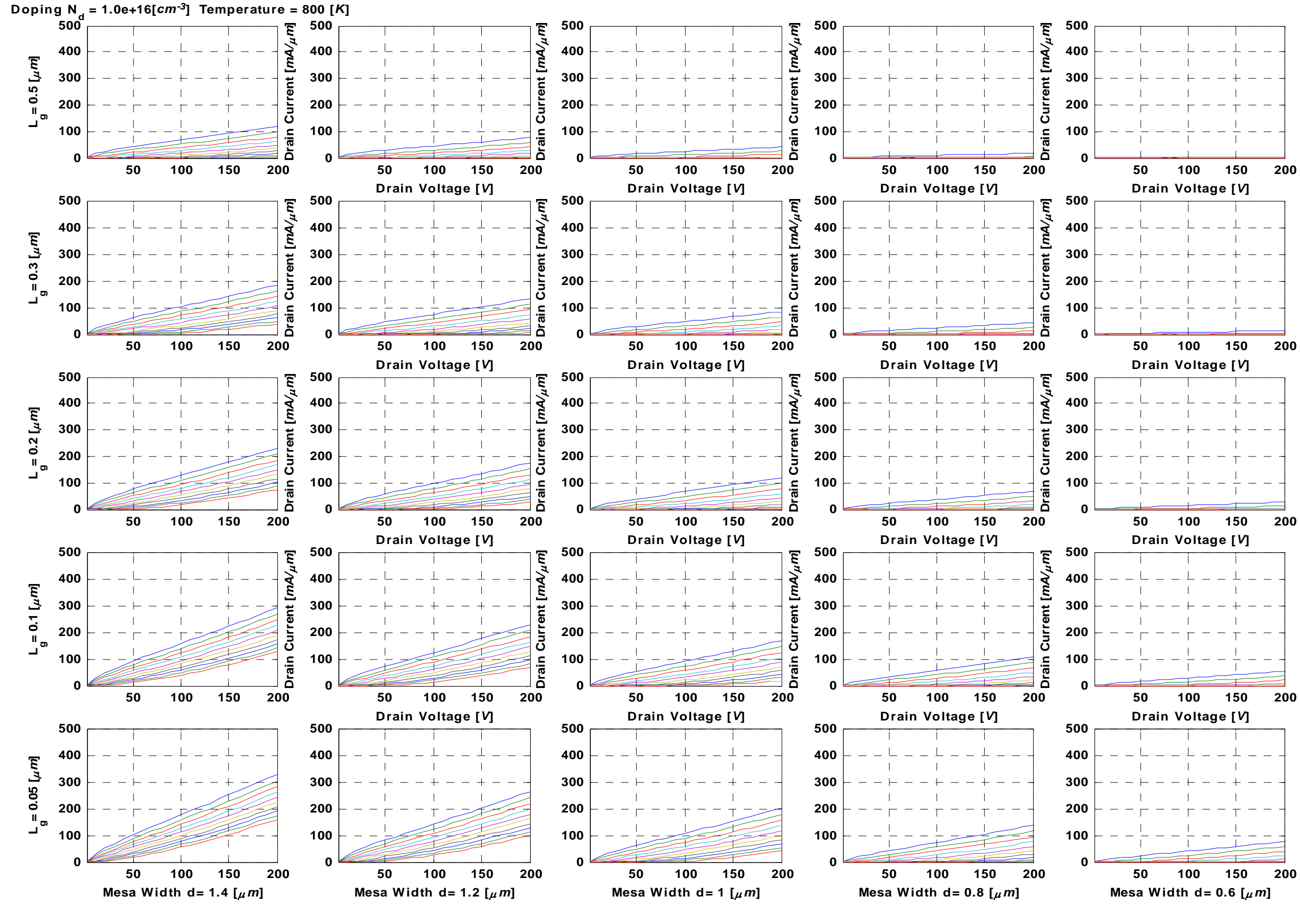

Figure B.12 I-V curves for different values of L_g and $2a$, with $N_D = 1{\cdot}10^{16}$ [cm^{-3}] and 800 [K].

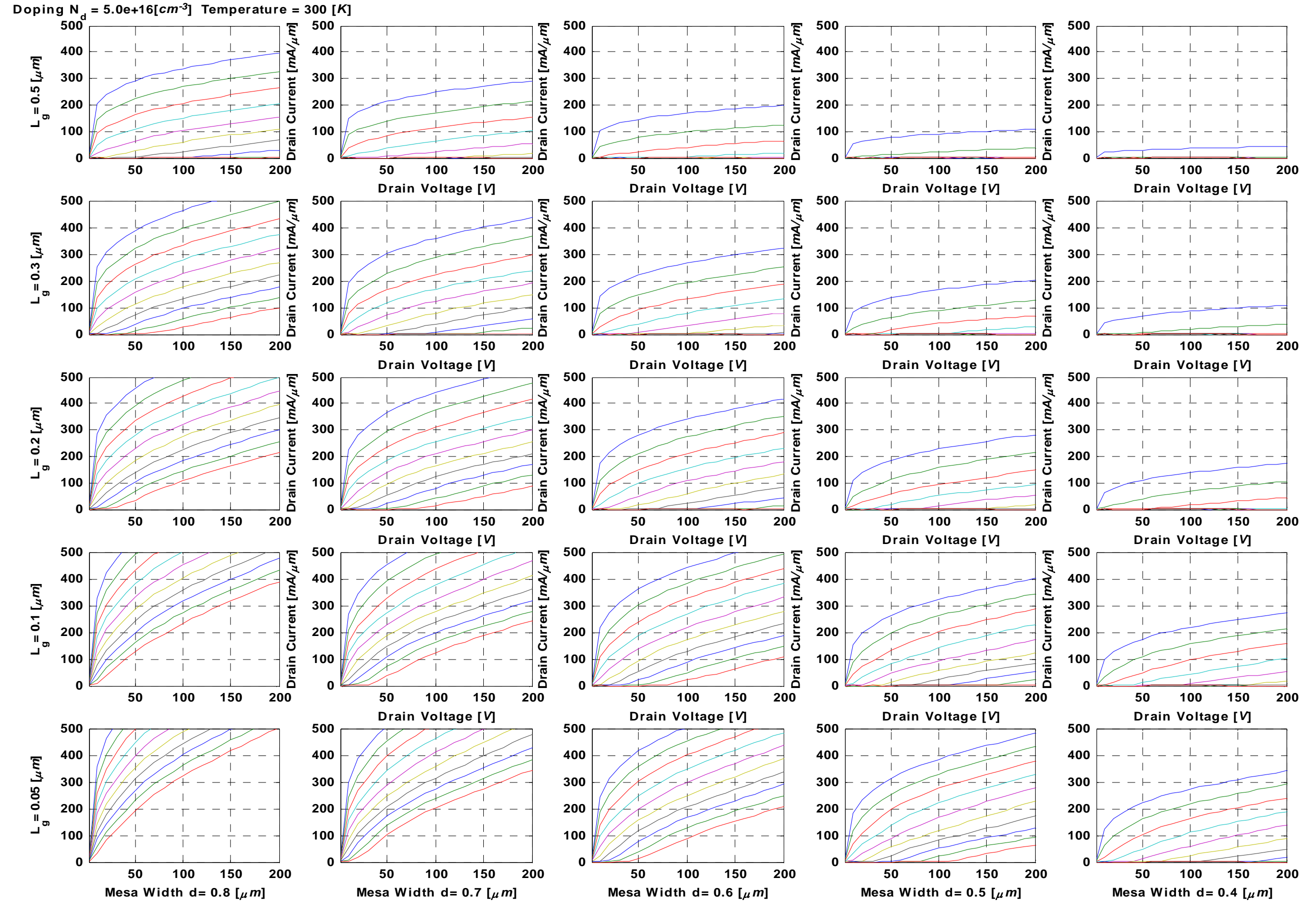

Figure B.13 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{16}$ [cm^{-3}] and 300 [K].

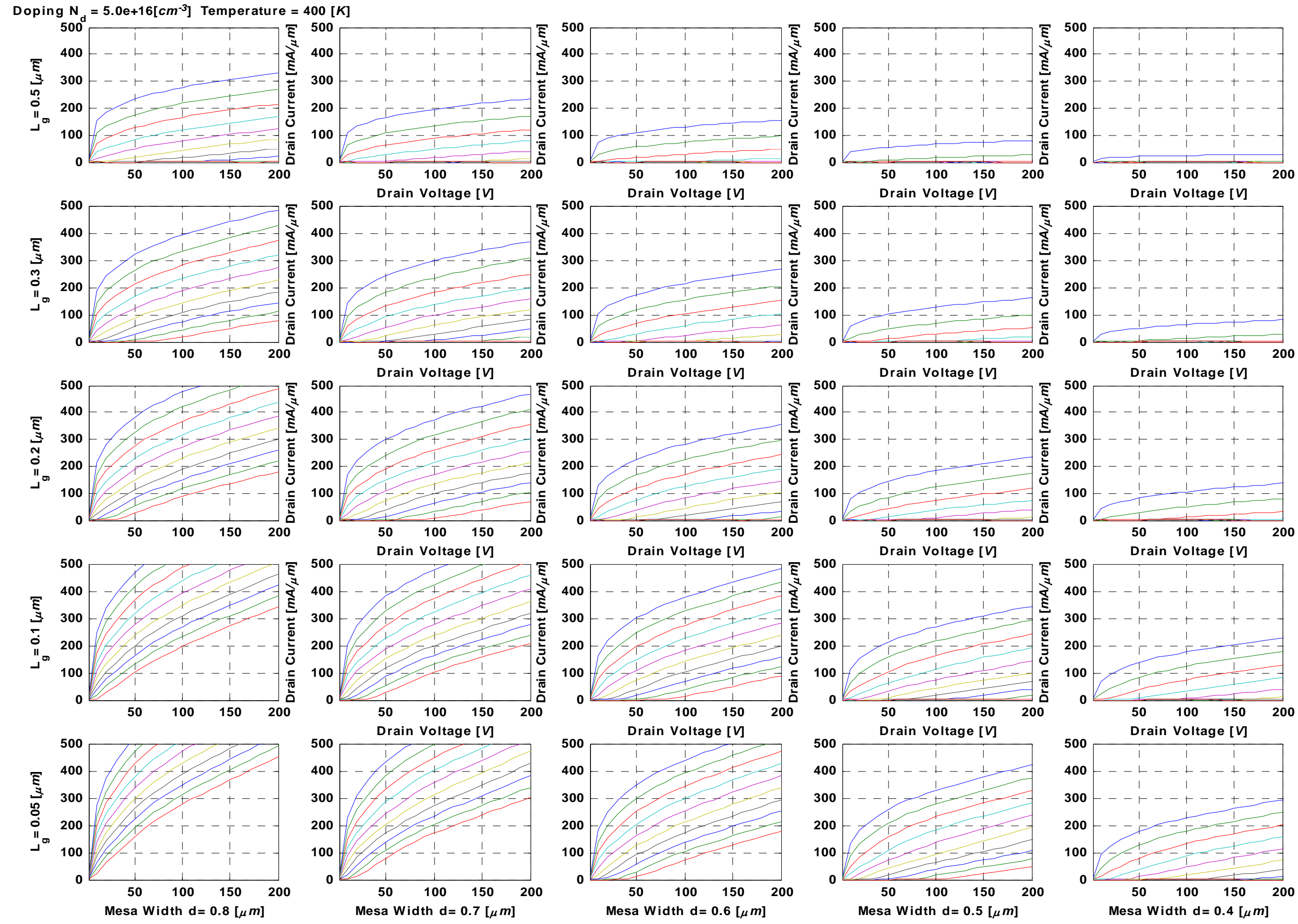

Figure B.14 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{16}$ $[cm^{-3}]$ and 400 $[K]$.

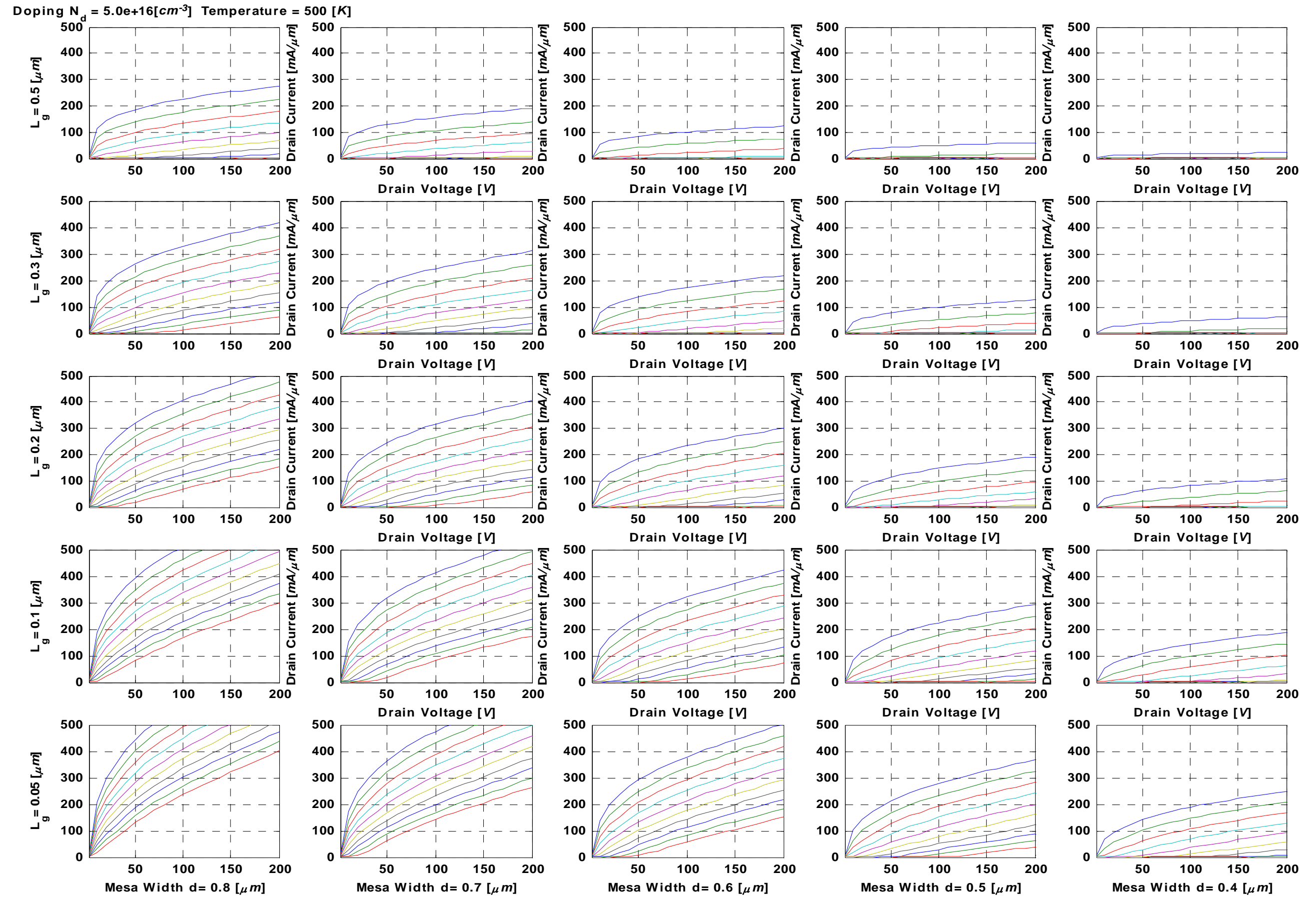

Figure B.15 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{16}$ [cm^{-3}] and 500 [K].

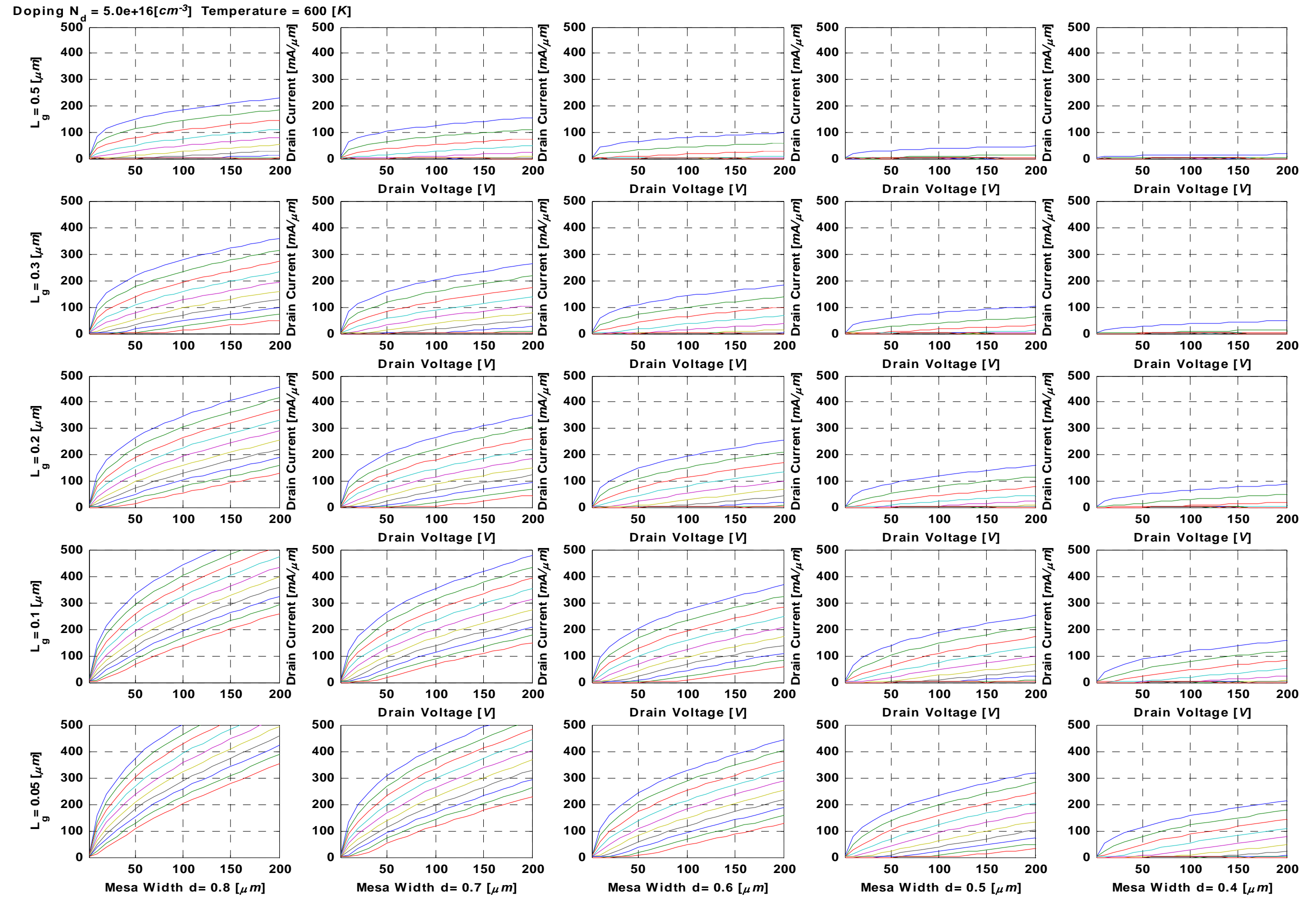

Figure B.16 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{16}$ [cm^{-3}] and 600 [K].

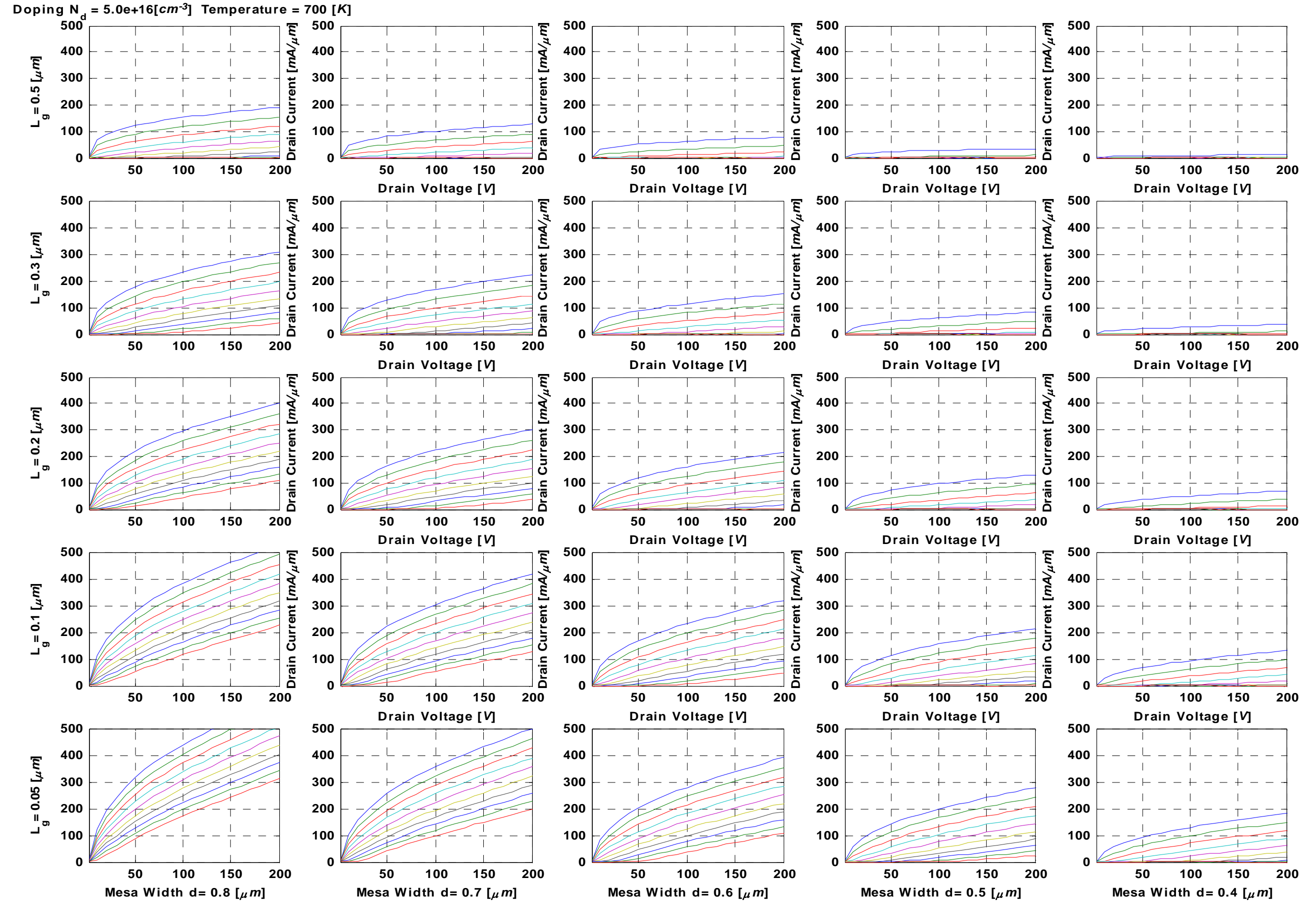

Figure B.17 I-V curves for different values of L_g and $2a$, with $N_D = 5 \cdot 10^{16}$ [cm^{-3}] and 700 [K].

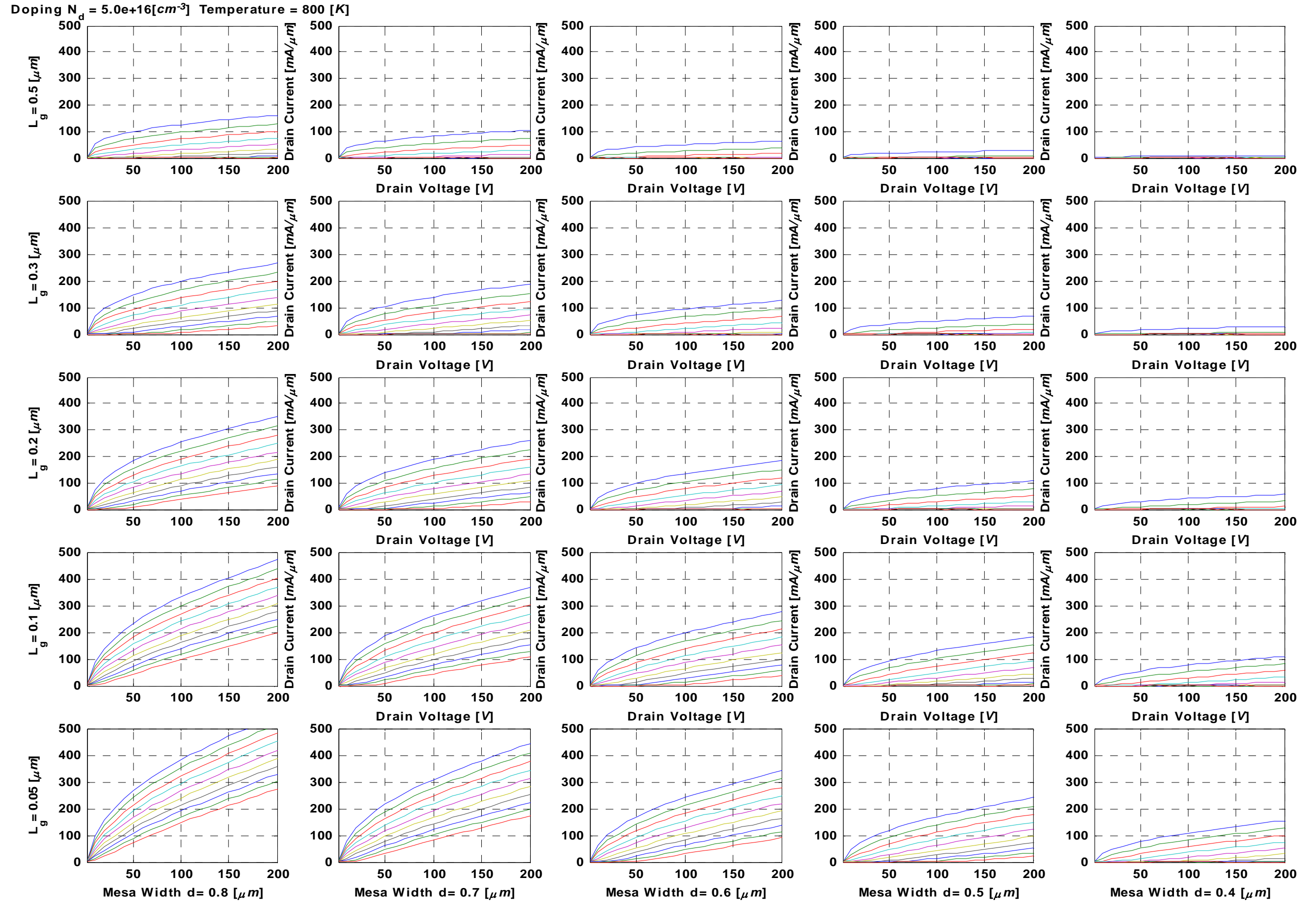

Figure B.18 I-V curves for different values of L_g and $2a$, with $N_D = 5{\cdot}10^{16}$ [cm^{-3}] and 800 [K].

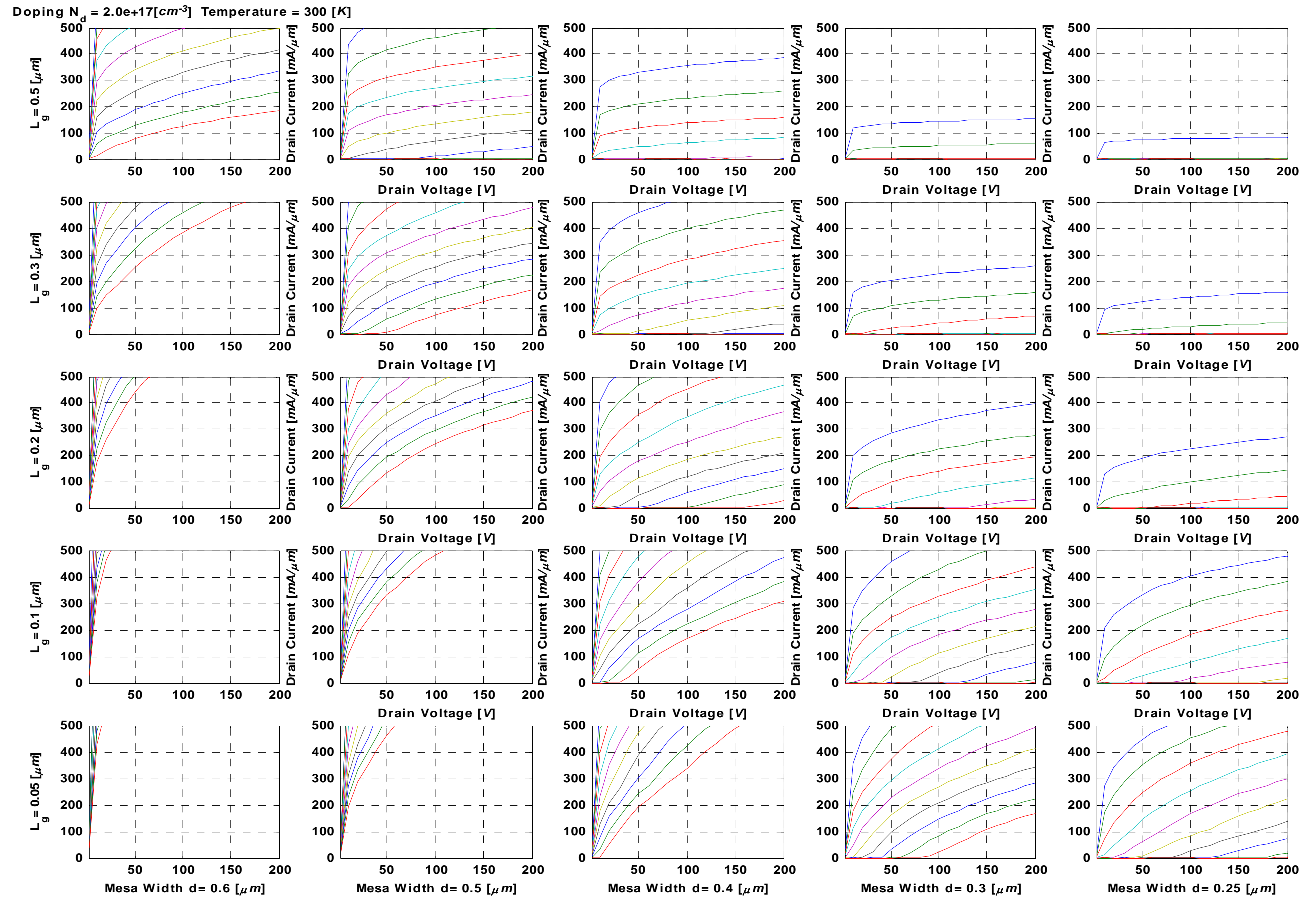

Figure B.19 I-V curves for different values of L_g and $2a$, with $N_D = 2 \cdot 10^{17}$ [cm^{-3}] and 300 [K].

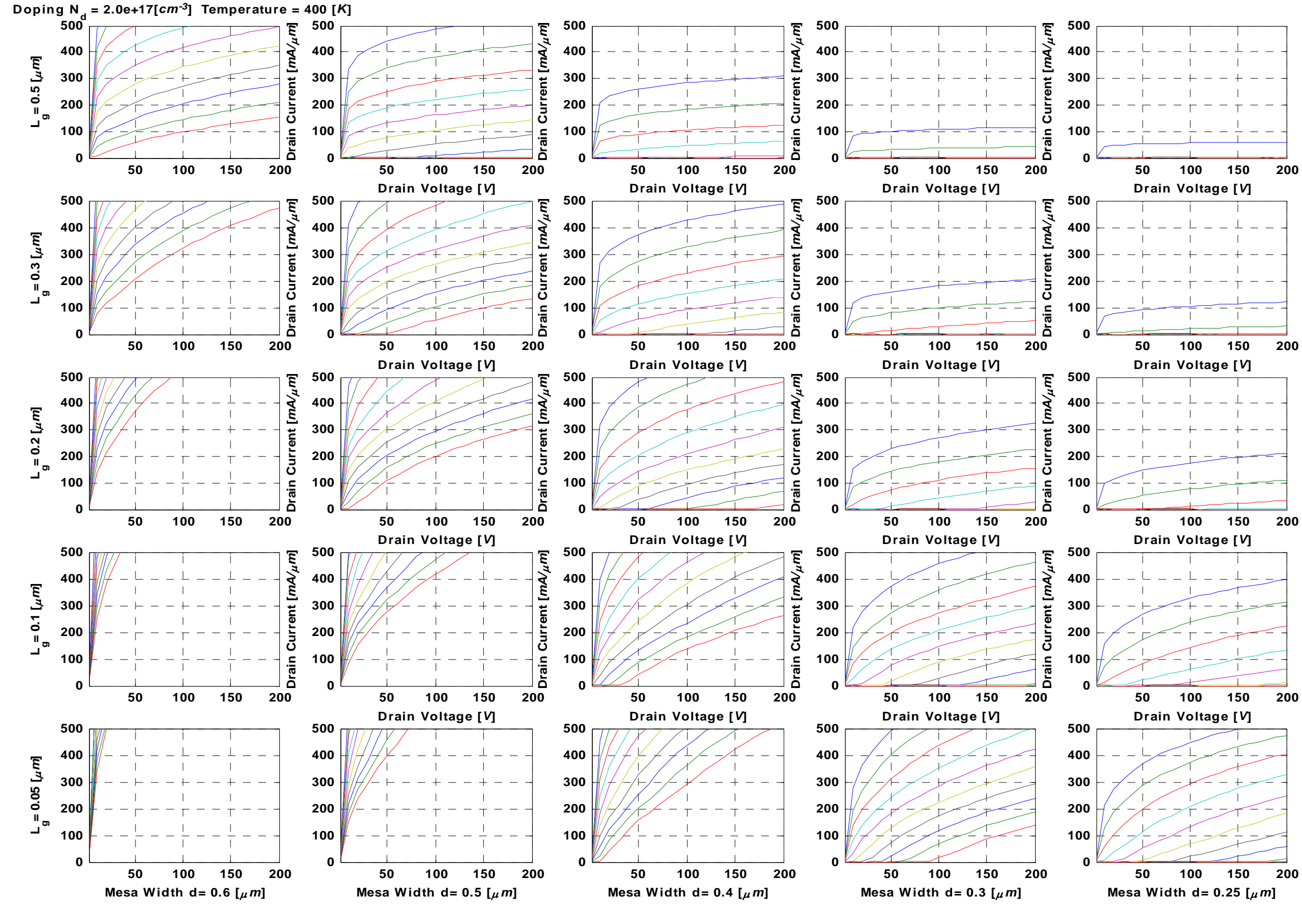

Figure B.20 I-V curves for different values of L_g and $2a$, with $N_D = 2\cdot10^{17}$ [cm^{-3}] and 400 [K].

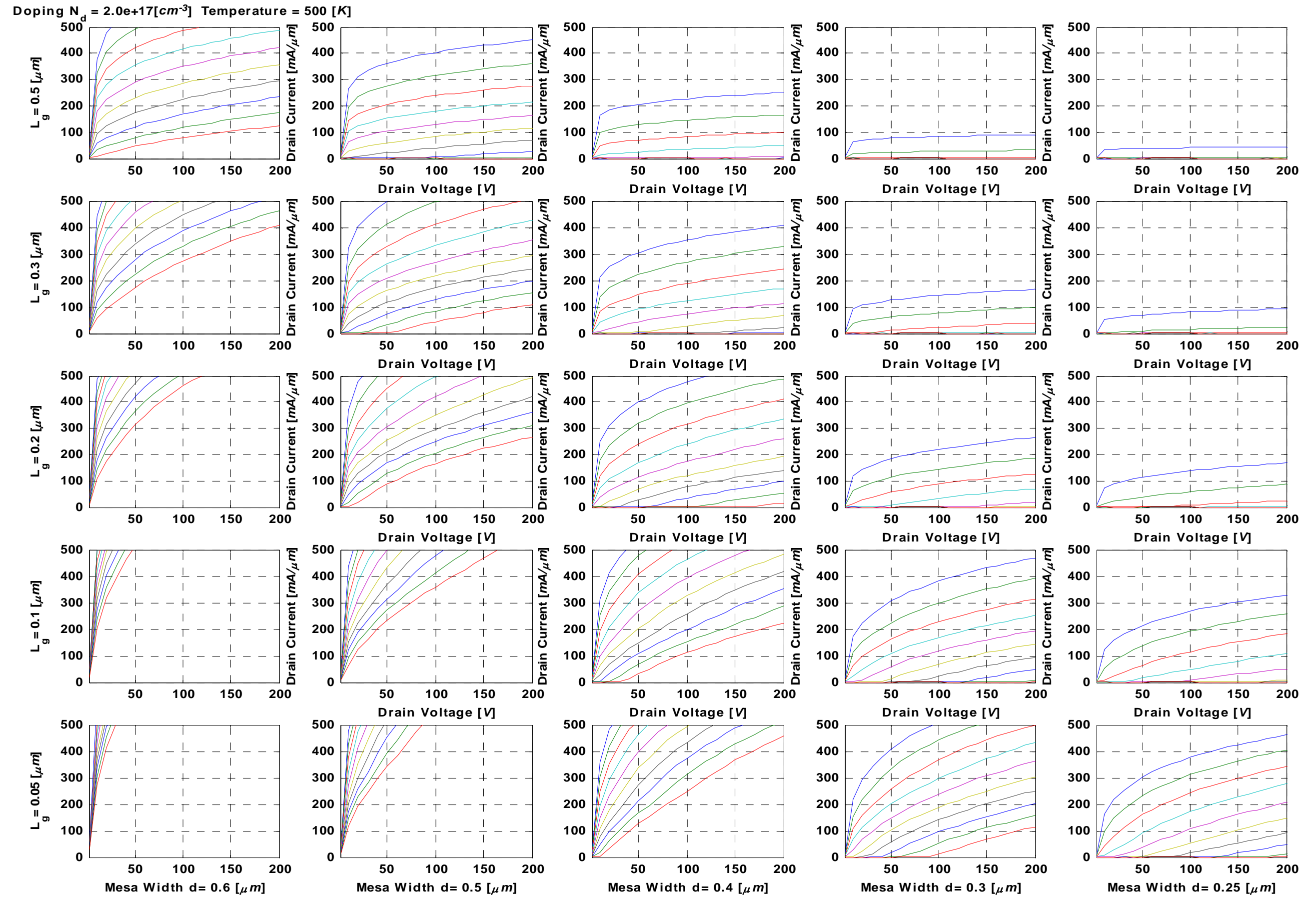

Figure B.21 I-V curves for different values of L_g and $2a$, with $N_D = 2{\cdot}10^{17}$ [cm^{-3}] and 500 [K].

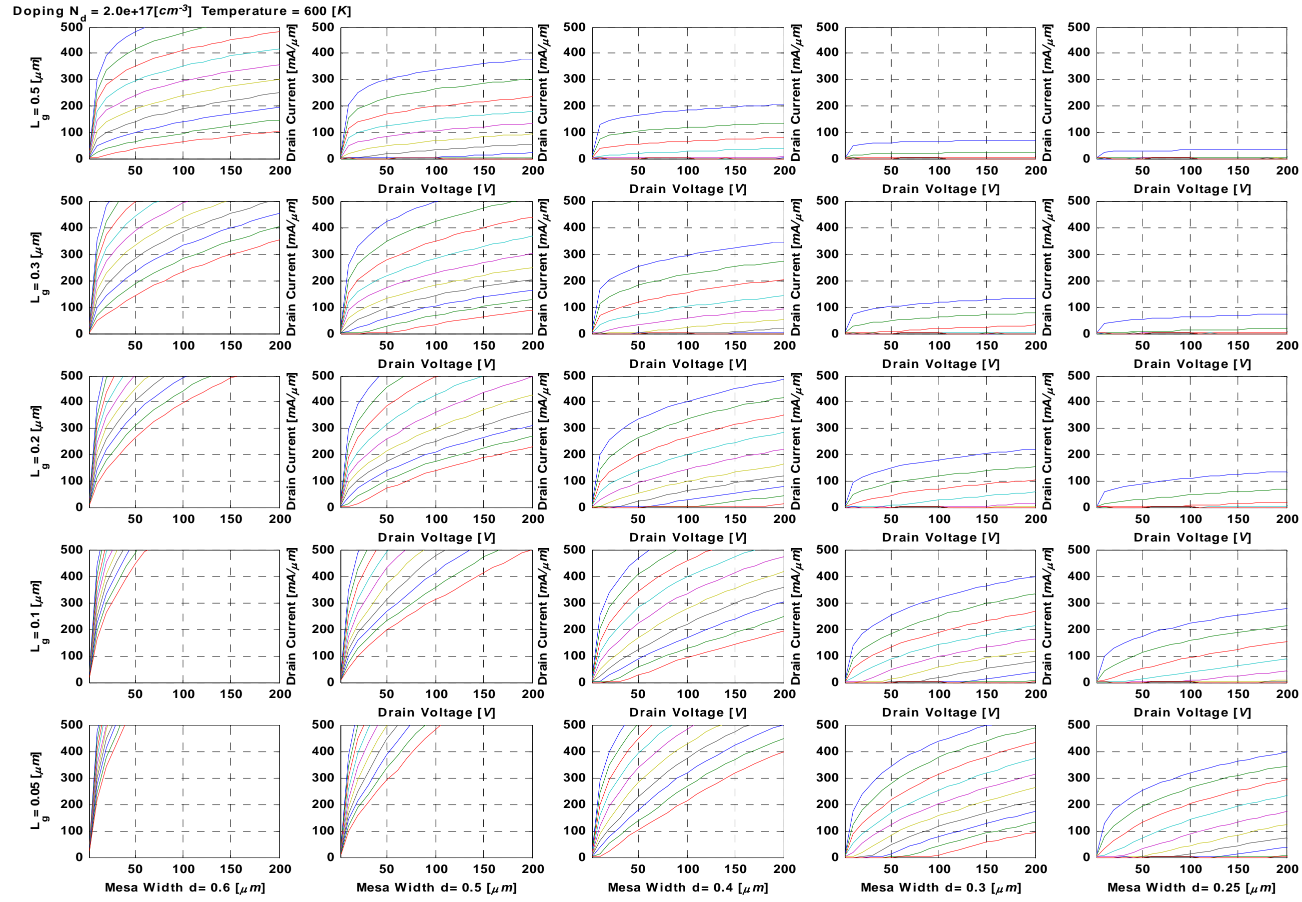

Figure B.22 I-V curves for different values of L_g and $2a$, with $N_D = 2 \cdot 10^{17}$ [cm^{-3}] and 600 [K].

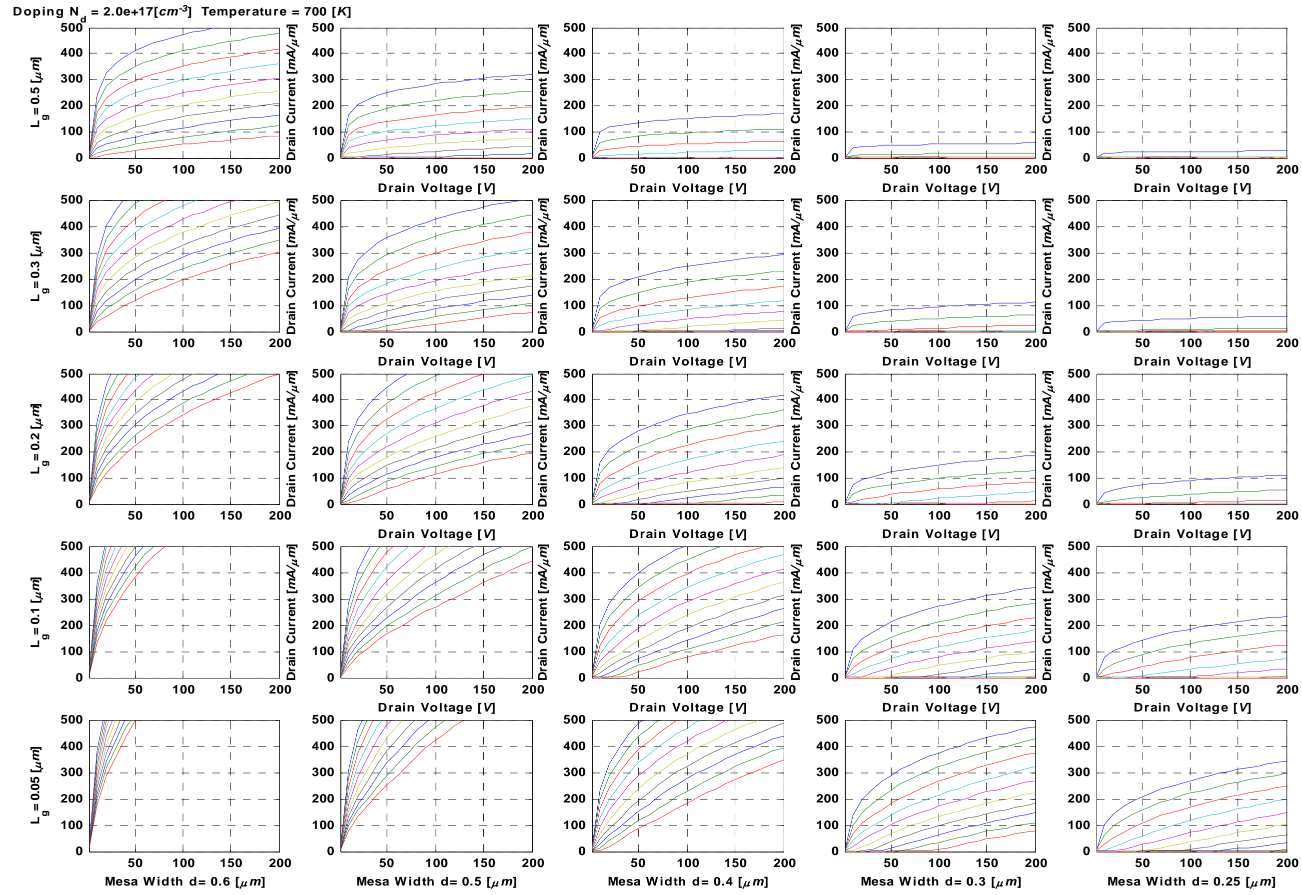

Figure B.23 I-V curves for different values of L_g and $2a$, with $N_D = 2{\cdot}10^{17}$ [cm^{-3}] and 700 [K].

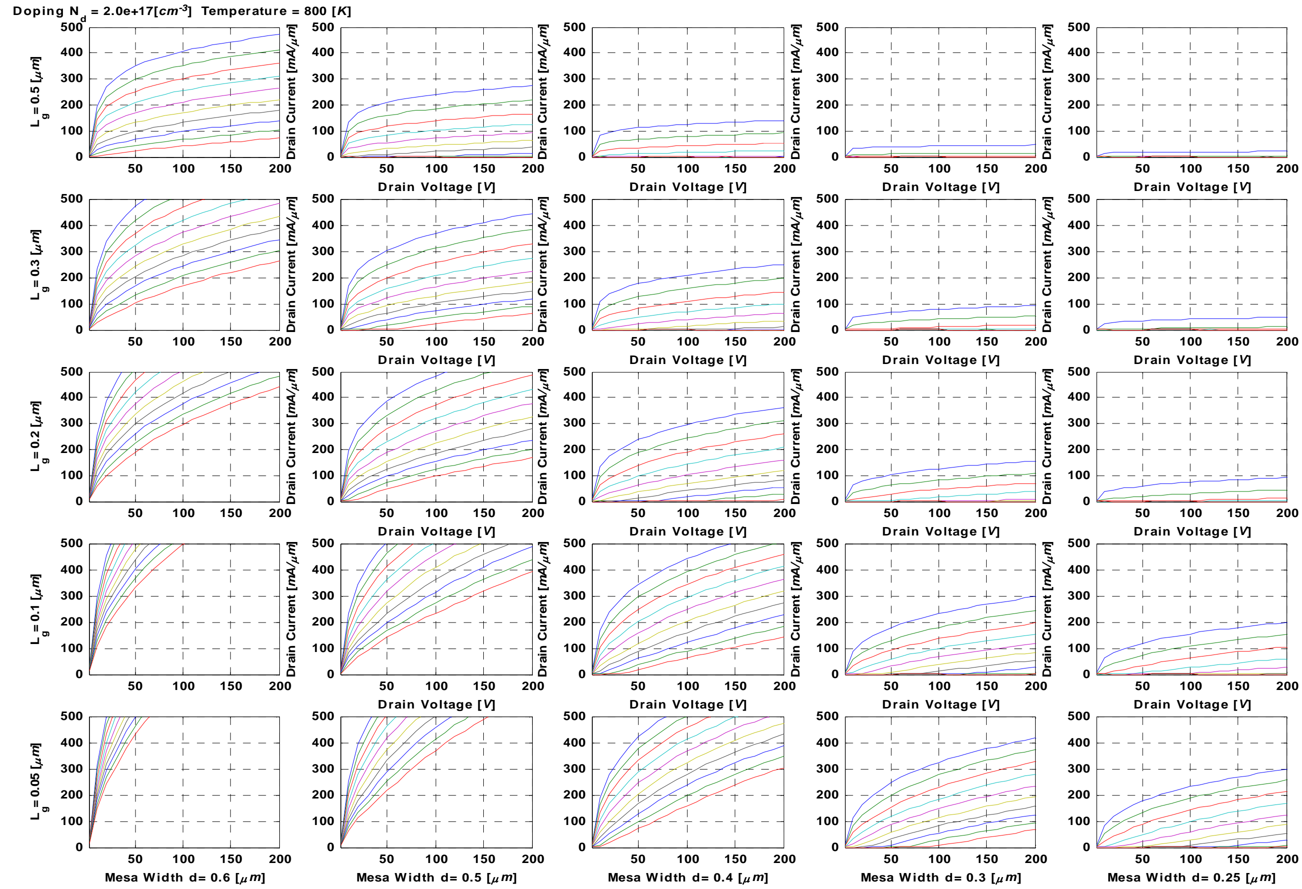

Figure B.24 I-V curves for different values of L_g and $2a$, with $N_D = 2{\cdot}10^{17}$ [cm^{-3}] and 800 [K].

APPENDIX C

Conversion from Y-parameter to S-parameter

Conversion from Y-parameter to S-parameter

$$Y_{11} = \frac{(1 - S_{11})(1 + S_{22}) + S_{12} \cdot S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12} \cdot S_{21}} = \frac{1}{h_{11}} \quad \text{(C-1)}$$

$$Y_{12} = \frac{-2 \cdot S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12} \cdot S_{21}} = \frac{-h_{12}}{h_{11}} \quad \text{(C-2)}$$

$$Y_{21} = \frac{-2 \cdot S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12} \cdot S_{21}} = \frac{h_{12}}{h_{11}} \quad \text{(C-3)}$$

$$Y_{22} = \frac{(1 + S_{11}) \cdot (1 - S_{22}) + S_{12} \cdot S_{21}}{(1 + S_{11}) \cdot (1 + S_{22}) - S_{12} \cdot S_{21}} = \frac{h_{11} \cdot h_{22} - h_{12} \cdot h_{21}}{h_{11}} \quad \text{(C-4)}$$

APPENDIX D

Simulation Results for Frequency and Transconductance Characteristics

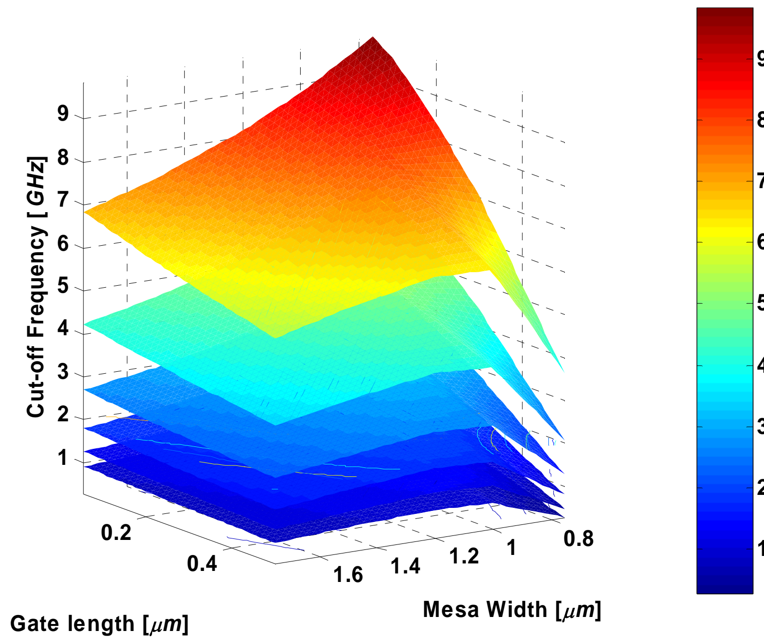

Fig. D.1 Cut-off frequency for different values of L_g and $2a$, with $N_D = 5{\cdot}10^{15}$ [cm^{-3}], from top to bottom, 300, 400, 500, 600, 700, 800 [K], respectively.

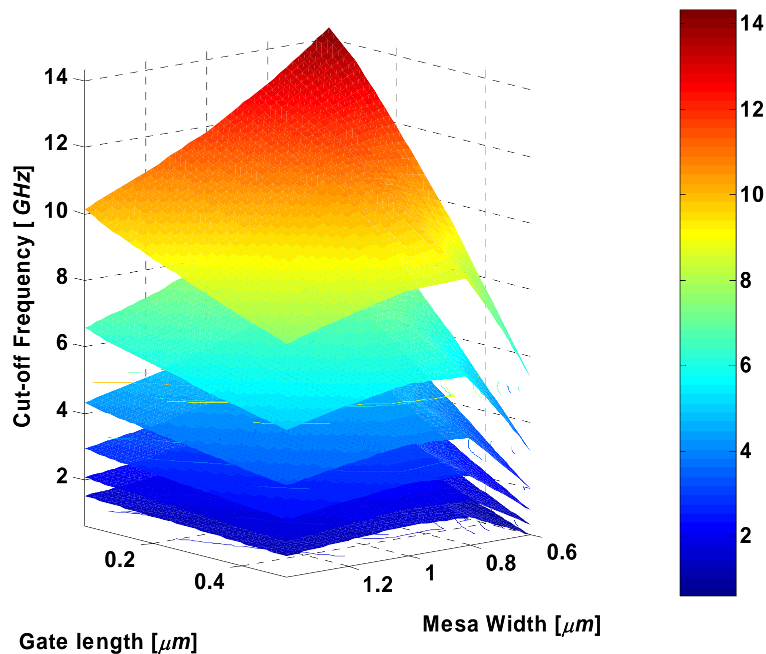

Fig. D.2 Cut-off frequency for different values of L_g and $2a$, with $N_D = 1{\cdot}10^{16}$ [cm^{-3}], from top to bottom, 300, 400, 500, 600, 700, 800 [K], respectively.

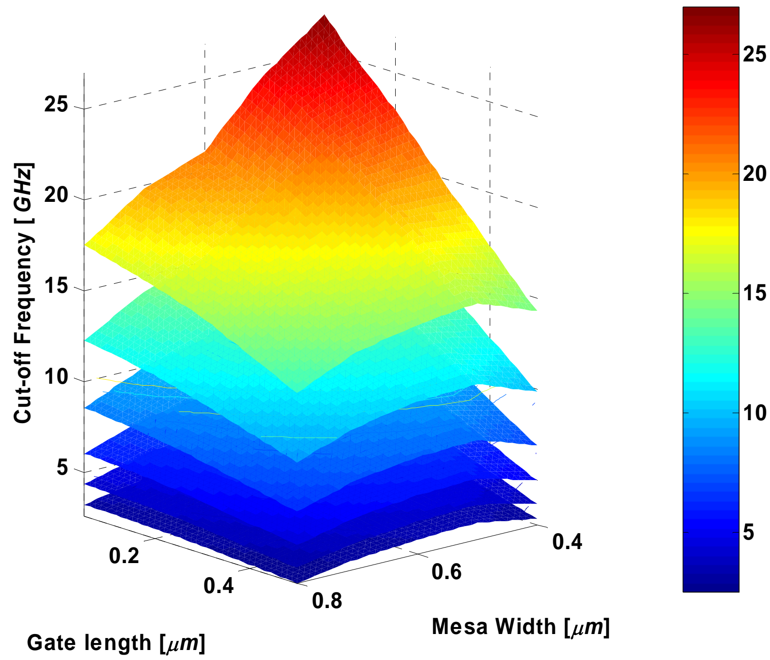

Fig. D.3 Cut-off frequency for different values of L_g and $2a$, with $N_D = 5{\cdot}10^{16}$ [cm^{-3}], from top to bottom, 300, 400, 500, 600, 700, 800 [K], respectively.

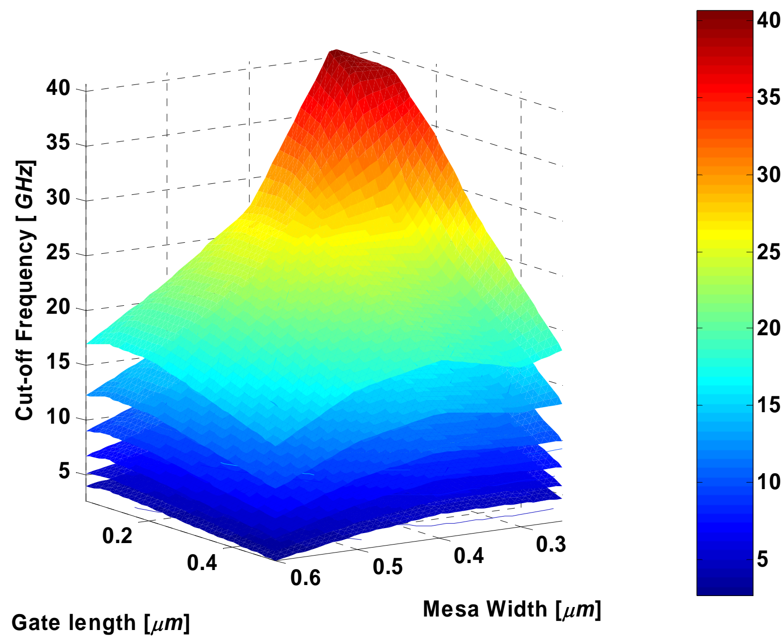

Fig. D.4 Cut-off frequency for different values of L_g and $2a$, with $N_D = 2{\cdot}10^{17}$ [cm^{-3}], from top to bottom, 300, 400, 500, 600, 700, 800 [K], respectively.

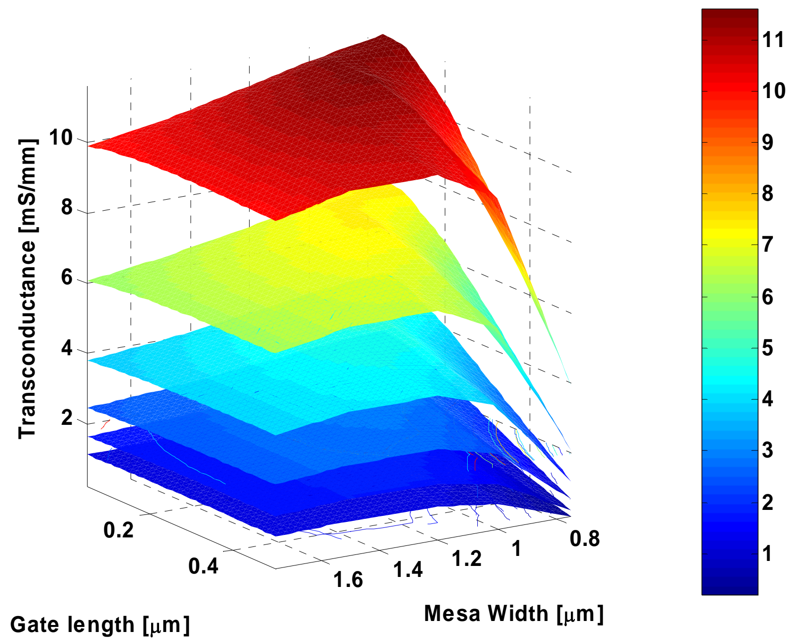

Fig. D.5 Transconductance for different values of L_g and $2a$, with $N_D = 5{\cdot}10^{15}$ [cm^{-3}], from top to bottom, 300, 400, 500, 600, 700, 800 [K], respectively.

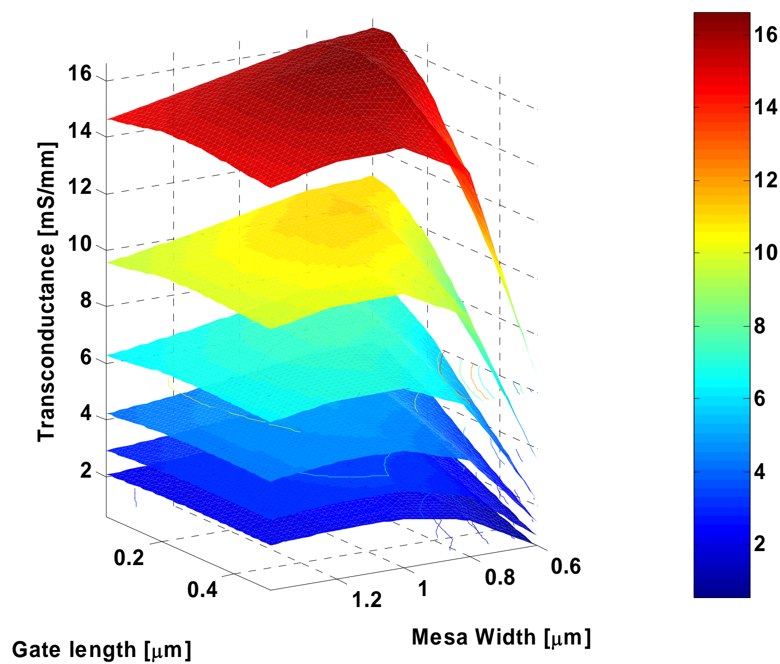

Fig. D.6 Transconductance for different values of L_g and $2a$, with $N_D = 1{\cdot}10^{16}$ [cm^{-3}], from top to bottom, 300, 400, 500, 600, 700, 800 [K], respectively.

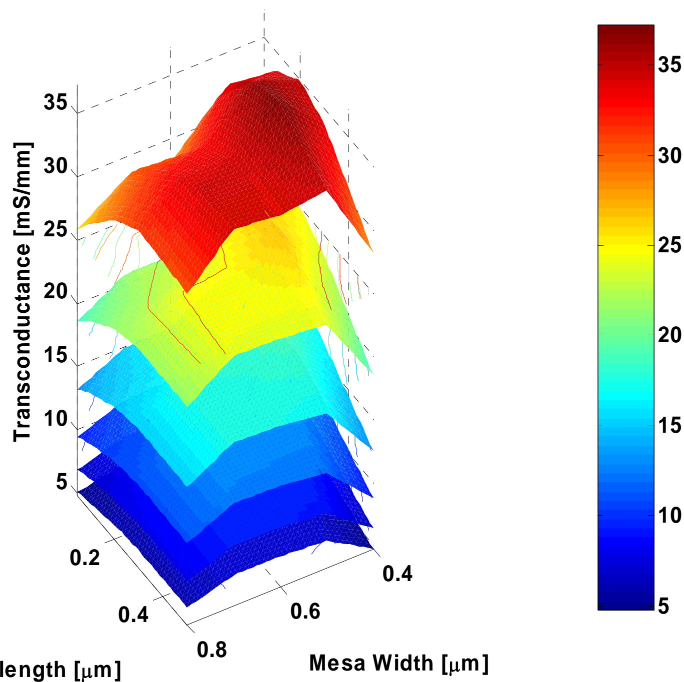

Fig. D.7 Transconductance for different values of L_g and $2a$, with $N_D = 5{\cdot}10^{16}$ [cm^{-3}], from top to bottom, 300, 400, 500, 600, 700, 800 [K], respectively.

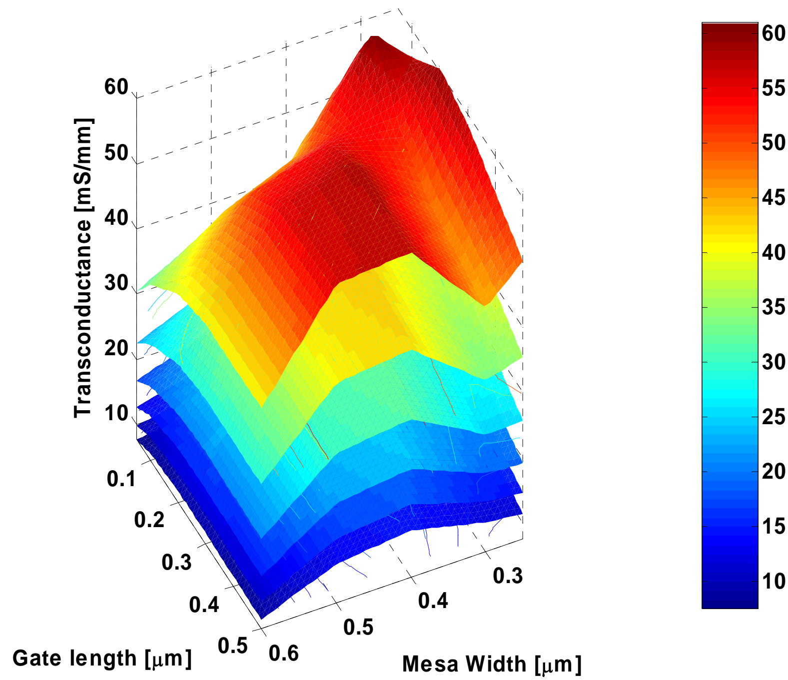

Fig. D.8 Transconductance for different values of L_g and $2a$, with $N_D = 2{\cdot}10^{17}$ [cm^{-3}], from top to bottom, 300, 400, 500, 600, 700, 800 [K], respectively.