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Siddharth Purohit

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# COMPACT MODELING OF SILICON CARBIDE (SIC) VERTICAL JUNCTION FIELD EFFECT TRANSISTOR (VJFET) IN PSPICE USING ANGELOV MODEL AND PSPICE SIMULATION OF ANALOG CIRCUIT BUILDING BLOCKS USING SIC VJFET MODEL.

By

Siddharth Purohit

A Thesis
Submitted to the Faculty of
Mississippi State University
in Partial Fulfillment of the Requirements
for the Degree of Master of Science
in Electrical Engineering
in the Department of Electrical and Computer Engineering

Mississippi State, Mississippi

December 2006

COMPACT MODELING OF SILICON CARBIDE (SIC) VERTICAL JUNCTION FIELD EFFECT TRANSISTOR (VJFET) IN PSPICE USING ANGELOV MODEL AND PSPICE SIMULATION OF ANALOG CIRCUIT BUILDING BLOCKS USING SIC VJFET MODEL.

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Pages in Study: 75

Candidate for Degree of Master of Science

This thesis presents the development of compact model of novel Silicon Carbide (SiC) Vertical Junction Field Effect Transistor (VJFET) for high-power PSpice circuit simulation using empirical Angelov model. The model is capable of accurately replicating the device behavior for the DC and Transient conditions. The model was validated against measured data obtained from devices developed by Mississippi Center for Advanced Semiconductor Prototyping at MSU and SemiSouth Laboratories. The modeling approach is based on extracting Angelov Equations Coefficients from experimental device characteristics using non linear fitting for different parameters (temperature, width, etc). Multi-Dimensional Interpolation Technique is used to incorporate the effect of more than one parameter. The models developed in this research are expected to be valuable tools for electronic designers.

The developed SiC VJFET model was applied for investigating the characteristics of few analog circuits. The selected circuits of interest were Voltage Follower, Common Source Amplifier, Current Source and Differential Amplifier.

# DEDICATION

I would like to dedicate this thesis to my parents, Dr. Mahesh Purohit and Mrs. Sudha Purohit and to my sisters.

ACKNOWLEDGMENTS

I would like to express my sincere gratitude to my advisor, Dr. Yaroslav Koshka for giving me an opportunity to work in his research group and whose guidance and support made this work possible. I would like to thank him for his valuable suggestions and discussions throughout my Master's Program.

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My special thanks to my parents and sisters for always being there for me.

TABLE OF CONTENTS

Page

DEDICATION .......... ii

ACKNOWLEDGMENTS .......... iii

LIST OF TABLES .......... vii

LIST OF FIGURES .......... viii

CHAPTER

I. INTRODUCTION .......... 1
1.1 Thesis motivation .......... 1
1.2 Thesis scope .......... 2
1.3 Thesis organization .......... 3

II. LITERATURE REVIEW .......... 4
2.1 Silicon Carbide (SiC) as a semiconductor material .......... 4
2.1.1 Electrical and material properties of SiC .......... 4
2.1.2 Crystal Structure of SiC .......... 6
2.1.3 Current status of SiC devices .......... 7
2.2 Vertical junction field effect transistor (VJFET) .......... 9
2.2.1 Device structure .......... 9
2.2.2 Device physics .......... 10
2.3 Circuit simulator .......... 15
2.3.1 Introduction to simulators .......... 15

III. SIC VJFET MODEL DEVELOPMENT APPROACH (PSPICE SIMULATION) .......... 17

CHAPTER Page


3.1 Semiconductor device modeling .......... 17
3.1.1 Different modeling techniques for semiconductor devices .......... 17
3.1.2 Modeling Methodology .......... 20
3.1.3 Interpolation Technique .......... 21
3.1.4 Modeling in PSpice .......... 23
3.1.5 Modeling the SiC VJFET .......... 24
3.1.6 Angelov Model Description .......... 24
3.1.7 Modeling of DC characteristics by Angelov Model .......... 26
3.1.7.1 Description of the Drain Current Model .......... 26
3.1.7.2 Description of the Gate Current Model .......... 27
3.1.8 Switching Characteristics .......... 28

IV. VALIDATION RESULTS .......... 30
4.1 Introduction .......... 30
4.2 Model Validation .......... 30
4.2.1 DC Analysis .......... 30
4.2.1.1 DC test circuit .......... 30
4.2.1.2 Drain current vs. Drain voltage for high values of current .......... 31
4.2.1.3 Drain current vs. Drain voltage for high values of voltage .......... 32
4.2.1.4 Gate current ($I_{gs}$) vs. Gate voltage ($V_{gs}$) .......... 33
4.2.2 Incorporation of parameters in the model .......... 34
4.2.2.1 Drain Current vs. Temperature .......... 35
4.2.2.2 Drain Current vs. Finger Width .......... 36
4.2.3 Transient Analysis .......... 38
4.2.3.1 Switching test circuit .......... 38
4.2.3.2 Switching Waveforms .......... 40

V. ANALOG CIRCUIT BUILDING BLOCKS .......... 43
5.1 Analog Circuit Building Blocks .......... 43
5.1.1 Voltage Follower .......... 43
5.1.1.1 Simulation results for voltage follower with SiC VJFET and Si JFET .......... 45
5.1.2 Common Source Amplifier .......... 47
5.1.2.1 Simulation results for Common Source amplifier with SiC VJFET and Si JFET .......... 48
5.1.3 Current Source .......... 49
5.1.3.1 Simulation results for Current Source with SiC VJFET and Si JFET .......... 51
5.1.4 Differential Amplifier .......... 53

CHAPTER Page

5.1.4.1 Simulation results for Differential Amplifier with SiC VJFET and Si JFET ........ 55

VI. CONCLUSIONS AND FUTURE WORK ........ 59

REFERENCES ........ 61

APPENDIX

A. PSPICE SIMULATOR ........ 64

B. MAJOR FILES ........ 73

LIST OF TABLES

TABLE Page

1 Key Characteristics of SiC vs. other materials ............................................. 5

2 Languages and their associated simulators ................................................... 16

3 Comparison of modeling techniques against various parameters [12] .......... 19

4 Comparison of Experimental and PSpice simulation switching data ........... 42

LIST OF FIGURES

FIGURE Page

1 Molecular arrangement of various SiC Polytypes [4] .......... 7

2 Unit cell representation of SiC –a = 3.8A$^{o}$ [4] .......... 7

3 Cross section view of SiC .......... 9

4 Triode Like DC characteristics of short channel VJFETs [7] .......... 12

5 Pentode Like DC characteristics of long channel VJFETs [7] .......... 13

6 Different regions of operation of VJFET [7,8] .......... 13

7 Flowchart showing the Modeling Methodology .......... 21

8 Bicubic Spline Interpolation .......... 22

9 Equivalent circuit representation of SiC VJFET large signal model [13] .......... 24

10 Test bench for DC measurement [22] .......... 31

11 SiC VJFET PSpice simulated (light grey) and measured (dark grey) drain current-drain voltage waveforms for high current at different gate voltages .......... 32

12 SiC VJFET PSpice simulated (light grey) and measured (dark grey) drain current-drain voltage waveforms for high voltage at different gate voltages .......... 33

13 SiC VJFET PSpice simulated (light grey) and measured (dark grey) gate current-gate voltage waveform .......... 34

14 SiC VJFET PSpice simulated (light grey) and measured (dark grey) drain current-temperature waveform for drain voltage=0.2V and gate voltage=0.5V .......... 36

FIGURE Page

15 SiC VJFET PSpice simulated (light grey) and Medici (dark grey) drain current-finger width waveform for drain voltage=2V, gate voltage=2V, and temperature=473K ........ 37

16 Test bench for transient analysis [22] ........ 40

17 Switching Waveforms for drain voltage (Vds), drain current (Id), and gate voltage (Vgs) for (a) Experimental (b) PSpice simulation ........ 41

18 Voltage Follower Circuit ........ 44

19 SiC VJFET Voltage Follower-Plot of Vout and Vin vs. time ........ 45

20 Si JFET Voltage Follower-Plot of Vout and Vin vs. time ........ 46

21 Common Source Amplifier [21] ........ 47

22 SiC VJFET Common Source Amplifier-Plot of Vout and Vin vs. time ........ 48

23 Si VJFET Common Source Amplifier-Plot of Vout and Vin vs. time ........ 49

24 Reference Generator [24] ........ 50

25 Current Source [6] [22] ........ 50

26 Si JFET Current Source - Plot of drain current vs. drain voltage ........ 52

27 Si JFET Current Source - Plot of drain current vs. drain voltage ........ 52

28 Differential Amplifier Circuit [20] [23] ........ 53

29 SiC VJFET Differential Amplifier-Plot of Differential Mode Gain vs. frequency ........ 56

30 Si JFET Differential Amplifier-Plot of Differential Mode Gain vs. frequency ........ 56

31 SiC VJFET Differential Amplifier-Plot of Common Mode Gain vs. frequency ........ 57

32 Si JFET Differential Amplifier-Plot of Common Mode Gain vs. frequency ........ 57

33 Diode characteristic curve and tangent line [9] ........ 66

FIGURE Page

34 Linear Companion model of diode [9] ..... 67

35 PSpice Algorithm ..... 69

36 Backward Euler Integration applied to approximate the next voltage [9] ..... 71

37 Linear companion model of a capacitor using the Backward Euler Formula [9] . 72

# CHAPTER I

# INTRODUCTION

## 1.1 Thesis motivation

Reliable device models are among the circuit designer's most vital tools. Any circuit needs to be simulated and analyzed many times before being built. Only after obtaining satisfactory results from the simulations, are the prototypes built. Prototyping costs would be too high and the time to market also dramatically increases without models and circuit simulators. PSpice (Simulation Program with Integrated Circuit Emphasis) is a circuit simulator widely used by the electronic designers to analyze the circuit by utilizing the device models present in the PSpice library. Most of the models that are present in PSpice are for silicon devices.

At this point, there is now a new challenge in terms of fundamental device technology. Devices made from Silicon Carbide (SiC) are becoming more than just laboratory curiosities. SiC devices perform many orders of magnitude better than their Si counterparts in respect to the breakdown voltage, high temperature capabilities, saturation drift velocity, etc. (Chapter 2). Hence, there is an increasing demand for these devices. Cree Inc., based in Raleigh, N.C. has commercially released Schottky diodes. SiCED GmBH (a spin-off from Infineon) and SemiSouth Laboratories (Starkville, MS) are now actively involved in developing SiC Junction Field Effect Transistors (JFET). As the electronics community readies itself to rapidly embrace this new technology, the

availability of reliable device models becomes another hurdle. Most of the device models are currently available for silicon devices. Circuit designers need validated models for Si counterparts in SiC to effectively utilize SiC based devices in circuits. These devices are currently very expensive. Hence, it is not economically viable to make circuits without simulating them as the devices can be destroyed during the circuit testing.

Given the increasing demand for SiC JFETs in various sectors such as automobiles, energy conversion, space and aviation, it is imperative that compact models are available to electronic designers for prototyping the circuits. As of now, only SemiSouth and SiCED have commercially released SiC JFETs. This is therefore a perfect time to develop and release a SiC JFET model.

## 1.2 Thesis scope

Mississippi Center for Advanced Semiconductor Prototyping (MCASP) at Mississippi State University has taken a step towards developing SiC VJFET models in PSpice that could be used to analyze the SiC based circuits. The objective of this thesis is to develop a SiC VJFET model in PSpice suitable for DC and transient analysis and to validate the model by comparing it with the experimental results.

SiC VJFETs are attractive option for high power applications under extremely low temperatures and high radiation environment. An experimental investigation of the effects of the temperature on the DC and the switching performance of the SiC VJFETs for temperature range as low as 30K to 390K has been done in our previous paper [7]. This temperature dependent device characteristic for low temperatures has been implemented in our PSpice model, which is done for the first time to our knowledge. The

device model has also been used for simulating basic analog circuit blocks. The simulation results are compared with Si JFET PSpice simulation.

## 1.3 Thesis organization

Chapter-I describes the motivation for developing the SiC VJFET model in PSpice and the scope of this work.

Chapter 2 provides an overview of SiC as a semiconductor material, current status of SiC devices and their applications. The chapter also discusses device physics of VJFETs.

The device modeling methodology is described in Chapter 3. The description includes modeling in PSpice, topology development for the model and the characteristic DC and transient empirical equations for the JFET using Angelov model.

Any device model has to be validated against actual device measurements to be termed as an accurate model. Chapter 4 discusses the validation results. The validation results of the model (DC and Transient) for SiC VJFET using measured data are shown.

One of the important aspects of this work is to apply the validate model to predict behavior of SiC transistor in electronic circuits. Chapter 5 shows the simulation of SiC VJFET and Si JFET devices in standard analog circuits.

Chapter 6 is the conclusion part of the thesis and also discusses the future work to be done.

Appendix A gives information about PSpice simulator and Appendix B describes major files used in PSpice source code for developing our model.

CHAPTER II

# LITERATURE REVIEW

## 2.1 Silicon Carbide (SiC) as a semiconductor material.

### *2.1.1 Electrical and material properties of SiC*

Silicon Carbide (SiC) has long been known as a prospective semi conducting material. It was in fact considered more promising than Silicon (Si) during the early days of semiconductor technology [1,2]. But during 1960s, the Czochralski technique for the growth of single crystal Si had matured and large diameter boules with low defect densities were introduced. This significantly reduced interest in emerging SiC devices and vast amounts of resources were diverted to Si development. Large diameter single crystal growth is still the major stumbling block for the acceptance of SiC devices as they are prohibitively expensive and therefore economically feasible only for niche markets such as the military and aerospace industries. In the last decade, there has been a revival of interest in SiC devices as the defect densities in the wafers have been steadily decreasing and new growth methods being developed.

SiC have many inherent properties that make it an ideal semiconductor material useful for high-temperature and high-power applications where silicon has its limitations [3]. Table 2.1 compares the salient features of SiC with other semiconductors. SiC's

higher breakdown electric field allows the design of SiC power devices with thinner ($1/10^{th}$ that of silicon devices) and more highly doped (more than 10 times higher) voltage blocking layers. For unipolar power devices such as power Schottky diodes and MOSFETs, the combination of $1/10^{th}$ blocking layer thickness with 10 times doping concentration can yield a SiC device with a factor of 100 advantage in resistance compared to that of Si unipolar devices. For bipolar conductivity modulated devices such as PiN diodes, BJTs, and thyristors a blocking layer of $1/10^{th}$ thickness of a Si device can result in a factor of 100 faster switching speed.

Table 1

Key Characteristics of SiC vs. other materials.

| **Property** | **Si** | **GaAs** | **4H-SiC** | **6H-Sic** |
|---|---|---|---|---|
| Band Gap(eV) | 1.1 | 1.42 | 3.2 | 3.0 |
| Relative Dielectric Constant | 11.9 | 13.1 | 9.7 | 9.7 |
| Breakdown Field (MV/cm) | 0.25 | 0.3 | 2.2 | ~2.3 |
| Thermal Conductivity (W/cmK) | 1.5 | 0.5 | 4.8 | 3-5 |
| Electron Mobility ($cm^2$/V-S) @Nd = $10^{16}/cm^3$ | 1200 | 6500 | 800 | 60 |
| Hole Mobility ($cm^2$/V-S) @Nd = $10^{16}/cm^3$ | 420 | 320 | 115 | 90 |
| Saturated electron velocity ($x10^7$cm/s) | 1 | 1.2 | 2 | 2 |

As seen in Table 1, the band gap of 4H-SiC is nearly 3 times that of Si. This translates to a very high breakdown field (nearly 10 times than Si) suitable for power applications. The saturated electron drift velocity of SiC which determines the maximum current density of the device is also twice that of Si.

Another important property is the thermal conductivity of SiC, which is more than three times that of Si. High thermal conductivity obviates the need to have bulky and expensive cooling systems for the devices in most applications. This in turn translates into high cost savings in weight critical applications such as fighter planes and space shuttles.

SiC is expected to enable significant improvements to a far-ranging variety of applications and systems. These range from greatly improved high-voltage switching for energy savings in public electric power distribution and electric motor drives to a more powerful microwave electronics for radar and communications to sensors and controls for cleaner-burning more fuel-efficient jet aircraft and automobile engines [10].

### *2.1.2 Crystal Structure of SiC*

Fig. 1 shows a few different types of SiC according to crystal orientation, known as polytypes. Despite the fact that all SiC polytypes chemically consist of 50% carbon atoms covalently bonded with 50% silicon atoms, each SiC polytype has its own distinct set of electrical properties. In fact there are approximately 200 polytypes available. But only a handful can be grown successfully in the laboratory. 4H-SiC is now accepted as the *de facto* standard polytype for the majority of the device applications since it has the

highest mobility amongst all polytypes. Most of the polytypes have a hexagonal frame and the distance between the Si and C atom is invariably 3.8 $A^0$ (Fig. 2).

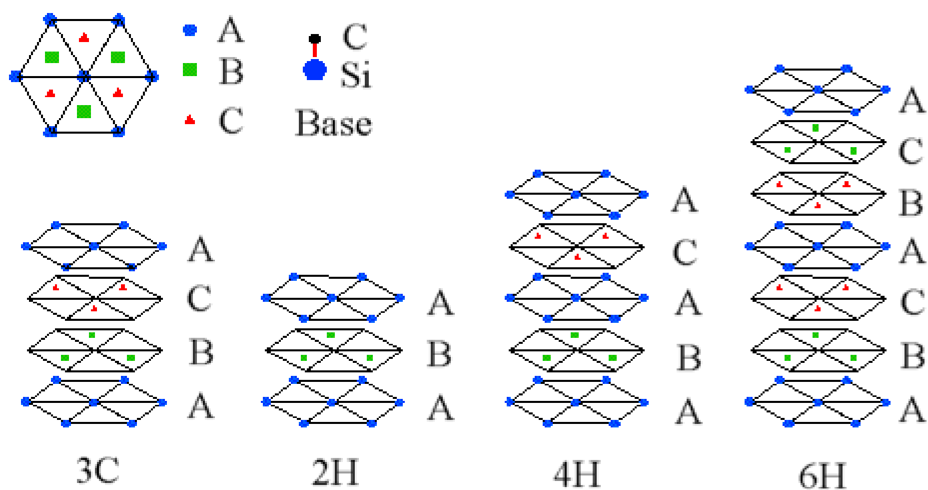



Figure 1 Molecular arrangement of various SiC Polytypes [4]

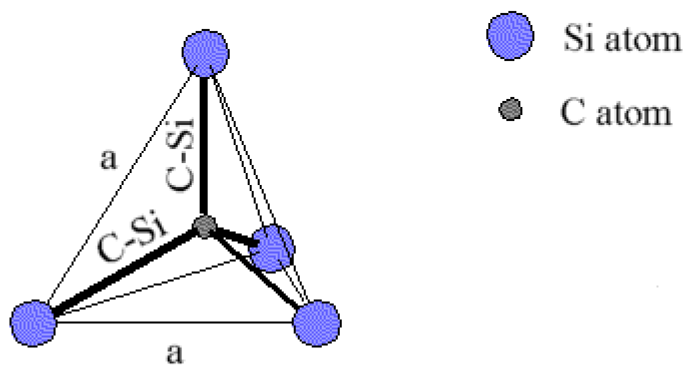



Figure 2 Unit cell representation of SiC –a = 3.8$A^o$ [4]

### *2.1.3 Current status of SiC devices*

For nearly a decade now, SiC devices have been available as prototypes. The reliability of the devices was very poor initially as expected. With the improvement in

wafer quality and device yield, reliability has also changed drastically. The list of early SiC device prototypes includes Schottky diodes, MOSFETs, JFETs, Static Induction Transistors (SITs) and the latest addition – BJTs [8,14,27,28,29]. The main players in this area are NASA Glenn, Cree, SemiSouth, Northrop Grumman, Rockwell Scientific, GE, Purdue University and SiCED. Given the immaturity of the technology and sometimes the potential applications/clients for this technology, the commercialization of SiC devices has been very slow. Cree's Schottky diodes are now available in the market in various current and voltage ratings. Cree's CSD20120D diode has a voltage rating of 1200V at 20A, the maximum operating temperature being quoted as $175^0$C. Cree is also actively involved in developing SiC BJTs, MESFETs and MOSFETs.

The most commonly available JFETs are normally ON devices that require a negative gate voltage to turn them off. They are considered viable SiC device for initial commercial success. This is because the oxide in SiC MOSFETs has been found to fail at a junction temperature $T_j$ of around $175^0$C. This rules out the MOSFET for high temperature applications, at least until progress is done in the oxide quality. But currently, SiC devices have spurned an interest because of their improved efficiency over Si devices rather than their high temperature capabilities.

Theoretically, SiC devices can operate even at 500-$600^0$C. Currently, it is difficult to realize operations at such temperatures mainly due to the limitations in the packaging. Polymer packages and lead based solder are ruled out for this temperature. Low Temperature Co-fired Ceramic (LTCC) is considered amongst the promising types of

packaging for SiC devices. But, LTCC packaging can drastically reduce the current handling capability of the devices. Therefore, very high temperature applications will have to wait till the packaging also evolves. Northrop Grumman is developing SITs that can be used as RF amplifiers in radars and other microwave applications. SemiSouth is actively involved in the development of rectifiers, JFETs and BJTs.

Other important devices such as Insulated Gate Bipolar Transistors (IGBT), Gate Turn Off transistors (GTO) etc. are still in the feasibility study/design stages and are not expected in the market in the next few years. Most of the devices are still too expensive and unreliable for mass production.

## 2.2 Vertical junction field effect transistor (VJFET)

### *2.2.1 Device structure*

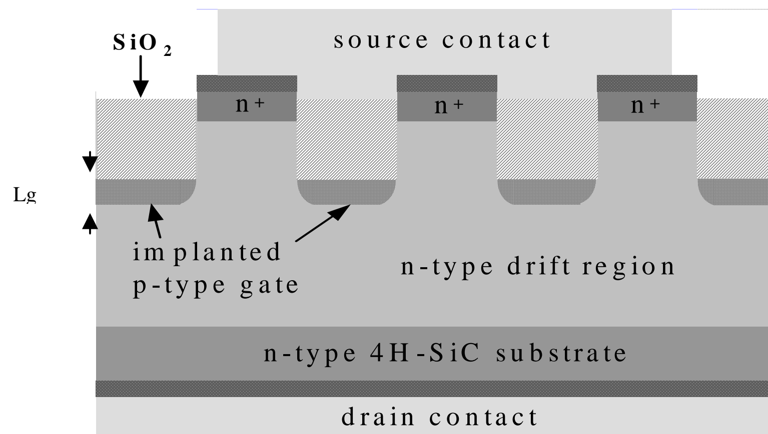



Figure 3 Cross section view of SiC VJFET

The cross-section of a Vertical channel JFET is shown in Fig. 3. As seen, the gates are recessed, and the conduction path is vertical (the high current carrying terminals, namely the source and the drain are placed on the top and bottom of the wafer respectively. This gives a higher packing density (as the chip area is greatly reduced) and many devices can be placed in parallel.

The circuit shown consists of a slab of an n-type SiC (n type channel) with p-type regions forming the gate. The device operation is based on reverse-biasing the pn junction between gate and channel. The reverse bias on this junction is used to control the channel width and hence the current flow from drain to source. The major role that the pn junction plays in the operation of this FET has given rise to its name: Junction Field Effect Transistor (JFET).

### *2.2.2 Device physics*

Consider an n-channel VJFET as shown in Fig. 3 above. When $V_{gs} >= 0$, the application of a voltage $V_{ds}$ causes current to flow from drain to the source. When a negative $V_{gs}$ is applied (reverse bias between gate and source), the depletion region of the gate-channel junction widens and the channel becomes correspondingly narrower, thus the channel resistance increases and the current $I_d$ (for a given $V_{ds}$) decreases. When $V_{ds}$ is small, the channel is almost of uniform width. The JFET is simply operating as a resistance whose value is controlled by $V_{gs}$. If we keep increasing $V_{gs}$ in the negative direction, a value is reached at which the depletion region occupies the entire channel. At this value of $V_{gs}$ the channel is completely depleted of charge carriers (electrons). This

value of $V_{gs}$ is defined as the threshold voltage of the device $V_t$, which is negative for an n-channel VJFET. For VJFETs, the threshold voltage is called the pinch-off voltage and is denoted by $V_p$.

Consider that $V_{gs}$ is held constant at a value greater (less negative) than $V_p$ and Vds is increased. Since $V_{ds}$ appears as a voltage drop across the length of the channel, the voltage increases as we move along from source to drain. It follows that the reverse-bias voltage between gate and channel varies at different points along the channel and is highest at the drain end. Thus the channel acquires a tapered shape and the $I_d$-$V_{ds}$ characteristic becomes non-linear. When the reverse bias at the drain end, $V_{gd}$ falls below the pinch-off voltage $V_P$, the channel is pinched off at the drain end and the drain current saturates.

With continued increase in $V_{ds}$ a voltage will be reached at which the gate-channel junction breaks down. This is the result of the charge carriers which makes up the reverse saturation current at the gate channel junction being accelerated to a high velocity and producing an avalanche effect. At this point, the drain current increases rapidly and the device may be destroyed. The normal operating region of the characteristics is the pinch-off region.

Unlike MOSFET, the depletion type SiC VJFET can’t be used in the enhancement mode by applying $V_{gs}>3$. If we attempt it, the gate-channel pn junction becomes forward biased and the gate ceases to control the channel [6].

The channel width can be controlled by the magnitude of $V_{gs}$. As $V_{gs}$ becomes increasingly negative, the channel width decreases. The on-state characteristics are dependent on the gate region design; specifically the channel width and gate implant depth $L_g$ (the distance from the surface to the deepest point that the implanted accepters penetrate) [7]. Depending on the gate depth in relation to the channel width, the structure can produce diode-like "triode" (Fig. 4) characteristics (short gate depths), FET-like "pentode" (Fig. 5) characteristics (long gate depths), or a combination of pentode and triode characteristics referred to as "mixed-mode" (Fig. 6) characteristics (intermediate gate depths).

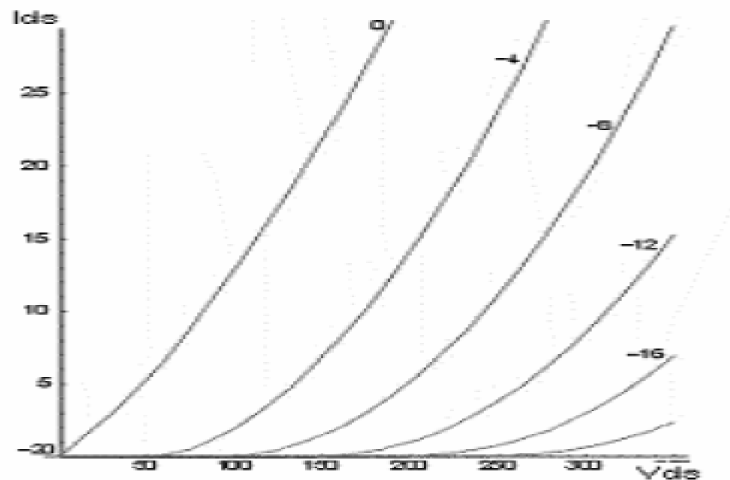



Figure 4 Triode Like DC characteristics of short channel VJFETs [7]

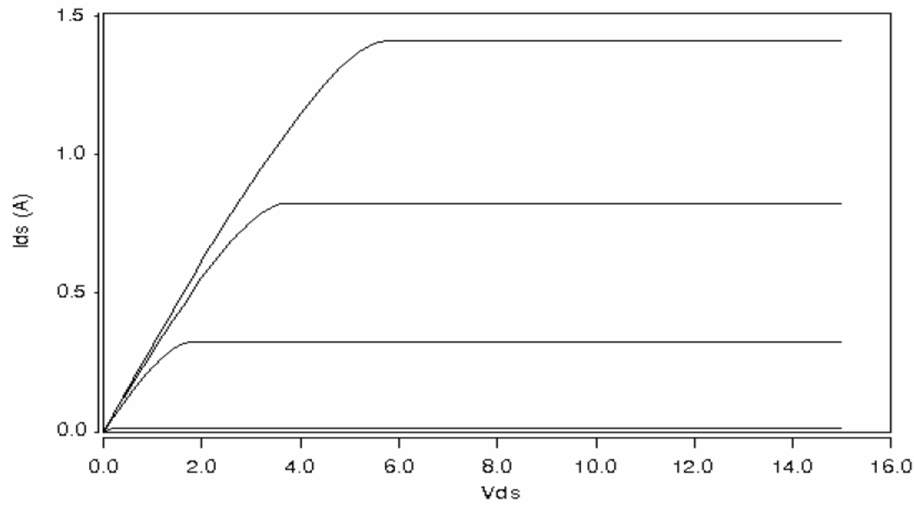



Figure 5 Pentode Like DC characteristics of long channel VJFETs [7]

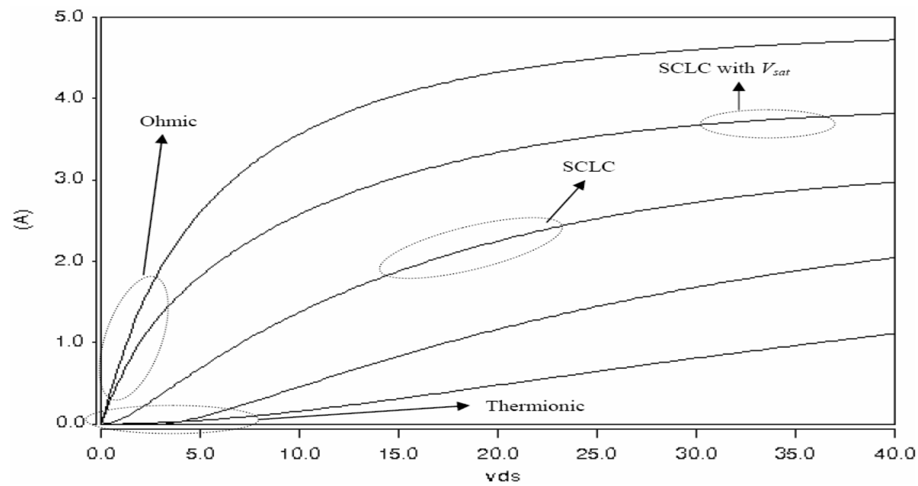



Figure 6 Different regions of operation of VJFET [7, 8]

Long channel JFETs exhibit pentode-like DC characteristics due to the drain current ($I_{ds}$) saturating at high drain voltages ($V_{ds}$). At higher $V_{ds}$, current saturation occurs, which is a strong function of the gate bias. In short-channel structures, the potential barrier established by the reverse gate-bias (off-state) extends over only small

vertical distances. As the voltage increases, the drain potential penetrates into the channel and lowers the potential barrier. Since the effect is exponential, the drain current is rapidly increased when the potential barrier is reduced. The pentode-like characteristics of a device increases the current handling capabilities, while the triode-like characteristics allow for high voltage blocking capability. Therefore, for devices optimized for power switching applications, the device exhibit mixed-mode characteristics [7]. For sufficiently negative gate voltages when the channel is "pinched off" due to the intersecting depletion regions, the mixed-mode characteristics may be described by the thermionic emission theory when the device operates in triode region at low currents. As $V_{ds}$ is increased, these structures produce the typical linear and saturation regions.

If the gate structure is designed with a small channel length compared to the channel width, the JFET characteristics are altered. Thus, a good power JFET contains a mixture of both sets of characteristic curves.

The mixed mode characteristics of this structure can be broken into four regions of operation as seen in Fig. 6 – (i) ohmic (ii) thermionic (iii) space charge limited current (SCLC) and (iv) SCLC with velocity saturation ($V_{sat}$) [8] depending on the gate design. Ohmic behavior is seen for less negative values of Vgs and thermionic effects are more dominant for more negative gate biases.

Real SiC VJFETs developed by different groups around the world today often exhibit complex (non-ideal) I-V characteristics influenced by some or all of the effects

described above. Device models for circuit simulators should incorporate this complexity in order to realistically predict the circuit behavior.

## 2.3 Circuit simulator

### *2.3.1 Introduction to simulators*

The behavior of semiconductor devices has to be accurately replicated in device models for circuit simulation. Simulation has become an indispensable part of application development as it greatly reduces the time, effort and expense required for building and testing circuits. As an example, it is estimated that the IGBT model developed at NIST has reduced Ford's annual cost of IGBT electronic ignition system design by $232,000 per year and that design improvements due to the use of the NIST IGBT model have reduced the production cost of Ford electric vehicle propulsion systems by $100 per vehicle [30].This leads to a faster turn around in production and a cheaper product. Models can be written in various languages depending on the simulator in which they have to be used.

PSpice is the most popular simulator among circuit design engineers. Custom device models for PSpice need to be written in C/C++. Hardware Description languages (HDLs) are also used to build model for some simulators like System Vision and Spectre. To build a model in PSpice requires much more efforts in comparison to HDLs because it requires a significant amount of simulator specific details. The PSpice code is very complex and includes Jacobian entries, matrix stamps and derivative information.

However, due to the wide acceptance and usage of PSpice we choose to develop the SiC VJFET model in PSpice. Further Information on PSpice Simulator can be referred from Appendix A. Table 2 below gives some of the popular languages in which semiconductor device models are created in their associated simulators.

Table 2

Languages and their associated simulators.

| **Language** | **Simulator** |
|---|---|
| C | PSpice |
| Verilog-A | Spectre |
| VHDL-AMS | SystemVision |
| MAST | Saber |

# CHAPTER III

# SIC VJFET MODEL DEVELOPMENT APPROACH (PSPICE SIMULATION)

## 3.1 Semiconductor device modeling

### *3.1.1 Different modeling techniques for semiconductor devices*

There are many modeling techniques available for developing device models. Some of the methods are as follows:

- Subcircuit Models
- Numerical Models
- Physics-based Models
- Hybrid Models
- Empirical Models

These modeling approaches vary widely according to the accuracy of the results and the computational cost. Subcircuit models use existing elements (voltage and current sources, resistors, diodes and other standard available models) to generate new device models. Subcircuit models are easy to write and compile and are also readily available as simulator libraries, but they have high complexity which results in very slow simulation speed, poor convergence and lower accuracy.

Numerical models use finite element analysis (FEA) of the physical processes that occur in the device. They provide very accurate results and are generally used for understanding the physics of the device. However, numerical methods are computationally expensive as they may take many hours to converge and find optimum solutions. Therefore, they are impractical to be used as models for circuit design. The parameters for such models are design and process specific and most often would be proprietary to the organization making these devices, thus making them unavailable to the circuit designer.

The core of the Physics based models is characteristic device equations that are derived using physical conditions or observations such as mobility of carriers, junction capacitances, channel modulation etc. A set of differential algebraic equations (DAEs) can be derived which can be implemented for device modeling. Such models have high computational efficiency. These models require extracting the parameters using electrical measurements which increase the cost of modeling and the time to market [11,12].

Hybrid models employing numerical techniques and analytical expressions are also possible, but they are not widely used for circuit simulations as they have the same disadvantage of numerical models.

Another widely used method is referred to as empirical modeling. Empirical models are considered ‘behavioral’ models as their main intention is to replicate the behavior of the devices at the terminals. They have very good accuracy. They converge well and are computationally efficient [11,12]. Empirical approach does not require extracting the parameters using electrical measurements which are very cost effective and also have fast time to market.

Developers of compact device models frequently have to grapple with the decision of making their models empirical or physical. While academicians say that only physical models can accurately predict the characteristics of semiconductor devices, circuit designers tend to be more flexible. Models are aimed at circuit designers and they tend to employ those models that converge easily and have less computational time. Other factors like ease of parameter extraction play an important role in the choice of models. Therefore, it is very difficult to pinpoint one method of modeling to be absolutely superior to the others. The table below shows the comparison of different modeling techniques.

Table 3

Comparison of modeling techniques against various parameters [12]

| | Accuracy | Computational Efficiency | Parameter Extraction | Development Time |
|---|---|---|---|---|
| Sub-circuit Models | Average for IC's, poor for power devices | High | Average | Fast |
| Empirical Models | Average to high | High | Average | Fast |
| Numerical Models | Very high | Poor | Poor | Slow |
| Physics based Models | High | High | Good | Average |
| Hybrid Models | High | Average | Poor | Slow |

### *3.1.2 Modeling Methodology*

While different methodology such as those shown above can be used according to particular application, the modeling methodology remains the same. Fig. 7 shows a flowchart showing all the different stages of modeling devices. Basically the whole methodology can be divided into three broad areas: (i) understanding the device physics, developing equations and implementing them in a language of choice (ii) extraction of the parameters of the device equations (iii) validating the model by comparing the simulated values with the experimental data.

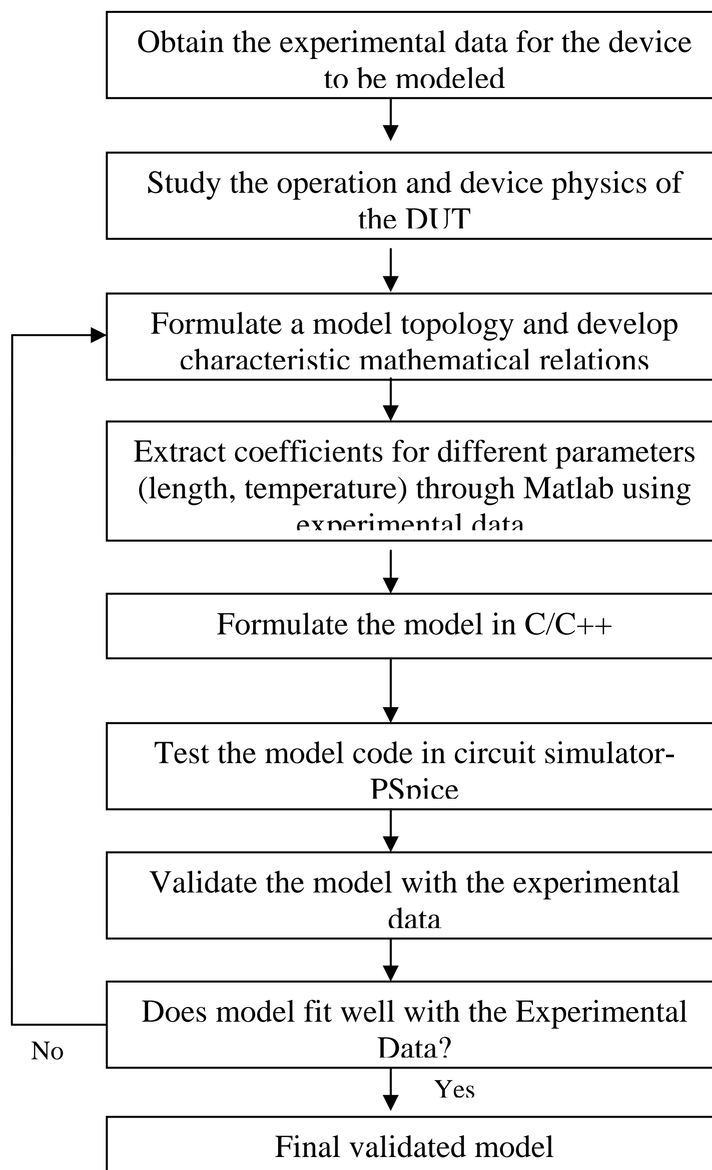



Figure 7 Flowchart showing the Modeling Methodology

### *3.1.3 Interpolation Technique*

The experimental data may be available at some known values of parameters (temperature, width, etc.). However, for the successful implementation of the model, it is

essential that the model should be able to accurately predict the device characteristics for continuum of the parameter’s values. For this purpose, an interpolation technique is implemented in our model. The technique that is used for interpolation in our model is Bi-cubic Spline. The other interpolation technique that is having the same accuracy as Bi-Cubic Spline is Bicubic Interpolation. The reason for choosing the Bi-Cubic Spline is that this method doesn’t require pre computation of the derivatives of the function at the grid points as is the case in the Bicubic interpolation.

The basic working of the Bicubic Spline can be understood by referring to Fig. 8.

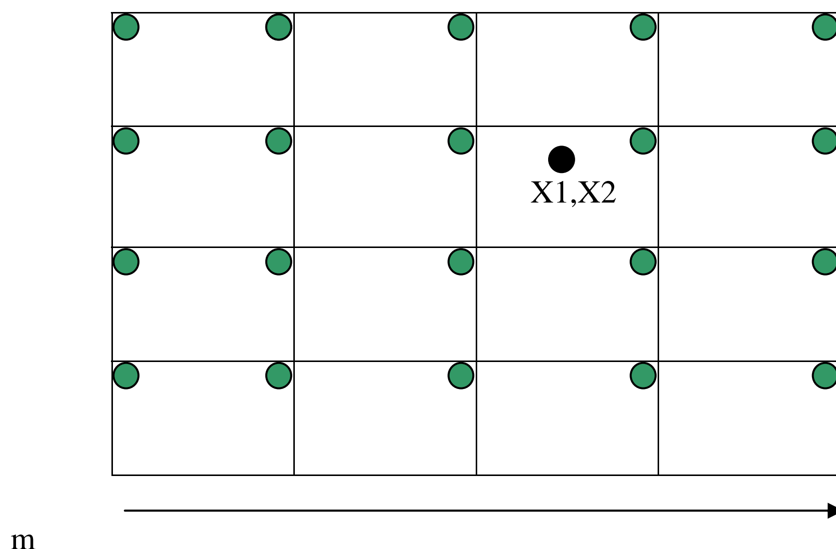



Figure 8 Bicubic Spline Interpolation

X1, X2 is the point at which the interpolation has to be found. The green circles are the known parameter values. Bisection method is used to find the location of the point (X1, X2) in the grid. To interpolate one functional value, we perform m one-dimensional splines across the rows of the table, followed by one additional one-dimensional spline

down the newly created column. In other words, after obtaining the location of X1, functional values are calculated along the rows. Using these functional values, derivatives are calculated along this newly formed line. The process is repeated and the location of X2 is determined and the value of the function is obtained at the grid point (X1, X2). The interpolation has been extended for multi- dimensional interpolation so that any number of parameters can be used [19].

### *3.1.4 Modeling in PSpice*

The SiC VJFET model described in this thesis is implemented in PSpice using Device Equations Developers Kit (DEDK), which is separate software available for the extension of PSpice models. The DEDK program includes the PSpice source code constructed in C/C++ high level language for the device model subroutines which can be modified to include new models. The source file becomes the input to the PSpice simulator. Once a device has been described in C/C++, the behavior of the model can be simulated with the PSpice simulator.

One of the limitations of the device equations is that it does not allow the addition of entirely new device. However, the same thing can be achieved by making use of any existing device. There is a parameter named 'LEVEL' in PSpice which can be extended and any number of devices can be added to the LEVEL. By referring different LEVELS, different devices can be accessed.

Important files that are used to develop our model in PSpice can be referred from Appendix B.

### *3.1.5 Modeling the SiC VJFET*

The SiC VJFET is to be primarily used as a power switch. The model should therefore accurately predict both the DC and the transient characteristics. An empirical modeling approach was used for modeling SiC VJFET. An empirical Angelov Model was used [13]. The model was selected because of its potential to provide better computational efficiency, development time, and accuracy in modeling non-ideal device behavior. The model equation has a hyperbolic tangential function for the DC and transient characteristics which help in better curve fitting with the experimental data.

### *3.1.6 Angelov Model Description*

The equivalent circuit model for a transistor using the Angelov Model is shown in Fig. 9 [13].

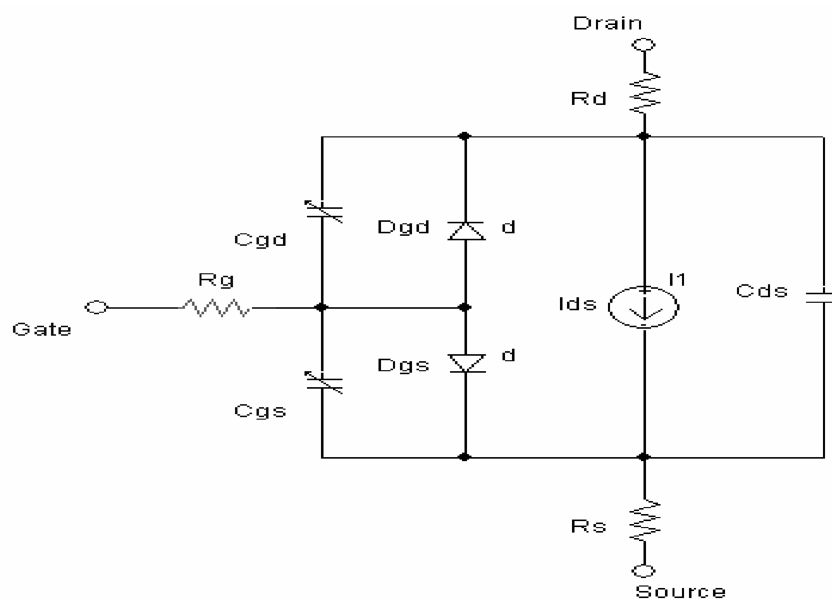



Figure 9 Equivalent circuit representation of SiC VJFET large signal model [13]

Resistances $R_d$ and $R_s$ represent source resistance and drain resistance respectively. $R_g$ is the gate resistance. There are capacitances between the three terminals. The gate-source capacitance $C_{gs}$ and gate-drain capacitance $C_{gd}$ are depletion area capacitances and they are modeled with charge sources $Q_{gs}$ and $Q_{gd}$. The values of the two capacitances depend on the applied voltage. Drain-source capacitance $C_{ds}$ is the geometrical capacitance whose value is dependent on cross sectional area but is independent of the applied voltage.

Ideally, the gate is isolated from the channel by the depletion region, and there is no significant conduction through the gate terminal. When the gate-drain or gate-source is forward biased, there may be a current through the pn junction. On the other hand, a large enough negative voltage between the gate and any other terminal causes an avalanche breakdown in the depletion region thus creating electric current through the gate. The avalanche breakdown is not implemented in our model. The gate conduction is included in the model as two controlled current sources, one between the gate and source and the other between the gate and drain. The sources are represented by pn junction models.

The Angelov model simulates the non-linear properties of the VJFET using a unique set of mathematical equations. These nonlinear properties can be related to elements of the equivalent circuit. The main nonlinear elements of the equivalent circuit are the following:

- The drain-source current $I_d$ controlled by voltages $V_{gs}$ and $V_{ds}$.
- The gate-source capacitance $C_{gs.}$
- The gate-drain capacitance $C_{gd.}$
- The diodes between gate-source ($D_{gs}$) and gate-drain ($D_{gd}$). [13,14,15]

### *3.1.7 Modeling of DC characteristics by Angelov Model*

#### ***3.1.7.1 Description of the Drain Current Model***

The drain current function is expressed as:

$$I_{ds}[V_{gs}, V_{ds}] = I_{da}[V_{gs}]\, I_{db}[V_{ds}] \qquad (1)$$

The $I_{db}$ [$V_{ds}$] term is the same as in the well-known Curtice and Statz model [15] [16]. The term $I_{da}$ [$V_{gs}$] in the Angelov Model is different from Curtice and Statz model. The hyperbolic tangent (tanh) dependence of this term provides much better fitting of the $V_{gs}$ dependencies in comparison to other models reported in literature.

The expression for the drain current is:

$$I_{ds} = I_{pk}.AFAC.\,(1+\tanh(\psi))(1+\lambda.V_{ds})\tanh(\alpha.V_{ds}) \quad [13] \qquad (2)$$

Where

$$V_{gr} = V_{gs} + b1.\,(V_{ds} - V_{db}) + b2.\,(V_{ds} - V_{db})^2 - V_{pk}$$

$$\Psi = p1.\, V_{gr} + p2.V_{gr}^2 + p3.\, V_{gr}^3$$

Where $I_{pk}$ is the drain current at which transconductance is maximum with the contribution from the output conductance subtracted, λ is the channel length modulation parameter and α is the saturation voltage parameter, $V_{pk}$ is the gate voltage for the

maximum transconductance, $V_{db}$ is the sub threshold voltage parameter and p1, p2, p3 are the polynomial coefficients.

All these model parameters are extracted by using non-linear fitting in Matlab using the drain current equation described above and the experimental data for different temperature and device dimensions.

### *3.1.7.2 Description of the Gate Current Model*

The gate current that would flow under forward bias or under breakdown conditions between gate-source and gate-drain is given by:

$$I_{gs} = I_s . (\exp (V_{gs}/ (N.V_{th}))-1) - I_{bo} . (\mathrm{Exp} (-(V_{gs}+V_{bd}) / (N_r.V_{th}))) \quad [17] \qquad (3)$$

$$I_{gd} = I_s . (\exp (V_{gd} / (N.V_{th}))-1) - I_{bo} . (\mathrm{Exp} (-(V_{gd}+V_{bd}) / (N_r.V_{th}))) \quad [17] \qquad (4)$$

$$I_g = I_{gs} + I_{gd} \qquad (5)$$

Where $I_{gs}$ is gate-source current, $I_{gd}$ is gate-drain current, $V_{gs}$ is the gate-source voltage, $V_{gd}$ is the gate-drain voltage, $I_{bo}$ is breakdown saturation current, $I_s$ is diode saturation current, N is diode ideality factor, $N_r$ is breakdown ideality factor, $V_{bd}$ is breakdown voltage, $V_{th}$ is thermal voltage.

The first term in the equations (3) and (4) is forward conduction current and the second term is the breakdown term.

As per Kirchoff's Current Law (KCL)

$$I_s = I_{ds} + I_{gs} \qquad (6)$$

### *3.1.8 Switching Characteristics*

In order for the complete large signal model to be implemented, it is essential that the capacitance-voltage relationship must also be included in the switching model. The same type of modeling functions as in DC analysis (tanh) was chosen to model the dependencies of $C_{gs}$ and $C_{gd}$ on gate and drain voltage:

$$C\,[V_{gs}, V_{ds}] = C_a\,[\tanh(V_{gs})]\; C_b\,[\tanh(V_{ds})] \tag{7}$$

The expression used for the gate-source and gate-drain capacitance is given by:

$$C_{gs} = \mathit{AFAC.CGSO}.\ (1+\tanh(\varphi_2))\,(1+\tanh(\varphi_1)) \quad [13] \tag{8}$$

Where

$$\Phi_1 = p_{10} + p_{11}\,(V_{gs})$$

$$\Phi_2 = p_{20} + p_{21}\,(V_{ds})$$

$$C_{gd} = \mathit{AFAC.CGDO}.\ (1+\tanh(\varphi_3))\,(1 - p_{400}\,(\tanh(\varphi_4)) \quad [13] \tag{9}$$

Where

$$\Phi_3 = p_{30} + p_{31}\,(V_{gs})$$

$$\Phi_4 = p_{40} + p_{41}\,(V_{ds})$$

The corresponding Charge functions are as follows:

$$Q_{gs} = \mathit{AFAC.CGSO}.\ (1+\tanh(\varphi_2))(V_{gs} + (1/p_{11})\log(\cosh(\varphi_1))) \quad [18] \tag{10}$$

$$Q_{gd} = \mathit{AFAC.CGDO}.\ (1+\tanh(\varphi_3))(V_{dg} - (p_{400}/p_{41})\log(\cosh(\varphi_4))) \quad [18] \tag{11}$$

Where $V_{gs}$ is the gate-source voltage, $V_{dg}$ is the drain-gate voltage, CGSO is the gate-source capacitance parameter, CGDO is the gate-drain capacitance parameter, AFAC is the gate width scale factor, $p_{10}$, $p_{11}$, $p_{20}$, $p_{21}$, $p_{30}$, $p_{31}$, $p_{40}$, $p_{41}$, and $p_{400}$ are the polynomial coefficients.

These equations are used to model the switching characteristics. The capacitances due to the depletion region ($C_{gs}$, $C_{gd}$) are the main component of the model of the transient response. The parameters in the capacitance equations are extracted using Matlab. All the above equations are implemented in C/C++ and included in the PSpice circuit simulator.

CHAPTER IV

# VALIDATION RESULTS

## 4.1 Introduction

The SiC VJFET test data from PSpice simulations have to be compared against measured data from devices in order to validate the model. All the characteristics of the actual test circuit have to be duplicated in the PSpice simulator to get accurate results. Test circuits were implemented for DC and transient simulation using the schematic option of PSpice. Different simulations can be done using this test circuits to study different VJFET characteristics. In the following section, the validations of this model are explained.

## 4.2 Model Validation

### *4.2.1 DC Analysis*

This section discusses the test circuit and the DC waveforms for the model validation of SiC VJFET.

#### *4.2.1.1 DC test circuit*

The test circuit used for simulating the DC characteristic is shown in Fig. 10 There are two independent voltage sources - $V_{ds}$ (drain to source voltage) and $V_{gs}$ (gate to

source voltage). DC measurements are done at steady state and therefore the parasitic elements are neglected in simulation (i.e, capacitances behave as open circuit while inductances behave as short circuit in DC analysis. However, they are included in the switching simulation.

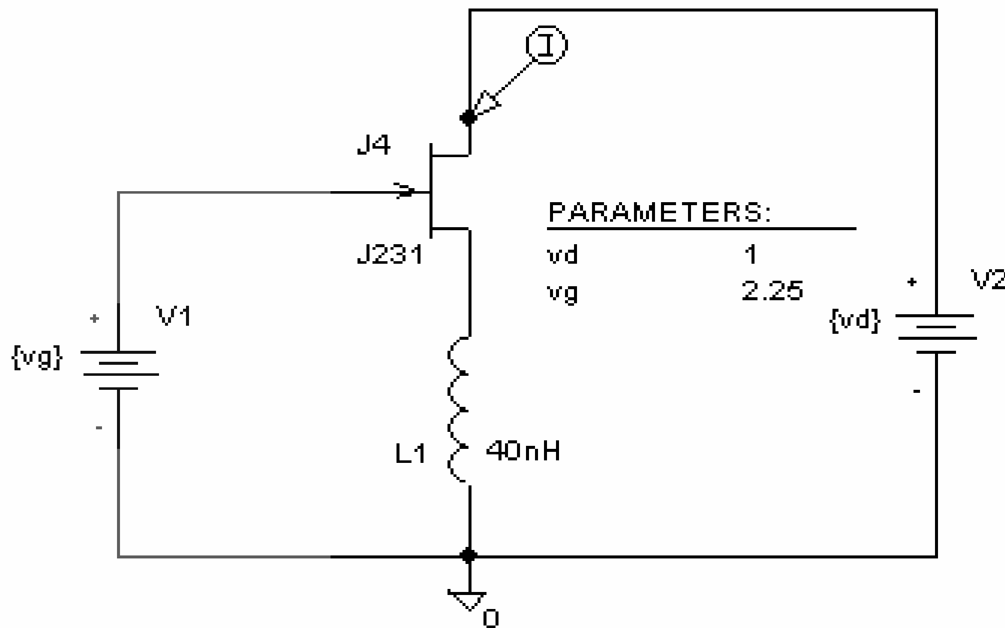



Figure 10 Test bench for DC measurement [22]

#### *4.2.1.2 <u>Drain current vs. Drain voltage for high values of current</u>*

For each value of $V_{gs}$, the $V_{ds}$ is swept and families of curves are obtained and compared with the measured data. Here, $V_{ds}$ is swept from 0 to 15 V and a family of curves is plotted for $V_{gs}$ varying from 0 to +3V. Fig. 11 compares the simulated and measured Drain current-Drain Voltage characteristics for high values of current. As can be observed from the plot, the simulated data accurately replicates the linear and saturation region of the SiC VJFET.

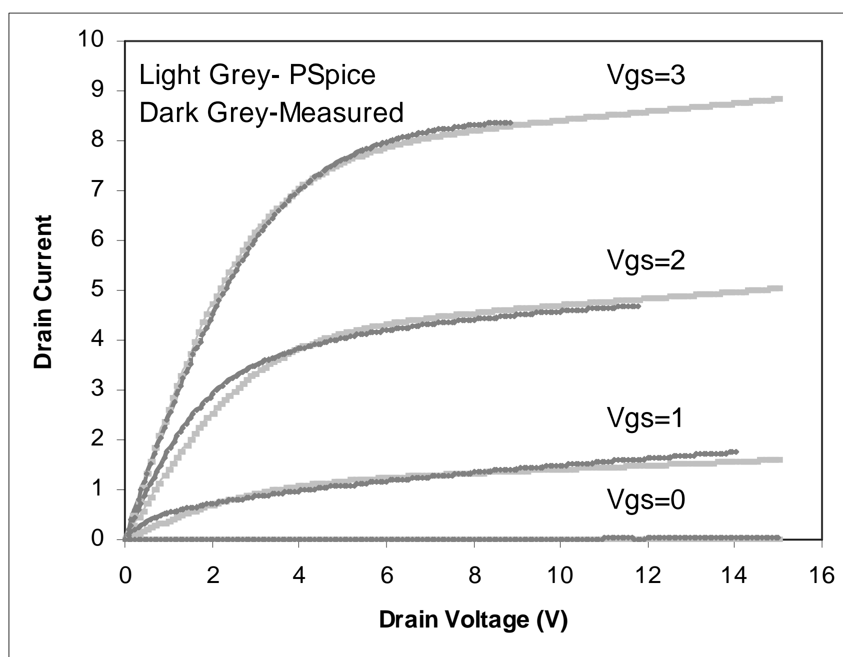



Figure 11 SiC VJFET PSpice simulated (light grey) and measured (dark grey) drain current drain voltage waveforms for high current at different gate voltages

These results were also compared with the simulation reported in Ref. 14. The simulated results were in much better agreement with measured data in our case compared to Ref.14.

#### *4.2.1.3 Drain current vs. Drain voltage for high values of voltage*

In this case, $V_{ds}$ was swept from 0 to 300V while $V_{gs}$ was varied from -4 to -1V. The compliance was set to 50uA. Fig. 12 compares the simulated and measured drain current-drain voltage characteristics for high voltage.

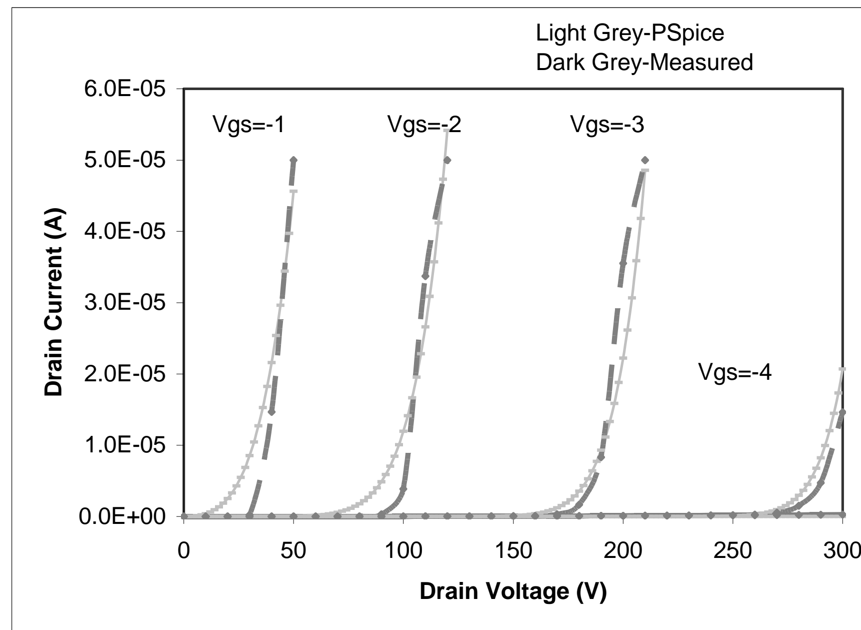



Figure 12 SiC VJFET PSpice simulated (light grey) and measured (dark grey) drain current drain voltage waveforms for high voltage at different gate voltages

As seen, the model reasonably well replicates the drain current-drain voltage characteristics even for very high voltages.

#### *4.2.1.4 <u>Gate current ($I_{gs}$) vs. Gate voltage ($V_{gs}$)</u>*

Simulation of the gate current is a challenging part of any VJFET model development since this current may cause significant deviation from the ideal transistor characteristics provided by analytical models. Fig. 13 compares the measured and simulated gate current-gate voltage characteristics for the gate voltage for the voltage range when the diode is reverse biased (-30V) to the values when it becomes forward biased (3V).

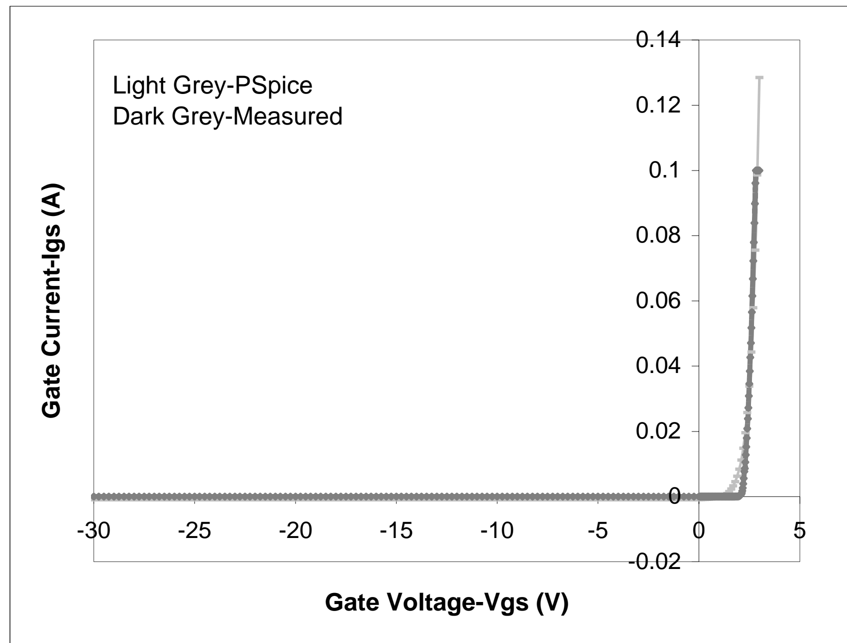



Figure 13 SiC VJFET PSpice simulated (light grey) and measured (dark grey) gate current-gate voltage waveform

Referring to Fig. 13, it can be said that the model accurately models the current flowing through the diode for forward bias when accurate modeling of this current is important for circuit simulation.

### *4.2.2 Incorporation of parameters in the model*

A functional PSpice model should provide user with a possibility to vary the most important parameters related to device design and operation conditions such as geometrical dimensions, temperature, etc. As mentioned before, any number of parameters (temperature, finger width, etc.) can be incorporated in our model using multi dimensional interpolation technique.

#### ***4.2.2.1 Drain Current vs. Temperature***

SiC VJFETs are attractive option for high power applications under low as well as high temperatures and high radiation environment. An experimental investigation of the effects of the temperature on the DC and the switching performance of the SiC VJFETs for temperature range from 390K down to as low as 30K was reported in our previous paper [5]. However, the temperature dependence is rather complex and its accurate modeling with a physics-based model would require a significant insight in the device physics at different temperatures. An interpolation of the experimental characteristics was included in our Angelov PSpice model to enable temperature dependence, which is for the first time to our knowledge. This would give circuit designers ability to predict circuit behavior at different temperatures.

Fig. 14 compares the experimental and simulated Drain Current versus temperature characteristics. The experimental data was measured for temperatures from 30 to 370 K with a step of 20K for drain voltage=0.2V, gate voltage=0.5V. PSpice simulations were conducted for arbitrary temperatures covering the experimental temperature range for different bias conditions. Entire families of I-V characteristics can be simulated for arbitrary temperatures.

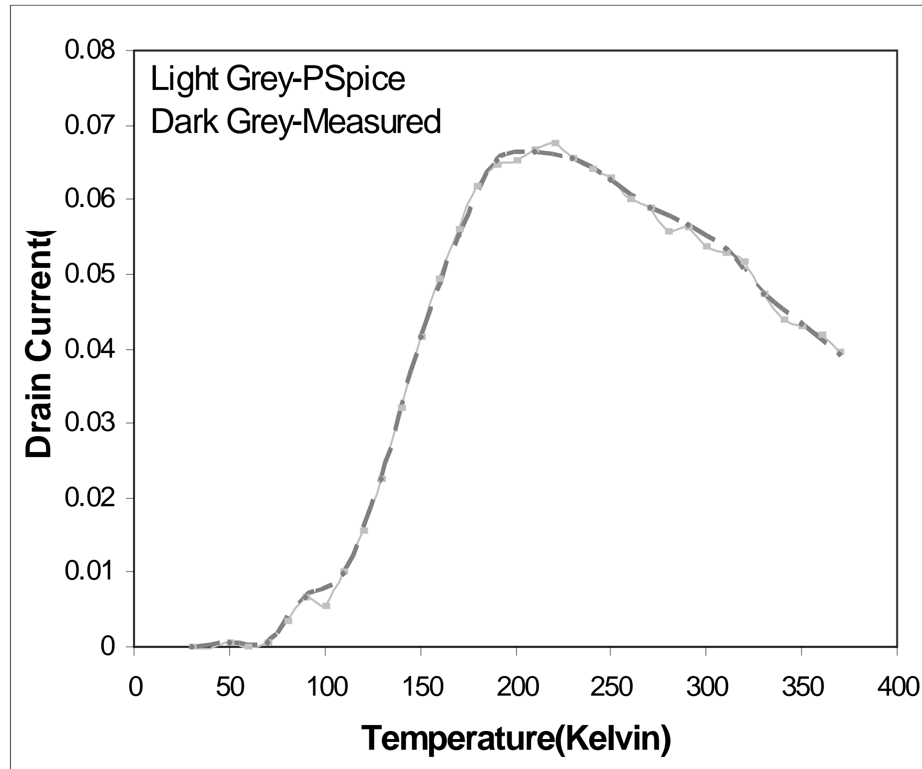



Figure 14 SiC VJFET PSpice simulated (light grey) and measured (dark grey) drain current-temperature waveform for drain voltage=0.2V and gate voltage=0.5V

The experimental and simulation data were found to be in good agreement with each other. The results show that the model is capable of emulating the device behavior at any temperature value in the given range (30K – 370K).

#### *4.2.2.2* ***Drain Current vs. Finger Width***

Another important requirement is a possibility to vary certain device dimensions as parameters of the model. One of the important parameters of SiC VJFET is finger width. Fig. 15 compares the Medici Simulation and PSpice simulation results for drain current-

finger width. The Medici simulation was done for Finger width from 1.2 μm to 1.4 μm with a step of 0.1 μm with gate voltage and drain voltage equal to 2V and temperature equal to 473K. PSpice simulation was done with a smaller step of 0.02 μm for the same bias voltage and temperature. PSpice simulation accurately replicates device behavior predicted by Medici Simulation. For this parameter, the dependence of the I-V characteristics is a linear. However, the same approach was used to implement this dependency as the one used to implement for temperature dependency. Due to the absence of experimental results for this parameter, validation of this part of the model is left for the future work.

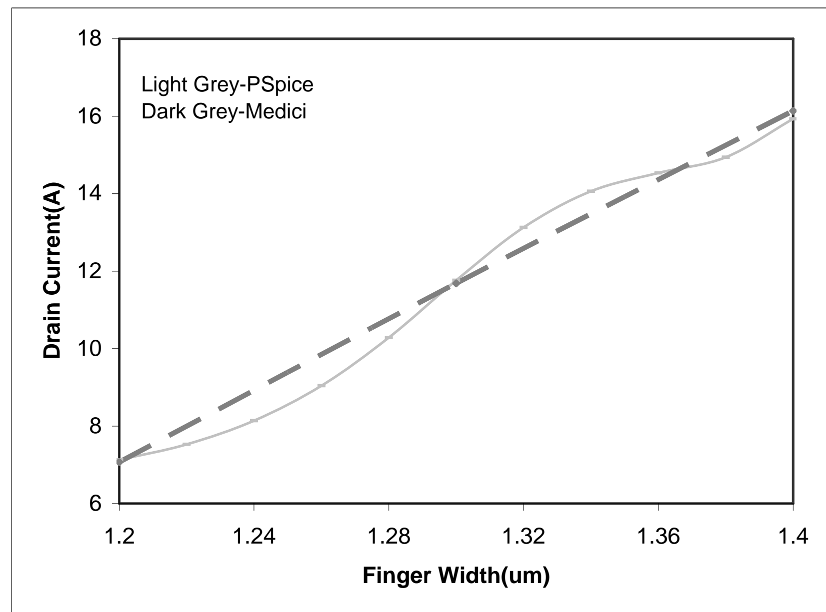



Figure 15 SiC VJFET PSpice simulated (light grey) and Medici (dark grey) drain current-finger width waveform for drain voltage=2V, gate voltage=2V, and temperature=473K

### 4.2.3 *Transient Analysis*

When analyzing circuits, circuit designers are usually interested in finding the response of the circuit to a given input signal as a function of time. This analysis mode is referred as transient analysis. A working device model should be capable of doing accurate DC and transient analysis.

#### 4.2.3.1 ***Switching test circuit***

For validating the model's switching performance, the experimental switching data were obtained on real VJFET devices developed by MSU and SemiSouth, Inc. The switching waveforms for $V_{ds,}$ $V_{gs}$ and $I_{ds}$ of SiC VJFET were measured at Center for Advanced Vehicular Systems (CAVS) at MSU using the test circuit shown in Fig. 16. The test circuit and the procedure that was followed for the experimental measurements are described in JEDEC standard JESD24 [25]. A gate pulse of –10 to +3V and a drain voltage equal to 50V is applied to the test circuit. $R_d$ (R14) is set for the rated current $I_{dss}$ (rated drain current) to flow through the device at drain voltage of 50V. $I_{dss}$ is measured at $V_{ds}$=2V and $V_{gs}$=3V. This value of $V_{gs}$ allows for maximum forward conduction. The industry standard for commercial FET devices marks the $I_{dss}$ at $V_{ds}$=2V. The convention for measuring the rise and fall times is 10-90% and 90-10% respectively.

The test circuit is used for PSpice switching simulation is shown in Fig. 16. A source inductance has been added in the test circuit to take into account the inductance due to wires, which is believed to be present in the device under test. The value of source inductance used in the simulation is 40 nH. This value was chosen by simulating the

switching characteristics for different source inductances and comparing with the experimental results. The reason for suspecting inductance as an important component of the test circuit was as follows – the value of the depletion capacitances that were obtained through experimental measurements were in pF. However, the measured switching times were in ns, which is too long to be explained solely by the influence of the capacitances. In order to resolve this discrepancy, the existence of the other circuit parameters has to be assumed. The two additional parameters that can contribute to switching time are series resistance of the diode in ECM and the inductance present in the device under test. Series resistance was calculated by including series resistance (rs) in the diode equation. The diode equation with series resistance can be written as:

$$I = I_o\,(e^{q(V-Irs)/nKT} - 1) \tag{12}$$

Where V is the measured voltage across the entire diode, $I_o$ is the reverse saturation current, n is the ideality factor and rs is the series resistance. Eq. 12 can be transformed as

$$I\,(dV/dI) = Irs + nKT/q \tag{13}$$

A plot of I (dV/dI) versus I gives series resistance (rs) as the slope [26]. The resistance was found to be around 2.5 ohms. The series resistance has a very small value which would not affect switching response significantly. Therefore it was inferred that it is the inductance of the wires along with the capacitances that is contributing to switching time. Prior experience with accounting for inductance in similar circuits also supports this suggestion as reasonable.

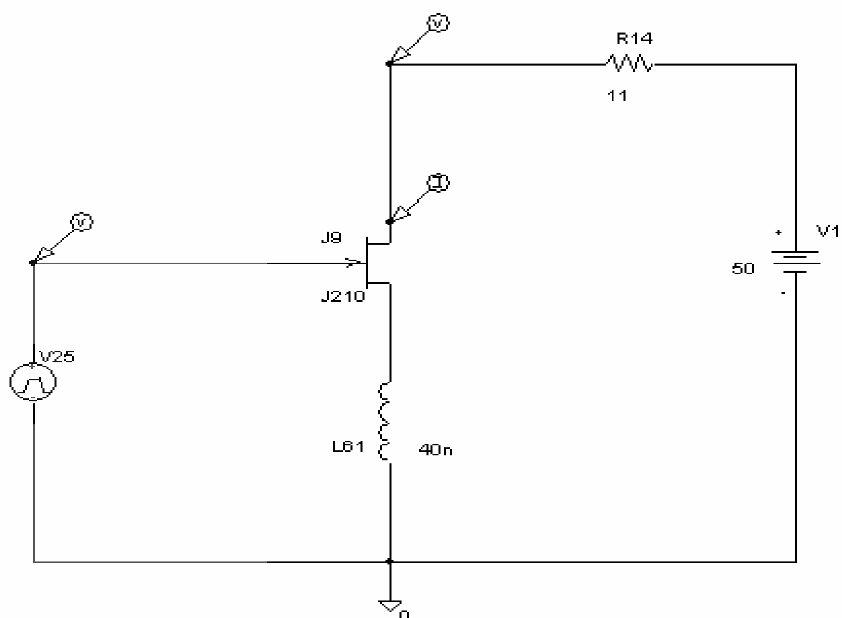
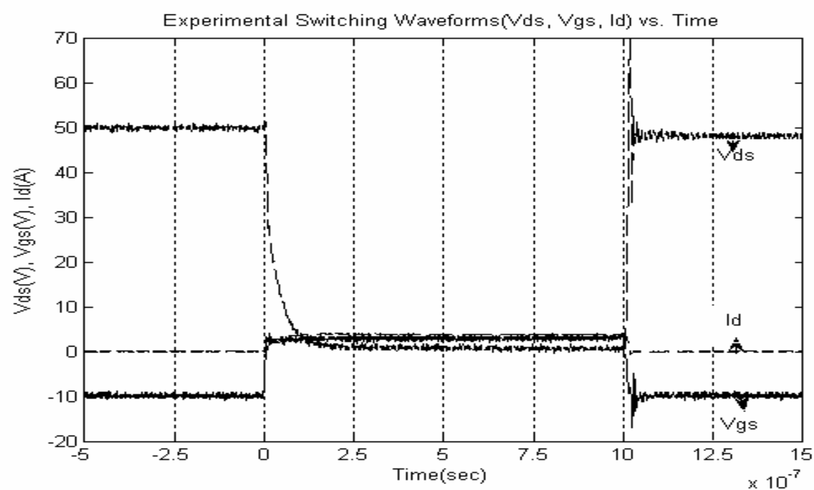


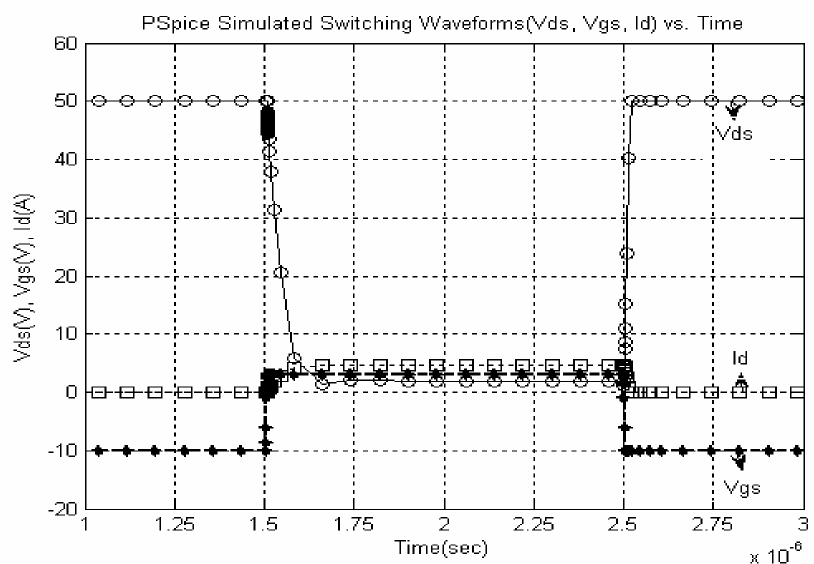

Figure 16 Test bench for transient analysis [22]

### *4.2.3.2* ***Switching Waveforms***

The switching waveform obtained from the experimental measurements and PSpice simulations using our model is shown in Fig. 17. Each waveform in Fig. 17 shares a common zero, identified by the value of $I_d$ during the time at which the device is blocking ($V_{gs}$ = -10V).




(a)




(b)

Figure 17 Switching Waveforms for drain voltage (Vds), drain current (Id), and gate voltage (Vgs) for (a) Experimental (b) PSpice simulation

The switching characteristics can be described by the various capacitances between the various internal nodes of the model. The switching waveform in Fig. 17 can

be described by the depletion capacitances $C_{gs}$ and $C_{gd}$. During the initial rise of gate voltage, the $C_{gs}$ and $C_{gd}$ starts to charge yielding the initial slope in $V_{gs}$. $C_{gs}$ needs to be charged up to threshold voltage before the VJFET begins to turn on. As $V_{gs}$ exceeds the threshold voltage, the VJFET begins to turn on and $V_{ds}$ begins to fall and drain current starts flowing. Now, $C_{gd}$ begins to be discharged as well as $C_{gs}$ being charged so the time constant is increased and the gradient of $V_{gs}$ is reduced. As $V_{ds}$ becomes less than $V_{gs}$, the value of $C_{gd}$ increases as it is depletion dependent. The gate resistance is kept zero as it would also contribute to the slope. The higher the gate resistance, the more time it takes to charge the capacitances which results in slower switching response.

The source inductance added in the circuit results in higher impedance which results in slower switching waveform. This inductance causes a negative feedback effect during switching. The increase in drain current results in higher voltage drop across inductance. This will oppose the build up of current in the VJFET resulting in slower turn on switching response compared to turn off response.

The experimental and simulated switching data has been shown in Table 4

Table 4

Comparison of Experimental and PSpice simulation switching data

| | $V_{gs}$ (V) | $I_d$ (A) | $V_{ds}$ (V) | $t_r$ (ns) | $t_f$ (ns) |
|---|---|---|---|---|---|
| Experimental | 3/-10 | 4.54 | 50 | 68 | 19 |
| Simulation | 3/-10 | 4.4 | 50 | 74 | 16.5 |

As it can be seen by comparing Fig. 17(a) and 17(b) and observing Table 4, the simulated and experimental waveforms are in good agreement qualitatively and quantitatively.

# CHAPTER V

# ANALOG CIRCUIT BUILDING BLOCKS

## 5.1 Analog Circuit Building Blocks

This section is the first attempt to apply the new PSpice model of SiC VJFET to predict behavior of the basic building blocks of analog circuits that are normally used to build more complicated analog circuits at later stages. These basic building blocks are used in this work to provide a preliminary demonstration of the capabilities of our model via comparing qualitatively simulated performance of the circuits using the new SiC VJFET model and the standard Si JFET device model available in the PSpice. Si JFET simulation is done to serve as a reference waveform.

The circuits included in this study are:

- Voltage Follower
- Common Source Amplifier
- Current Source
- Differential Amplifier

Small signal analysis of these circuits can be referred from [20] [21].

### *5.1.1 Voltage Follower*

A voltage follower is a circuit, which is used as a buffer amplifier having a unity voltage gain. The voltage follower circuit is shown in Fig. 18.

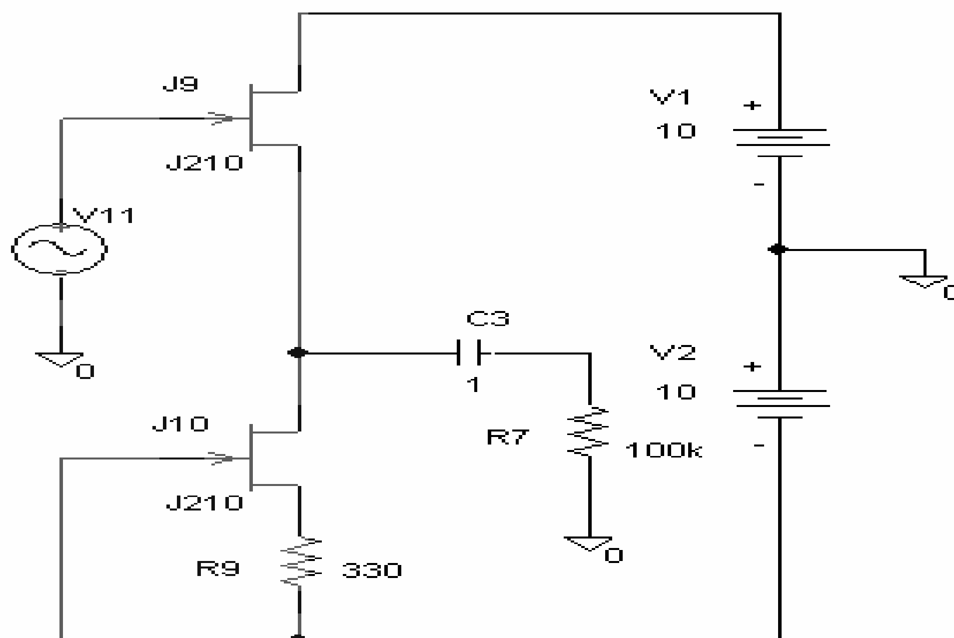



Figure 18 Voltage Follower Circuit

In Fig. 18, transistor J9 is the voltage follower and J10 is the active load for J9. Transistor J9 is biased by the constant current source formed by the transistor J10. R9 biases the J10. C3 is a coupling capacitor and R7 references the output to ground. This amplifier is also referred to as common-drain amplifier, since the input and the output nodes are at the gate and source nodes respectively. It is capable of driving low impedance loads with little loss of gain since its output resistance is low. As the input current is given by the gate leakage current, the input resistance of the voltage follower is high. One of the applications of the voltage follower is at the output stage in a multistage amplifier [6,20].

#### ***5.1.1.1 Simulation results for voltage follower with SiC VJFET and Si JFET***

The voltage follower circuit shown in Fig. 18 is simulated in PSpice with a sine wave input and the output of the voltage follower is observed. The simulation results of the voltage follower for SiC VJFET device and Si JFET device are shown in Fig. 19 and Fig. 20 respectively.

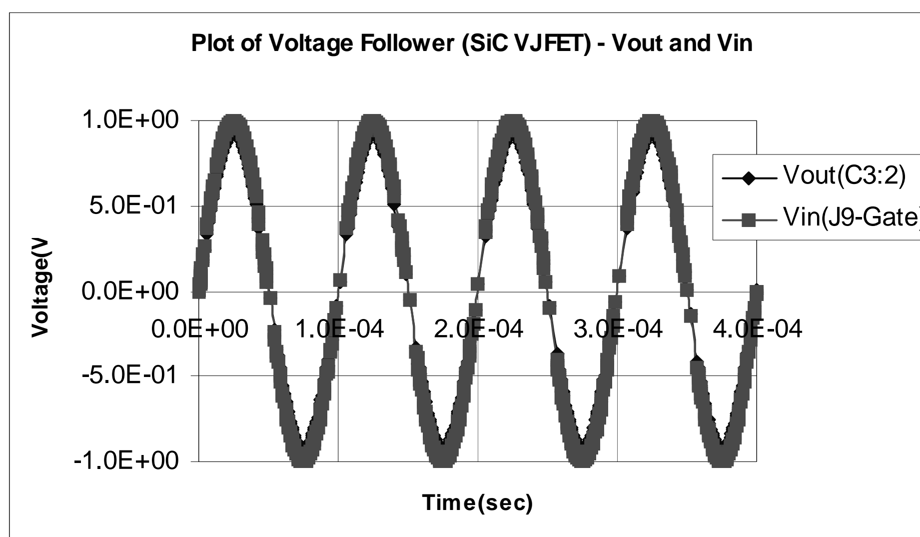



Figure 19 SiC VJFET Voltage Follower-Plot of Vout and Vin vs. time

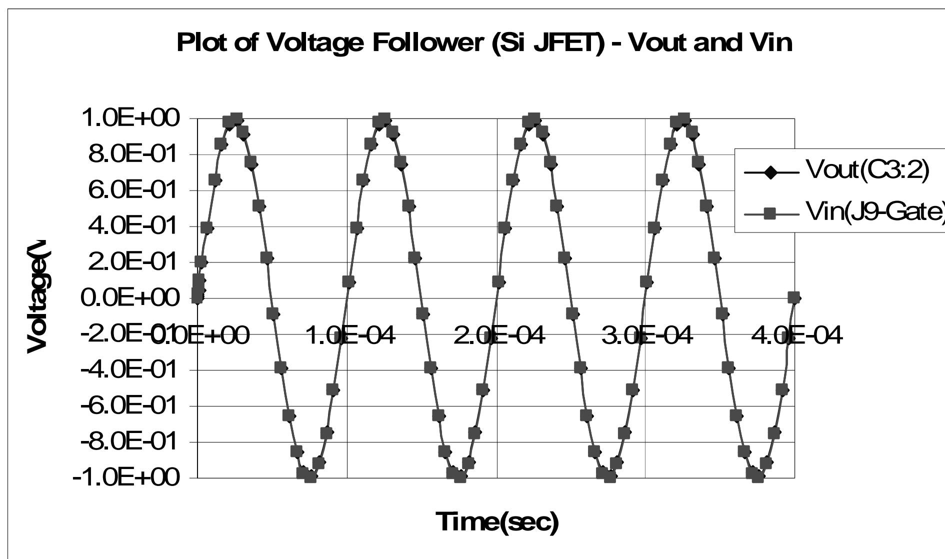



Figure 20 Si JFET Voltage Follower-Plot of Vout and Vin vs. time

Qualitatively, voltage follower with SiC VJFET has similar waveform as that of Si JFET. Hence, it can be concluded that our model for SiC VJFET is able to accurately predict the circuit behavior of the voltage follower.

The voltage gain ($A_v$) is calculated by measuring the peak-peak voltage of output and input.

$A_v$=Vout (peak-peak)/Vin (peak-peak) (14)

The voltage gain for SiC VJFET is 0.93. The current driving capability is measured from drain current. Drain current for SiC VJFET is 9.7 mA for $V_{ds}$=10V.

### *5.1.2 Common Source Amplifier*

A common source amplifier is a circuit capable of providing voltage gain greater than 1. The common source amplifier is shown in Fig. 21. The common source topology is the most popular gain stage, when high input impedance is required [20].

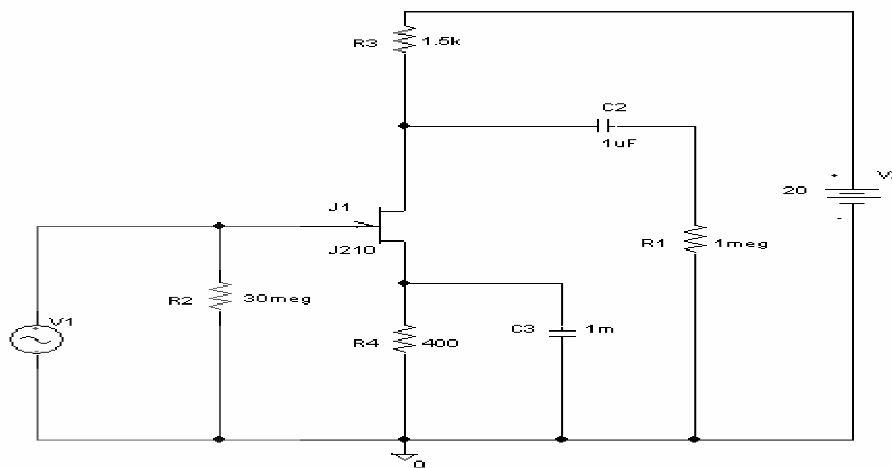



Figure 21 Common Source Amplifier [21]

Transistor J1 in Fig. 21 acts as a common source transistor while resistor R3 acts as a load resistor. The R3 value is chosen so that the transistor operates in the active region. The common source amplifier exhibits a high input and output resistance. R2 determines the input impedance and references the J1 gate to ground. C2 is a coupling capacitor and R1 references the output to ground. R4 biases the J1. This can compensate for some variation in JFET characteristics - if the JFET is conducting too much current, the voltage across R4 will raise making the JFET gate more negative with respect to the

JFET source, and thus reducing the current in the JFET. The capacitor labeled C3 (bypass capacitor) is chosen to bypass the source resistor at signal frequencies [20] [21].

### *5.1.2.1 Simulation results for Common Source amplifier with SiC VJFET and Si JFET*

The circuit shown in Fig. 21 is simulated in PSpice with a sine wave input and the output of the common source amplifier is observed. The simulation results of the common source amplifier for SiC VJFET device and Si JFET device are shown in Fig. 22 and Fig. 23 respectively.

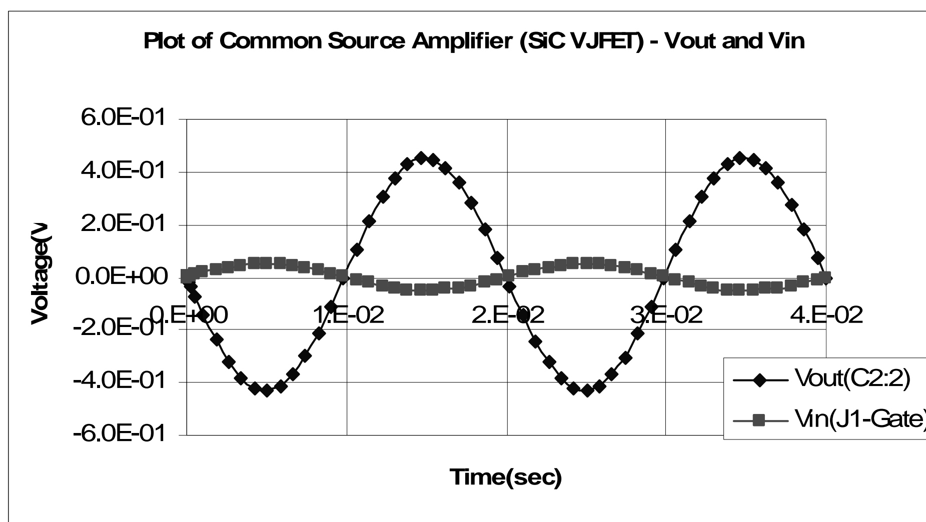



Figure 22 SiC VJFET Common Source Amplifier-Plot of Vout and Vin vs. time

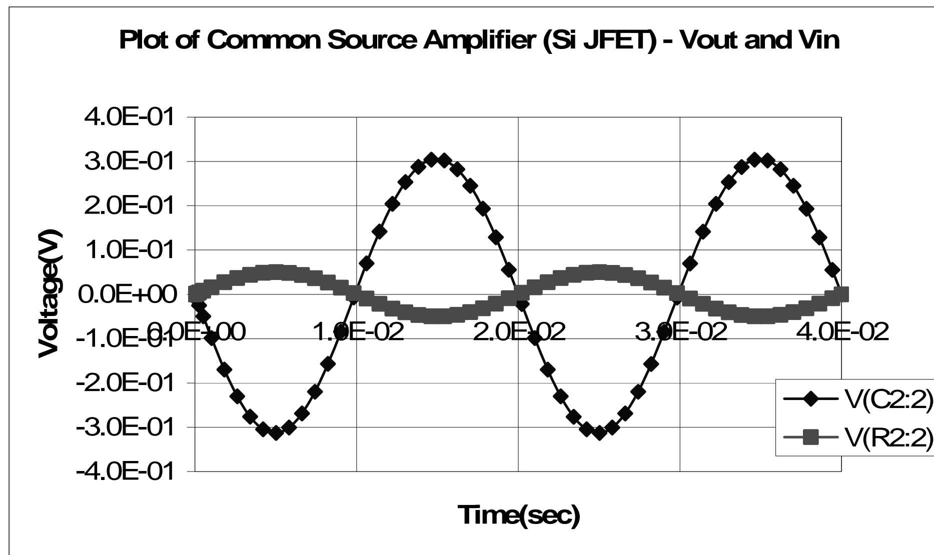



Figure 23 Si VJFET Common Source Amplifier-Plot of Vout and Vin vs. time

Qualitatively, common source amplifier with SiC VJFET has similar waveform as that of Si JFET. Hence, it can be concluded that our model of SiC VJFET common is able to accurately predict the circuit behavior of the source amplifier.

The voltage gain for SiC VJFET common source amplifier is calculated using eq. 14. and is equal to -9 (negative sign represents inverting amplifier). The current driving capability is measured from drain current. Drain current for SiC VJFET is 7.219 mA for $V_{ds}$=20V.

### *5.1.3 Current Source*

A current source is a circuit used to provide constant current to complex analog circuits. The design of current sources in analog circuits is based on copying current from the reference, with an assumption that one precisely defined current source is already available. It is carried out as illustrated in the Fig. 24 [24].

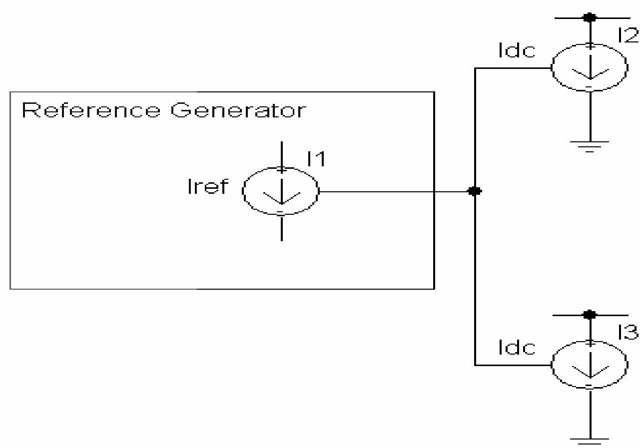



Figure 24 Reference Generator [24]

The self-bias current source circuit is shown in Fig. 25.

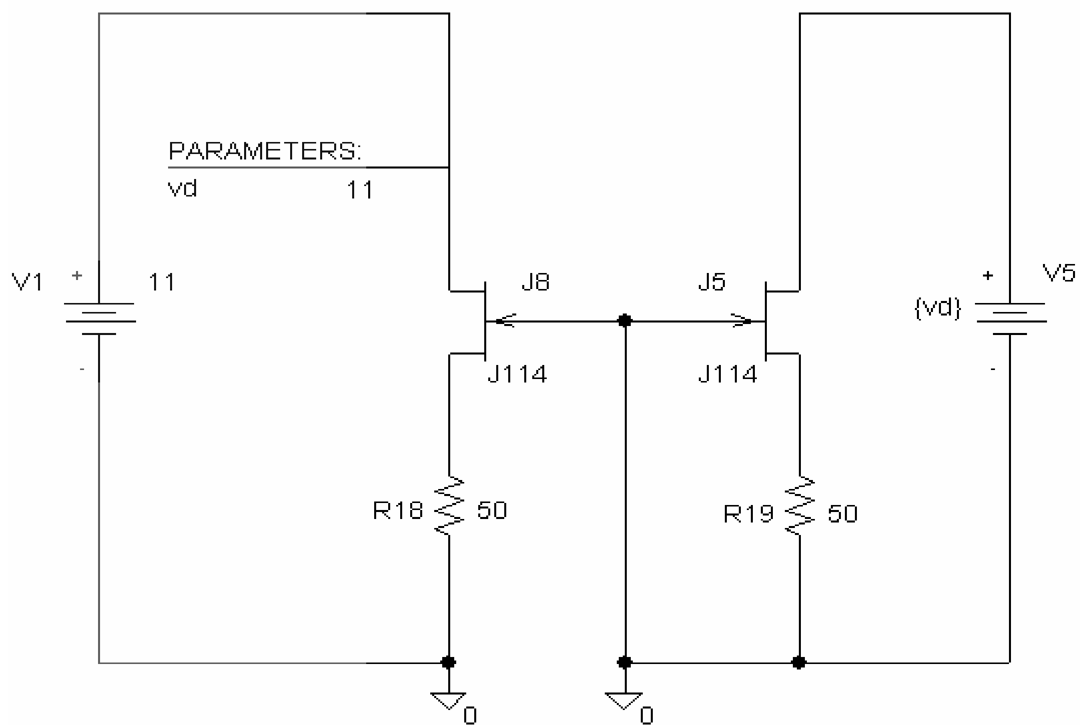



Figure 25 Current Source [6] [22]

A JFET operated in the saturation region acts as a current source. Changing the value of resistors R18 and R19 programs the size of drain current. The advantage of self-bias current source is that the additional battery is not required to bias the gate voltage. The circuit functioning depends on feedback in which the output controls the input. In Fig. 25 transistor J8 is the reference transistor while J5 is sweep for drain voltage 'vd'. The circuits functioning can be described as follows:

Initially, let's assume that the vd source is turned on abruptly and no current is flowing through the JFET. Then the voltage drop across the resistor R19 and $V_{gs}$ is equal to zero. This allows the drain current to flow through the J5. As the current increases, the voltage drop develops across the resistor and the upper end of the resistor becomes positively biased. This would result in gate to be negative biased. Negative value of $V_{gs}$ would start to turn off the J5. Ultimately, equilibrium would be attained where $V_{gs}$ is just right for the current flowing through the J5. Once in equilibrium, if the current would increase, the drop across the resistor would increase, resulting in J5 source to become more positive, hence $V_{gs}$ more negative which would cause the J5 to shut off slightly. If the current were to decrease, the drop across the resistor would decrease thereby $V_{gs}$ would become less negative and the J5 would turn on slightly. Hence the circuit regulates its output by feeding back a signal proportional to its output into its input [22].

#### *5.1.3.1 Simulation results for Current Source with SiC VJFET and Si JFET*

The current source circuit shown in Fig. 25 is simulated in PSpice. The J8 transistor in circuit shown in Fig. 25 acts as a constant current source. $V_{ds}$ of the J5 is

varied from 0 to $V_{dd}$ to obtain DC characteristics of the J5. I-V characteristics of the simulation results of the current source for SiC VJFET device and Si JFET device are shown in Fig. 26 and Fig. 27 respectively.

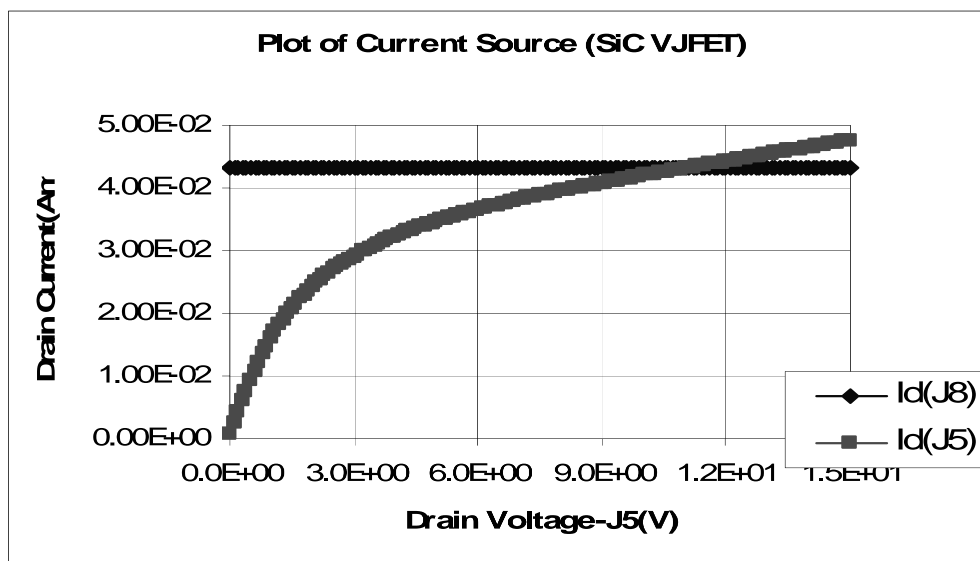



Figure 26 Si JFET Current Source - Plot of drain current vs. drain voltage

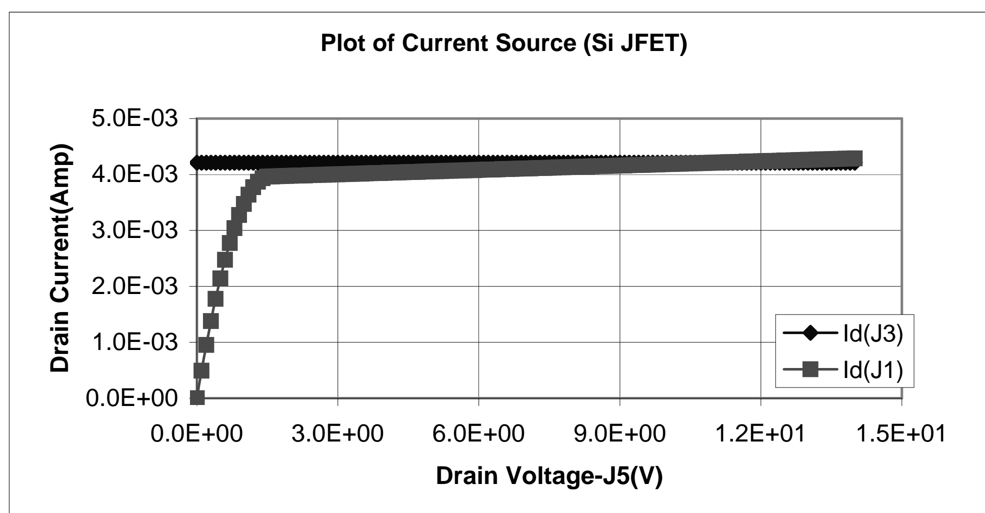



Figure 27 Si JFET Current Source - Plot of drain current vs. drain voltage

Qualitatively, current mirror with SiC VJFET has similar waveform as that of Si JFET. The current driving capability is measured from drain current. Drain current for SiC VJFET is 43 mA.

### *5.1.4 Differential Amplifier*

A differential amplifier amplifies the difference between the two signals. The differential amplifier circuit is shown in Fig. 28.

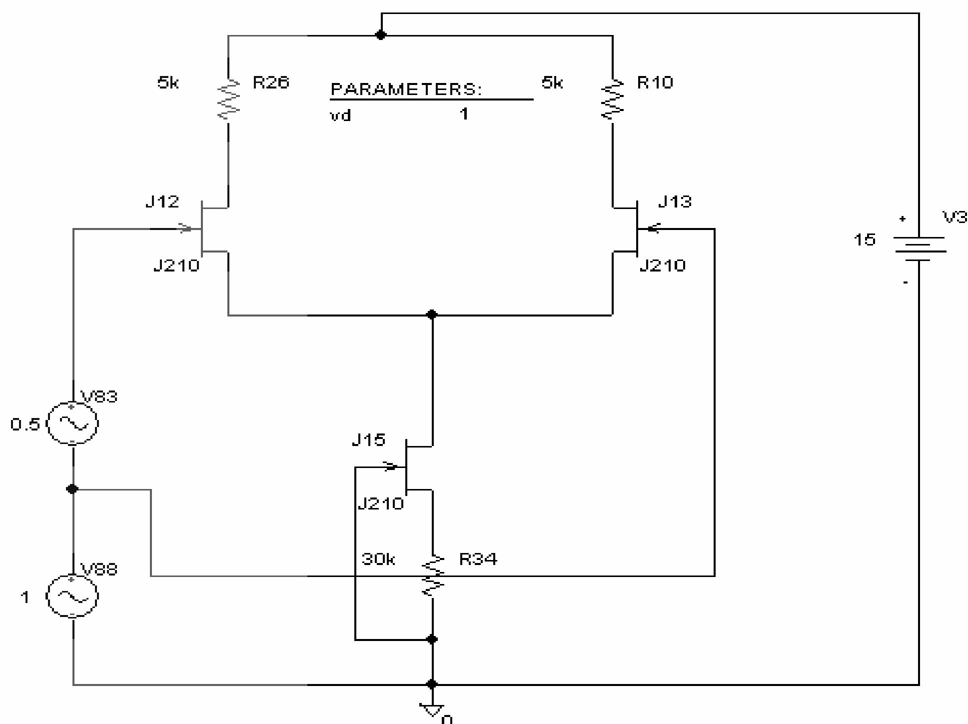



Figure 28 Differential Amplifier Circuit [20] [23]

In an ideal differential amplifier, the amplifier's output depends solely on the difference between the two inputs $V_d = V_g$ (J12) – $V_g$ (J13). Practically, the output of a

differential amplifier also depends weakly on the average between the two inputs. This average $V_{cm}$ = ½ ($V_g$ (J12) + $V_g$ (J13)) is called the common mode of the amplifier. Differential amplifiers are amongst the most common building blocks in analog circuit design [21,23]. The front end of every Op-Amp, for example consists of differential amplifier. Differential amplifiers are used whenever a desired signal is the difference between the two signals, particularly when this difference is masked by common mode noise (e.g., electrocardiogram) [22]. Differential amplifier consists of two matched transistors J12 and J13, whose sources are joined together and biased by a self-biased constant current source (J15) as shown in Fig. 28. The load circuit is such that the two transistors are in the active region. The drain of either transistor can be used as output. In some cases both JFETs drains are used to provide differential output.

Consider a pure common mode input for which $V_g$ (J12) = $V_g$ (J13). Since the JFETs are identical, due to symmetry of the circuit, the dc bias current splits equally between the two differential amplifier pairs J12 and J13. Thus provided that the output impedance of the current source is infinite, so that current does not change, the currents in the JFETs do not depend on the common-mode input voltage. Therefore, the output voltages are independent of the common mode input.

The effect of differential input voltage is to steer the majority of the bias current through one device or the other. For example if $V_g$ (J12) is greater than $V_g$ (J13), a larger current flows through J12 [21,23].

The important parameters to be considered in differential amplifier are Differential mode gain (ADM), Common mode gain (ACM) and Common mode rejection ratio (CMRR).

Common Mode Rejection Ratio (CMRR) is the ability of a differential amplifier to reject the common mode signal applied to both inputs. As in analog systems the signals are transmitted differentially, the ability of an amplifier to reject coupled noise is desirable. Ideally CMRR is infinity. It is given by the expression:

$$CMRR = 20 \log_{10} (ADM/ACM) \tag{15}$$

#### ***5.1.4.1 Simulation results for Differential Amplifier with SiC VJFET and Si JFET***

The circuit shown in Fig. 28 is simulated in PSpice with a differential and common mode input. The waveforms obtained for Differential mode gain is shown in Fig. 29 and Fig. 30 for SiC VJFET and Si JFET respectively.

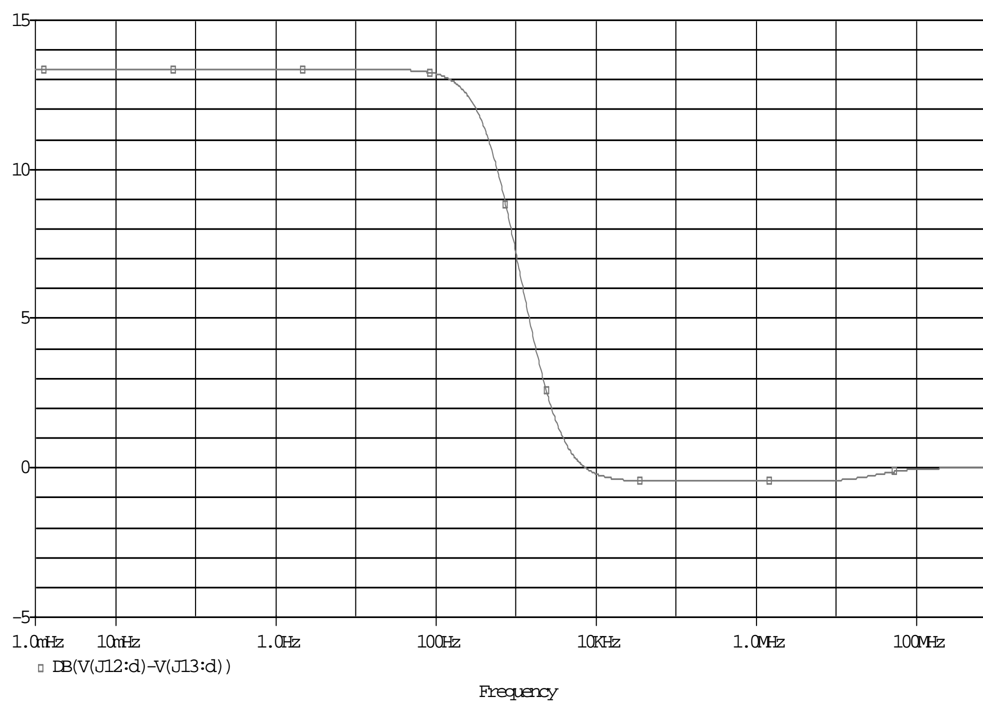



Figure 29 SiC VJFET Differential Amplifier-Plot of Differential Mode Gain vs. frequency

The Differential mode gain for SiC VJFET is 13.357 DB.

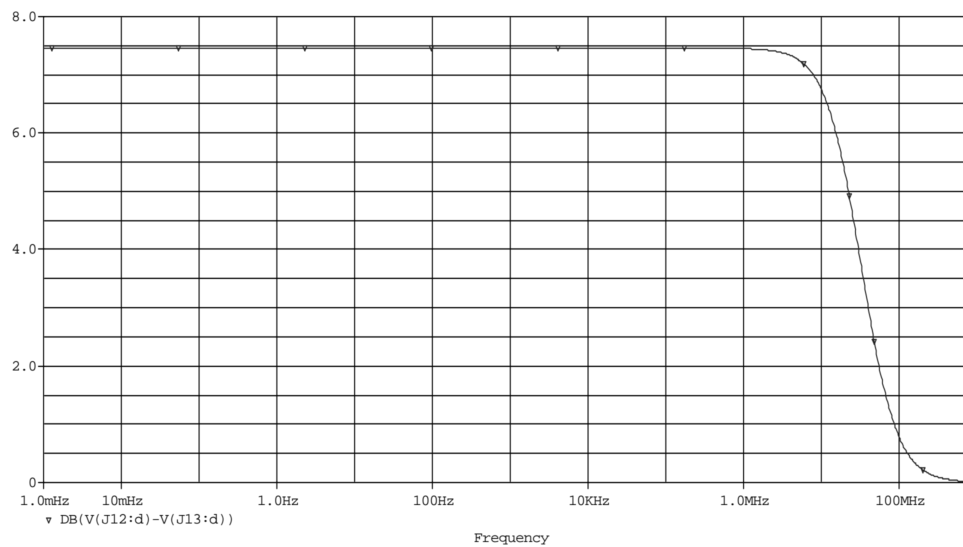



Figure 30 Si JFET Differential Amplifier-Plot of Differential Mode Gain vs. frequency

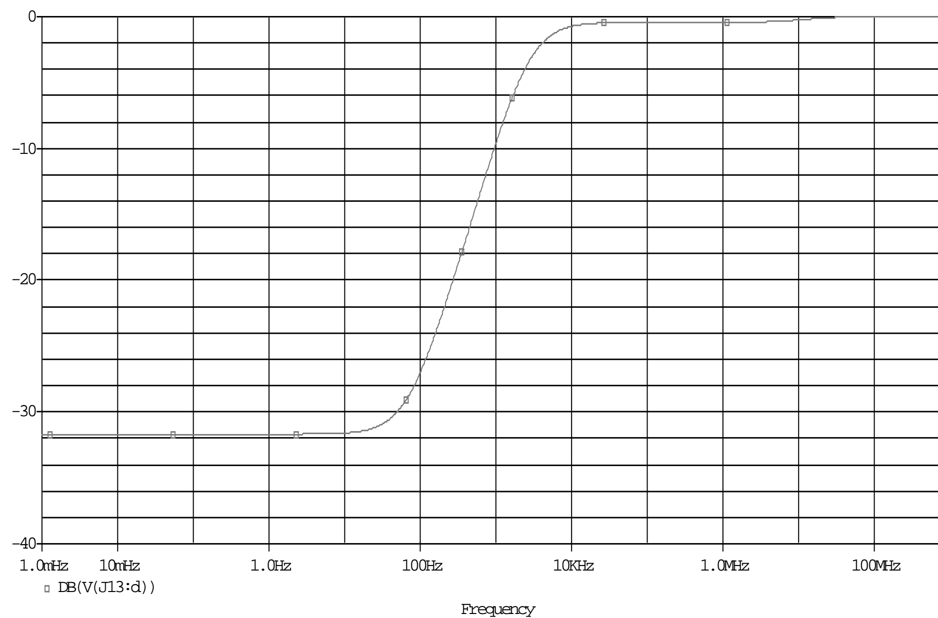



Figure 31 SiC VJFET Differential Amplifier-Plot of Common Mode Gain vs. frequency

The waveforms obtained for common mode gain is shown in Fig. 31 and Fig. 32 for SiC VJFET and Si JFET respectively.

The Common mode gain for SiC VJFET is -31.687 DB.

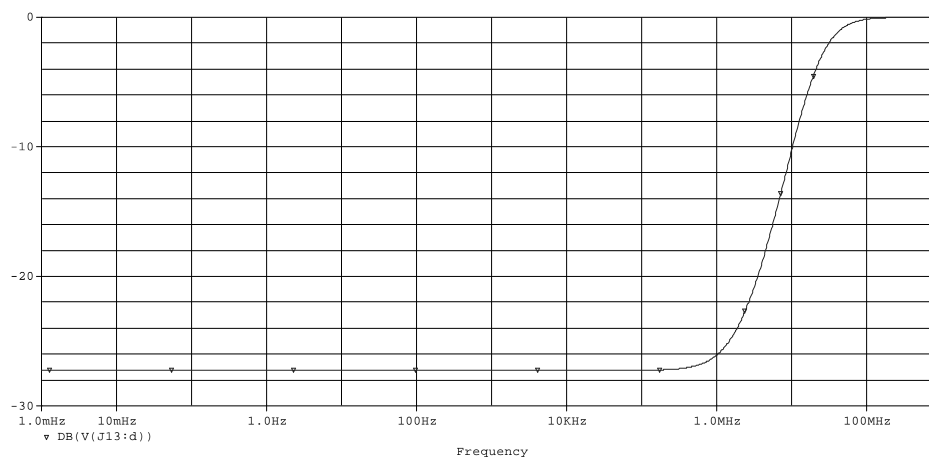



Figure 32 Si JFET Differential Amplifier-Plot of Common Mode Gain vs. frequency

Qualitatively, differential amplifier with SiC VJFET has similar Differential mode gain and Common mode gain waveform as that of Si JFET. CMRR obtained for SiC VJFET using eq. 15 is 45.044 DB

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# CHAPTER VI

# CONCLUSIONS AND FUTURE WORK

The objective of this thesis of creating a device model for novel silicon carbide n-channel VJFET was successful. An empirical Angelov model used for implementing SiC VJFET in PSpice was studied. The equivalent Circuit Model (ECM), DC and transient equations were developed and implemented in C/C++ and simulated in PSpice simulator. The model was shown to be predicting the DC and transient response of silicon carbide JFETs having different finger-width and operating at different temperatures.

A few classical analog circuits were analyzed with SiC VJFET replacing the standard Si JFET using the new model in order to demonstrate capabilities of the model and the feasibility of analog circuit design using SiC devices. It was demonstrated that SiC VJFETs provide the expected functionality of the selected analog circuits qualitatively similar to their Si counterparts. It is expected that with at least comparable performance of the analog circuits based on SiC transistors, the advantages of high-temperature and high-radiation-hardness operation will stimulate development of SiC devices for the wide range of applications.

The future work includes increasing the number of parameters of the model. Presently only the temperature and finger width are the parameters that a user is given an access to, with the other parameters corresponding to the parameters of the specific

experimental device that was used during the model development. The interpolation code has been made such that it can be automatically extended to more than 3 dimensions.

Validation of the Finger Width dependency has to be done upon availability of experimental data.

REFERENCES

[1] J.R. Connor and J. Smiltens, Silicon Carbide, A High Temperature Semiconductor, Pergamon, Oxford, 1960.

[2] R.B. Campbell, “Whatever Happened to Silicon Carbide?”, IEEE Transactions on Industrial Electronics, vol. IE-29, no. 2, pp. 124-128, May 1982.

[3] A.K. Agarwal, G. Augustine, V. Balakrishna, C.D. Brandt, A.A. Burk, A.A. Li-Shu Chen, R.C. Clarke, P.M. Esker, H.M. Hobgood, R.H. Hopkins, A.W. Morse, L.B. Rowland, S. Seshadri, R.R. Siergiej, T.J. Smith, S. Sriram, “SiC Electronics”, International Electron Devices Meeting, 1996, pp. 225-230, 8-11 Dec. 1996.

[4] Linkopings University, Department of Physics and Measurement Technology, Linkopings, Sweden. www.ifm.liu.se/matephys/AAnew/research/sicpart/kordina2.htm

[5] L. Cheng, I. Sankin, J.N. Merrett, V. Bondarenko, R. Kelley, S. Purohit, Y. Koshka, J.R.B. Casady, J.B. Casady and M.S. Mazzola, “Cryogenic and High Temperature Performance of 4H-SiC Vertical Junction Field Effect Transistors (VJFETs) for Space Applications”, $17^{th}$ IEEE International Symposium on Power Semiconductor Devices and IC’s, May 23-26, 2005.

[6] Adel S. Sedra, Kenneth C. Smith, “Microelectronic Circuits, $4^{th}$ edition”, Oxford University Press.

[7] B.J. Baliga, Modern Power Devices, John Wiley & Sons, New York, 1987, pp. 133-195.

[8] R.R. Siergiej, R.C. Clarke, A.K. Agarwal, C.D. Brandt, A.A. Burk, Jr., A. Morse, and P.A. Orphanos, “High Power 4H-SiC Static Induction Transistors”, International Electron Devices Meeting, 1995., 10-13, pp. 353-356, Dec. 1995.

[9] http://www.ecircuitcenter.com/SPICEtopics.htm

[10] P.G. Neudeck, “SiC Technology”, in the VLSI Handbook, The Electrical Engineering Handbook Series, W.K. Chen, Ed. Boca Raton, Florida: CRC Press and IEEE Press, 2000, pp. 6.1-6.24.

[11] R. Kraus and H. Jurgen, "Status and Trends of Power Semiconductor Device Models for Circuit Simulation," IEEE Transactions on Power Electronics, vol. 13, no. 3, pp. 452-465, May 1998.

[12] B. Fatemizadeh, P.O. Lauritzen, D. Silber, "Modeling of Power Semiconductor Devices, Problems, Limitation and Future Trends," IEEE Workshop on Computers in Power Electronics (COMPEL 1996), pp. 120-127, Aug. 11-14, 1996

[13] Iltcho Angelov, Herbert Zirath, and Niklas Rorsman, "A New Empirical Nonlinear Model for HEMT and MESFET Devices," IEEE Transactions On Microwave Theory And Techniques, Vol. 40, No. 12, December 1992.

[14] Avinash S. Kashyap, Prasanna L. Ramavarapu, Sharmila Maganlal, Ty. R. McNutt, Alexander B.Lostetter, and H. Alan Mantooth, "Modeling Vertical Junction Field Effect Devices In Silicon Carbide," 2004, 35th Annual IEEE Power Electronics Specialists Conference.

[15] J. Michael Golio, "Microwave MESFETs and HEMTs", page 128-147, Artech House Publisher, February 1991.

[16] Curtice, W.R., "A MESFET Model for Use in the Design of GaAs Integrated Circuits," IEEE Transactions on Microwave Theory and Techniques, Vol. 28, pp. 448-456, May, 5, 1980.

[17] Michael B. Steer and Paul D. Franzon, "SPICE: User's Guide and Reference," August 20, 2002.

[18] Jaakko Ala-Paavola, Martti Valtonen, Antti Kallio, "Chalmers MESFET Model in APLAC," Helsinki University of Technology, Department of Electrical and Communications Engineering, Circuit Theory Laboratory. February 2000.

[19] Willian H. Press, Brian P. Flannery, Saul A. Teukolsky, William T. Vetterling, "Numerical Recipies in C: The Art of Scientific Computing" Second Edition, pages 105-128, Cambridge University Press.

[20] David A. Johns, Ken Martin, "Analog Integrated Circuit Design,", John Wiley and Sons Publisher.

[21] R. Jacob Baker, Harry W. Li, David E. Boyce, "CMOS circuit design, layout and simulation", Wiley-IEEE Press.

[22] Joel Fajans, "Basic Semiconductor Circuits Manual", University of California at Berkeley.

[23] Nilesh KirtiKumar Aurangabadkar, "Simulations of Analog Circuit Building Blocks based on Radiation and Temperature Tolerant SiC JFET Technologies", Mississippi State University, Department of Electrical and Computer Engineering, August 2003.

[24] Razavi, 2001, pp. 135-136.

[25] JEDEC Solid State Technology Association, JEDEC Standard # 24, July 1985 http://www.jedec.org/download/search/jesd24.pdf

[26] Schroder, Dieter K., "Semiconductor Material and Device Characterization, 1990", A Wiley-Interscience publication.

[27] T. McNutt, A. Hefner, A. Mantooth, J. Duliere, D. Berning, R. Singh, "Parameter Extraction Sequence for SiC Schottky, Merged PiN Schottky, and PiN Power Diode Models," Conf. Rec. of IEEE Power Electronics Specialists Conf (PESC), pp. 1269-1276, Cairns, Australia, June 2002.

[28] T. McNutt, A. Hefner, A. Mantooth, D. Berning, S.H. Ryu, "Silicon Carbide Power MOSFET Model and Parameter Extraction Sequence," Conf. Rec. of IEEE Power Electronics Specialists Conf. (PESC), pp. 217-226, Acapulco, Mexico, June 2003.

[29] R.C. Clarke, "Silicon Carbide Devices for Power Applications,"Bipolar/BiCMOS Circuits and Technology Meeting, Proceedings of the 2001.

[30] National Institute of Standards and Technology, http://www.nist.gov/public_affairs/factsheet/auto2.html

# APPENDIX A.

# PSPICE SIMULATOR

## A.1 Nodal Analysis

At the core of the PSpice engine is a basic technique called Nodal Analysis. It calculates the voltage at any node given all of the circuit resistances (conductances) and current sources. Whether the program is performing DC, AC, or Transient Analysis, PSpice ultimately casts its components (linear, non-linear and energy-storage) into a form where the innermost calculation is Nodal Analysis. Nodal analysis provides a general procedure for analyzing circuits using node voltages as the circuit variables. Nodal analysis utilizes Kirchoff's Current Law (KCL) to solve nodal voltages from nodal equations written in matrix form. Mathematically, it can be written as

$$V=G^{-1}.I$$

Where $G^{-1}$ is the matrix inverse of G. and I and V are the current and voltage vectors respectively. However, Nodal analysis does not accommodate a voltage source. Voltage sources are handled in one of two ways. The first one requires that every voltage appear in series with a resistor so that the source may be transformed into a Norton equivalent current source. The second approach is known as Modified Nodal Analysis (MNA). In this, the nodal equations are first assembled including all elements other than the voltage sources by assuming the current in the equations for each voltage source. The additional equations come from the voltage relation between the nodes where the voltages sources are connected. For example, if voltage V is connected between the nodes 1 and 2, then $V_2-V_1=V$ is the relation between node voltage 1 and 2 [9].

## A.2 Non-linear DC Analysis

Nodal analysis is used to find the voltages at every node in the DC linear circuit. But this approach can't be directly used for non-linear components such as diode. The solution method used by PSpice is based on Newton-Raphson iteration technique. The solution technique requires starting from some trial operating point voltages and then generating a sequence of voltage iteration until the solution is reached. Here we are going to take diode as an example to understand the working of non-linear components in PSpice.

The current vs. voltage relationship for a diode is given by

$$I_d = I_s . (\exp (V_d/V_t) - 1) \qquad (16)$$

Where $I_s$ is the saturation current and $V_t$ the thermal voltage.

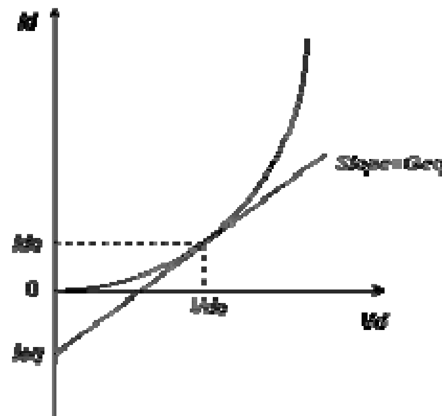


Figure 33 Diode characteristic curve and tangent line [9]

The behavior approximation of a diode curve can be done by a tangent line at Vdo. A straight line can be modeled using linear components - a parallel combination of a conductance Geq and a current source Ieq.

$$G_{eq} = dI_d/dV_d = (I_s/V_t).\exp(V_{do}/V_t) \quad (17)$$

$$I_{eq} = I_{do} - G_{eq}.V_{do} \quad (18)$$

Hence, the non linear diode model is transformed into linear companion model.

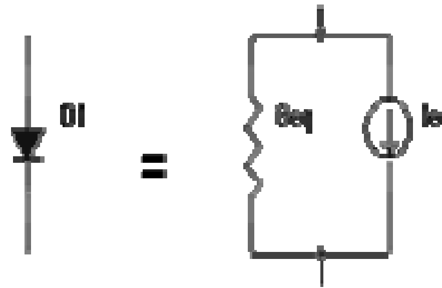


Figure 34 Linear Companion model of diode [9]

The linear companion model was created at some trial operating point. The voltages found by solving the nodal equation serve as the next trial operating point and a new companion model is formed. This process is repeated until a solution is reached. If the change in circuit voltages and currents, between one iteration (n) and the last iteration (n-1), are smaller than some limit, then the solution is reached.

It can be summarized as:

- Guess at the diode's initial trial operating point.
- Create linear companion models
- Solve nodal equations

- Convergence?

|V (n)-V (n-1)|<VLIMIT and |I (n)-I (n-1)|<ILIMIT?

- **No**-use the calculated diode voltage as new trial operating point for another iteration. Start again at step 2.
- **Yes**- jump to step 6.
- Stop iterations, solution reached. [9]

## A.3 PSpice Algorithm

A simplified block diagram of the main PSpice program is shown in Fig. 35

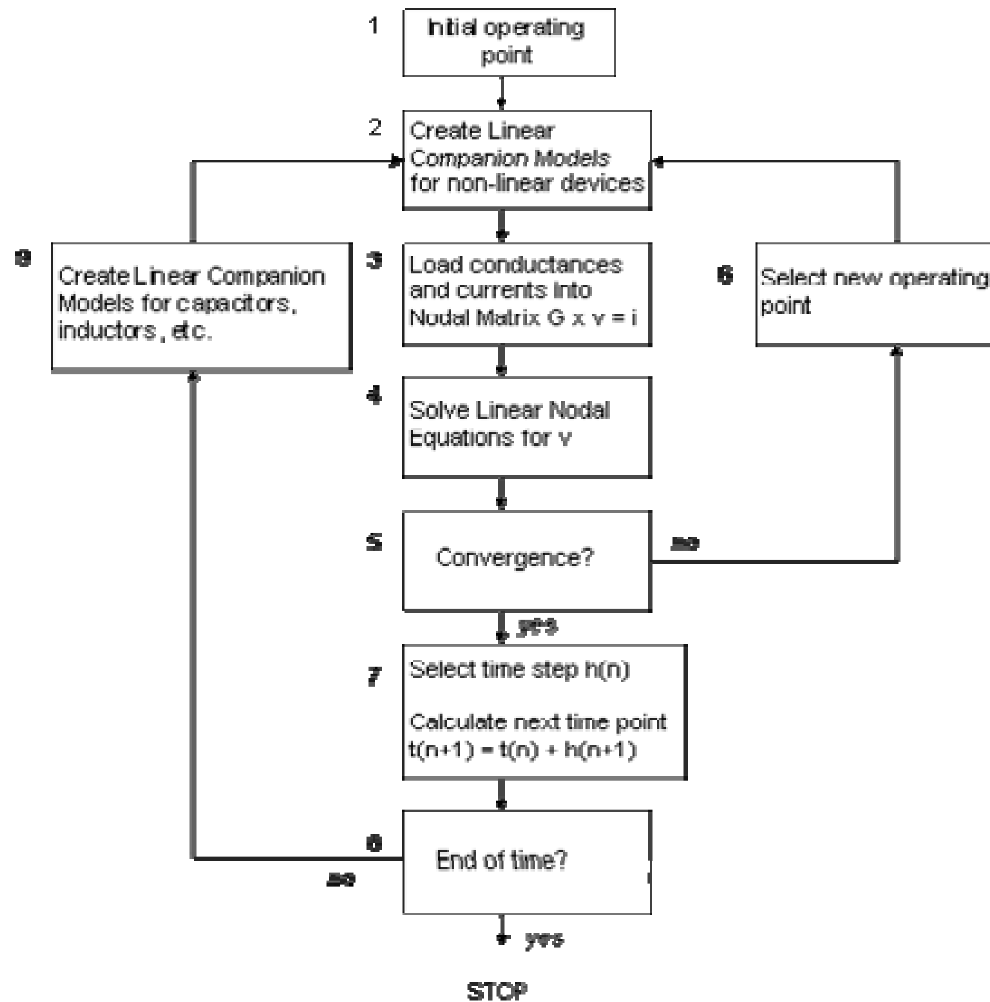


Figure 35 PSpice Algorithm

Three key points about the algorithm"

At the heart of the PSpice is nodal analysis (blocks 3 and 4) accomplished by formulating the Nodal Matrix and solving the nodal equations for the circuit voltages.

The inner loop (2-6) finds the solution for non-linear circuits. Non-linear devices are replaced by equivalent linear models. It may take much iteration before the calculations converge to a solution.

The outer loop (7-9), together with the inner loop, performs a transient analysis creating a equivalent linear models for energy storage components for capacitors, inductors etc and selecting the best time points.

### A.4 Transient analysis

One of the most complex and intriguing capabilities of the PSpice algorithm is the transient analysis. PSpice first transforms the energy-storage components into their linear companion models, which is then used to do nodal analysis. PSpice attempts to find a solution at discrete time points using numeric integration. Knowing the function at time $t_n$, we can approximate the function at a future time point $t_{n+1}$ by looking at the slope of the curve and multiplying the slope by the time step $h = t_{n+1} - t_n$ and adding it to the present voltage. The more intuitive approach is to take slop at point $t_n$ know as Forward-Euler Integration Formula. But, it’s not very accurate. Therefore, PSpice uses Backward-Euler (BE) Integration formula which takes the slope at point $t_{n+1}$.

Mathematically, it can be expressed as

$$x_{n+1} = x_n + h.dx_{n+1}/dt \tag{19}$$

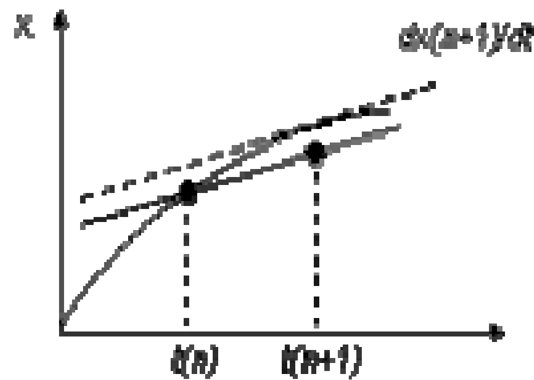


Figure 36 Backward Euler Integration applied to approximate the next voltage [9]

This method is more accurate and less sensitive to size of the time step compared to the FE method.

The approach to convert energy component to linear component model can be best explained by taking example of a capacitor.

A capacitor is transformed to linear model by 2 steps

Apply numeric integration to the current- voltage relationship of a capacitor.

Use the result to develop a linear companion model well-suited for nodal analysis to calculate circuit's output waveform.

We know for a capacitor

$$V=Q/C \tag{20}$$

$$I=dQ/dt \tag{21}$$

Applying the BE formula to predict the capacitor's voltage at the next time point

$$V_{n+1} = V_n + h.dV_{n+1}/dt \tag{22}$$

Using eq. 20, 21, 22

$V_{n+1} = V_n + (h/C).I_{n+1}$ (23)

Arranging eq. 23

$I_{n+1} = (C/h).V_{n+1} + (C/h).V_n$ (24)

C/h is equivalent to conductance Geq as multiplying it by V produces current.

$I_{n+1} = Geq.V_{n+1} + Geq.V_n$ (25)

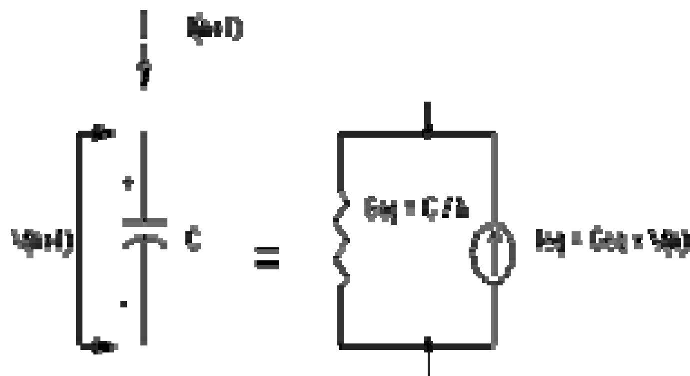


Figure 37 Linear companion model of a capacitor using the Backward Euler Formula [9]

This equation can be implemented with simple circuit components as shown in Figure 37.

Conductance Geq describes the part of C1's current dependent on its new voltage $V_{n+1}$, current source Ieq describes the other part based on the past voltage $V_n$. [9]

# APPENDIX B.

# MAJOR FILES

## B.1 Major Files

The major files in which the functionality of the device model is defined are

**j.h:** This file contains two important class definitions:

- The class for the JFET transistor.
- The class for the JFET model.

During read-in, the simulator creates an instance of the transistor class for every JFET in the circuit and an instance of the model class for every MODEL statement of type NFET or PFET.

**j.cpp:** This file contains auxiliary functions that implement the AC equations, matrix setup.

**acjfet.cpp:** This file process JFET for ac analysis

**jfet.cpp:** The device equations are present in this file. The code in it is arranged into separate functional subsections. Each subsection occurs at least once, but can occur several times if more than one Level is present. The subsections are outlined below:

**Initialization:** This consists of locating and binding the device instance and its model, initializing any local variables, and obtaining appropriate values for the device branch voltages.

**Computing new nonlinear branch voltage:** This is needed to monitor progress towards a Newton-Raphson Solution.

**Test if the solution has changed:** If there is no significant change, bypass the rest of the computation, otherwise continue.

**Limit any nonlinear branch voltage:** This code ensures that the branch voltages are in the appropriate operating region.

**Compute current and conductances:** This is the meat of the device equations code, and involves obtaining all the branch currents as well as the derivatives to be used in the conductance matrix.

**Charge calculation:** Internal charges are calculated and updated.

**Check convergence:** Check to see if the nonlinear device branches now have that are within a small tolerance range of those obtained in the last repeat cycle, and set a return flag to signal whether the device converged.

**Load the current and conductance matrix:** This is used to obtain handles to the proper matrix elements, and the elements are assigned their values based on the present evaluation of the device equations and derivatives.