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A Design Methodology for a High Power Density, Voltage Boost, Resonant DC-DC converter

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A DESIGN METHODOLOGY FOR A HIGH POWER DENSITY, VOLTAGE BOOST, RESONANT DC-DC CONVERTER

By

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A full-bridge, parallel-loaded, resonant, zero current/zero voltage switching converter has been developed for DC-DC voltage transformation. The power supply was used to condition power sourced by a 28-V, 400-A Neihoff alternator installed in a HMMWV that delivered power to a 5-kW mobile radar. This design focuses on achieving maximum power density at reasonable efficiency (i.e. > 80%) by operating at the highest resonant and switching frequencies possible. A resonant frequency of 392-kHz was achieved while providing rated power. The high resonant frequency was facilitated by the development of an extremely low inductance layout (< 20 nH) capable of conducting the high resonant currents associated with this converter topology. A design methodology is presented for parallel-loaded, resonant voltage boost converters utilizing the development of a converter prototype as a basis. The experimental results are presented as validation of the methodology.

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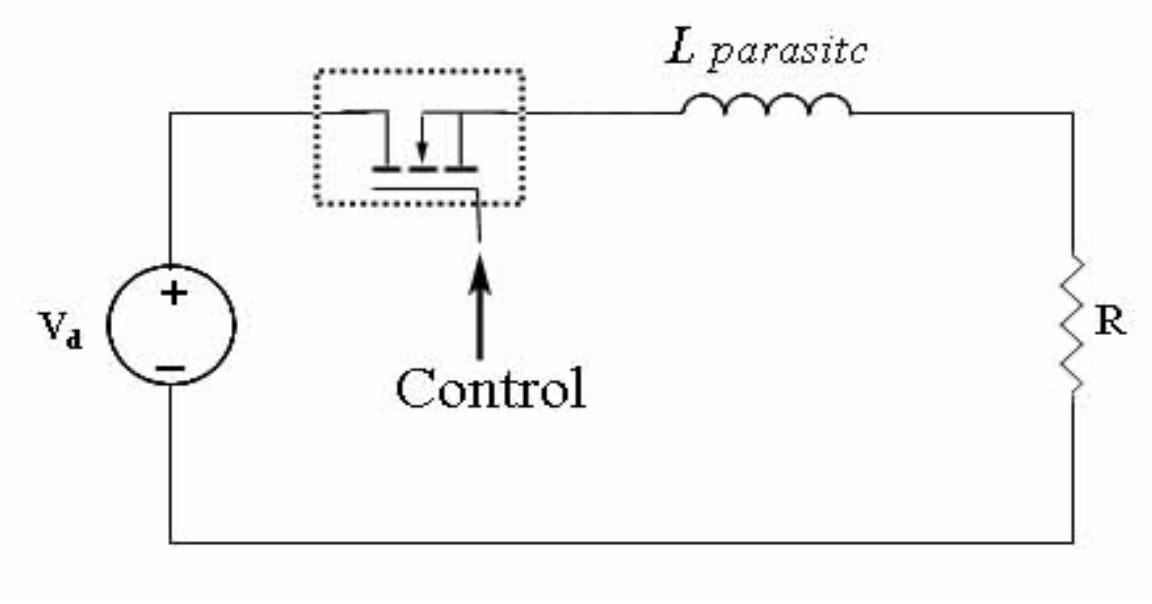
CHAPTER I

INTRODUCTION TO THE LOAD RESONANT CONVERTER

There are a multitude of applications for high power density, high current, step-up power supplies; however, achieving reasonable efficiency and power density continues to be a challenging task. Resonant power converters are increasingly becoming the popular choice for dc power conversion due to the low losses associated with this type of power supply at high conversion frequency. Advances in semiconductor technology, magnetics, and controls have been extending the limits of operating conditions such as voltage, power, and switching frequency. This in turn broadens the applications for resonant power converters by increasing or maintaining efficiency as power density increases. The motivation behind this thesis is the development of a layout methodology for designing a parallel-loaded, resonant converter (PLRC) that achieves high power density at high switching frequency and resonant frequency (i.e. > 100kHz) by minimizing parasitic loop inductance through careful component arrangement, high frequency transformer design, and bus design. The validity of this methodology is verified through experimental results from a low input, voltage step up PLRC developed at Mississippi State University.

Conventional pulse-width modulated (PWM) converter topologies or "hard switched" converters interrupt the entire supply voltage and load current during each switching cycle such as the case in Fig. 1.1a [1]. This action leads to high stresses on the switching components as illustrated by the switch voltage and current waveforms in Fig. 1.1b. Figure 1.1a depicts a circuit containing a MOSFET being switched in series with a resistive load and a finite amount of parasitic inductance. The waveforms in Fig. 1.1b are typical of a circuit such as Fig. 1.1a. The parasitic inductance included in the circuit is an unavoidable consequence in a real device. This could be resulting from interconnections as well as inductance inherent to any switch, such as the MOSFET. The fall and rise of the voltage at turn on and turn off in the figure are typical of MOSFT switching. In this circuit, during both turn on and turn off of the switch, current is being conducted through the switch while the voltage across the switch terminals begins to rise. Naturally current conduction through a potential difference results in power dissipation. In the case of switching losses generated by forced current commutation the power dissipation is manifested by heating of the switch. The shaded area in Fig 1.1b illustrates the power lost at the switching instances in relation to the current and voltage conditions imposed by hard switching. Dissipative snubbers can be used to relieve component stress, however; this only shifts power dissipation to the snubber circuit and does not offer any substantial improvement in overall system efficiency [2].

High switching frequencies are often desired in power converters to reduce the size and weight of passive components and thereby increase power density. Unfortunately in hard-switched PWM converters, dynamic power loss becomes



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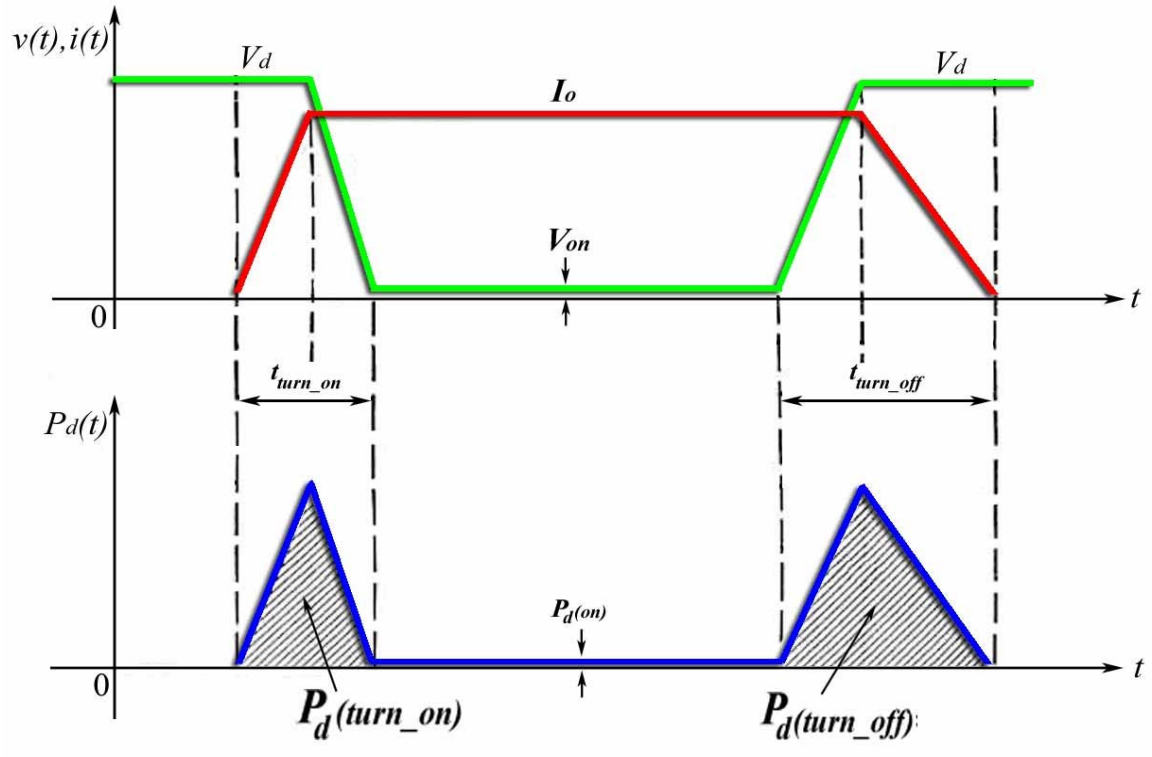
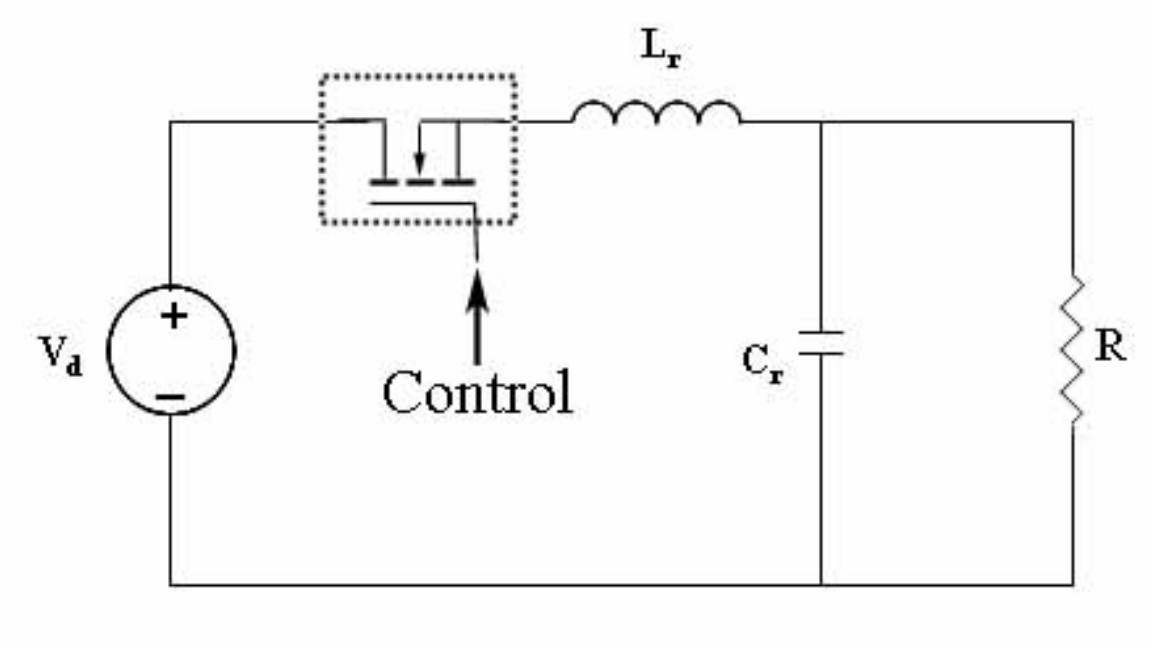


(b)

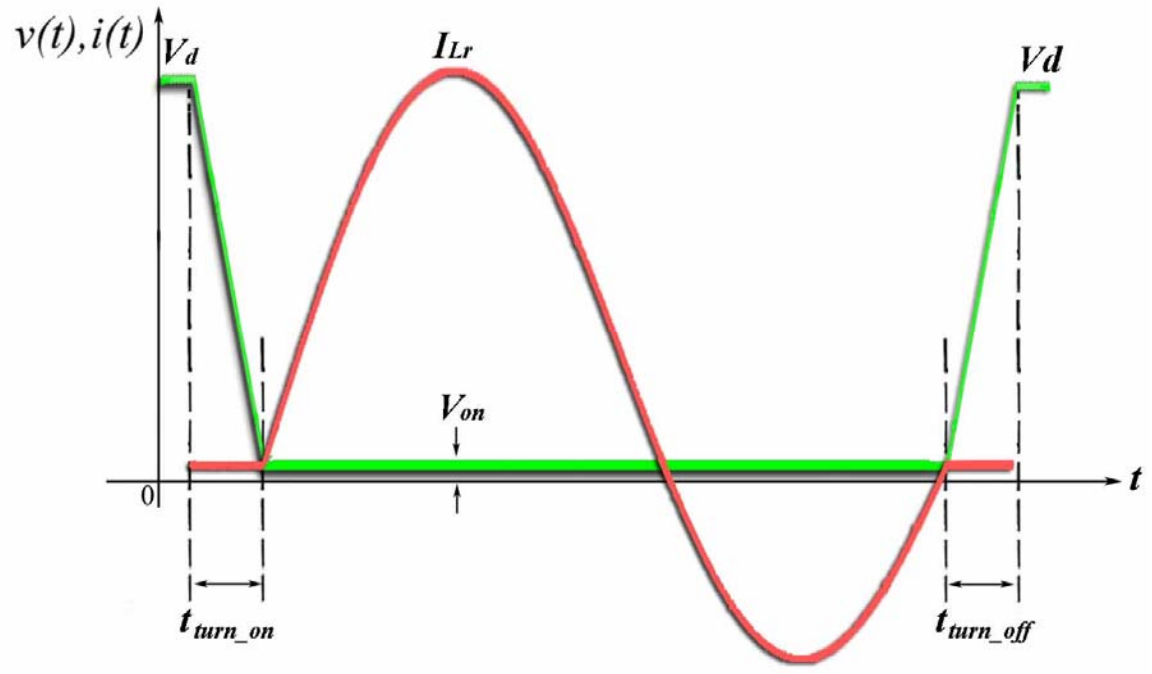
Figure 1.1: Switching losses in hard switched converters. (a) generic hard switching circuit schematic (b) switching losses (from [1])

significant at moderate switching frequencies and therefore increasing frequency often reduces system efficiency. The inability of switch-mode converters to operate efficiently at high switching frequencies places natural limits on the frequency that can be reasonably achieved. Lower frequency operation in turn forces the use of large reactive components thereby limiting power density [3]. One approach to alleviate this problem is to switch at a time when either the switch current or voltage is zero. Elimination of switching losses will allow for switching frequencies to be increased without decreasing efficiency. Power density can be improved while maintaining or improving efficiency. In theory soft switching converter technologies are capable of achieving higher power, higher power density, and greater efficiency than hard switched converters.

One method that produces waveforms suitable for soft-switching is the addition of a series L-C resonant circuit into certain hard-switched topologies. As an example of a method for utilizing L-C resonance, Fig. 1.2a shows a circuit that incorporates a series resonant tank into the circuit in Fig. 1.1a with the load placed in parallel with the resonant capacitance. The waveforms for voltage across the switch and the current through the switch are shown in Fig. 1.2b. Unlike the PWM case the current in this figure does not begin to increase significantly until after the voltage across the switch has fallen eliminating power loss at turn on and similar transition occurs at turn off. Also, the parasitic inductance included in Fig 1.1a is now incorporated into the resonant inductance. The current rise and fall times can be controlled by adjusting the resonant inductance for a given resonant frequency. The circuit in Fig. 1.2a is the basis for a class of converter topologies, known as parallel-loaded, resonant converters. Most of the



(a)



(b)

Figure 1.2: Series resonant circuit with a parallel loaded capacitor. (a) circuit (b) voltage across the switch and current through the switch

literature described in the following section refers to converters utilizing a parallel-loaded series resonant (PLR) tank.

Previous Investigations

Much work has been conducted in the study of resonant converters and more specifically in the area of PLR converters for the past twenty years. The advent of fast switching power transistors and the continued improvement in the devices has pushed the development of power converter technology to ever greater power and frequency. This has also produced higher power density converters with continually improving efficiency. One of the first documented studies of load resonant converters using modern semiconductor devices was done by Steigerwald [4] in 1984. Before this period although possibilities of high frequency resonant converters had been theorized, typical design implementations were low frequency, thyristor-based circuits due to the lack of viable switch technology. This report describes several high frequency, resonant converter topologies including the series resonant converter and the parallel loaded resonant converter. In this first of many studies by Steigerwald on this subject there is presented a low power design example showing proof of principle of high frequency operation of a parallel loaded resonant tank for dc-dc conversion.

Steigerwald followed up his first study with a publication in 1988 again examining several resonant converter topologies including the PLR [5]. Although this document primarily deals with converters operating at switching frequencies above the resonant frequency, several general conclusions were drawn which impact the design of

any parallel loaded resonant converter design. For example, the light load inefficiency of this type of converter is pointed out as well as the load independence of the output voltage. The stability of a PLR converter under a wide load range makes it an ideal choice for any voltage source application where load conditions are expected to vary. The author concludes that the parallel load resonant converters are uniquely suited for development of high power voltage sources.

Around this same time Kang and Upadhyay published and excellent study on the design of a half-bridge PLRC [6]. A steady-state mathematical model was developed for operation below resonance in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM). A 150-W 500-kHz off-line converter was constructed and operated under both operating conditions. From experimental results, they concluded that DCM is, for this case, a more efficient mode of operation than CCM below resonance. The various modes of operation will be discussed in greater detail in Chapter II.

Also in 1988 a team of researchers at the University of Colorado compared a PLRC to a series resonant converter and a hybrid series parallel resonant converter for a high voltage, low power application (i.e. < 100 W) [7]. Their design goal was to develop a 24-V to 8-kV, 1-mA converter. They concluded that for large boost applications requiring a voltage source converter the parallel load resonant converter is a suitable topology due to the ability to incorporate both the transformer interwinding capacitance and leakage inductance into the resonant components. This ability is essential for dealing

with the significant transformer parasitic elements associated with the high turns ratios required for a large voltage boost.

The following year an analysis of the PLRC including the effects of a high frequency transformer was published for converters operating above resonance. The authors of this study, Bhat and Swamy, provide a design example which includes the non-idealities associated with a high-frequency transformer. A 1-kW experimental converter was developed in order to validate the design procedure [8].

Kang, Upadhyay, and Stephens published a study in 1991 similar to Kang and Upadhyay's previous paper. This new document again addresses the analytical issues in the design of half-bridge PLR converters. In this study they investigate the steady state operation of PLR converters operating in continuous conduction mode switching above resonance. The authors present a set of equations for describing the operation of the resonant tank in this mode. This information was employed in the design of a small experimental converter offered as proof of principle [9].

A research team at the Kyosan Electric Manufacturing Company in Japan produced a step down PLR converter operating in discontinuous conduction mode a few months later in 1991. Their analysis describes several notable characteristics of this type of converter. Those characteristics being the voltage stability across a wide load range due to the parallel placement of the resonant capacitance and the tolerance of this topology to transformer parasitics. This article also provides a detailed description of the dead period short circuiting of the resonant capacitor due to the freewheeling action of the output rectifiers [10].

Swamy and Bhat published their analysis of a PLRC with the resonant capacitance across the secondary transformer winding with a goal of explaining the effects of such a placement of this component. In their work they reported the experimental design of three 1-kW converters operating from an input of 230 V with output voltages of 48 V, 115 V, and 230 V operating in CCM above resonance. Their analysis in this paper shows the viability of a PLRC with secondary side resonance; however, the effects of snubber capacitors are expressly neglected. The authors do acknowledge that operation in CCM above resonance without the use of snubber capacitors is not advisable [11]. This issue will also be discussed in greater detail in Chapter II.

Steigerwald published a new study on the subject of a parallel loaded resonant circuit operating above the resonant frequency in 1992. In this work he presents a methodology for rapid development of point designs for resonant converters. Steigerwald's methodology employs sine wave approximation techniques of the waveforms produced in the continuous conduction mode above resonance to estimate key values for use in component selection. Brief design examples were provided for validation of this concept [12].

A group of engineers at Auburn University published a discussion on various resonant converter topologies in their most common application, the electronic lighting ballast. Transfer functions and frequency analyses are presented in concise forms for three common resonant converter topologies. It is pointed out that the PLR converter exhibits direct proportionality between the quality factor (Q) and the load, where Q is the

ratio of reactive power to real power transferred by the resonant tank. This results in high input currents under light loading conditions but also produces high efficiency at full load [13]. Further discussion of quality factor will be presented in Chapter II.

A year after their study on secondary side resonance Swamy and Bhat published another paper detailing the development of a 1-kW PRC operating in discontinuous capacitor voltage mode (DCVM) [14]. Initially their converter appears similar to a PLRC operating in DCM with secondary side resonance; however, DCVM is borne out to be merely a special case of above resonance operation.

In 1999 there was presented a brief tutorial covering the operation of both series resonant and parallel resonant converters. This article primarily focuses on both continuous conduction modes for each of these circuits but offers some insight into the different applications for which the two types are best suited. It is pointed out yet again the characteristic voltage source property of the PLR converter. This is in contrast to the series resonant topologies which exhibit the properties of a current source [15].

In another paper published in 1999 by Garabandic there is discussed the design of a zero voltage, zero current, switching (ZVZCS) high voltage full-bridge pulse-width modulated converter using the interwinding capacitance of a high frequency power transformer [16]. Although his work has little impact on the design of PLR converters, it is an interesting alternative solution to some of the same problems which the design that will be discussed in this thesis addresses. Garabandic's work does offer insight into the design of a transformer for limiting interwinding capacitance to the secondary windings

of a multiple output transformer as well as intriguing use of the interwinding capacitance for achieving ZVZC switching.

Perhaps the work most closely related to this thesis was produced by Isurin and Cook in 2001 [17]. They describe the development of a high boost (Vout/Vin > 10) multi kilowatt class converter. The device operation shares some similarities to a PLR converter in DCM; however, they attempt to alleviate the problems associated with a large turns ratio transformer by using an active output rectifier capable of voltage multiplication. The apparent abilities of this novel topology are offset by the complexity of the controls necessary for proper operation.

Thesis Scope and Organization

This thesis describes a full-bridge parallel-loaded resonant DC-DC converter capable of converting 28 VDC to +/- 200 VDC at a sustained output of 5 kW. This device has a full load efficiency of 83% with an output voltage regulation of better than 1% over the full load envelope. To achieve this, a low inductance, high current design methodology was developed. Furthermore, a design focused not only on reducing parasitics, such as loop inductance and differential impedance, but making use of the parasitics wherever possible was employed. This thesis will report the complete details of the development of this design methodology. This thesis will also provide insight into the electrical and mechanical considerations that must be dealt with as well as an introduction to the operation of a PLR converter operating in discontinuous conductions mode.

This work is divided into six main sections. Chapter II will discuss the theory of operation of a PLR converter. Motivation for the use of DCM operation will be provided by looking into the three possible modes of operation and a mathematical model for DCM operation will be presented. Chapter III will address the practical design challenges by exploring the implications of inductor physics on bus design and component arrangement. Chapter IV will employ the information set forth in Chapter III by detailing the complete design methodology. The next chapter will discuss the construction of a prototype device and the development of a computer model of the proposed design using PSpice. Chapter VI will report experimental results. Finally, Chapter VII will summarize the results and report the conclusions drawn from this work.

CHAPTER II

PARALLEL LOADED RESONANT CONVERTER THEORY OF OPERATION

Load resonant converter is a term that is used to describe a class of converter topologies that integrate an L-C resonant tank into the circuit and apply the oscillating voltage and current waveforms it produces directly to the load. Resonant converters utilize the natural resonance of the L-C resonant tank to generate zero voltage or zero current crossings during a switching cycle. If the active components are switched during one of these zero crossing events the results would be a reduction or elimination of switching losses. This in turn allows for operation at higher switching frequencies as well as increasing efficiency compared to their hard switched counterparts. Switching of this type is referred to as zero voltage switching (ZVS), zero current switching (ZCS), or zero voltage, zero current switching depending on the conditions when the switching action occurs.

In Fig. 1.2 from the previous chapter is a schematic representation of a series resonant circuit with a capacitor in parallel with the load. In this figure the closure of the switch will effectily apply a unit step function to the resonant tank. The application of this unit step will result in waveforms shown in Fig. 2.1 for this circuit under partial

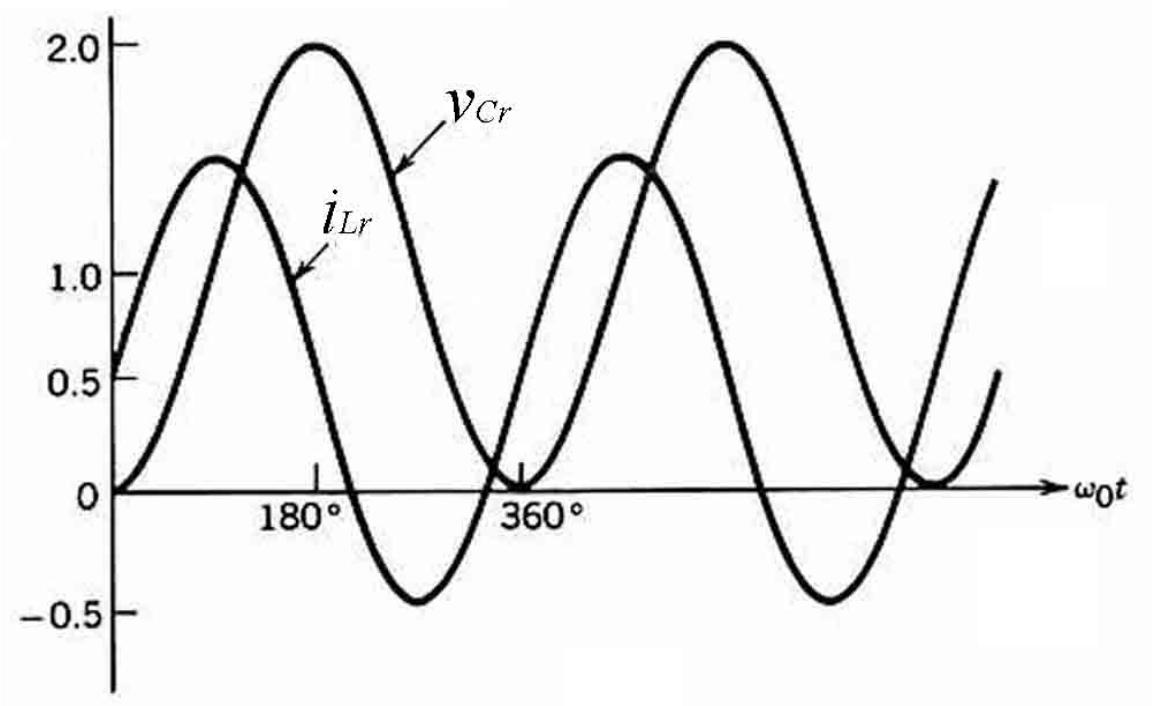


Figure 2.1: Resonant capacitor voltage and resonant inductor current waveforms for a parallel-loaded series resonant tank. (from [1])

loading of the resonant tank. For the normalized case shown in this figure the input voltage (V_d) is one and the output current (I_o) is 0.5. In the circuit of Fig. 1.2 the resonant capacitor voltage (V_{cr}) oscillates around the input voltage V_d, and in this case the unit step magnitude, and has an excursion equal to plus and minus V_d. This leads to peak resonant voltages equal to $2V_d$ while the resonant inductor current oscillates around the current through the resistive load which is I_o. The frequency of these oscillations is determined by the two components of the resonant tank as stated in Eq. 2.1.

$$\omega_o = \frac{1}{\sqrt{L_r C_r}} \tag{2.1}$$

One other item of interest from these waveforms is the zero crossings of both the resonant current and voltage. If a switch were added to the circuit of Fig. 2.1a in such a way that the source would be disconnected from the load and was turned on or off at one of these zero crossings then ideally there would be no stress on the switch. Furthermore, oscillations of the resonant tank could be controlled in this manner as well due to the fact that there would be no energy stored in the resonant tank if the switch were turned off at the zero crossings.

The Parallel loaded resonant converter refers to circuit topologies based on Fig. 1.2 where the oscillating voltage across the resonant capacitance is applied directly to the load. Typically the implementation of the PLR converter is arranged in either a half-bridge or full-bridge switching configuration due to the high power handling capabilities and these circuits and the natural ability to generate an alternating current flow through the resonant tank, although implementation in other configurations is

possible. Through proper control of the switches in the bridge topologies the simple circuit of Fig. 1.2 is essentially reproduced in a controllable manner. As with its switch-mode counter part, the full-bridge topology as used for PLR conversion has the advantage of applying the full input voltage (V_d) across the load and in this case the resonant tank. Conversely the half-bridge circuit only applies ½ V_d to the load which limits it power handling and voltage boosting abilities. This thesis is primarily concerned with PLR converters in high-power, high-boost applications; for this reason the focus of this thesis will be on the full-bridge topology, however the waveforms, operating principles, and design methodology are similar for the half-bridge.

Figure 2.2 is provided to clearly define the interconnection of the components within the full-bridge parallel loaded resonant converter. This ideal schematic eliminates the high frequency transformer found in most designs for simplicity. The anti-parallel diodes in the figure placed across ideal switches are not required; however these devices do play an important role in simplifying the control of this converter. For consistency with later chapters it is necessary to include these devices at this time. The resonant tank in the figure is comprised solely of two components, the resonant inductor (L_r) and the resonant capacitor (C_r). It should be noted that the arrangement of the resonant capacitor in this figure places it in parallel with the load. The natural resonance (ω_o) of the converter is determined by the components in the resonant tank as explained by Eq. 2.1. There also is included a full-wave bridge rectifier placed between the load, modeled as an ideal current source here and the resonant tank. This full-bridge rectifier converts

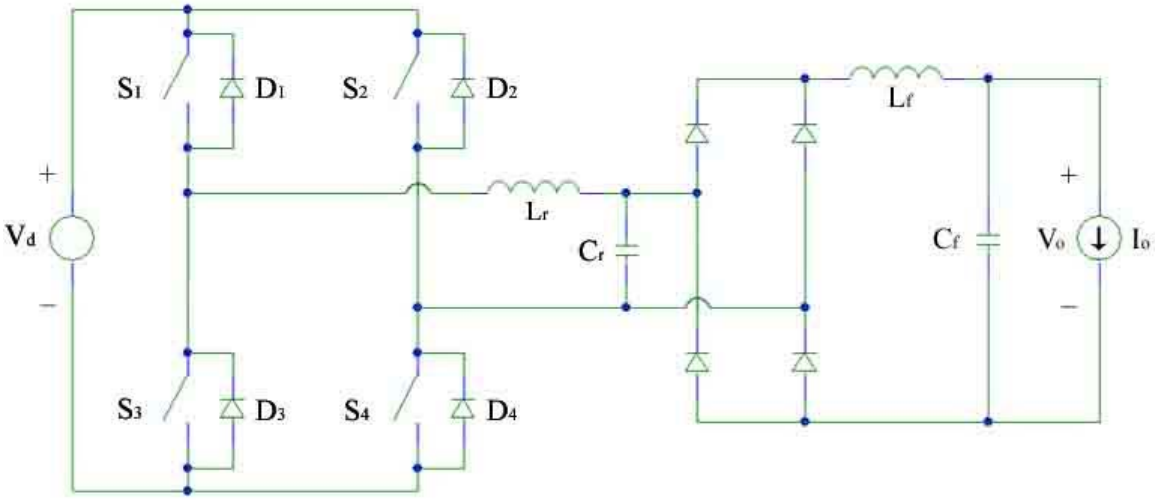


Figure 2.2: Ideal full-bridge parallel loaded resonant converter schematic

the alternating currents of the resonant tank into direct currents that are applied to the load once filtered.

Modes of Operation

There are three distinct and commonly implemented modes of operation for the PLR converter. These are discontinuous conduction mode (DCM), continuous conduction mode (CCM) switching below resonance, and continuous conduction mode switching above resonance. Each of these modes of operation is determined by the relationship between the resonant frequency and the switching frequency [1].

Discontinuous conduction mode is defined as operation where both the resonant inductor current (i_{Lr}) and the resonant capacitor voltage (v_{Cr}) are equal to zero for a finite amount of time before each half cycle of operation. This concept is made obvious by the waveforms of Fig. 2.3. This figure contains typical resonant capacitor voltage and resonant inductor current waveforms found in a PLR converter operation in DCM for one full cycle. Each half cycle contains one full resonant tank cycle thus requiring the switching frequency to be less than one half of the resonant frequency (i.e. $\omega_s < ½\ \omega_o$). Because both the current and voltage waveforms cross zero during each half cycle of operation it is possible to achieve zero voltage zero current switching (ZVZCS) when operating in discontinuous conduction mode [6]. A more thorough description of DCM operation will be covered later in this chapter.

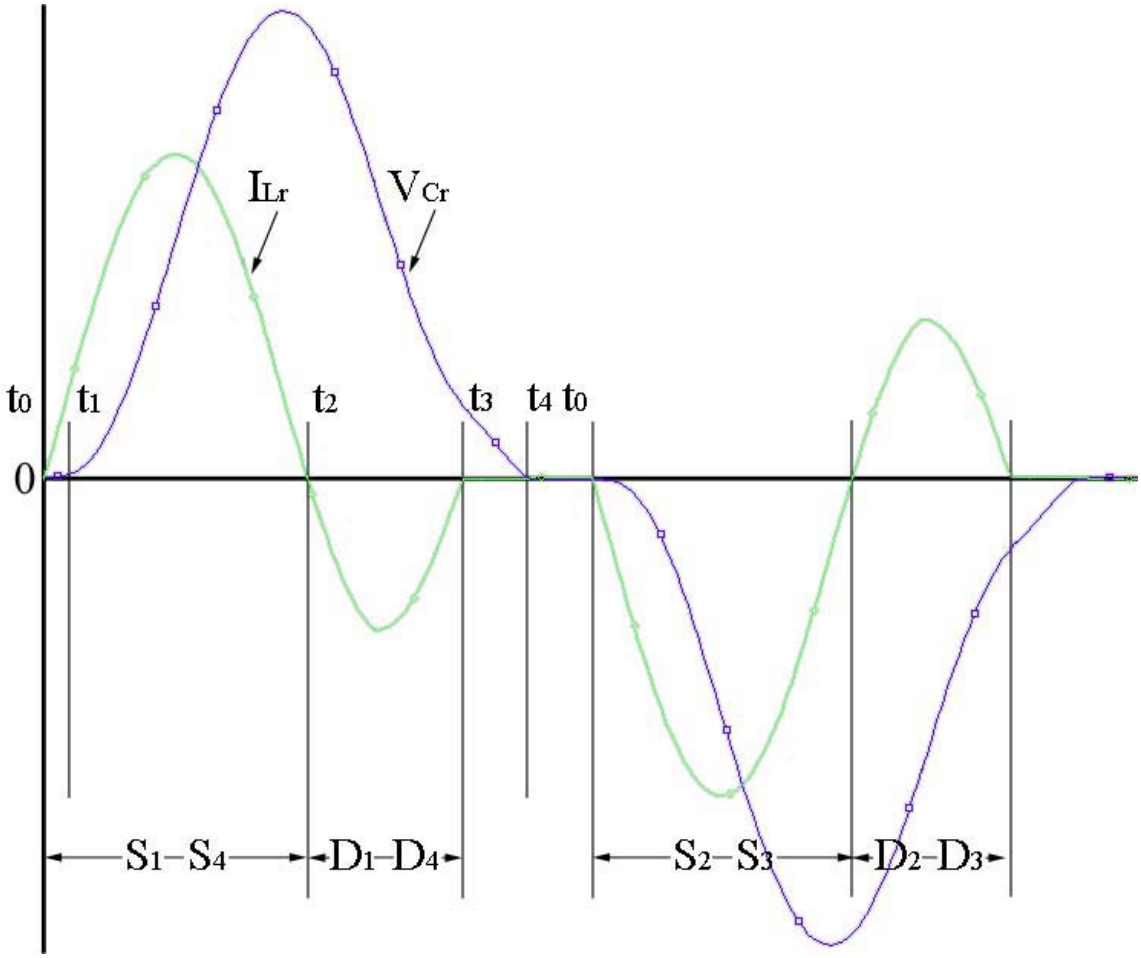


Figure 2.3: Resonant capacitor voltage (V_{cr}) and resonant inductor current (I_{Lr}) waveforms for a full-bridge PLR converter operating in discontinuous conduction mode.

Operation in continuous conduction mode is as its name implies achieved when both i_{Lr} and v_{Cr} remain continuous throughout an entire cycle of operation. Below resonance switching occurs when the switching frequency is less than the resonant frequency. However, to achieve CCM the switching frequency must be greater than or equal to one half the resonant frequency (i.e. $\frac{1}{2}\,\omega_o \leq \omega_s < \omega_o$) [5]. Figure 2.4 describes one full cycle of operation in this mode. In this figure at time equal t_0 one leg of the circuit turns on at a finite current i_{Lr} resulting in turn on losses which cannot be avoided. Later during this cycle at time t_2 this current naturally commutates from the switch to the anti-parallel diodes of the opposite leg. Due to the natural current commutation at t_2 turn off-losses are avoided [1].

A PLR converter operating in continuous conduction mode switching above resonance also has a continuous inductor current and capacitor voltage as is evident in Fig. 2.5. In this figure one leg of the full-bridge is switched on at zero current at time t_1 when current naturally commutates from the anti-parallel diodes to the switch due to the oscillations of the resonant tank. Switches are turned off some time later at time t_3, which results in turn off losses [7]. There is significant discussion in the literature of the use of "lossless" snubbers to alleviate turn off losses for this mode of operation [5, 7]. The implementation of lossless snubber capacitors is possible due to the fact switches are on during a zero voltage transition. Any energy stored in the capacitor would be delivered to the load or returned to the source because of this and not dissipated.

Traditional wisdom in power electronics holds that increasing switching frequency yields higher power density, which could explain the popularity in the

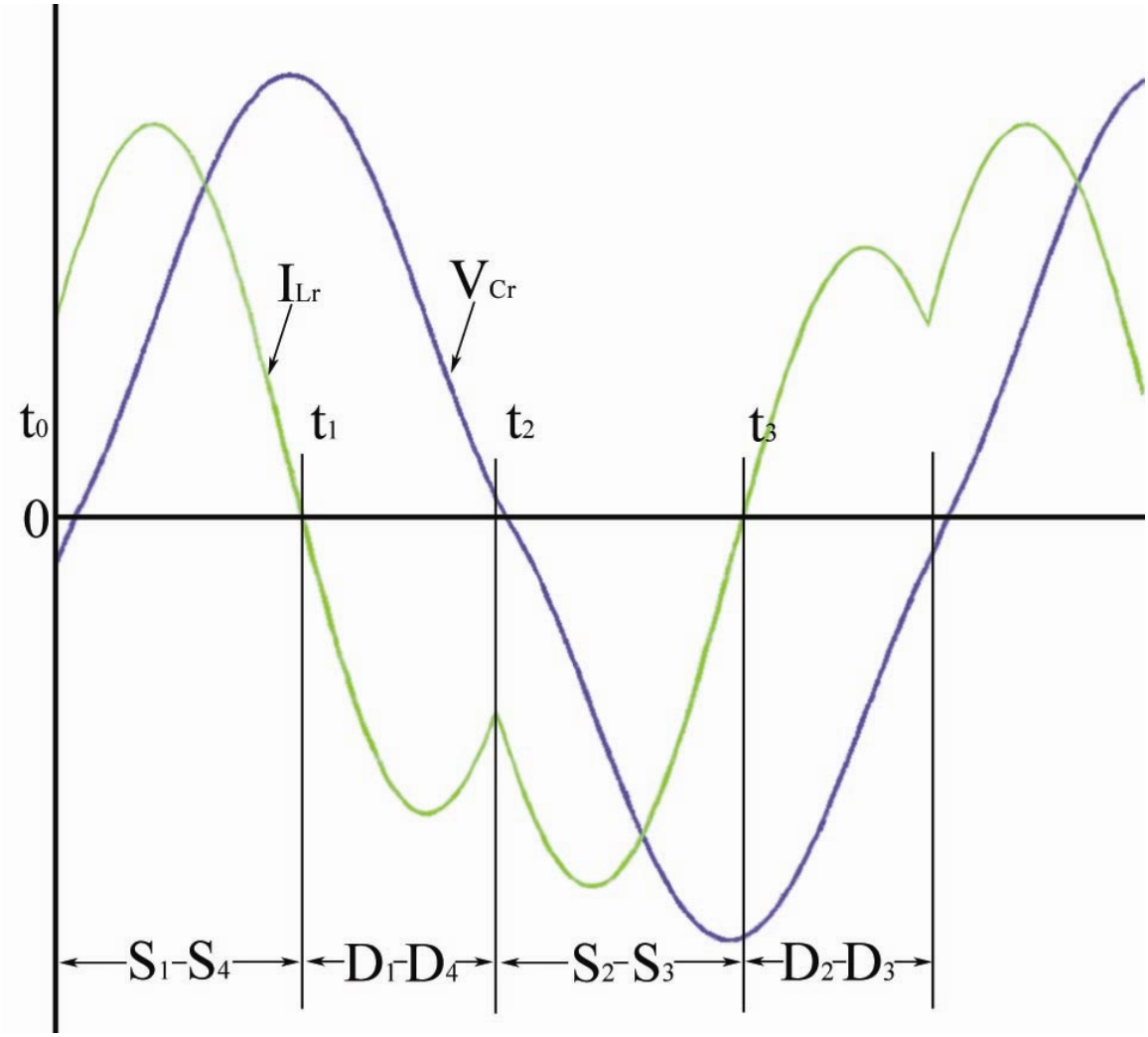


Figure 2.4: Resonant capacitor voltage (V_{cr}) and resonant inductor current (I_{Lr}) waveforms for a full-bridge PLR converter operating in continuous conduction mode below resonance switching.

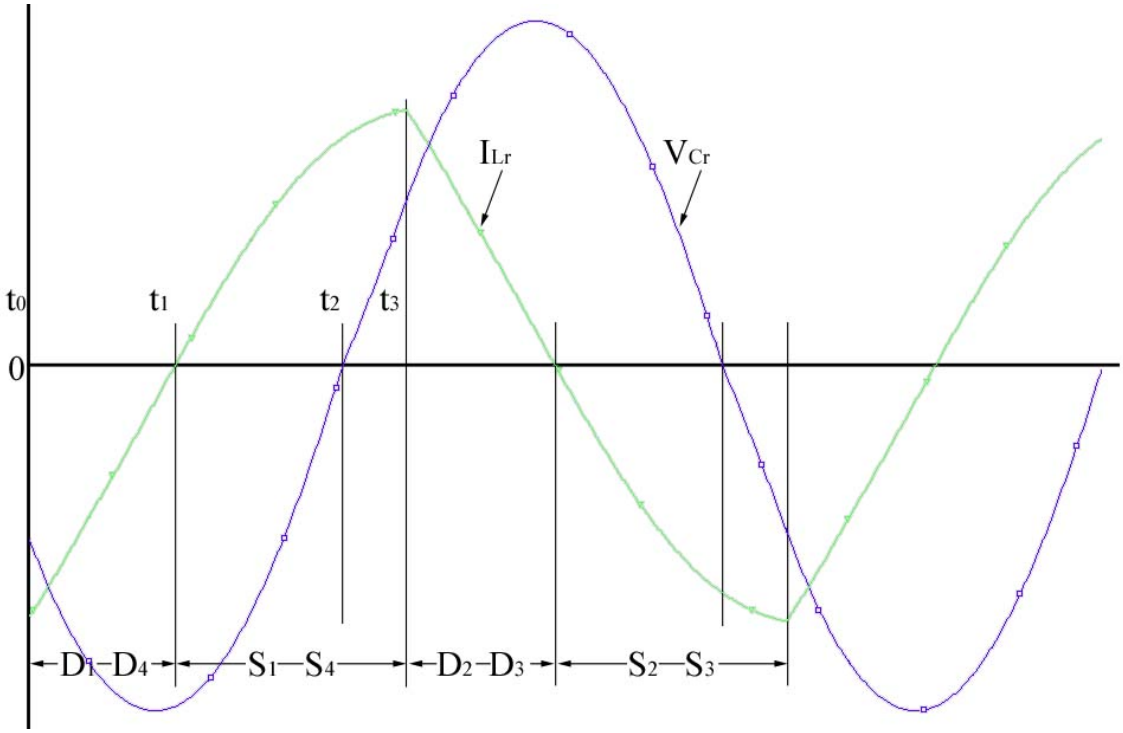


Figure 2.5: Resonant capacitor voltage (V_{cr}) and resonant inductor current (I_{Lr}) waveforms for a full-bridge PLR converter operating in continuous conduction mode above resonance switching.

literature of PLR converters switching above resonance [4, 5, 7, 9, 14]. Unfortunately increasing switching frequency often increases the effects of parasitics in most applications, including parasitics associated with lossless snubber capacitors. At high frequency and high current, the equivalent series resistance and inductance of a snubber capacitor can no longer be ignored. Furthermore, equivalent series inductance, which limits the di/dt can render these capacitors ineffectual at high frequencies and high current. Given that the work discussed in this thesis will largely concern high-frequency, low input voltage, high-current, voltage boost converters, the effects of these parasitics cannot be neglected.

Study of the frequency response of the circuit in Fig. 2.1a offers further insight into the capabilities of a converter based on the series resonant circuit with a parallel loaded capacitor. The transfer function for this circuit is

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{1}{\sqrt{\left(1-\left(\frac{\omega}{\omega_o}\right)^2\right)^2 + \left(\frac{\omega}{\omega_o Q}\right)^2}} \tag{2.2}$$

In Eq. 2.2 (Q) is a dimensionless term known as the quality factor. Quality factor is a measure of the proportionality between real and reactive power in the resonant tank as defined in Chapter I [13, 18]. The reactive power in the circuit is largely dependent upon the natural impedance of the resonant tank (Z_o). Which is defined as

$$Z_o = \omega_o L_r = \frac{1}{\omega_o C_r} = \sqrt{\frac{L_r}{C_r}} \tag{2.3}$$

Mathematical expressions defining Q as it relates the natural impedance is found in Eq. 2.4.

$$Q = \frac{\omega_o L_r}{R} = \frac{1}{\omega_o C_r R} = \frac{Z_o}{R} \tag{2.4}$$

Eq. 2.4 states that the quality factor is determined by the ratio of the natural impedance to the load impedance placed on the circuit. As the load impedance approaches Z_o the quality factor approaches one. That is to say that the maximum load that can be safely driven by a PLR converter while maintaining purely resonant operation occurs when the natural impedance of the resonant tank is matched to the load. At this point Q is equal to one and there is zero reactive power being transferred by the circuit. This allows PLR converters to achieve maximum efficiency at maximum load. This also presents a key design point which is that the resonant tank must be tuned so that the natural impedance cannot exceed the maximum load impedance. Figure 2.6 plots the transfer characteristics for the PLR circuit for frequency normalized to the natural frequency of the tank for various values of Q. The equivalent circuit model in Fig. 2.1a is upon closer inspection essentially a low pass filter. Increasing values of Q can be viewed as increasing the load impedance in parallel with the resonant capacitor. The load impedance provides damping for the resonant tank when it is excited near the natural frequency hence there is very little voltage gain for Q = 1 (i.e. critical damping), while large gains can are seen near the $\omega = \omega_o$ for high Q circuits.

It should be noted that the term “high-Q” circuit can have a double meaning. On one hand a high-Q circuit can denote a resonant tank that has been expressly designed to

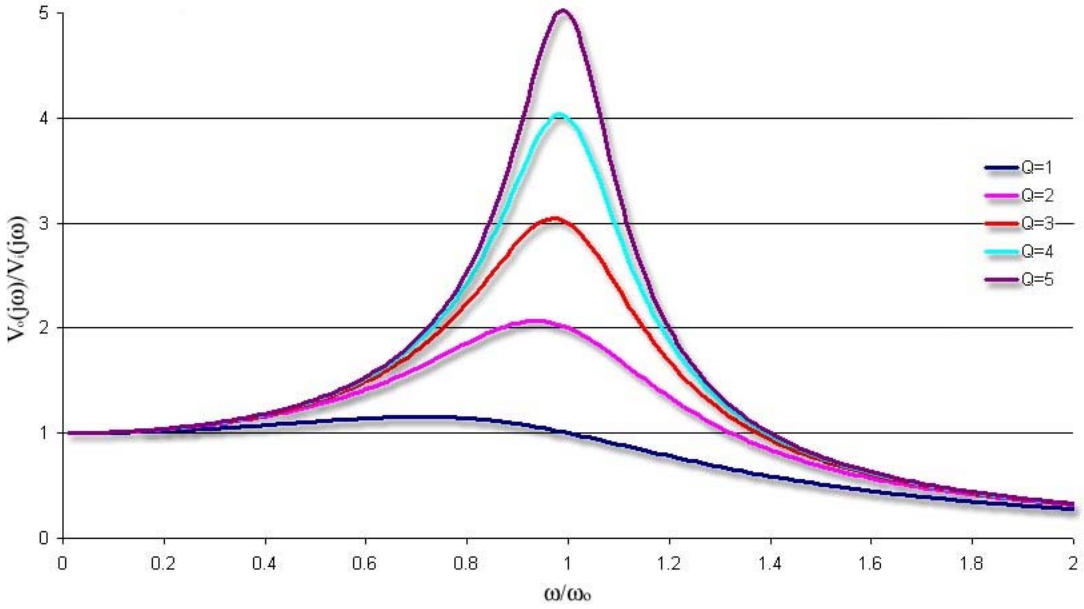


Figure 2.6: Series resonant tank with a capacitor parallel load transfer characteristics normalized to the resonant frequency.

achieve low natural impedance. On the other hand a high Q circuit could be classified as a resonant tank that is only lightly loaded hence large voltage gains are seen when exciting the circuit near the resonant frequency. Much of the literature available on the subject of PLR circuits points to the voltage boosting capabilities of operating near resonance as justification for continuous conduction mode designs [12, 19, 20]. However, designing for operation in a high Q condition can be disadvantageous due to the large amounts of reactive power that must be conducted. This reactive power leads to larger conduction losses and reduces overall system efficiency versus converters designed for a load matched natural impedance (i.e. Q=1). For excitation of the tank at low quality factor the transfer function predicts little voltage gain for all frequencies in the pass band of the resonant tank. To achieve voltage boost high Q operation is essential as the resonant tank must remain underdamped.

Another problem associated with operating near resonance is that load changes result in changes in the quality factor per Eq. 2.4. This could lead to output instability under varying load conditions for converters in continuous conduction mode. Conversely discontinuous conduction mode operates well below the cutoff frequency of the resonant tank. At these frequencies changes in Q have little effect on the voltage gain as illustrated in Fig. 2.6. This leads to relatively high independence of the output voltage for PLR converters operating in DCM with respect to the load. Avoidance of problems associated with turn-off losses and snubber capacitors, output voltage instabilities due to load changes, and inefficiencies due to the conduction of large reactive currents in high Q operation make DCM a more attractive mode of operation than CCM for many

applications. For these reasons the focus of this thesis will primarily be limited to PLR converters operating in discontinuous conduction mode.

Discontinuous Conduction Mode Operation

The following is a description of one half cycle of operation for a PLR converter in DCM and how zero voltage zero current switching is achieved. This operation can be broken down into several distinct time periods. The periods that will be described here correspond to the time marks clearly displayed in the waveform of Fig. 2.3. This waveform is typical of the operation the full-bridge circuit of Fig. 2.2. In this figure switches S_1 and S_4 and their corresponding anti-parallel diodes D_1 and D_4 each comprise one leg of the converter. The complementary leg is made of switches S_2, S_3, D_2, and D_3. The voltage across the resonant capacitor is full-wave bridge rectified by D_{S1}, D_{S2}, D_{S3}, and D_{S4}. L_f and C_f are each components of a low pass filter to provide a DC voltage to the load represented by the current source I_o.

At time t_0 in Fig. 2.3 switches S_1 and S_4 are gated on. This creates the equivalent circuit of Fig. 2.7a which is derived from the undamped L-C resonant circuit of Fig. 2.1a. At the switching instant both the resonant inductor current and resonant capacitor voltage are zero therefore, zero voltage and zero current turn on occur. Due to reconfiguration of the circuit the resonant inductor i_{Lr} begins increasing linearly until time t_1. During this period the resonant capacitor voltage, $v_{Cr,}$ is clamped at zero because until i_{Lr} reaches the value of the output current, $I_{o,}$ the output rectifiers are freewheeling. This freewheeling state of the output rectifiers is caused by the filter inductors being forced to supply the

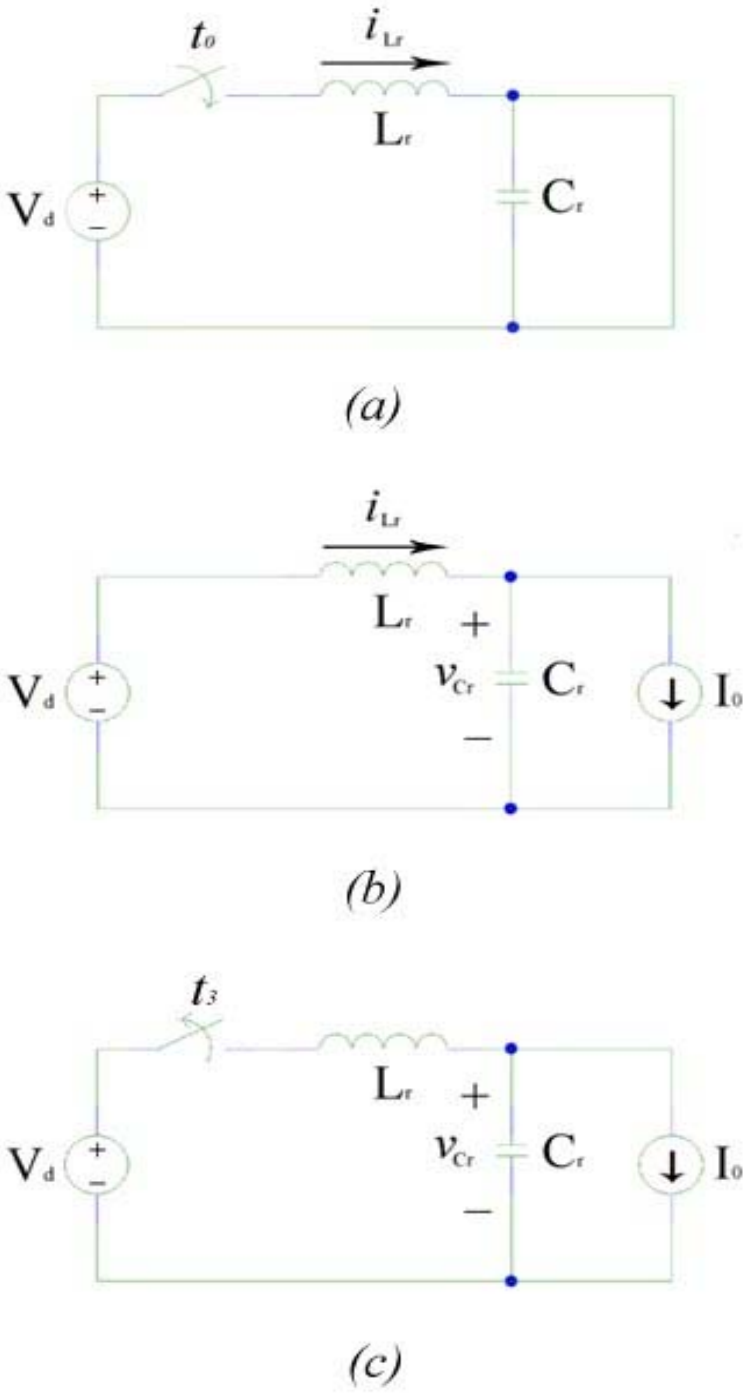


Figure 2.7: Equivalent circuits formed during each half cycle of operation of a PLR converter for discontinuous conduction mode. (a) $t = t_0$ to t_1 (b) $t = t_1$ *to* t_3 (c) $t = t_3$ to t_4

load current. Because the rectifiers are all conducting during this time, a short circuit is created across C_r.

An equivalent circuit for the period t_1 to t_2 can be found in Fig. 2.7b. During this time i_{Lr} continues increasing at t_1 and i_{Lr} begins to supply the output current I_o. The remainder of this current begins charging the resonant capacitor causing the voltage across it to rise. The resonant nature of this circuit now forces the i_{Lr} and v_{Cr} to follow a haversine curve. Between time t_1 and t_2 i_{Lr} again crosses the value of I_o and at this time v_{Cr} reaches the apex of the curve and begins to decrease as the resonant capacitor is forced to discharge to supply the portion I_o not being supplied by i_{Lr}. S_1 and S_4 naturally turn off as I_{Lr} crosses zero at time t_2 and the current is naturally commutated to the anti-parallel diodes D_1 and D_4. While D_1 and D_4 are conducting the switches S_1 and S_4 are gated off. These switches will remain off until the beginning of the next cycle. The current returns to zero at time t_3 and remains at zero until the next half cycle begins. No current is flowing through the switch when it is gated off during this interval and the anti-parallel diode turns off when it becomes reverse biased thus zero current turn off is achieved. For all practical purposes the equivalent circuit for this time period in Fig. 2.3 from t_2 to t_3 is the same as the previous period from t_1 to t_2 even though i_{Lr} is being conducted by the anti-parallel diodes. Therefore Fig. 2.7b accurately describes this period as well.

As mentioned in the previous paragraph at time t_3 the resonant inductor current has returned to zero. At this time the resonant capacitor, which still has some charge, discharges linearly while supplying I_o until the voltage across it reaches zero at time t_4.

The equivalent circuit of this period is found in Fig. 2.7c. At t_4 v_{Cr} and i_{Lr} are both zero and will remain zero until the beginning of the next half cycle when S_2 and S_3 are turned on. The output rectifiers begin freewheeling to allow the filter inductors to supply current to the load. They will remain in this state until I_{Lr} can supply the entire load current. The next half cycle of operation is identical to this description with the currents and voltages in and across the resonant components being inverted [21].

Mathematical Analysis of Discontinuous Conduction Mode Operation

The following analysis will describe the operation of the resonant tank mathematically as it relates to the previous section. This will effectively be a circuit analysis of each of the circuits in Fig. 2.7. The active components of the full-bridge circuit, if assuming these components are ideal, will produce discontinuities which cannot be reconciled mathematically. Therefore this analysis must address each phase of operation in a piecewise fashion. This analysis also assumes operation under steady-state conditions. The foundation for this analysis is based on a specific case of operation for the circuit in Fig. 2.1. That case being that at the start of each period both the resonant inductor current and resonant capacitor voltage begin at zero. This produces a result for the resonant inductor current and resonant capacitor voltage found in Eqs. 2.5 and 2.6 [1].

$$i_{Lr}(t) = \frac{V_d}{Z_o} \sin \omega_o (t - t_0) \tag{2.5}$$

$$v_{Cr}(t) = V_d \left[1 - \cos \omega_o (t - t_1)\right] \tag{2.6}$$

Defining operation in DCM is not a simple matter of using these two equations to describe the resonant operation of the tank due to the fact that the resonant period does not begin when the switch closes at (t) equal zero in Fig. 2.7a. First a determination must be made of what occurs before the beginning of the resonant period, when does the resonant period begin, and what are the initial conditions at that time.

At time equal to t_0 in Fig. 2.3 and 2.7a the following initial conditions exist

$$I_{Lr_o} = 0 \tag{2.7}$$

$$V_{Cr_o} = 0 \tag{2.8}$$

While $i_{Lr}(t)$ is less than the output current I_o the output filters will maintain I_o as a constant given that they have sufficient energy storage capability. This forces the output rectifiers into a freewheeling state to provide a path for this current. The freewheeling action of the rectifiers effectively produces a short circuit across the resonant capacitor. This forces the voltage across the resonant capacitor to remain zero until $i_{Lr}(t)$ is greater than I_o at t_1. With this being the case Eqs. 2.9 and 2.12 define the resonant capacitor voltage and the resonant inductor current respectively from t_0 to t_1.

$$V_{Cr}(t) = 0 \qquad \text{for} \qquad t_0 \le t < t_1 \tag{2.9}$$

The resonant inductor current is found from a basic relation for inductance given in Eq. 2.10.

$$V_d = L_r \frac{di_{Lr}}{dt} \quad \text{for} \qquad t_0 \le t < t_1 \tag{2.10}$$

Integration of both sides of Eq. 2.10 yields Eq. 2.11.

$$i_{Lr}(t) = \frac{V_d}{L_r} \cdot t \quad \text{for} \qquad t_0 \le t < t_1 \tag{2.11}$$

Eq. 2.11 is consistent with the previous section describing a linear current rise of $i_{Lr}(t)$ for this period of operation.

The period of operation from time t_1 to t_3 is as was stated earlier defined by the equivalent circuit of Fig. 2.7b. Time t_1 is the beginning of the resonant period. The initial conditions for this period are

$$i_{Lr}(t_1) = I_0 \tag{2.12}$$

$$V_{Cr}(t_1) = 0 \tag{2.13}$$

Time t_1 marks the start of the resonant cycle as the output rectifiers are no longer producing a short circuit across the resonant capacitor and the remainder of the resonant current not supplying I_o begins charging C_r. At this time the resonant inductor current begins to oscillate around a point determined by I_0. Its maximum value can be found simply by using ohms law

$$i_{Lr\max} = \frac{V_d}{Z_0} + I_0 \tag{2.14}$$

Applying the initial condition of Eq. 2.12 to Eq. 2.5 it can be deduced that the proper form of $i_{Lr}(t)$ can be described by Eq. 2.15.

$$i_{Lr}(t) = \frac{V_d}{Z_0} \cdot \sin \omega_0 (t - t_1) + I_0 \qquad \text{for} \qquad t_1 \le t < t_3 \ [1] \tag{2.5}$$

where time t_1 is derived from Eq. 2.11 and presented in Eq. 2.16.

$$t_1 = \frac{L_r}{V_d} I_o \tag{2.16}$$

Finding a function describing the resonant capacitor voltage can be found using the same method as employed for finding Eq. 2.15. Being that it is known that $V_{Cr}(t)$ is a function that based on Eq. 2.6 and that the same initial condition is still true. $V_{Cr}(t)$ now begins at t_1 instead of t_0 as stated in Eq. 2.17.

$$V_{Cr}(t) = V_d[1 - \cos\omega_0(t - t_1)] \qquad \text{for} \qquad t_1 \le t < t_3 \ [5] \tag{2.17}$$

The last unknown quantity in Fig. 2.7b is the resonant capacitor current which can simply be found using Kirchoff's current law

$$i_{Cr}(t) = i_{Lr}(t) - I_0 \qquad \text{for} \qquad t_1 \le t < t_3 \tag{2.18}$$

The next period begins at t_3 when i_{Lr} returns to zero and the anti-parallel diode ceases to conduct current at t_3. This ends the resonant period of operation as the current path linking the two resonant components has been broken. With no path for current to flow through L_r, as depicted in Fig. 2.7c, the inductor current will remain at zero as stated in Eq. 2.19.

$$i_{Lr}(t) = 0 \qquad \text{for} \qquad t_3 \le t < t_4 \tag{2.19}$$

At this time there is still potential across the resonant capacitor which must be discharged before the rectifiers can begin freewheeling to allow output filter to supply I_0 during this dead period. Therefore the resonant capacitor will discharge at a rate determined by I_0 until the voltage across it reaches zero. The rate of discharge is of course proportional to the capacitance as shown in Eq. 2.20

$$v_{Cr}(t) = v_{Cr}(t_3) - \frac{I_o}{C_r} \cdot (t - t_3) \qquad \text{for} \qquad t_3 \le t < t_4 \tag{2.20}$$

where t_3 is found using Eq. 2.21 which is derived from 2.17.

$$t_3 = 2\pi - \sin^{-1}\left(\frac{Z_o I_o}{V_d}\right) + t_1 \tag{2.21}$$

Once the potential across the resonant capacitance reaches zero at time t_4 the rectifiers begin freewheeling again and remain in this state until t_0 which initiates the next half-cycle of operation.

DC conversion using parallel load resonance is achieved simply by rectifying and filtering the high frequency waveforms produced by the resonant tank. Mathematically the DC output voltage can be determined by integration of the resonant capacitor voltage over one half cycle [6].

$$V_o = \frac{2}{T_s}\left[\int_{t_1}^{t_0} V_{Cr}(t)dt + \int_{t_1}^{t_3} V_{Cr}(t)dt + \int_{t_3}^{t_4} V_{Cr}(t)dt\right] \tag{2.22}$$

$$V_o = \frac{2}{T_s}\left[\int_{t_1}^{t_3} V_d\left(1 - \cos\omega_o(t - t_1)\right)dt + \int_{t_3}^{t_4}\left(v_{Crt3} - \frac{I_o}{C_r}(t - t_3)\right)dt\right] \tag{2.23}$$

where

$$T_s = \frac{2\pi}{\omega_s} \tag{2.24}$$

therefore

$$V_o = \frac{\omega_s}{\pi}\left[V_d\left((t_3 - t_1) - \frac{\sin\omega_o(t_3 - t_1)}{\omega_o}\right) + \left(v_{Crt3}(t_4 - t_3) - \frac{I_o(t_4 - t_3)^2}{2C_r}\right)\right] \tag{2.25}$$

To determine the DC gain is simply a matter of dividing Eq. 2.25 by the input voltage which yields Eq. 2.26.

$$\frac{V_o}{V_d} = \frac{\omega_s}{\pi}\left[\left((t_3 - t_1) - \frac{\sin\omega_o(t_3 - t_1)}{\omega_o}\right) + \frac{\left(v_{Crt3}(t_4 - t_3) - \frac{I_o(t_4 - t_3)^2}{2C_r}\right)}{V_d}\right] \qquad (2.26)$$

Plotting V_o/V_d versus switching frequency shows the linear response of the output with the switching frequency as shown in Fig. 2.8. This figure has been plotted for several values of I_o; however, this may not be apparent in this figure due to the fact that changes in the load have little effect on the voltage conversion ratio. As mentioned previously load changes effectively change the quality factor for the resonant tank. However, operation in discontinuous conduction mode has now been proven to be unaffected by changes in Q. In Fig. 2.8 the dc gain for each of the different loads calculated will be laid on top of each other resulting in only a single visible plot. The linear frequency response and the independence from changes in the load give rise to an exceptionally stable voltage source topology.

Figure 2.8 not only proves that their exists a linear relationship between the switching frequency and dc voltage gain for an ideal case in discontinuous conduction mode operation, but also shows the simplicity of attaining a given output voltage through modulation of the switching frequency. Similar to pulse-width modulation, output voltage control is achieved through adjustment of a quantity known as duty ratio (D). This is the ratio between the conduction period of the switching elements and the time between switching cycles. Unlike PWM converters, PLR converters have a fixed

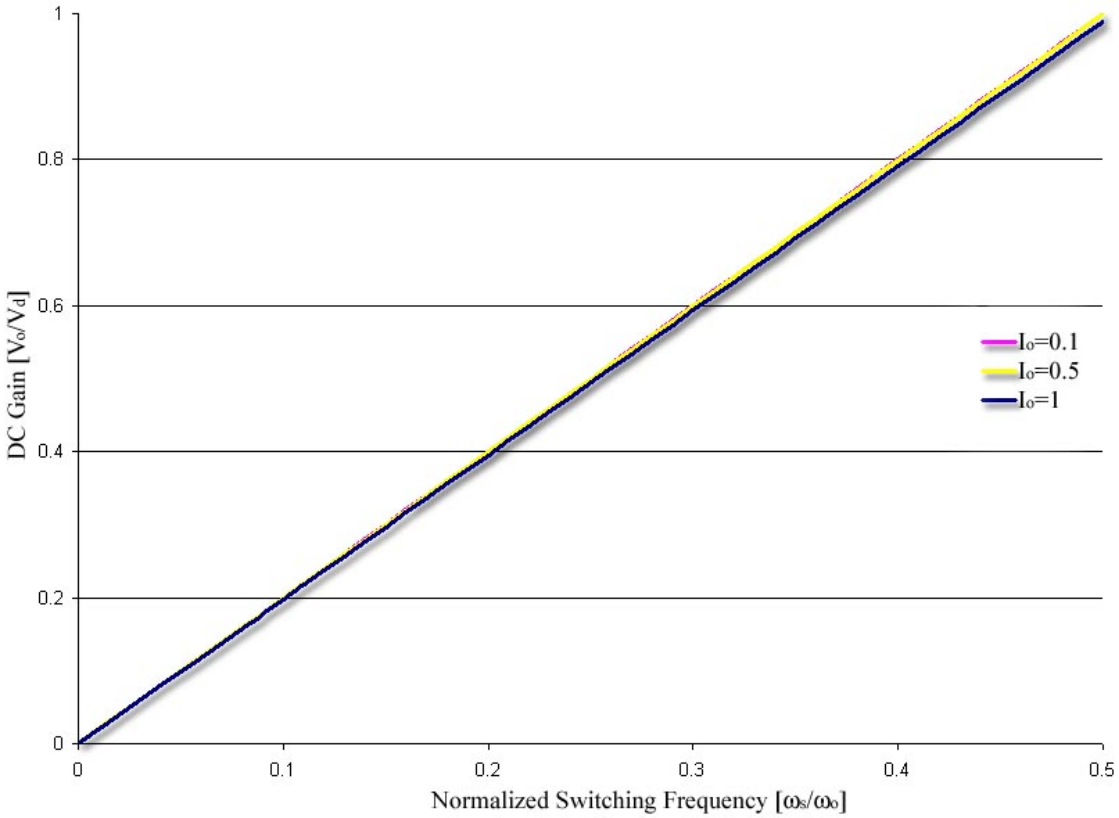


Figure 2.8: DC gain for a PLR converter operating in discontinuous conduction mode.

conduction time determined by the natural frequency of the resonant tank. The inability to change the conduction period results in a need to modulate the periodicity of the fixed resonant cycles. Therefore, adjustment of the switching frequency can be used to control the duty factor for producing a desired output voltage. The duty ratio for PLR converters operating in discontinuous conduction mode operation is determined using Eq. 2.27.

$$D = \frac{2\omega_s}{\omega_o} \tag{2.27}$$

The complete operation of an ideal full-bridge PLR converter operating in discontinuous conduction mode has now been covered. A strong foundation having been laid for use of this topology as a high power voltage source the following chapters will detail a complete design methodology for implementing a functional kilowatt class PLR high voltage boost dc-dc converter. The key to this methodology will be the development of an approach for coping with the non-idealities associated with designing such a converter. A validation for this methodology will be presented in the form of an experimental PLRC constructed at Mississippi State University.

CHAPTER III

PRACTICAL DESIGN CONSIDERATIONS

Low voltage high power systems present unique challenges to power electronic designers trying to achieve efficient energy conversion with high power density. A significant voltage step ($V_{out}/V_{in}>10$) further complicates the problem with parasitics from a high turns ratio transformer. While resonant converter topologies are well suited for utilizing these parasitic components they cannot be all together overlooked, this is especially true for high frequency operation. Through careful examination of these elements and the physics that causes them, a method for minimizing their effect can be achieved. This chapter aims to identify, examine, and minimize both the size and effect that parasitic components have on the operation of PLR converters.

It was shown in Chapter II that for all three modes of operation a direct relationship exists between the switching frequency and resonant frequency. Therefore, to achieve higher switching frequencies it is necessary to increase the resonant frequency as well. According to Eq. 2.1 ω_o is solely dependent upon the resonant inductance and resonant capacitance. Increasing the resonant frequency can only be accomplished by reducing L_r and/or C_r.

For applications involving low input voltage and large voltage boosts a large number of transformer secondary turns will be required. A disadvantage of the chosen

converter topology is the high peak currents associated with the resonant nature of the waveforms. The resonant inductor current waveform in Fig. 2.3 helps make this point evident. At full load these currents can often exceed twice the amplitude of the dc input current. Operating at higher resonant frequencies can reduce the stress imposed by these peak resonant currents while allowing for higher switching frequency operation which will reduce the required size of passive components. Unfortunately higher frequency operation only serves to exacerbate problems associated with parasitic elements. Therefore, to maximize output power, efficiency, and power density it is essential to maximize both the resonant frequency and the switching frequency while minimizing the natural impedance of the resonant tank.

Determining the maximum load for a converter design is essentially impedance matching the resonant tank to the desired load. The maximum current that can be delivered to a resistive load can be determined by Ohm's law as described by Eqs. 3.1 and 3.2.

$$Z_o = R_{load} \tag{3.1}$$

$$I_o = \frac{V_o}{Z_o} \tag{3.2}$$

If the maximum load that can be efficiently driven is fixed by Z_o, and resonant frequency and switching frequency are inversely proportional to the size of the resonant components, only a reduction of the resonant inductance will produce both higher switching and resonant frequencies while reducing the natural impedance which directly translates to an ability to drive larger loads [21].

Elimination of the resonant inductor as an externally realized component will aid in the minimization of the total resonant inductance with in any converter; however, parasitic elements present in any circuit can serve as a resonant element. Utilization of these parasitics within the resonant tank is a critical step to achieving high frequency operation simultaneously with low natural impedance. Placing the resonant capacitance across the secondary winding of a high frequency transformer will allow both the primary loop inductance as well as the transformer leakage inductance to serve as part of the resonant tank [5, 7, 8, 11, 14, 22]. The schematic of Fig. 3.1 is included to illustrate a PLR converter design including a high frequency transformer. Figure 3.1 shows this placement of the resonant capacitance across the secondary winding of the transformer. In this configuration the total resonant inductance is simply the sum of the loop inductances (L_{loop}) and transformer leakage inductance ($L_{leakage}$) as defined by Eq. 3.3.

$$L_r = L_{loop} + L_{leakage} \tag{3.3}$$

In this caveat on the basic full bridge PLR topology the parasitic inductances become a vital element in the converter operation. While it is still necessary to minimize them to as great an extent as possible to achieve high resonant frequencies and low natural impedance, these components no longer pose detrimental effects to the proper operation of the circuit. Strictly speaking, these elements are not parasitic quantities in this

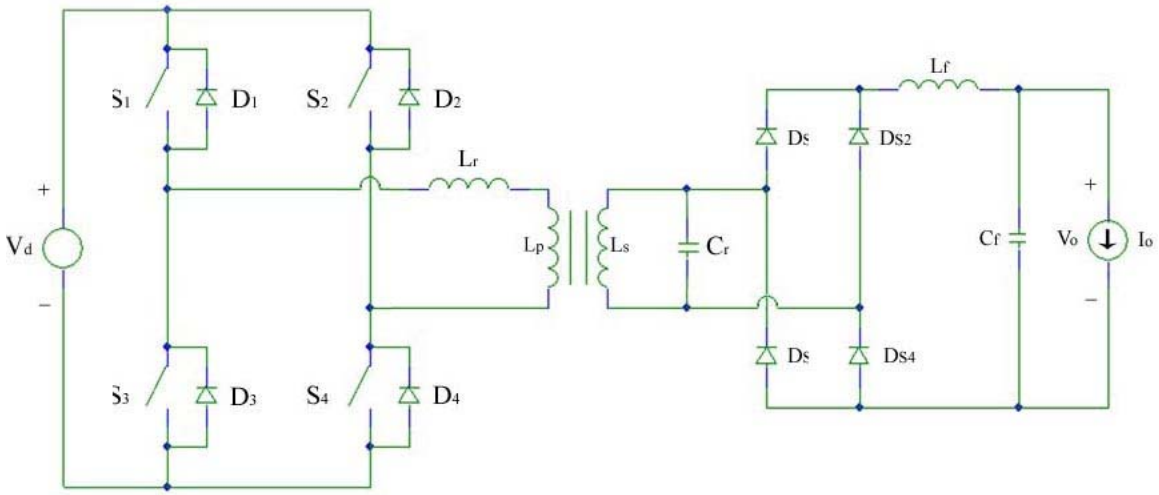


Figure 3.1: Schematic of a full-bridge parallel loaded resonant converter including a high frequency transformer with the resonant capacitor across the secondary winding.

capacity. This simplifies circuit design, reduces component stress and leads to increases in efficiency.

Inductor Physics

The design of any converter involving high current will require the design of a bus to carry this current to any of the major components of the chosen topology. That being the case the design of such bus work on an academic level is often overlooked as evidenced by the limited literature on the subject. Typical literature shows component layouts based on efficient thermal design with electrical interconnections taking a secondary role. Often times the inefficiencies generated by the parasitics associated with the interconnections are tolerated and dealt with through the use of power dissipating snubber networks. However, as explained in the previous section, parasitic inductance, specifically those associate with transformer leakage inductance and primary loop inductance, can play a critical role in not only efficient but effective operation in certain converter topologies such as load resonant converters. Higher power and higher frequency converters depend greatly on the designer's efforts to limit these non-idealities.

To understand how to limit these parasitics requires a closer look into the physics of their generation. This section will review some of the basic elements of induction which will be employed in Chapter IV to develop the layout methodology used in the prototype converter design. The first element for understanding induction, as it will apply to the successful development of a prototype PLRC, is the special case for the magnetic field generated by two parallel plate conductors carrying the same current in

opposite directions as illustrated in Fig. 3.2. The magnectic field for this case can be found using Eq. 3.4.

$$B = \frac{\mu_o I}{d} \tag{3.4}$$

Where B is the magnetic field generated, μ_o is the permeability of free space, I is the current in the conductor, and d is the width of the conductor normal to the flow of the current within it. Eq. 3.4 states that any flow of current produces a magnetic field whose strength is proportional to the rate at which the current is flowing and the size of the conductor through which it is flowing [23]. The path enclosed by any current loop consequently generates a magnetic flux. It can be shown that the magnetic flux of any current loop is greatly dependent on the geometry of the current loop. For simplicity, and for reasons which will soon be made clear, this chapter will look at the effects of a current path involving two parallel plates and neglect the effect of the necessary interconnection between these two plates. The magnetic flux generated by current flowing through two parallel plate conductors is then

$$\Phi_m = BA = \frac{\mu_o I}{d} A \tag{3.5}$$

In Eq. 3.5 Φ_m is the magnetic flux and A is the cross-sectional area defined by the current path, in this case two parallel plate conductors. Obviously there exists a strong direct relationship between magnetic flux and the area defined by the current path as shown in Fig. 3.2. This leads directly to the definition of inductance in Eq. 3.6 which is also dependent on conductor geometry as it incorporates Eq. 3.5.

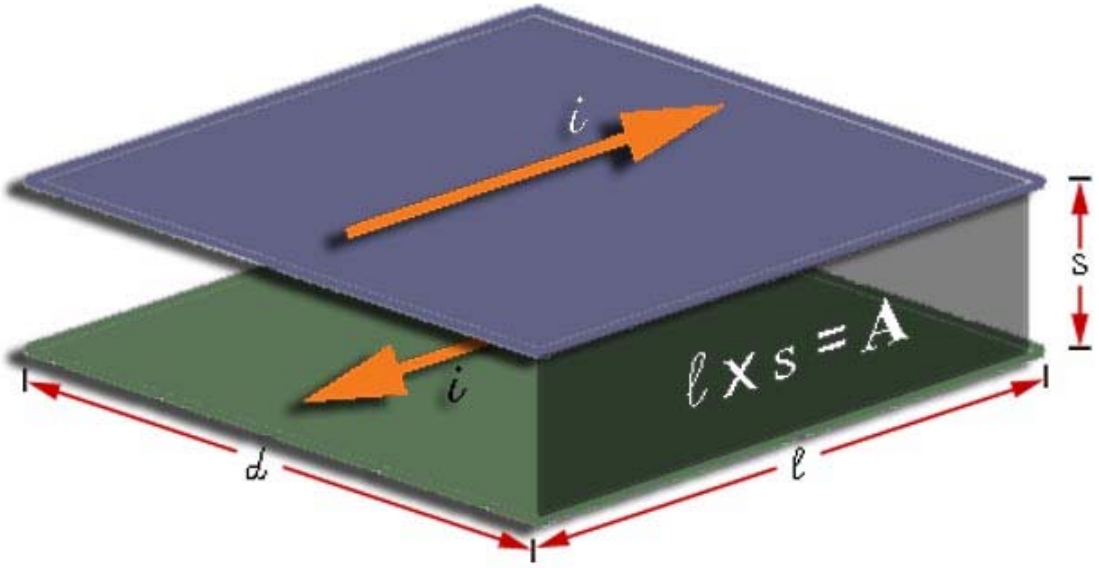


Figure 3.2: Cross-sectional area of a current path enclosed by two parallel plate conductors.

$$L = \frac{\Phi_m}{I} = \frac{\mu_o A}{d} \tag{3.6}$$

According to Eq. 3.6, inductance is directly proportional to the cross-sectional area defined by the current path. Reducing the area created by the flow of current in any circuit design should have the net effect of reducing the parasitic loop inductance associated with it. Figure 3.2 further explains the cross-sectional area that the current path defines. This path is separated into two parts for this simple geometry, length (*l*) and separation distance (s) combine to create the area (A). The width (*d*) of the current path is another item of merit in the definition of the loop inductance which is inversely proportional to the inductance. Therefore, in order to minimize the primary loop inductance of the proposed full-bridge PLR converter, reducing the total cross-sectional area of current flowing in the primary will be the most important factor to consider for the primary interconnections and component layout in the prototype. Increasing the width of the current path is another effect element in reducing the primary loop inductance as well as the current density in the primary current path.

High Frequency Transformer Design Considerations

The specifics of the design of a high frequency transformer fall outside the scope of this thesis. However, pragmatic decisions must be made when specifying the design of the transformer in a PLR converter. Primary concern in this transformer design is the minimization of leakage inductance as the leakage inductance contributes to the total resonant inductance as explained in the preceding section. The effort to reduce leakage inductance will often require the concession of low magnetizing inductance (L_{mag}), but

given that high frequency operation is a design goal low magnetizing inductance in the transformer is not a significant issue. High magnetizing inductance will reduce di/dt required for magnetic coupling in the transformer but at high frequency Δt is short and peak currents are naturally governed by Z_o. Therefore, based on these factors, in order to reduce the transformer leakage inductance the number of transformer turns should be kept to a minimum. This often demands that for a boost transformer the primary will contain only a single turn.

For achieving high frequency operation, skin effect issues cannot be neglected. However, given that high currents associated with a high power low voltage application, reducing conductor size to accommodate skin effect limitations is not practical. This naturally leads to a strip wound transformer design. Wide yet thin conductors will allow for high current conduction while eliminating any issues associated with skin effects by reducing conductor thickness to that equal to or less than the penetration depth which the operating frequency dictates.

A secondary issue for transformers with large turns ratios is the interwinding capacitance. This problem is further complicated by the strip wound construction previously mentioned. Fortunately, just as the leakage inductance is incorporated into the resonant inductance, the secondary interwinding capacitance is similarly incorporated into the resonant capacitance. Unlike the resonant inductance, reduction of the resonant capacitance is not a critical design goal. Reducing the capacitance will produce higher resonant frequencies; however it will increase the natural impedance. Therefore it is often necessary to add capacitance to the resonant tank to achieve the desired natural

impedance to drive the full design load. This issue will be elaborated in the discussion of layout methodology in Chapter IV.

Figure 3.3 is included as a derivative of Fig. 3.1. This figure presents the major parasitic elements discussed in this chapter as equivalent components. The primary loop inductance is not actually realized as a single series component but rather is distributed over the entire current path. For practical purposes this approximation is useful for developing an accurate circuit model. Parasitics of second order concern, such as the equivalent series inductance of the source, have been neglected in this circuit. Problems such as these will be dealt with before the development of an experimental device.

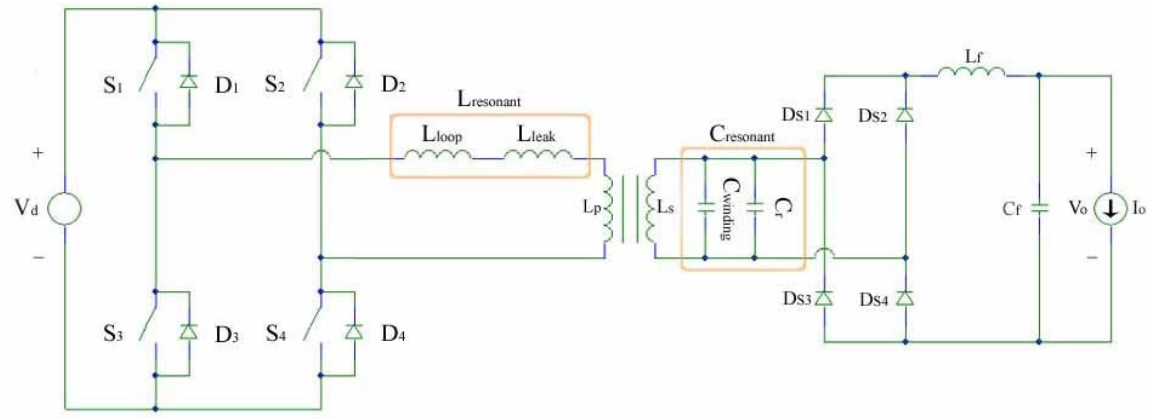


Figure 3.3: Schematic of a full-bridge PLR converter including transformer and primary loop parasitic elements.

CHAPTER IV

LAYOUT METHODOLOGY

The design goals of this particular PLR converter are in general high power, high power density, and high efficiency. The path to achieving these goals are found in high frequency operation, zero voltage zero current switching, and low natural impedance. Sound design principles must be established to attain these objectives, particularly for large boost applications. This chapter aims to explain how converter layout can be focused on attaining these goals while incorporating the essential aspects of high current conduction, sound thermal design, and practical assembly.

Utilization of Parasitics

The major parasitic components of this design loop inductance, leakage inductance, and interwinding capacitance are by nature elements which are inherent to any design and unfortunately cannot altogether be eliminated. They may be put to useful purpose which can reduce or eliminate their deleterious effects on converter operation. As it applies to parallel load resonance one simple solution for incorporating all three of the mentioned components into the resonant tank is to place the resonant capacitance of the resonant tank across the secondary windings of a boost transformer.

Utilization of parasitics does not eliminate the need to minimize their occurrence in converter design. As explained in Chapters II and III, the size and the ratio of the resonant components determine the resonant frequency, switching frequency, and natural impedance of the converter. The minimization of these elements will produce increased power, increased power density, and increased efficiency for any given converter design. Chapter III laid out the principles for reducing the primary loop inductance and transformer leakage inductance. These ideas will be employed in this chapter to achieve the goal.

Reducing Current Path Length

Switch placement with respect to the transformer is the largest determining factor in the primary current path length. Any layout for the full bridge circuit should place the primary switches as close to the high frequency transformer as possible. The shortening of this distance will help to reduce loop inductance as the current path length is a significant factor producing inductance. If this path were not kept to a minimum, the total path length will produce large inductances incorporated into the resonant tank and could lead to complex geometries that produce stray inductances that cannot be used by the resonant tank. These stray inductances can lead to distortion of the resonant wave form that could increase electromagnetic interference and also inhibit current commutation during switch transitions. This will lead to either commutation losses in the switches or to the need for dissipative snubber circuits to aid commutation. This in turn increases the complexity of the converter design and layout and decreases efficiency due

to the energy lost in the switches or snubbers. The commutation losses due to these inductances can eliminate the benefits of zero voltage zero current switching in parallel load resonant topologies.

A DC source is used to power the full bridge circuit; however, the switching of the resonant tank requires AC currents to be delivered. In practice it is often not feasible to place the source directly at the input terminals of the converter. This leads to large inductances between the source and the high side switches of the bridge. The source itself is typically inductive in nature as well. This places limits on the rate of change of current that can be supplied. A solution to this problem must be found which decouples the source from the AC currents in the resonant tank. Placing energy storage elements in the form of a large capacitive bank should achieve this goal. This bank should be large enough so that it is capable of delivering practically 100% of the AC currents circulating in the primary current path. The input energy storage capacitance reduces the overall inductive current path of the circuit by effectively moving the source from an external supply to a point within the converter. The source is only required to deliver DC current which is not affected by inductance.

Typically the input capacitors will be an aluminum-electrolytic construction specifically designed for low equivalent series resistance (ESR) and equivalent series inductance (ESL). The ESL and ESR of most large aluminum-electrolytic capacitors should be minimal but cannot be overlooked. These two elements are in the primary current path and contribute to the resonant tank. Although the input capacitance is required to deliver AC currents, electrolytic capacitors can be used as the voltage is still

unipolar. The primary winding of the transformer does see an AC voltage and current but due to the design of the full bridge circuit the input voltage does not fluctuate so long as parasitic inductance has been eliminated between the input and the high side switches. The capacitors must have low ESR as this resistance will lead to energy dissipation in the capacitors that not only decreases efficiency but manifests as heat generated in these components and reduces their effectiveness as energy storage elements. Furthermore, the energy dissipation in the capacitors can lead to failure of these devices. The ESL of the capacitors is an element that will add inductance to the primary current loop. Again this is detrimental to the goal of reducing the inductance of this path.

The input capacitors should be arranged so that they are as close as possible to the switching elements. This will aid in the reduction of the current path. Again, the AC input for the current path effectively begins and ends at the input capacitors. Therefore, to reduce the current path length the input capacitors should be placed in close proximity to both the input of the high side switches and the output of the low side switches.

Reducing Current Path Separation Distance

Reducing the length of the current path is only half the solution to minimizing the loop inductance. Since it is necessary to minimize the total cross-sectional area of the current loop the forward and return current path must be placed in close proximity to each other. The simplest geometry to achieve this would be the use of planar bus bars for all of the interconnections. This type of connection will allow the return current path to be placed underneath or above the forward current path with only a thin insulating

material separating them. This should all but eliminate the area of the path defined by the current thus greatly minimizing the inductance. This arrangement is consistent with the analysis of inductance in Chapter III.

If a heatsink is required by the design an aluminum extrusion formed with a flat surface on one side will allow some components to be attached directly to it with a planar bus designed to be placed on this surface. The semiconductor components placed on this heatsink will require packaging that includes an isolated pad for mounting to this sink. Given that aluminum is highly conductive this heatsink may then serve as the return current path. The forward current path can be separated from the heatsink by a thin insulating material thus achieving the goal of minimizing *S*, simplifying the layout of the primary components, and eliminating the need for a separate bus for returning currents to the source. The separation distance of the total cross-section of the current path will be reduced to the thickness of the material separating the forward and return paths The use of planar busses has the added advantage of reducing the skin effects associated with high frequency current provided that its thickness is selected based on the penetration depth defined by the frequency of operation. Some designs may necessitate the use of laminated busses to achieve low AC resistance.

Placement of Secondary Components

Due to the nature of large turns ratio boost transformers the placement of components on the transformer secondary is not as critical as the component placement on the primary side. The boost transformer actually has two important benefits when the

resonant capacitance is placed across the secondary windings. If the turns ratio is defined as stated in Eq. 4.1,

$$a = \frac{N_2}{N_1} \tag{4.1}$$

then the resonant capacitance placed across the secondary windings is reflected to the primary by the inverse square of the turns ratio.

$$C_{r\_pri} = C_{r\_\sec} \cdot a^2 \tag{4.2}$$

This reduces the size of the additional resonant capacitance required to achieve the desired natural impedance and resonant frequencies for large boost applications. Because of the voltage boost large amounts of energy can be stored in a relatively small amount of resonant capacitance.

The secondary loop inductance conversely is reflected to the primary with the inverse square of the turns ratio.

$$L_{\sec(reflected)} = \frac{L_{\sec}}{a^2} \tag{4.3}$$

This fact eliminates the secondary loop inductance as a first order problem. Any design involving a large boost turns ratio will likely reduce the reflected inductance to an insignificant value. The secondary loop inductance should not go overlooked, however, and is a concern for any converter not needing a large turns ratio. The resonant capacitance and the output rectifiers should be placed as close to the secondary windings of the high frequency transformer as possible but this is not a key point in designing the component layout as was the case with the primary components. Finally, the inductance

of any current path on the output side of the rectifier is of no consequence. Typically a large filter inductor will be part of the output filter; any inductance found in connections on the output side of the rectifiers should be in series with the filter and will likely be dwarfed by this filter inductance.

Adherence to the principles laid out in this chapter will yield an extremely low inductance primary current loop. This has been shown to be crucial for the construction of a PLR converter which can achieve both high resonant frequency and low natural impedance. These two qualities lead to efficient designs with high power density.

To summarize, the keys to utilizing and minimizing the effects of parasitics in a full bridge parallel loaded resonant converter, incorporation of the parasitics into the resonant tank is essential. This is achieved by placing the resonant capacitor on the secondary of the high frequency transformer which allows the total series inductance of the primary as well as the secondary interwinding capacitance of the transformer to be used in the resonant tank. Minimizing the transformer leakage inductance and primary loop inductance is critical to achieving low natural impedance and high resonant frequency operation. Using a minimal number of transformer turns and arranging components in a fashion that produces the smallest possible cross-sectional area of the primary current loop will yield low resonant inductance.

CHAPTER V

MODELING, SIMULATION, AND PROTOTYPE DESIGN

The motivation for the design methodology detailed in the previous chapters was due to the need for providing regulated high voltage DC power derived from a 28 V vehicle battery/alternator source. The specific alternator in question is a 400 A model produced by the Neihoff Corporation. An initial point design was first developed based on the characteristics of the source and the load. The rigorous constraints imposed by the preliminary design specifications led to the need to develop the design methodology that has been detailed and employed in the prototype that will be discussed in this chapter. The experimental device provides validation for both the design methodology and the model based on it principles.

Point Design

A point design was developed to initially detail the design specifications and goals. Many of the design specifications for this point design were derived from the constraints imposed by the source limitations or load requirements. These specifications are detailed in Table 5.1. For implementation of the converter design the full-bridge

Table 5.1

Converter Point Design Specifications

V_{in}	=	24 V – 32 V
V_{out}	=	400 V
$V_{out\ reg}$	<	± 1%
$I_{in\ max}$	=	245 A
$I_{out\ max}$	=	12.5 A
$P_{in\ max}$	=	5.88 kW
$P_{out\ max}$	=	5.00 kW
η	>	85%
$f_{s\ nominal}$	>	100 kHz

topology was selected for it power handling ability. The decision to proceed with a resonant design was borne out of the difficulties encountered when using a large turns ratio transformer and the high switching losses that would be otherwise incurred due to large input currents. This selection led naturally to the choice of the PLR converter operating in discontinuous conduction mode as a suitable resonant circuit based on the analysis in Chapter II and because of the low switching stress, stable voltage source characteristics, and the lack of a series capacitor. The lack of a series capacitor is an important design selection element because of the prohibitively large primary currents this component would encounter.

Component Selection

Using the terminal specifications along with the basic theory of operation of a PLRC the selection of specific components was required before further development of the design could proceed. Due to the limited option in the packaging of components, which is a large determining factor in the design of the interconnections, specific device selection will play a crucial role in determining the arrangement of the components. The transformer is the one component which requires the greatest effort in designing but also affords the greatest design flexibility as this will likely be a custom made part.

The primary concern of the transformer design for this particular converter is the leakage inductance. The leakage inductance of the boost transformer will play an essential role in yielding successful operation of the proposed design as this parasitic element will contribute to a large portion of the total resonant inductance. The large

number of secondary windings needed to produce substantial boost leads to interwinding capacitance that must be considered as well. A complete design of the high frequency transformer is outside the scope of this thesis; however a point design similar to the initial converter point design in the previous section must be preformed to establish the operating conditions the transformer will encounter.

The turns ratio (a) is the most critical parameter to be determined. The process for selecting the minimum turns ratio required to achieve a desired DC output voltage is fairly straight forward as defined by Eq. 5.1.

$$a = V_{out} \Big/ (V_{in\_\min} \cdot D_{\max}) = \frac{400V}{24V \cdot 0.95} = 17.54 \cong 18 \qquad 5.1$$

Where (a) is defined by Eq. 4.1 and the maximum duty ratio has been set at 95% to provide a small margin for maintaining DCM operation. The value arrived at in Eq. 5.1 must be rounded to the nearest whole number to ensure that the desired V_{out} can be reached and whole turns are wound. For this converter design the bipolar output will be derived from a center-tap on the transformer, therefore the turns ratio must also be an even value to produce an equal number of turns on either side of the transformer center-tap.

The maximum terminal voltages present on the windings will be related to twice the DC input voltage due to the resonant tank. Eqs. 5.2 and 5.3 define these values.

$$V_{pri\_\max} = 2V_{in\_\max} \qquad 5.2$$

$$V_{\sec\_\max} = 2 \cdot V_{in\_\max} \cdot a \qquad 5.3$$

The maximum DC input and output currents of the converter can be used as estimates of the current ratings for which these windings should be designed. Although large peak currents are present, the DC values are representative of the average current present. The maximum power provided by the source which is related to the maximum input voltage and current can be used to specify the kVA rating of the transformer.

At this stage of the design it is difficult to determine the maximum switching frequency that can be achieved without an established value of resonant inductance. The initial operating frequency stated in the point design must be used in specifying the transformer operating frequency. This value is slightly more muddled due to the modulation of the switching frequency to regulate the output voltage. The transformer specifications determined by the point design is listed in Table 5.2. A specification commonly found in many transformer designs not presented here is the magnetizing inductance. However, due to the proposed high frequency operation and a need to minimize leakage inductance a large magnetizing inductance is not critical in the transformer point design.

The primary switches which are connected directly to the transformer primary windings must be capable of conducting the full load current, withstand the full input voltage and be able to operate at frequencies greater than 100 kHz. It would also be advantageous if these parts were packaged with anti-parallel diodes in order to reduce the total number of components and simplify the interconnections. Switches that can be easily paralleled could broaden the scope of the component selection while simultaneously reduce the series inductance imposed by the component packaging and

Table 5.2

High Frequency Transformer Specifications

$V_{pri\ max}$	=	64 V
$V_{sec\ max}$	=	1152 V
$I_{pri\ max}$	=	350 A
$I_{sec\ max}$	=	12.5 A
kVA_{max}	=	10 kVA
f_s	=	100 kHz
N	=	1:18

reduce the on state resistance. The MOSFET is the switch technology that best meets all of these criteria. Fortunately at 28 V the modest input voltage is well within the current state of available technology. However, the extremely large input currents will require several devices in parallel for each of the four switches if the targeted operating frequency is to be reached. International Rectifier's FB180SA10 is a MOSFET that meets all of the criteria required of this component. It will be necessary to employ five of these devices in parallel to ensure that the high resonant currents can be conducted. A fortunate advantage of this part is the packaging. This MOSFET is housed in an SOT-227 package. This package has screw terminal inputs and an isolated base which will allow for simple secure, low inductance connection to the primary bus and the device can be thermally bonded directly to the heatsink without providing any electrical insulation.

The selection process for the output rectifiers is similar to the switch selection; however these components must be able to tolerate the higher voltage low current conditions that occur at the transformer secondary terminals. Present technology of silicon based components limits most fast switching rectifiers to a DC blocking voltage of 1200 V. This is only slightly higher than the maximum voltage present on the secondary transformer windings. Fairchild semiconductor produces a 1200 V ultrafast rectifier (RURG30120) capable of conducting 30 A which does meet the stated requirements for this component. Table 5.3 provides a listing of the key criteria used in selecting both the switches and rectifiers.

Table 5.3

Semiconductor Component Specifications

Switch			**Rectifier**		
V_{DS}	≥	64 V	V_{RM}	≥	1200 V
I_D	≥	245 A	$I_{F(AV)}$	≥	12.5 A
f_s	≥	100 kHz	f_s	≥	100 kHz

Without a reference for the amount of resonant inductance present it is difficult to select the resonant capacitance, resonant frequency, and maximum switching frequency without experimental results. In the point design a target of 100 kHz nominal switching frequency was selected. This will require the resonant frequency to be 1.57 Mrads/s at a duty factor of 80% under the nominal input voltage of 28 V. The natural impedance of the resonant tank should be matched to the maximum load impedance as explained in chapter two. From the point design Z_o can be determined as shown in Eqs. 5.4 and 5.5.

$$Z_{o\_\sec} = \frac{V_{out}}{I_{out}} \cdot \eta \cdot D = \frac{400V}{12.5A} \cdot 0.85 \cdot 0.80 = 21.7\ \Omega \tag{5.4}$$

$$Z_{o\_pri} = \frac{Z_{o\_\sec}}{a^2} = 0.067\ \Omega \tag{5.5}$$

Using the natural impedance desired for a given resonant frequency the resonant capacitance can be shown to be

$$C_{r\_pri} = {}^{1}\!\!\diagup\!\!_{\omega_o \cdot Z_{o\_pri}} = 9.48\ uF \tag{5.6}$$

The implementation of this PLR design will place the resonant capacitance on the secondary of the transformer. The value found in Eq. 5.6 is the equivalent capacitance reflected to the primary as seen by the resonant tank. The actual capacitance placed on the secondary windings is determined using Eq. 5.7.

$$C_{r\_\sec} = \frac{C_{r\_pri}}{a^2} = 29.2\ nF \tag{5.7}$$

Metallized polyester film capacitors designed for use in snubber applications are well suited for the role required by the resonant capacitance. This capacitor technology is

ideally matched for the high voltage high frequency environment of the secondary. The metallized film capacitor typically has extremely low equivalent series resistance and inductance which will contribute insignificant impedances to the resonant tank.

Using the calculations for the resonant capacitance a maximum value of primary loop inductance can be determined for reaching the design goals. A base value for L_r is calculated in Eq. 5.8.

$$L_r = \frac{1}{\omega_o^{\,2} \cdot C_{r\_pri}} = 42.8 \ \ nH \qquad 5.8$$

The value of resonant inductance found in Eq. 5.8 can be used in the preliminary design model but will likely change once experimentally determined values of resonant inductance are found.

Component Arrangement and Bus Design

A solid copper bus was design to make interconnections between the selected components using the low inductance principles described in Chapters III and IV. An extruded aluminum heatsink with a large planar surface was selected which served as a base for the converter primary layout. The two legs of the full bridge circuit were created by placing the MOSFETs in two rows each containing 10 devices. Each row contained switches alternating in orientation. The FETs in these rows either comprise the high side switch of one leg or the low side switch of the opposite leg depending on orientation and termination. The low side switches were terminated directly to the heatsink. This allowed the heatsink to serve as the return path for primary currents. This arrangement required that the input bus be split into two segments laid along the outer edges of the top

surface of the heatsink. These segments of the input bus were isolated from the heatsink using a “sil pad” produced by Berquist. Other parts of the primary bus network were isolated in a similar fashion. With the heatsink conducting the return current, the placement of the separation distance between the forward and return current paths is only the thickness of the sil-pad separating the two paths. The transformer was placed in cavity beneath the top plane of the heatsink between the two rows of MOSFETs. This provides a secure location for this component while placing it in close proximity to both legs of the full-bridge circuit. Two large banks of aluminum electrolytic capacitors were similarly placed in cavities underneath the two segments of the input bus providing the necessary input energy storage Figures 5.1 and 5.2 illustrate the description of the primary layout. Figure 5.1 is provided to show a clear illustration of how the primary components are to be arranged. The blue boxes in this figure (labeled 1-5 and 16-20) comprise one leg of the full-bridge topology. The high side switches (1-5) are terminated to the input bus and one input of the transformer primary winding. The low side switches (16-20) are placed on the opposing side of the high side switches. These devices are terminated to the second input to the transformer primary winding and to the heatsink. The complementary leg of the converter is arranged in a similar fashion although the connections to the transformer are opposite to those of the leg already described. The switches in the complementary leg are represented by the orange boxes (labeled 6-15).

Figure 5.2 further illustrates the arrangement of the primary components in the form of a cross-section which describes how each of the components is oriented with respect to the planar surface of the heatsink. Underneath the top surface the input

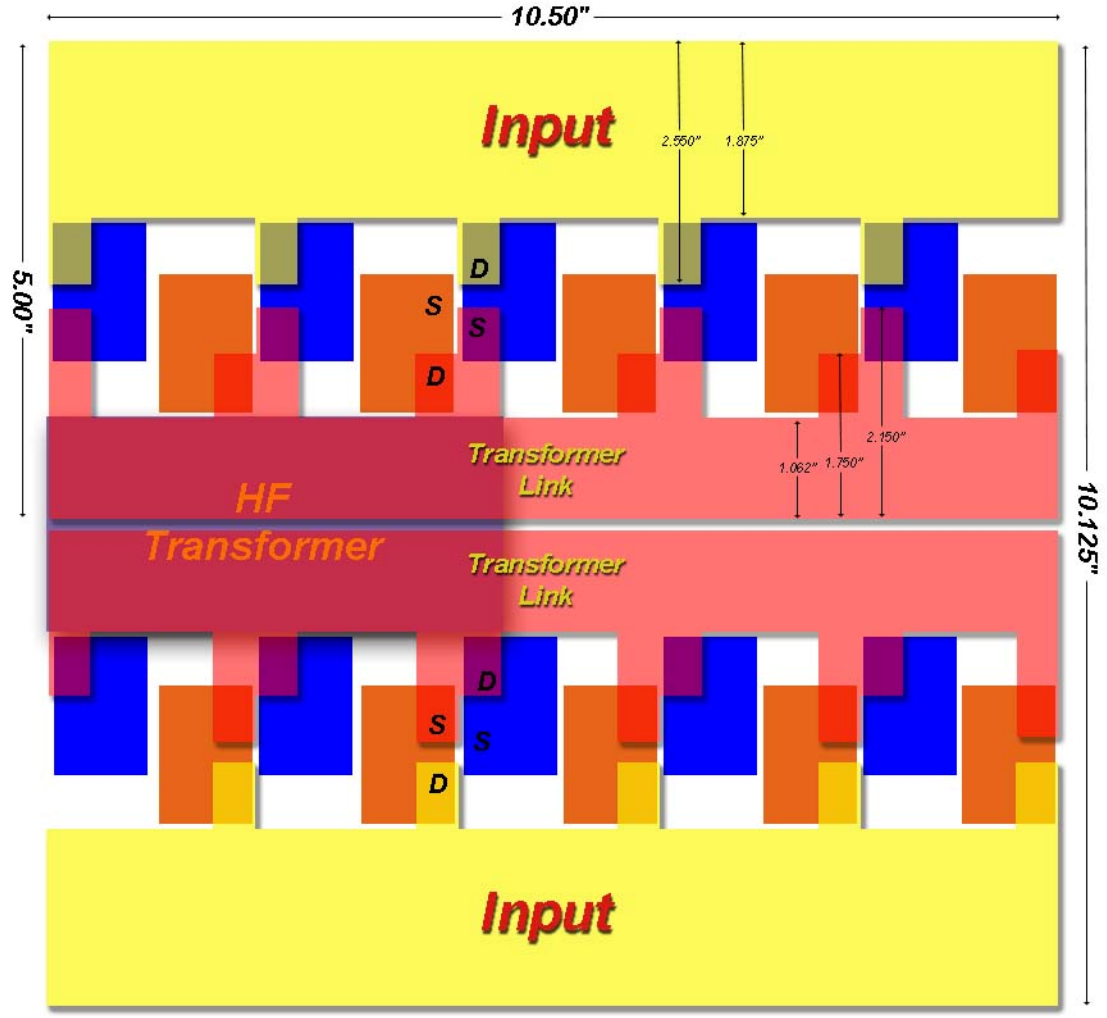


Figure 5.1: Illustration of primary component arrangement and interconnections

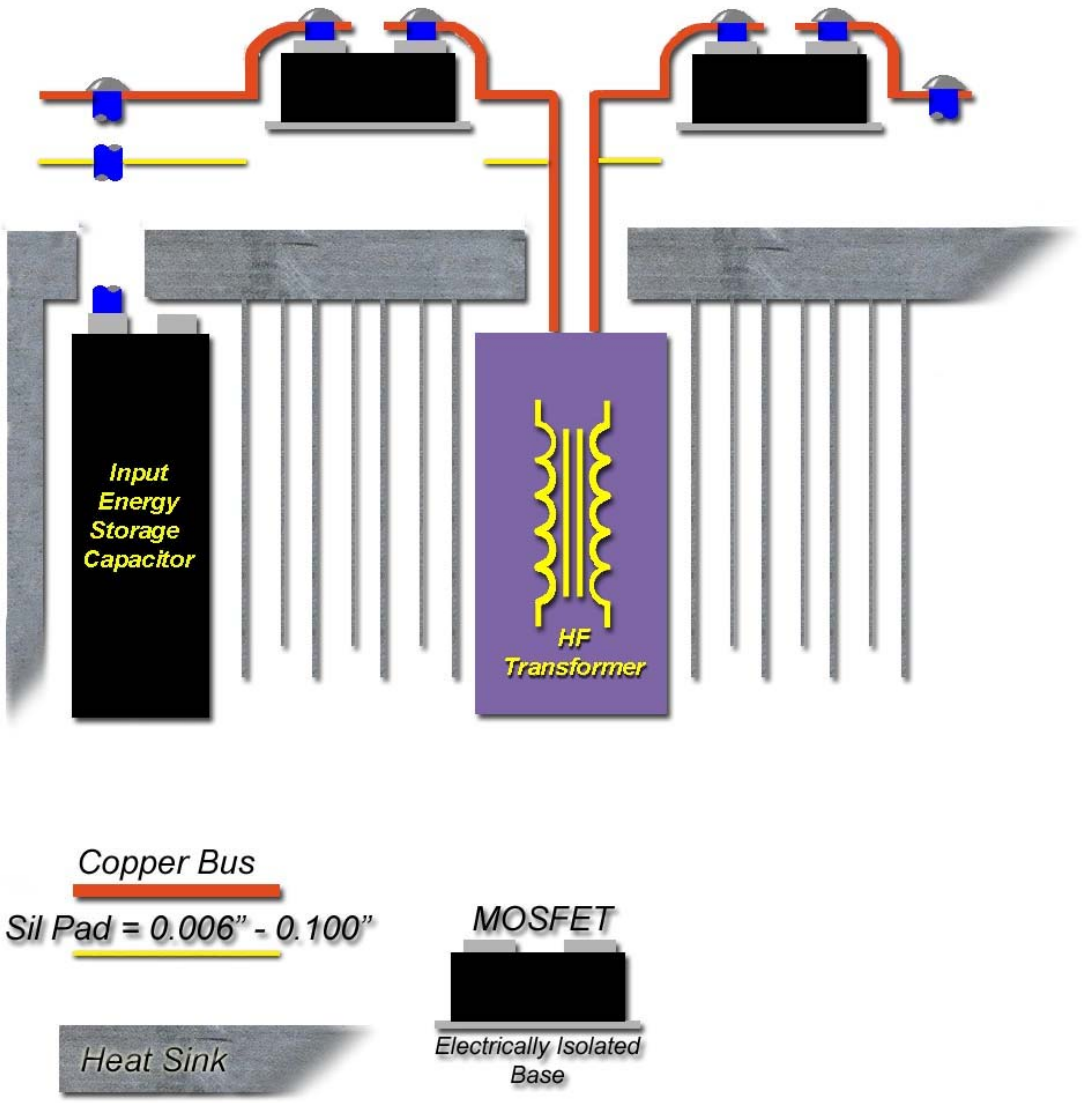


Figure 5.2: Illustration of primary bus cross-section and component arrangement

capacitors and the transformer have been placed in cavities created by removing heatsink fins. The switches and the primary bus are fixed on top to the heatsink's planar surface. Thus all of the components in the primary path are densely packed and secured. The heatsink fins have not been removed from the space directly beneath the switches in order to help reduce the thermal impedance to ambient of these components in order to ensure thermal stability. The transformers and capacitors have also been arranged specifically to allow for unimpeded air flow across these fins.

Modeling and Simulation

Utilizing the selected components an accurate model of the physically realized prototype can be developed. This model offers an opportunity to find inherent design flaws before completion of the prototype. Most manufacturers of the components utilized in this design provide detailed data sheets that will allow for the inclusion of parasitic and otherwise non-ideal elements into the model. Some manufactures offer accurate computer based component models that can be used in conjunction with electric circuit design capture software.

The development of a useful model must consider accepting certain approximations for some of the unknown elements as well as utilizing simulation techniques that will provide steady-state results without requiring prohibitively large file sizes or simulation run times. Therefore the initial model will estimate the values of the resonant tank components to be those that will produce viable natural impedance and switching frequency from the point design. These values have already been calculated in

Eqs. 5.4 through 5.8. The source should include a large series inductance to limit the AC currents as expected in operation that will force the input capacitor models to deliver the majority of the high frequency currents. This in turn will require that the proper initial conditions be set on the capacitors as well as including the ESL and ESR values supplied in the data sheet. Finally in an effort to produce a useful model the output filter will be eliminated. In its place a DC current source will mimic both the filter and load operation to produce equivalent results of steady state operation of a highly inductive filter by forcing a constant current be delivered to the load.

With all of the known model non-idealities included and useful approximations for unknown values determined a schematic for the completed model is provided in Fig. 5.3. Using PSpice circuit design software the simulation results for the model are show in Figs. 5.4 and 5.5. Figure 5.4 are the results for operation under light load conditions while Fig. 5.5 was performed for full load operation. The results are similar to the ideal model as expected and simulation agrees in general with PLR converter theory of operation. Chapter 6 will detail the experimental results of the model developed in this chapter. A more accurate model utilizing the experimentally determined values for the resonant components is included in appendix A.

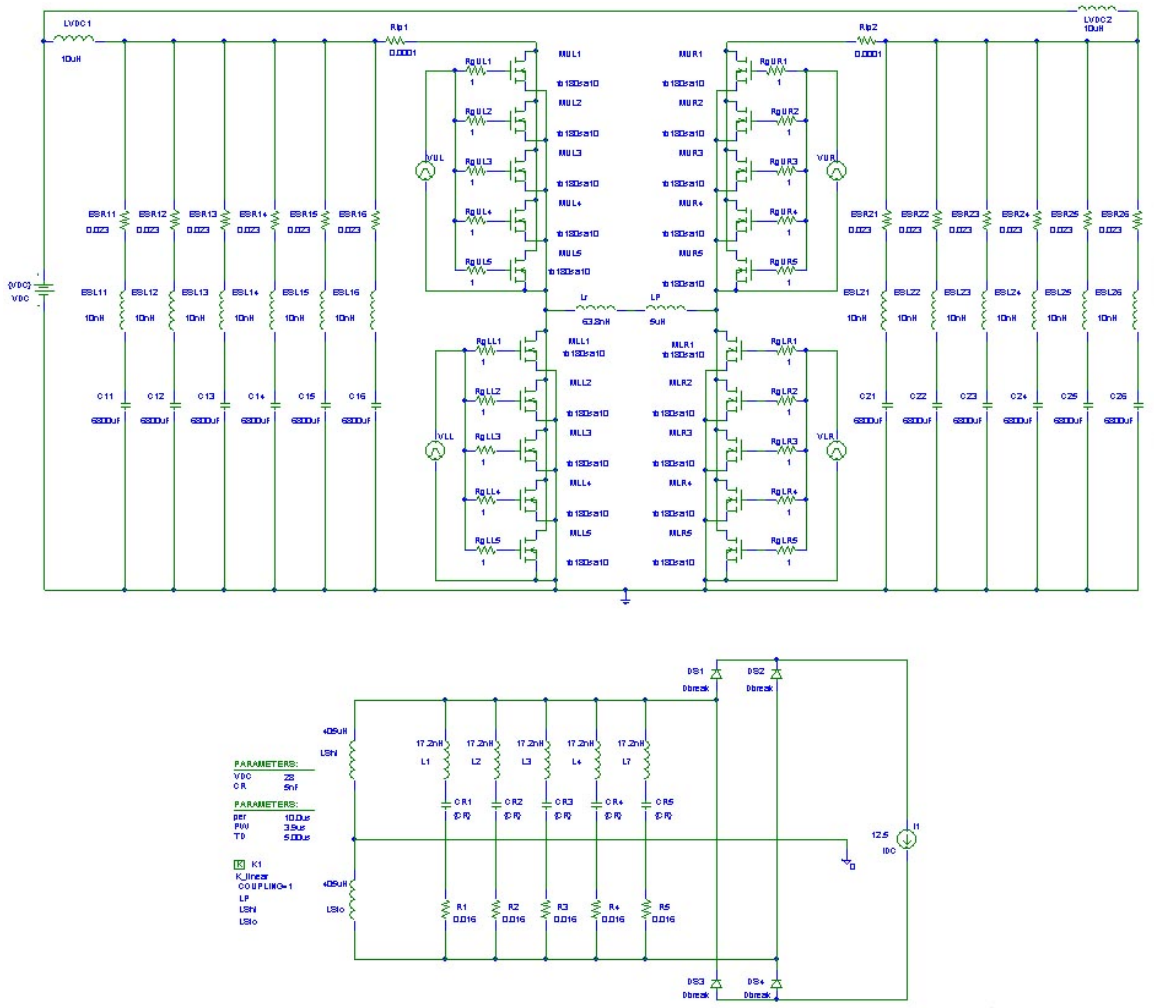


Figure 5.3: Schematic of prototype PLR converter model developed for PSpice.

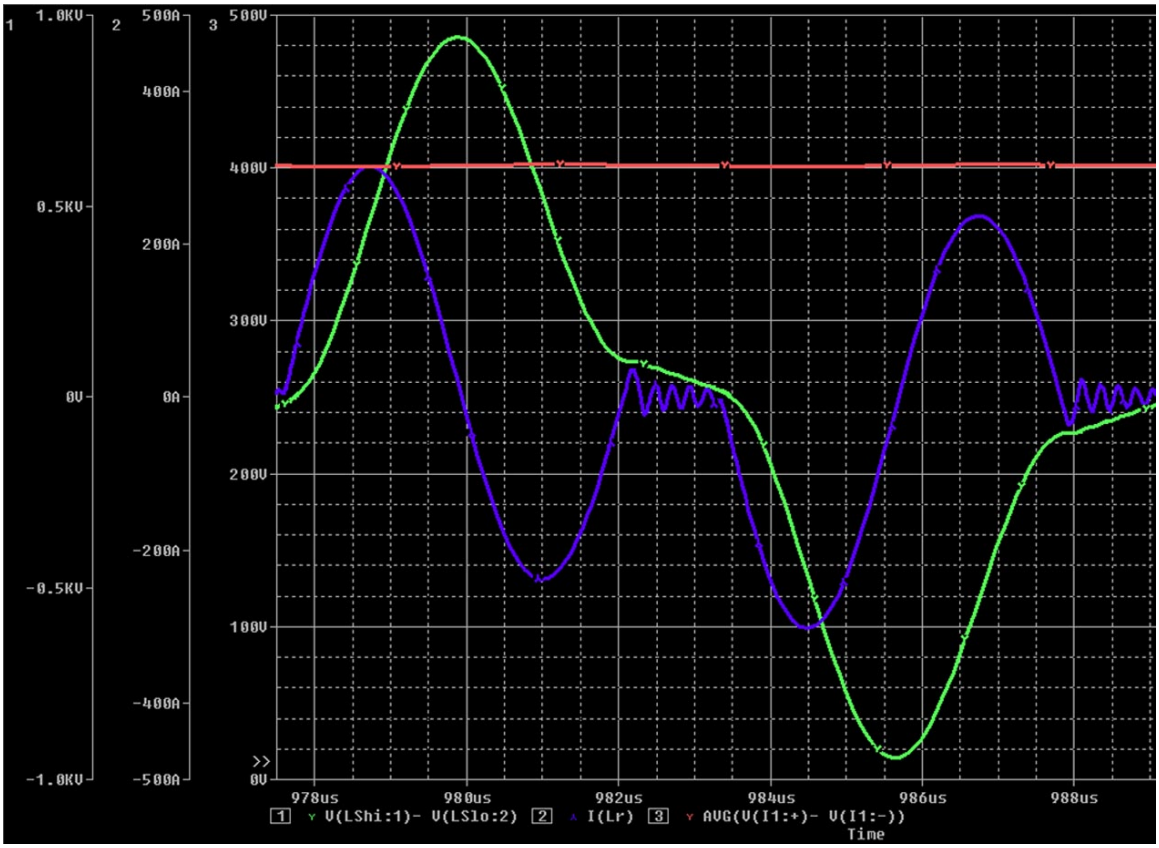


Figure 5.4: Light load simulation results obtained using PSpice.

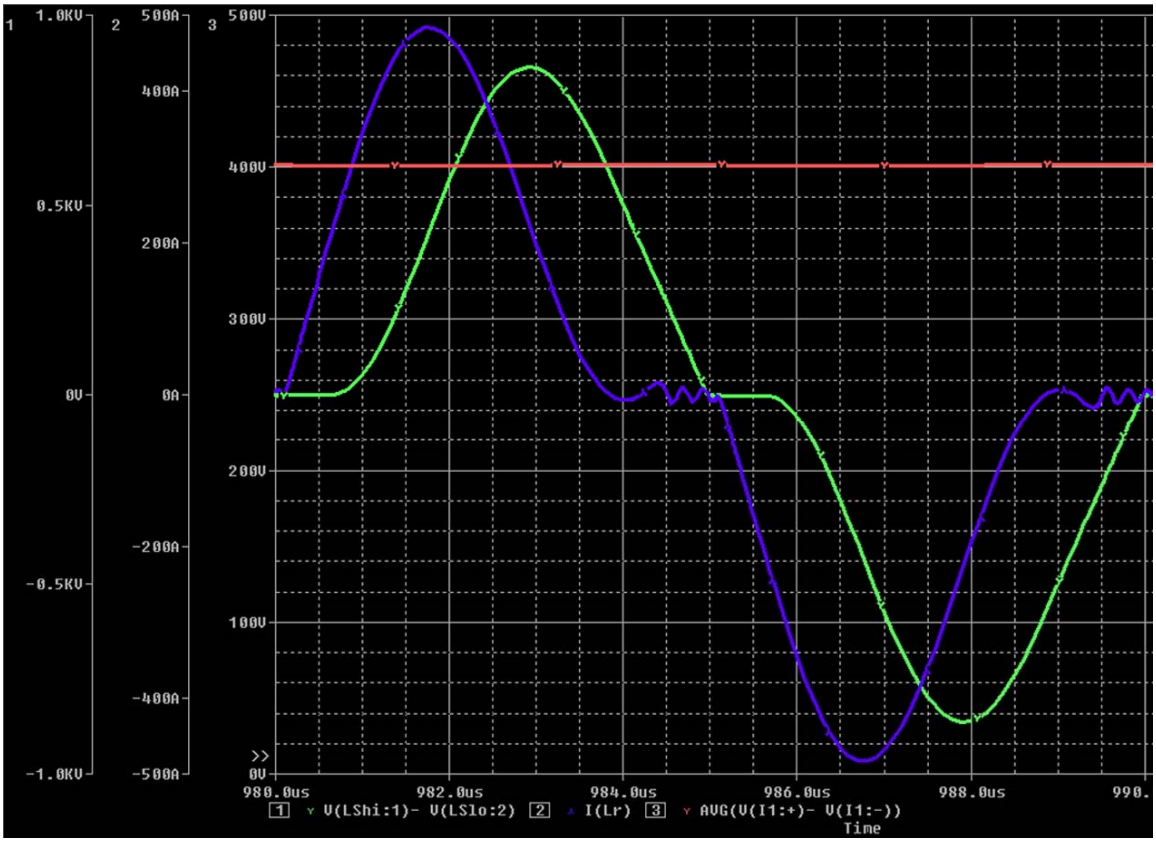


Figure 5.5: Full load simulation results obtained using PSpice.

CHAPTER VI

EXPERIMENTAL RESULTS

A prototype PLR converter was constructed following the design presented in Chapter V. A rigorous power scaling test plan was completed to determine how well the experimental device satisfies the point design specifications and how the model agrees with actual operation. Calculations have been made to determine how effective the design methodology limits the resonant inductance for producing high frequency, high power, and high power density converters.

The completed bus design was machined from 0.062" solid copper sheeting to the design specifications that allowed it to mate to the primary switches, transformer and input connections. The components were arranged in a manner in accordance with the layout discussed in Chapter V. A custom built 1:18 high frequency transformer was professionally wound by a transformer manufacturer. This transformer was wound specifically to achieve the lowest leakage inductance possible while meeting the input terminal requirements and kVA rating. A photo of this transformer can be seen in Fig. 6.1. Testing yielded final specifications for this component, the results of this testing are listed in Table 6.1.

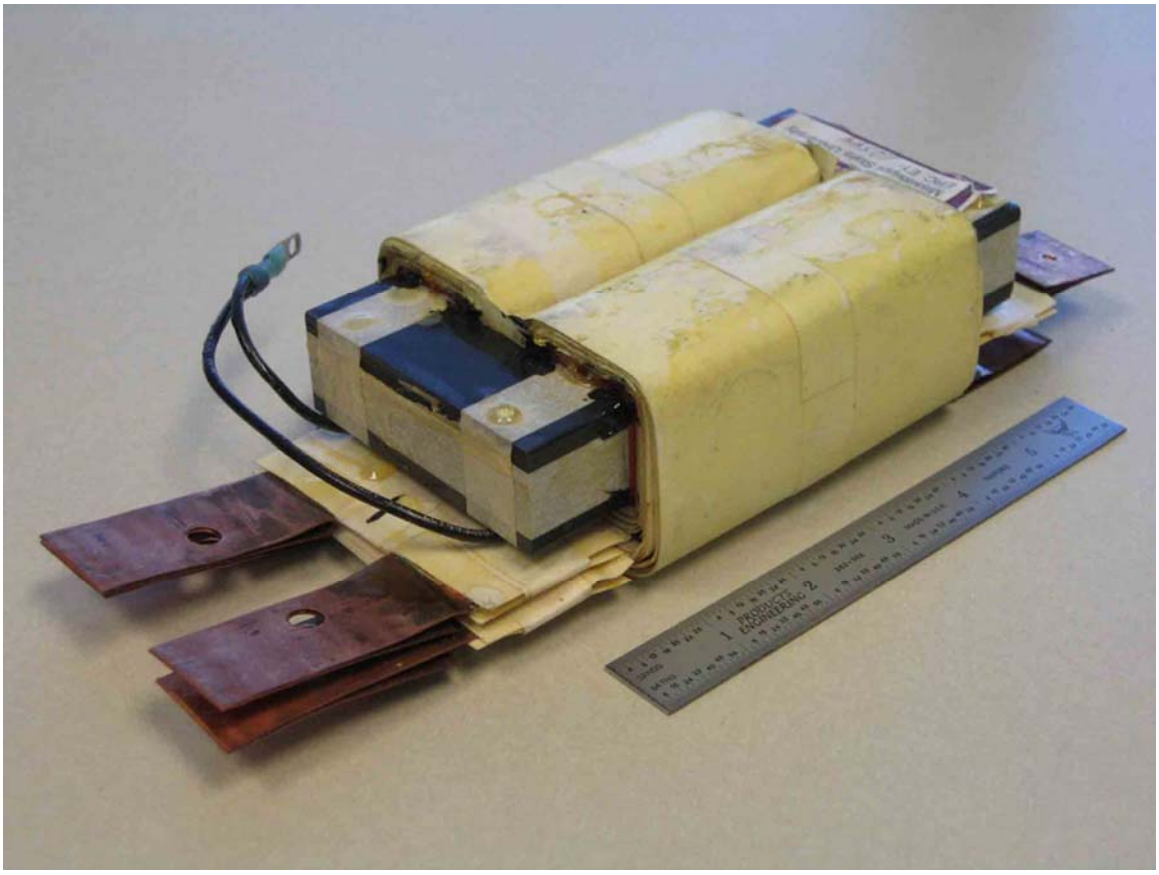


Figure 6.1: High frequency boost transformer using foil windings used in converter prototype.

Table 6.1

High Frequency Boost Transformer Experimentally Verified Specifications

$V_{pri\ max}$	>	64 V
$V_{sec\ max}$	>	1152 V
$I_{pri\ max}$	>	245 A
$I_{sec\ max}$	>	12.5 A
kVA_{max}	=	10 kVA
f_s	=	100 kHz
T_{pri}	=	1 turn
T_{sec}	=	18 turns
N	=	1:18
$L_{mag\ pri}$	=	5 uH
$L_{mag\ sec}$	=	1280 uH
$L_{leak\ pri}$	≈	15 nH
$C_{winding\ sec}$	<	1000 pF
Volume	≈	135 in^3
Mass	≈	2.25 kg

The machined bus work was cut and bent specifically to mate directly to the primary windings of the high frequency transformer with the lowest inductance connections practical. The transformer was secured in a cavity formed by cutting away the interfering fins of the extruded aluminum heatsink per the converter layout. Images of the completed converter prototype are provided in Figs.6.2 and 6.3. These images are labeled in order to clearly define the placement of components obscured due to the overlying bus or extraneous devices.

Initial testing of the completed converter was preformed under light load conditions in order to measure the actual total resonant inductance. This was determined simply by measuring the resonant frequency. Given that a known amount of resonant capacitance has been placed on the secondary estimating the resonant inductance is simply a matter of using Eq. 2.1 to solve for L_r. Eq. 2.1 yields a total resonant inductance of 27.0 nH. Subtracting the measured leakage inductance from Table 6.1 determines the primary loop inductance to be approximately 12 nH. These calculations do not consider the effects due to the transformer secondary interwinding capacitance. However, it is believed that this value is not significantly large enough (i.e. < 1 nF) to greatly affect the resonant frequency.

The experimentally verified total resonant inductance is considerably smaller than the initial estimate for the total inductance utilized in the model from the previous chapter. This will allow for the resonant and switching frequencies to be appreciably greater than the target values of the point design. Increasing the resonant capacitance to produce a resonant frequency consistent with the preliminary specification will yield a

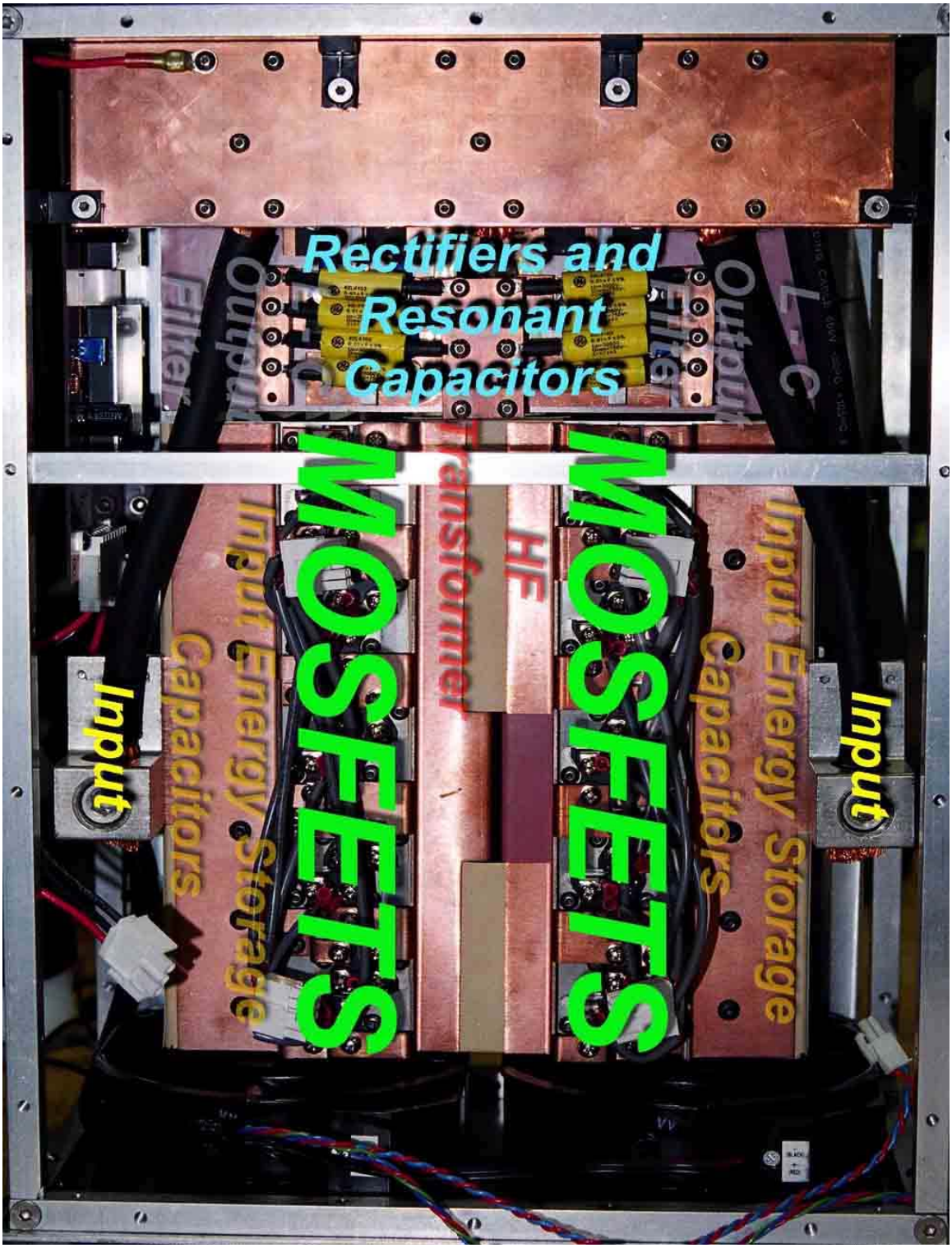


Figure 6.2: Prototype PLR converter image (TOP)

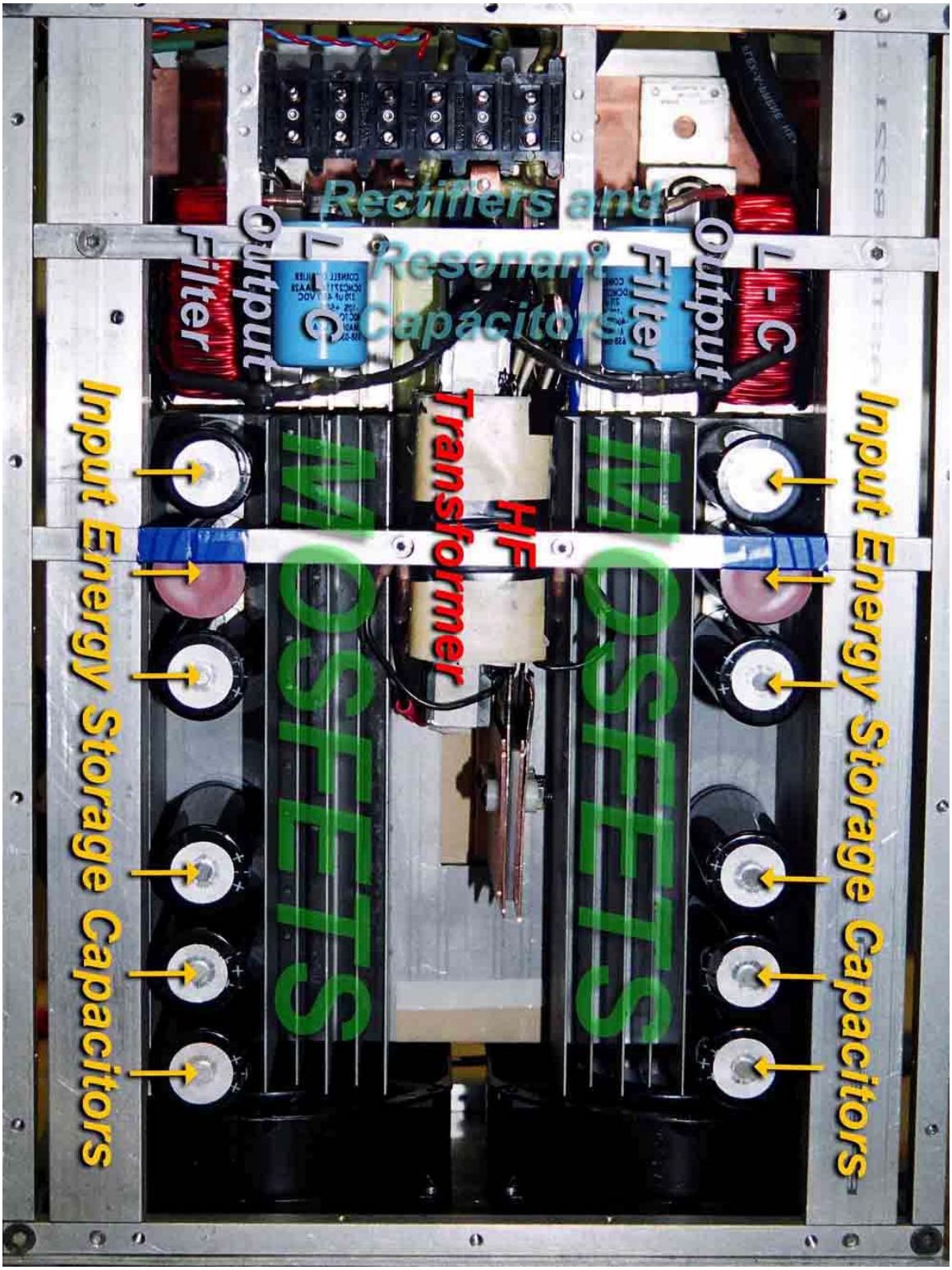


Figure 6.3: Prototype PLR converter image (BOTTOM)

natural impedance considerably lower than the impedance required to drive the desired load. The lower impedance will result in larger peak currents as well as reactive energy to be delivered to the resonant tank at full load producing easily avoidable power loss. Conversely, higher frequency operation could have the added benefit of allowing for reduction in the size of passive components such as the transformer and output filter capacitors in later design iterations. Therefore the new design calculations in Eqs. 6.1 – 6.3 are aimed at achieving the natural impedance necessary for driving the full load specification.

$$C_{r\_\sec} = \frac{L_{r\_pri} \cdot a^2}{Z_{o\_\sec}^{\ 2}} = 17.8nF \cong 20\ nF \tag{6.1}$$

$$\omega_o = \frac{1}{\sqrt{L_{r\_pir} \cdot C_{r\_\sec} \cdot a^2}} = 2.39\,Mrads/s = 380\ kHz \tag{6.2}$$

$$f_{s\_\max} = \frac{V_{out} \cdot f_o}{2 \cdot V_{in\_\min} \cdot a} = 176\ \ kHz \tag{6.3}$$

Adjusting the control circuitry to allow for operation at the maximum switching frequency of 176 kHz will allow for the rated output voltage to be maintained under full load conditions. Feedback circuits were implemented to provide voltage control feedback through simple op-amp error amplifiers to the application specific integrated circuit (ASIC) implemented to produce frequency modulation of the PLR converter. The inherent stability of the resonant tank and the output voltage allow for a reasonably low bandwidth feedback technique such as voltage mode control to be used. The feedback circuit was implemented in such a way as to limit the switching frequency to satisfy that

DCM conditions are maintained. The complete design of the control circuitry is outside the scope of this thesis. Schematics of the control circuits and gate drivers are provided in appendices B and C.

A complete test plan was implemented to explore the capabilities of the finalized design. The results of two the test performed under this plan are presented in Table 6.2. These tables are indicative of results obtained throughout the entire envelope of operation. These two particular test results are presented to show operation under nominal input voltage conditions at light and full load respectively. Waveforms captured during these tests show the proper operation of the resonant tank and ensure that ZVZCS is achieved. These waveforms can be found in Figs. 6.4 and 6.5 for light and full load respectively.

Plotting the data taken during one of the load profile tests reveals relevant information regarding the operation of the converter. Figures 6.6, 6.7, and 6.8 were each derived from a single test with an increasing load profile performed with the complete system integration including the vehicle battery/alternator source. This accounts for the minor instabilities in the source voltage throughout the test envelope. Figure 6.6 depicts the efficiency curve for the prototype. This curve shows a direct relationship between increased load and efficiency as expected with a maximum efficiency of slightly greater than 80%. Figures 6.7 and 6.8 show the percent output voltage regulation versus output power and input voltage respectively for the entire operational envelope. A target regulation of ± 1% as stated in the initial design specifications is well within the

Table 6.2

Selected Test Results

	Light Load	**Full Load**
V_{in}	28.30 V	27.16 V
I_{in}	44.00 A	220.3 A
V_{out}	402.2 V	400.5 V
I_{out}	2.130 A	12.07 A
f_o	392 kHz	392 kHz
f_s	132 kHz	161 kHz
P_{in}	1.245 kW	5.983 kW
P_{out}	0.856 kW	4.834 kW
η	68.75%	80.78%
Mass	22.7 kg	
Volume	35961 cm^3	
$\rho_{(mass)}$	212.9 W/kg	
$\rho_{(vol)}$	0.146 W/cm^3	

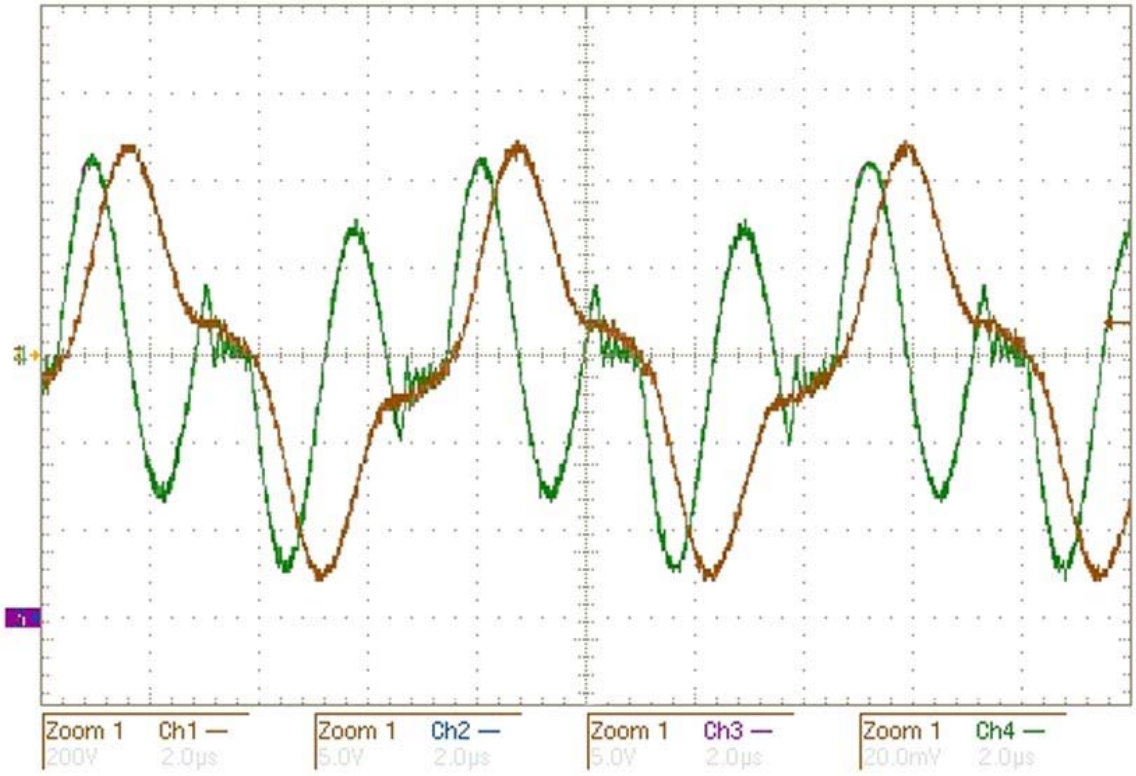


Figure 6.4: Resonant capacitor voltage and resonant inductor current waveforms captured during light load operation.

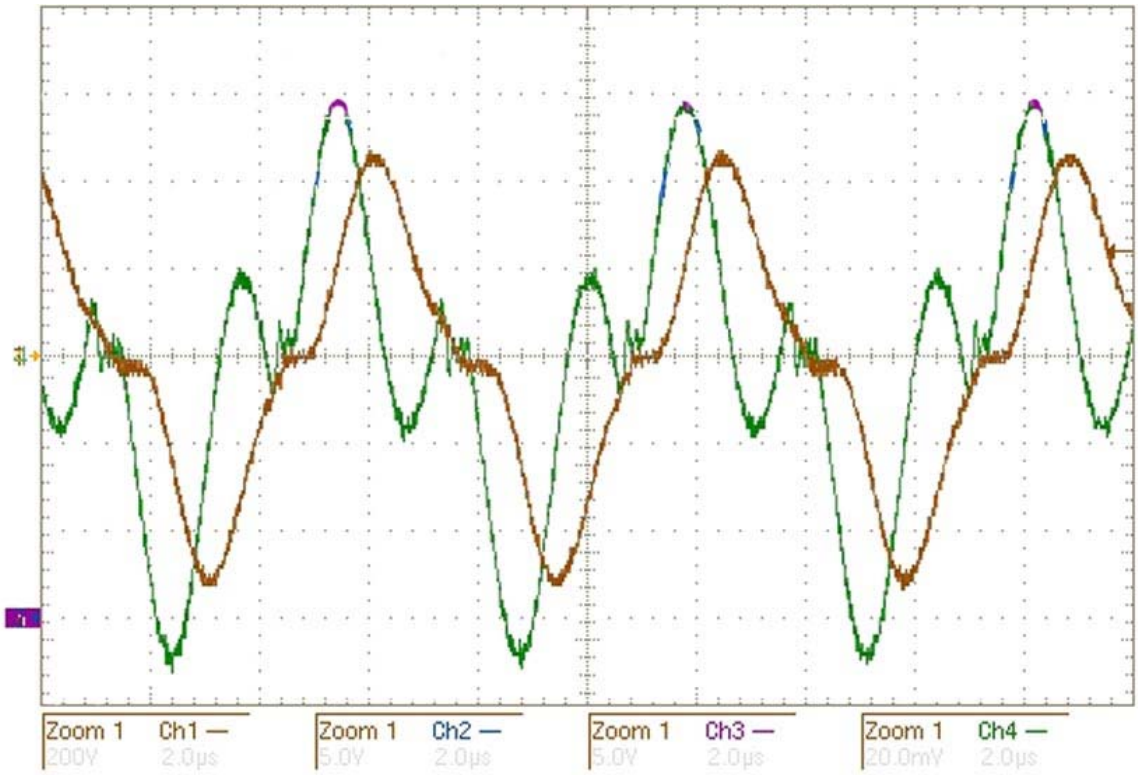


Figure 6.5: Resonant capacitor voltage and resonant inductor current waveforms captured during full load operation.

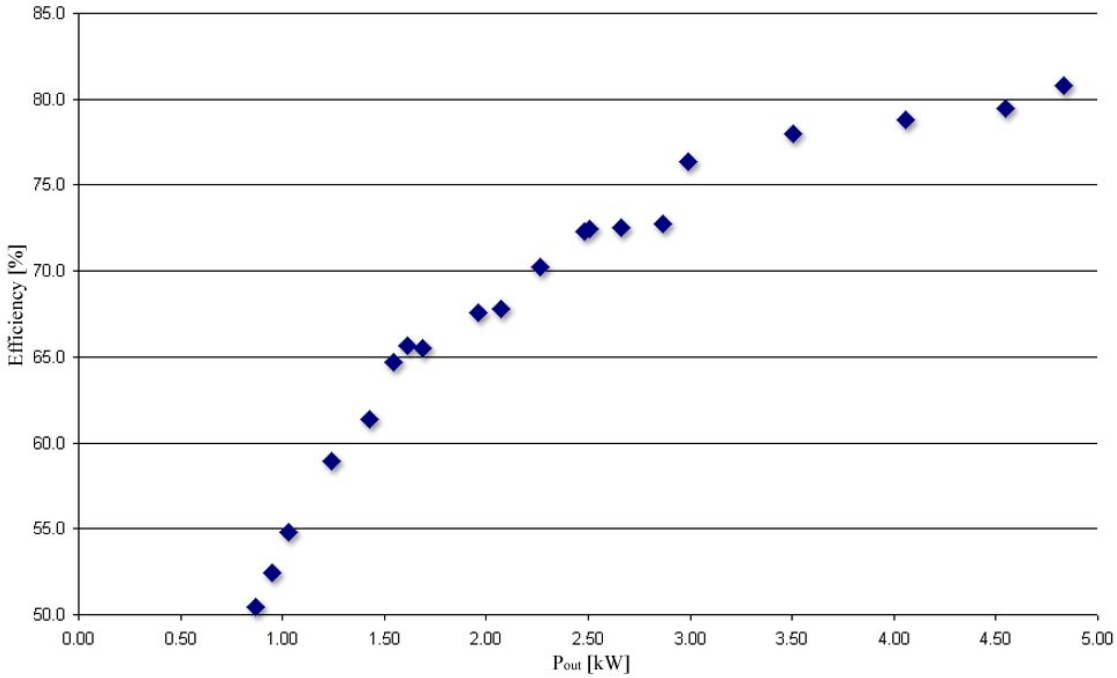


Figure 6.6: Efficiency vs. output power for a single load profile test

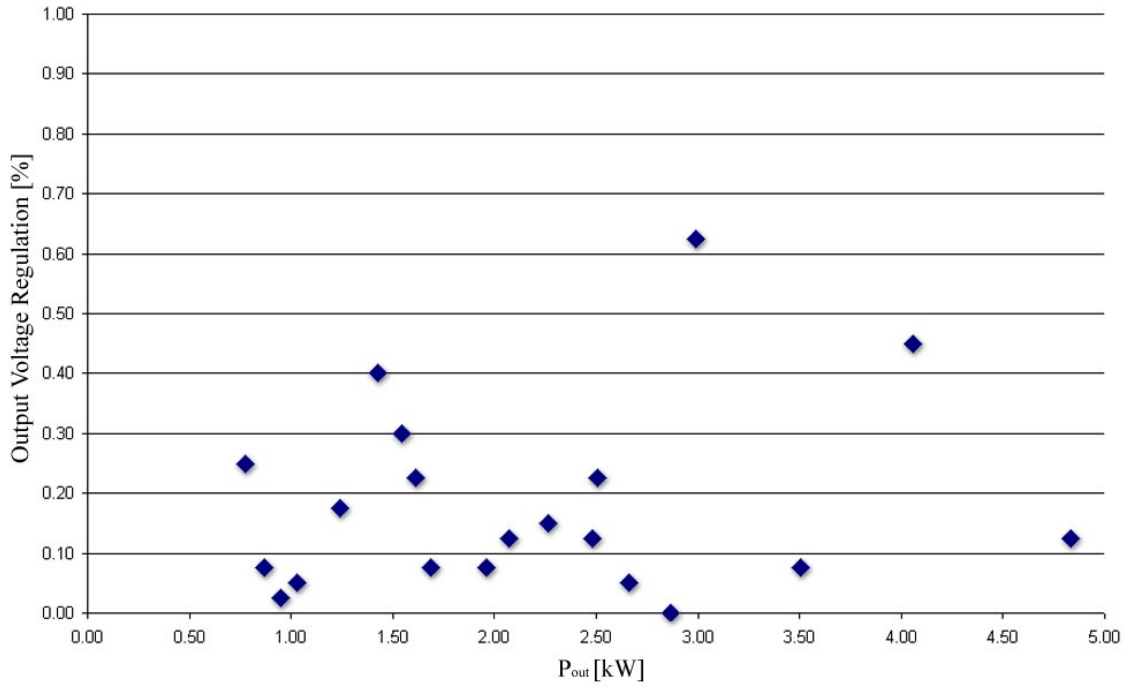


Figure 6.7: Output voltage regulation vs. output power for a single load profile test

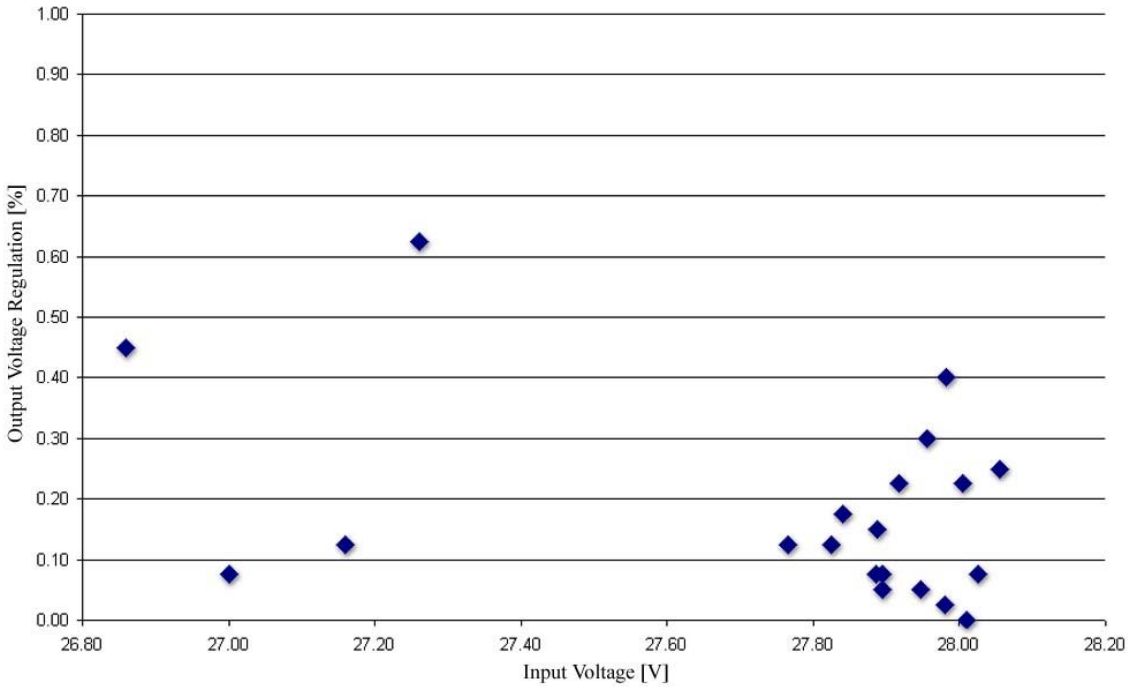


Figure 6.8: Output voltage regulation vs. input voltage for a single load profile test

capabilities of this device, as shown in these two figures. With the exception of efficiency each of the specifications stated in the point design were met or exceeded.

Output voltage regulation was maintained using voltage feedback to an application specific integrated circuit (ASIC). The Motorolla MC34066 resonant controller was used to provide frequency modulation control necessary to achieve the output voltage regulation shown in Figs. 6.7 and 6.8. The control signal was delivered to the gate driver circuit specifically designed to provide the proper gate-source voltage necessary to switch the MOSFETs in the primary full-bridge circuit. The complete design of the frequency modulation control circuitry and the gate driver circuitry are outside the scope of this thesis. A Schematic of the control circuitry designed specifically for the converter prototype is included in appendix B. A schematic for a single gate driver designed specifically for the converter prototype is included in appendix C.

CHAPTER VII

CONCLUSIONS

The design methodology presented in this thesis has been applied to the design of an experimental kilowatt class full-bridge parallel loaded resonant voltage boost converter. The prototype device has been thoroughly studied and performance specifications for the device have been extracted using the data collected. A boost converter capable of delivering a highly regulated output voltage to a specified load has been achieved.

The prototype developed is capable of sustaining five kilowatts of power to a load at a stable output voltage of 400 VDC. Output voltage regulation can be maintained with less than one percent voltage ripple over the entire load envelope powered by a 28-V source with greater than fourteen percent input voltage swings. A voltage boost of approximately 1:14 has been achieved using this method while achieving greater than 80 percent efficiency and power density of 212 W/kg.

The theory of operation and reasoning for selecting the parallel loaded resonant full-bridge topology operated in discontinuous conductions mode has been shown to be a practical design solution for DC to DC power conversion in this application. The experimental results prove the technique developed in Chapters III and IV can

produce predictable and efficient results. These results demonstrate the prototype to be stable load independent voltage source as expected. Thus experimentation confirms the argument presented in Chapter II for use of this topology and operating mode for high power voltage boost converters.

The initial design specifications of Chapter V have been met with the sole exception of the full load efficiency. Failure to meet this specification however, does not nullify the claims of this thesis. On the contrary, evaluation of the design performance provides validation for the methodology developed in Chapter IV, the converter model based on this design methodology in chapter V, and the key assertion in chapter I, that the parallel loaded resonant converters operating in discontinuous conduction mode are viable for use in high power density voltage boost applications.

Using data collected during testing of the converter the model created in Chapter V has been altered to more accurately represent actual converter operation. The model has been enhanced and now agrees well with the experimentation results. This enhanced model is included appendix A along with simulation results relevant for evaluation. The model can be used to provide validation for the claim that PLR boost converters with secondary side resonance are scalable for both voltage and power. Furthermore the methodology and construction techniques of Chapters III and IV can be used to produce easily scaled designs for low input voltage (i.e. V_{in} <100V) similar to the prototype presented in this thesis. Due to characteristics inherent to PLR converters with secondary side resonance, use of this design methodology is particularly suited for large voltage boost (i.e. V_{out}/V_{in}>10) kilowatt class applications.

The key to achieving the goals set in this thesis was recognition of the role parasitic elements pose in altering the ideal operation of the circuit. The methodology developed is focused on minimizing and utilizing these elements to the fullest extent possible. Application of basic inductor physics and electromagnetic theory to the component arrangement process produced practical means for minimizing parasitics. Using known properties of secondary side resonance and recognition of the applicability of this arrangement to voltage boost conversion allowed for the utilization of the non-idealities to a great extent.

Further study of the prototype should yield explanations for greater than expected power dissipation at full load operation. Future design iterations focused on reducing resistive losses could produce dramatic improvements in efficiency. This in turn would generate less component stress, high power handling ability, and higher power density converters.

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APPENDIX A

VALIDATED PSPICE SIMULATIONS

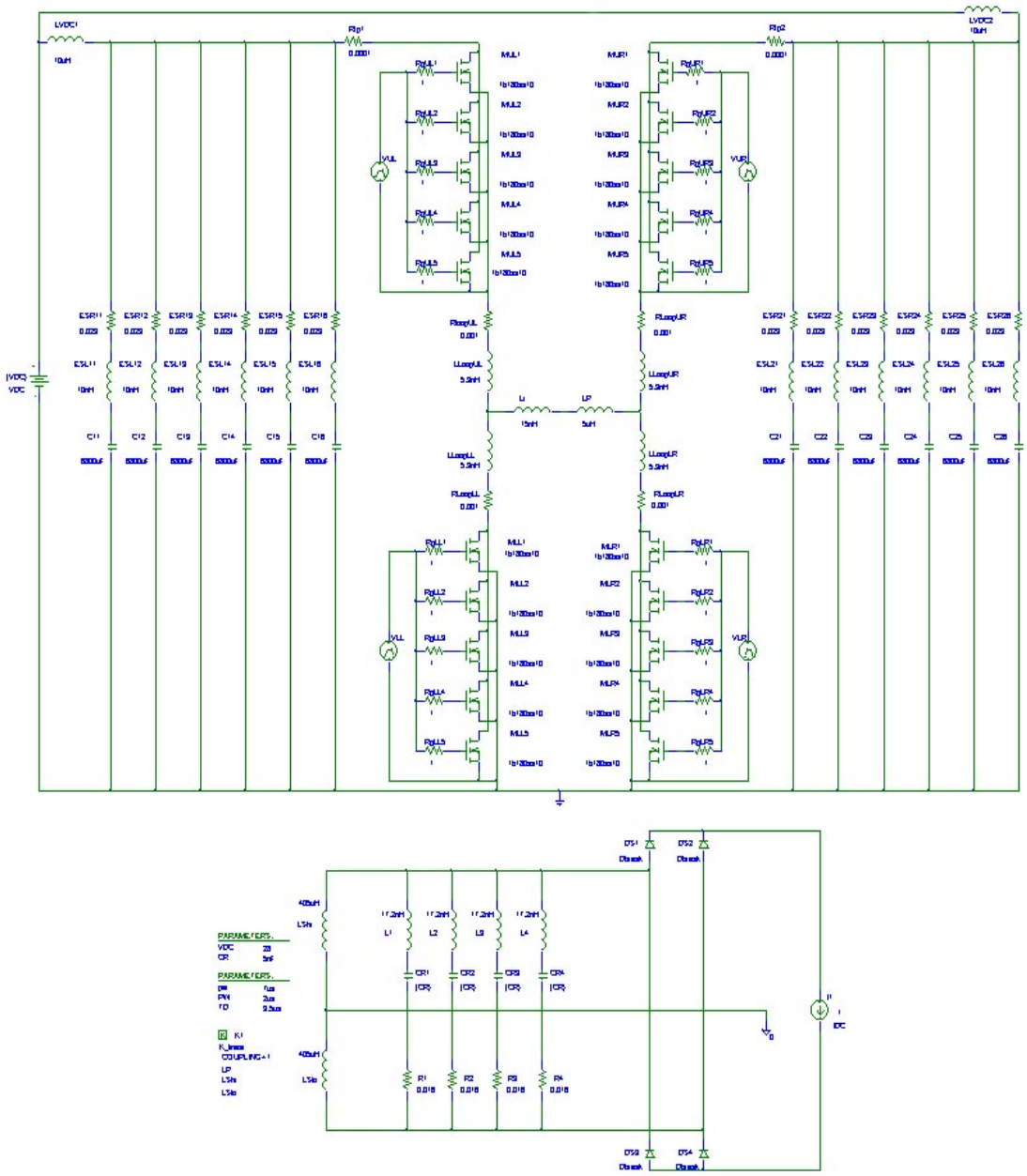

Figure A.1: Schematic of the prototype PLR converter utilizing experimental results.

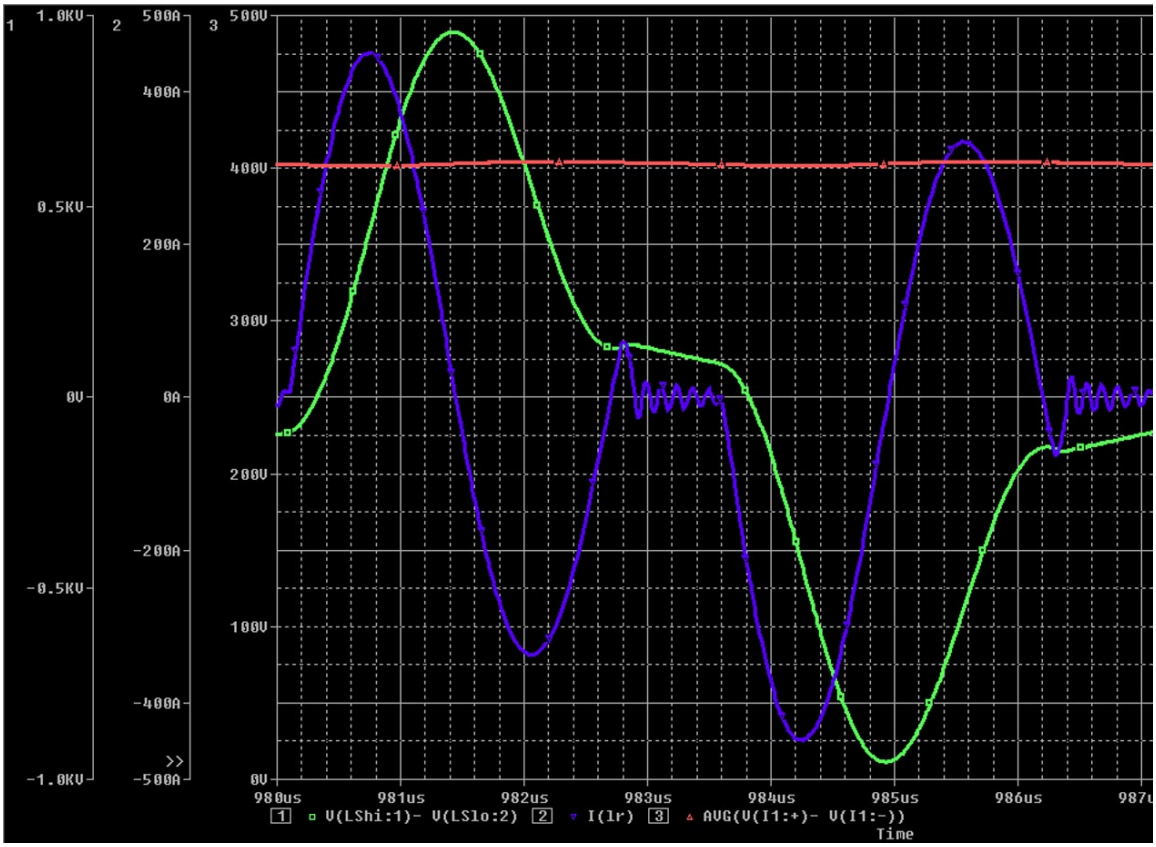

Figure A.2: Revised light load simulation results obtained using PSpice.

$V_{in} = 28V$

$I_{in} = 35A$

$V_{out} = 400V$

$I_{out} = 1A$

$f_o = 380kHz$

$f_s = 142kHz$

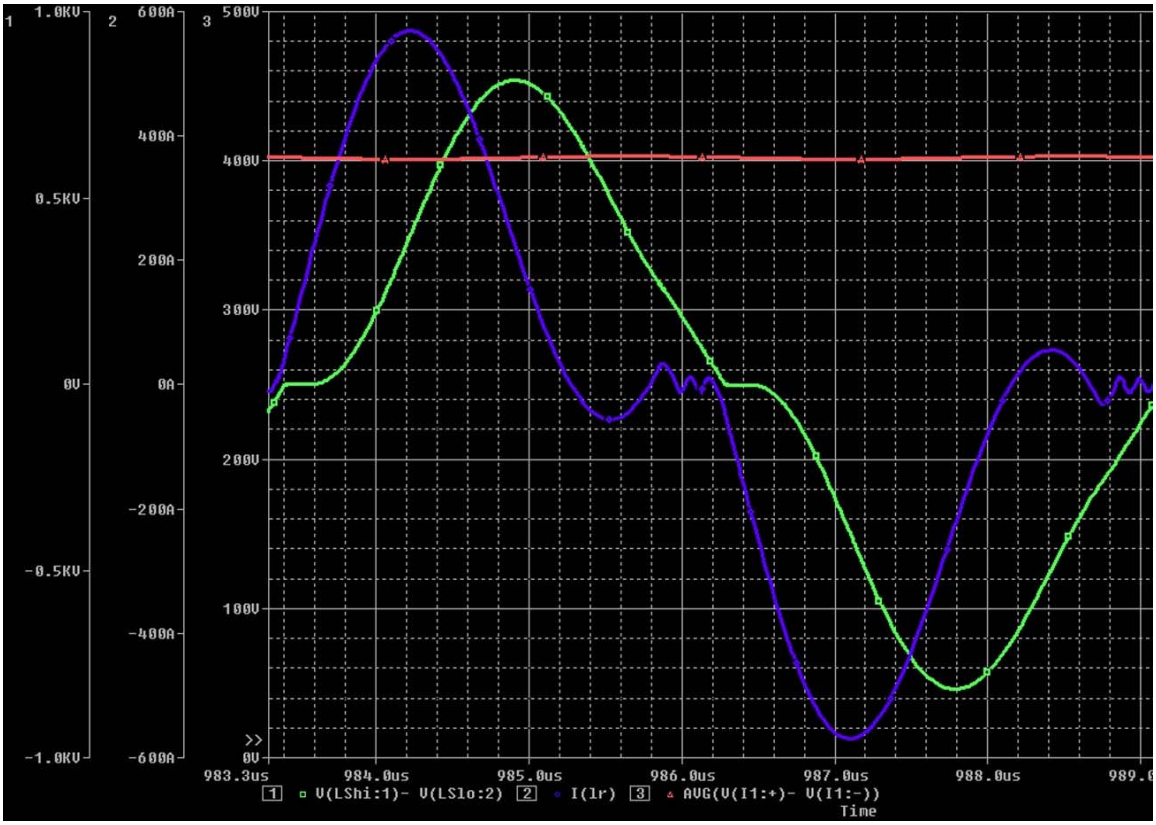

Figure A.3: Revised full load simulation results obtained using PSpice

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$V_{in} = 28V$

$I_{in} = 220A$

$V_{out} = 400V$

$I_{out} = 1A$

$f_o = 380kHz$

$f_s = 174kHz$

APPENDIX B

FREQUENCY MODULATION CONTROL CIRCUIT

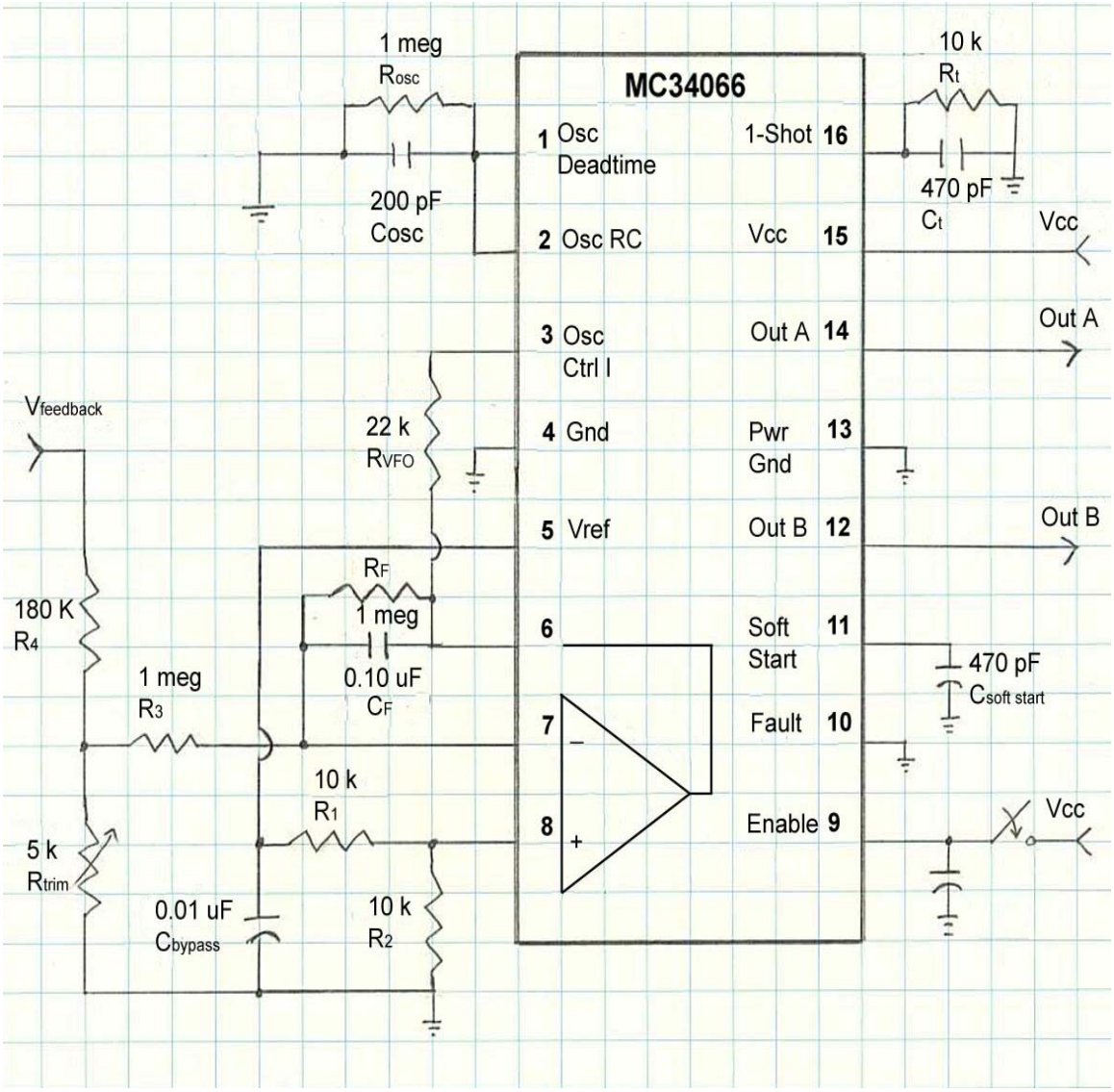

Figure B.1: Schematic of the prototype PLR converter control circuit

The motorolla MC34066 is a frequency modulation control ASIC designed for use in resonant converters or other application where voltage feedback frequency modulation control can be used. The prototype output voltage was scaled using a simple voltage divider (R_4 and R_{trim}) and feed into an error amplifier in the controller. The pulse widths of the control pulses delivered to the gate drivers is determined via an RC network

connected to a 1-shot timer circuit in the controller. Outputs A and B provide control pulses for the gate drivers connected to their respective legs of the primary full bridge circuit.

APPENDIX C

GATE DRIVER CIRCUIT

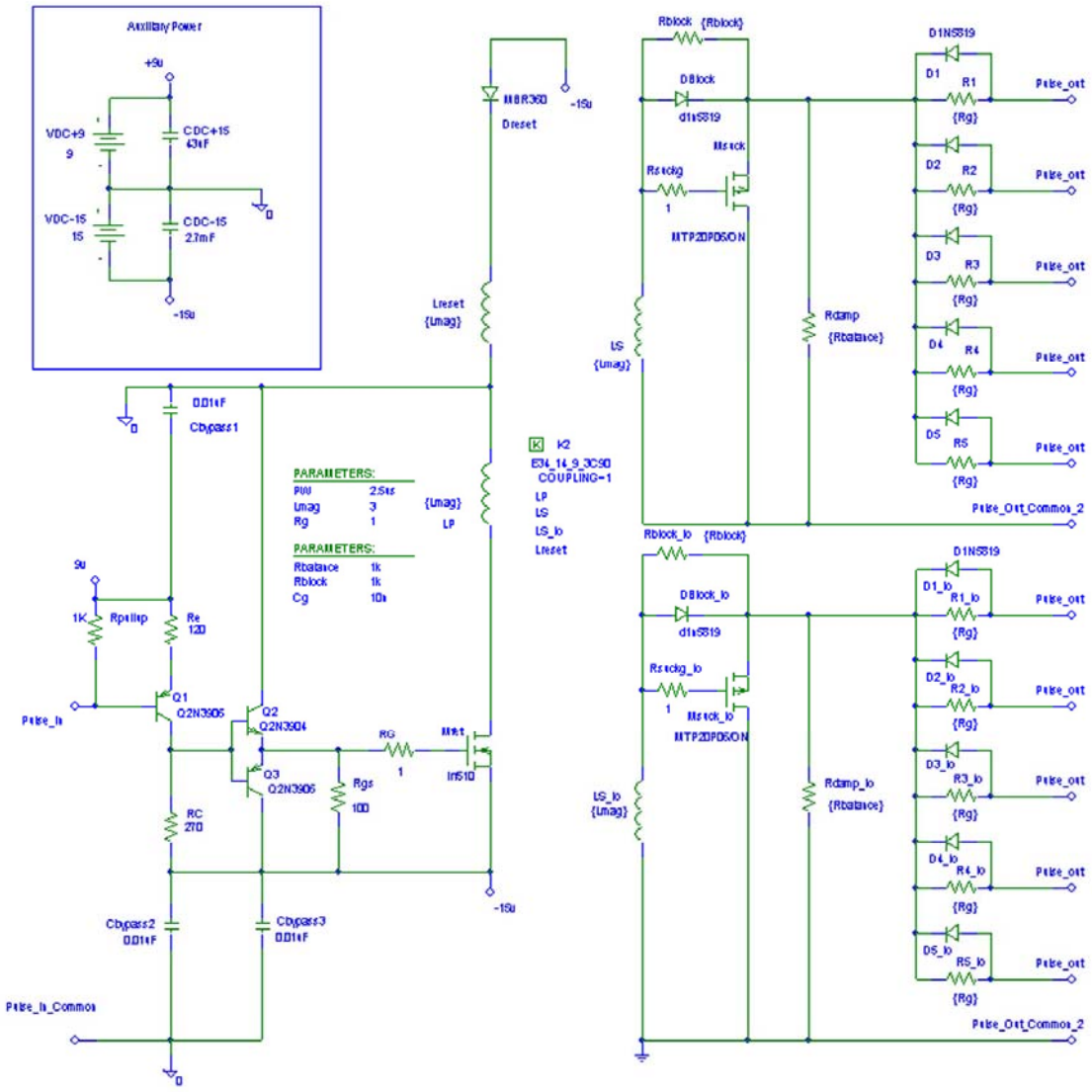

Figure C.1: Schematic of prototype PLR converter gate driver

This gate driver is designed to simultaneously switch both the upper and lower half of a single leg of the full-bridge circuit. Two gate drivers are required for proper operation. One gate driver is required to switch each leg.