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Edge Termination and RESURF Technology in Power Silicon Carbide Devices

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EDGE TERMINATION AND RESURF TECHNOLOGY IN POWER SILICON CARBIDE DEVICES

By

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EDGE TERMINATION AND RESURF TECHNOLOGY IN POWER

SILICON CARBIDE DEVICES

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The effect of the electrical field enhancement at the junction discontinuities and its impact on the on-state resistance of power semiconductor devices was investigated. A systematic analysis of the mechanisms behind the techniques that can be used for the edge termination in power semiconductor devices was performed. The influence of the passivation layer properties, such as effective interface charge and dielectric permittivity, on the devices with different edge terminations was analyzed using numerical simulation.

A compact analytical expression for the optimal JTE dose was proposed for the first time. This expression has been numerically evaluated for different targeted values of the blocking voltage and the maximum electric field, always resulting in the optimal field distribution that does not require further optimization with 2-D device simulator. A compact set of rules for the optimal design of super-junction power devices was developed. Compact analytical expressions for the optimal dopings and dimensions of the

devices employed the field compensation technique are derived and validated with the results of numerical simulations on practical device structures.

A comparative experimental study of several approaches used for the edge termination in SiC power diodes and transistors was performed. The investigated techniques included the mesa termination, high-k termination, JTE, and the combination of JTE and field plate edge termination. The mesa edge termination was found to be the most promising among the techniques investigated in this work. This stand-along technique satisfied all the imposed requirements for the "ideal" edge termination: performance, reproducibility (scalability), and cost-efficiency. First of all, it resulted in the maximum one-dimensional electric field (E_{1DMAX}) at the main device junction equal to 2.4 MV/cm or 93% of the theoretical value of critical electric field in 4H-SiC. Secondly, the measured E_{1DMAX} was found to be independent of the voltage blocking layer parameters that demonstrate the scalability of this technique. Lastly, the implementation of this technique does not require expensive fabrication steps, and along with an efficient use of the die area results in the low cost and high yield.

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CHAPTER I

INTRODUCTION

Today, in the era of growing energy crisis, the role of power electronics in the reduction of energy consumption becomes more and more vital. Struggling to minimize the size and weight of systems, and reduce both static and dynamic losses, power electronics remains in continuous search for new technological solutions. The SiC power device technology is on the frontline of this quest. SiC provides a unique opportunity to avoid many fundamental limitations caused by the properties of the traditional semiconductors by offering numerous material advantages such as a wide bandgap, high thermal conductivity and high saturation drift velocity. The constantly maturing SiC power electronics is experiencing an exciting time, when the fundamental material studies give place to the applied design and process development, bringing this technology close to the commercial market.

This chapter provides a systematic analytical review of the state-of-the-art SiC power device technology. Although all the major directions in SiC power device technology are covered, some areas where the author made an original contribution are discussed in more details. In particular, these areas include vertical power JFET switches; power rectifiers; RF bipolar transistors; self-aligned MESFET and SIT power L-band amplifiers; and lateral trench JFET smart power technology

1.1 SiC Power Switches

The historical review of the power switch development in silicon reveals an evolution from JFETs and BJTs to ultra-high power GTOs, IGBTs and IGCTs. Unfortunately, the state-of-the-art design solutions from the silicon industry can not, in most cases, be easily applied to the SiC industry because of the fundamental differences in the material properties and processing technologies. In spite of the fact that advanced SiC devices, such as IGBTs and GTOs have been reported [1, 2], the commercial SiC power switch development is still confined to the basic VJFET, MOSFET, and BJT devices. This section discusses the performance of the recently published power SiC VJFETs, BJTs, and MOSFETs and identifies the key issues related to the device design and processing.

1.1.1 Vertical JFETs

SiC Vertical Junction Field Effect Transistor (VJFET) is a voltage-controlled device that utilizes all the superior properties of SiC, resulting in low-on-resistance, ultra-fast switching, and excellent high-temperature and high-radiation stability [3-6]. There are two general approaches in the 4H-SiC VJFET design. The schematic cross-sections of typical devices that implement these designs are shown in Fig. 1.1 [4, 7]. Both the approaches have their strong and weak sides. For low-to-medium voltage applications (ranging from 600 V to 1800 V), where the channel component of the total on-state resistance is dominant, the first design (shown in Fig. 1.1 a) provides obvious advantages over the second one (shown in Fig. 1.1 b). First of all, a single vertical channel configuration allows for an inexpensive self-aligned process, which means that a high channel packing density is achievable without imposing aggressive

photolithography requirements. Such high channel packing density (*e.g.*, $5x10^3$ cm/cm^2) offered by the first design virtually eliminates the channel component of the total device resistance, and optimizes the usage of the drift layer. Secondly, this device offers extremely low switching losses, since it has negligible source-to-drain capacitance as compared to the second approach. The last (but not least) advantage of the first design is the simple reproducible fabrication process that along with the efficient use of material reduces the cost of the final product.

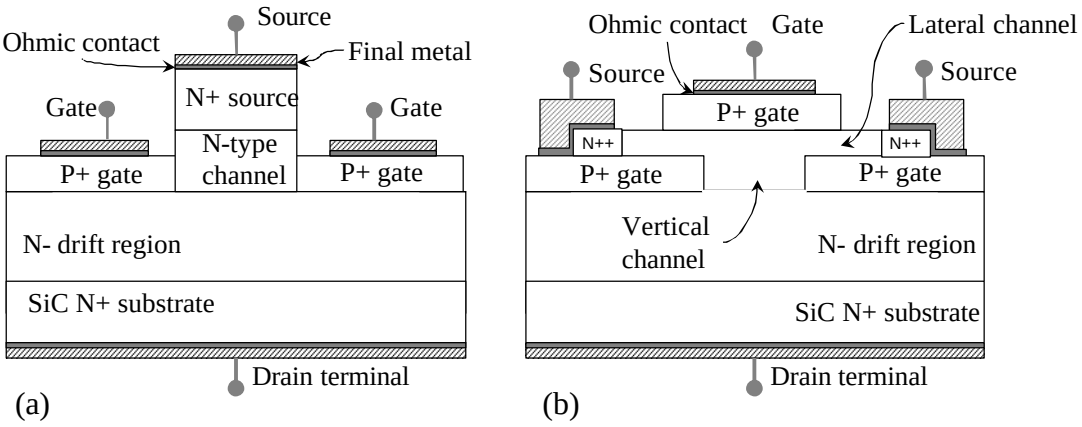


Figure 1.1: Schematic cross-sections of (a) a single vertical channel SiC VJFET [4], and (b) dual-channel SiC VJFET [7].

For the higher voltage applications (above 1800 V), the second design solution offers certain advantages over the first approach. It can be noticed, that the second device structure comprises two JFETs connected in cascode. This suggests an elegant way to make this device normally-off because the voltage required to punch through the lateral channel is at he same time applied to the bottom gate structure that pinches-off the vertical channel. In today's power electronics dominated by Si MOSFETs and IGBTs, the systems are designed for normally off power switches. In

this situation, offering a plug-and-play SiC part would grant an easy pass to the market. Naturally, the cumulative resistance of the lateral and vertical channels designed for normally-off operation would be quite high. However, since in the high voltage devices the resistance of the voltage blocking layer becomes a significant part of the total resistance, the increase in the channel resistance might be a reasonable pay-off for the opportunity of having a normally-off device. Another advantage of this design solution is that at the breakdown conditions, the avalanche current does not flows through the control circuit (as in the first device), but rather through the source-drain network. Several attempts to design a dual-channel JFET for the bipolar mode operation where the gate bias in the on-state exceeds the built-in potential of the gate-drain p-n junction were also published [8].

1.1.2 Power BJTs

Reported for the first time in 1978 by Münch and Hoeck [9], the SiC bipolar junction transistor (BJT) technology has experienced dramatic progress over the recent years. 4H-SiC BJTs have demonstrated excellent current carrying and blocking capabilities, and offer a good high-temperature performance. Figure 1.2 (a) shows a schematic cross-section and (b) I-V characteristics of a 17 A, 1.3 kV 4H-SiC BJT reported by A. Agarwal *et al* in 2003 [10]. Due to the negative temperature coefficient of the current gain, 4H-SiC BJTs are easier to parallel than their Si counterparts. In contrast to the vertical MOSFETs and JFETs, these devices do not have junction discontinuities in the active region. With an appropriate edge termination, they could be easily scalable to high blocking voltages.

Despite the above advantages, the SiC power BJT has certain application limitations as it is a current-driven device. In order to reduce the required control power, an integrated Darlington structure can be used [11], at the expense of the switching speed. Promising efforts toward the integration of SiC MOSFETs and BJTs in a power monolithic voltage controlled switching module have been made recently [12]. There are also certain processing issues that cause high surface recombination velocity at the edge of the emitter finger and poor emitter injection efficiency. The most recent study revealed a significant reliability problem of power SiC BJT. Dramatic reduction of current gain was observed in power 4H- SiC BJTs just after a few hours of operation due to the recombination-induced nucleation of stacking faults from the basal plane dislocations [13].

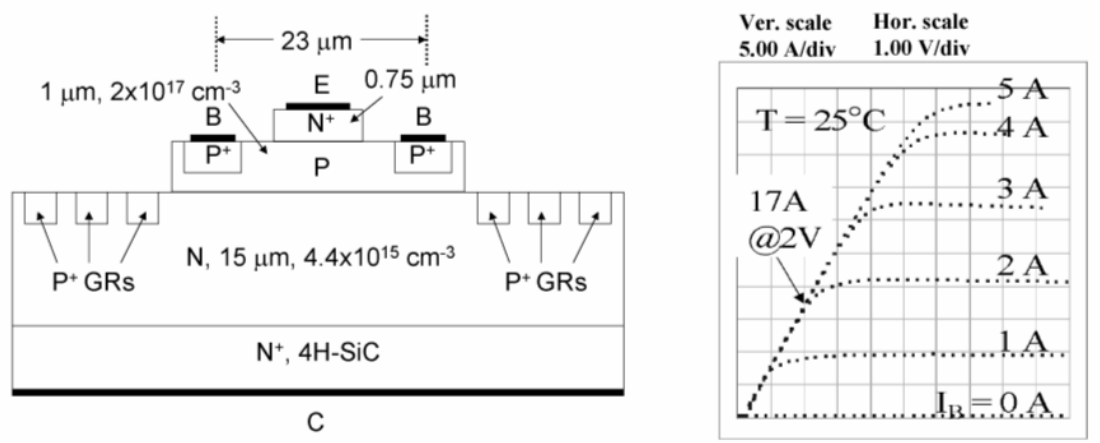


Figure 1.2: (a) The schematic cross-section, and (b) the drain characteristics of a 17 A 1.3 kV 4H-SiC BJT (after A. Agarwal *et al* [10]).

1.1.3 *Vertical Power MOSFETs*

Recent publications demonstrated significant progress in the development of high-power vertical SiC MOSFETs. Two basic designs compete in this area: UMOSFET (a vertical U-grooved MOS-channel structure [14]) and DMOSFET (a structure that combines the lateral MOS-channel with the vertical JFET region [15, 16]). The simplified cross-sections of an n-channel UMOSFET and an n-channel DMOSFET are shown in Fig. 1.3. Despite their advantages as normally-off, voltage driven switches ideal for many applications, both types of MOSFETs suffer from low inversion layer mobility and poor high-temperature, high-field reliability.

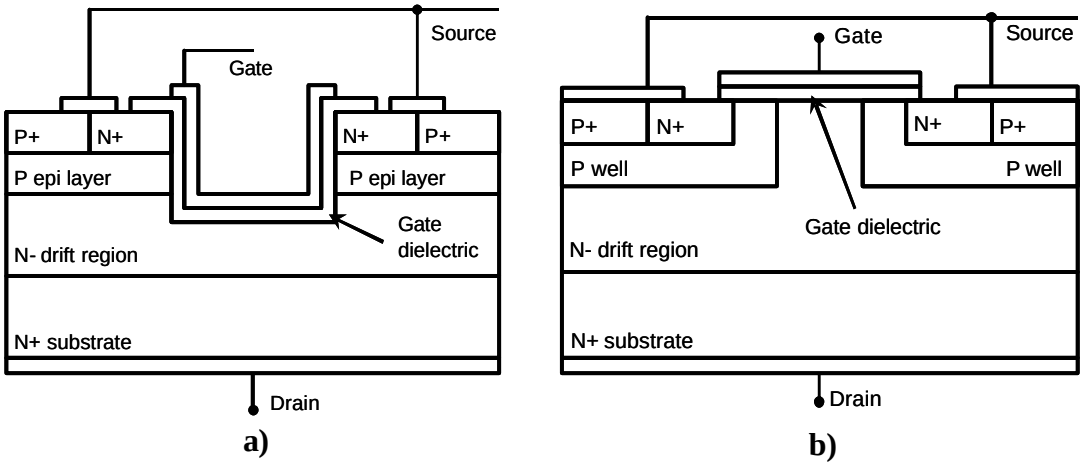


Figure 1.3: Schematic cross-sections of (a) a conventional UMOSFET, and (b) a DMOSFET device structures.

As shown in Fig. 1.3 (a), the classical UMOSFET in SiC is a vertical device, which comprises an epitaxially grown thick n- drift region and p-type base region. The n+ source and p+ body contact regions can be either epitaxially grown or implanted. Dry plasma etch is used to form a trench, and a thin dielectric layer is then

thermally grown or deposited followed by metal or polysilicon gate deposition to define the vertical MOS channel.

Potentially, the 4H-SiC UMOS transistor structure can offer the following advantages over the other design solutions (in particular, over various DMOS structures):

- Vertical configuration, where the absence of the JFET region allows for taking maximum advantage of the excellent blocking/conductive properties of SiC drift layer;
- Relatively simple structure that can be made using a self-aligned fabrication process resulting in significant increase in the channel packing density;
- The doping profiles in the entire device structure can be realized by epitaxial growth.

However, the years of development revealed the following issues limiting the performance of the 4H-SiC UMOSFET:

- On-state insulator reliability due to the much smaller conduction band offset of SiC to SiO_2 compared to that of silicon, resulting in electron injection into the gate dielectric;
- High electric field in the gate insulator under off-condition due to the electric field enhancement at the sharp corner of the U-trenches;
- Low inversion channel mobility on a vertical sidewall due to the high interface state density at the p-SiC/SiO_2 interface and high fixed charge density in the insulator.

Furthermore, since the operating electric field in thermally grown SiO_2 is limited to 2 MV/cm [17], and in order to satisfy the Gauss' law ($e_{oxide}E_{op,oxide} \geq e_{SiC}E_{op,SiC}$), the maximum operating electric field in the underlying SiC layer must be held less than 0.8 MV/cm which is less than 30% of its critical value. This limitation results in the

resistance of the drift region 64 times higher than its theoretical minimum. In Ref. [18], we show that this issue dramatically suppresses the inherent advantages of SiC UMOS transistors over their silicon counterparts (Fig. 1.4).

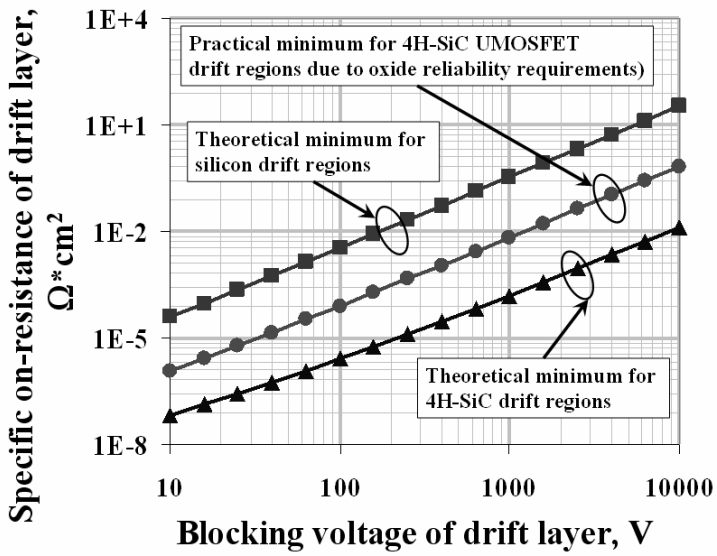


Figure 1.4: The practical minimum for the drift region specific on-resistance of 4H-SiC UMOSFET with SiO_2 gate dielectric compared to the theoretical values calculated for 4H-SiC and Si as a function of blocking voltage [18].

A typical vertical SiC DIMOSFET shown in Fig. 1.3 (b) comprises both the horizontal inversion channel under the gate oxide (MOS region) and the vertical channel confined between two p-well implanted regions (JFET region). Because of its dual-channel structure, the vertical SiC DIMOSFET offers high blocking capabilities along with low on-state voltage drop. In contrast to the SiC UMOSFETs where the gate oxide is the weakest part of the device because of its location in the region of the highest electric field, DIMOS structure provides excellent protection of the gate oxide from electric breakdown by screening it with p-n junctions. Partial sacrifice of on-state conductance by the introduction of a JFET region can be justified

in the case of SiC MOSFETs, where channel resistance is still the dominant part of the total device resistance due to very low inversion channel mobility. Moreover, higher electric field is permitted in the drift region of SiC DIMOSFET, and this allows for significant reduction of drift resistance as compared to the UMOS drift region. Another benefit

of using the DMOS configuration is that the MOS channel can be made on the planar silicon-face surface of SiC, where SiC/SiO_2 interface quality is found to be optimal as opposed to the vertical trench surfaces in the UMOS [19]. Although the low channel-packing density due to the presence of the lateral MOS channel and the high resistance of the JFET region seriously impact the total device on-resistance, the vertical 4H-SiC DMOS-like transistors are the power SiC MOSFETs closest to the market. They are now under very intense investigation by leading SiC device developers. Increasing channel packing density by implementing self-aligned fabrication process and advanced layout solutions in conjunction with sophisticated gate oxide growth/annealing techniques will help to overcome the issues of low inversion channel mobility and gate oxide reliability for a SiC MOSFETs.

1.2 SiC Power Rectifiers

1.2.1 PiN diodes

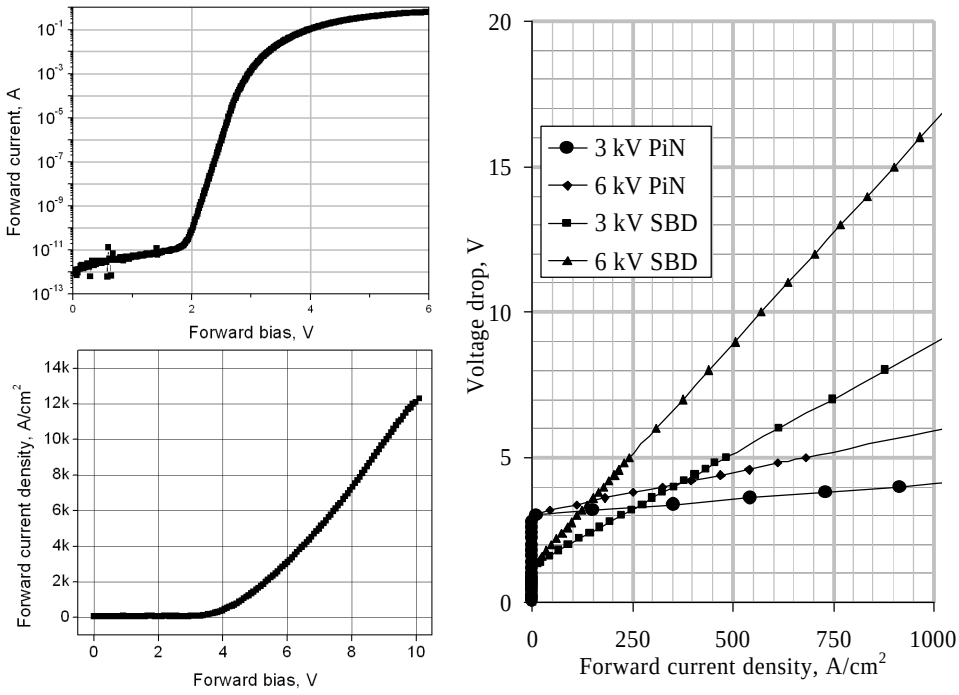
Recently rather revolutionary results were reported for ultra-high power 4H-SiC PiN diodes [21-23]. As compared to SiC Schottky barrier diodes (SBDs) and Merged Schottky-PiN diodes (MPS, JBS or pitch diodes), PiN diodes can offer higher forward current and blocking voltage [24]. The simulation results shown in Fig. 1.5 demonstrate the dramatic advantage of PiN diodes over SBDs in the high voltage

application, where ultra-fast switching is not required. Even though the injected minority carriers affect the switching performance, SiC power PiN diodes still demonstrate extremely fast reverse recovery due to relatively small minority carrier lifetime. For example, when switching from 20 A to 0 A, a recovery time of 105 ns was reported for a 10 kV PiN diode at room temperature [25].

The major challenge in the commercialization of high-voltage high-current SiC PiN diodes is related to by the long-term reliability issue due to the recombination enhanced stacking fault formation. This phenomenon has been investigated in numerous studies (*e.g.*, [26]). In commercially available SiC substrates, where the traditional 8º off-axis crystal orientation is used, stacking faults may create numerous potential barriers to the current flow. These barriers act as recombination centers, resulting in shorter effective ambipolar lifetime in the base region, and consequently, an increase of the forward potential drop.

Moreover, the released energy during recombination promotes further development of these defects, which penetrate through the crystal along the basal plane. To solve this problem in vertical bipolar devices, so called “a-face” crystal orientation can be used plane the carriers do not meet any potential barriers, and the recombination enhanced defect formation does not occur. Unfortunately, the PiN diodes built on the “a-face” material exhibit lower breakdown voltages than those built on the traditional substrates [27]. To prevent an extensive stacking fault formation when using “off-axis” substrates, the maximum current density in a PiN diode should be limited to a safe value. Since stacking faults originate from the basal plane dislocations, availability of dislocation-free material may be the way to solve the problem of

forward current degradation. Ref. [27] also reports on encouraging results of fabricating 4H-SiC PiN diodes with low forward degradation using processes that reduce basal plane dislocations in the epitaxially grown layers.



(a) (b)

Figure 1.5: Measured forward characteristics of a 3 kV PiN diode fabricated in SemiSouth (a), and a theoretical comparison of a forward voltage drop for power rectifiers as a function of current density (b).

1.2.2 *Schottky Barrier Diodes*

The major advantages of Schottky barrier diodes (SBDs) are ultra fast switching characteristics, low turn-on voltage, and cost-effective fabrication processes. As they are majority carrier devices, SBDs can be easily paralleled to achieve high forward current without the danger of thermal runaway.

As the built-in potential of the Schottky barrier is usually lower and the junction is physically located at the semiconductor surface, the blocking voltage of a SBD is typically smaller than that of a PiN diode for the same thickness of the voltage blocking layer. However, the use of a proper surface passivation/termination technique allows achieving blocking capability of SiC SBDs close to that of SiC PiN diodes. For example, in Ref. [28], we reported on SBDs, with a blocking voltage of 1.6 kV on a 10 μm, $5x10^{15}$ cm^{-3} drift region (Fig. 1.6).

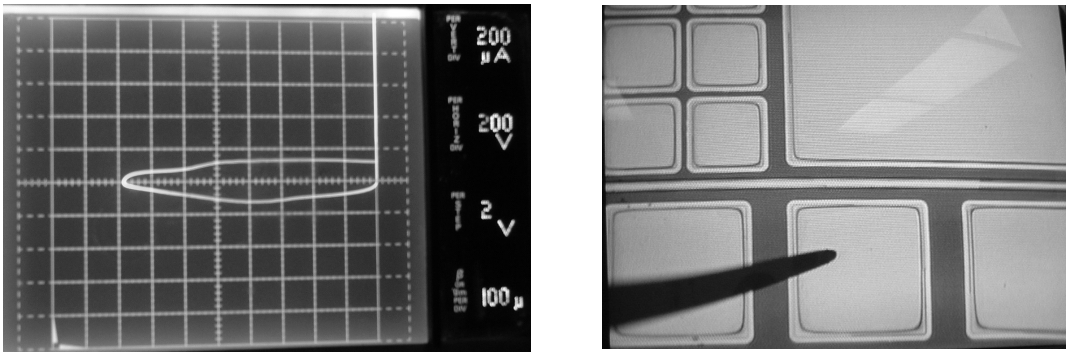


Figure 1.6: Reverse blocking characteristics of a 1.6 kV 4H-SiC SBD (left), and a die-level view of probed SBD's (right) [28].

1.2.3 JBS and MPS Diodes

Junction Barrier Schottky (JBS) or Merged PiN Schottky (MPS) diodes comprise both p-n and Schottky barrier junctions in the same device. In SiC, such combination allows the device to exhibit the best characteristics of both types of junctions, providing surge current and overvoltage protection, while maintaining low turn-on voltage and ultra-fast switching. At normal operating conditions, the device acts as a Schottky barrier diode, when the majority of the current flow occurs through the Schottky contacts. At surge current conditions, however, the current flows mainly

through the p-n junctions because of significant reduction in drift resistance due to conductivity modulation at high current densities. In Ref. [29], we proposed a mesa-terminated MPS diode structure with epitaxially grown anode islands. A schematic cross-section of this device is shown in Fig. 1.7. As compared to SBDs where the reverse leakage current is caused mainly by thermionic field emission through the Schottky barrier, JBS diodes provide significant improvement in the breakdown strength by shielding the Schottky barrier regions with p-n junctions, especially at elevated temperatures. The recent publications showed great potential for the JBS diode to combine the best characteristics of PiN and Schottky diodes [24, 30].

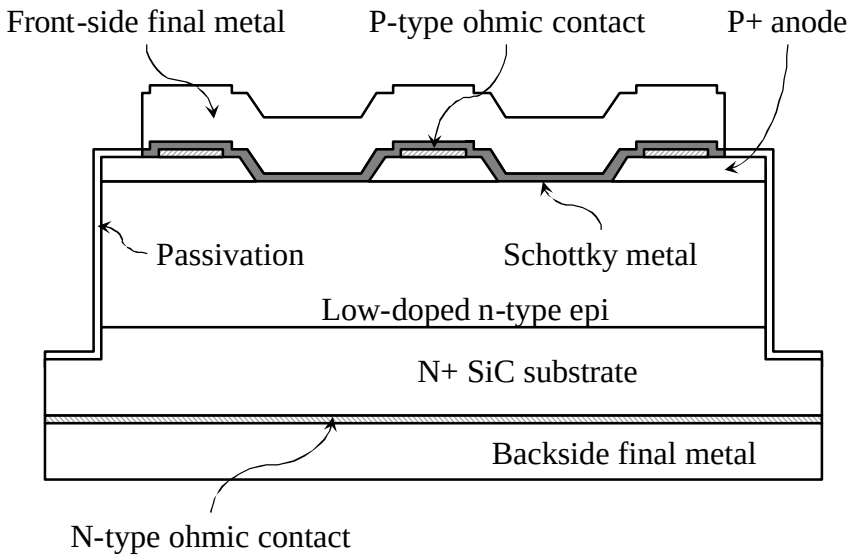


Figure 1.7: A schematic cross-section of a Schottky barrier diode with surge current protection.

1.3 SiC Power RF Devices

1.3.1 MESFETs

SiC MESFET has attracted tremendous attention of the developers as the ideal device for high power pulsed and continuous-wave (CW) high-frequency (from UHF to X band) linear wide bandwidth monolithic microwave integrated circuits (MMICs) [31]. Significant success has been achieved in the power SiC MESFET development in the past decade; however, some issues still remain to be solved.

One of the major problems preventing wide commercialization of power SiC MESFETs is the current instability due to the trapping effects. Trapping effects occur when electrons get trapped by the acceptor-like levels either in the semi-insulating (SI) substrate (so called backgating) or at the surface. Figure 1.8 shows the schematic cross-section of a SiC MESFET fabricated on a SI substrate with a p-type buffer layer. In this figure, the regions where electrons get trapped by acceptor states are indicated in the drawing by minus signs.

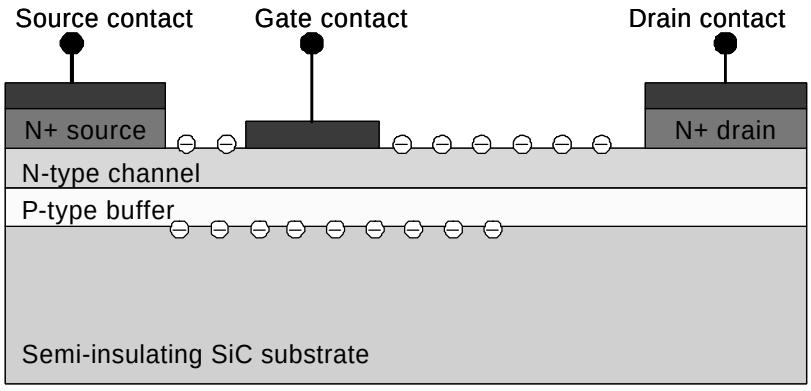


Figure 1.8: Schematic cross-section of a SiC power MESFET.

The use of a p-type buffer layer that separates the channel from the substrate has been proven as an efficient way to reduce backgating [32]; however the choice of the buffer layer doping concentration becomes a trade-off of several factors. The doping of the buffer layer must be chosen high enough to prevent electron injection into the substrate. On the other hand, an increase of the p-doping concentration would result in corresponding increase of the parasitic p-n junction capacitance which will automatically degrade the high frequency performance. The doping concentration typically used in the p-type buffer layer is less than $5?10^{15}$ cm^{-3}. The use of the recently introduced high-purity semi-insulating substrates was reported to significantly minimize current instabilities caused by the backgating effect [33].

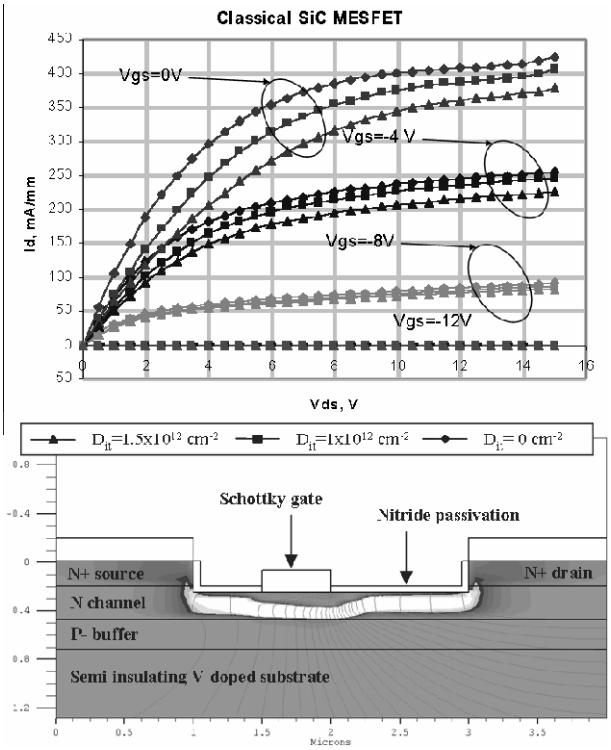


Figure 1.9: Atlas™ simulation of MESFET drain current instability in due to surface trapping effects (top), and current density distribution in the channel at zero gate bias (bottom) [34].

Table 1.1: Reported approaches for the reduction of the surface trapping effects.

Reported approach	***Advantages***	***Drawbacks***
➢ Surface passivation	Improved current stability due to reduction in the interface state density	Even after passivation, D_{it} still remains in the 10^{12} $eV^{-1}cm^{-2}$ range [35].
➢ Gate-recessed or buried gate structure	Improved current stability by distancing the main current stream away from the surface	Extremely complicated fabrication, that requires expensive critical alignment steps [36]

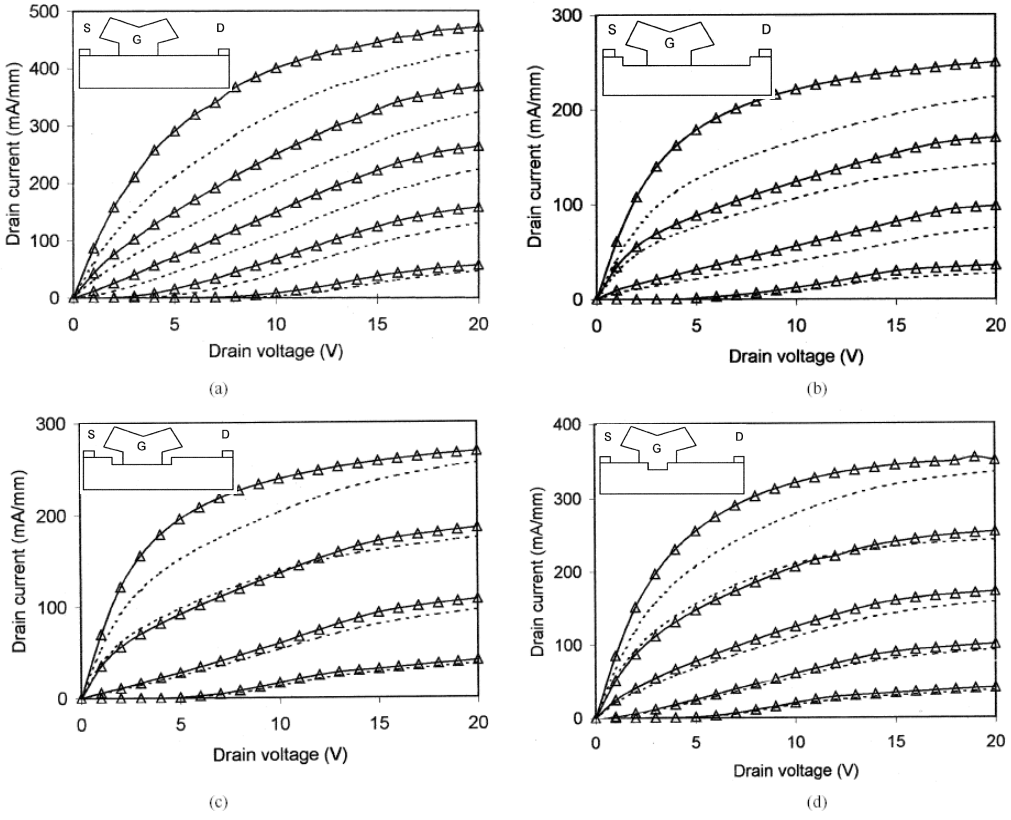


Figure 1.10: Comparison of current instability phenomena for different gate designs (After Ho-Young Cha *et al* [36].)

In Ref. [34], we investigated the influence of the surface trapping effects on the drain current stability of 4H-SiC MESFET using Silvaco Atlas™ simulation, as illustrated in Fig. 1.9. In this simulation, the transient of charging-discharging interface states is modeled by simulating the drain current with different density of interface states occupied by electrons. The vanadium doped semi-insulating substrate has been modeled by introducing occupied acceptor-like traps with an energy $E_T=E_V+1.05eV$ and a concentration of $1x10^{17}$ cm^{-3} into the non-doped material.

There are several ways to reduce surface trapping effects. First of all, different techniques may be employed to passivate the interface states, although even after advanced passivation the interface state density remains in the 10^{12} range [35].

The introduction of a stable negative charge at the SiC/insulator interface may improve current stability by repelling electrons from the surface and preventing their trapping by the interface states. However, in the conventional MESFET structures, the fixed negative interface charge would increase the extrinsic channel resistance by narrowing down the current path between the gate and drain contacts.

An alternative approach is to use a device structure that minimizes the influence of interface traps on current stability by displacing the main current stream away from the surface. Encouraging results have been reported in Ref. [36], where devices with different structures were compared in terms of current stability. Figure 1.10 shows, that current stability can be significantly improved by utilizing gate-recessed or buried gate structures. In this figure, forward measurements are shown in solid lines and backward measurements are shown in dashed lines. The corresponding device structures are shown at the top left corner of each family of curves: non-

recessed (a), channel-recessed (b), gate-recessed (c), and buried-gate (d). It can be noticed, however, that even this structure cannot completely eliminate the instability of the drain current at low gate biases, when electrons flow in close vicinity to the surface. Table 1.1 summarizes the reported approaches for the reduction of surface trapping effects listed above.

In Ref. [37], we proposed a new approach to eliminate current instability in SiC MESFETs resulted from surface trapping. Figure 1.11 shows the schematic cross-section, SEM image, and measured DC and RF characteristics of a fabricated 4H-SiC self-aligned MESFET structure. In order to minimize the surface trap density, this devise uses the basic surface passivation. However, even with a high interface state density, the surface trapping effect is virtually eliminated, because in the source-to-gate and gate-to-drain segments current does not flow in the close vicinity to the surface, but rather in the bulk material of the source and drain fingers.

DC testing has been done on the fabricated structures to determine if the self-aligned MESFET design indeed has improved current stability. Very little (if any) hysteresis was observed in the I-V characteristics of the self-aligned MESFETs. For comparison, a planar SiC MESFET with the traditional design was tested using the same method as the self-aligned MESFET. The traditional MESFET had very pronounced I_D vs. V_{DS} hysteresis when compared to the self-aligned MESFET as shown in Fig. 1.12. These I-V curves indicate that the drain current in the conventional MESFET was noticeably reduced due to charge trapping while the self-aligned MESFET showed no such current reduction under these conditions.

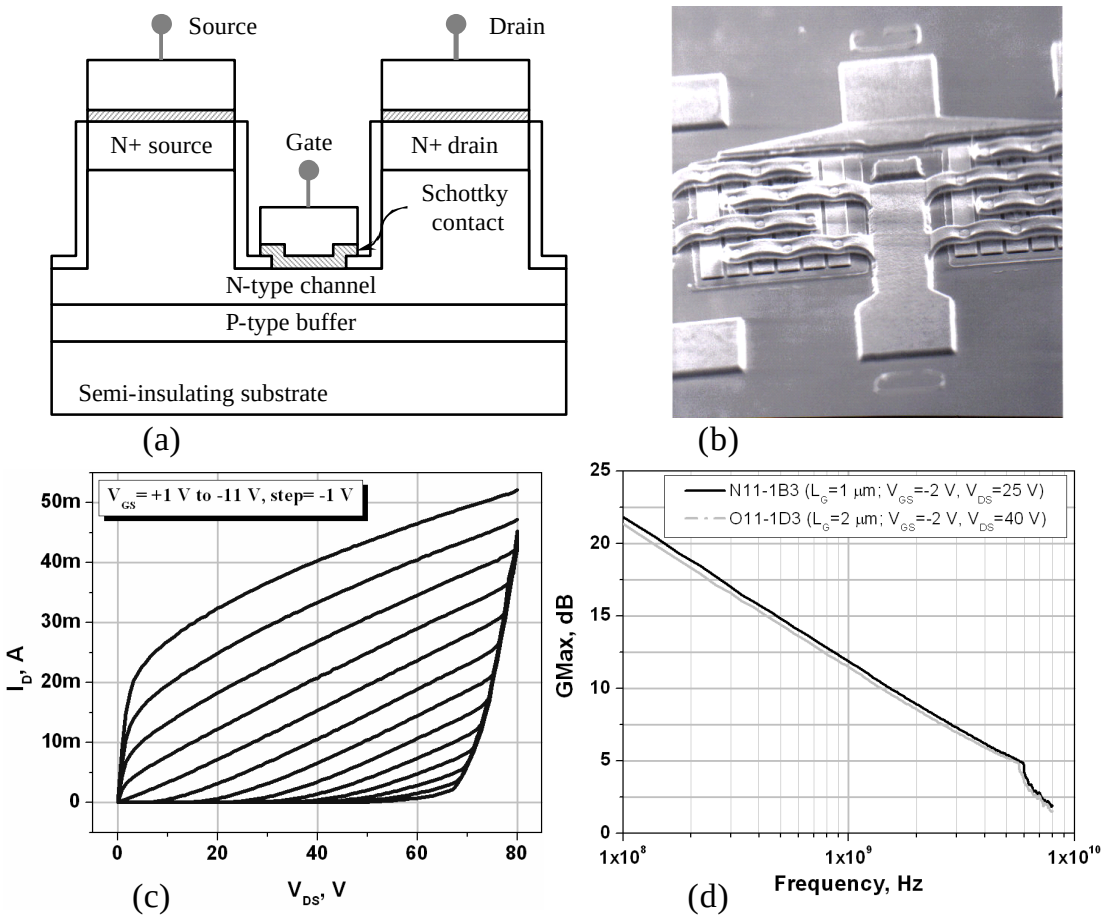


Figure 1.11: Schematic cross-section (a), SEM image (b), and measured DC (c) and RF (d) characteristics of a self-aligned 4H-SiC MESFET.

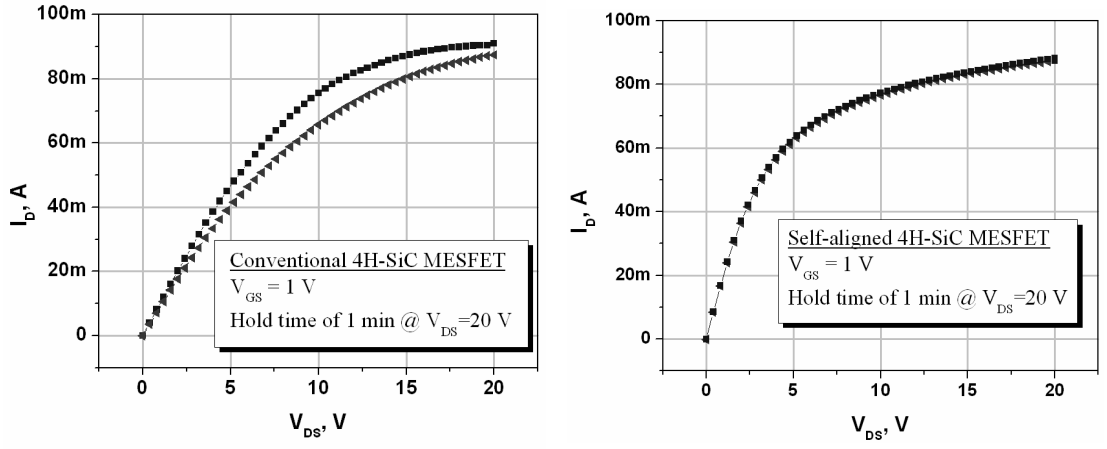


Figure 1.12: Comparison of current stability in conventional and self-aligned MESFETs.

From the fabrication point of view, the distinctive feature of this design is the gate formation using a self-aligned process. Unlike many other MESFET- and SIT-related "self-aligned" processes (*e.g.*, [38]), the process described in [37] is truly self-aligned, because it excludes all the critical alignment steps.

1.3.2 SITs

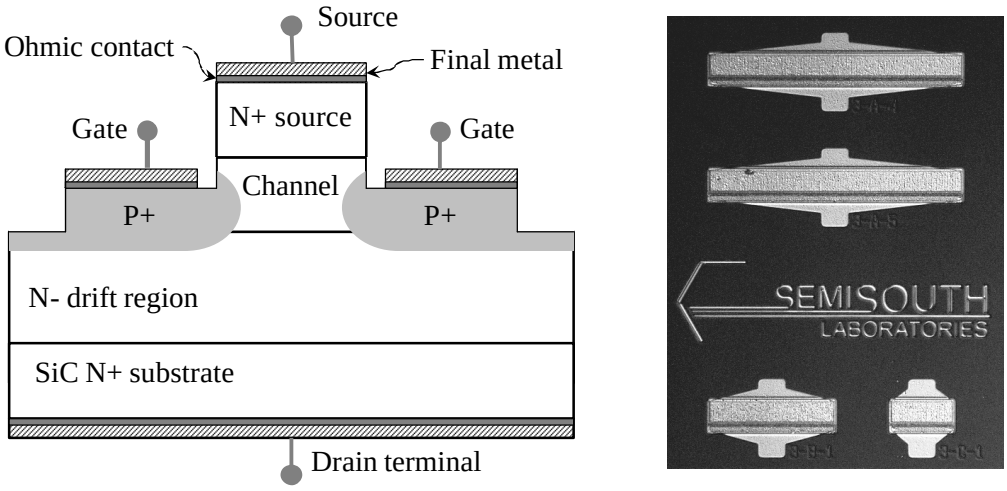
The Static Induction Transistor (SIT) is a vertical, short channel MESFET or JFET type device, which has the gates close together resulting in space charge limited current conduction. Unlike the bipolar junction transistor (BJT), the SIT is a majority carrier device that is voltage-controlled and it offers higher breakdown voltage and input impedance for the same frequency range. SiC SIT is based on the original SIT concepts published in 1950 [39], which have received continued development for the past 5 decades [40-45]. While most initial SIT developments have occurred in Si, the availability of high quality SiC substrates over the past 10 years has triggered a renewed interest in this device. By use of SiC, it is possible to increase the voltage (and thus power) rating of high-frequency amplifiers, and increase the power density by a factor of 4 to 10 in UHF to S-band transistors. Parasitic capacitances are reduced, by shrinking the device area, while maintaining the power level of the devices that often require little or no external impedance matching.

There are two types of gate, which are commonly used in the SiC SIT: ion-implanted p-type gate [42] and Schottky gate [43]. Both of them have their advantages and drawbacks. While Schottky-gated 4H-SiC SITs offer higher operating frequency, the devices with p-type gates are much more suitable for high power

applications. In general, using a channel structure with p-type implanted gates is more preferable because of the following advantages over the Schottky-gated devices:

- Lower gate leakage allows for higher operation voltages and thus output power;
- Robust structure less susceptible to rough environmental conditions;
- Simple fabrication process.

In Ref. [46], we report on the design and fabrication of 400 V L-band 4H-SiC SITs with implanted-gate channel structure. A schematic cross-section and an optical photograph of the fabricated devices are shown in Fig. 1.13. The family of I-V characteristics measured using a Tektronix 576 curve tracer and the results of load-pull measurements performed on the fabricated devices are shown in Fig. 1.14. Detailed discussion on the fabrication and testing of these devices can be found elsewhere [46].



(a) (b)

Figure 1.13: Schematic cross-section and a photograph of fabricated 4H-SiC L-band SITs.

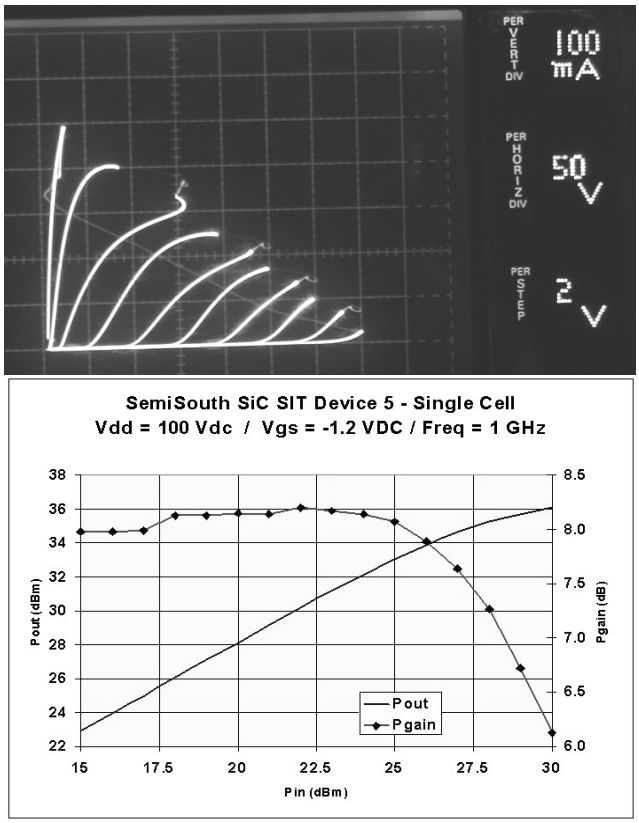


Figure 1.14: DC (a) and RF (b) characteristics of fabricated 4H-SiC L-band SITs.

1.3.3 RF BJTs

As a vertical RF device, SiC BJT can potentially offer several advantages over SiC MESFET:

- Much lower specific on-resistance for the same breakdown voltage allows for much higher output power;
- High field regions are buried, which makes the device less susceptible to surface effects;
- Threshold voltage uniformity, which is critical for analog operation
- High linearity;

Several attempts to achieve RF performance on 4H-SiC bipolar junction transistors have been published recently [47, 48]. Despite the optimistic simulation

results that predict possibility of achieving a 700 V SiC BJT device with a f_T of 10 GHz and h_{21} of 100 [49], the state of the art 4H-SiC RF BJTs demonstrate only very moderate RF performance. The best RF SiC BJT published to our knowledge has shown h_{21} of 15 and f_T of 1.5 GHz [47]. This device has demonstrated an output power of 50W/cell using 80 V supply in common emitter Class AB mode with collector efficiency of 51% and power gain of 9.3 at 425 MHz. It has been concluded in Ref. [49], that the implanted emitter approach is not suitable for the BJT fabrication in the SiC technology, and both the base and the emitter region have to be grown epitaxially. Making the epitaxial base as thin as possible is very desirable in high frequency applications. However, the fabrication of a SiC BJT with very thin base becomes extremely challenging. The major issues that arise are how to make an ohmic contact to such a base, and how to make the peripheral base resistance reasonably small? The first issue is related to the material consumption by the metal silicide that can lead to punch-through of the base under the contact region. It is also very difficult not to overetch a thin base layer with a thickness of, for example, 0.1 μm. The sheet resistance of this region may be too high to get an acceptable microwave performance. The possible way to solve the problem with he high peripheral base resistance was proposed in Ref. [9], where the authors first formed the active base region having it thinned down to 0.8 um, and then overgrew the emitter region.

In Ref. [50], we suggest another approach to solve all the problems listed above by using a heavily doped overgrown base region. As shown in Fig. 1.15, this region provides the electrical contact to the narrow base, and minimizes the

peripheral base resistance. The high doping level of the overgrown extrinsic base layer prevents minority carrier injection inside it from the emitter because the potential barrier between the emitter and overgrown p+ layer is higher than that between the emitter and p-type base region. It also avoids expensive ion implantation and post-implant anneal steps when making the p-type base ohmic contact.

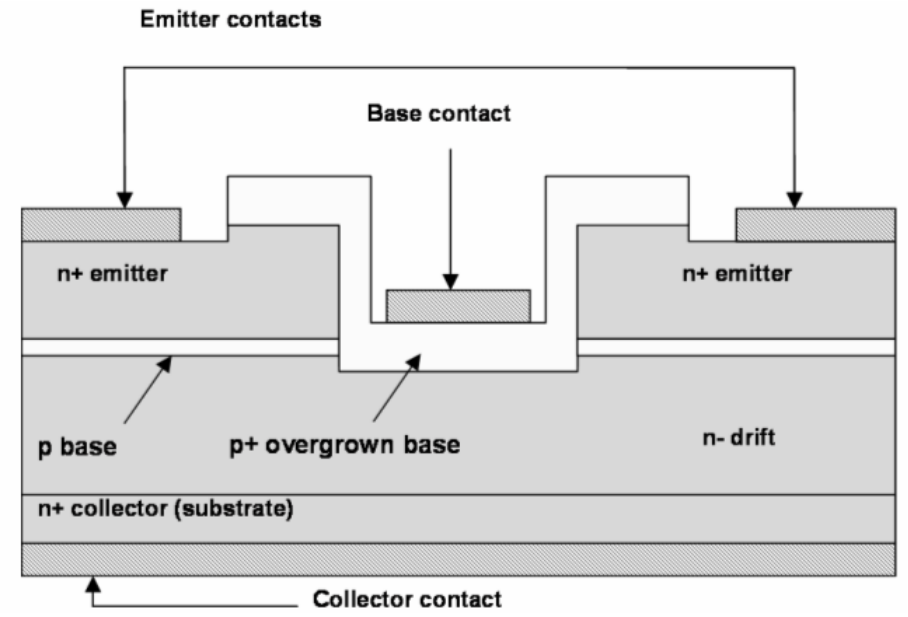


Figure 1.15: SiC BJT with overgrown p+ base region.

1.3.4 *IMPATT Diodes*

Silicon and GaAs impact-ionization-avalanche-transit-time (IMPATT) diodes are widely used in a broad range of microwave and millimeter wave applications. The most typical of them are pulsed and continuous wave (CW) injection-locked amplifiers, active frequency multipliers, cavity stabilized and voltage controlled oscillators, pulsed power sources, etc. The use of silicon carbide (SiC) as the building material for IMPATT diodes in these applications opens an exciting

possibility to exceed the power limits far beyond those dictated by the Si and GaAs material properties.

Avalanche transit time devices are considered to be potentially the most powerful solid-state power sources for microwave applications, particularly for solid-state transmitters in pulsed radar systems. The theoretical estimations of the maximum output power of an IMPATT diode operating at frequency f under pulsed conditions is given by Ref. [51]:

$$P_{out\,\max} \le \frac{h \cdot E_{crit}^{2} \cdot v_{sat}^{2}}{4 \cdot p^{2} \cdot X_{C} \cdot f^{2}} \tag{1.1}$$

In (1.1), X_C is the capacitive reactance of the diode and other values have their usual significance. It can be seen from the expression above, that the peak output power of a diode has a square law dependence upon the saturation drift velocity and the critical electric field of the underlying material. Such dependence makes SiC the most promising semiconductor to use in fabrication of IMPATT diodes because of its high breakdown field strength and high electron saturation velocity. When considering the expression for maximum output power and the properties of SiC in comparison with Si and GaAs, it becomes evident that a SiC IMPATT diode would produce microwave power at least two orders of magnitude higher than Si or GaAs IMPATT diodes.

Recently, extensive analytical and numerical studies of SiC IMPATT structures including large- and small-signal analysis as well as Monte-Carlo simulations have been performed by several groups [52-54]. A large-signal simulation performed for both Ka-band and X-band 4H-SiC IMPATT oscillators

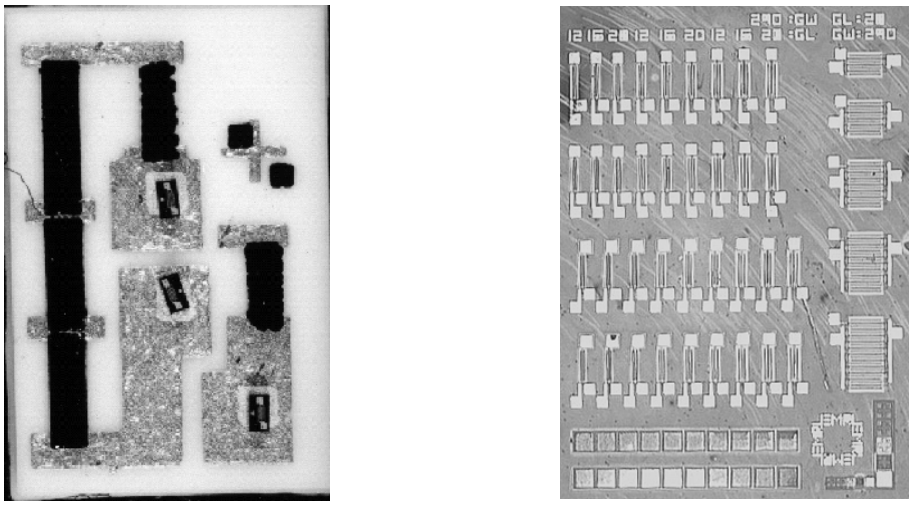
predicts the peak power capability of more than 1 kilowatt, with greater than 15% power efficiency [55].

To achieve the high output power, the IMPATT diode must conduct as much avalanche current as possible. Experimental results have shown that 4H-SiC diodes can sustain an avalanche current density of 60kA/cm^2 without catastrophic failure [56]. When the diode is operating at such tremendous current densities, the dissipated heat in the semiconductor junction becomes a significant factor limiting the output device power, and the thermal properties of the material become of major importance. In this respect, SiC is once again the material of choice because of its superior thermal conductivity, which is 8.9 times higher than that of GaAs, and 3.8 times higher than that of Si and GaN. The wide bandgap, and consequently, small intrinsic carrier concentration allows SiC IMPATT diodes generate useful power even at extremely high junction temperatures.

To the best of our knowledge, only two groups have published experimental results on SiC IMPATT diodes so far [57, 58]. High-low single-drift 4H-SiC IMPATT diodes fabricated in Purdue University demonstrated a power level of 1 mW at 7.75 GHz [57]. 4H-SiC IMPATT diodes have also been demonstrated by Vasillevski *et al* [58]. The diodes have an avalanche breakdown voltage of ~290 V. Microwave oscillations appeared in X-band at a threshold current of 0.3 A. The maximum output power of 300 mW was measured at an input pulsed current of 0.35 A. These first experimental results from SiC IMPATT diodes, however, show efficiency and power output far below the theoretically predicted values of SiC and significant improvement for this technology is expected.

1.4 SiC Smart Power Technology

As a wide bandgap semiconductor, SiC is very attractive for use in high-power, high-temperature, and/or radiation resistant electronics. Monolithic or hybrid integration of a power transistor and control circuitry in a single or multi-chip wide bandgap power semiconductor module is highly desirable for such applications in order to improve the efficiency and reliability. SiC smart power technology has been a topic of discussion in recent years. The majority of the efforts related to this topic were focused on the development of SiC MOS-based technologies including NMOS and CMOS ICs [59-61] and power LDMOS transistors [62, 63].



(a) **(b)**

Figure 1.16: a) The photograph of a hybrid temperature sensor which operated from 500°C to -150°C built on lateral 6H-SiC JFETs [66]; b) The photograph of lateral JFET die [67].

Despite the demonstration of sufficient high-temperature performance (up to 600ºC), the MOS-based SiC integrated technology has a fundamental problem concerning the long-term reliability in harsh radiation environment due to radiation-

induced degradation of gate oxide [64]. To circumvent the fundamental problems of MOS based devices in SiC, JFET IC logic capability can be developed based on the results of single lateral SiC JFETs and JFET-based hybrid circuits, which have been designed and fabricated [66, 67] as shown in Fig. 1.16. Recently, SiC power RESURF Lateral JFETs have also been published [68].

In Ref. [69-71], we proposed a novel SiC JFET structure, Lateral Trench JFET (LTJFET), as a potential transistor-candidate for use in SiC high-temperature smart power electronics. A schematic cross-section of this device, which combines a vertical source-channel-drift structure with a lateral drain layer, is shown in Fig. 1.17.

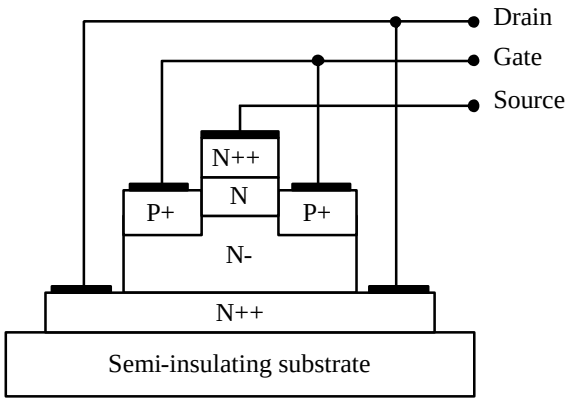


Figure 1.17: A schematic cross-section of a Lateral Trench JFET (LTJFET).

LTJFETs can be monolithically integrated by using a p-type buffer layer between the n+ drain layer and the conducting substrate for junction isolation or using a semi-insulating substrate. The pinch-off voltage of the LTJFET depends on the thickness of the vertical channel (finger width), which can be defined by photolithography. The simplicity to define the pinch-off voltage by the layout design allows the LTJFETs to be implemented for enhanced and depletion modes of

operation on the same chip to form digital or analog control circuitry. Moreover, the monolithic integration of power enhanced- and depletion-mode LTJFETs in cascode fashion results in normally-off power switch that can be formed on the same chip and controlled by the logic levels of the LTJFET control circuitry [70]. The detailed discussion of these topics is given in the following subsections.

1.4.1 LTJFET Control ICs

The high-temperature performance of a monolithic SiC LTJFET inverter built of enhanced- and depletion mode n-channel devices has been investigated by numerical device simulation using Silvaco Atlas software. The schematic cross-section and the simulated waveforms of this logic gate are shown in Fig. 1.18. As shown in Fig. 1.18 (b), the switching waveforms exhibit insignificant distortion with temperature rising from for 0ºC to 500ºC. The vertical channel geometry, where the current is confined between two p-type regions, makes the LTJFETs highly tolerant to interface-related issues that have significantly slowed down the development of MOSFET-based SiC integrated circuits. First, the vertical-channel SiC JFETs demonstrate a negligible shift of threshold voltage with the temperature [71]. Secondly, high electron mobility is obtainable in the vertical n-type epitaxially-grown channel of the LTJFET, unlike the SiC MOSFETs which still suffer from poor inversion channel mobility.

In order to show the feasibility of LTJFET ICs, simple logic gates have been built using discrete E- and D-mode vertical JFETs fabricated by SemiSouth. These circuits were tested with 2.75 V power supply and input levels of 0.25 V (LOW) and

2.75 V (HIGH). The photograph, room-temperature switching waveforms, and logic performance of a hybrid NOR gate where E- and D-mode vertical JFETs were output HIGH and LOW levels almost identical to the input levels. The rise and fall times of the output voltage have been measured to be 30 ns and 10 ns respectively. This high switching speed demonstrated by a *hybrid* circuit built of power multi-finger devices with 1-cm gate periphery demonstrate the feasibility of ultra-fast *monolithic* circuits based on the SiC LTJFET technology.

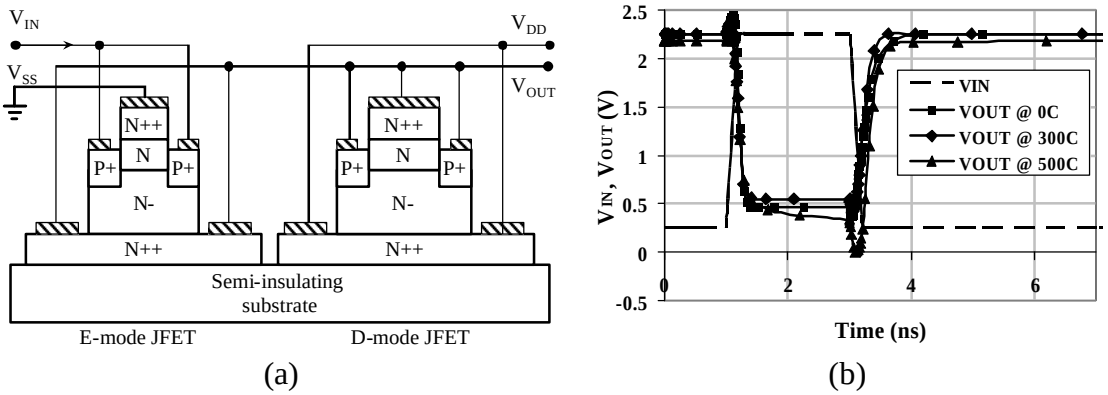


Figure 1.18: (a) Schematic cross-section and (b) waveforms of a monolithic SiC LTJFET inverter simulated for 0ºC, 300ºC, and 500ºC using a 2-D device simulator.

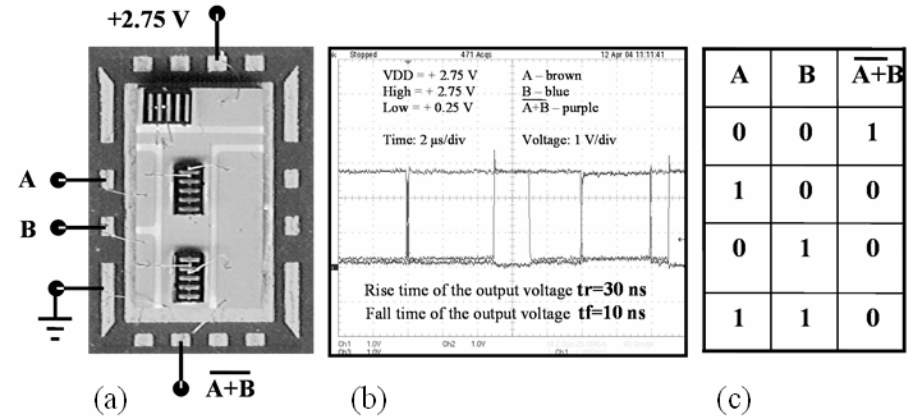


Figure 1.19: (a) The photograph, (b) the measured waveforms, and (c) the measured truth table of a hybrid SiC JFET NOR gate.

1.4.2 LEDFET Power Switch

Monolithic cascode integration of JFETs was proposed several decades ago [73]. More recently, hybrid cascode circuits comprising Si MOSFET and SiC VJFET were published [7]. In Ref. [69, 71], we proposed a normally-off Lateral Enhanced-Depletion Field-Effect Transistor (LEDFET) obtained through monolithic integration of E- and D-mode power LTJFETs. The LEDFET can be controlled by the logic levels of the LTJFET control circuitry formed on the same chip. The schematic cross-section and the I-V characteristics of a simulated monolithic SiC LEDFET power switch are shown in Fig.1.20.

In order to demonstrate the feasibility of a normally-off SiC monolithic cascoded switch, it was emulated using discrete non-terminated E- and D-mode vertical JFETs fabricated in SemiSouth. Fig. 1.21 shows a photograph and the measured characteristics of a hybrid normally-off, 900 V power switch. Despite a relatively high leakage current (I_D=330 μA @ V_{DS}=900 V and V_{GS}=0V) and somewhat low forward conduction induced by the D-mode device built on the early stage of development, this circuit credibly demonstrated the potential of the investigated device as the only SiC power switch that can be controlled by a voltage sweep from 0V to 2.5 V.

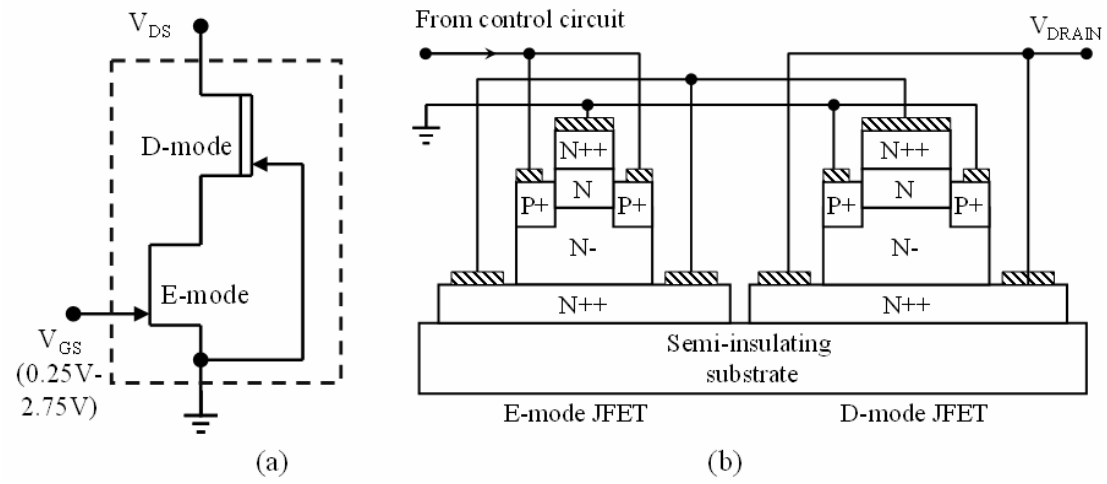


Figure 1.20: (a) The equivalent circuit and (b) the schematic cross-section of a SiC LEDFET.

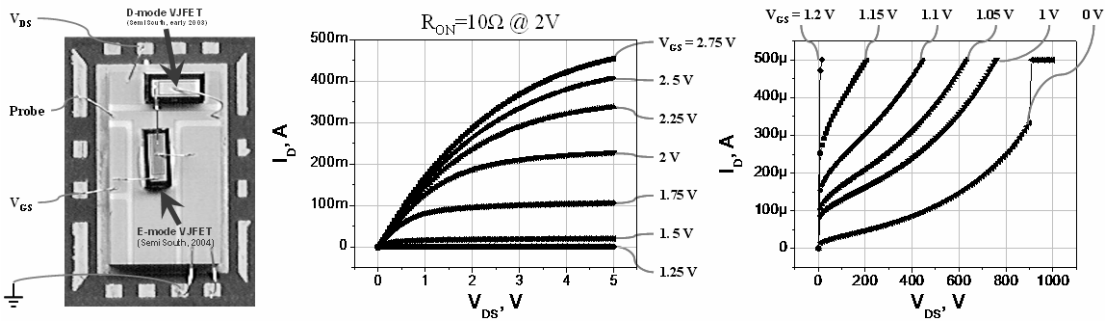


Figure 1.21: The photograph (left) and the measured I-V characteristics (right) of a hybrid SiC SIT normally-off power switch.

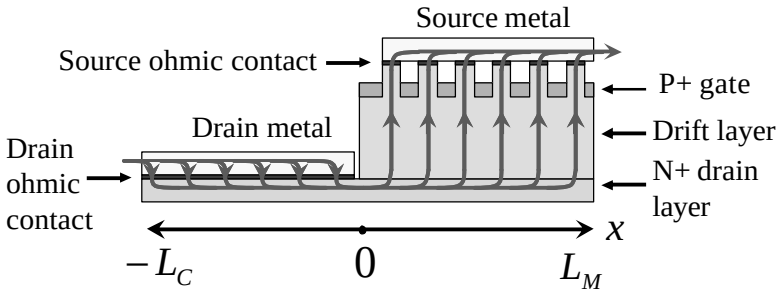


Figure 1.22: The current flow in a multi-finger LTJFET.

Obviously, the lateral nature of the current conduction imposes specific requirements on the lateral dimensions of a power multi-finger LTJFET (Fig. 1.22). The lengths of the drain contact L_C and the mesa L_M should be chosen to minimize the total specific on-resistance of the LTJFET. The following expression can be used to determine the optimal values of L_C and L_M :

$$R_{sp-on} = \sqrt{r_S} \cdot (L_C + L_M) \cdot \left[\sqrt{r_C} \cdot \frac{a+1}{a-1} + \sqrt{r_M} \cdot \frac{b+1}{b-1} \right]$$
$$a = \exp\left(2 \cdot L_C \cdot \sqrt{\frac{r_S}{r_C}} \right) \qquad (1.2)$$
$$b = \exp\left(2 \cdot L_M \cdot \sqrt{\frac{r_S}{r_M}} \right)$$

In (1.2), r_S represents the sheet resistance of the drain layer, r_C is the drain specific contact resistance, and r_M is the specific resistance of the device mesa.

1.5 Challenges to SiC Device Technology and Research Motivation

Despite the overall progress made in the development of SiC power device technology, certain challenges related to the device performance and reliability are still present. The most common and difficult to solve issues that slow the expansion of SiC into industrial applications are summarized in Table 1.2. Although solving all the listed problems is very important, this work is focused on the reduction of the resistance of voltage-blocking layer, as the most general issue that impacts the whole SiC power device technology. The following chapters study different edge-termination and field-compensation approaches that optimize electric field distribution in the voltage blocking layer in order to reduce its resistance.

Table 1.2: The most significant challenges to SiC power device technology.

Issue	Result	Technology affected
Material defects resulted from SiC bulk and epitaxial growth	Low current due to yield-limited die size	Vertical SiC devices
	Poor long-term reliability due to recombination-enhanced stacking fault formation from basal plane dislocations	SiC bipolar devices
Poor SiC/dielectric interface properties	High channel resistance due to poor inversion channel mobility; Temperature dependence of threshold voltage due to ionization of interface states	SiC MOS-based devices
	Reduced current gain due to high surface recombination velocity	SiC BJTs
	Reduced current due to surface trapping effects	SiC lateral devices
Non-optimal electric field distribution in voltage-blocking layer	Increased resistance of voltage-blocking layer due to thicker (or longer) and lower-doped voltage-blocking layers required to maintain electric field below its critical value.	SiC power devices

Chapter II theoretically investigates the mechanisms behind different edge termination techniques. The influence of the passivation layer properties, such as net interface charge and dielectric permittivity, on the devices with different edge terminations is also analyzed using numerical simulation. The chapter also presents an analytically derived optimal set of the design rules for JTE-terminated vertical device without conductivity modulation in the voltage blocking layer.

Chapter III studies the applicability of a field-compensation principle in lateral SiC devices that allows for dramatic reduction of the resistance of voltage blocking

layer. A set of compact analytical expressions for the optimal dopings and dimensions of the devices implementing the field compensation principle are derived and validated with the results of numerical simulations that are also presented.

Chapter IV experimentally investigates different edge termination approaches to reduce the maximum electric field in the SiC power diodes, and Chapter V discusses the design and fabrication of a lateral SiC MOSFET with the surface electric field reduced by a combination of two edge termination techniques.

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CHAPTER II

THEORETICAL STUDY OF EDGE TERMINATION TECHNIQUES

2.1. Introduction

This chapter discusses the effect of the electrical field enhancement at the junction discontinuities and its impact on the on-state resistance of power semiconductor devices. A systematic analysis and quantitative comparison of the techniques that can be used for the edge termination in power semiconductor devices is also given with respect to their applicability in the power SiC electronics. The influence of the passivation layer properties, such as effective interface charge and dielectric permittivity, on the devices with different edge terminations is analyzed using numerical simulation. A simple analytical expression for the optimal JTE dose is proposed for the first time. This expression has been numerically evaluated for different targeted values of the blocking voltage and the maximum electric field, always resulting in the optimal field distribution that does not require further optimization with 2-D device simulator. Numerical analysis of SiC diode structures used in this chapter was confined to solving 2-D Poisson equations under the steady state reverse bias conditions without carrier transport and generation-recombination. All acceptors and donors were assumed ionized and no deep levels were introduced into the simulated device structures.

2.2 On-resistance as a Function of Edge Termination

In power semiconductor devices with high blocking requirements, the resistance of the voltage blocking layer becomes one of the dominant components of the total specific on-state resistance. This means that at a fixed forward voltage drop, conduction current density strongly depends on the thickness t and doping profile $N(x)$ of the voltage blocking layer. The voltage blocking layer in which no conductivity modulation caused by minority carrier injection occurs and in which current flow can be described by drift equations is usually called the drift region. In power SiC electronics, the list of typical devices without conductivity modulation in the voltage blocking layer includes Schottky barrier diodes, VJFETs, vertical MOSFETs and BJTs. Assuming a uniform doping concentration in the drift region N, specific resistance of the drift layer in such devices is given by the following expression:

$$R_{drift}(t_{drift}, N) = \frac{t_{drift}}{q \cdot m \cdot N}, \tag{2.1}$$

where q is electronic charge, and m is the low-field electron mobility. The voltage blocking layer with conductivity modulation where current flow can be approximated by drift-diffusion model [1] is usually called the base region. The list of the devices with conductivity modulation in the voltage blocking layer includes PiN diodes, IGBTs, thyristors, etc. In SiC power electronics, 4H-SiC PiN diode is the closest to commercial release of all devices listed above. Assuming uniform doping concentration in the base layer of a PiN diode N_{base}, the specific resistance of the

base region at high-level injection can be roughly approximated by the following expression [2]:

$$R_{base}\left(t_{base,}\, N_{base}\right) = \frac{t_{base}}{qm_n N_{base} + \dfrac{(m_n + m_p) J_F t_a}{t_{base}}} \tag{2.2}$$

In this formula, μ_n and μ_p are electron and hole mobility respectively, J_F is the forward current density, and t_a is the ambipolar lifetime. Comparing equations (2.1) and (2.2), it can be noticed that the resistance of the base region experiences higher dependence on thickness than that of drift region, although its dependence on the doping concentration is less pronounced.

Let us consider a device having voltage-blocking layer w/o conductivity modulation (*i.e.*, drift region) under high-voltage off-state conditions. Assuming that the entire voltage drop occurs over the drift region and the entire drift region is depleted, the blocking voltage of the device V_b can be expressed in terms of the maximum 1-D electric field under the junction $E_{1D\,MAX}$, as well as the doping and thickness of the drift region N and t_{drift}, respectively:

$$V_b = E_{1DMAX} \cdot t_{drift} + \frac{q \cdot t_{drift}^2 \cdot N}{2 \cdot e_r \cdot e_0} = \mathrm{g}(t_{drift}, N) \tag{2.3}$$

where e_0 and e_r are the dielectric permittivity of vacuum and the relative dielectric constant of the semiconductor, respectively. In order to minimize the specific resistance of a drift layer subject to the constraint $g(t_{drift}, N)$, one can use the method of Lagrange multipliers:

$$\begin{aligned}
&\frac{\partial}{\partial t_{drift}}\left[R_{drift}\left(t_{drift},N\right)-l\cdot g\left(t_{drift},N\right)\right]=0\\
&\frac{\partial}{\partial N}\left[R_{drift}\left(t_{drift},N\right)-l\cdot g\left(t_{drift},N\right)\right]=0\\
&g(t_{drift},N)=V_b
\end{aligned} \tag{2.4}$$

The above derivation assumes that the mobility in the drift layer is constant. In reality, it is a complicated function of the doping concentration and temperature; however this is a reasonable assumption considering a narrow range of the practical doping concentrations used in the voltage blocking layers. Solving the above equation system (2.4) with respect to t_{drift}, N and l results in the optimal epi parameters for the drift region:

$$\begin{aligned}
t_{opt}\left(V_b,E_{1DMAX}\right)&=\frac{3}{2}\cdot\frac{V_b}{E_{1DMAX}}\\
N_{opt}\left(V_b,E_{1DMAX}\right)&=\frac{4}{9}\cdot\frac{e_0\cdot e_r}{q}\cdot\frac{E_{1DMAX}^2}{V_b}
\end{aligned} \tag{2.5}$$

Consequently, the optimal epi parameters yield in the minimal resistance value:

$$R_{driftMIN}\left(V_b,E_{1DMAX}\right)=\frac{27}{8}\cdot\frac{V_b^2}{e_0\cdot e_r\cdot m\cdot E_{1DMAX}^3} \tag{2.6}$$

As shown in (2.6), for a given blocking requirement, the minimum on-state resistance is reversely proportional to the third power of the maximum one-dimensional electric field. This provides a strong motivation to increase the 1-D electric field in power devices in order to reduce on-state losses. Unfortunately, in real semiconductor devices, the maximum electric field cannot be calculated using one-dimensional Poisson's equation. The field increases dramatically at junction discontinuities, such as sharp corners of the Schottky contact or the heavily doped anode mesa in PiN

diodes. Figure 2.1 illustrates the electric field distribution in a 4H-SiC PiN diode with a voltage blocking layer designed for E_{1DMAX}=1.8MV/cm @ V_B=600V when reverse bias of 600 V is applied. Although, the maximum 1-D electric field in the device is well below the critical value for 4H-SiC, the peak electric field that occurs at the edge of the main device junction is high enough to cause device failure due to avalanche breakdown. This peak electric field is proportional to the maximum 1-D electric field:

$$E_{peak} = x \cdot E_{1-DMAX} \tag{2.7}$$

where x is a dimensionless coefficient that is a function of an edge termination technique and the quality of surface passivation. Obviously, the upper limit for E_{peak} should be equal to the critical electric field E_{crit}, at which impact ionization can be triggered. The combination of equations (2.6) and (2.7) gives a direct correlation between the on-state power losses and the quality of edge termination / passivation in power devices with drift region:

$$R_{driftMIN} = x^3 \cdot \frac{27}{8} \cdot \frac{V_B^2}{e_r \cdot e_0 \cdot m \cdot E_{crit}^3} \tag{2.8}$$

Equation (2.8) illustrates the importance of developing an edge termination-passivation technique that makes x as close to unity as possible. Figure 2.2 illustrates the dependence of the specific resistance of an optimally designed 4H-SiC drift region on the quality of the edge termination technique.

The following sections provide a detailed discussion of various methods that help to reduce the peak electric field in power semiconductor devices.

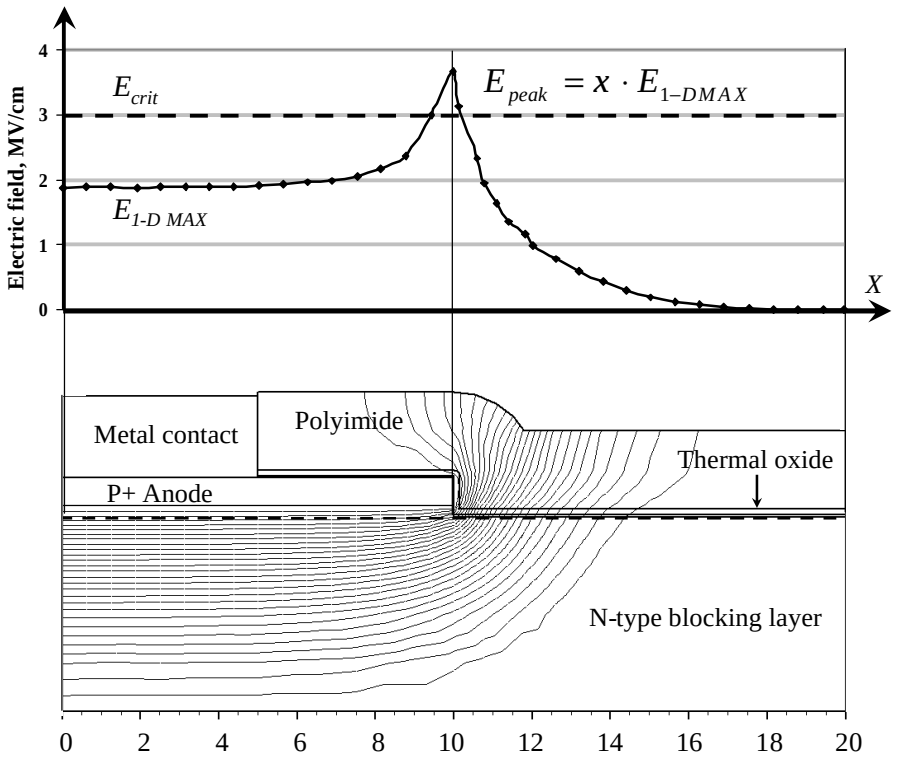

Figure 2.1: Electric field and potential distributions simulated for a 4H-SiC PiN diode without edge termination at reverse bias of 600 V.

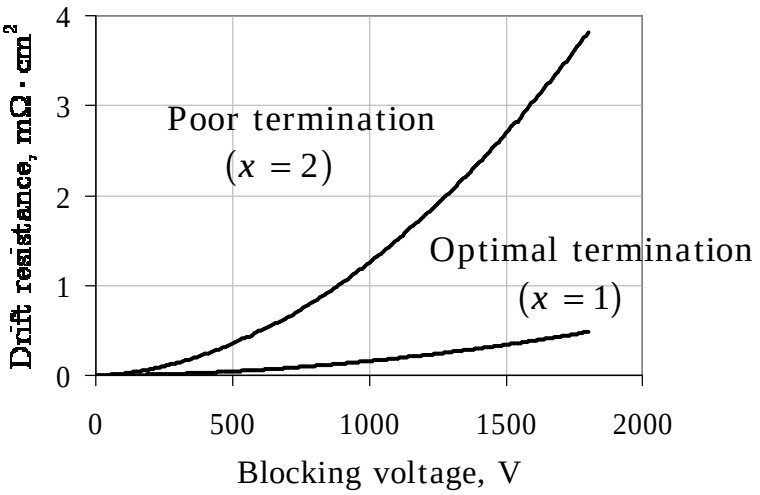

Figure 2.2: Specific resistance of optimally designed 4H-SiC drift layer as a function of blocking voltage for different edge termination-passivation quality.

2.3. System of Edge Termination Techniques

There are two major approaches to eliminate or minimize the electric field enhancement in the semiconductor at the edge of the main junction:

1. Physical removal of semiconductor material from the point of the highest electric field using mesa etching through the main junction and the voltage blocking layer.
2. Lateral extension of the depletion region from the edge of the main junction by one of the following methods or their combinations:
    - Use of a high-k field dielectric on the semiconductor surface surrounding the main junction;
    - Introduction of electrical charge (negative in case of n-type drift region or positive, in case of p-type) at or near the exposed surface of the drift region surrounding the main junction;
    - Introduction of high resistivity layer on the semiconductor surface surrounding the main junction.

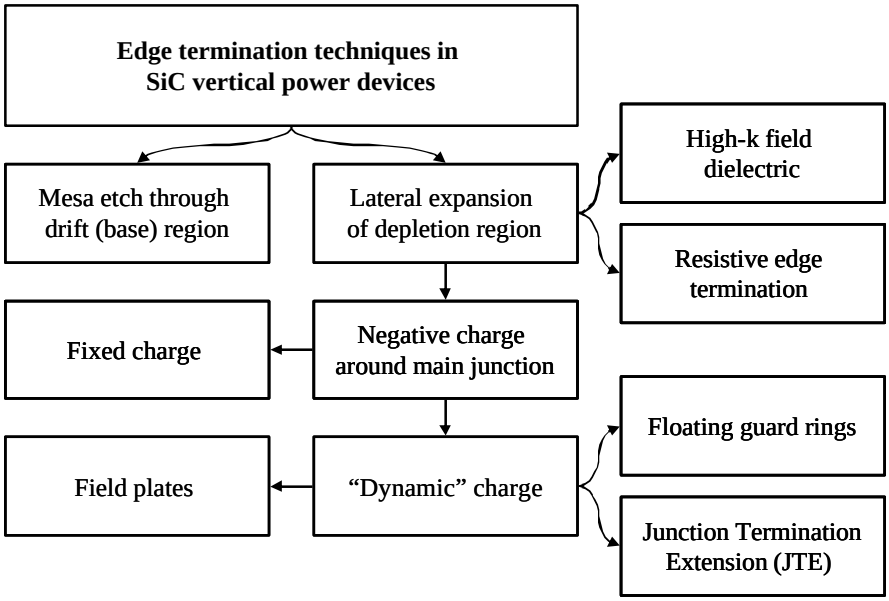

Figure 2.3: Edge termination techniques in SiC vertical power devices.

The chart in Fig. 2.3 intends to systematize various approaches and techniques used to eliminate or minimize the electric field at the edge of the main junction. The following sections provide detailed discussions of some of these techniques.

2.4 Mesa Termination

Mesa etching through the main junction and the voltage blocking layer is an elegant and theoretically the most efficient method to eliminate electric field enhancement caused by two-dimensional effects. Indeed, assuming that there is no interface charge on the mesa sidewalls, the electric field distribution in the device can be calculated using one-dimensional Poisson equation resulting in field enhancement factor k equal to unity. This technique is relatively simple from the fabrication point of view because it does not require fabrication steps that are difficult to control and expensive such as high-temperature ion implantation and post-implant annealing. Because the depletion region in mesa-terminated devices does not spread laterally at the reverse bias, this method also allows for more efficient use of area than other edge termination techniques, resulting in lower cost and higher yield.

Despite the aforementioned advantages, mesa edge termination requires careful sidewall passivation in order to minimize the interface trap density and the amount of fixed charge stored at or near the mesa sidewalls. Figure 2.4 illustrates the influence of the interface charge on the field distribution along the sidewall of a mesa-terminated 4H-SiC PiN diode at a reverse bias of 600 V.

Generally speaking, a certain amount of negative charge in the passivation layer could be beneficial, since it would further reduce the maximum electric field along the mesa sidewalls as shown in Fig. 2.4. However, in practice, the fixed charge

in the silicon dioxide used for passivation in SiC devices is usually positive. The negative charge introduced by interface traps and electrons injected into the passivation layer may cause memory effects and compromise the high-temperature performance of the device. In order to prevent an electrical discharge (so-called arcing) between the top and the bottom of the device mesa, a thick dielectric layer should be deposited. A presence of a thick dielectric film along the mesa sidewall creates another potential issue that should be paid a certain attention. It was found, that the electric field distribution along the mesa exhibits a high sensitivity to the k-value of the field dielectric. Figure 2.5 illustrates this phenomenon on the example of a surface electric field distribution along the mesa sidewalls covered with different dielectric materials. The figure presents field distribution in the device structures from Fig. 2.4 with 2-μm-thick SiO_2 and SiN_3 field dielectrics in comparison with the same structure, but without field dielectric.

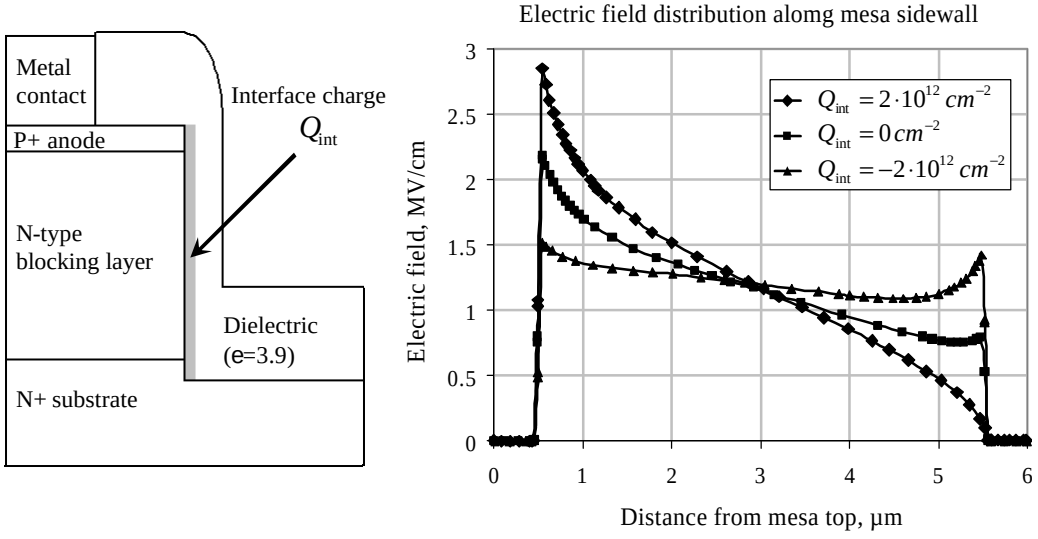

Figure 2.4: Schematic cross-section of a mesa-terminated 4H-SiC PiN diode (left) and the simulated electric field distribution along the mesa sidewall for different interface charge densities at reverse bias of 600 V (right).

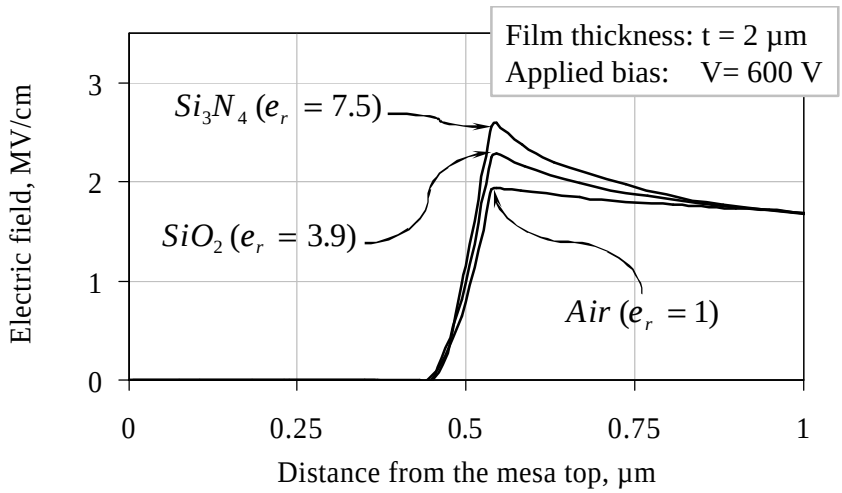

Figure 2.5: Simulated electric field distribution along the mesa sidewall for the different materials used for surface passivation at a reverse bias of 600 V.

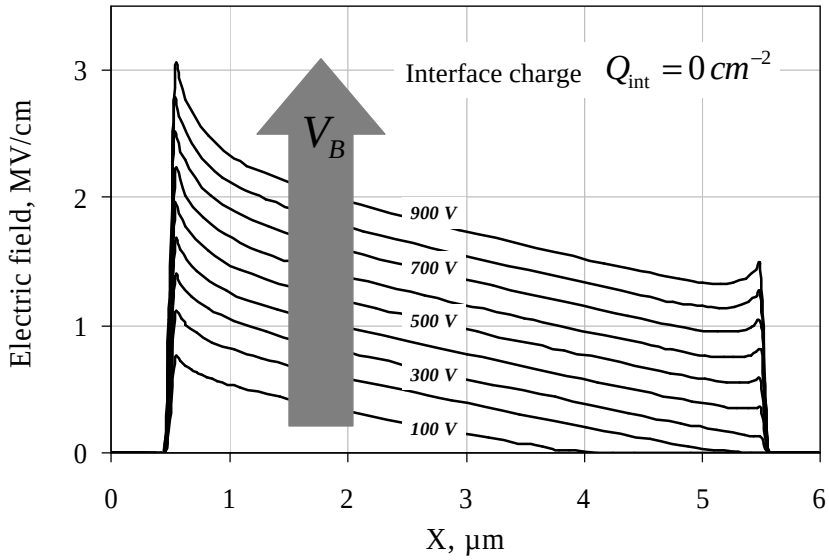

Figure 2.6: Simulated electric field distribution along the mesa surface in 4H-SiC PiN diode (Fig. 2.4) with voltage blocking layer designed for E_{1DMAX} =1.8MV/cm@V_B =600V .

As shown in Fig. 2.5, the peak electric field that occurs on the sidewall at the junction depth (~0.5 μm from the mesa top) can be significantly enlarged by the use of Si_3N_4 field dielectric with k-value of 7.5. It will be shown later, that use of high-k dielectric can be quite beneficial in order to spread electric field away from the junction in planar structures, but in mesa-terminated devices, low-k field dielectrics would be preferable.

In order to illustrate the almost one-dimensional nature of the field distribution along the mesa sidewalls, the surface electric field has been investigated as a function of the applied reverse bias. Figure 2.6 shows the field along the mesa surface at reverse voltages from 100 V to 600 V when no surface charge is present. As shown in the figure, the surface field experiences a linear increase with applied reverse bias, and the field distribution remains fairly linear along the mesa sidewall regardless of the applied bias.

The first SiC devices that employed mesa edge termination have been reported almost three decades ago [3]. Although well known from Si, mesa-termination technology was believed to be hardly used in SiC devices due to difficulties related to removing the damage caused by the etching process [4, 5]. Several groups have reported the use of the mesa edge termination in low-voltage SiC diodes [6, 7]. The results of the first (to our knowledge) successful use of this technique in high-voltage 4H- SiC PiN diodes are discussed in Chapter IV.

2.5 High-k Field Dielectric

The use of field dielectric with high dielectric constant has been developed as another edge termination technique in power SiC devices. High-k dielectric deposited

on the exposed surface of the voltage blocking layer allows to efficiently spread the depletion region laterally from the main junction. In order to investigate the influence of the dielectric constant of the field dielectric on the surface electric field distribution, a 600 V 4H-SiC Schottky barrier diode has been studied using 2-D device simulator. Figure 2.7 shows a schematic cross-section of the diode and the surface electric field distribution for field dielectrics with different k-values. Dielectric constant $k = 3.9$ corresponds to silicon dioxide that is typically used as a field dielectric in power SiC devices. As shown in Fig. 2.7, surface electric field distribution exhibits two peaks. The first peak occurs at the edge of the main device junction (Schottky contact), and the second corresponds to the outer edge of the high-k dielectric film (breaking the high-k field dielectric at some extent from the main junction is required to reliably stop electric field before the scribe line of the die).

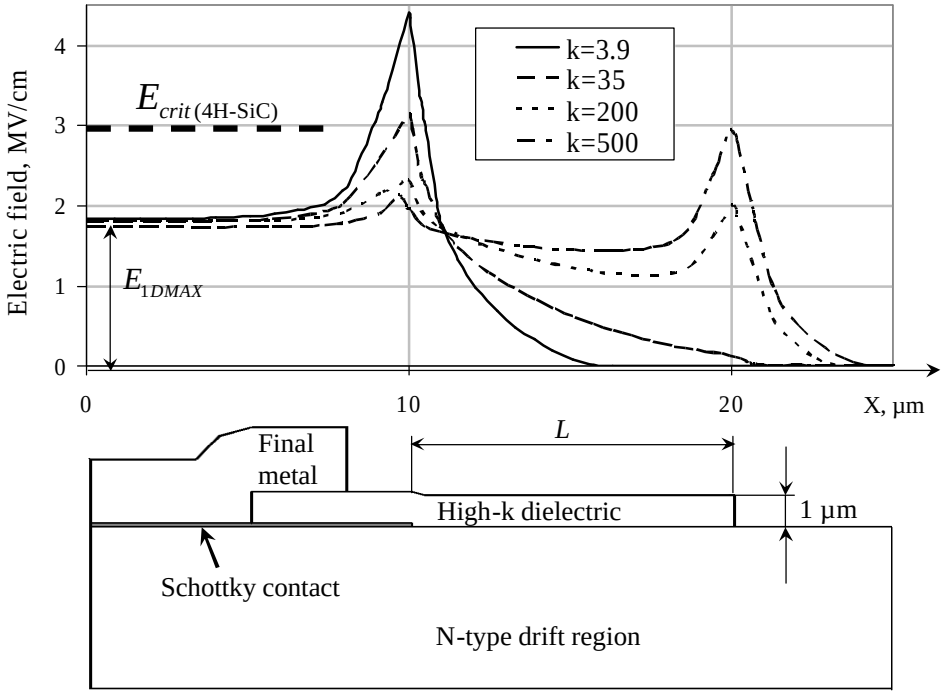

Figure 2.7: Simulated electric field distribution along the surface of the voltage blocking layer in a 4H-SiC Schottky barrier diode with high-k field dielectric at a reverse bias of 600 V.

It can be noticed from Fig. 2.7, that with increasing k-values, the first peak becomes smaller, and the second grows. Obviously, the surface electric field distribution shown in Fig. 2.7 is a complicated function of numerous parameters. The set of parameters includes the thickness and doping of voltage blocking layer; thickness, lateral extension, and k-value of field dielectric as well as applied reverse bias. It is also to be realized that the optimal surface field distribution is not necessarily the one at which two peaks are of the same magnitude. In the case of a Schottky barrier diode, for example, it is preferable to keep the peak at the Schottky contact as small as possible in order to suppress reverse leakage current caused by thermionic field emission [8].

Potential obstacles that may delay the use of this promising technique for the edge termination in commercial SiC devices are the material properties of high-k dielectrics such as their band offsets to 4H-SiC and the high-temperature stability [9]. The most promising inorganic high-k dielectric for the use in SiC power devices is HfO_2 that has the product of the relative dielectric constant and the operating field several times higher than that of SiC. This is an important property, because it allows the electric field to reach its critical value in SiC without exceeding it in the overlaying dielectric. Unfortunately, HfO_2 has a conduction band offset to 4H-SiC that is smaller by 2 eV than that of SiO_2, which makes it vulnerable to injection of hot electrons. Although the use of a thin native oxinitride layer as an electron barrier between 4H-SiC and HfO_2 resulting in low interface defect density and good insulating properties has been reported [10], the cumulative dielectric constant of $SiON/HfO_2$ stack is too small to be used for a sufficient edge termination. Polymer-

based composites for embedded capacitor applications that offer ultra-high dielectric constants (200-1000) with low loss factors (<0.02) have been recently developed [11]; however, high-temperature reliability of these dielectrics is yet to be investigated.

Another edge termination approach that laterally expands the depletion region is the introduction of electrical charge (typically negative in power devices) at or near the surface of the voltage blocking layer surrounding the main device junction. Such charge can be either fixed at the interface of SiC and dielectric, or can be applied dynamically as a function of reverse bias. These techniques are investigated in the following sections.

2.6 Fixed Charge Edge Termination

The influence of the negative fixed charge on lateral spreading of the depletion region has been investigated using a device structure similar to that used in the previous subsection. 4H-SiC Schottky barrier diode has been simulated with 1-µm SiO_2 field dielectric (e=3.9) for different amounts of fixed charge introduced at SiC/SiO_2 interface. Figure 2.8 shows a schematic cross-section of the diode and the surface electric field distribution simulated for different fixed charge densities. Similar to the case of the high-k edge termination, the surface electric field distribution exhibits two peaks. The first peak occurs at the edge of the main device junction (Schottky contact), and the second corresponds to the outer edge of the dielectric film with fixed charge (the need of breaking the field dielectric to stop electric field is the same as in the case of the high-k edge termination). With increasing the fixed charge density, the first peak lowers and the second grows.

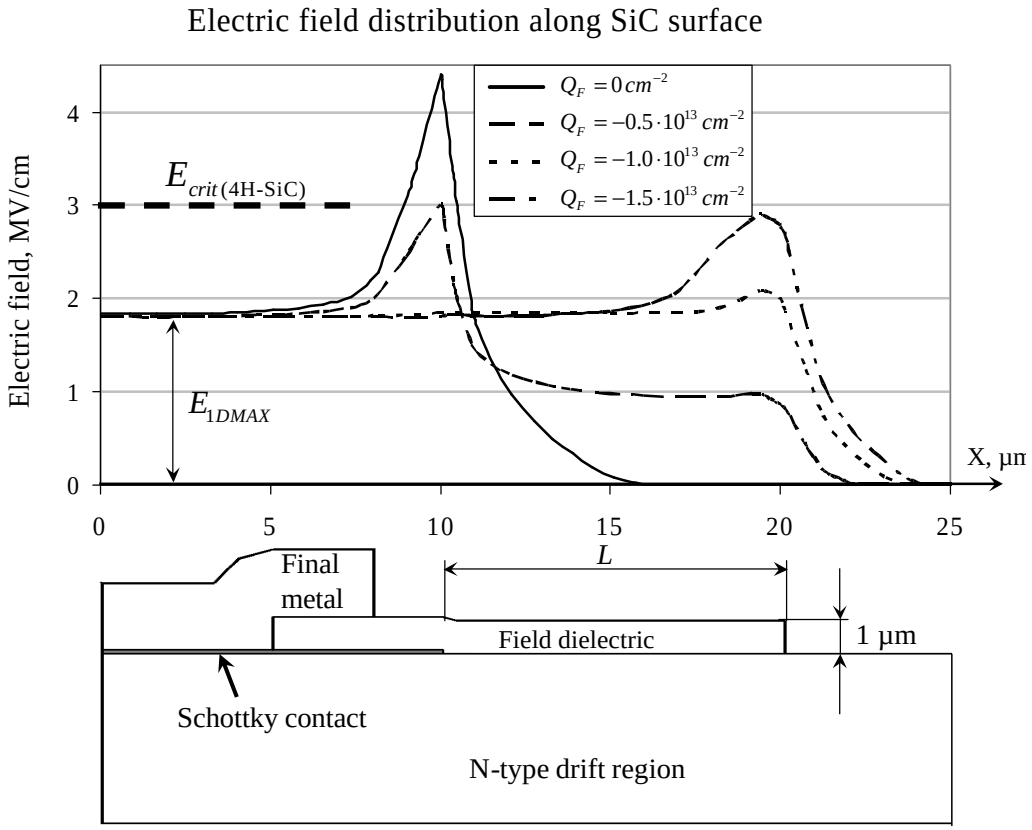

Figure 2.8: Surface electric field distribution in a 4H-SiC Schottky barrier diode with the fixed charge edge termination at a reverse bias of 600 V for different charge densities.

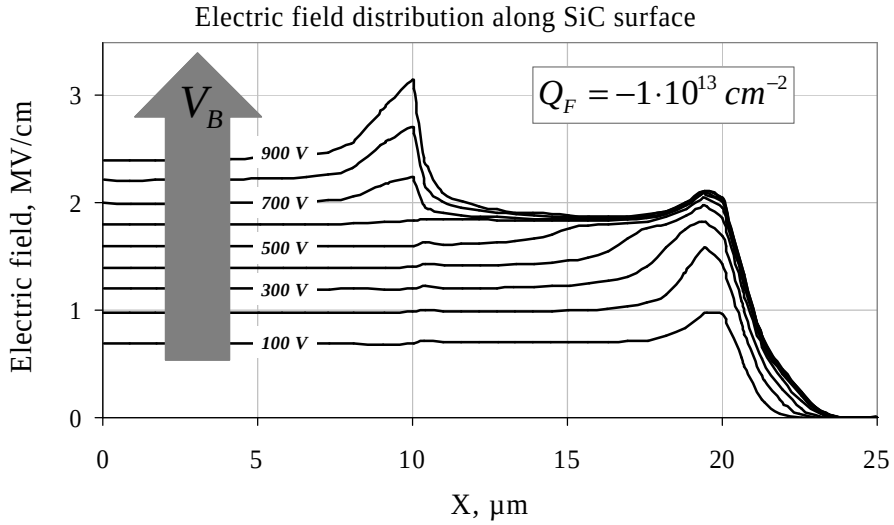

Figure 2.9: Dynamics of the surface electric field distribution in a 4H-SiC Schottky barrier diode (see Fig. 2.8) with the fixed charge edge termination and drift designed for E_{1DMAX}=1.8MV/cm@V_B=600V .

Just like the optimal k-value in the case of the high-k field dielectric edge termination, the optimal charge density in this edge termination technique is a complicated function of the thickness and doping of the voltage blocking layer; the lateral extension of the field dielectric as well as the applied reverse bias. In order to investigate the behavior of the surface electric field as a function of the applied reverse bias, the field distribution in the device structure shown in Fig. 2.8 has been simulated at reverse voltages ranging from 100 V to 600 V for a fixed value of surface charge density. Figure 2.9 shows the electric field distribution along the SiC surface for different reverse biases at a surface charge density of $Q_F = -1 \cdot 10^{13}\, cm^{-2}$. As shown in Fig. 2.9, the shape of the surface field demonstrates a significant change with applied reverse bias, when the magnitude of the first peak experiences a dramatic increase after the reverse bias exceeds 600 V. Despite its elegancy and apparent simplicity, the implementation of the fixed charge edge termination can be quite complicated. High dose (4 MRad) gamma irradiation of 4H-SiC Schottky barrier diodes using $^{60}\mathrm{Co}$ source has been demonstrated to increase the total effective charge density in the field oxide from $-1.67 \times 10^{-12} cm^{-2}$ to $-3.26 \times 10^{-12} cm^{-2}$ resulting in more than 200 V increase in breakdown voltage.

An alternative to the fixed charge edge termination is an approach described below. Instead of permanently introducing negative charge into the field dielectric, the required amount of negative charge can be produced at or near the surface of SiC dynamically with applied reverse bias. This type of charge can be either created by negatively charged ions in the depletion region or accumulated on a capacitor plate connected to one of the sides of the main junction. Several techniques such as guard

ring edge termination and junction termination extension (JTE) implement the first approach, while the second approach can be implemented by the so-called field plate edge termination. The following sections provide detailed discussions of these techniques.

2.7 Field Plate Extension

Field plate extension is a relatively simple edge termination technique in which a Metal-Insulator-Semiconductor (MIS) capacitor surrounding the main junction is produced by extending the contact metal over the field dielectric.

The depletion region induced in the semiconductor at the field dielectric under the contact metal extension laterally spreads the potential drop and reduces the electric field at the edge of the main device junction. Figure 2.10 shows a schematic cross-section of a 4H-SiC Schottky barrier diode with the simplest geometry of field plate edge termination and simulated field distributions in field dielectric and SiC surface. The drift region in the diode structure shown in Fig. 2.10 has thickness and doping parameters chosen for $E_{1DMAX} = 1.8 MV/cm$ @ $V_B = 600\,V$. As shown in Fig. 2.10, the electric fields in SiC and the field oxide exceed their critical values even at 600 V reverse bias, although the drift layer in the simulated device was kept the same as was used for the analysis of other termination techniques in previous sections.

The surface field distribution can be significantly improved with a sloped field plate. Figure 2.11 shows a comparison of the electric field distributions at the SiC surface in the devices with parallel and sloped field plates. Both devices have a drift region designed for $E_{1DMAX} = 1.8MV/cm @ V_B = 600V$. The use of the sloped field plates allows for a significant field reduction not only in SiC, but also in the field

oxide. However, despite the apparent simplicity, sloped field plate edge termination may be difficult to implement using traditional processes. Besides that, even though the electric field at the SiC surface varies in a safe range well below its critical value, the electric field in the oxide under the outer edge of the sloped field plate raises serious reliability concerns.

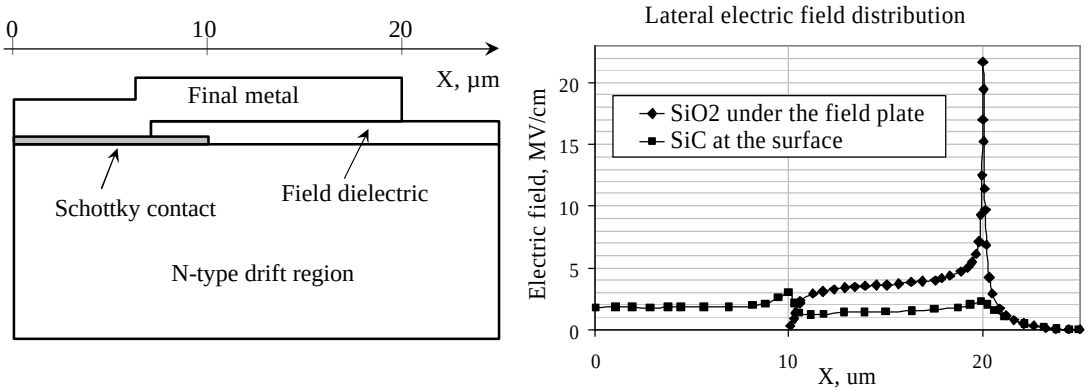

Figure 2.10: Schematic cross-section of a 4H-SiC SBD with the parallel field plate edge termination (left) and simulated field distributions in the device at 600 V (right).

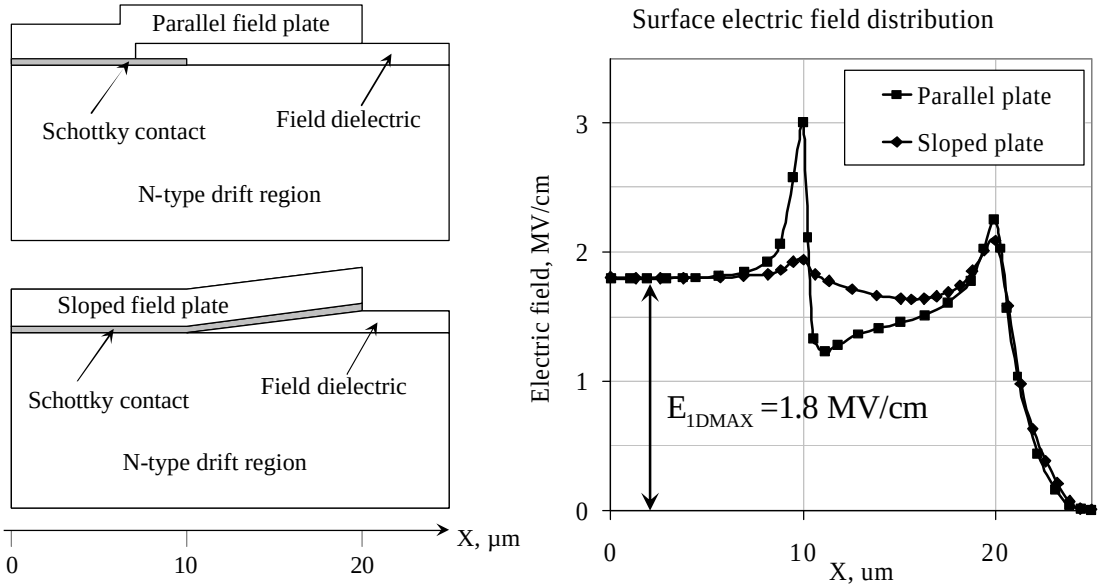

Figure 2.11: Comparison of surface electric field distribution in 4H-SiC SBDs with parallel and sloped field plates at a reverse bias of 600 V.

2.8 Floating Guard Rings

Another method that dynamically introduces negative charge along the surface of an n-type voltage blocking layer is the use of one or more floating auxiliary junctions (P-N or Schottky) surrounding the main device junction. This method of reducing the surface electric field in power semiconductor devices was first proposed four decades ago (US Patent 3,335,296) [13]. Since then, the so-called guard rings became the most widely used edge termination technique in power semiconductors.

Both the experimental and numerical investigations of this technique in SiC have been reported by several groups (*e.g.*, [14-16]). Because of the extremely low diffusion coefficients in SiC, the auxiliary P-N junctions in SiC devices are formed by selective high-dose implantation followed by high-temperature post-implantation annealing. The implantation itself should also be done at elevated temperature to avoid severe damage formation destroying the crystalline structure of the implanted layer [17]. A schematic cross-section of a SiC PiN diode with epitaxial anode and implanted guard ring edge termination is shown in Fig. 2.12. This edge termination technique does not require precise doping control in the implanted regions; however the distance between the floating P+ rings should be optimized as a function of the doping of the voltage blocking layer. Since the heavily doped guard rings form abrupt junctions with the low-doped underlying layer, the surface electric field in the guard ring terminated device experiences multiple sharp peaks. These peaks occur at the outer edges of the rings reached by the depletion region that originates at the main junction. The wider the spacing between the rings, the higher the field spikes. In order to smoothen out the surface field distribution, the distance between the rings and their

doping can be reduced. In the extreme case, the rings can be merged together in a single moderately doped region surrounding the main junction resulting in the so-called Junction Termination Extension, or JTE. The next section provides a quantitative theoretical investigation of JTE that has become the most widely used edge termination technique in SiC power electronics.

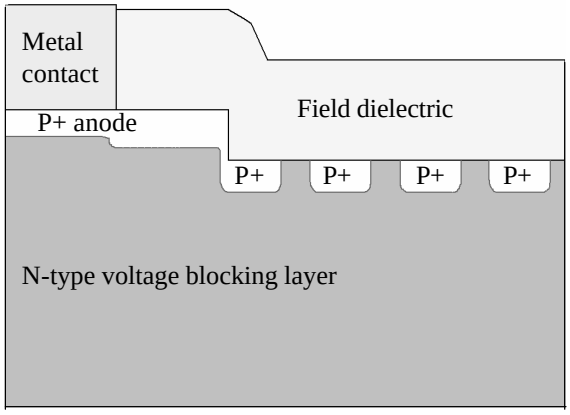

Figure 2.12: Schematic cross-section of a 4H-SiC PiN diode with heavily doped floating guard rings formed by Al ion implantation.

2.9 Junction Termination Extension (JTE)

Junction Termination Extension, or JTE, is a semiconductor region surrounding the main device junction. This region has a conductivity type opposite to that of the voltage blocking layer. In power semiconductor devices, the voltage blocking layer usually has n-type conductivity due to the fact that the mobility of electrons is higher than that of holes; therefore, the JTE region is usually made of p-type material. The mechanism of JTE performance is similar to that of the fixed charge edge termination, where fixed negative charge applied to the surface of the n-type voltage blocking layer laterally spreads the depletion region and reduces the field spike at the edge of the main junction. The major difference between these two

techniques is that in the case of JTE, the charge is built in the semiconductor region, which makes this type of edge termination much more stable and manufacturable. Fig. 2.13 shows a schematic cross-section of a 4H-SiC PiN diode with an epitaxially-grown anode layer and an implanted JTE region.

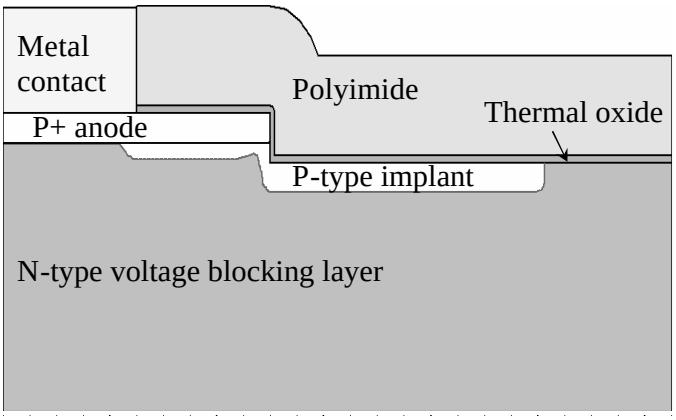

Figure 2.13: Schematic cross-section of a 4H-SiC PiN diode with an epitaxially-grown anode layer and implanted JTE region.

Figure 2.14 shows the electric field distributions in a 4H-SiC PiN diode with a base region designed for E_{1DMAX}=1.8MV/cm@V_B=600V and the total ion charge stored in the JTE region $Q_{JTE} = -1.3 \cdot 10^{13}\, cm^{-2}$. The field distribution has been simulated in the lateral plane at the junction depth of the JTE region (Fig. 2.13) where the field reaches its maximum values. Again, as in the case of the fixed charge edge termination, the field distribution exhibits two peaks. The first peak occurs at the edge of the main junction (inner edge of the JTE region), and the second peak occurs at the outer edge of the auxiliary PN junction formed by the JTE.

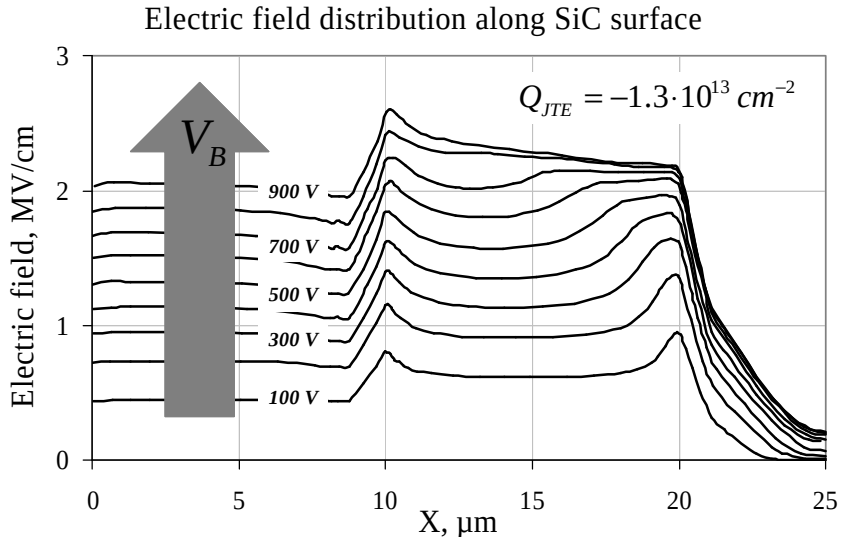

Figure 2.14: Dynamics of the surface electric field distribution in a 4H-SiC PiN diode (see Fig. 2.13) with base layer designed for E1D MAX = 1.8 MV/cm @ VB = 600 V.

Figure 2.14 also demonstrates the major difference between the mechanisms behind the JTE and the fixed charge edge terminations. In the JTE, the negative charge is built up from unit charges introduced by the individual ionized acceptor atoms in the depleted portion of the JTE region. Since the depletion width increases with the applied reverse bias, the total dose of the net negative charge located in the p-type JTE region increases dynamically. For the optimally designed JTE implantation dose, the two peaks of the electric field have the same magnitude in a wide range of reverse biases. At some point, however, the JTE region becomes fully depleted. This process first starts at the outer edge of the JTE, where the second peak occurs. Once fully depleted, the JTE region cannot produce any more charge. In the simulated device, this phenomenon starts at the reverse bias of 600 V at the outer edge of the JTE and is reflected by the shape of the field distribution shown in Fig. 2.14. At reverse biases above 600 V, the second peak stops growing, and the field

distribution becomes a straight line along the fully depleted part of the JTE region. An indirect reflection of this phenomenon is also shown in Fig. 2.15 where the maximum electric field in the bulk of a simulated device is plotted as a function of the applied reverse bias. As shown in Fig. 2.15, at reverse biases below 600V (the voltage for which the JTE dose has been designed), the maximum electric field shows a tendency to saturate. However, when the reverse bias exceeds 600 V, the maximum field in the device starts growing again, with the slope of the linear growth proportional to the maximum 1-D electric field under the main junction. Such behavior of the maximum electric field in the device bulk provides a simple optimization criterion for the optimal JTE dose using a 2-D device simulator.

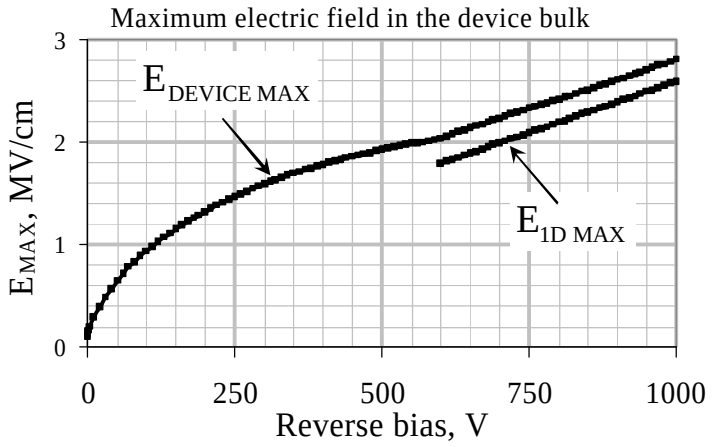

Figure 2.15: Maximum electric field $E_{DEVICE\ MAX}$ simulated in the device bulk and the maximum calculated one-dimensional electric field $E_{1D\ MAX}$ in JTE-terminated 4H-SiC PiN diode (see Fig. 2.13) as a function of reverse bias.

The performance of the JTE edge termination is highly dependent on the dose of the activated acceptor atoms in the JTE region. The difficulty to control process parameters, such as implantation and post-implant anneal schedules, or gas flow and

temperature uniformity in epitaxial reactor is not the only issue related to achieving the optimal JTE dose. Unfortunately, due to the two-dimensional nature of the problem of electric field distribution in a JTE-terminated device, a straightforward analytical solution for the optimal dose of the JTE region is not possible. Commercial two-dimensional device simulators, such as MEDICI™ or Atlas™, allow solving the problem of the optimal JTE dose as a function of the epi parameters and the targeted blocking voltage using numerical algorithms. In order to make the design efforts more efficient, however, it is important to have an accurate initial guess for the optimization task. As discussed above, the criterion for the optimal JTE dose is that the JTE region starts becoming fully depleted at a reverse bias equal to the targeted blocking voltage. Let us consider a simplified structure of a JTE-terminated Schottky barrier diode shown in Fig. 2.16.

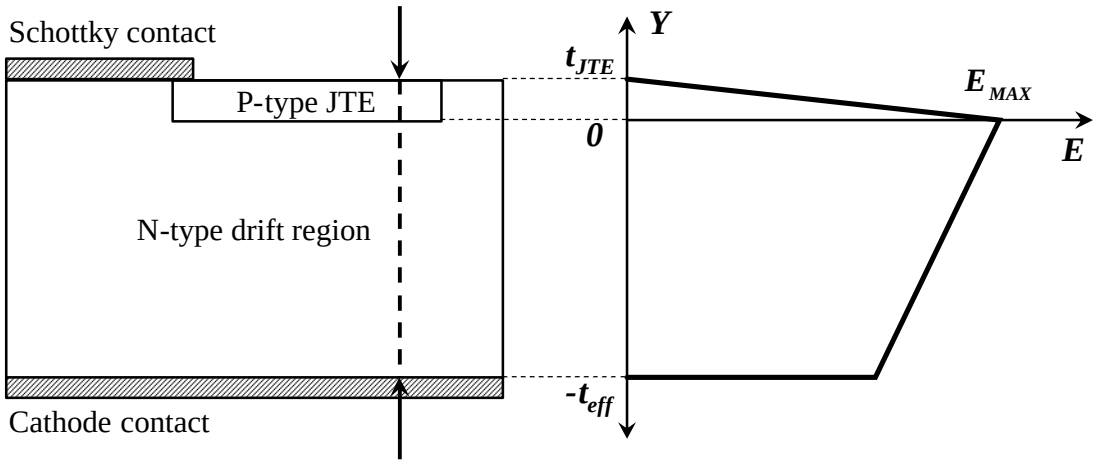

Figure 2.16: Schematic cross-section of a Schottky barrier diode (left), and the 1-D electric field distribution across the fully depleted JTE region and the drift region at the targeted blocking voltage (right).

Suppose that the active doping concentrations in a p-type JTE region and the n-type drift layer are N_{JTE} and N_{drift}, respectively. The thickness of the JTE region is

t_{JTE} and the thickness of the drift region is chosen so that the distance between the JTE junction and cathode contact is equal to t_{eff}. Let us also assume that the JTE region is wide enough so that at some distance from its outer edge two-dimensional effects can be neglected. Then, when a reverse bias equal to the targeted blocking voltage V_B is applied, the electric field distribution across the JTE region and the drift region can be found using the one-dimensional Poisson equation as shown in Fig. 2.16. For the electric field profile shown in Fig. 2.16, one can write the following equation:

$$\frac{q \cdot N_{JTE} \cdot t_{JTE}}{\varepsilon_0 \cdot \varepsilon_r} = \frac{V_B}{t_{eff}} + \frac{q \cdot N_{drift} \cdot t_{eff}}{2 \cdot \varepsilon_0 \cdot \varepsilon_r} \tag{2.9}$$

Solving equation (2.9) with respect to $D_{JTE} = N_{JTE} \cdot t_{JTE}$ gives an expression for the optimal active JTE dose as a function of the drift layer parameters and the targeted blocking voltage:

$$D_{JTE} = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot V_B}{q \cdot t_{eff}} + \frac{N_{drift} \cdot t_{eff}}{2} \tag{2.10}$$

This simple quasi-empirical expression provides a sufficiently accurate initial guess for the numerical optimization of the JTE dose using a 2-D device simulator. The lateral extension of JTE region L_{JTE} is not a critical parameter as long as it exceeds the thickness of the drift region.

When combining the expression for the JTE dose (2.10) with optimal drift parameters from (2.5), we may put together a set of the design rules for the JTE-terminated device structure that has a drift region with no conductivity modulation:

$$\begin{cases} t_{drift} = \dfrac{3}{2} \cdot \dfrac{V_B}{E_{\max}} + t_{JTE} \\ N_{drift} = \dfrac{4}{3} \cdot \dfrac{\varepsilon_r \cdot \varepsilon_0 \cdot E_{\max}^2}{q \cdot V_B} \\ D_{jte} = \dfrac{\varepsilon_r \cdot \varepsilon_0 \cdot E_{\max}}{q} = \dfrac{3}{2} \cdot N_{drift} \cdot \left(t_{drift} - t_{JTE} \right) \\ L_{JTE} \geq t_{drift} \end{cases} \tag{2.11}$$

In order to numerically validate the design rules given by (2.11), a 600 V JTE-terminated Schottky barrier diode structure shown in Fig. 2.16 has been simulated using 2-D device simulator for $E_{\max}$ of 1.8 MV/cm. Figure 2.17 shows the electric field distribution at the surface and at the JTE-drift junction depth in the simulated device. The set of design rules (2.11) has been numerically evaluated for different targeted V_B and $E_{\max}$, always resulting in the optimal field distribution that does not require further optimization with 2-D device simulator.

2.10 Resistive Edge Termination

Resistive edge termination in SiC power devices has been investigated by several groups [14, 18-21]. The reported techniques implementing this method include resistive Schottky barrier field plate [14], damage of SiC surface with high dose argon [18] or boron [19] ion implantation, and vanadium implantation [20]. Despite the encouraging early results, the resent studies on implanted resistive edge terminations revealed high-voltage pulse instabilities that limit the safe-operating-area (SOA) of SiC devices fabricated using this type of edge termination [21].

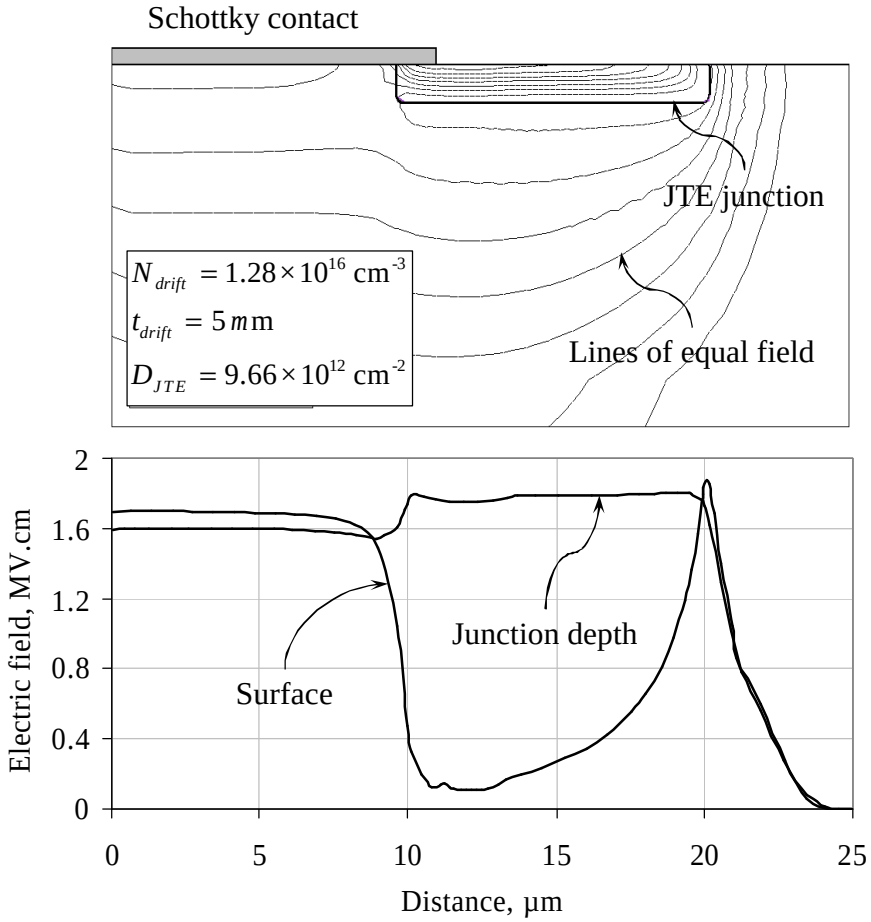

Figure 2.17: Electric field distribution in a 4H-SiC SBD with structural and doping parameters chosen using design rules (2.11) simulated at reverse bias of 600 V.

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CHAPTER III

THEORETICAL STUDY OF FIELD COMPENSATION TECHNIQUES

3.1 Introduction

The idea of electric field reduction along the junction formed by two semiconductor regions with the opposite type of conductivity (RESURF or compensation principle) has been employed in the power semiconductor industry for many years [1, 2]. Silicon LDMOS transistors that can be monolithically integrated with the control circuitry or matching network are used in a wide spectrum of power switching and RF applications (*e.g.*, [1]). Implementing the compensation principle in vertical power Si MOSFETs has allowed for a dramatic five-fold reduction in the on-state resistance and has broken the limits predicted for Si power MOSFETs [2]. In the commercially available power vertical Si MOSFETs (CoolMOS™), the plurality of vertical auxiliary junctions is defined by a series of ion-implantation and epitaxial regrowth steps. This results in the so-called super-junction. Unfortunately, vertical SiC super-junction power devices implementing the field compensation principle as it is done in Si CoolMOS™ transistors may not be practical because of the high cost of the high-temperature implantation and epitaxial growth. However, the lateral power transistors that implement field compensation can be built in SiC on both semi-insulating and conducting substrates. The SiC LDMOS transistor that has been

considered as the key building block of the future SiC Smart Power electronics was first demonstrated on a semi-insulating substrate in 1997 [3], and since then it has attracted enormous attention of researchers and engineers.

In spite of such a popularity of the field compensation technique, the analytical model for the optimal design of a field compensated devices is still a hot topic for discussion. Multiple models, both one- and two-dimensional, have been proposed in recent years showing rather inconsistent results sometimes [4-8]. Unfortunately, so far, a two-dimensional device simulator remains the ultimate tool for the optimal design of super-junction devices. In this chapter, a simple set of rules for the optimal design of super-junction power devices is developed. The analytical expressions for the optimal dopings and dimensions of the devices implementing the field compensation principle are derived and validated with the results of numerical simulations that are also presented. Numerical analysis of SiC diode structures used in this chapter was confined to solving 2-D Poisson equations under the steady state reverse bias conditions assuming that no carrier transport or generation-recombination phenomena. All acceptors and donors were assumed ionized and no deep levels were introduced into the simulated device structures.

3.2 Basic Understanding of Field Compensation Principle

Let us consider two idealized 1-D bipolar diodes with the base layers of different conductivity and equal doping concentration shown in Fig. 3.1 (a). Assuming abrupt p-n junctions, the distribution of the lateral electric field in such diodes has a triangular shape because it is defined by the doping concentration in the base regions and can be described by Poisson equation. However, when such diodes

are merged together as shown in Fig. 3.1 (b), the electric field distribution along the auxiliary junction formed by their base region does not depend on the doping concentration any more and becomes flat. The fact that the electric field distribution does not depend on the doping concentration of the individual diodes results in a dramatic increase of voltage blocking capability of the layer for the same on-state resistance. Obviously, the field compensation at the outer surfaces of the low doped layers of the composite diode would not be as effective as at their junction and is limited by the dielectric permittivity of a semiconductor. In SiC ($e \approx 9.7$), the thickness of the layers can be in the order of 1 μm without causing significant distortion of the lateral electric field on the surface.

As discussed earlier, the fabrication of the *vertical* SiC devices implementing the field compensation could be quite problematic. However, the *lateral* SiC super-junction devices can be fabricated even at the present state of technology. Although Fig. 3.1 illustrates the field compensation principle with the example of a bipolar diode, the same principle can also be implemented in various device structures without conductivity modulation in the voltage blocking layer. Potentially, the RESURF principle could be implemented in all kinds of the SiC power lateral devices, including bipolar and unipolar diodes, field-effect transistors, BJTs, IGBTs, thyristors, etc.

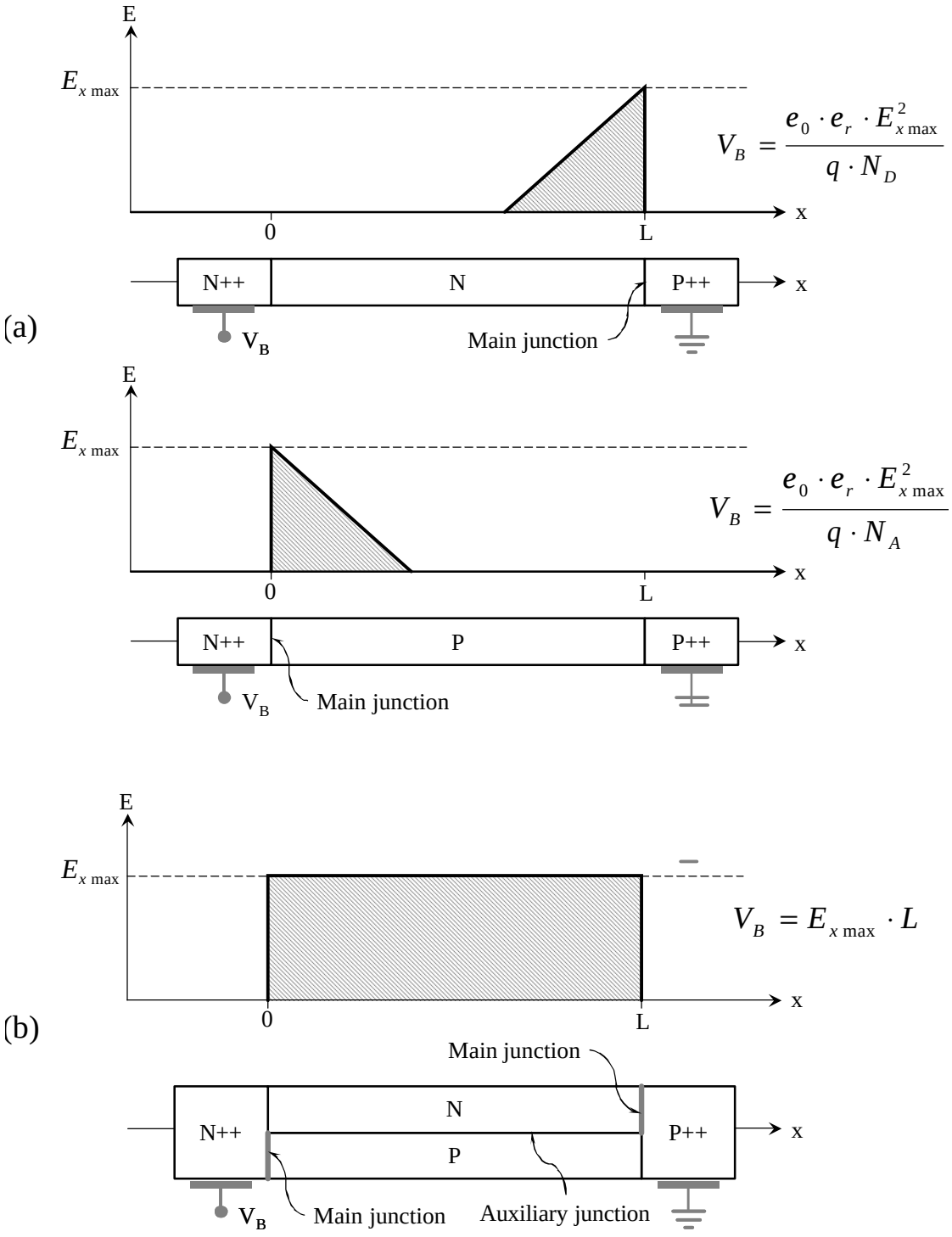


Figure 3.1: (a) Lateral field distribution in 1-D $p^+ - n - n^+$ and $p^+ - p - n^+$ diodes, and (b) in a composite bipolar diode formed by the combination these two structures.

3.3 Development of the Design Rules for Field Compensated Structures

The intuition suggests that implementing the field compensation principle can allow for a significant reduction in the on-resistance in the devices with both types of voltage blocking layer: with or without conductivity modulation. However, let us narrow the topic to the latter type (*i.e.*, to the devices with the drift region). In order to take full advantage of the field compensation, both structural and doping parameters of a super-junction structure should be optimized. In order to simplify the discussion, let us imagine a hypothetical super-junction structure shown in Fig. 3.1 (b) where the current conduction occurs only through the n-type region and is caused only by the drift of majority carriers (electrons). In the further discussion this n-type region will be denoted as a "drift region" or "drift," and the p-type region will be referred to as an "auxiliary" region. Let us also assume that the voltage drop V_B applied to the n-type drift region makes it fully depleted, resulting in a box field profile along the x-axis as shown in Fig. 3.1 (b). Then the maximum lateral electric field that occurs in the drift region of the length L can be expressed as follows:

$$E_x = \frac{V_B}{L} \tag{2.12}$$

Let us consider the case when the drift and auxiliary regions have the same thicknesses and doping concentrations. Since the drift region is fully depleted, the normal to the auxiliary junction component of the electric field produced by the cumulative charge of the ionized atoms is

$$E_y = \frac{q \cdot D}{e_r \cdot e_0}, \tag{2.13}$$

where D is the charge dose stored in the depleted drift region is given by

$$D = N \cdot t \tag{2.14}$$

In (2.14), N and t are the doping concentration and the thickness of the drift region, respectively. The resulting total maximum electric field in the device can be then derived from (2.12)and (2.13) as follows:

$$E^2 = E_x^2 + E_y^2 = \left(\frac{V_B}{L}\right)^2 + \left(\frac{q \cdot D}{e_r \cdot e_0}\right)^2 \tag{2.15}$$

Then the resistance of the drift region normalized in the third dimension ($\Omega \cdot cm$) is given by

$$R_{drift} = \frac{L}{q \cdot m \cdot D} \tag{2.16}$$

where m is electron mobility, which is a function of the concentration and the temperature. The optimal length and dose of the drift region that minimize its resistance for a targeted blocking voltage V_B and the maximum allowed electric field $E = E_{\max}$ could be found as follows.

First, the expression for L can be written from (2.15) as follows:

$$L = \frac{V_B}{\sqrt{E_{\max}^2 - \left(\frac{q \cdot D}{e_r \cdot e_0}\right)^2}} \tag{2.17}$$

Plugging (2.17) into (2.16) yields the following expression for the drift resistance:

$$R_{drift} = \frac{V_B}{q \cdot m \cdot D \cdot \sqrt{E_{\max}^2 - \left(\frac{q \cdot D}{e_r \cdot e_0}\right)^2}} \tag{2.18}$$

Assuming $m = const$ for a given temperature and a narrow doping range, we then solve $\frac{dR_{drift}}{dD} = 0$ with respect to D, which returns the optimal value for the dose in the drift region:

$$D_{opt} = \frac{1}{\sqrt{2}} \cdot \frac{e_r \cdot e_0 \cdot E_{\max}}{q} \tag{2.19}$$

This is an interesting result, because, that the optimal dose of the drift region D_{opt} does not depend on the targeted blocking voltage, as indicated in (2.19). Another interesting thing that can be noticed from (2.19) and (2.13), is the fact that in the optimal configuration, $E_y = E_{\max} / \sqrt{2}$ along the interface of the semiconductor regions. In other words, for achieving the minimal drift resistance, the normal and lateral components of the electric field should be equal along the auxiliary junction:

$$E_{xopt} = E_{yopt} \tag{2.20}$$

Plugging (2.19) into (2.17) results in the optimal length of the drift region:

$$L_{opt} = \sqrt{2} \cdot \frac{V_B}{E_{\max}} \tag{2.21}$$

Plugging (2.19) and (2.21) into (2.18) returns the minimum drift resistance as shown below:

$$R_{drift\min} = 2 \cdot \frac{V_B}{m \cdot e_r \cdot e_0 \cdot E_{\max}^2} \tag{2.22}$$

Comparing (2.22) with the minimum resistance of the drift region in the traditional vertical devices given by (2.6), it can be noticed, that the resistance of a properly designed drift region with field compensation exhibits much softer dependence on the targeted blocking voltage and the maximum allowed electric field.

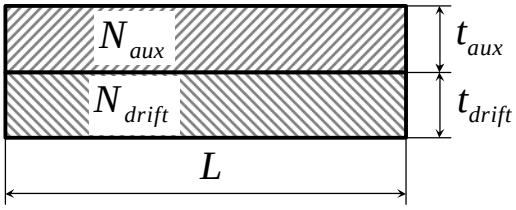


Figure 3.2: Schematic cross-section of a field compensated structure with a single auxiliary junction.

Rewriting (2.19) and (2.22) in terms of N and t, we may put together a simple set of design rules for the field compensated structure with a single auxiliary junction shown in Fig. 3.2.

$$\begin{cases} t_{drift} = t_{aux} = t \\ N_{drift} = N_{aux} = \dfrac{1}{\sqrt{2} \cdot t} \cdot \dfrac{e_r \cdot e_0 \cdot E_{\max}}{q} \\ L_{opt} = \sqrt{2} \cdot \dfrac{V_B}{E_{\max}} \end{cases} \tag{2.23}$$

The set of design rules (2.23) was derived using a simplified hypothetical device structure. In order to validate the formulas given by (2.23), let us now design a practical device that uses a field compensated drift region with a single auxiliary junction, and can be implemented in 4H-SiC using existing processing technology. A power normally-off LDMOS built on p-type epitaxial layer grown on semi-insulating substrate can serve as an example of such a structure. A schematic cross-section of this device is shown in Fig. 3.3. As shown in Fig. 3.3, the source and drain ohmic contacts are formed on heavily doped n-type regions formed by ion implantation. Heavily doped p-type region is also formed with ion implantation to provide a p-type body contact. The third implantation step is used to define a lateral drift region.

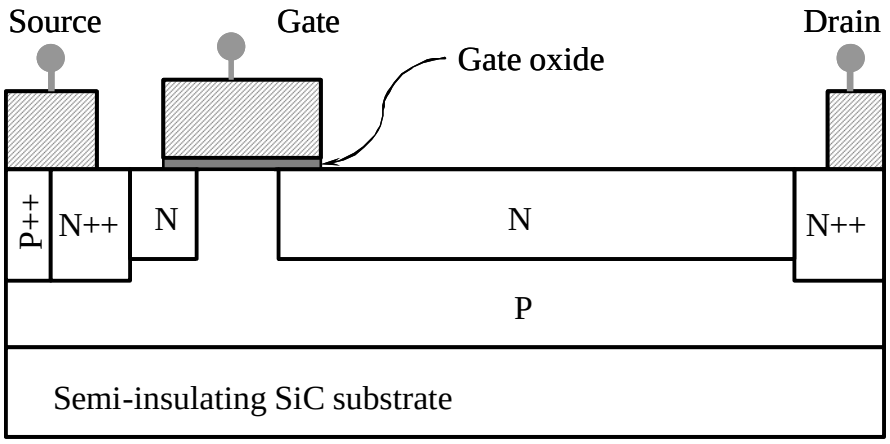


Figure 3.3: A schematic cross-section of a lateral triple-implanted 4H-SiC MOSFET.

The device shown in Fig. 3.3 has three main junctions that can potentially cause device breakdown:

1. Base-to-drain p-n junction;
2. Gate-to-drift metal-oxide-semiconductor junction;
3. Gate-to-source metal-oxide-semiconductor junction;

The breakdown of the third junction can occur only in on-state conditions due to the failure of the gate oxide, while the first two junctions may cause device breakdown under high-bias off-state conditions.

Suppose, that given a targeted blocking voltage V_B=1800 V, we need to determine the optimal structural and doping parameters in order to minimize the drift resistance. First, let us define the set of the design parameters. As discussed above, under the high-bias off-state conditions, the main action in the considered device occurs between the gate-to-drift and base-to-drain junctions. This provides the first design parameter – the distance L between the gate contact and n^+ drain region or the length of the drift region which can be found from (2.23). The optimal doping of the drift region that depends on its thickness and the maximum allowed electrical field

can also be determined using (2.23). Since this study is done for the purpose of demonstration, the value of the maximum allowed field in SiC could be chosen in the range between 1.5 MV/cm and 2 MV/cm. Suppose that the drift region is formed by multi-energy ion implantation resulted in a box profile with the depth of 0.25 μm. Then the optimal values of the doping concentration and the length of the designed drift region can be calculated from (2.23) . In Fig. 3.4, these values are plotted as functions of the maximum electric field for the targeted blocking voltage of 1800 V. From Fig. 3.4, choosing the maximum field $E_{\max}$ to be 1.7 MV/cm, the optimal length of the drift region L_{opt} is 15 μm, and the corresponding drift doping concentration is equal to 2.62×10^{17} cm^{-3}. Since the this value also corresponds to the doping of the base region, this raises a serious concern about the threshold voltage.

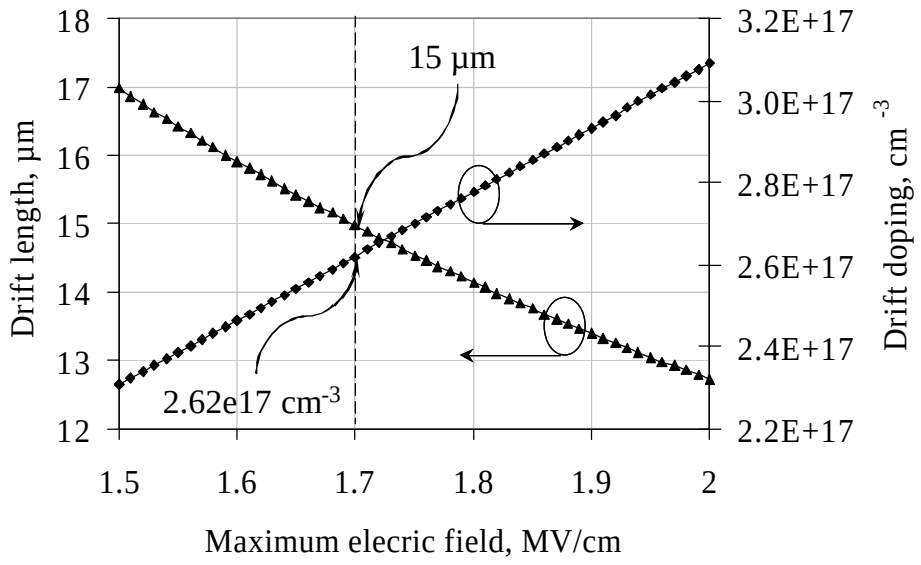


Figure 3.4: Optimal parameters of the drift region calculated for V_B of 1800 V using design rules (2.23) for $E_{\max}$ ranging from 1.5 MV/cm to 2 MV/cm.

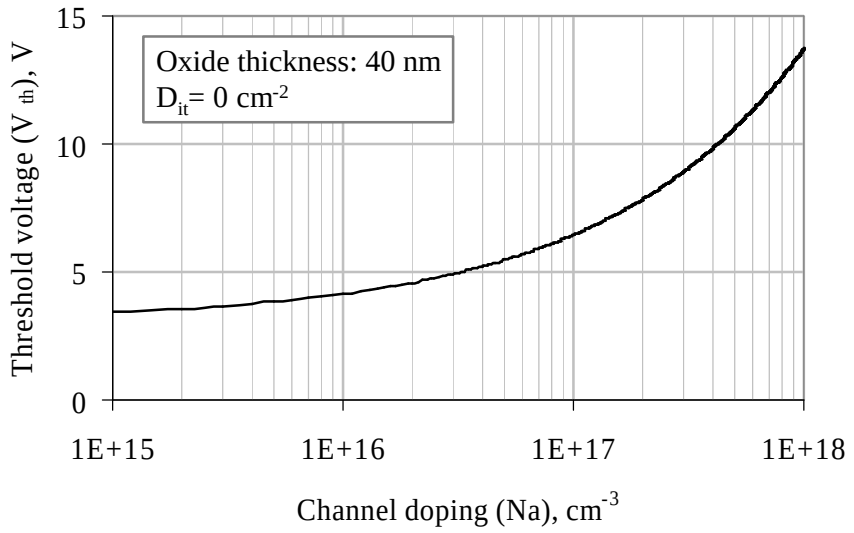
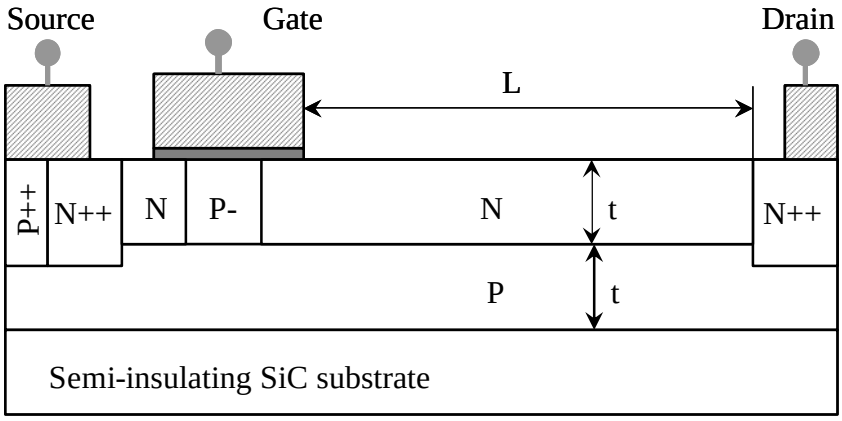


Figure 3.5: Ideal threshold voltage of a 4H-SiC MOSFET with the gate oxide of 40 nm assuming zero effective interface charge density.

Figure 3.5 shows the dependence of the ideal threshold voltage of a 4H-SiC MOSFET for the gate oxide thickness t_{OX} of 40 nm assuming zero interface charge density. As shown here, the channel acceptor concentration of 2.6×10^{17} cm^{-3} results in the threshold voltage V_{TH} of 8.5 V. The problem of a high threshold voltage, however, can be easily corrected by introducing one more p-type epitaxial layer with lower acceptor concentration. A schematic cross-section of the resulting triple-implanted lateral 4H-SiC MOSFET structure is shown in Fig. 3.6. This figure also provides the thickness and doping parameters calculated for this device using (2.23). The device structure shown in Fig. 3.6 has been simulated using Silvaco Atlas™ 2-D device simulation software. The on-state conduction was simulated assuming zero effective interface charge density, and the effective channel mobility adjusted to about 20 cm^2/(V·sec), which is the typical value for the 4H-SiC MOSFETs.



P++	: $1x10^{19}$ cm^{-3}
N++	: $1x10^{19}$ cm^{-3}
P	: $2.62x10^{17}$ cm^{-3}
N	: $2.62x10^{17}$ cm^{-3}
P-	: $1x10^{16}$ cm^{-3}
L	: 15 µm
T	: 0.25 µm

Figure 3.6: Simulated device structure with the optimal drift and base parameters.

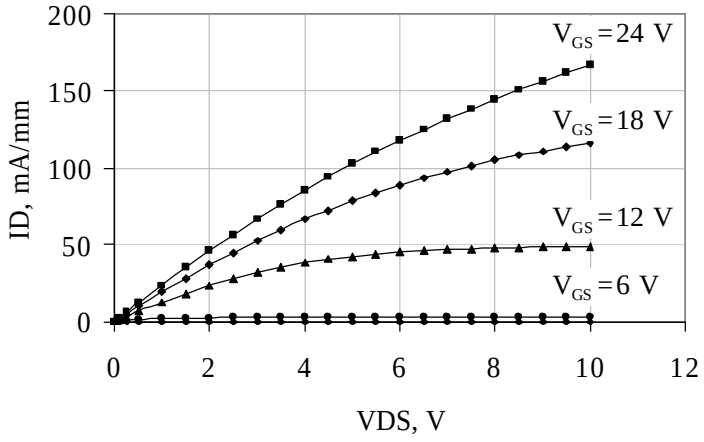


Figure 3.7: Simulated family of curves for zero interface charge and effective channel mobility adjusted to ~20 $cm^2/(V?sec)$.

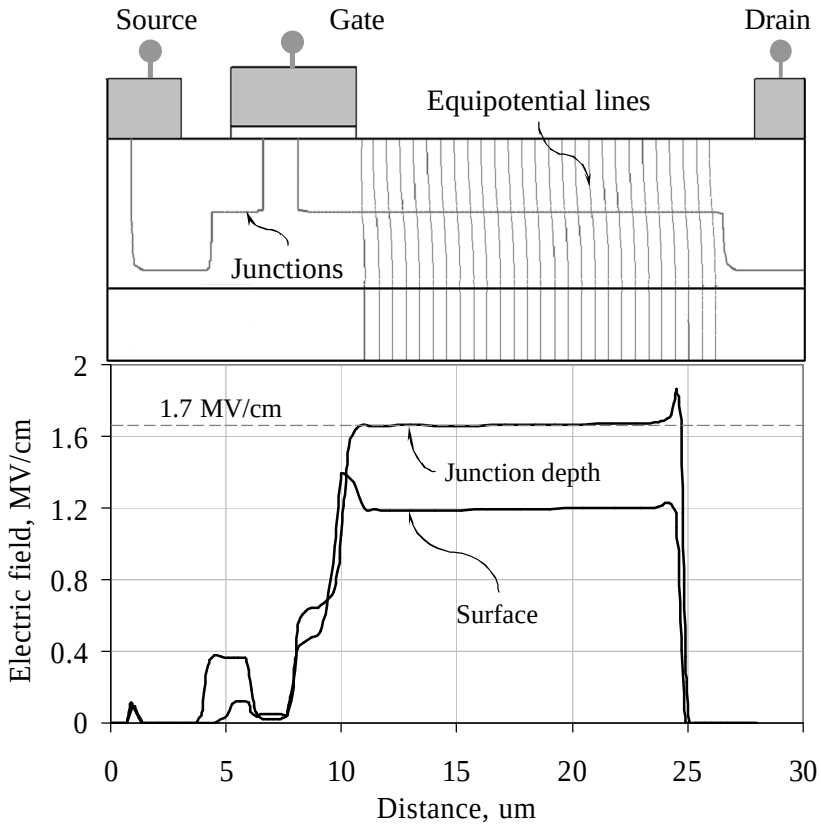


Figure 3.8: Simulated distribution of the electrostatic potential in the device bulk (top) and the electric field distribution at the junction depth and at the surface (bottom) in a field compensated 4H-SiC LDMOS with a single auxiliary junction at V_B=1800 V.

Fig. 3.7 shows a family of curves with the gate-to-source voltages ranging from 0 V to 24 V with the step of 6V. Fig. 3.8 shows the simulated distribution of the electrostatic potential in the device bulk and the electric field distribution at the junction depth and at the surface at the targeted blocking voltage V_B equal of 1800 V. As shown in the Fig. 3.8, the electric field simulated at the junction depth, exhibits almost flat profile with an average of 1.7 MV/cm, which is equal to the targeted maximum electric field. The average value of the surface electric field is equal to 1.2 MV/cm. Since the normal electric field at the surface should be equal to zero, the

simulated surface field has only its lateral component. It is easy to check that the simulated $E_{surf} = E_x$ is equal to $E_{\max} / \sqrt{2}$, which perfectly satisfies the condition in (2.20). The obtained simulation results shown in Fig. 3.8 clearly demonstrate the correctness of the analytically derived design rules in (2.23) used for the optimal choice of the parameters of the simulated device structure.

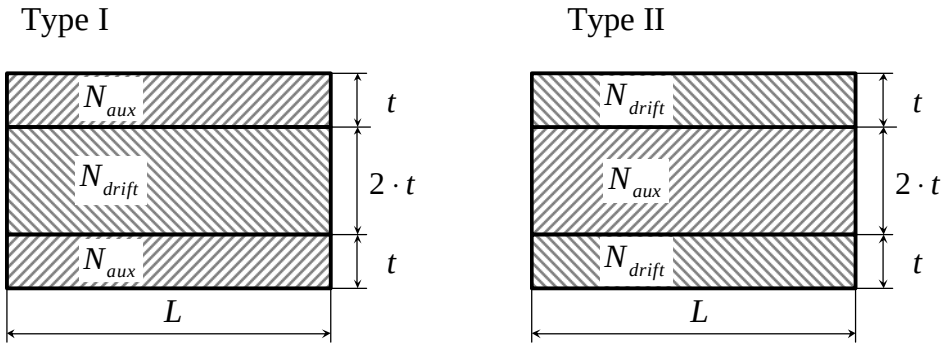
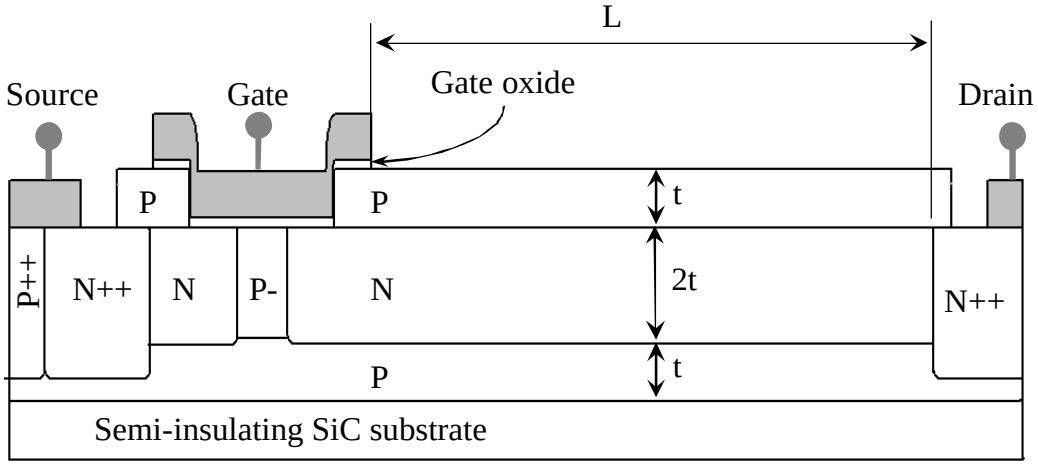


Figure 3.9: Field compensated structures with two auxiliary junctions.

As discussed earlier, in the field compensated structure with a single auxiliary junction shown in Fig. 3.2, the normal component of the electric field at the outer sides of the regions is equal to zero. This means that if two structures shown in Fig. 3.2 merge together in such a way that the resulting stack has two parallel p-n junctions, the maximum electric field in the resulting "sandwich" will stay unchanged. Figure 3.9 shows the two possible ways of such stacking. It can be noticed that in both cases the dose of the drift region is doubled, which means that the resistance is reduced by a factor of 2. The set of the design rules for the field compensated structures with two auxiliary junctions can be expressed as follows:

$$Type\ I: \begin{cases} t_{drift} = 2 \cdot t \\ t_{aux} = t \\ N_{drift} = N_{aux} = \dfrac{1}{\sqrt{2} \cdot t} \cdot \dfrac{e_r \cdot e_0 \cdot E_{\max}}{q} \\ L_{opt} = \sqrt{2} \cdot \dfrac{V_B}{E_{\max}} \end{cases} \quad (2.24)$$

$$Type\ II: \begin{cases} t_{drift} = t \\ t_{aux} = 2 \cdot t \\ N_{drift} = N_{aux} = \dfrac{1}{\sqrt{2} \cdot t} \cdot \dfrac{e_r \cdot e_0 \cdot E_{\max}}{q} \\ L_{opt} = \sqrt{2} \cdot \dfrac{V_B}{E_{\max}} \end{cases} \quad (2.25)$$



P++	: $1x10^{19}$ cm^{-3}
N++	: $1x10^{19}$ cm^{-3}
P	: $2.62x10^{17}$ cm^{-3}
N	: $2.62x10^{17}$ cm^{-3}
P-	: $1x10^{16}$ cm^{-3}
L	: 15 µm
t	: 0.25 µm

Figure 3.10: 4H-SiC LDMOS with a field compensated drift structure with two auxiliary junctions.

Although the resistance of the drift region in both cases (2.24) and (2.25) is the same and is given by

$$R_{drift} = \frac{V_B}{m \cdot e_r \cdot e_0 \cdot E_{\max}^2}, \qquad (2.26)$$

for a particular application, one of the “sandwich” structures may be more preferable than the other. For example, in 4H-SiC LDMOS structure discussed earlier, only the Type I field compensated structure can be implemented. Figure 3.10 shows a 4H-SiC LDMOS with a field compensated drift structure with two auxiliary junctions. The optimal structural and doping parameters determined by (2.24) are taken unchanged from Fig. 3.6 with the exception made only for the drift thickness that in this structure is equal to 0.5 μm.

It might be noticed, that the introduction of the epitaxially grown second auxiliary region in a triple-implanted structure would not significantly complicate the fabrication process. Moreover, the high-temperature activation annealing step can be eliminated, because it will be done during the epitaxial growth of the second layer.

Fig. 3.11 shows the simulation result on the structure of Fig. 3.10 done for the electrostatic potential in the device bulk (the top), and the bottom part of the figure shows the distribution of the electric field at the auxiliary junctions and at the surface. Again, just like in the case with a single auxiliary junction, the electric field exhibits almost flat profile with the average magnitude of 1.7 MV/cm at both junctions, and the average magnitude of the surface electric field is equal to 1.2 MV/cm. These values perfectly match the targeted electric field distribution. The highest electric field (2.2 MV/cm) occurs in the device bulk far from the gate oxide and does not compromise its reliability. Simulation results on SiC LDMOSFET structures have

confirmed the correctness of the analytically derived design rules for the field compensated structures. Although these devices were designed for the same value of doping in the drift and auxiliary region(s), the use of different doping concentration is also possible. It was found that the condition for the field compensation along the auxiliary junction is the equity of the doses in the drift and auxiliary region(s). The design rules rewritten in terms of the doses are summarized in Table 3.1.

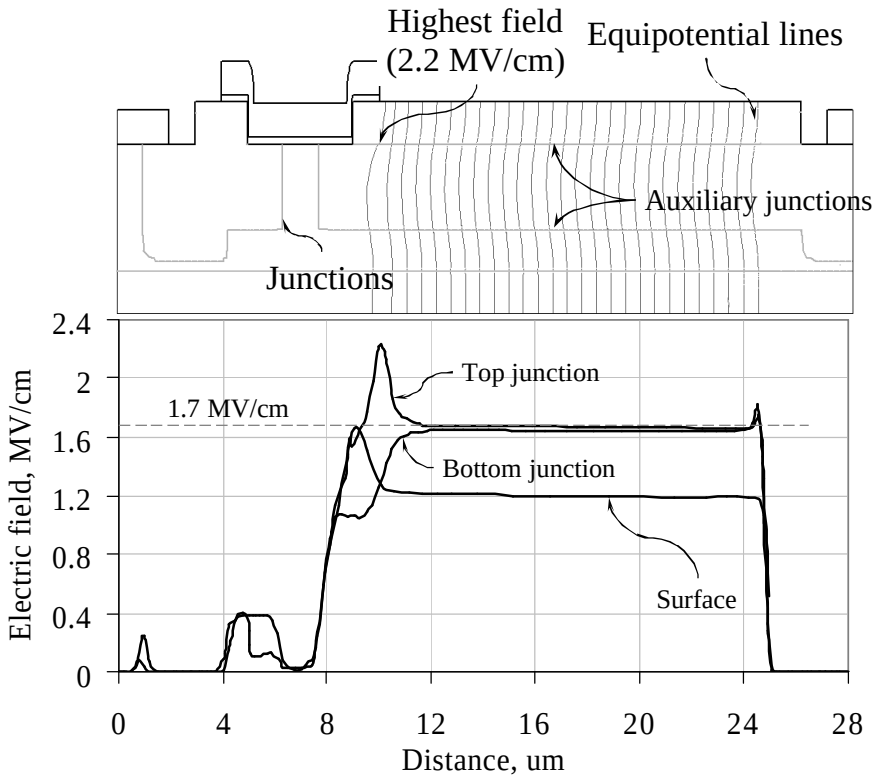
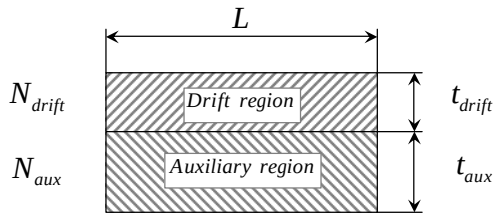


Figure 3.11: Simulated distribution of the electrostatic potential in the device bulk (top) and the electric field distribution at the junctions and at the surface (bottom) in a field compensated 4H-SiC LDMOS with two auxiliary junctions at V_B=1800 V.

Table 3.1: Design rules for lateral field compensated structures.

Structure with one auxiliary region



$$D_{drift} = D_{aux}$$

$$\left(N_{drift} \cdot t_{drift} = N_{aux} \cdot t_{aux}\right)$$

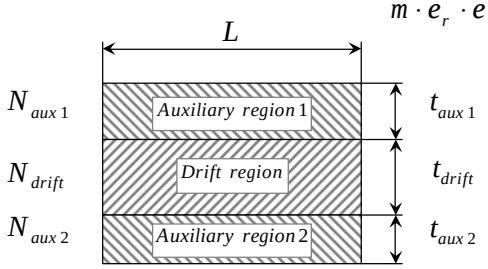
$$R = \frac{2 \cdot V_B}{m \cdot e_r \cdot e_0 \cdot E_{\max}^2} \quad [\Omega \cdot \mathrm{cm}]$$

$$L_{opt} = \sqrt{2} \cdot \frac{V_B}{E_{\max}}$$

$$D_{opt} = \frac{1}{\sqrt{2}} \cdot \frac{e_r \cdot e_0 \cdot E_{\max}}{q}$$

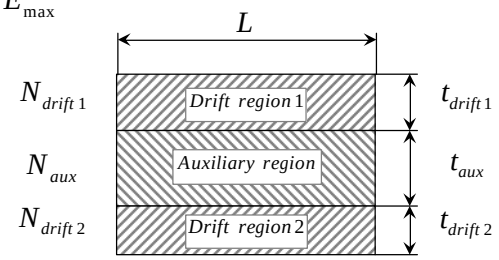
Structures with the reduced normal field (sandwich)

$$R = \frac{V_B}{m \cdot e_r \cdot e_0 \cdot E_{\max}^2} \quad [\Omega \cdot \mathrm{cm}]$$



$$D_{drift} = D_{aux\,1} + D_{aux\,2}$$

$$\left(N_{drift} \cdot t_{drift} = N_{aux\,1} \cdot t_{aux\,1} + N_{aux\,2} \cdot t_{aux\,2}\right)$$



$$D_{drift} = D_{drift\,1} + D_{drift\,2} = D_{aux}$$

$$\left(N_{drift\,1} \cdot t_{drift\,1} + N_{drift\,2} \cdot t_{drift\,2} = N_{aux} \cdot t_{aux}\right)$$

$$L_{opt} = \sqrt{2} \cdot \frac{V_B}{E_{\max}}$$

$$D_{opt} = \sqrt{2} \cdot \frac{e_r \cdot e_0 \cdot E_{\max}}{q}$$

3.4 Compensated Structures with Unequal Doses

In addition to auxiliary junctions, every field compensated structure has two main junctions. Sometimes, one of the main junctions may be less vulnerable to the high electric field than the other. The lateral MOSFET structure discussed above provides a good example. Unfortunately, in silicon carbide MOSFETs, one cannot take the full advantage of the superior breakdown strength of SiC because of the reliability issues caused by the gate oxide. The breakdown strength of SiO_2 has been measured to be above 10 MV/cm. However, in order to ensure long term reliability, the normal operating electric field in the gate oxide should be much lower. In the case of SiC MOSFETs, the problem is further enhanced by the fact that SiC has smaller conduction band offset to SiO_2 as compared to that of silicon [9]. The biggest problem with SiC MOSFETs is related to the ratio of dielectric permittivity of SiC and SiO_2. Gauss' law ($\nabla \bullet ee_0 \vec{E} = 0$) requires the product of the relative dielectric constant and the normal field of two materials to be constant at their interface. This implies that the normal field in the gate oxide would be 2.5 times higher[1] than that in the underlying SiC layer. Since the operating electric field in thermally grown SiO_2 is limited to 2 MV/cm [10], the maximum normal field in the underlying SiC layer must be less then 0.8 MV/cm, which is only 25% of its critical value.

As shown in Fig. 3.11, the surface electric field exhibits a peak at the sharp corner of the gate electrode. Although this peak value does not exceed the targeted maximum electric field of 1.7 MV/cm, which is well below the critical value for SiC,

[1] Dielectric constants for 4H-SiC and SiO_2 are equal to 10 and 3.9, respectively.

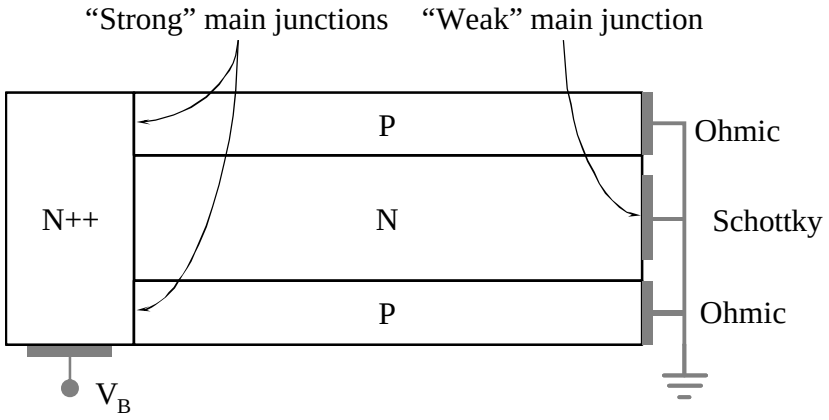


Figure 3.12: An example of a field compensated structure with different breakdown strengths of the main junctions.

it causes a significant difference in the oxide field. Such field enhancement at the corner of the gate electrode could be eliminated using one of the edge termination techniques discussed earlier in the Chapter II, for example, by using tilted field plate. However, it is still not reasonable to sacrifice the drift conductance just because of one “week” junction, while the other one can withstand 3 MV/cm. The example of a SiC MOSFET is not the only one that illustrates such kind of situation. Another example can be a super-junction Schottky barrier diode, shown in Fig. 3.12, where the breakdown strength of $n^{++} - p$ junctions is much higher than that of a Schottky barrier. In these cases it might be beneficial to design a field compensated structure in such a way, that the field distribution along the auxiliary junction is tilted. This can be achieved when using different doses in the drift and auxiliary region(s).

3.5 Bibliography

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CHAPTER IV

EXPERIMENTAL STUDY OF EDGE TERMINATION TECHNIQUES IN SIC POWER DIODES

4.1 Introduction

Several edge termination techniques from those discussed in Chapter II have been experimentally investigated in 4H-SiC PiN and Schottky Barrier diodes. The techniques studied in this chapter include floating guard ring [1, 2], Junction Termination Extension [1, 3], resistive edge termination [3], mesa termination [4], and a novel high-k dielectric edge termination [5, 6] The following sections provide a detailed discussion on the studied fabrication processes and the results of these studies.

4.2 Comparative Study of 4H-SiC PiN Diodes with JTE and Guard Ring Edge Termination

In order to compare the performance of different edge termination techniques in 4H-SiC PiN diodes, the devices utilizing different edge termination approaches were fabricated on the same substrate. The devices of the first type were fabricated with an implanted JTE region. The second type of edge termination was formed by heavily doped implanted floating guard rings. The devices with the third type of edge termination were fabricated with heavily doped floating mesa guard rings (MGRs). Non-terminated devices were left on the same substrate for comparison. The

schematic cross-sections of the fabricated devices with different edge terminations are shown in Fig. 4.1 [1].

4.2.1 Experimental

The diodes were fabricated on a heavily doped n-type substrate with an epitaxially grown base layer. The base layer was 10 μm thick and the n-type doping concentration was ~$2x10^{16}$ cm^{-3}. A heavily doped anode layer was formed by a 4-energy aluminum implantation with the total dose of $2.9x10^{15}$ cm^{-2} performed at 650ºC. The wafer was subsequently annealed for 30 min at 1650ºC in argon using a carbon cap to prevent degradation of surface morphology. Based on the experimental results published in [6], the aluminum activation percentage was estimated to be approximately 4%.

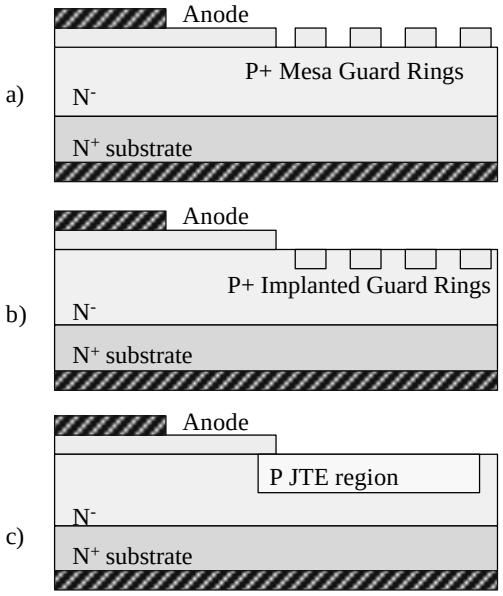


Figure 4.1: Schematic cross-sections of the fabricated PiN diodes: (a) with MGRs, (b) with traditional implanted guard rings, and (c) with JTE region.

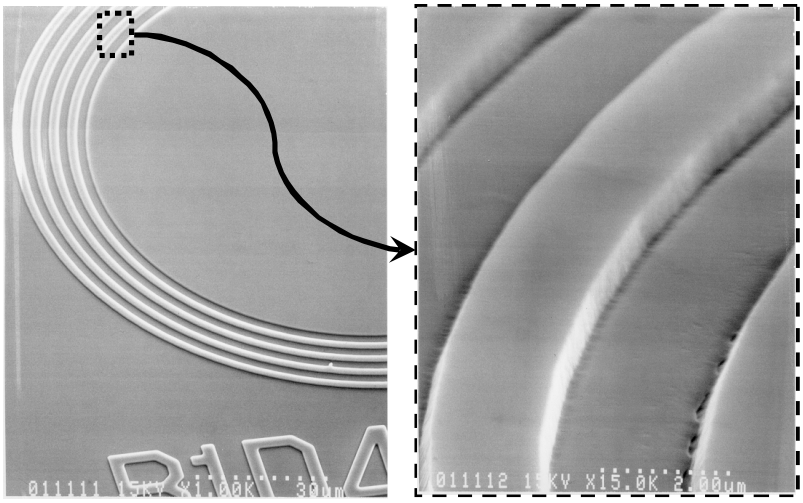


Figure 4.2: SEM pictures of a MGR-terminated 4H-PiN diode structure after SF_6 ICP etch.

The resulting 0.4-µm p-type layer was expected to have a free hole concentration of $4x10^{18}$ cm^{-3}. The anode regions and the mesa guard rings were then defined by ICP etching through 0.5 µm of SiC using SF_6 plasma. Fig. 4.2 shows the SEM images of a MGR-terminated diode structure after ICP etch. The left image shows the top view of a 4-ring, 0.01 mm^2 device, and the image on the right shows the etched guard ring mesas at x15 K magnification. The backside ohmic contact was formed by Ni annealed for 2 min at 1050ºC, and the anode contact was formed using Ti evaporation followed by a annealing at 850 ºC for 2 min. One micron of silver was then evaporated on both the anode and cathode contacts to reduce the contact resistance. The resulting structure of an MGR-terminated PiN diode is shown on Fig. 4.1 (a). No intentional surface passivation was done on the fabricated devices. In addition to the MGRs-terminated devices, diodes with traditional implanted guard rings and those having JTE regions were fabricated on the same wafer (Fig. 4.1 b, c). Implanted guard rings had the same implantation schedule as MGRs, and the

implantation dose of the JTE region was chosen to be $2.2x10^{13}$ cm^{-2}. Annealing of all the implanted regions was performed in the same step. The die layout and an optical photograph of the fabricated devices are shown in Fig. 4.3.

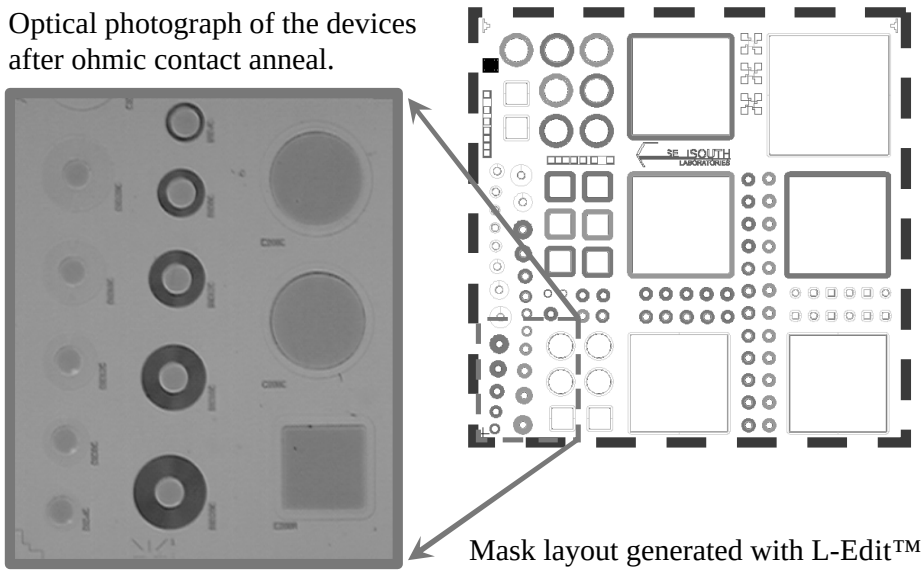


Figure 4.3: Optical photograph of the fabricated 4H-SiC PiN diodes (left), and die layout (right).

4.2.2 Results and discussion

After the fabrication was completed, current-voltage measurements were carried out using a Keithley 237 SMU and a Tektronix 576 curve tracer. Devices with different edge terminations demonstrated similar forward current density of approximately $1kA/cm^2$ at 7.5V, while showing different blocking capabilities.

As shown in Fig. 4.4 and Table 4.1, the average blocking voltage for the devices with 12 MGRs was 852 V. At the same time, the average blocking voltages of the devices with implanted guard rings and JTE were 954 V and 1078 V, respectively (upper values were limited by 1.1 kV – the maximum source voltage for

Keithley 237 SMU). The best devices of each category have shown more than 1.1 kV breakdown voltages.

In general, the average reverse breakdown voltage of the diodes with MGRs was found to be smaller than that of the devices with the traditional edge terminations. The two-dimensional device simulation shows that the spacing between the mesa rings has to be reduced as much as possible to spread the potential smoothly from the edge of the device. Such tight spacing dictates rather aggressive photolithography requirements. For example, the 2-D analysis using ISE, Inc.'s DESSIS SiC module performed by another group [8] has shown that reducing the space between the MGRs from 1 µm to 0.5 µm results in almost a two-fold increase of the breakdown voltage on a GTO structure with n-type mesa guard rings. In this work, we have analyzed the fabricated devices with real geometry and doping parameters using Medici ™ software. It was found, that for the 4-ring device with 2-µm spacing between the rings, the simulated electrical field at the surface between the anode and the first ring reaches 4.7 MV/cm at a reverse bias of only 700V, and it significantly exceeds 5 MV/cm at 900 V (Fig. 45). This electrical field far exceeds the critical value for the SiC.

Table 4.1: Dependence of blocking voltage on the type of edge termination for the PiN diodes with an active area of 0.01 mm^2.

Edge termination	12 MGRs	8 MGRs	4 MGRs	30-µm JTE Region	8 Implanted Guard Rings
Average blocking, V	852	810	653	1078	954
Best blocking, V	>1100	1036	874	>1100	>1100

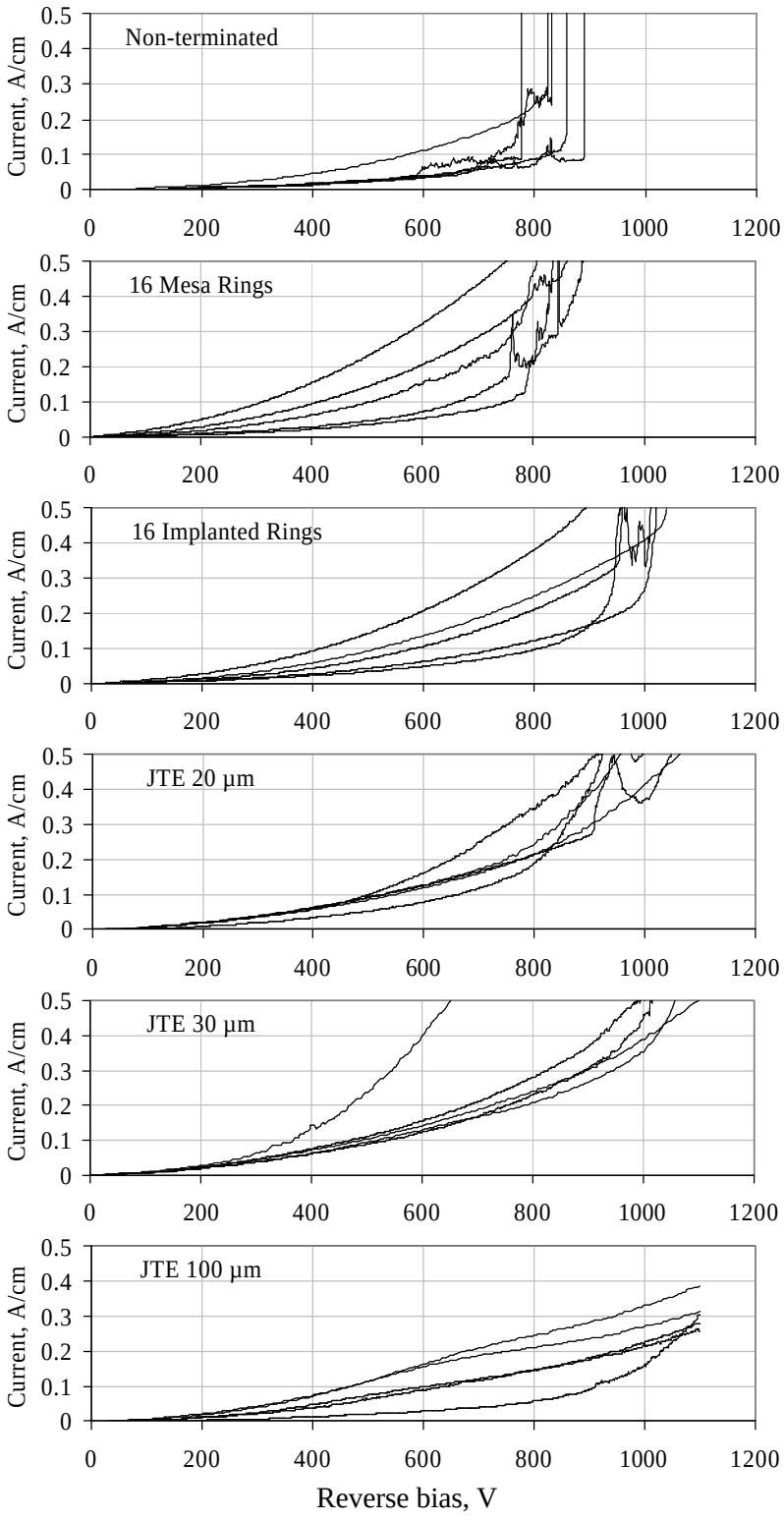


Figure 4.4: Typical reverse I-V characteristics measured on fabricated devices with different edge terminations (the type of the edge termination is shown in the top-left corner of each plot).

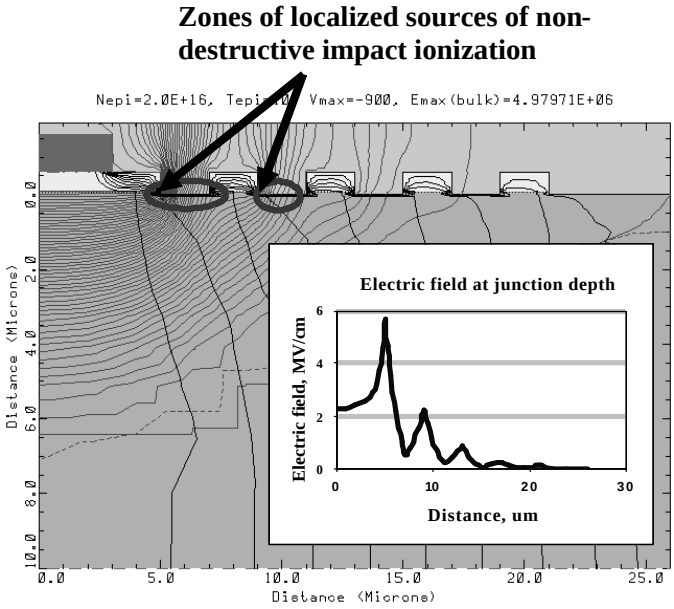


Figure 4.5: Simulated potential distribution and current flow in a MGR-terminated 4H-SiC PiN diode at the reverse bias of 900 V. The crowding of the equipotential lines corresponds to the electric field shown in the insertion plot.

On the other hand, the best 4-ring device fabricated with the same device parameters used in the above simulation has demonstrated a breakdown of 874 V. In the previous work [1], we speculated that this apparent contradiction between the simulation and the experimental results may have a possible explanation in the dynamic spreading of the potential by localized non-destructive sources of impact ionization (Fig. 4.5). These sources, located at the surface between guard rings closest to the device active area, virtually short these rings to the anode, and move the regions of the highest electric field further away from the main junction, which saves the devices from a premature failure. However, later analysis of the results with respect to the fabrication process suggested another explanation of the high blocking capability of the MGR-terminated devices. The guard ring mesa etch was perform

through 0.5 μm of SiC assuming the depth of the p-n junction formed by the implanted and activated aluminum acceptors to be less than 0.4 μm. Fig. 4.6 shows the as-implanted Al concentration profile calculated for the used implantation schedule calculated using Pearson Type IV distribution with fitted coefficients [9, 10]. Assuming 4% aluminum activation, the junction depth was expected to be ~3.7 kÅ. In 8º off-axis 4H-SiC, the Pearson Type IV distribution is well established for the highly accurate description of dopant profiles. Unfortunately, at the concentration level of ~0.2% of the peak concentration, the implanted Al profiles exhibit the so-called tails, that cannot be described by Pearson formulas. In MGR-terminated devices, such implantation tail could result in the junction depth much deeper than the etch depth, causing an unintentional JTE-type edge termination in addition to the mesa guard rings. The fact that the "non-terminated" diodes have demonstrated breakdown voltages similar to those of MGR-terminated devices further supports this hypothesis.

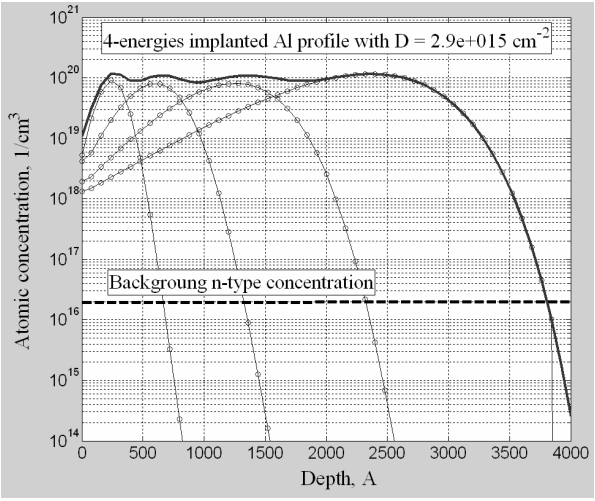


Figure 4.6: Al^+ concentration profile in fabricated diodes calculated using Pearson IV distribution.

4.3 Comparative Study of 4H-SiC PiN Diodes with JTE and Resistive Edge Termination

The second lot of the 4H-SiC PiN diodes has been fabricated on three research grade n-type substrates, bought from two different vendors. The thickness of the epitaxially grown n-type base layer ranged from 10 µm to 11 µm, while the doping varied from $5x10^{15}$ cm^{-3} to $1x10^{16}$ cm^{-3}. The epitaxially grown p-type anode layers had thickness of 0.5 µm and the measured active doping concentration ranged from $1.5x10^{19}$ cm^{-3} to $2x10^{19}$ cm^{-3}. A schematic cross-section of the fabricated diodes is shown in Fig. 4.7. Assuming a perfect material quality, the active device area that defines the current capability can be scaled without limitation. However, to get the number of working devices fabricated on the research grade material large enough for a statistical comparison of different edge termination approaches, the active area of the fabricated PiN diodes had been chosen to be $8.4x10^{-5}$ cm^2. Such a small active area allowed minimizing the influence of micropipes and other structural and surface defects on the device performance [11].

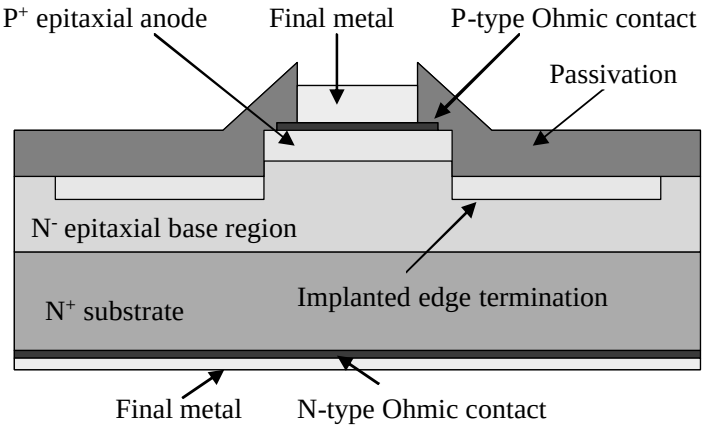


Figure 4.7: Schematic cross-section of the fabricated 4H-SiC PiN diodes.

4.3.1 Experimental

After the mesa formation using ICP etch, the devices were selectively implanted to form 100-µm and 200-µm edge termination regions. Two wafers received a multiple energy aluminum implantation with the total dose of $2x10^{13}$ cm^{-2}, and the third wafer received a single energy boron implantation with the dose of $1x10^{15}$ cm^{-2}. The implantation dose for the aluminum JTE regions was chosen based on the epi thickness and doping, targeted blocking voltage as well as the activation percentage of implanted Al atoms. The Al-implanted wafers were annealed with the same parameters as described in the previous section. From the comparison of the simulation results and the CV data obtained on a test sample, ~70% post-anneal activation of aluminum was expected.

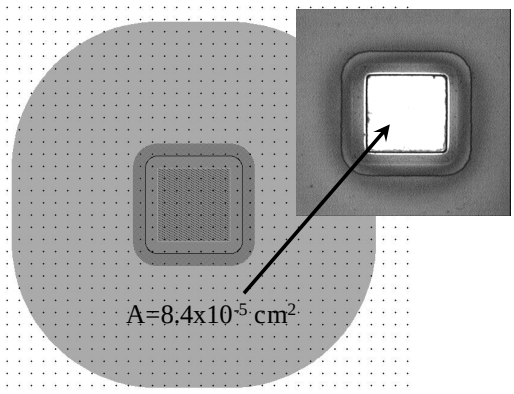


Figure 4.8: The layout design and a photograph of a fabricated $8.4x10^{-5}$ cm^2 4H-SiC PiN diode after passivation and final metal deposition.

The boron-implanted wafer was annealed for 30 min at 1050ºC. This anneal is sufficient to partially repair the implant damage, but does not activate the dopant. The resulting implanted layer produces a lateral potential drop in the blocking state,

tapering the electric field and minimizing field crowding at the anode edge [12]. After the ohmic contact formation as described in the previous section, a thick passivation layer and final metal were deposited. The layout design and the appearance of the fabricated diodes are shown in Fig. 4.8.

4.3.2 Results and discussion

The diodes with both types of edge termination demonstrated sharp non-destructive breakdowns with a yield higher than 80% at above 1.7 kV without using Fluorinert™. The average measured forward current density was 1.2 kA/cm^2 at V_F = 5 V and 6.5 kA/cm^2 at V_F=8V. Fig. 4.9 shows the forward and reverse I-V characteristics of a fabricated 4H-SiC PiN diode with the Al-implanted JTE region, measured on a Tektronix 371 curve-tracer. The reverse leakage current has been measured using a Keithley 237 SMU with the maximum source voltage of 1.1kV. An interesting tendency was found when comparing leakage current on the devices with different sizes of the JTE region. The diodes with wider JTE region exhibited higher reverse leakage current than those with narrower JTE. It was found that at reverse biases below 800 V, the leakage of the JTE-terminated devices was proportional to the outer perimeter of the JTE region.

In order to analyze this phenomenon, the leakage currents measured on the devices with different JTE size were normalized to the anode area and to the outer perimeter of the JTE region. As shown in Fig. 4.10, below 800 V, the currents normalized to the perimeter remain essentially the same for both types of device, while at higher voltages, the normalized current of the larger devices starts growing faster. The result of the numerical simulations shown on the right side of Fig. 4.10

with respect to the device cross-section helps to explain this observation. At low to medium voltages, the leakage current is caused by the generation of the electron-hole pairs along the outer JTE perimeter, where the peak electric field occurs. At higher voltages, however, the electric field distribution flattens, while growing to the values that cause the generation of free carriers. At such high voltages the current becomes proportional to the total device area rather than to the outer JTE perimeter, which explains the faster growth of the normalized current measured on a device with a 200-µm JTE region.

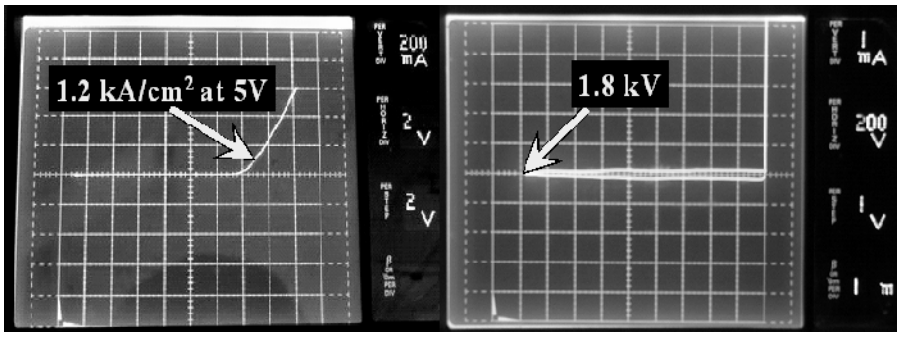
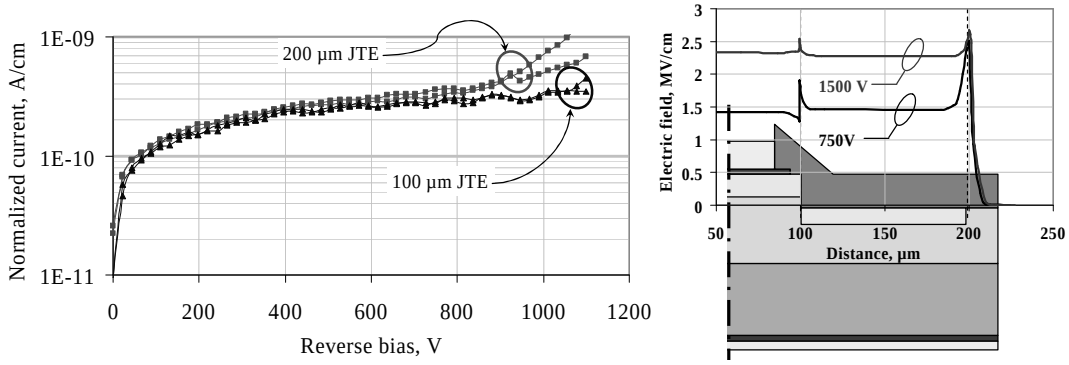


Figure 4.9: Forward (left) and reverse (right) I-V characteristic of a fabricated 4H-SiC PiN diode.



(a) (b)

Figure 4.10: (a) Leakage current measured on the JTE terminated devices normalized to the outer perimeter of JTE region as a function of the applied reverse bias, and (b) electric field distribution along the JTE region for different reverse biases.

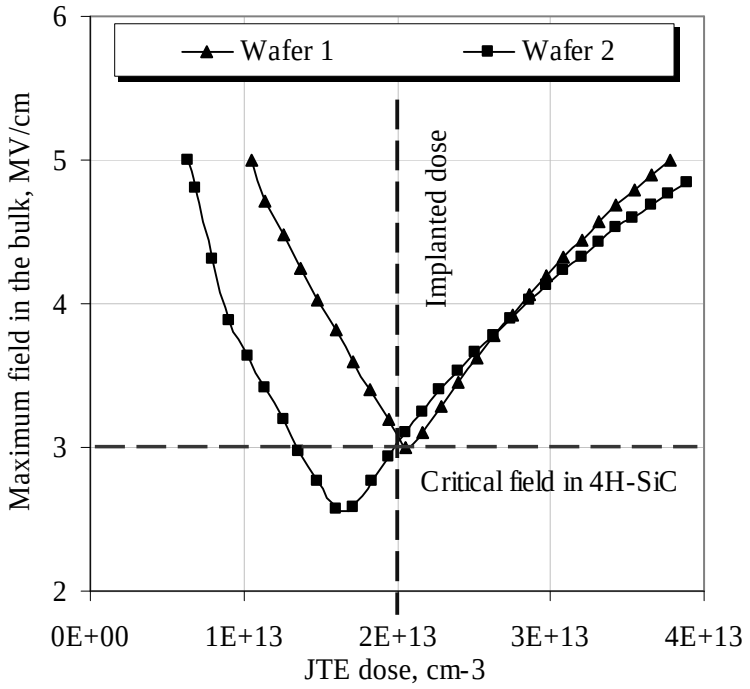


Figure 4.11: Simulation results showing the dependence of the maximum electric field in the device bulk on the implantation dose of the JTE region for the devices with different parameters of the base region.

Table 4.2: Comparative summary of the measured results and structural parameters of the fabricated 4H-SiC PiN diodes.

Wafer # and vendor	1 (vendor 1)	2 (vendor 2)	3 (vendor 2)
N-type epi thickness, μm	11	10	10
N-type epi doping, cm^{-3}	$1x10^{16}$	$5x10^{15}$	$5x10^{15}$
Implant ion	Aluminum	Aluminum	Boron
Implant dose, cm^{-2}	$2x10^{13}$	$2x10^{13}$	$1x10^{15}$
Blocking voltage, kV	1.8	1.7	1.7
Maximum 1D electric field, MV/cm	2.63	2.1	2.1
Maximum simulated electric field in the bulk, MV/cm	3	3	n/a

The results obtained on the Al JTE-terminated devices with different epi parameters closely match the simulation results. This confirms the reproducibility and scalability of the design to much higher blocking voltage and forward current levels. As shown in Fig. 4.11, the maximum electric field in the device bulk is the same for the wafers with different epi thickness and doping. This field occurs at the device edge, and is equal to 3 MV/cm, which is close to the critical electric field in 4H-SiC. The implantation JTE dose (equal for both wafers) fits the optimal simulated value for the wafer with a heavier doped epi layer, which explains the better blocking capability of the devices fabricated on this wafer. Table 4.2 presents a summary of measured results for different edge termination techniques and base layer parameters. It can be noticed from this table, that the PiN diodes fabricated on the substrates from the same vendor with identical parameters of the base layer have demonstrated the same voltage blocking capabilities with independent to the chosen edge termination technique whether it is Al-implanted JTE or resistive boron-implanted termination. Since the nature of the high-dose low-temperature boron edge termination is still not clear, no simulation has been performed for the boron-terminated devices at this time.

4.4 Comparative Study of 4H-SiC PiN Diodes with Resistive and Mesa Edge Termination

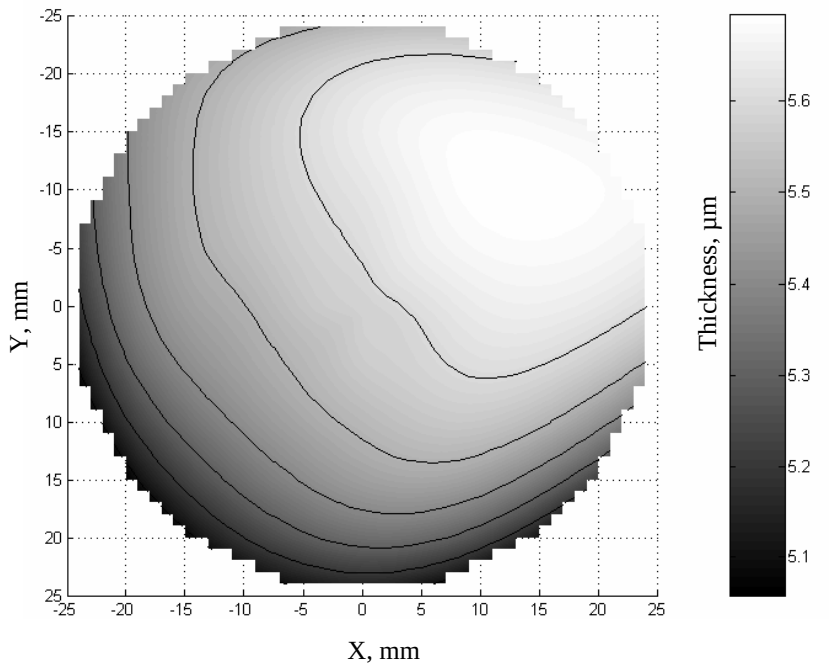
The encouraging results achieved on the PiN diodes with resistive edge termination formed by high-dose boron implantation have been discussed in the previous section. This technique allows for a relatively simple fabrication process by eliminating the high-temperature implantation and post-implantation annealing steps required for the Al-implanted JTE. However, as discussed earlier, the resent studies on the implanted resistive edge terminations revealed high-voltage pulse instabilities

in SiC devices fabricated using this type of edge termination. This instability is found to be caused by slow response of deep traps produced by implantation damage.

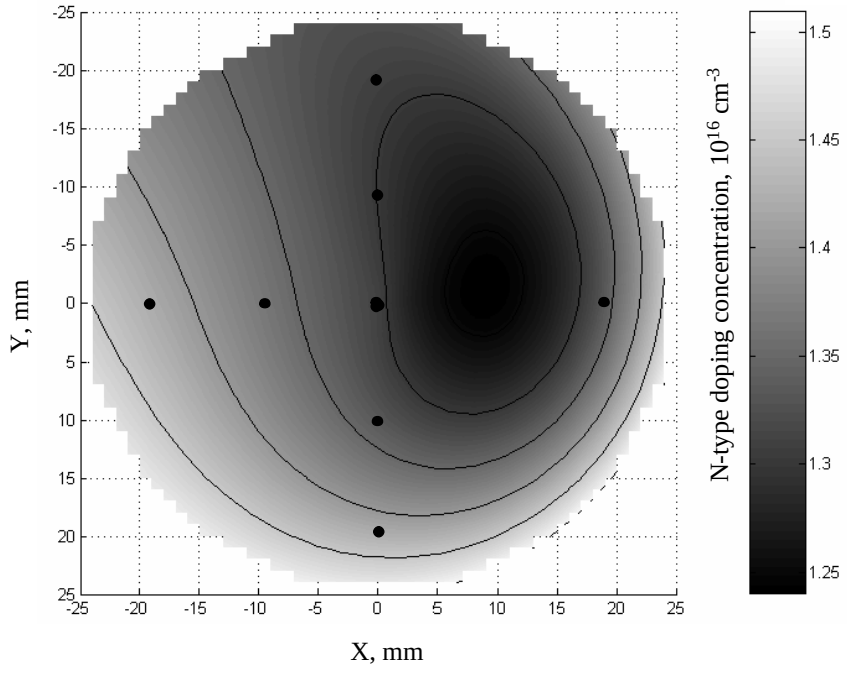
Another simple and scalable edge termination technique discussed in Chapter II, mesa edge termination, should be inherently secure to high-voltage pulse instabilities because it does not rely on the distribution of the negative charge dynamically built along the voltage blocking layer. As discussed earlier, this stand-along edge termination technique that does not laterally spread the depletion region also allows for more efficient use of area than other techniques, resulting in lower cost and higher yield.

4.4.1 Experimental

Mesa-terminated PiN diodes with base layer designed for the maximum plane-junction electric field E_{1DMAX} = 1.8 MV/cm at V_B = 600 V were fabricated on three 2-in 4H-SiC substrates. Epitaxially grown voltage-blocking layers were characterized using FTIR (61 point per 2-in substrate) and Hg-probe CV (9 points per 2-in substrate at 100 kHz) to extract their thickness and doping distributions. The measured values were then interpolated/extrapolated using cubic splines in polar coordinates using MATLAB. A typical epi thickness map is shown in Fig. 4.12 (a), and the doping map is shown in Fig. 4.12 (b). For comparison, 4H-SiC PiN diodes with resistive termination formed by high-dose boron implantation have been fabricated on another three 2-in wafers having the same base layer parameters as the devices with mesa termination.



(a)



(b)

Figure 4.12: (a) A typical FTIR-measured thickness map and (b) CV-measured doping map of voltage blocking layer of mesa-terminated and boron-terminated 4H-SiC PiN diodes.

4.4.2 Results and discussion

After completing the fabrication, on-wafer I-V measurements were done in Fluorinert™ using Keithley 237 SMU and a Tektronix 576 curve tracer. The devices with both types of edge termination demonstrated a reversible avalanche breakdown. Figure 4.13 shows a non-destructive avalanche breakdown measured on a mesa-terminated diode using Tektronix 576 curve tracer.

Wafer-scale measurements of the breakdown voltage were done with a 25 V step increment of reverse bias on semi-automatic probe-station. A typical V_B map (measured on the same substrate as in Fig. 4.12) is shown in Fig. 4.14 (a). The maximum 1-D electric field E_{1DMAX} was then extracted from the measured epi parameters and breakdown voltage using expression

$$E_{1DMAX} = \frac{V_B}{t} + \frac{q \cdot t \cdot N}{2 \cdot e_0 \cdot e_r} \tag{4.1}$$

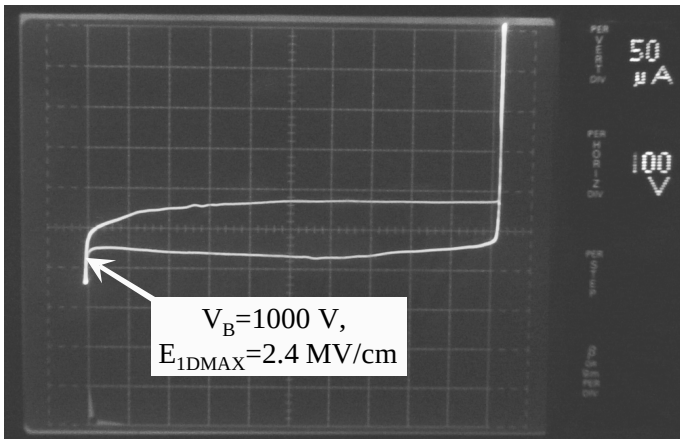
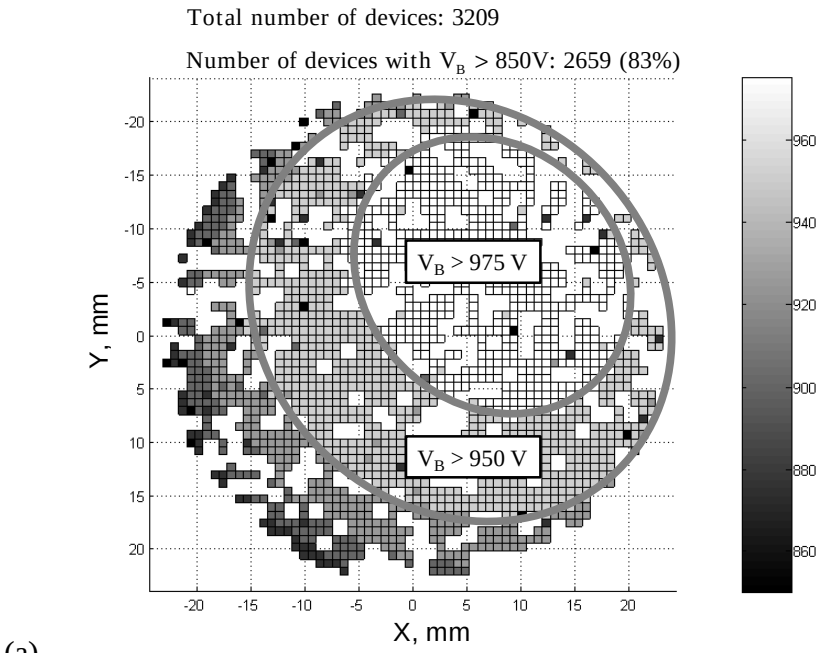
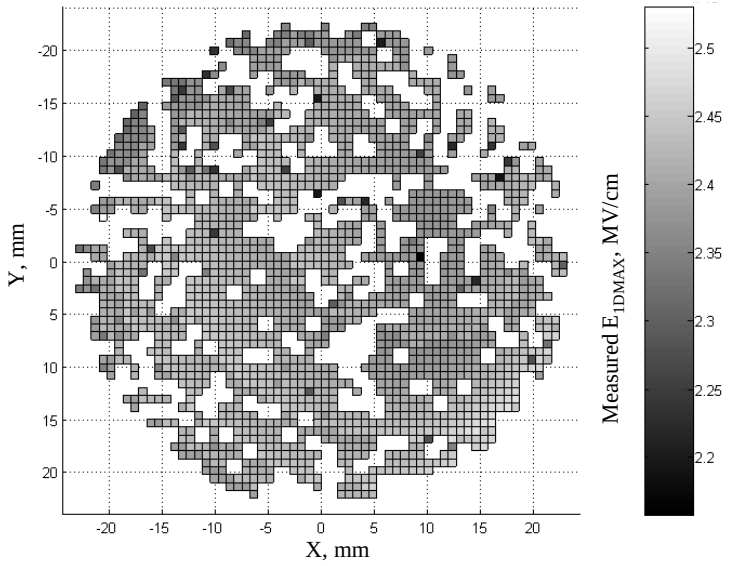


Figure 4.13: A non-destructive avalanche breakdown measured on a mesa-terminated diode with 5.7 μm, 1.25×10^{16} cm^{-3} base layer.



(a)



Highest $E_{1D\,MAX}$ = 2.53 MV/cm;

Mean $E_{1D\,MAX}$ = 2.40 MV/cm;

$E_{1D\,MAX}$ standard deviation: s = 0.035 MV/cm;

$E_{1D\,MAX}$ uniformity: $\frac{s}{\text{mean}} = 1.45\%$

(b)

Figure 4.14: Wafer maps showing (a) measured breakdown voltages and (b) extracted E_{1DMAX} on the same substrate as in Fig. 4.12. Reverse bias measurements were done with 25 V step. Devices with V_B < 850 V are excluded from the maps.

On mesa-terminated diodes, the mean value of this field was found to be of 2.4 MV/cm with a standard deviation s =35 kV/cm. Such small standard deviation from the mean value corresponded to E_{1DMAX} uniformity of 1.45%. In reality, this value should be even smaller, because of the 25 V step used in the measurements of the breakdown voltage (the thickness and doping were approximated with smooth cubic polynomials). A map of E_{1DMAX} is shown in Fig. 4.14 (b). These results convincingly demonstrate that the critical electric field in 4H-SiC is *at least* equal to 2.4 MV/cm. The experimentally achieved E_{1DMAX} of 2.4 MV/cm corresponds to ~93% of the "theoretical value" of critical electric field in 4H-SiC given by Ref. [13]:

$$E_C = \frac{2.49 \cdot 10^6}{1 - \frac{1}{4}\log_{10}\left(\frac{N_D}{10^{16}}\right)} \ (V/cm) \qquad (4.2)$$

Although the charge conditions on the mesa sidewalls are unknown, the simulation results suggest that the electric field may experience a certain non-linear increase as shown in Figs. 2.5 and 2.6. In this case, the electric field reaches its true critical value at the anode junction that triggers an avalanche breakdown. The majority of the mesa-terminated devices measured on all 3 substrates (5584 of 8222 tested, or 67.9%) demonstrated an average breakdown voltage ranging from 925 V to 975 V.

The majority of the devices with resistive edge termination (4999 of 8853 tested, or 56.5%) demonstrated an average breakdown voltage ranging from 875 V to 925 V that corresponds to the average maximum one-dimensional electric field under the main device junction E_{1DMAX} of 2.26 MV/cm. Figure 4.15 shows a comparison

between yield distributions of the diodes fabricated using different edge termination techniques.

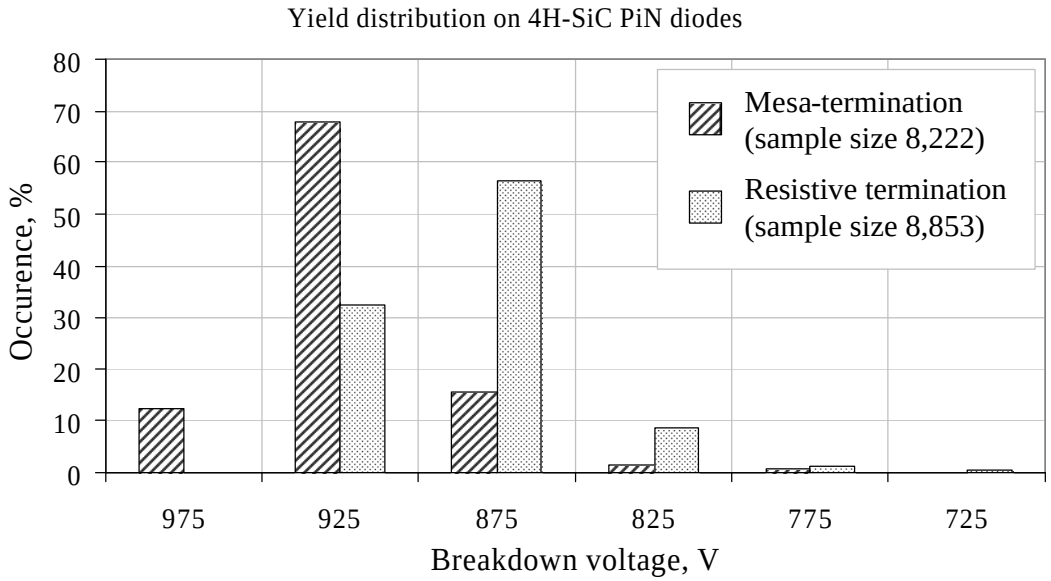


Figure 4.15: Comparison of yield distribution between 4H-SiC PiN diodes with different edge termination techniques.

4.5 4H-SiC Schottky Barrier Diodes with High-k Edge Termination

In order to demonstrate the feasibility of the high-k edge termination discussed in the previous chapter, 4H-SiC Schottky barrier diodes have been fabricated on two quarters of a 2-inch 4H-SiC wafer from Cree Inc. The samples had epitaxially grown n-type layer with the thickness of 10 μm and the doping of $5x10^{15}$ cm^{-3}. The devices were fabricated using a low cost two-mask design with no implanted edge termination. The diodes fabricated on one quarter obtained nickel Schottky contact; the others were made using titanium Schottky contact. The fabricated diodes were then passivated using a high-k spin-on dielectric.

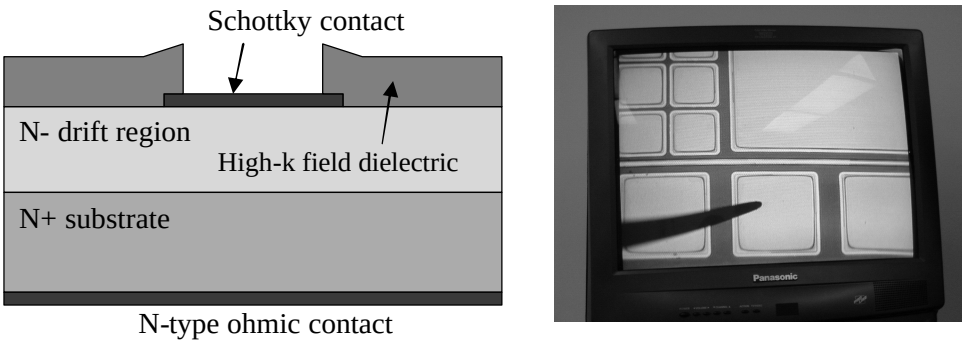
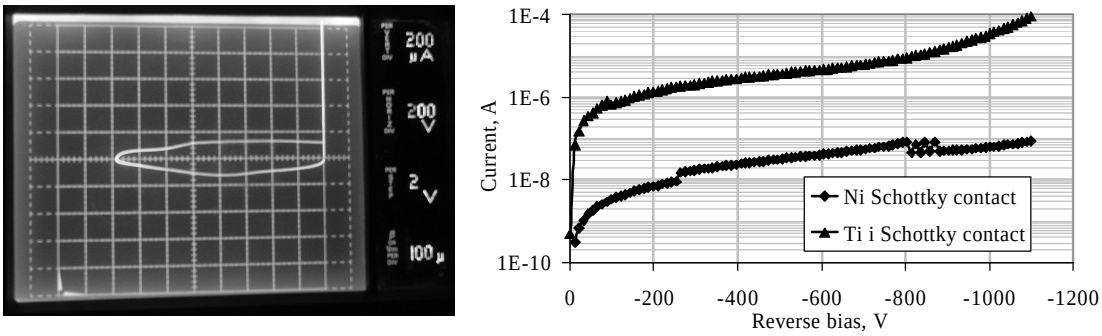


Figure 4.16: Schematic cross-section (a) and display appearance (b) of the fabricated 4H-SiC SBDs with high-k edge termination.

Since the main goal of the experiment was to the test performance of the high-k edge termination applied to the Schottky barrier rather than the high-current performance, no final metal was deposited. A schematic cross-section and display appearance of the fabricated 4H-SiC Schottky barrier diodes with high-k edge termination are shown in Fig. 4.16.

The reverse I-V characteristics of the fabricated diodes were measured using a Keithley 237 SMU, and a Tektronix 576 curve-tracer. The small area devices with both nickel and titanium Schottky contacts demonstrated non-destructive reversible breakdown at voltages up to 1.6 kV, which corresponded to the maximum one-dimensional (1D) electric field that was determined to be 2MV/cm. Fig. 4.17 (a) shows a screenshot of the Tektronix 576 curve-tracer with displaying the reverse characteristic of a 4H-SiC SBD with an area of 6.25×10^{-4} cm^{-2}. At 1.2 kV, the production size 1 mm^2 diodes showed a yield greater then 90%. A significant difference in the reverse leakage current of more than 2 orders of magnitude was observed between the diodes fabricated with nickel and titanium Schottky contacts as

shown in Fig. 4.17 (b). In order to investigate the temperature stability of the high-k edge termination, the temperature dependence of reverse leakage current was investigated for the small-area high-k-terminated 4H-SiC Schottky diodes with Ti Schottky contact.



(a) (b)

Figure 4.17: (a) Reverse characteristic of $6.25\times10^{-4}cm^2$ 4H-SiC SBD, measured on Tektronix 576 curve-tracer and (b) Comparison of the reverse leakage current measured on $1mm^2$ high-k-terminated SBDs with Ti and Ni Schottky contacts.

As shown in Fig. 4.18, with the temperature increase from 25ºC to 200 ºC the leakage current through the Schottky contact increased by as much as 3 orders of magnitude. When analyzing the cause of the reverse leakage, it was found, that the leakage current was not proportional to the area, but rather to the perimeter of the Schottky contact as demonstrated in Fig. 4.19, where the leakage current measured on the devices with different contact areas is normalized to the contact perimeter and plotted as a function of the reverse bias. This observation results in the following implications.

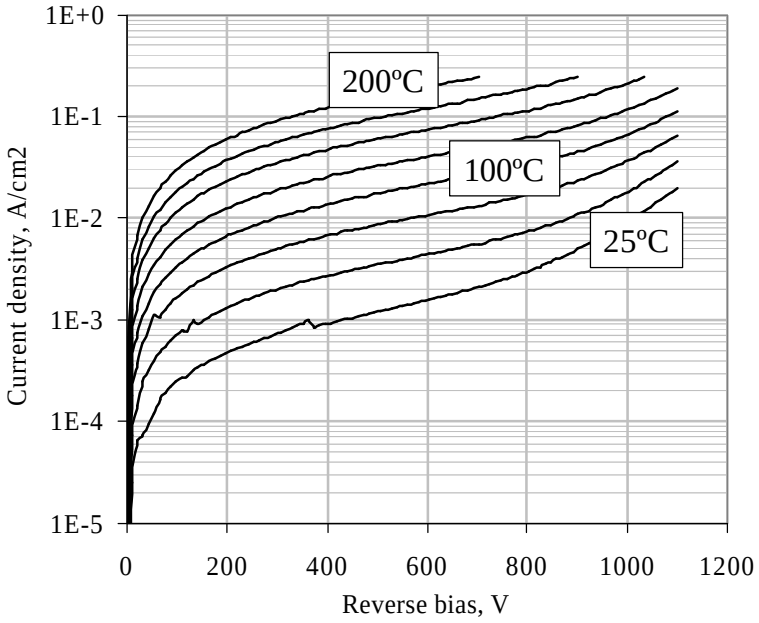


Figure 4.18: Temperature dependence of reverse leakage current of a $6.25\times10^{-4}cm^2$ high-k-terminated 4H-SiC SBD with Ti Schottky contact measured with temperature increment step of 25ºC.

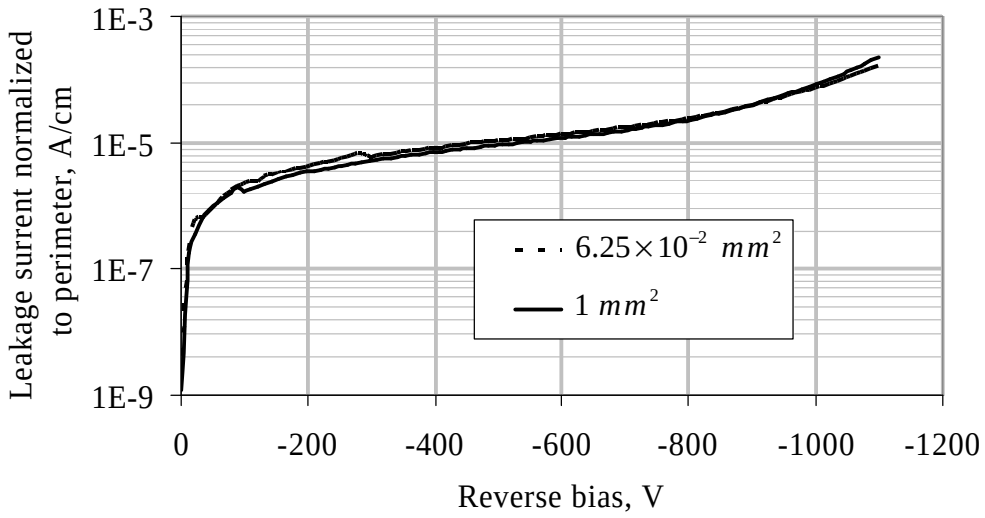


Figure 4.19: Leakage current measured on high-k terminated Ni SBDs normalized to the correspondent device perimeter plotted as a function of the reverse bias.

First, the proportionality of the leakage current to the device perimeter implies that scaling up the device area will result in better forward/reverse current ratio.

Second, it confirms the fact that, as shown in Fig. 2.8 in Chapter II, the electric field applied to the Schottky barrier experiences an increase at the edge of the main junction resulting in leakage current caused by the thermionic field emission to be proportional to the perimeter of the Schottky contact.

The k-value of the dielectric used for the high-k edge termination was measured on parallel-plate capacitors with platinum contacts. The C-V measurements were conducted at 1 MHz and 100 kHz resulting in the k-value of the investigated dielectric approximately equal to 40. The results of the measurements are shown in Fig. 4.20, where the extracted dielectric constant is plotted as a function of the applied DC bias.

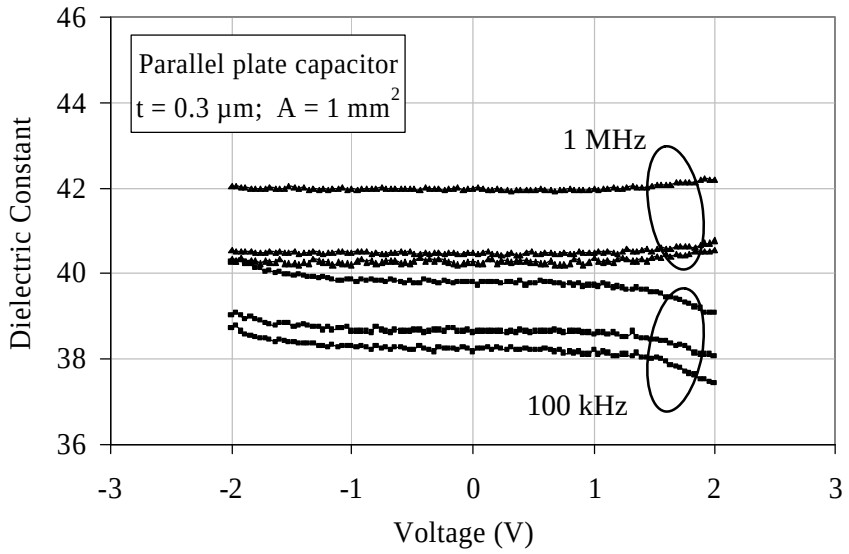


Figure 4.20: Results of the C-V measurements of the dielectric constant of the high-k spin-on dielectric used for the edge termination on the fabricated diodes.

Another set of Ti 4H-SiC Schottky barrier diodes with high-k edge termination was fabricated on a 2-inch 4H-SiC wafer with 5 µm, $8x10^{15}$ cm^{-3} n-type epitaxial layer. The fabricated devices had a structure similar to that shown in Fig. 4.16 (a), but with thick final metallization formed in order to characterize the forward current density, switching performance, and long-term reliability. The backside ohmic contacts were formed using a vacuum anneal of a sputtered Ni contact followed by e-beam deposition of a diffusion barrier / final metal stack. The Schottky contacts were formed by Ti evaporation followed by e-beam deposition of a diffusion barrier / final metal stack. The fabricated diodes received the same high-k field dielectric edge termination as was used in the first run. The mask set consisted of devices having three different areas: 0.07 mm^2, 1 mm^2, and 4 mm^2.

The testing of the fabricated 4H-SiC Schottky barrier diodes was performed using a Keithley 237 SMU and a Tektronix 576 curve-tracer. While showing a leakage current of 100 µA at a reverse bias of 800 V, the small 0.07 mm^2 diodes demonstrated a current of 1 A at 2 V forward bias, which corresponds to a current density of 1.5 kA/cm^2. To our knowledge, this is the highest current density at 2 V ever reported for 800 V 4H-SiC Schottky diodes. Fig. 4.21 shows reverse and forward characteristics of a 0.07 mm^2 diode. Forward and reverse stress measurements were performed to identify the potential issues with the long-term reliability of the high-k edge termination. As shown in Fig. 4.22, these measurements demonstrated negligibly small changes in both the reverse and forward currents. Fig. 4.22 (a) shows the result of a 6-hr testing at a reverse stress of 600 V, and Fig. 4.22 (b) shows the result of a 4-hr testing of the same device at a forward stress of 750 A/cm^2.

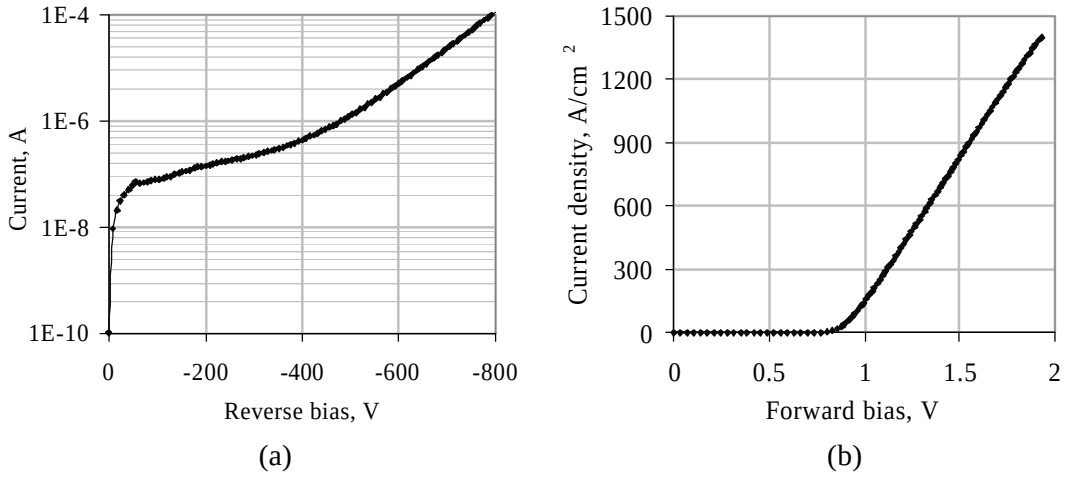


Figure 4.21: Reverse (a) and forward (b) I-V characteristics measured on a 0.07 mm^2 Ti 4H-SiC Schottky diode with high-k edge termination.

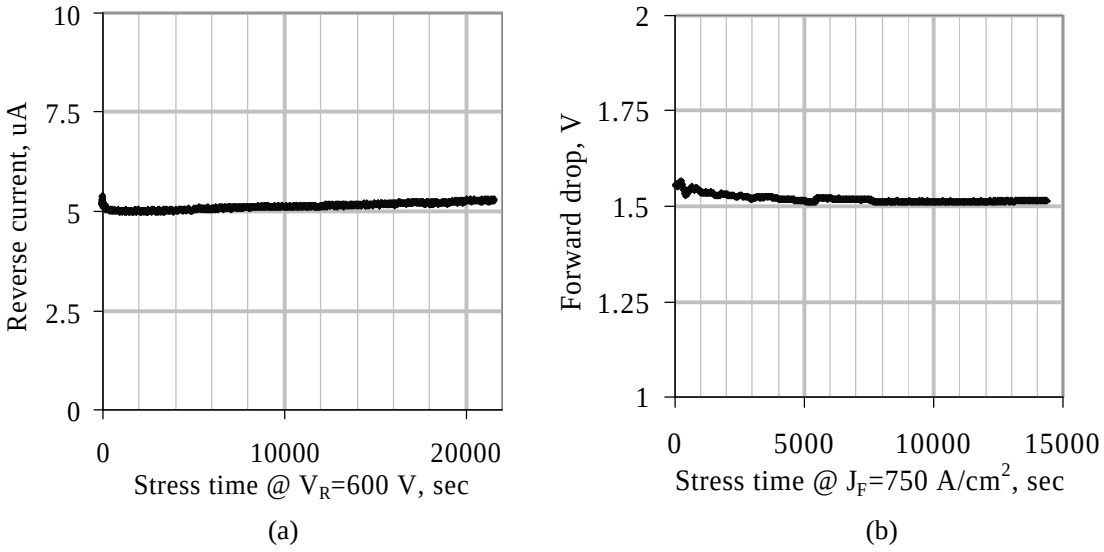
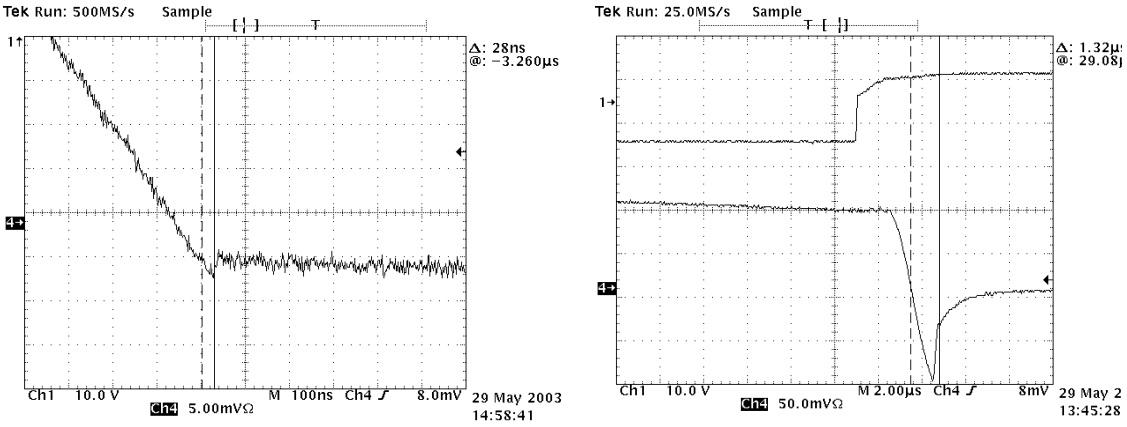


Figure 4.22: Stress measurements on a 0.07 mm^2 Ti 4H-SiC Schottky diode with high-k edge termination.

Transient-time measurements performed on a 1A, 800V 4H-SiC Schottky diode demonstrated almost zero reverse recovery time, as shown on Fig. 4.23.

In order to reduce the on-state resistance, 1 mm^2 Ti 4H-SiC high-k-terminated Schottky diodes were fabricated on the substrate thinned from 400 μm down to 200 μm with an n-type epitaxial layer with higher doping concentration than in the previous experiments. Again, a high-k edge termination was formed using the same process as in the previous lots. Although the fabricated devices had somewhat lower breakdown strength, their forward characteristics demonstrated almost ideal behavior that proved the process compatibility of the Schottky contact formation and the high-k edge termination. The current density measured on the packaged devices exceeded 1 kA/cm^2 at the forward voltage drop below 2 V, while the ideality factor of Schottky junctions calculated for these devices was below 1.1. The forward characteristics of four 1 mm^2, 500 V, Ti 4H-SiC SBDs with high-k edge termination are shown in Fig. 4.24 in comparison of reverse recovery of a 200 V silicon diode 1N4141 (b).



(a) (b)

Figure 4.23: Almost zero reverse recovery of a tested 800 V 4H-SiC SBD (a) is given in comparison of reverse recovery of a 200 V silicon diode 1N4141 (b).

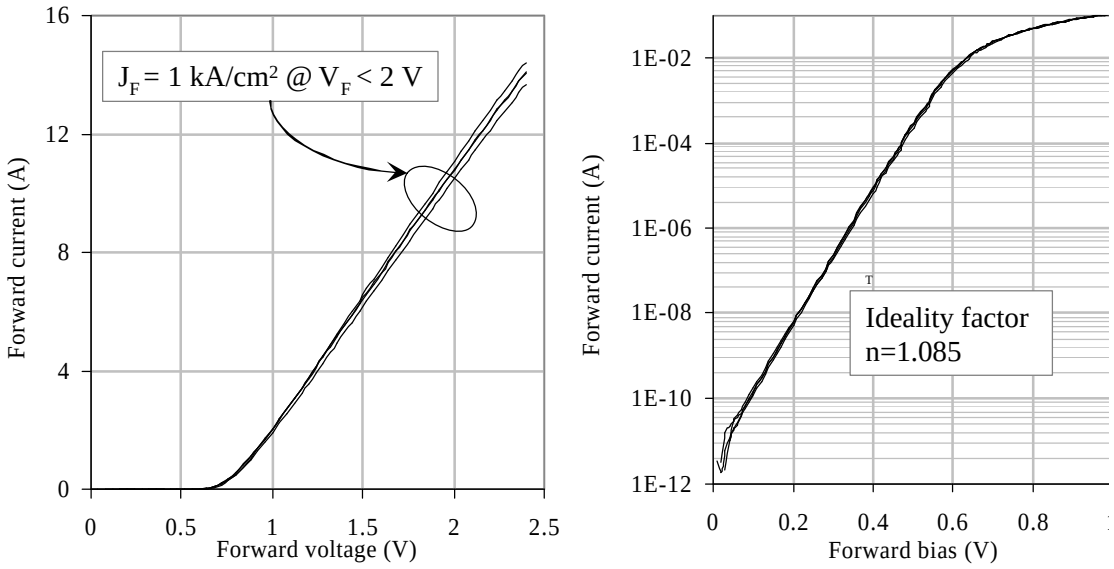


Figure 4.24: Forward characteristics of four 1 mm^2, 500 V, Ti 4H-SiC SBDs with high-k edge termination.

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CHAPTER V

DESIGN AND FABRICATION OF LATERAL DMOSFET IN 6H-SIC

5.1 Introduction

The work on SiC power MOSFETs strove to achieve very low ideal on-resistance values made possible by the high saturation drift velocity of SiC ($2x10^7$ cm/s), which is twice higher than that of Si. However, very low channel mobilities in lateral and vertical SiC MOSFETs have prevented the actual on-resistance from reaching its theoretical low values [1-7]. Much of the previous studies in SiC MOSFETs have yielded effective channel mobility values (m_{eff}) from less than 1 $cm^2/V \bullet s$ [2] to above 100 $cm^2/V \bullet s$ [3]. Lipkin, *et al.*, reported 6H-SiC MOSFET channel mobility of 72 $cm^2/V \bullet s$ in 1996, which was a substantial improvement over previous values [1]. This success was found to be a result of the improved oxidation procedures, which lowered the very high interface trap density, in particular with the energy states near the conduction-band edge [2, 6]. The Work by Schörner *et al*, reported the differences found between MOSFETs fabricated with three different polytypes (6H, 4H, and 15R) of SiC [2]. The devices built in 4H-SiC demonstrated an effective channel mobility of 0.4 $cm^2/V \bullet s$, while MOSFETs fabricated in 6H- and 15R-SiC polytypes had higher values of 24 $cm^2/V \bullet s$ and 33 $cm^2/V \bullet s$, respectively. The additional work focused on 6H-SiC n-channel enhancement-mode devices,

revealed that μ_{eff} decreased strongly (from 42 $cm^2/V\bullet s$ to 27 $cm^2/V\bullet s$) with increasing channel doping (from $2x10^{14}$ cm^{-3} to $2x10^{16}$ cm^{-3}) [6], but, unlike the previous reports, it also decreased moderately with increasing temperature [6,7].

The effective mobility in the channel is determined by many factors, such as the crystal orientation, bulk mobility, dopants concentration, surface roughness, and cumulative surface charge density. Generally, much lower μ_{eff} values have been observed in 4H-SiC MOSFETs than in 6H devices, caused by the larger density of interface trap states in the bandgap, in particular near the conduction band edge [6-7]. Additionally, the implanted source and drain regions require a higher activation temperature in 4H-SiC (1500ºC versus 1200ºC for 6H-SiC in the case of nitrogen donor), which contributes to increased surface roughening or step-bunching [4, 8-10]. Although it currently appears that the interface density of states at the edge of the conduction band is the primary factor limiting μ_{eff}, the severe step-bunching on the wafer surface after the implant annealing is also expected to significantly influence the μ_{eff}, as well as the reliability of the gate oxide. In the case of power lateral MOSFETs with implanted drift region, the surface roughness caused by the post-implant anneal is also expected to suppress the current flow near the surface of the implanted drift region.

In this chapter, we discuss the results of high-voltage 6H-SiC LDMOSFETs that was for the first time successfully annealed at 1600ºC in Ar with silane-overpressure to activate the n-type implants without degrading the surface morphology. The comparisons with a control wafer annealed in Ar without silane overpressure revealed different device characteristics at room temperature.

5.2 Design

The schematic cross-section of a typical lateral MOSFET built on a conducting p-type substrate is shown in Fig. 5.1. The device shown in this figure differs from the MOSFETs discussed in Chapter III because in addition to the lateral drift region, it also contains a vertical $n^+ - p - p^+$ drain-to-body diode. This means that the design rules derived earlier for lateral super-junction devices are not applicable in this case, because the drain-to-body diode requires a thick base layer in order to withstand the high bias applied under the off-state conditions.

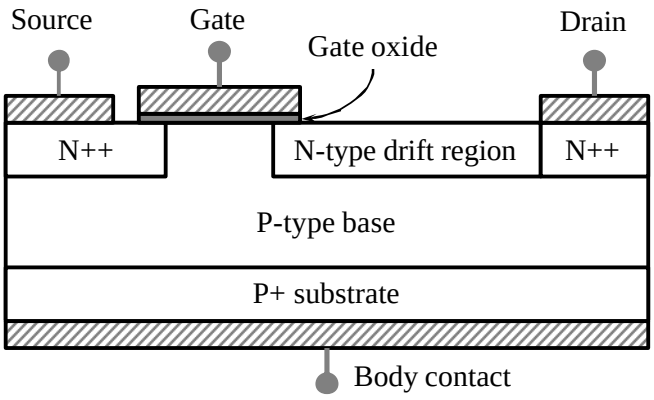

Figure 5.1: Schematic cross-section of lateral MOSFET on a conducting substrate.

There are several limitations imposed on the doping of this base layer. First, it should be high enough to prevent the channel punch-through at a targeted blocking voltage. Second, it should be low enough to minimize the threshold voltage, and to provide sufficient breakdown strength of the diode. It can be noticed, that the n-type implanted lateral drift region may serve as a Junction Termination Extension for the $n^+ - p - p^+$ diode. However, the set of quasi-empirical design rules for vertical

unipolar JTE-terminated devices derived in Chapter II cannot be used for this structure. Under the off-state conditions, the drift region that serves as a JTE region for the vertical diode forms an abrupt reverse biased junction with the gate electrode, which should also be terminated. There are two approaches to resolve this issue. First, the doping of the drift region may be reduced so that the field peaks at both junctions would not exceed the allowed values. This, however, will result in a significant increase in the drift resistance. The other approach is to employ one of the techniques discussed in Chapter II to eliminate field enhancement at the gate-to-drift junction. The theoretical investigation on the reduction of the surface electric field in lateral MOSFETs using high-k dielectric was conducted by Chen [11]. An example of using field plates in 4H-SiC lateral MOSFET can be found in [5].

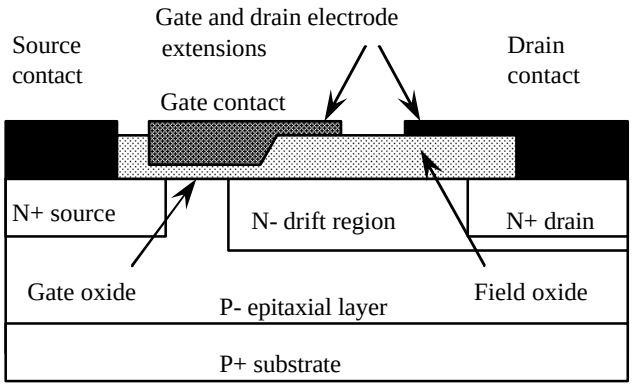

Figure 5.2: Schematic cross-section of the designed lateral 6H-SiC MOSFET.

In the present work, the field-plate approach was chosen as more manufacturable. Fig. 5.2 shows a schematic cross-section of the designed lateral MOSFET structure with drain and gate extensions over the field oxide. Two-dimensional device simulation was performed using MEDICI™ software in order to

optimize the device parameters, such as the doping of the drift region and the lateral extensions of the gate and drain electrodes.

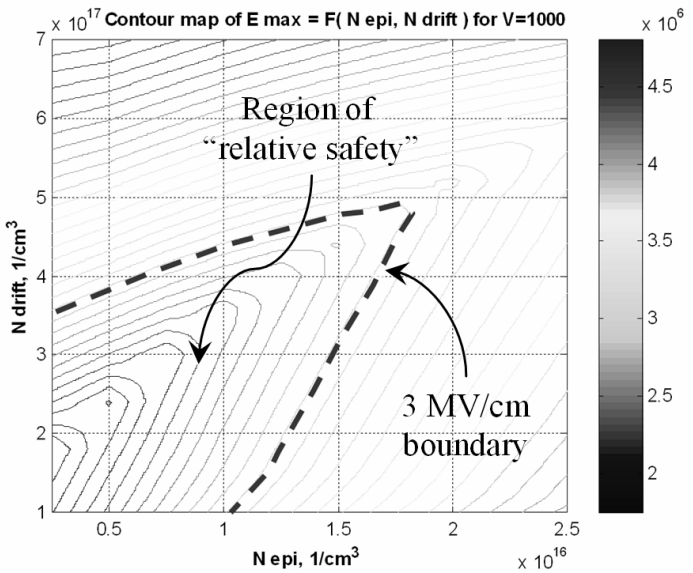

Figure 5.3: Contour map of the maximum electric field in the device bulk as a function of doing concentrations.

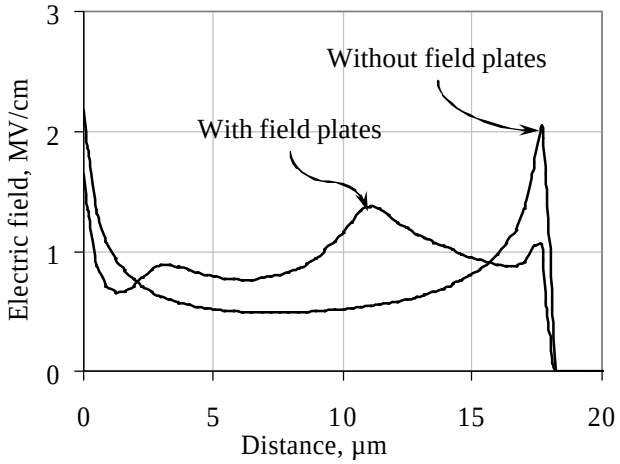

Figure 5.4: Simulated distribution the surface electric field along the drift region.

It should be mentioned, that while the implanted profile was typically uniform across the wafer, the acceptor concentration uniformity in the low-doped p-type

epitaxial layer was much less controllable and varied in a wide range. In our case, the doping concentration in the p-type base layer epitaxially grown in a cold-wall research reactor varied from $2x10^{16}$ cm^{-3} to $7x10^{16}$ cm^{-3}. In order to determine a region of "relative safety" for the implantation dose, a massive simulation was done for the different values of the base and drift doping concentrations. Fig. 5.3 shows a contour map of the maximum electric field in the device bulk simulated as a function of n- and p-type doping concentrations. Fig. 5.4 shows the effect of field plates on the simulated distribution of the surface electric field in the designed device structure.

5.3 Fabrication

Four p-type 35-mm 6H-SiC Si-face substrates, 3.5° off-axis toward $[1\bar{1}20]$ orientation, doped at $5x10^{18}$ cm^{-3} were obtained from Cree, Inc. Ten micrometers thick epitaxial layers were grown at atmospheric pressure in our horizontal cold-wall SiC CVD reactor at a growth temperature of 1600°C. Hydrogen was used as a carrier gas and silane and propane as precursors. The full growth procedure was described elsewhere [12]. C-V measurements were used to extract the net doping concentration in the range of $2\text{-}7x10^{16}$ cm^{-3} across the four wafers. Additional Secondary Ion Mass Spectroscopy (SIMS) data confirmed the uniform doping concentration of aluminum (p-type dopant) versus thickness. After the CVD growth and epi characterization, 2.0 μm of SiO_2 was deposited, densified, patterned, and selectively etched before the nitrogen source/drain implant. The source/drain implant was done at 1000ºC, with a total dose of 4.7×10^{14} cm^{-2} and implant energy schedule of 25, 50, 87, 137, 280, and 380 keV. After implant, the oxide was stripped and the process repeated for the nitrogen drift implant with the same energy schedule, but the dose was reduced to

1.32 x 10^{13} cm^{-2}. After drift region implantation, the oxide mask was again stripped, and the wafers were annealed for 30 min. at 1600ºC. Three wafers were annealed in Ar ambient with silane overpressure, as reported elsewhere [8], while the fourth wafer was annealed in argon ambient without silane overpressure.

The surface morphology of the wafers was examined using Atomic Force Microscopy (AFM) after the implant activation and before the subsequent thermal oxidation. The AFM surface plots shown in Fig. 5.5 compare one of the wafers annealed with silane overpressure and the wafer that was annealed without silane overpressure. The plots show the surface of the n^+-implanted regions, n-type drift regions, and regions with no implant. As shown in Fig. 5.5 (a), the wafer annealed in the argon ambient exhibited significant surface roughness, or step-bunching. The average height of the steps was measured to be 25 nm, even on un-implanted surfaces (*i.e.* similar to the un-implanted channel regions), and the average distance between the steps was estimated to be 1.0 μm.

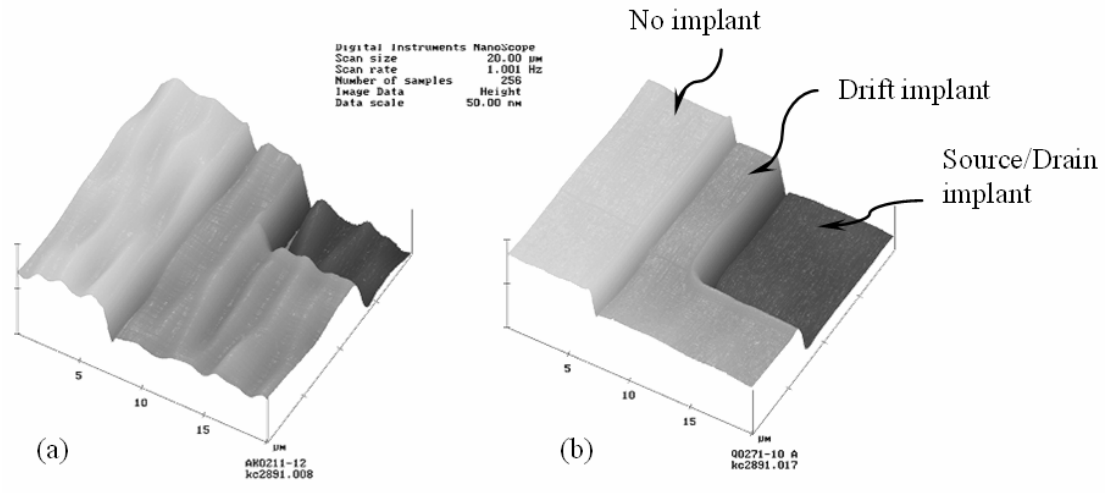

Figure 5.5: AFM images of 6H-SiC surface after post-implantation anneal performed in argon without silane overpressure (a) and with silane overpressure (b).

As discussed earlier, such rough surface is expected to impact the inversion-layer charge transport, and affect the reliability of the gate oxide. The step-bunching was more pronounced on the implanted surfaces, which could impact charge transport in the drift-region. A the same time, as shown in Fig. 55 (b), the sample annealed with silane overpressure demonstrated negligible surface roughness as compared to one annealed in argon ambient.

After annealing, the wafers were thermally oxidized and then coated with a high-temperature deposited oxide for a total passivation oxide thickness of 1.0 μm. This oxide was selectively wet etched back to the bare SiC to form the active regions of the devices. The 40 nm gate oxide was then grown at 1100ºC in steam ambient, followed by a 950ºC re-oxidation anneal. A Mo gate electrode was deposited and patterned, followed by an additional 0.6 μm of inter-level oxide deposition. After densification at 925ºC in nitrogen, source/drain and backside body contacts were formed using nickel-based ohmic contacts. The optical images of the fabricated 6H-SiC lateral MOSFETs are shown in Fig. 5.6.

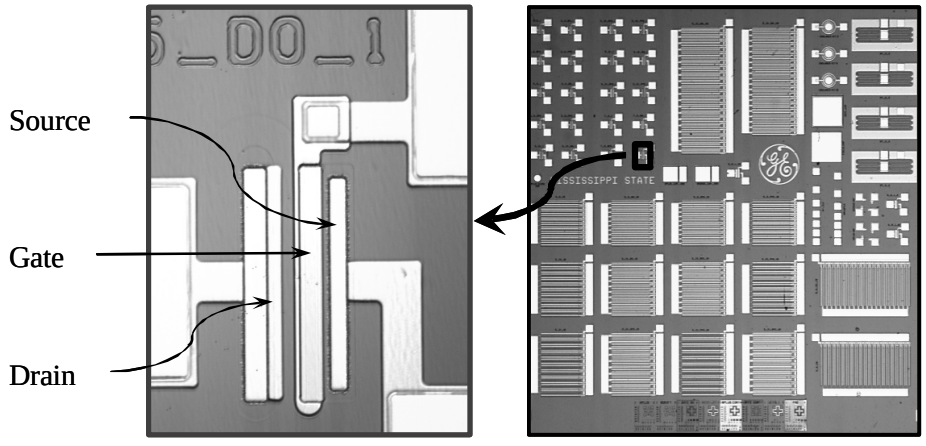

Figure 5.6: Optical images of the fabricated 6H-SiC MOSFETs.

The photograph on the left side of Fig. 5.6 shows a single-finger device with the gate width/length ratio of 112/5 (μm/μm), and the drift length of 9 μm. The right image shows the fabricated die that accommodated both single- and multi-finger devices along with various test structures. The gate lengths (L) were set at 3, 5, and 7 μm, while the gate width (W) of single-finger devices was 112 μm. Multi-finger devices (up to 20 fingers) were also employed for a higher effective W/L. The drift region length (L_D) was set at 9, 15, or 21 μm, which included 3 μm of gate oxide overlap onto the drift region.

5.4 Results and Discussion

After the fabrication had been completed, current-voltage measurements were carried out using Keithley 237 and 238 SMUs. The breakdown voltages were measured up to 600 V for the devices with 9 μm drift region length. Figure 5.7 shows I-V characteristics for a typical single-finger MOSFET with W/L of 112/5 (μm/μm). In the on-state, this small device had a drain current I_{DS} of 4.2 mA at V_{DS} of 10 V and V_{GS} of 24 V (5.85 MV/cm on gate oxide). Larger area 20 finger devices with 21 μm drift region length exhibited blocking voltage over 500 V and I_{DS} of more then 0.7 A at V_{DS} of 20 V and V_{GS} of 25 V. Typical families of curves for large 21-μm drift region devices in both kinds of wafers are shown in Fig. 5.8. Because in the long drift regions charge transport occurs mainly near the surface, significantly larger current exhibited by the devices fabricated on the wafers annealed using silane overpressure may be attributed to the negligible surface roughness of those wafers.

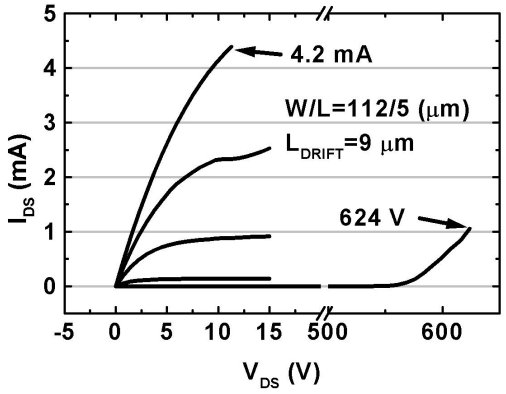

Figure 5.7: I-V characteristics of a single-finger MOSFET with W/L of 112 / 5 (μm/μm).

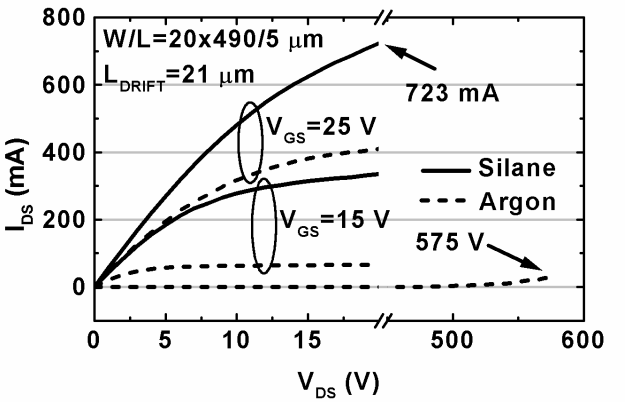

Figure 5.9: Comparison of I-V characteristics measured on large devices fabricated with and without silane-overpressure anneal.

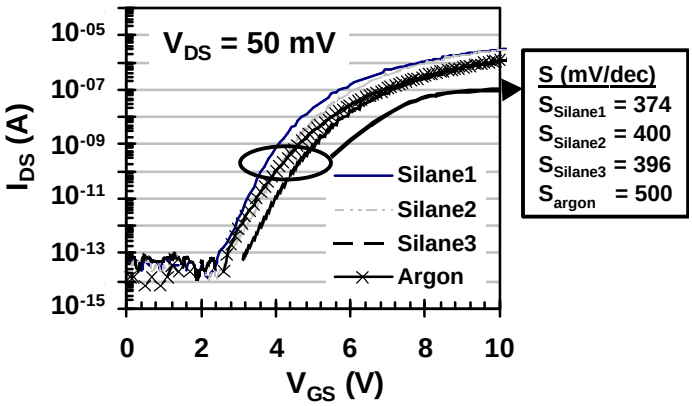

Figure 5.8: Typical linear region (V_{DS} = 50 mV) transfer characteristics of the fabricated MOSFETs measured at room-temperature, and a summary of the average inversed subthreshold slope measured on each substrate.

The effective channel mobility (μ_{eff}), extrinsic linear-region peak transconductance (g_m), and threshold voltage (V_{TH}) were extracted from the measurements done on MOSFETs without drift region and with the gate length L of 10 and 20 μm. As shown in Fig. 5.9, both the g_m and μ_{eff} were extracted from linear region transfer characteristics with V_{DS} = 50 mV. The average values and standard deviations for the extracted parameters from silane-overpressure and pure argon annealed 6H-SiC MOSFETs are summarized in Table 5.1. As shown Table 5.1 and Fig. 5.9, the devices measured on the substrate annealed in Ar ambient demonstrated lower average effective channel mobility and maximum transconductance than on any of the silane-annealed wafers. As shown in Table 5.1 and Fig. 5.8, using silane overpressure post-implant anneal increases the average effective channel mobility by 30% in comparison with the wafer annealed in pure argon, and more significant increase of drain current in the devices with long drift regions.

Table 5.1: The average and standard deviation for the extracted parameters from silane-overpressure-annealed and argon-annealed 6H-SiC MOSFETs.

Wafer ID	$\mu_{eff}, \left[\frac{cm^2}{V \cdot \sec^2}\right]$ (mean)	$\mu_{eff}, \left[\frac{cm^2}{V \cdot \sec^2}\right]$ (st. dev.)	$g_m, \left[\frac{\mu S}{mm}\right]$ (mean)	$g_m, \left[\frac{\mu S}{mm}\right]$ (st. dev.)	V_{TH}, [V] (mean)	V_{TH}, [V] (st. dev.)
Silane1	42.7	7.54	12.8	8.4	12	2.12
Silane2	44.1	15.1	17.0	15.4	10.5	1.81
Silane3	35.2	7.54	11.2	9.6	13.3	2.17
Argon	30.0	10.4	9.5	5.9	13.4	1.9

It is difficult to draw a strong conclusion about the effectiveness of the edge termination technique designed in this work because of the uncertainty introduced by

the doping non-uniformity and the general material quality of the research grade 6H-SiC substrates purchased in 1999. However, as shown in Figs. 5.7, the small area devices demonstrated a non-destructive reversible breakdown at ~ 550 V that would not be possible without a working edge termination.

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CHAPTER VI

SUMMARY AND DIRECTIONS FOR FUTURE RESEARCH

6.1 Summary

This study pursued three major goals:

1. Better understand the issues behind the optimization of electric field distribution in the voltage blocking layers of SiC power devices required to reduce their resistance;

2. Derive compact analytical rules for the optimal design of wide spectrum of the power SiC devices without conductivity modulation in the voltage blocking layer;

3. Determine the best edge termination approach for SiC vertical power devices in terms of performance, reproducibility (scalability), and cost-efficiency.

In order to accomplish the first task, the effect of the electrical field enhancement at the junction discontinuities and its impact on the on-state resistance of power semiconductor devices was investigated. A systematic analysis of the mechanisms behind the techniques that can be used for the edge termination in power semiconductor devices was performed. The influence of the passivation layer properties, such as effective interface charge and dielectric permittivity, on the devices with different edge terminations was analyzed using numerical simulation.

When pursuing the second goal, the following was accomplished. A compact analytical expression for the optimal JTE dose was proposed for the first time. This expression has been numerically evaluated for different targeted values of the blocking voltage and the maximum electric field, always resulting in the optimal field distribution that does not require further optimization with 2-D device simulator. A compact set of rules for the optimal design of super-junction power devices was developed. Compact analytical expressions for the optimal dopings and dimensions of the devices employed the field compensation technique are derived and validated with the results of numerical simulations on practical device structures.

The third goal was achieved through a comparative experimental study of several approaches used for the edge termination in SiC power diodes and transistors. The investigated techniques included the mesa termination, novel high-k termination, JTE, and the combination of JTE and field plate edge termination. Although the experimental study was not systematic because it was done on different projects, the mesa edge termination found to be the most promising among the techniques investigated in this work. This stand-along technique satisfied all the imposed requirements: performance, reproducibility (scalability), and cost-efficiency. First of all, it resulted in the maximum one-dimensional electric field (E_{1DMAX}) at the main device junction equal to 93% of the theoretical value of critical electric field in 4H-SiC. Secondly, the measured E_{1DMAX} was found to be independent of the voltage blocking layer parameters that demonstrate the scalability of this technique. Lastly, the implementation of this technique does not require expensive fabrication steps, and along with an efficient use of the die area results in the low cost and high yield.

6.2 Directions for Future Research

Although the mesa edge termination was shown as the most promising edge termination technique in SiC power devices, the results of numerical simulation suggest that its performance is vulnerable to the properties of the surface passivation. Since no experimental investigation of effective interface charge along the mesa sidewalls was done in this work, this potential issue should be addressed in the future research efforts. The ideal passivation of the mesa sidewalls should comply with the following requirements:

1. The maximum electric field in SiC at the mesa sidewalls is less than E_{1DMAX};
2. Reproducible definition of net surface charge on the mesa sidewalls;
3. High-temperature and high-voltage pulse stability;
4. High dielectric breakdown strength to prevent a device failure due to electrical discharges (arcing) between the metal contact and passivated SiC surface;
5. Compatibility with the overall fabrication process.

The future research should also investigate the applicability of mesa edge termination in different SiC device structures including power rectifiers and switches.

Analytical design rules derived for the field compensated structures in Chapter III could be expanded for the case when a tilted field distribution along the auxiliary junction is desirable. The sensitivity of the electric field distribution on the variations in the doping concentration and thicknesses of the drift and auxiliary region(s) should be also investigated.

APPENDIX

SILICON CARBIDE MATERIAL PROPERTIES

Table A.1: SiC material properties comparing to other major semiconductors.

Property\Material	4H-SiC	6H-SiC	GaN	Si	GaAs
Thermal conductivity [W/cm*K]	4.9	4.9	1.3	1.3	0.55
Bandgap [eV]	3.26	3.0	3.39	1.1	1.4
Saturation field velocity [10^5m/s]	2	2	2.5 (peak)	1	2 (peak)
Low field electron mobility (300^oK, 1e16cm^{-3}) [cm^2/V*s]	980 (‖) 865 (⊥)	81 (‖) 405 (⊥)	~ 900	1224	6555
Dielectric constant	9.7	10	9.0	11.8	12.8
Critical electric field [MV/cm]	~ 3	> 2.4	~ 3	0.3	0.4
Direct/Indirect Bandgap	I	I	D	I	D
Commercially available substrates	4”	3”	n/a	12”	8”