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The Multiple Gate Mos-Jfet

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By

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A new multiple-gate transistor, the SOI MOS-JFET, is presented. This device combines the MOS field effect and junction field effect within one transistor body. Measured I-V characteristics are provided to illustrate typical modes of operation and the functionality associated with each gate. Two-dimensional simulations of the device's cross-section will be presented to illustrate various conduction modes under different bias conditions. Test results indicate the MOS-JFET is well suited for both high-voltage and low-voltage circuit demands for systems-on-a-chip applications on SOI technology. Analog building-block circuits based the MOS-JFET are also presented.

DEDICATION

I would like to dedicate my research in memory of the people injured or deceased on September 11, 2001. May we never forget and strive to achieve the astonishing amount of heroism and bravery shown that day.

ACKNOWLEDGEMENTS

I would like to thank several people who have helped me throughout my research. First, I would like to thank my wife for her guidance and support during my research, which is unmistakably the reason for my accomplishments. Secondly, admiration and gratitude are the least of the qualities I wish to express to Dr. Ben Blalock, major professor and friend. Dr. Blalock is recognized for the sacrifice of many hours to aid in the development of my comprehension of fundamentals. Dr. Blalock has also taught me valuable analog design experience. Next, I wish to acknowledge Dr. Bob Reese for his aid with this defense and digital design teachings. Dr. Reese has given me valuable experience in VLSI with challenging projects. I am also thankful for the device design teaching of Dr. Jeff Casady. I also wish to acknowledge Dr. Ray Winton for his advice on the modeling of transistors and the physics of devices. I wish to thank these committee members for their advice and time spent improving this thesis.

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CHAPTER I

INTRODUCTION

Field effect transistors (FET) are key elements in integrated circuit (IC) design today. This thesis introduces an innovative FET. The transistor presented in this thesis allows designers maximum channel control. This transistor combines the theory of the metal oxide semiconductor field effect operation (MOSFET) and the junction field effect operation (JFET); for this reason the device was named the MOS-JFET. This thesis expands upon the original work described in Blalock, Cristoloveanu, Dufrene, Allibert, and Mojarradi [1].

The research presented in this thesis has been developed through a variety of disciplines and collaborators. The present study started with the concept of an SOI (Silicon on Insulator) CMOS (Complimentary Metal Oxide Semiconductor) compatible JFET. This concept has spawned into the novel idea of the MOS-JFET.

The knowledge learned during research has aided in development of applications and ideas for the MOS-JFET. The major concentration of research has been SOI analog/mixed-signal devices and circuits. Primary design efforts have used partially-depleted (thick-film) silicon on insulator (SOI) technologies. These technologies include 0.8μm, 0.35μm, and 0.25μm.

The majority of previous research has dealt with analog/mixed-signal circuit design, analog/mixed-signal layout, testing development, data collection, test

instrumentation control, high voltage device design, model development, MOS-JFET circuit design, MOS-JFET device design, and documentation.

Knowledge and industry experience has been enhanced through collaboration with universities and companies. The universities include University of Idaho (high voltage circuit design and device development), Kansas State University (RF circuit design), University of North Carolina, Charlotte (low noise circuit design and low power circuit design), University of Arkansas (transducer circuit development), University of Tennessee (analog design), and Mississippi State University (Digital Design, analog/mixed-signal design and cadence tools). This work is sponsored in part by NASA/JPL and The Boeing Company.

SOI technologies and common FET devices used in today's IC industry are described in Chapter 2. Applications and characteristics of silicon on insulator technologies are described. The applications and definitions of today's common FET devices are explained. The question of why this research is being conducted is also summarized. Topics of future problems facing the IC design in the near and distant future are discussed. Explanations of why this research is needed and what problems the device can solve are presented.

Chapter 3, the main focus of the thesis, describes the MOS-JFET. The chapter also includes descriptions of device simulations and test results of the MOS-JFET. Also, a simple model of this device is also presented. Also presented are the common building blocks for analog and mixed-signal design using the MOS-JFET. This chapter shows circuit setup and test data using a single transistor circuit.

Finally, a summary of the MOS-JFET is provided in Chapter 4. This chapter summarizes the work and explores different applications for the future of this device. Also listed in the chapter are the contributions this device could make to the IC industry.

CHAPTER II

SILICON ON INSULATOR AND FIELD EFFECT TRANSISTORS

As technologies decrease in size, limitations of bulk silicon are rapidly approaching. Present semiconductor research has concentrated on new methods of "bending" these limits. Silicon on insulator (SOI) is a primary candidate for minimizing scaling limitations. Semiconductor research has also developed various types of FETs to suit the needs of ASIC (Application Specific Integrated Circuits) and SOC (System-On-a-Chip) development. This chapter explores the advantages and disadvantages of SOI and describes the various FET devices used in ASIC and SOC applications.

2.1. Silicon On Insulator (SOI)

Introduced as a radiation hard technology, SOI was first developed using silicon on sapphire wafers. Through innovations in fabrication techniques, the integrated circuit (IC) world is seeing SOI wafer markets and SOI fabrication facilities materialize in the semiconductor industry. Today the market for SOI mainly consists of silicon substrates with a buried oxide. SOI has spawned a new revolution in the IC industry.

SOI is proving to be the technology of the future. The radiation hard feature of SOI has a distinct advantage for space and military applications. SOI also offers a higher maximum temperature versus bulk silicon (350^{o}C vs. 250^{o}C). The bulk silicon industry has also gained interest as a result of SOI's improved sub-threshold slope [2], order of

magnitude reduction in S/D (Source and Drain) capacitance, reduced short channel effects [3], latch-up immunity, speed improvement (up to 30%)[2], reduced power consumption (up to 80%), and low voltage operation without circuit degradation [4].

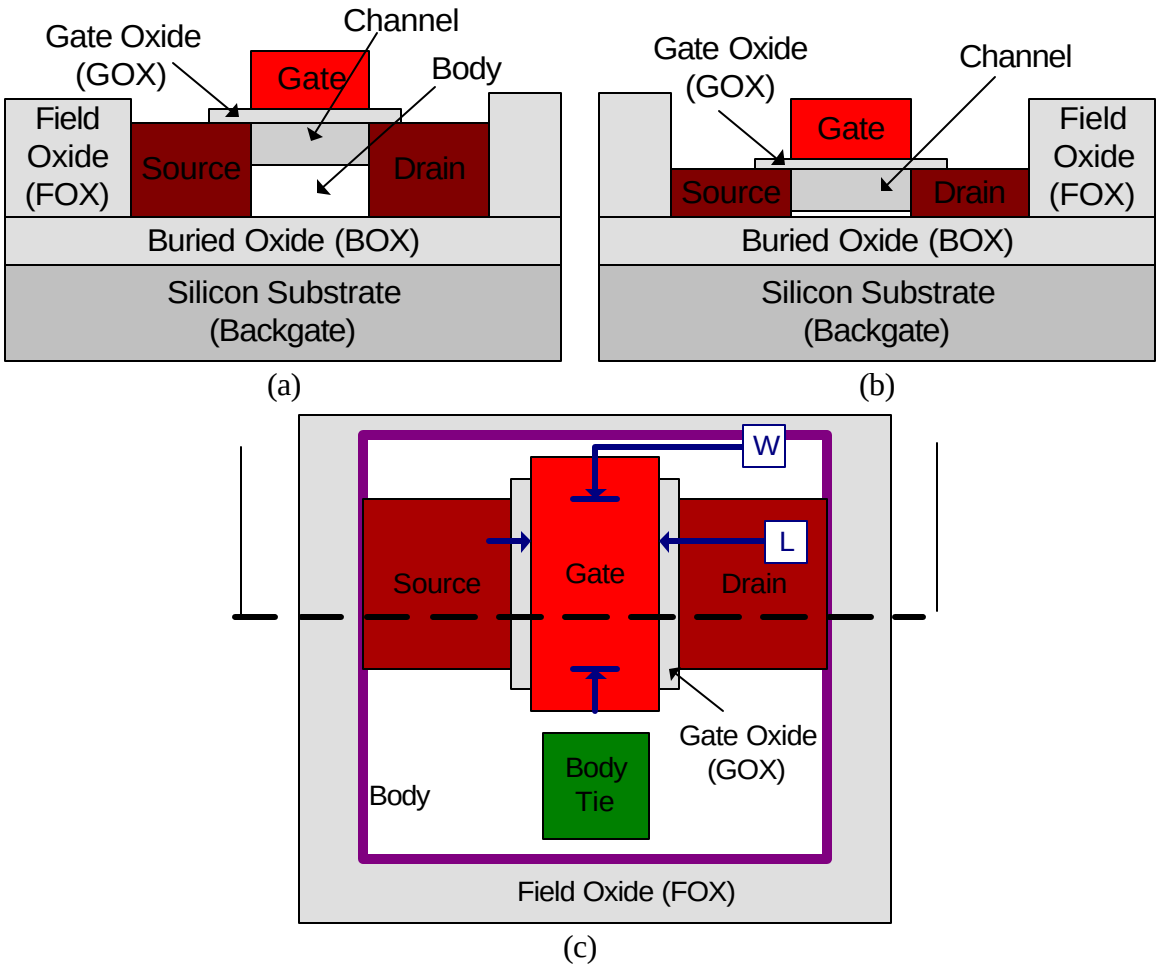


Figure 2.1. Cross section of SOI MOSFET.
(a) Partially-depleted cross section, (b) fully depleted cross section, and (c) aerial view with separate body tie connection.

Devices in SOI are classified by various qualities of the silicon island. SOI devices are classified using the terms partially-depleted (PD) or thick film, fully depleted (FD) or thin film, and buried oxide thickness variance. Figure 2.1 shows a cross section

of a partially-depleted SOI (PDSOI) device and fully-depleted SOI (FDSOI) device. The thickness of the film is determined by the Silicon thickness above the buried oxide. Thick film devices are approximately 200Å and greater. Thin film wafers are less than 200Å.

PDSOI offers distinct advantages over FDSOI and bulk CMOS. The PDSOI process can use bulk fabrication processes. Source and Drain resistance is lower than FDSOI. PDSOI devices have similar DC characteristics to bulk silicon when the body connection is used. The technology is also scaleable below 0.18μm. The radiation tolerance is high with the devices capable of handling up to 10Mrad permanent dose [2]. The major disadvantages are the floating body effects, when body connections are not used. Overshoot, undershoot, self-heating, and kink can become significant problems depending on the process development. Figure 2.2 shows these effects.

FDSOI devices offer better control of short channel effects than PDSOI. Threshold voltage reduction to 0.3V is possible. The body effects are minimal in the FDSOI since the transistor body is fully inverted in the "on" state. This technology is best suited for dual gate devices, using the buried oxide as an additional gate insulator. Problems exist with difficult scaling below 0.18um, modeling, and self-heating. Models are harder to construct because they are entirely based on the process (silicon thickness, oxide thickness, etc.). Scaling difficulties arise from raised S/D contact resistance and film thickness control.

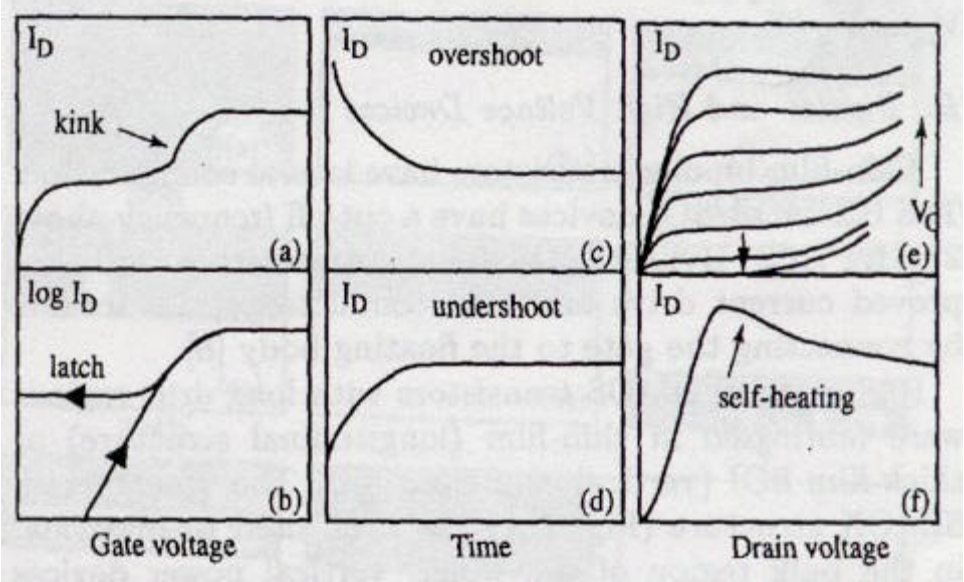


Figure 2.2. PDSOI disadvantages of floating body.
(a) Drain current IV kink, (b) latch in drain current vs. gate voltage, (c & d) overshoot and undershoot current, (e) premature breakdown, and (f) self-heating[2].

Fabrication vendors currently sell SOI products and fabrication opportunities to the public. MIT Lincoln Lab offers a FDSOI 0.18µm process. Peregrine offers a SOS 0.50µm process. Honeywell offers MOI (PDSOI) 0.35µm process.

SOI shows great promise for future scaling of CMOS. SOI's future will depend on research of compounds and lithography just as with bulk silicon in the realm of nanometer feature sizes. The difference is that SOI offers entirely new possibilities with device design and device development. A few devices in recent publications are multiple layer SOI [5], four control gate FETs [1], two control gate FETs, and quantum wire FETs [6]. These devices are all possible in SOI.

2.2. State-of-the-Art FET Devices

Diverse applications in the IC industry have produced various types of FET devices. Some of these FET devices are gate all around (GAA), dual gate, low voltage, high voltage, and high speed [6]. These new devices involve various layout and process changes. Many foundries concentrate on the low voltage or high speed FET devices. GAA, dual gate, and high voltage are FET devices currently being optimized in research fields.

The GAA FET is a FET that completely surrounds the channel with a poly gate from all four sides. This allows for improved current drive through volume inversion, improved short channel effects, and nanometer electronic applications. Fabrication difficulties have been a major stumbling block for wide spread device use. Despite these problems, the device shows promising quantum wire operation in future applications.

Dual gate devices are being explored to help cope with technology limits detailed in the semiconductor roadmap.[7] The dual gate transistor has higher current drive, improved (nearly ideal) sub-threshold slope, separate gate control, and improved short channel effects. Buried gate fabrication difficulties and channel thickness reliability are weak points of the device.

High voltage FET devices are crucial to mixed-voltage circuits and SOC applications that need high voltage interfaces. These devices are normally used to interface on-chip MEMS and off chip circuits using higher supply voltage. A common high voltage MOSFET is the double diffused MOSFET (DMOS). Design rule violations

and non self-aligned gate associated with the DMOS have caused matching problems and processing difficulties.

High speed FET devices, used for high speed digital, analog and RF (Radio Frequency) applications, tend to require unique process doping levels. Another solution is to have the process use a different semiconductor (i.e. SiGe and GaAs). These processes can be costly and hinder SOC applications.

Low voltage FET devices are the main drive of industry today. The devices are used for low voltage and low power applications. The main disadvantage is that when operating at low voltage, the speed of the transistor is limited. There are numerous applications for these transistors.

Table 2.1. Types of FET devices.

High Voltage FET	Low Voltage FET	High Speed FET	Non-Classical FET
Mixed Voltage Systems	Low Supply Voltage	Fast Digital Logic	Improved Current Drive
SOC Applications	Decreased Power Consumption	Increased Processor Speed	Improved Short Channel Effect
MEMs Control	Decreased Threshold Voltage	RF applications	Improved Subthreshold Slope

Various FET devices and applications are shown in Table 2.1. High speed FET category includes the high speed FET devices. The low voltage FET devices and high voltage FET devices are in low voltage and high voltage FET categories, respectively. The GAA FET device and dual gate FET device are included in the non-classical FET category.

2.3. Present Research Drive

The drive of material and device researchers today is to solve problems the semiconductor industry will face in the near and distant future. Major problems of the semiconductor industry are addressed in the 2001 Edition of the International Technology Roadmap for Semiconductor (ITRS) [7]. This roadmap addresses semiconductor industry challenges in the next 15 years. The Process Integration, Devices, and Structures (PIDS) section of the roadmap explores present research. Recently, PIDS has been expanded to include emerging research devices. These new emerging research devices include SOI, band engineered, vertical, FINFET, and double gate transistors. These transistors are possible solutions to lower power, higher speed, and increased transistor density applications [7].

The MOS-JFET has dual gate qualities and is fabricated on SOI technology. The MOS-JFET introduces a new method on decreasing density with multiple gate operation.

Table 2.1 shows the transistor divisions that have affected the idea of a complete SOC. This is a significant problem because of the issues with parasitic increase with the introduction of interfaces. Ideally, if everything would be on one chip, the system would depend on the optimum speed of the technology, not the interface. Thus, technology optimization is necessary. However, if the technology is faster than the interface or is not equipped to drive the interface, then the interface is the limitation of the technology. An ideal solution is a technology that offers all transistor divisions effectively. Unfortunately, this is not possible in most cases without costly process alterations.

Table 2.2. MOS-JFET Applications.

FET Divisions	MOS-JFET Characteristics
High Voltage FET	Mixed Voltage Systems SOC Applications MEMs Control
Low Voltage FET	Low Supply Voltage Decreased Power Consumption Decreased Threshold Voltage
High Speed FET	Fast Digital Logic Increased Processor Speed RF applications
Non-Classical FET	Improved Current Drive Improved Short Channel Effect Improved Subthreshold Slope

Present MOS-JFET research demonstrates strong potential for SOC applications. Table 2.2 shows where the MOS-JFET would fit into the divisions of transistors. The chart indicates that the MOS-JFET has many of the capabilities introduced by each division of the transistor chart without costly process changes. In short, the MOS-JFET offers the performance attributes of different FETs within a single device. The following chapter will show how the MOS-JFET has these capabilities using SOI technology.

This thesis will present the physical simulations and tested operation modes of the MOS-JFET device in Chapter 3. Chapter 3 will present the MOS-JFET used in common analog and mixed-signal building blocks. The building blocks will show that the MOS-JFET is not only functional, but also adds distinct advantages due to the multiple gate nodes.

CHAPTER III

THE MOS-JFET

The MOS-JFET is a new field effect transistor. As mentioned in the introduction, the MOS-JFET combines the junction field effect with the metal oxide semiconductor field effect within a single transistor body. This device is only possible in SOI. The MOS-JFET is derived from a SOI MOSFET layout with two body ties on either end of the poly gate as shown in Figure 3.1 (b). The figure shows the body as a conduction channel of the MOS-JFET. This means a n-channel MOS-JFET is derived from a p-type MOSFET, the MOS-JFET is an accumulation-mode device. The two junction field effect gates of the MOS-JFET are formed from the source and drain regions of the MOSFET layout (gates one and two). The poly gate of the MOSFET layout is the MOS-JFET's third gate. Using the poly gate allows the top portion of the MOS-JFET's body to be biased in depletion, neutral, or accumulation. The substrate beneath the buried oxide acts as a fourth gate and has a similar impact on the bottom portion of the MOS-JFET's body. In essence, the MOS-JFET device consists of a dual gate JFET and a dual gate MO structure to provide a remarkable four gate field effect transistor.

Figure 3.1 shows the top and side views of a MOS-JFET device. A PMOSFET layout translates into a n-channel MOS-JFET. The width and length dimension are reversible (see Figure 3.1(b)). The length and width of the MOS-JFET are normally the

width and the length of the MOSFET, respectively. Table 3.1 summarizes the transformation of the MOSFET layout to MOS-JFET device.

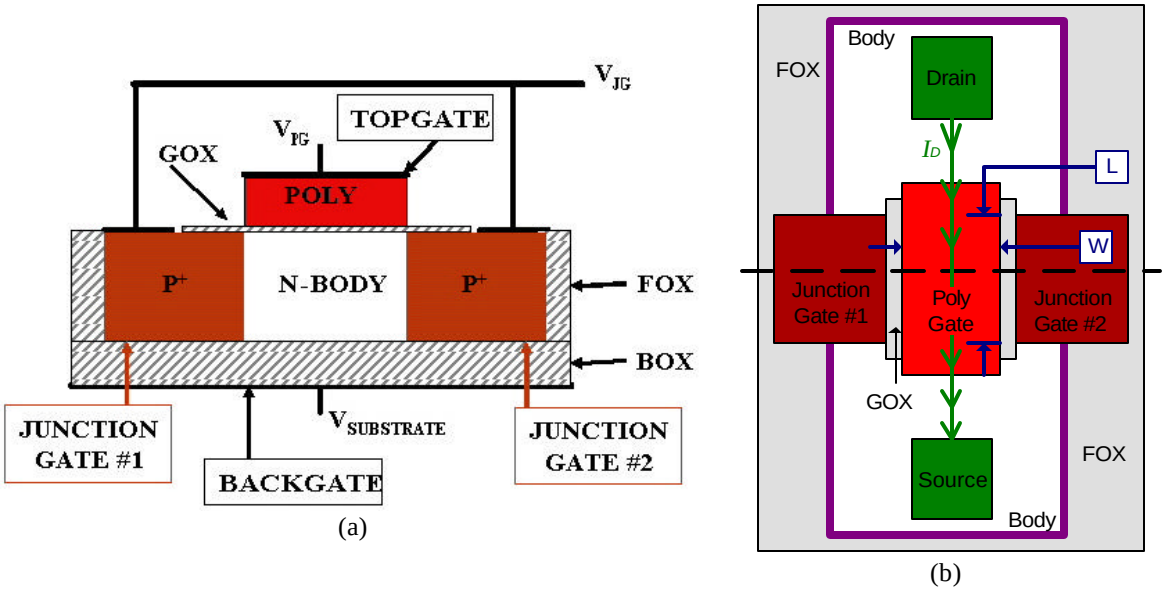


Figure 3.1. MOS-JFET structure.
(a) Cross-section and (b) top view.

Table 3.1. Transformation parameters from MOSFET layout to MOS-JFET.

MOSFET	⇔	MOS-JFET
PMOS	⇔	N-channel
NMOS	⇔	P-channel
Width	⇔	Length
Length	⇔	Width

A sample layout of the MOS-JFET is shown in Figure 3.2. An important feature of the layout is the intersection of the junction gates and the body tie region to ensure channel conduction solely underneath the poly gate.

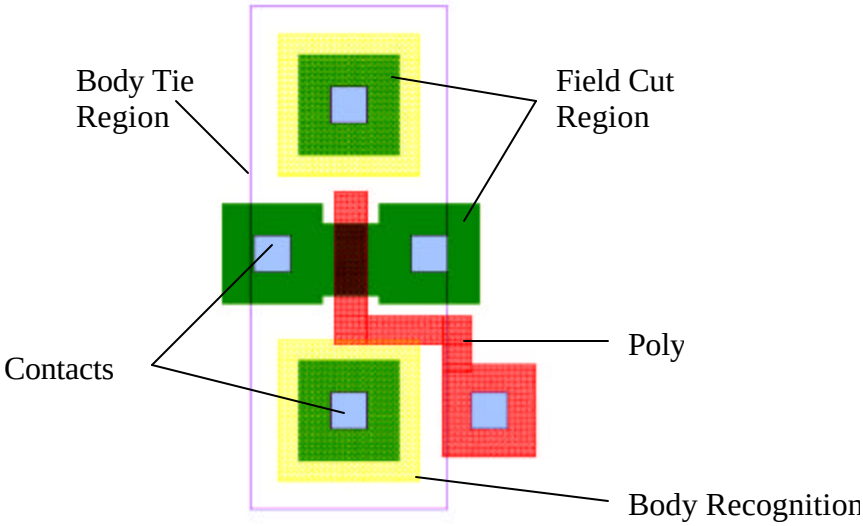


Figure 3.2. Sample layout of MOS-JFET.

The following sections describe the operational modes (Section 3.1.), two dimensional simulations (Section 3.2.), parameter extraction (Section 3.3.), and applications (Section 3.4.) of the MOS-JFET. The MOS-JFET applications listed in this thesis provide an early look at the numerous applications of this new device.

3.1. Operational Modes of the Multiple Gate MOS-JFET

The MOS-JFET has four possible gates. This section will show the functionality and highlight the modes of operation for the poly gate or top gate (V_{PG}), the back gate or bottom gate (V_{SUB}), and the junction gates (V_{JG}). The junction gates were connected together for simplicity. A schematic of the MOS-JFET is displayed in Figure 3.3 with the nodes labeled as described in this section. Each junction gate has nearly identical effects on the conduction channel, which will be shown in the applications section (Section 3.4). The device is fabricated from a commercial 0.35µm PD-SOI process with

a drawn channel width of 0.35µm and a drawn channel length of 1.5µm. Figures 3.4 through 3.11 show the normal operation modes of a n-channel MOS-JFET.

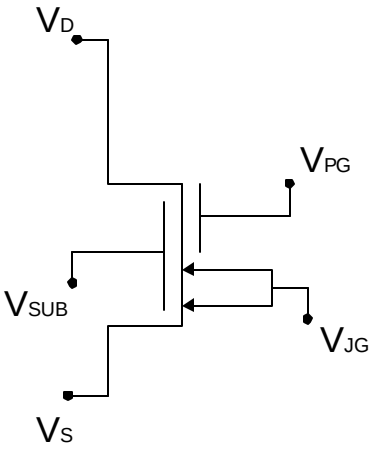


Figure 3.3. Schematic of MOS-JFET.

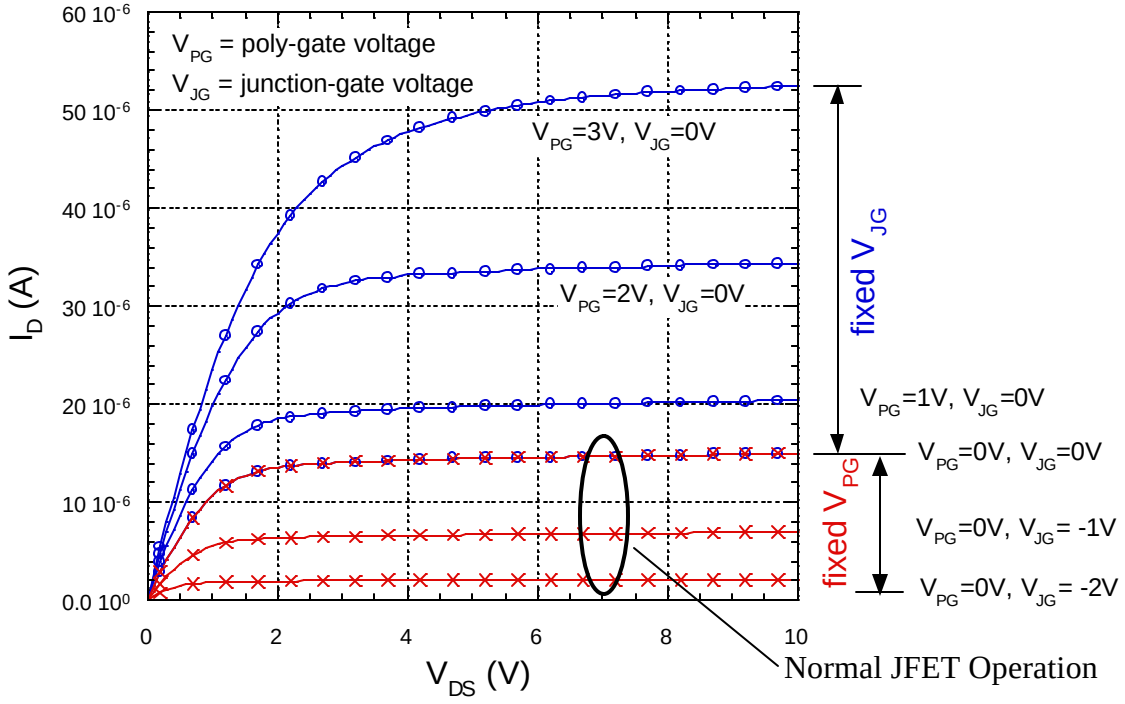
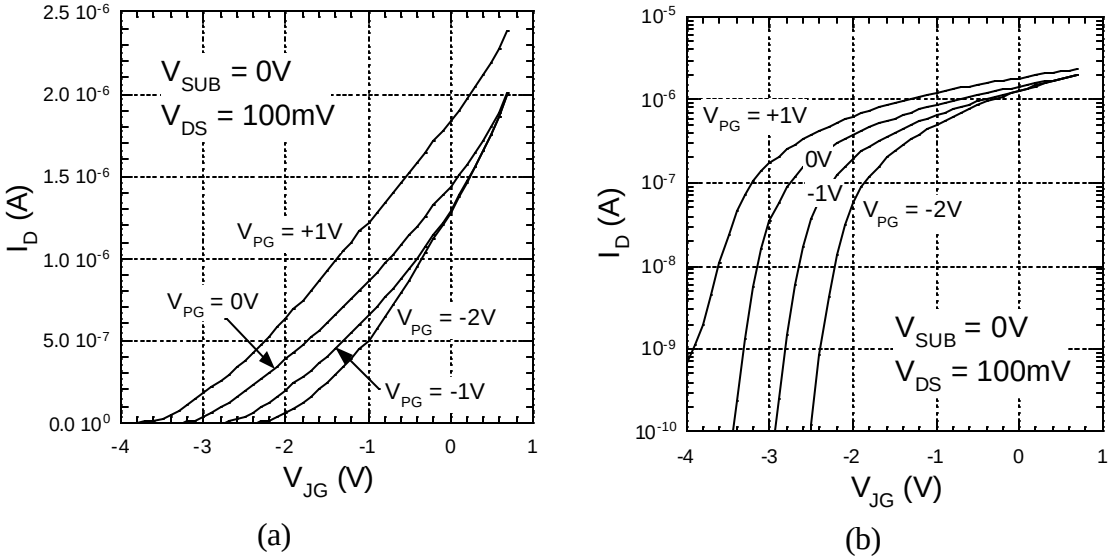


Figure 3.4. Measured ID vs. VDS for a n-channel MOS-JFET.
L=1.5µm, W=0.35µm, and VSUB=0V.

Figure 3.4 shows the current versus voltage (IV) curves of the MOS-JFET. The top gate (V_{PG}) is biased to 0V while the junction gates (V_{JG}) are biased from 0V to -4V in -1V steps for normal depletion mode JFET operation. Then V_{PG} is biased from 0V to 3V in 1V increments with V_{JG} biased at 0V to demonstrate enhanced current drive through top gate accumulation. The back gate (V_{SUB}) is biased at 0V for these measurements. The drain source voltage (V_{DS}) is swept from 0V to 10V. Notice there is no breakdown shown, which portrays the high voltage characteristics of the MOS-JFET. V_{DS} breakdown of this device is 11V and is shown in the applications section (Section 3.4.1).

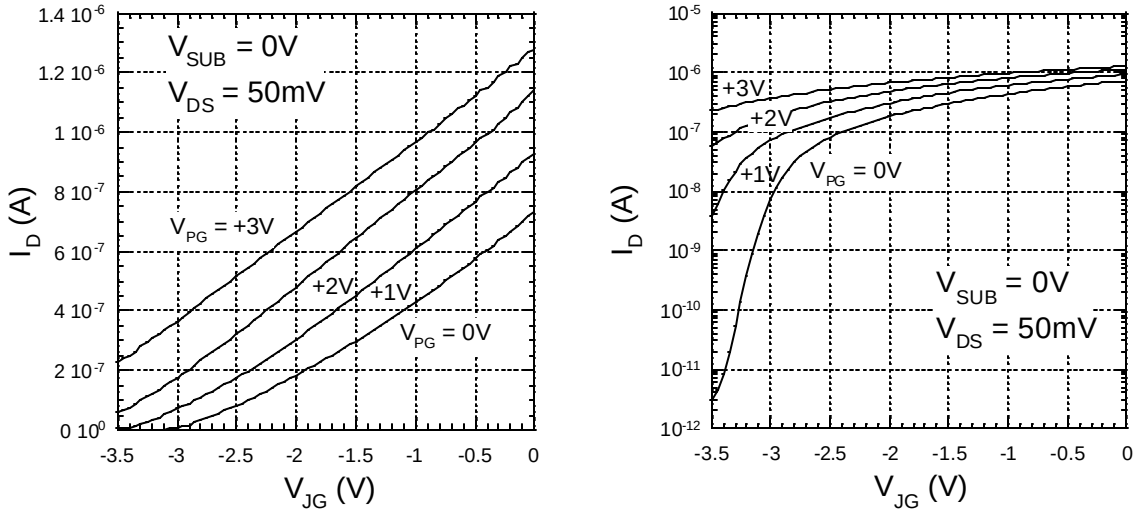
The drain current (I_D) versus gate voltage for the various gate bias conditions of the MOS-JFET will now be shown. The MOS-JFET's conduction characteristics during linear or saturation operation are provided under MOS (top or bottom) gate depletion or accumulation conditions. Figure 3.5 shows the MOS-JFET in linear operation (V_{DS}=100mV) with V_{PG} biased in accumulation (+1V) to depletion (-2V) mode. V_{JG} is swept from -4V to 0.5V in the figure. The figure shows V_P (pinch-off voltage) control with VPG in depletion or weak accumulation mode. Subthreshold characteristics are improved as poly gate depletion increases (see Figure 3.5(b)).

As the top gate enters accumulation, the MOS-JFET displays increased drain current, but at the expense of reduced subthreshold swing and increased pinch-off voltage magnitude. These characteristics are shown in Figure 3.6. I_D versus V_{JG} is plotted with V_{PG} swept into strong accumulation (0V to 3V).



(a) (b)

Figure 3.5. Linear operation with V_{PG} depleted to moderately accumulated. V_{JG} varied shown on (a) linear scale and (b) semilog scale.

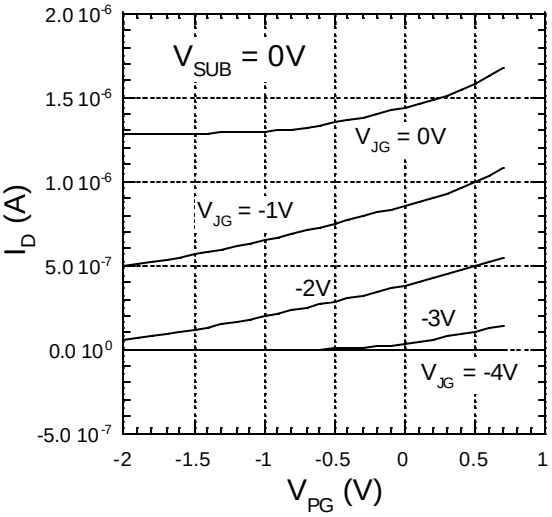


(a) (b)

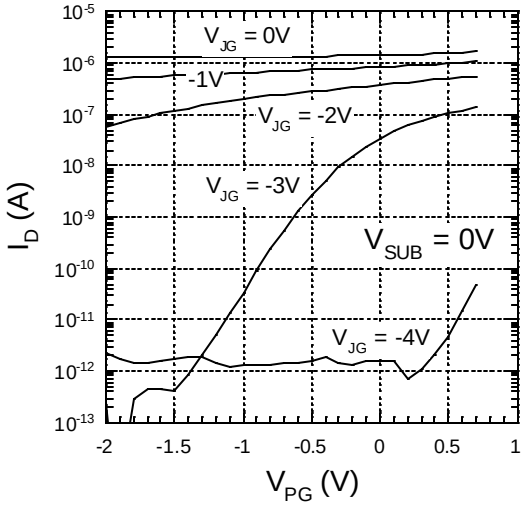
Figure 3.6. Linear operation with V_{PG} accumulated. V_{JG} varied shown on (a) linear scale and (b) semilog scale.

Figure 3.7 shows that device cut-off is achievable with V_{PG} when the junction gates are also depleted. However, Figure 3.8 shows that the device cannot be turned off when V_{PG} is in full accumulation, regardless of the junction gate bias. Transconductance of the MOS-JFET top gate is shown to increase as the amount of junction gate depletion

decreases (see Figure 3.9). The transconductance roll off as V_{PG} becomes deeply accumulated is related to MOS transconductance effects (such as carrier scattering).

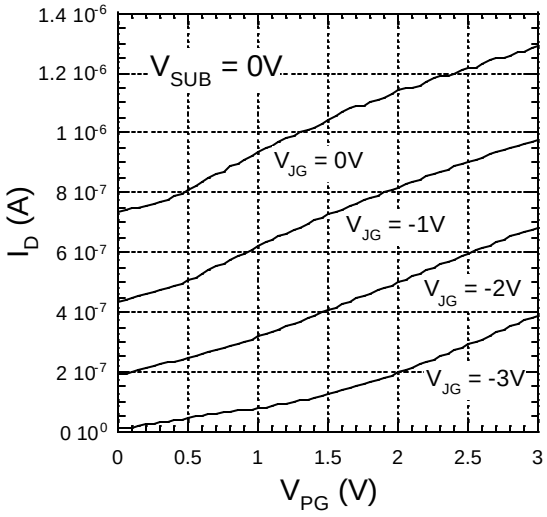


(a)



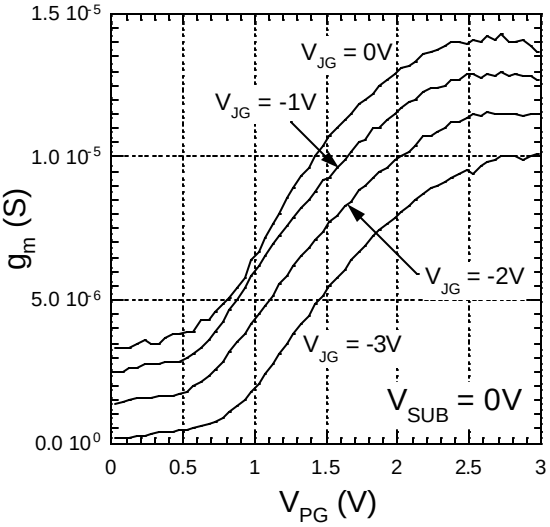
(b)

Figure 3.7. Pinch-off characteristics in linear operation of depleted V_{PG}. Shown on (a) linear scale and (b) semilog scale.



(a)

Figure 3.8. Incapability pinch-off characteristics in linear operation of accumulated V_{PG}.



(b)

Figure 3.9. V_{PG} transconductance (g_m) plot with V_{JG} varied.

The previous data was measured with the substrate (V_{SUB}) grounded. Figures 3.10 and 3.11 show the characteristics of V_{SUB} depleted (-20V) and accumulated (+20V). Large V_{SUB} gate voltages are needed because the buried oxide is considerably thicker than the top gate oxide thickness. With V_{SUB}=-20V, channel pinch-off is now achievable, even when V_{PG} is in moderate accumulation (see Figure 3.10(a)). Figure 3.10(b) shows junction gate transconductance curves for the MOS-JFET in linear operation.

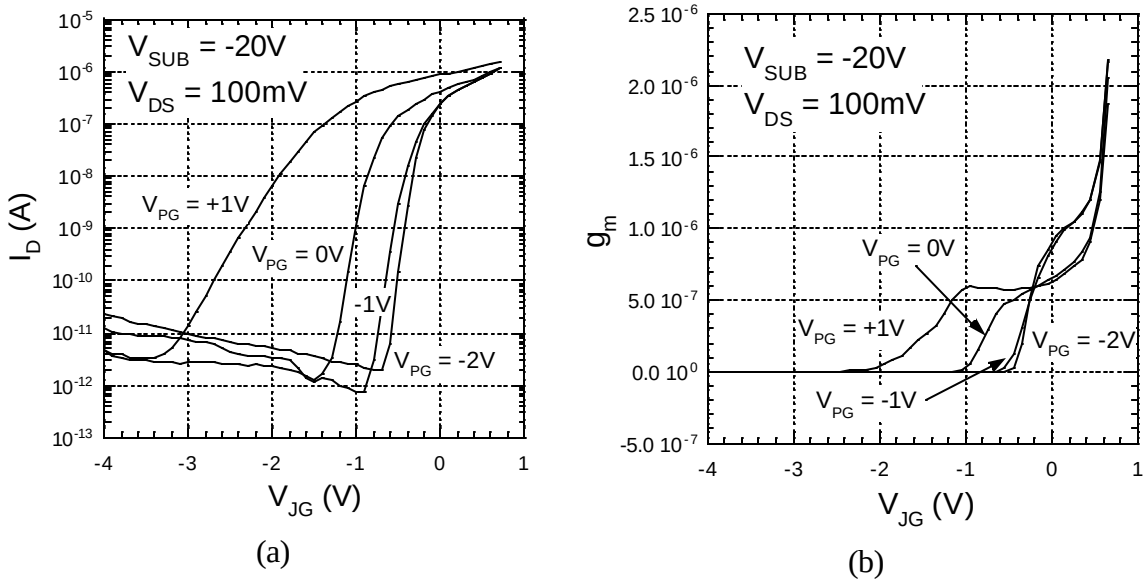
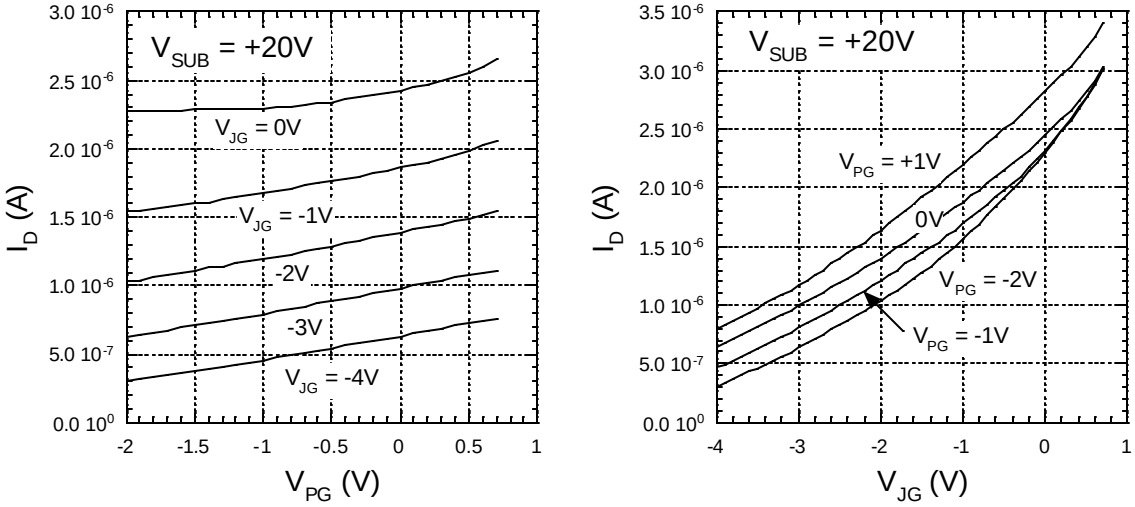


Figure 3.10. Measured (a) I_D versus V_{JG} (semilog scale) and (b) transconductance curves of V_{JG}.

As mentioned in Chapter 2, the dual gate MOSFET improves current drive (compared to single gate). Figure 3.11 shows this effect with V_{SUB} and V_{PG} in accumulation. The device is not capable of pinch-off, but V_{JG} and V_{PG} are able to modulate the current and large currents are possible.



(a) (b)

Figure 3.11. Accumulated V_{SUB} (+20V) showing increased channel conductance. (a) V_{PG} varied and V_{JG} incremented and (b) V_{JG} varied and V_{PG} incremented.

The previous figures (Figures 3.4 through 3.11) show that the MOS-JFET is capable of operating in multiple modes based on gate bias conditions. Figure 3.12 shows a p-channel MOS-JFET. As expected, the p-channel MOS-JFET has less desirable curves, analogous to normal p-channel JFET devices. The p-channel device breakdown is less than n-channel breakdown values (approximately 6V). Pinch-off control is difficult, but this should improve with technology scaling. Despite these disadvantages, the p-channel MOS-JFET shows full current control with all four gates.

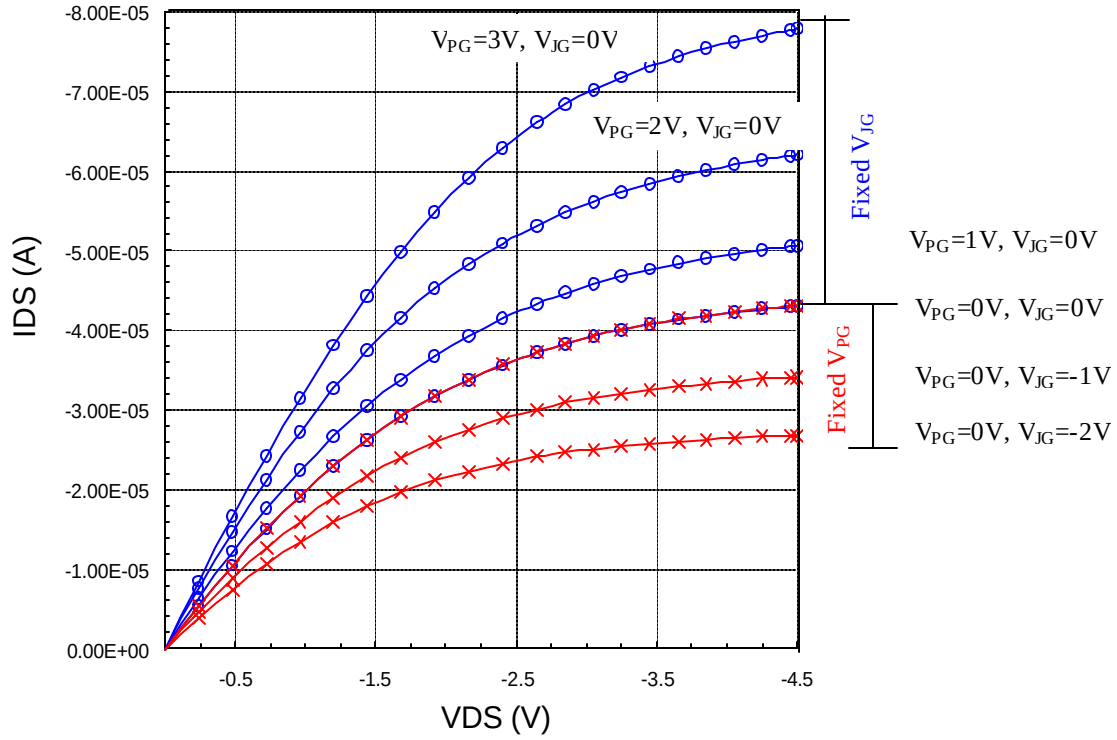


Figure 3.12. Measured ID vs. VDS for a p-channel MOS-JFET. L=1.5µm, W=0.35µm, and VSUB=0V.

3.2. 2-D MOS-JFET simulations

The MOS-JFET measured results prove that this device can be used for multiple operational modes, implying multiple applications. This section displays two-dimensional simulations for the device's cross section. Figures 3.13 through 3.17 will be used to describe the device physics and to visualize the ideal bias conditions for various device applications [1]. Long channel (10µm) and short channel (0.3µm) simulations are provided. The doping profiles were selected through an iterative process. Throughout the two-dimensional simulations the junction gates were again tied together for simplicity.

3.2.1. Long Channel simulations

Figure 3.13 shows a 2-D simulation of a wide channel MOS-JFET with neutral substrate biasing and the depletion substrate biasing. For wide channel devices, the figure shows the junction gates have minimal effect on the conduction channel. In each figure shown in this chapter, gray represents 'not depleted', white represents 'totally depleted', and black represents 'accumulated'. For the wide channel device, the conduction plane has two regions, the top and bottom channel. The wide channel device cannot be shut off, however, current modulation is possible with either the top (V_{PG}) or bottom (V_{SUB}) gate.

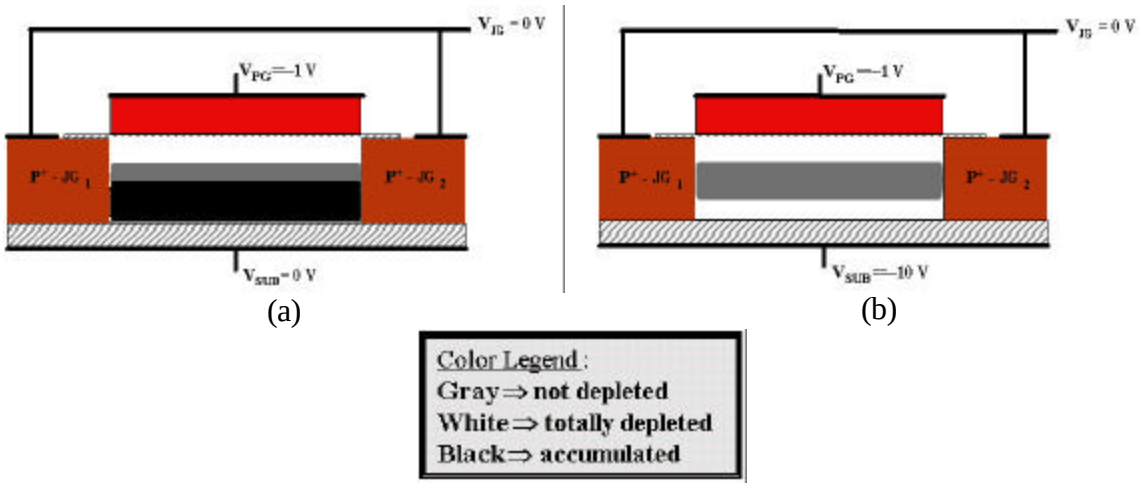


Figure 3.13. Wide channel simulations.
(a) Neutrally biased V_{SUB} (0V) and (b) depletion biased V_{SUB} (-10V).

3.2.2. Short Channel Simulations

Standard JFET structures with narrow channels show improved junction gate control. This also holds true for the MOS-JFET. Figure 3.14 shows the effect of V_{PG} when V_{JG} and V_{SUB} are neutrally (0V) biased. Accumulation (V_{PG}=0.5V), neutral

(V_{PG}=0V), and depletion (V_{PG}=-0.75V) bias levels of the top gate illustrates adjustment of channel conductance as the channel becomes narrow. The channel conducts in all bias conditions shown in Figure 3.14, showing good agreement with the measured results.

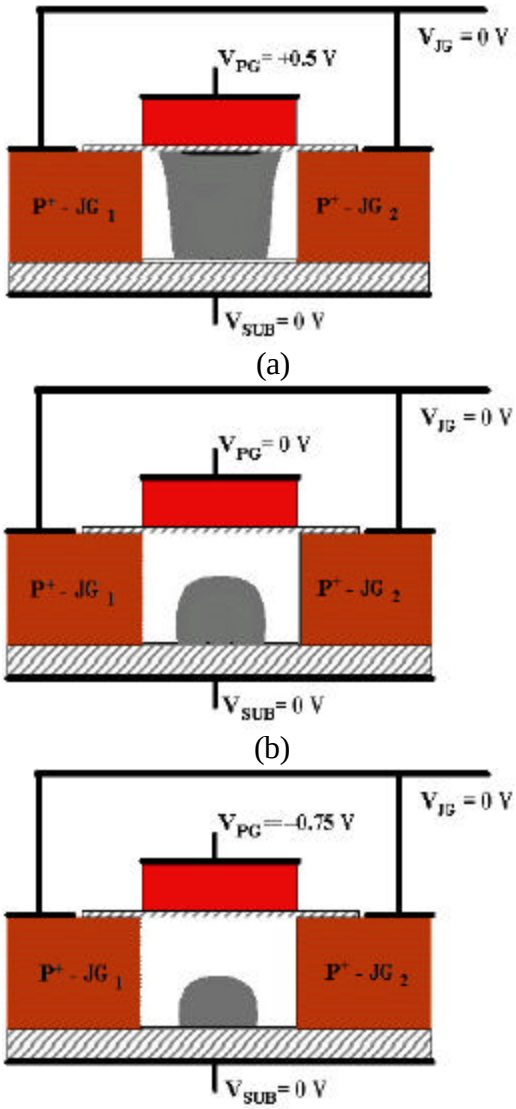


Figure 3.14. V_{PG} with (a) accumulation, (b) neutral, and (c) depletion biasing conditions and V_{SUB} and V_{JG} biased neutrally (0V).

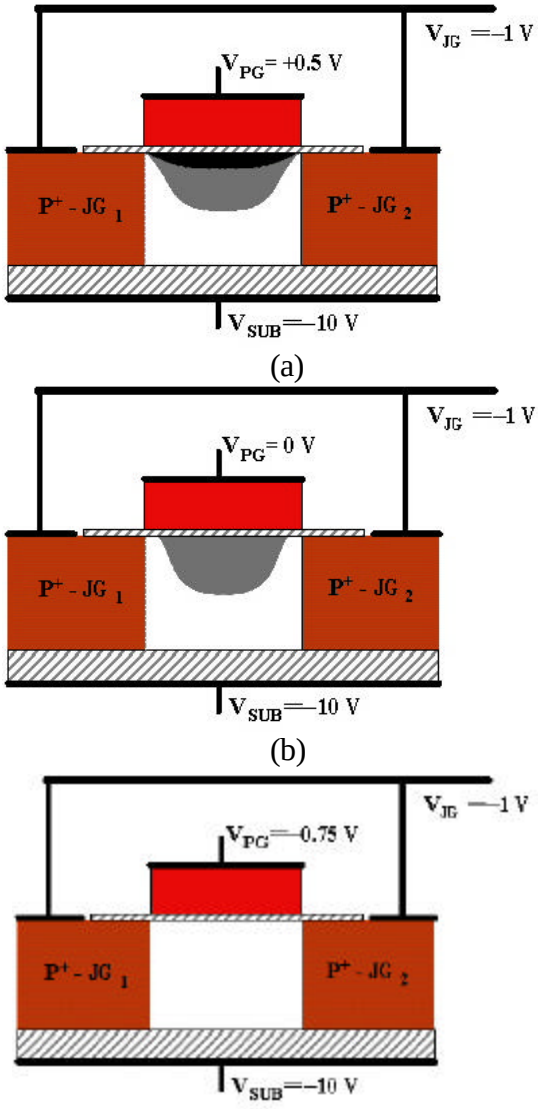
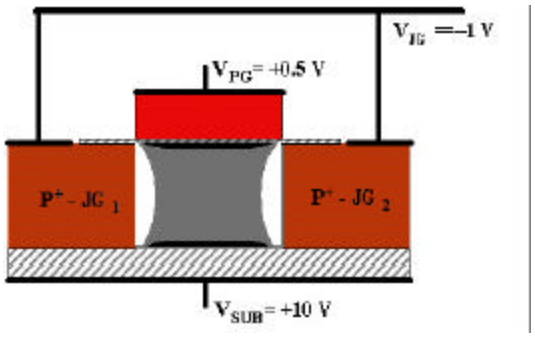
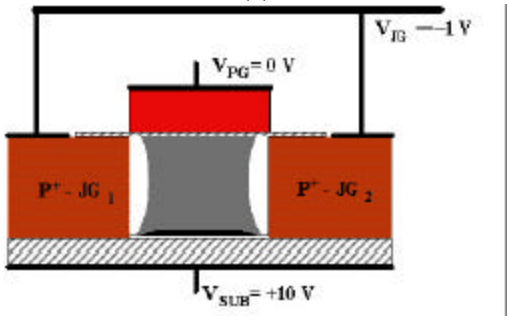


Figure 3.15. V_{PG} with (a) accumulation, (b) neutral, and (c) depletion biasing conditions and V_{SUB} biased neutrally (0V) and V_{JG} depleted (-1V).

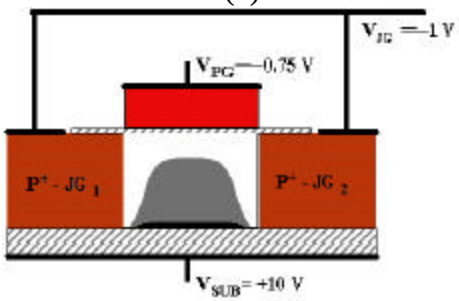
Figure 3.15 shows the same V_{PG} biasing but with V_{JG} depleted. This shows turn off via the top gate is possible when the junction gates are depleted. Also, the top gate is able to control current magnitude despite junction gate depletion. Figure 3.14 and Figure 3.15 develop the idea of two channels (top and bottom) with an added variable control (V_{JG}) for the top channel.



(a)

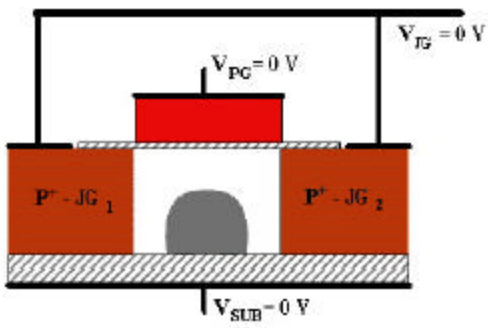


(b)

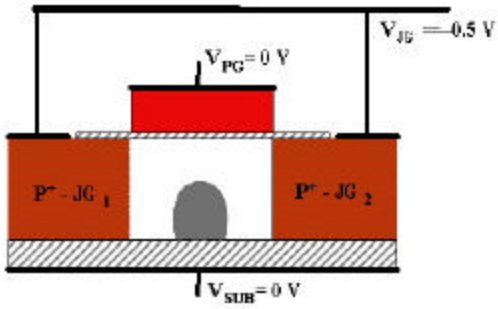


(c)

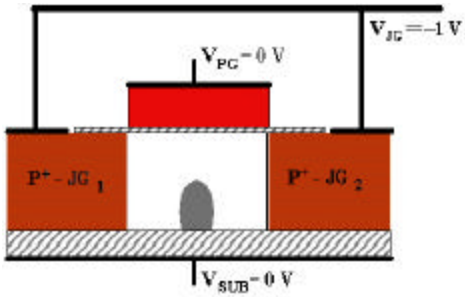
Figure 3.16. V_{PG} with (a) accumulation, (b) neutral, and (c) depletion biasing conditions and V_{SUB} accumulated (10V) and V_{JG} depleted (-1V).



(a)



(b)



(c)

Figure 3.17. V_{JG} (a) neutrally, (b) partially-depleted, and (c) near fully depleted biasing conditions with V_{SUB} and V_{JG} neutrally biased (0V).

Figure 3.16 shows similar control of the back channel with substrate biasing. The substrate bias is accumulating the bottom channel (V_{SUB}=10V). With the combination of the top channel and bottom channel, high current is possible. Figure 3.17 displays the effect of the junction gates biased into depletion, near device cut off. Figure 3.17 also shows how an electrically controlled wire with varying thickness is attainable, possibly providing a quantum wire.

3.3. MOS-JFET Parameters

A simple model was created to facilitate circuit design efforts using the MOS-JFET. The model presented is extracted using curve fitting techniques. Parameters shown in Table 3.2 are the extracted parameters for the model. These parameters were extracted with the junction gates connected together, V_{SUB}=0V, and V_S=0V.

Table 3.2. Extracted parameters for MOS-JFET.

Parameter Name	Parameter Symbol	Parameter Value
Effective Zero Bias Drain Current	I_{D0eff}	72.1 µA
Effective Pinch-off Field	E_{Peff}	-8.325104 V/µm
Drain Current Constant	k_{ID}	3.30787 µ
Pinch-off Voltage Constant	k_{VP}	-1.1
Effective Linear Slope	G_{0eff}	15 pA
Built-in Voltage Potential	V_{bi}	0.315 V
Fit Parameter	f_x	1 V
Channel Width	W	---------
Channel Length	L	---------
Junction Gate Voltage	V_{JG}	---------
Poly Gate Voltage	V_{PG}	---------
Drain Current in Saturation	I_{Dsat}	---------
Drain Current	I_D	---------

The saturation region was the first region to be extracted. The saturated drain current can be found using [8]

$$I_{Dsat} = I_{D0}(1 - \frac{V_G}{V_P})^2 \tag{3-1}$$

where:

I_{D0} = $I_{Dsat|V_G=0}$,

V_G = Gate Voltage,

V_P = Pinch-off voltage

This simple model was used as the base equation for the complete MOS-JFET saturation current model. For a V_{PG}=0V bias condition the following equation was used:

$$I_{Dsat} = I_{Deff} * (W/L) * (1 - \frac{V_{JG}}{E_{Peff} * W})^2 \tag{3-2}$$

Figure 3.18 shows four devices with varying channel length and constant channel width. The model derived for zero poly gate bias is fairly accurate. Since this n-channel model can only be used for zero poly gate bias, another model was created with respect to the poly gate to allow more complete utilization of the MOS-JFET's multiple gates.

The accumulation mode and the depletion mode of the poly gate have two different transconductance characteristics. For this work, poly gate accumulation mode was selected for modeling. By introducing new parameters for the poly gate, an equation was formed based on (3-1). Equation (3-3) shows the new parameters for the accumulated poly gate condition while equations (3-4) and (3-5) show the poly gate voltage influence.

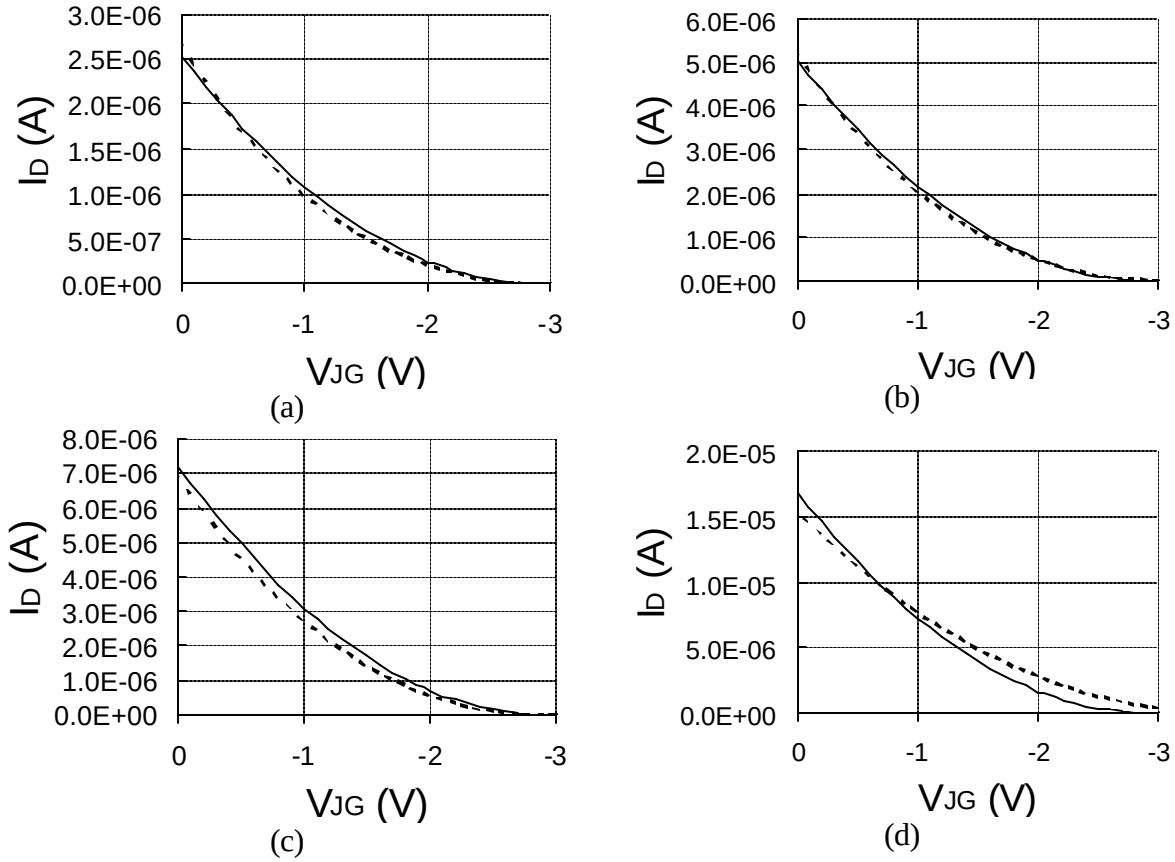


Figure 3.18. N-channel MOSJFET saturation model (——) versus measured (-----) data. For a constant channel width of 0.35µm and channel lengths of (a) 10µm, (b) 5µm, (c) 3.5µm, and (d) 1.5µm, respectively. For all cases, V_{SUB}=0V, V_D=3V, V_{PG}=0V and V_S=0V.

$$I_{Dsat} = I_{D0\,pg} * \left[1 - \frac{V_{JG}}{V_{Ppg}}\right]^2 \tag{3-3}$$

where

$$I_{D0\,pg} = I_{Deff} * (W/L) + \left(\frac{k_{ID}}{e^{j_x/V_{PG}}}\right) * V_{PG} \tag{3-4}$$

and

$$V_{Ppg} = E_{Peff} * W + \left(\frac{k_{VP}}{e^{j_x/V_{PG}}} - 1^{j_x/V_{PG}}\right) * V_{PG} \tag{3-5}$$

Figure 3.19 shows the measured data versus model solutions for a MOS-JFET with channel width and length of 0.35µm and 5µm, respectively, under accumulated poly gate conditions.

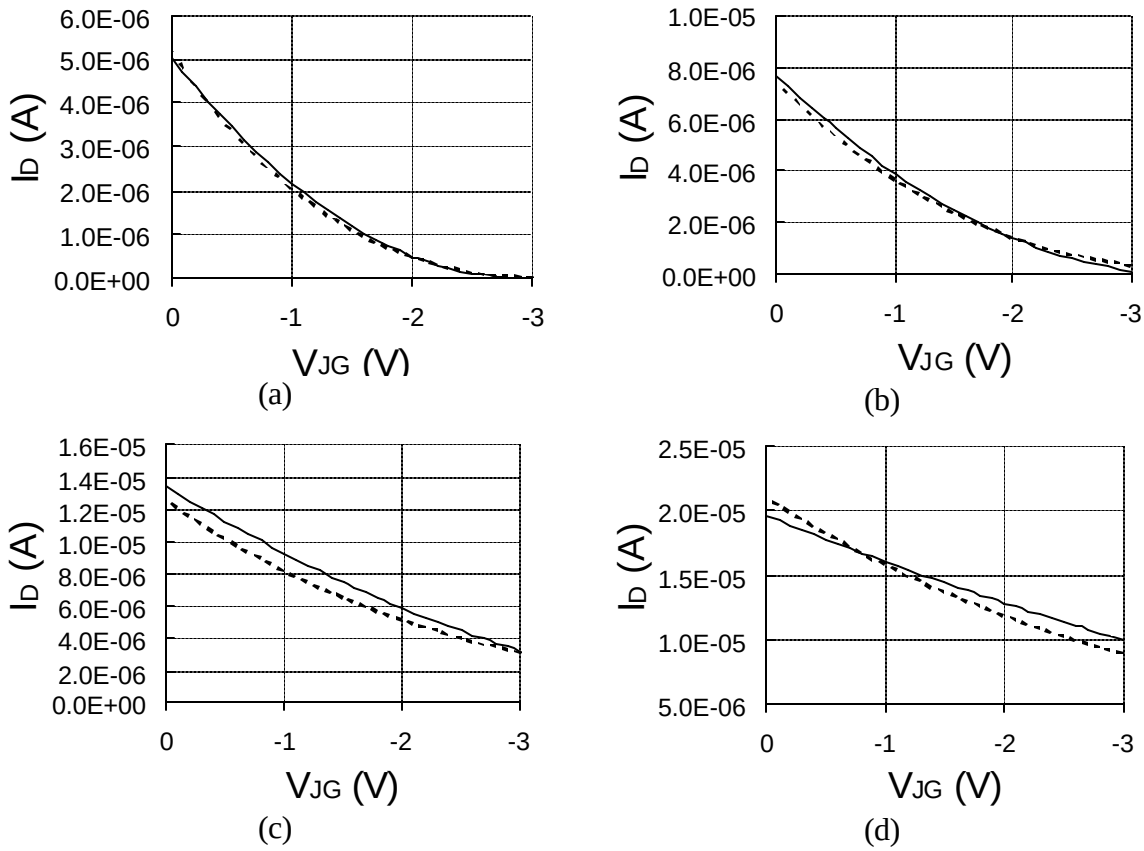


Figure 3.19. N-channel MOSJFET saturation model (——) versus measured (-----) data for a width of 0.35µm and length of 5µm with VPG biased.
V_{PG} is biased at (a) 0V, (b) 1V, (c) 2V, and (d) 3V. For all cases V_{SUB}=0V, V_D=3V, V_{JG}=0V and V_S=0V.

The linear mode of the MOS-JFET cannot be modeled with the simple model shown in equation (3-1). The model selected in this work for linear mode operation is equation (3-6) [8].

$$I_D = G_0 * \left\{ V_D - \frac{2}{3}(V_{bi} - V_P) \left[\left(\frac{V_D + V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} - \left(\frac{V_{bi} - V_G}{V_{bi} - V_P} \right)^{3/2} \right] \right\} \qquad (3\text{-}6)$$

where

$$G_0 = 2.05 * \frac{G_{0eff}}{L},$$

$$V_P = V_{Peff} * W$$

Figure 3.20 shows the accuracy of the linear model with the junction gate biased at 0V and -1V. This model is not as accurate as the previous models, but can be used for approximations.

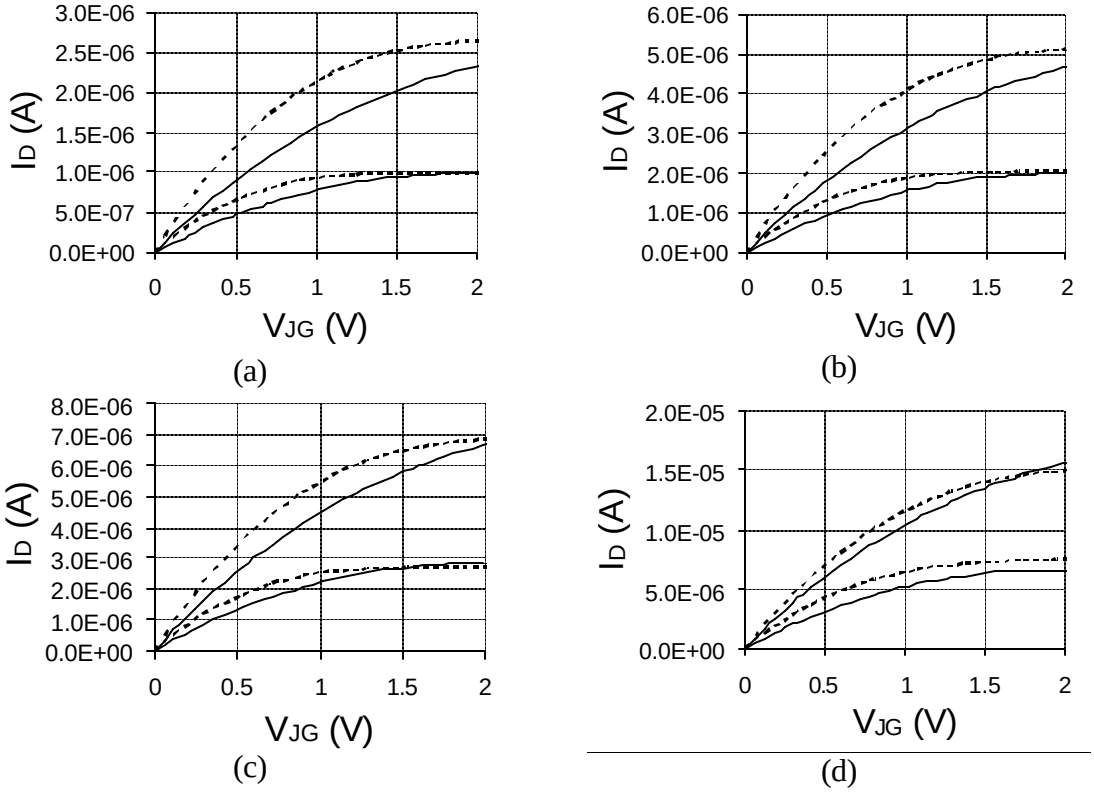


Figure 3.20. N-channel MOSJFET linear model (—) versus measured (-----) data. For a constant width of 0.35µm and lengths of (a) 10µm, (b) 5µm, (c) 3.5µm, and (d) 1.5µm. For all cases V_{SUB}=0V, V_D=3V, V_{PG}=0V and V_S=0V.

In summary, the first two models developed in this work can be readily used to predict I-V characteristics under different junction gate and poly gate bias conditions during saturation operation. The linear model developed for the MOS-JFET is less accurate than both saturation models and subsequently requires more development effort. MOS-JFET circuit designers, however, may still use the linear mode to provide rough estimates of I-V characteristics.

3.4. Analog and Mixed-Voltage Building Blocks

Extensive research has uncovered multiple applications for circuits using the MOS-JFET. The multiple gates of the MOS-JFET expanded the opportunities for signal processing. The next sections (Section 3.4.1 to Section 3.4.10) describe a sample of the applications envisioned. Schematics, layout, and test data will be presented where applicable.

3.4.1. High Voltage

The devices needed for high voltage applications within SOC are mentioned in Chapter 2. DMOS devices have been the standard high voltage transistors used for most high voltage applications using CMOS technologies. Figure 3.21 shows the aerial view of a high voltage MOS-JFET with an added drain extension (R_D). Extension of the drain increases the drain resistance which in turn allows for increased drain to source voltage limit. Several flavors of layout styles were drawn to invest high voltage breakdown capabilities.

The normal layout of the n-channel MOS-JFET already has a breakdown of 11V, but with the added drain extension (R_D) the high voltage n-channel MOS-JFET has a breakdown of at least 14V. Figure 3.22 shows the high voltage n-channel MOS-JFET with breakdown of up to 14V with the same operation shown in Figure 3.4. This demonstrates the extended high voltage tolerance of the n-channel MOS-JFET, particularly for SOC applications. There were no special process alterations and the drain remains self-aligned, unlike some DMOS structures.

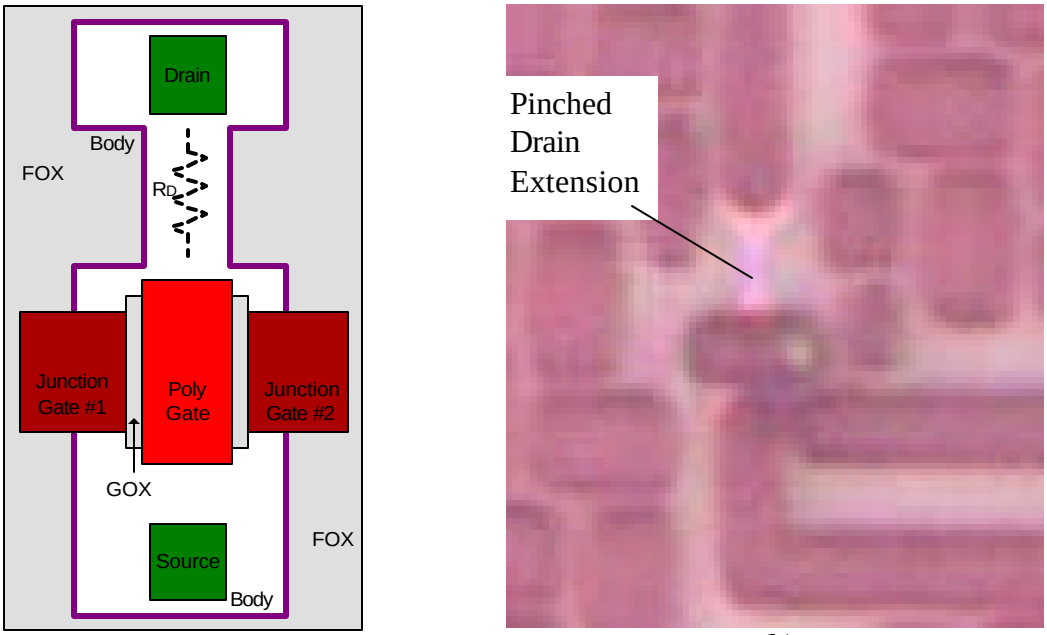


Figure 3.21. High voltage version of MOS-JFET (a) figure and (b) actual device microphotograph.

The breakdown shown in Figure 3.22 was caused from the breakdown of the junction gate diodes. To achieve higher voltages, the junction gates were left floating. Figure 3.23 displays a high voltage version of the n-channel MOS-JFET with a breakdown of approximately 40V. Note that the top gate still modulates the drain

current. This measured breakdown voltage far exceeds (nearly twice) that of recently published SOI MOSFETs with highly resistive drain structures [9].

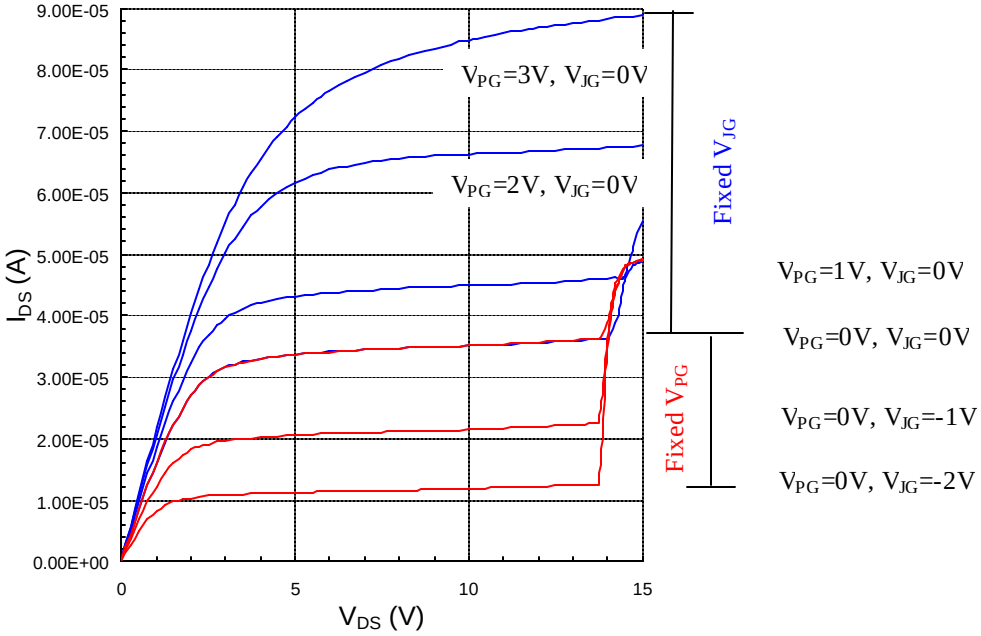


Figure 3.22. Measured ID vs. VDS for a n-channel MOS-JFET with extended drain. L=1.5µm, W=0.35µm, and VSUB=0V.

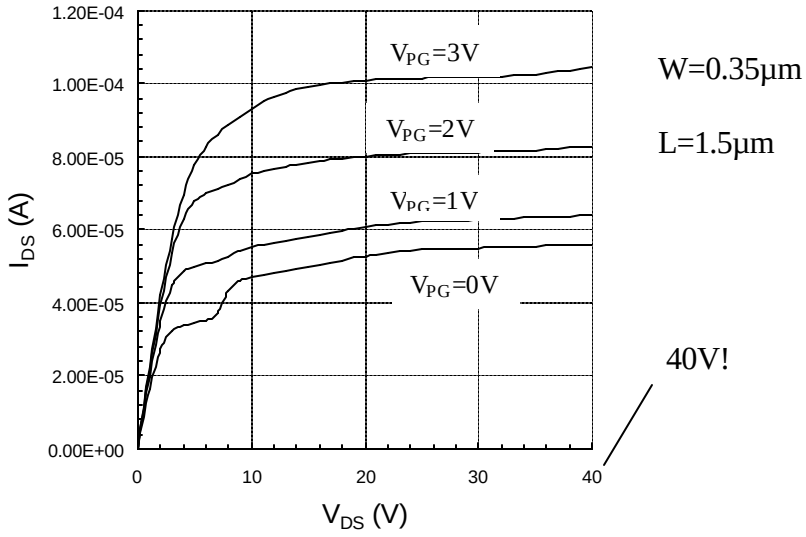


Figure 3.23. Ultra high voltage curves of MOS-JFET. V_{JG} floating and V_{SUB}=0V.

3.4.2. Low Voltage

As mentioned in Chapter 2, low voltage transistors are used for the majority of the IC industry's circuits. Since the MOS-JFET is fabricated in a technology that is optimized for low voltage, the MOS-JFET can be intrinsically operated in the low voltage region, but has added benefit of offering a depletion-mode device for low voltage circuits with zero added cost to the fabrication process (no added masks or process steps). Figure 3.24 shows low voltage curves of a MOS-JFET with a width and length of 10µm and 0.3µm, respectively. This n-channel MOS-JFET has full gate control and has a pinch-off voltage of -2V. In addition, increased current as shown in most dual gate devices is displayed in this figure as well.

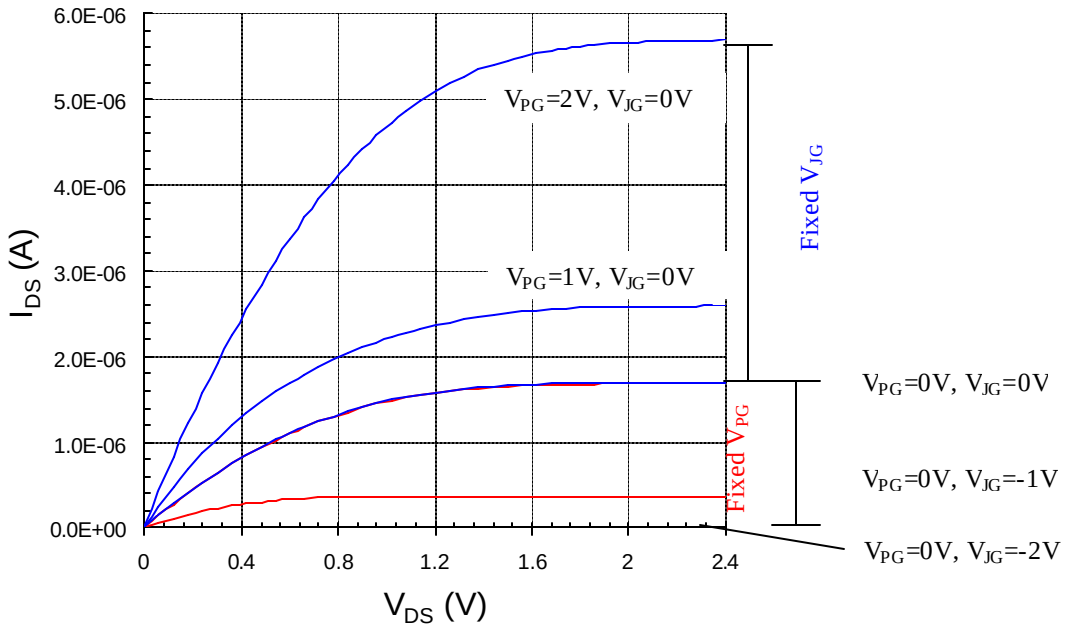


Figure 3.24. Measured ID vs. VDS for a n-channel MOS-JFET at low voltages. L=10µm, W=0.3µm, and VSUB=0V.

3.4.3. Current Mirror

Depletion mode JFET simple current mirrors are not possible because of the low p-n junction turn-on voltage. The MOS-JFET voltage however, can be used in current mirror circuits since the top gate can be taken positive with respect to the source (similar to an enhancement mode MOSFET). Figure 3.25 shows a MOS-JFET current mirror circuit.

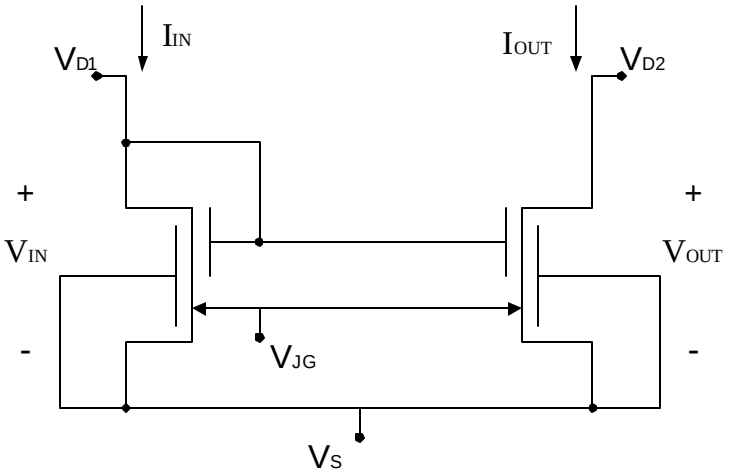
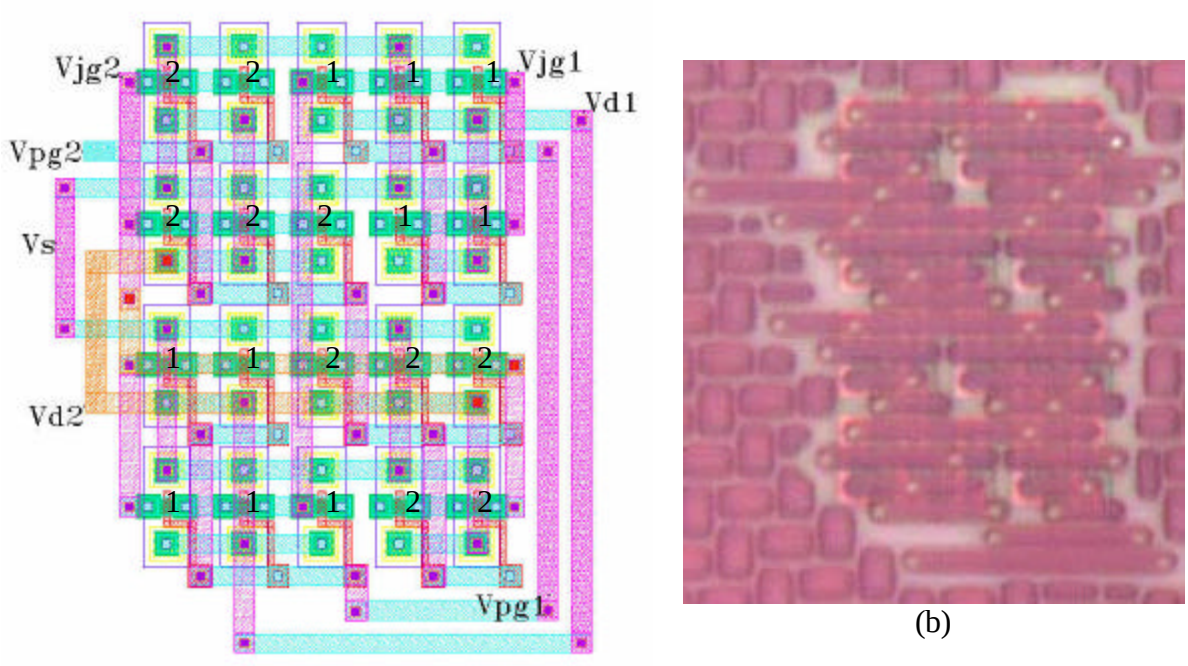


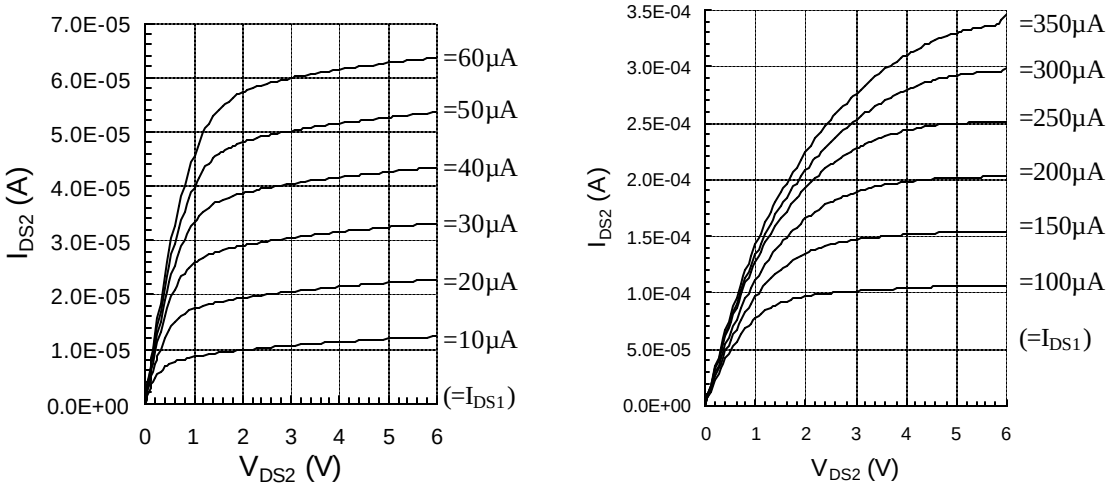
Figure 3.25. Schematic of MOS-JFET single current mirror.

Figure 3.26 shows a generic common centroid layout of the n-channel MOS-JFET pair. A current mirror was implemented using this layout by combining the junction gates (V_{JG1}=V_{JG2}) into one node. The poly gates and the input drain (V_{PG1}=V_{PG2}= V_{D1}) were tied together as the input node. Both transistors have 10 gate fingers, each with a width of 0.35µm and length of 1.5µm. Using multiple gate fingers increased the effective width (increasing transconductance), improved current drive, and improved transistor matching (by facilitating common centroid layout).



(a) (b)

Figure 3.26. Common centroid layout of n-channel MOS-JFET pair used to implement the MOS-JFET current mirror.
(a) Generic layout and (b) corresponding circuit microphotograph with same orientation.



(a) (b)

Figure 3.27. N-channel MOS-JFET single current mirror.
VJG=-3V, VSUB =0V, and VS=0V for (a) low current and (b) high current applications.

With V_{JG} depleted (-3V) and V_S grounded, the MOS-JFET current mirror's measured DC performance is shown in Figure 3.27. Figure 3.27 (a) displays the low

current (10µA to 60µA) performance of the simple n-channel MOS-JFET current mirror. High current characteristics (100µA to 350µA) are provided in Figure 3.27 (b). As expected, optimal matching between I_{out} and I_{in} occurs when $V_{out}=V_{in}$, just as with standard MOSFET simple current mirrors. The MOS-JFET current mirror, however, provides high voltage performance.

3.4.4. Full-wave Rectifier

A full wave rectifier can be realized using one MOS-JFET transistor. The characteristics are nearly ideal because the junction gate dopant levels and surroundings are identical. Figure 3.28 shows the characteristics of dual gate differential biasing.

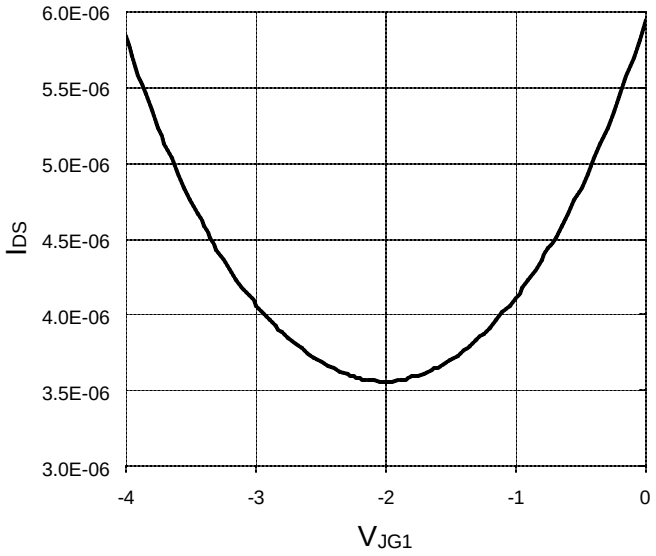


Figure 3.28. Dual junction gate differential biasing.
Drain current for junction gate #1 swept from -4V to 0V and junction gate #2 swept from 0V to -4V synchronized. V_{PG} and V_{SUB} are biased at 0V.

Figure 3.29 shows the input and expected output of a full-wave rectifier. A full wave rectifier effectively is an absolute value circuit. The expected output is the absolute value of the input.

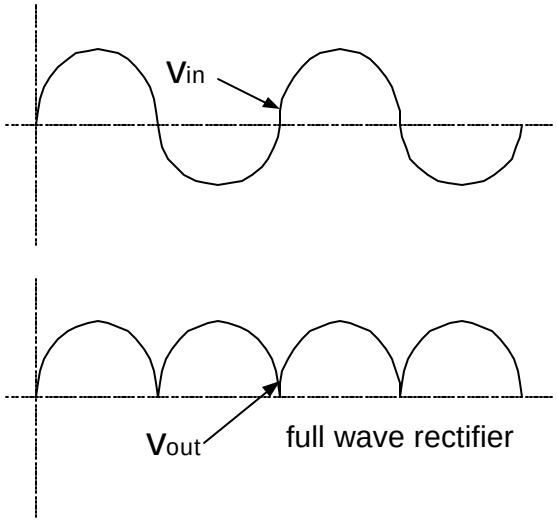


Figure 3.29. Sample output for a full-wave rectifier.

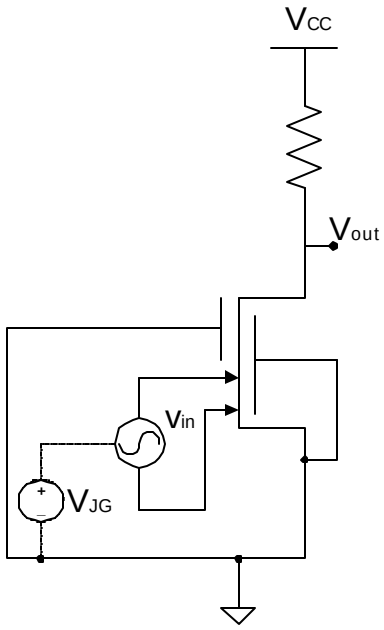


Figure 3.30. MOS_JFET full wave rectifier.

Figure 3.30 shows the schematic of a full wave rectifier using a single n-channel MOS-JFET. The resistor is used to bias the drain voltage and monitor the current. A DC offset is applied to the junction gate to achieve ideal bias conditions.

Figure 3.31 show the measured output of a n-channel MOS-JFET configured as a full-wave rectifier. The measured output displays the characteristics previously shown in Figure 3.29. The DC offset applied at the gate is -2V and the output is AC coupled.

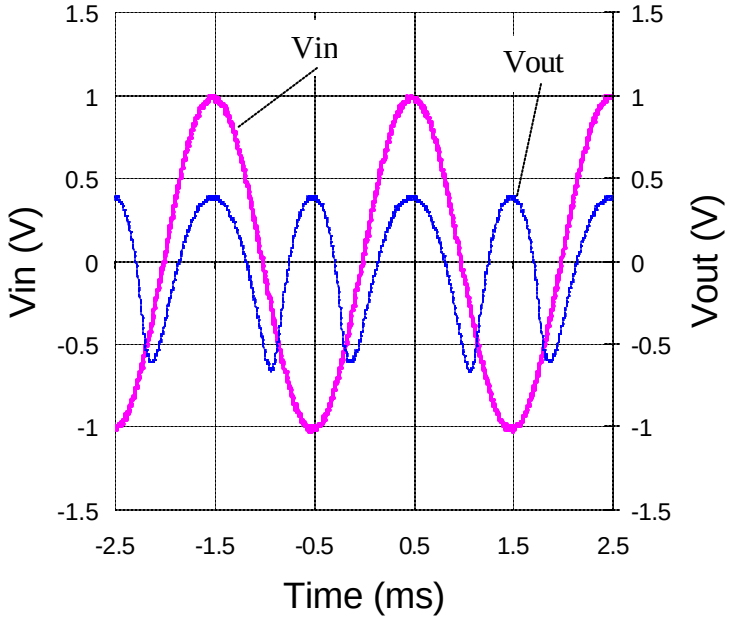


Figure 3.31. MOS-JFET full-wave rectifier measured output.
Using a n-channel MOS-JFET with width and length equal to 0.30µm and 10µm.

CHAPTER IV

CONCLUSION

In conclusion, the MOS-JFET is a viable solution to the problems presented in Chapter 2. The two-dimensional simulations provide theoretical support for the observed measured performance. The presented measured data has proven that separate control of each gate is a significant advantage offered by this device. Test data has shown this device works in all regions and bias situations described. Although this device has some unique qualities, further research is needed to fully understand and utilize the potential of this device. Device optimization and circuit utilization are two directions that will need to be explored in the years to come.

4.1. Summary of Contributions

The MOS-JFET is a novel device that can be used in multiple applications without any changes to the existing fabrication process. The device also reduces the number of transistors for some circuits. Although not described in this work, additional circuits that should benefit from the MOS-JFET include: low flicker noise, radiation tolerance, amplitude modulation, single transistor NAND gate, ICMR differential pair, differential difference amplifier, and many not yet envisioned.

4.2. Future Research

This MOS-JFET device has much potential in today's IC design. Envisioned applications include extremely low flicker noise, voltage controlled wires, inherent radiation tolerance, mixer circuits, specialized differential circuits, and programmable circuits.

The extremely low flicker noise is likely possible when all gates are depleted so that the current path is strictly in the center of the channel and does not flow near Si/SiO_2 interfaces (see Figure 4.1). The noise generated will only depend on the body doping characteristics.

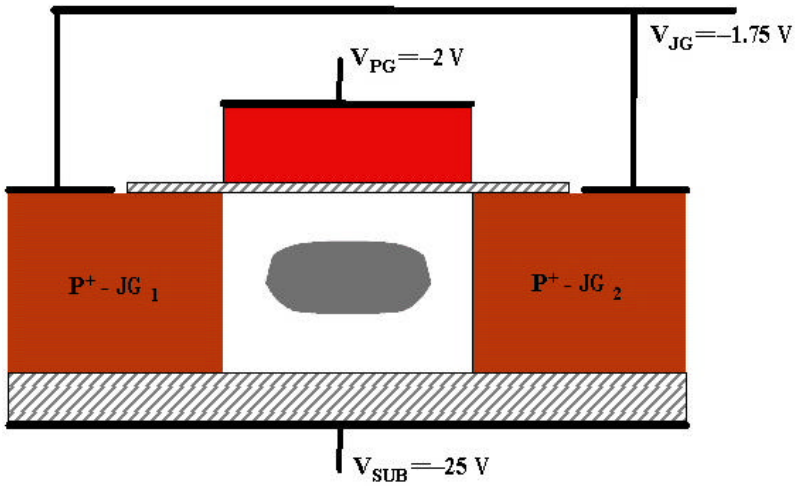


Figure 4.1. Channel conduction with all gates depleted.

Figure 4.1 also shows the idea of a voltage controlled wire. The voltage controlled wire is possible because of the gate control mentioned above. Certain bias conditions will allow the designer to move the wire to different sections of the channel via the level of gate depletion. This could result in a quantum wire with scaling technology features.

The radiation tolerance is mentioned because this device exhibits some JFET-like behavior and is in SOI. JFET devices have long been used to improve radiation tolerance and SOI has been proven to have radiation tolerance characteristics [6].

MOS-JFET is able to simplify multiplier circuits because of the dual junction gates, when V_{JG1} and V_{JG2} are used as separate inputs.

A mixer application the MOS-JFET can be used for is amplitude modulation. Figure 4.2 shows the circuit configuration in which a single MOS-JFET can be used as an amplitude modulation circuit. With the junction gates connected as one input and V_{PG} used as a second input, the device can be turned on and off when the poly gate is modulated in the depletion region.

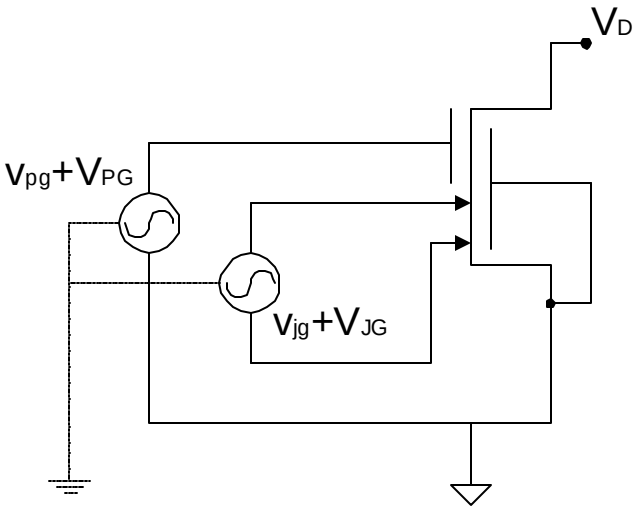


Figure 4.2. Amplitude modulation circuit.
V_{JG1} and V_{JG2} are connected as one input and V_{PG} as the second input.

The programmable MOS-JFET is derived from floating gate programmable devices.[10] The added advantage is there are four control inputs remaining after this device is implemented. Figure 4.3 shows a programmable MOS-JFET schematic. V_{CG} is

the node at which a signal is applied to program the floating poly gate or adjust the MOS-JFET drain current.

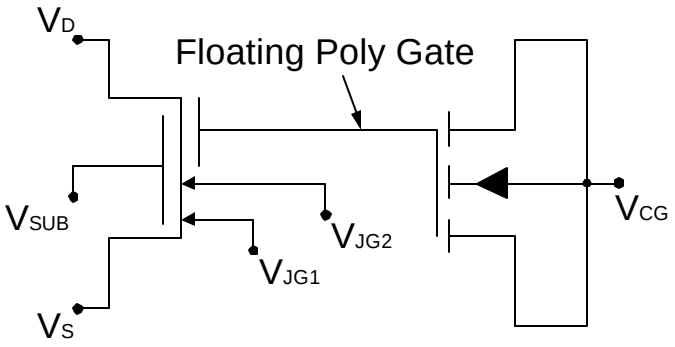


Figure 4.3. Programmable JFET schematic.

These devices can be used as a post-process trimming device. EEPROM cells have been used to improve current matching accuracy in analog current mirrors [11]. This device can also be used as an on-chip programmable resistor in IC chips.

Unique differential circuits can also be envisioned. ICMR differential pair and differential difference amplifier circuits can directly benefit from the MOS-JFET. The MOS-JFET can reduce the number of transistors and also increase the accuracy of these circuits due to the increased gate control.

Finally, this device has shown to be beneficial to circuit designers, through its numerous circuit applications. Much work is needed, however, to explore SOI and this device before its ultimate can be gauged.

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