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Partitioning And Interface Requirements Between System And Application Control For Power Electronic Converter Systems

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PARTITIONING AND INTERFACE REQUIREMENTS BETWEEN SYSTEM AND APPLICATION CONTROL FOR POWER ELECTRONIC CONVERTER SYSTEMS

By

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Applications of power electronics in power systems are growing very rapidly and changing the power system infrastructure in terms of operation speed and control. Even though applications of power electronics are wide spread, the cost and reliability of power electronics are the issues that could hinder their penetration in the utility and industrial systems. The demand for efficient and reliable converter controllers gave rise to modularized converter and controller design. The objective of this dissertation is to determine the appropriate partitioning and interface requirements between the system and application control layers for power electronic converters so that the minimum set of system layer to application layer control interfaces is compatible across all power electronic controllers.

Previous work, using the Open System Architecture (OSA) concept has shown that there is a set of common functions shared by different converters at the low-level control layers. It has also shown that, depending on the application, there is a variation in control functions in application/middle control layers. This functional variation makes it

difficult to define system functionality of power converters at upper control layers and further complicates the investigation into the partition requirements of system to application control layer. However, by analyzing the current or voltage affected by a converter in terms of orthogonal components, where each component or group of components is associated with a power-converter application, and the amount of required DC bus energy storage, a common functionality can be observed at the application control layer. Therefore, by establishing common functionality in terms of affected current or voltage components, a flexibility of operation can be realized at upper control layers that will be a major contribution towards standardizing the open system architecture.

In order to a construct functional flexible power converter control architecture, the interface requirements to the system control layer and the partitioning between the system control layer and application control layer need to be explored. This will provide flexibility of system design methodology by reducing the number of constraints and enabling system designers to explore possible system architectures much more effectively.

DEDICATION

I would like to dedicate this work to my wife and my family members.

ACKNOWLEDGMENTS

I would like to take this opportunity to express my deepest gratitude to my advisor Dr. Herbert L. Ginn III for his support, guidance, and encouragement throughout this research. I would also like to extend thanks to the other committee members Dr. Noel Schulz, Dr. Randolph Follett and Dr. Anurag Srivastava for serving on my committee to improve this work.

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CHAPTER I

INTRODUCTION

This chapter introduces the dissertation topic by giving a brief background on layered control architecture of three-phase power electronic converters used in utility and industrial applications. Also, it addresses the research problem by recognizing the issues in the power electronic business with regard to the control interfaces and current design practices.

1.1 Topic Background

Applications of power electronics in power systems are growing very rapidly and changing the power system infrastructure in terms of operation speed and control. The cost and reliability of the power electronics are the issues that could hinder the penetration of their applications in utility systems. Recognizing these issues while supporting high power density and high-speed operation for high power applications, the Power Electronics Building Block (PEBB) concept has been proposed [1]. In the construction of PEBB based modular systems, the characteristics of the interfaces between the control modules are of prime importance [1]-[2]. Presently power electronic systems especially in the medium and high-power range, employ custom control architectures and their control interfaces and control modules are also specific to the type

and manufacturer [3]. This limits the system designer's choices when considering the power electronic converters for various power system applications. Thus, an open architecture power converter system with standardized modules and control interfaces was introduced that would allow system designers to explore the design space much more effectively [2]. This architectural openness would contribute to healthy industrial competitiveness and reduction of the recurring engineering costs.

The concept of the PEBB as a basic building block in power conversion has been developed and analyzed for generic power electronics applications [1]. When control functions of many different power converter systems are investigated and evaluated, at the lower level control layers, a common control functionality emerges irrespective of the target application [2], [4]. Using the concept of system level layers, it is possible to define hierarchical control architectures for these systems. A block diagram of the layered control architecture of a power electronic converter system is shown in Figure 1.1. The control architecture is partitioned into several common control layers. A system control layer determines the overall mission of the system, application control layer dictates the operation of the overall mission of the system, converter control layer implements many of the common functions of converters, switching control layer handles modulation and pulse generation, and the hardware control layer manages all operations specific to the power hardware.

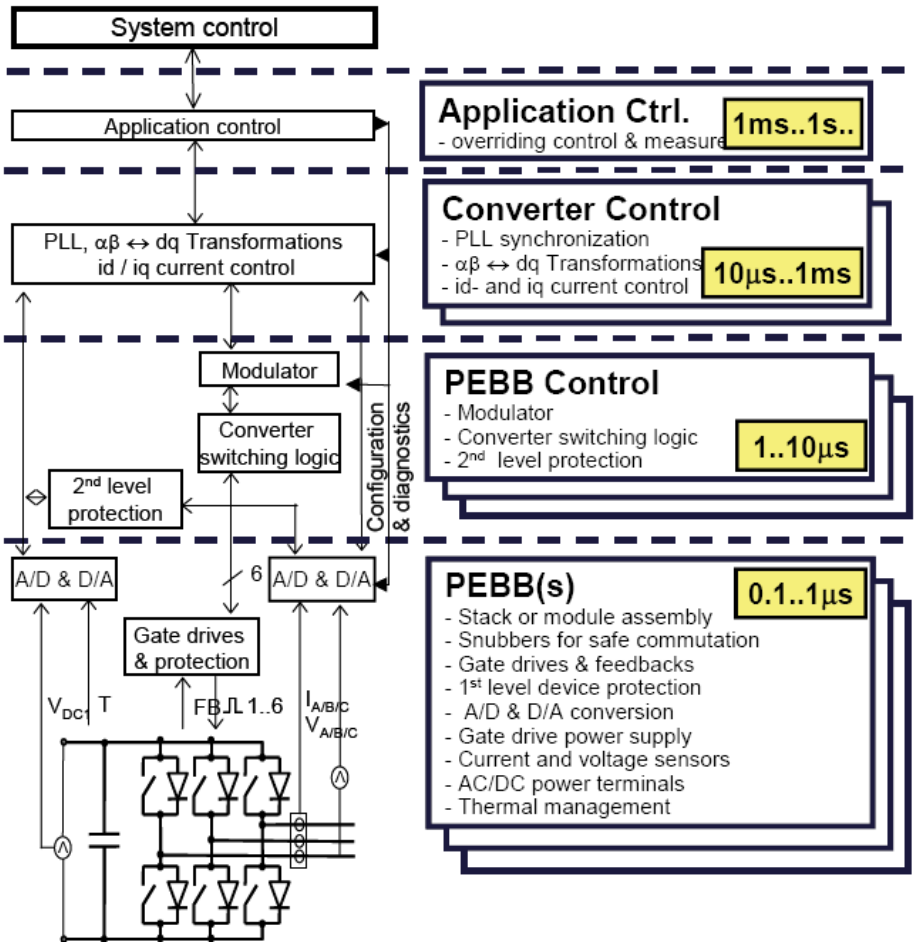


Figure 1.1 Control architecture for a power electronic converter system [5].

The control partitioning approach, based on functional and temporal distribution into system layers, is considered to be a basic step towards modularization [4]. Controller partitioning of power converter architecture alone is not sufficient and will not provide significant advancements in power electronics technology if partition interface standardization is not achieved in parallel. Finding common denominators for different power architectures and standardizing interfaces between layers could bring a new constructive approach to power electronics design and practice [6], [7]. In the literature [2], [4], an Open System hierarchical Architecture (OSA) is proposed, based on

functional distribution, to standardize control architecture in power converter applications using the concept of hierarchical system layer partitioning. The objective of OSA is to standardize the PEBB based controller design through standardization of interface between layers from a set of common basic functions. OSA also suggests that the partition for a power converter system control involving multiple subsystems should have several levels or layers corresponding to a system control layer, an application control layer, and low-level control layers (converter/functional layer, switching layer, and the PEBB hardware control layer).

Some work in standardizing the control architecture [2] has presented the partitioning interface characteristics and requirements of low-level control layers by showing that the control functions are nearly uniform for all type of converters. It has also shown that there is a variation in control functions, in the application/middle control layer, depending on applications. This variation is because of the functional blocks corresponding to the reference signal generation having employed a different control reference frame according to the application. This does not allow the OSA to provide flexibility of operation at the upper or system and application control layers. In order to construct functional flexible power converter control architecture, the possible commonality in system and application control functions, along with the partitioning interface requirements between the system control layer and application control layer, need to be explored.

1.2 Objective of Dissertation

As discussed in the topic background some example implementations [2] using the OSA concept showed that there is a set of common functions shared by different converters at the low-level control layer. It has also showed that there is a variation in control function, in the application/middle control layer, depending on application. This functional variation makes it difficult to define a common functionality of power converters at the upper control layers and further complicates the investigation into the partition requirements of the system to application control layer. However, by analyzing the current or voltage affected by a converter in terms of orthogonal components [8], where each component or group of components is associated with a power-converter application, and the amount of required DC bus energy storage, a common functionality can be observed at the application control layer that contributes to determining the partitioning requirements of the system to application control layer partition. Thus, by establishing common functionality in terms of affected current or voltage components, a flexibility of operation can be realized at upper control layers that will be a major contribution towards standardizing the open system architecture.

The goal of this research is to determine the appropriate partitioning and interface requirements between the system and application control layers for systems of power electronic converters so that the minimum set of system layer to application layer control interfaces is compatible across all power electronic controllers. This will provide flexibility of system design methodology by reducing the number of constraints and enabling system designers to explore possible system architectures much more

effectively. The research plan consists of several aspects, including investigation into appropriate control layers, partitioning of their interfaces, finally the modeling and simulation in order to validate the suggested interface requirements.

1.3 Approach

This research is mainly focused on three-phase power converters widely used in power system utility and industrial applications like Power Quality, Flexible AC Transmission Systems (FACTS), High Voltage DC Transmission (HVDC), Distributed Generation and Motor Drive applications, etc. Three-phase converter topologies consist of either Shunt Connected Current Controllers (ShCC), Series Connected Voltage Controllers, or a combination of the two [9], but shunt converters are more common. Therefore, the work will focus on shunt connected converter systems with an expectation that the approach can be extended to series connected converters. The working approach for the proposed research consists of three major tasks:

Task 1: Application Control Layer to Converter Control Layer Partitioning

Separating the application and system control functions from the lower level control functions so that the boundary location between the system and application control layers can be explored.

Task 2: System Control Layer to Application Control Layer Partition

Determining the effect of boundary location on the system to application control layer partition interface based on the following criteria: total number of interface signals, commonality of signals across the typical applications, and bandwidth requirements of the signals.

Task 3: Modeling and Simulation

Validating system and application control layer partitioning interface requirements using simulations for several example applications.

1.4 Dissertation Outline

The dissertation is organized as follows: Chapter II gives a background view on the principles of control partitioning in power electronic converter architectures. Chapter III presents a formulated criterion of application control layer to converter control layer partitioning for three phase power converters. Chapter IV presents system control layer to application control layer partitioning. This is based on developing generalized control architectures for several power converter applications. Chapter V explores partition and temporal requirements through various options and considerations in the partitioning of system control layer to application control layer. Chapter VI addresses modeling, and validation of partition requirements between the system control layer and application control layer interface using MATLAB/Simulink models. Chapter VII gives a definition for the system to application control layer interface so that it is compatible across all power electronic controllers. Chapter VIII includes the conclusions and future work.

CHAPTER II

PRINCIPLE OF CONTROL PARTITIONING

Chapter I introduced the concept of layered control architecture and mentioned that in the construction of modular power electronics converter systems, the characteristics of the interfaces between the modules are of prime importance. This chapter presents the criteria behind the partitioning of the system components into a hierarchical layered architecture.

2.1 Partition Criteria

In the literature [6], [10], the general partitioning of control architecture was proposed for generic power electronics systems and is based on following criterion [2]:

- Functional distribution
- Temporal distribution: protection, switching frequency and modulation, time constants and control bandwidth.
- Technology distribution: physical nature of values and property of materials, and manufacturing process.
- Spatial distribution: power level and system requirements.

“All four criteria: functional, temporal, spatial, and technological criteria can be used for partitioning of the control functions. However, because technology distribution and spatial distribution are specific to particular implementations, functional

and temporal distributions are considered to be the driving criteria. It is expected that both technology and spatial distributions may modify the distributions for particular implementations. Furthermore, in a majority of cases functional and temporal distributions will naturally occur at the same boundaries," [11]. Figure 1.1, shown in Section 1.1, is a typical voltage source power electronic converter application with a partition of the control system based on functional and temporal distribution.

In order to determine the locations of the control layer boundaries it is instrumental to categorize power electronic systems into one of three broad categories: Shunt Connected Current Controller, Series Connected Voltage Controllers, and Impedance Controllers [9]. The criteria for establishing the boundary locations for lower level control layers are listed as follows:

Converter Control Layer: The converter control layer implements many of the common functions of converters. It is responsible for maintaining such functions as synchronous timing (PLL), current and voltage filtering, measurements, and feedback control calculations. Thus, the functional control layer will have some common functions depending on the particular target applications. The primary application of this layer is the feedback control system, while the other components support the input and output requirements of the feedback control system.

Switching Control Layer: The switching control layer will contain many common functions irrespective of the final application. The functions include switching or modulation control, and pulse generation. The switching control layer and all lower layers enable the power electronics to behave as a PWM controller source. Here the

PWM controlled source is defined as having its terminals directly at the power terminals of the power electronics hardware.

Hardware Control Layer: The hardware control layer manages everything specific to the power electronics, and it may exist as multiple modules depending on final power configurations. Gating, measurements, galvanic isolation, safe commutation and 1st level protection are functions of this layer and will be common for virtually any PEBB based application.

Determining the partition criteria for upper control layers, system control layer and application control layer, and their interface requirements are primary objectives of this dissertation and these will be discussed in detail in the remaining chapters.

2.2 Typical Control Architectures

Two main types of power electronic converter systems used in power distribution and industrial applications are shunt connected current controllers (ShCC) and series connected voltage controllers (SeVC) [9]. Shunt connected current controllers can be grouped by applications [2], [8] where the bi-directional voltage source converter is the basic power electronic module. It is also the basic module for series connected voltage controllers. Table 2.1 lists some common shunt connected current controllers for distribution system applications and Table 2.2 lists some series connected voltage controllers, where HGL denotes a harmonic generation load.

The available amount of current for shunt connected devices depends on the voltage at the point of connection and the available voltage drop across series devices depends on the current in the system. Thus, they behave as controlled impedances. From

the standpoint of the system control there is no difference between the controlled impedance and the controlled voltage or current source, with the exception of their operating limits.

Table 2.1 Some typical shunt connected current controller applications [8].

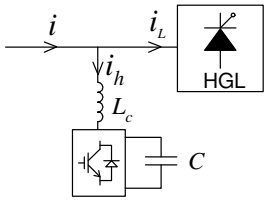
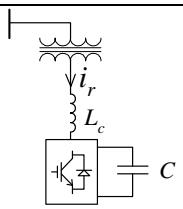
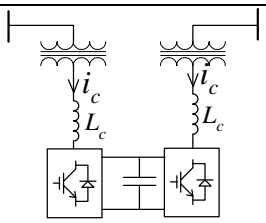
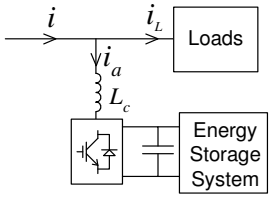
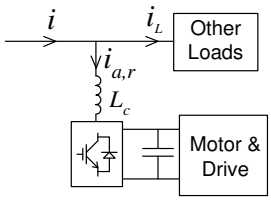
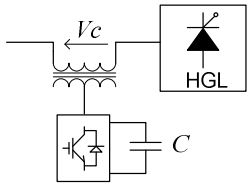
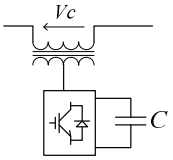
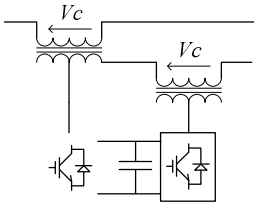
Converter System Description	Function	Simple One-line Diagram
Active Filter	Cancel harmonic currents by injecting appropriate current into the node	
Static Synchronous Compensator (STATCOM)	Provide desired reactive current for VAR compensation, voltage regulation and stability enhancement	
Mini-HVDC (HVDC Light)	Provide interconnection between two AC nodes for active and reactive power flow control	
Energy Storage System Interface	Provide active power for load leveling or UPS function	
Active Front End for Motor Drives	Provide active and reactive power for motor VSD	

Table 2.2 Some typical series connected voltage controller applications.

Converter System Description	Function	Simple One-line Diagram
Series Active Filter	Cancel voltage harmonics by adding a cancelling voltage drop into the line	
Static Synchronous Series Compensator (SSSC)	Provide desired voltage for VAR compensation, voltage regulation and stability enhancement	
Inter line Power Flow Controller (IPFC)	Provide interconnection between multiple AC nodes for active and reactive power flow control	

Although each of the applications in the three basic classes discussed in Table 2.1 and Table 2.2 have the same basic circuit structure within a class, each one is made unique and has fixed and limited application due to custom control architectures and interfaces that are tailored to the specific application. This does not provide the flexibility of operation at the upper or system and application control layers. In order to construct functional flexible power converter control architecture, the interface requirements to the system control layer and the partitioning between the system control layer and application control layer need to be explored.

As mentioned above, both shunt and series connected converters are employed to implement different power electronic applications, but shunt converters are more common. Therefore, the rest of the work will focus on shunt connected converters with the expectation that the approach can be extended to series connected controllers.

CHAPTER III

APPLICATION CONTROL LAYER TO CONVERTER CONTROL LAYER PARTITIONING

The criteria for establishing the boundary locations for lower level control layers were given in Chapter II. This chapter introduces a formulated criterion of application control layer to converter control layer partitioning for three phase power converters. The application and system control functions are then separated from the lower level control layers for each of the typical applications outlined in Table 2.1 of Chapter II.

3.1 Partition Criteria

In power converter applications the shunt connected current controllers are used when particular components of the current are drawn from or injected into a system. The operating principle of ShCC is like a controlled current source where the application dictates the functionality of the control components that generate the reference current. Thus, the lower-level control layers with ShCC converter topology behave as a controlled current source. This will be selected as the criteria for the division of lower control layers from the application and system control layer. Figure 3.1 depicts a simplified ShCC with the control partitioned into four layers [8]. The converter layer and hardware

layer controls enable the PEBB hardware to behave as a controlled current source, as depicted by the dashed line. All control layers that act to create high power current source using the PEBB hardware are considered as those control layers that are below the application and system layers. The application and system control functions will be separated from the lower control layers for all typical applications of converter topologies.

Similarly, the operating principle of the series connected voltage source converters is like a controlled voltage source. Thus, the lower-level control layers with SeVC converter topology behave as a controlled voltage source and those that enable it to behave as such are separated from the application and system control layers. Therefore, the same approach can be applied to the SeVC class of applications.

Some typical shunt connected current controller applications shown in Table 2.1 along with current components affected are summarized in Table 3.1, where each current orthogonal component or group of components associated with a ShCC application [8] were shown in column III of Table 3.1. Here, the components $\boldsymbol{i_a}, \boldsymbol{i_r}, \boldsymbol{i_u}$ are the active, reactive and unbalanced components of the current fundamental respectively, $\boldsymbol{i_h}$ is the current component that corresponds to harmonics present in the system and $\boldsymbol{i_c}$ is the overall converter current.

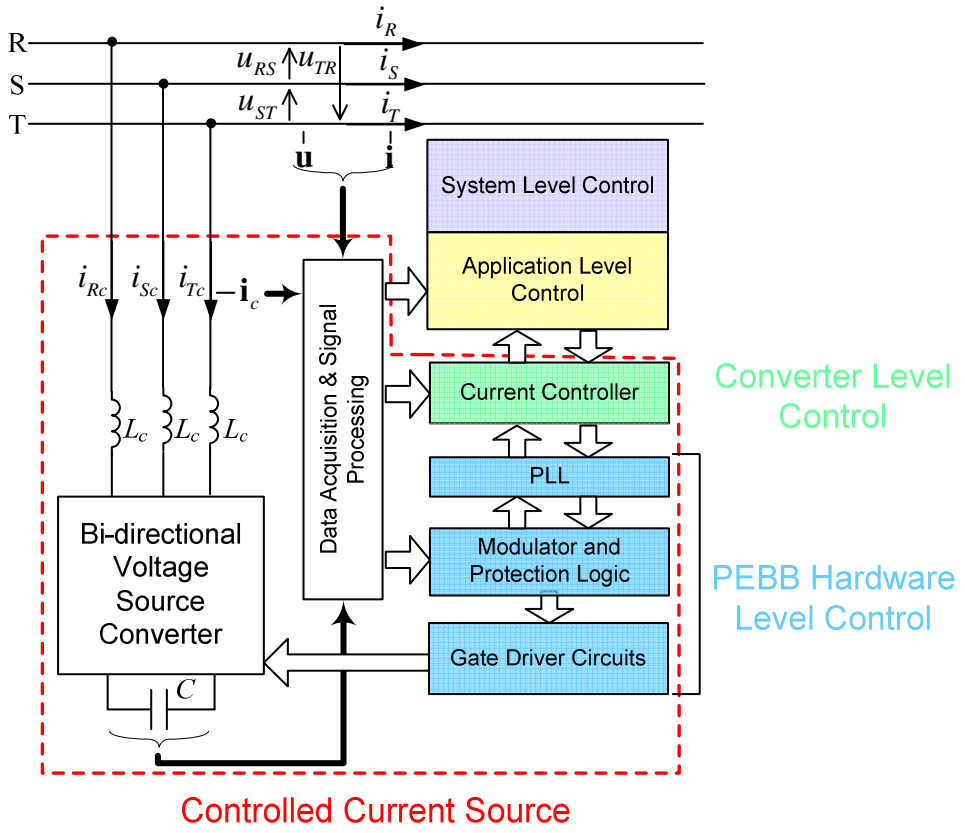
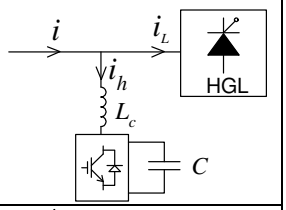
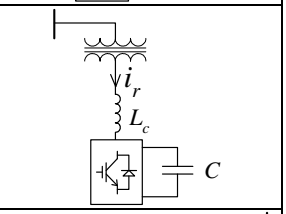
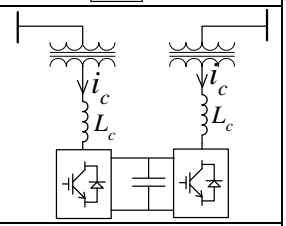
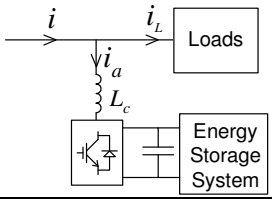
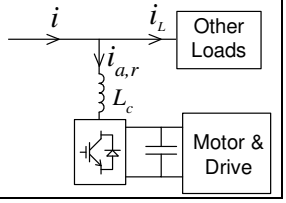


Figure 3.1 Functional diagram of a converter with partitioned control architecture.

Table 3.1 Some typical shunt connected current controller applications with affected current components [8].

Converter System Description	Function	Current Components Affected	Simple One-line Diagram
Active Filter	Cancel harmonic currents by injecting appropriate current into the node	$i_c = i_h$ $i_c = i_h + i_r$ $i_c = i_h + i_r + i_u$	
Static Synchronous Compensator (STATCOM)	Provide desired reactive current for VAR compensation, voltage regulation and stability enhancement	$i_c = i_r$	
Mini-HVDC	Provide interconnection between two AC nodes for active and reactive power flow control	$i_c = i_a + i_r$	
Energy Storage System Interface	Provide active power for load leveling or UPS function	$i_c = i_a$	
Active Front End for Motor Drives	Provide active and reactive power for motor VSD	$i_c = i_a + i_r$	

3.2 Typical ShCC Control Architectures

This section provides generalized control architectures that have been derived from an extensive review of the commonly used control architectures for the ShCC application listed in Table 3.1. These generalized architectures are then partitioned into the converter with lower layers and application and above layers.

3.2.1 STATCOM Application and System Control

STATCOMs are employed at both distribution and transmission levels, though for different purposes. When a STATCOM is employed at the distribution level or at the load end for power factor improvement and voltage regulation alone, it is called a D-STATCOM. In transmission system applications, STATCOMs provide voltage support to buses for both steady-state system operations as well as for modulation of bus voltages during transient and dynamic disturbances in order to improve transient stability margins and to damp dynamic oscillations. The primary STATCOM applications discussed are as follows:

- VAR Control
- Voltage Regulation
- Power oscillation damping
- Transient stability enhancement

3.2.1.1 VAR Control

To achieve good dynamic response in inverter output voltage, a STATCOM control scheme with fixed V_{dc} must to be included [12]. Figure A.1 in the Appendix A.1

shows the block diagram of the control scheme for VAR control. The PLL block generates the basic synchronizing-signal that is the phase angle of the transmission system voltage. The Rotating Axis Co-ordinate Transformation block computes d-axis and q-axis components of the voltage and currents, the VAR reserve control block provides the reference reactive current (i_q^*) and the DC voltage block provides the reference active current (i_d^*). Here, the Rotating Axis Co-ordinate Transformation block computes the d-axis and q-axis components of the voltage and currents, the Reference Current Calculation block and the DC Voltage Regulation block will determine current components for the shunt-connected converter. Thus, these are included in the application control layer and are separated from other lower level control functions.

3.2.1.2 Voltage Regulation

In voltage regulation applications a STATCOM is employed to regulate the bus voltage by absorbing or generating reactive power to the network [13]-[16]. A generalized decoupled control system for STATCOM reactive power compensation is shown in Figure A.2. The basic difference, as part of the application layer, between this structure and the one for the VAR control is the presence of the voltage regulator. Here, the voltage regulator provides the reference current (i_q^*) for the current regulator that is always in quadrature with the terminal voltage to control the reactive power. The voltage reference value for the reactive power compensation is calculated using V/Q droop characteristics: $V_{ref}^* = V_{abc} + k_v Q_{meas}$, where V_{abc} (or V^{stp} in Figure 3.2) is the voltage at

the point of common connection, Q_{meas} is the measured compensator reactive power and k_v is the voltage droop coefficient.

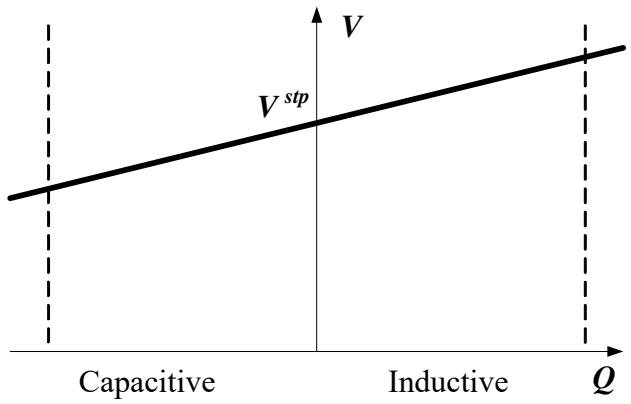


Figure 3.2 Voltage set point with droop characteristic

3.2.1.3 Power Oscillation Damping

STATCOM power oscillation damping requires the variation of the voltage at the terminal of the compensator in proportion to the rate of change of the effective rotor angle (or rotor angle speed ω_r). Rotor angle changes cause real power variation [9]. After reviewing the literature [17]–[20], it was observed that the power oscillation damping for STATCOM can be achieved by just adding additional control blocks and signals to the STATCOM controller that can perform the voltage regulation. Figure A.3 shows the complete generalized STATCOM control structure for power oscillation damping.

The additional control input signal is designed for local oscillation damping. It is implemented by calculating real/reactive power flows. This additional signal is fed through a gain block and then through a washout control block to avoid effecting steady

state operation of the controller [18], [20]. The washout control block serves as a high-pass filter, with the time constant T_W. The gain block determines the amount of damping introduced by the STATCOM.

3.2.1.4 Transient Stability Enhancement

In transient stability enhancement applications STATCOMs are employed at the transmission level. Transient stability of a system refers to the stability when subjected to large disturbances such as faults and switching of lines [9]. The resulting system response involves large variations of generator rotor angles and is influenced by the nonlinear power angle relationship. Stability depends upon both the initial operating conditions of the system and the severity of the disturbance. Transient stability at a given power level and fault clearing time is primarily determined by the power (P) versus load angle (δ) characteristic of the post-fault system that controls the electric power (P_e) transmission. When a fault occurs, P_e suddenly decreases and the synchronous machines accelerate. At the fault clearing, P_e suddenly increases and the value of the load angle δ will change accordingly. After reviewing the literature [20]-[24], a control structure that is convenient for the generalization was chosen, which improves the stability limit first by maximizing the decelerating area and then fully utilizing it in counter balancing the accelerating area [25]. Here, the transient stability enhancement is implemented by increasing the reference voltage during the first swing of a major disturbance.

Figure A.4 shows the STATCOM control structure for transient stability enhancement. This strategy requires the information about generator parameters and

transmission line impedance. All this information is needed to calculate the rotor angle speed. The measuring, processing and actuating control blocks will calculate the required rotor angle for transient stability enhancement for the entire range of power system operation. The actuating circuit is designed to switch the measuring processing and actuating circuit at appropriate times during the fault conditions. It should be noted that the mechanical power is not directly obtained, but only estimated using an observer fed by measurements taken at the point where the STATCOM is connected to the system.

3.2.1.5 Generalized STATCOM Control System

All common control system functions have been identified for each possible STATCOM application and combined together to form the generalized STATCOM control system shown in Figure 3.3. The various possible STATCOM applications correspond to modes of operation for a general STATCOM that can be used in any of the typical applications. Control functions of each mode are encircled using a different dashed line and functions common to all modes are encircled by a dotted line. Consideration of the various modes results in several potential sources of reference signals at a layer boundary. However, because the STATCOM acts as a source of reactive current, only the reactive current reference signal can be used as the point of division between the application plus system functions and the lower control layer functions as denoted by the double dashed line.

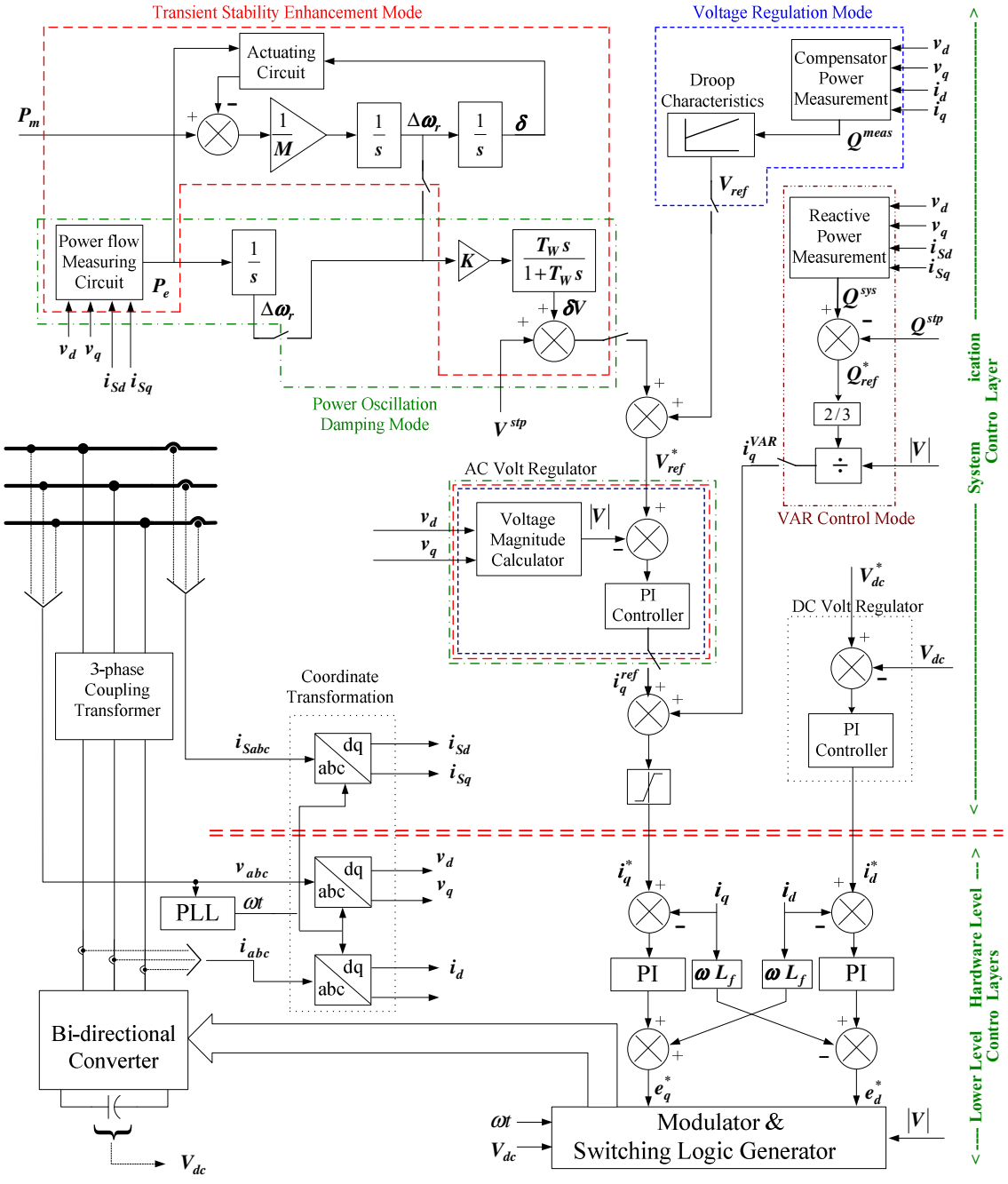


Figure 3.3 Typical STATCOM control functions with division between lower functions and application plus system functions.

3.2.2 Mini-HVDC Control Functions

The function of a Mini-HVDC system is to provide interconnection between two AC nodes for active and reactive power flow. The Mini-HVDC application selected for this interface study is a DPGS (Distributed Power Generation Systems) using a wind turbine system and for interconnection between two AC nodes for medium voltage DC transmission (MVDC). In general, the control tasks of the DPGS based systems can be divided into two major parts [25].

1) *Input-side Controller (Sending-end):* The main function of this controller is to extract maximum power from the input source.

2) *Grid-side Controller (Receiving-end)*: The main functions of this controller are as follows:

   - Control of reactive power transfer between the DPGS and the grid.
   - Control of DC-link voltage.
   - Grid synchronization.

The integration of wind systems to the grid is generally implemented by conversion of generated power from an AC-DC-AC system, due to some advantages such as: independent control of reactive and active power [26]-[28], and continuous voltage and frequency regulation at the wind turbine [29]. After reviewing various DPGS based on wind power systems [29]-[33], it was concluded that the implementation of AC-DC-AC power conversion for variable wind speed power conversion is done mostly using two topologies:

- DC-DC boost chopper between a 3-phase diode rectifier and a Voltage Source Inverter (VSI).
- HVDC transmission with a two-stage, 3-phase Voltage Source Converter (VSC)

The DC-DC boost chopper is employed for power ranges up to several hundred kW [30] while the HVDC transmission with VSC is considered for power ranges in MW [28].

3.2.2.1 DC-DC Boost Chopper between 3-Phase Diode Rectifier and VSI

Figure 3.4 shows the transmission power system for AC-DC-AC conversion using DC-DC boost chopper between a three-phase diode rectifier and bi-directional converter. Here, bus-B1 is connected to the wind power system and bus-B2 is connected to the AC grid. Using a simple three-phase diode rectifier with a DC-DC chopper, a constant voltage is maintained at the DC link irrespective of generator output voltage and frequency. This topology is also well suited to hybrid (combination of wind, photovoltaic and fuel cells) power systems.

Input-side control structure: The function of the control structure for the input-side of the system is to control the input current of the boost chopper that is obtained from the maximum power point tracking of the turbine without any information of either wind speed or generator rpm [30], [32], [33]. The use of DC-DC boost chopper will provide constant DC output at DC-link for a wide range of variable speed operation of wind power system. The chopper control block diagram for the DC-DC chopper on the input-side section is shown in Figure 3.5. Here, the input DC current is regulated to

follow the optimized current reference for maximum power point operation of turbine system. In order to capture the maximum power, a maximum power point tracker (MPPT) is required. The maximum power point of wind power generation is the function of the amount of power harnessed from the variation of wind speed and the power coefficient of wind turbine.

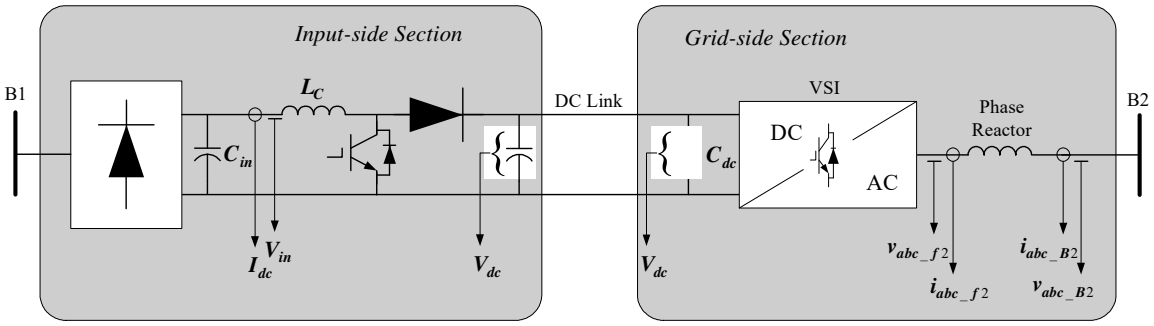


Figure 3.4 Power system using DC-DC boost chopper.

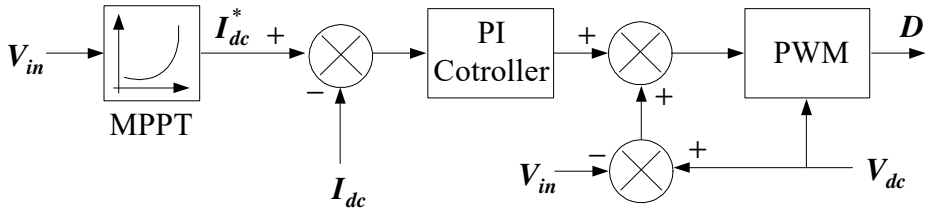


Figure 3.5 Control diagram of boost chopper.

Grid-side Control Structure: The bi-directional converter on the grid side is designed to control active power flow through the use of the DC-link voltage controller as well as to provide reactive power if desired [25]-[30]. Here, the control scheme employed for DC-link voltage control is based on droop control, since this control

scheme does not require any communication between the converters on both sides of the DC-link [28]. The DC-link controller output is the reference for the active current controller, whereas the reference for the reactive current is usually obtained from measured reactive power. Figure 3.6 shows the control structure of the grid-side converter. The power calculation bock corresponding to Q^{meas} signal is similar to the reactive power calculation block of the STATCOM VAR control mode.

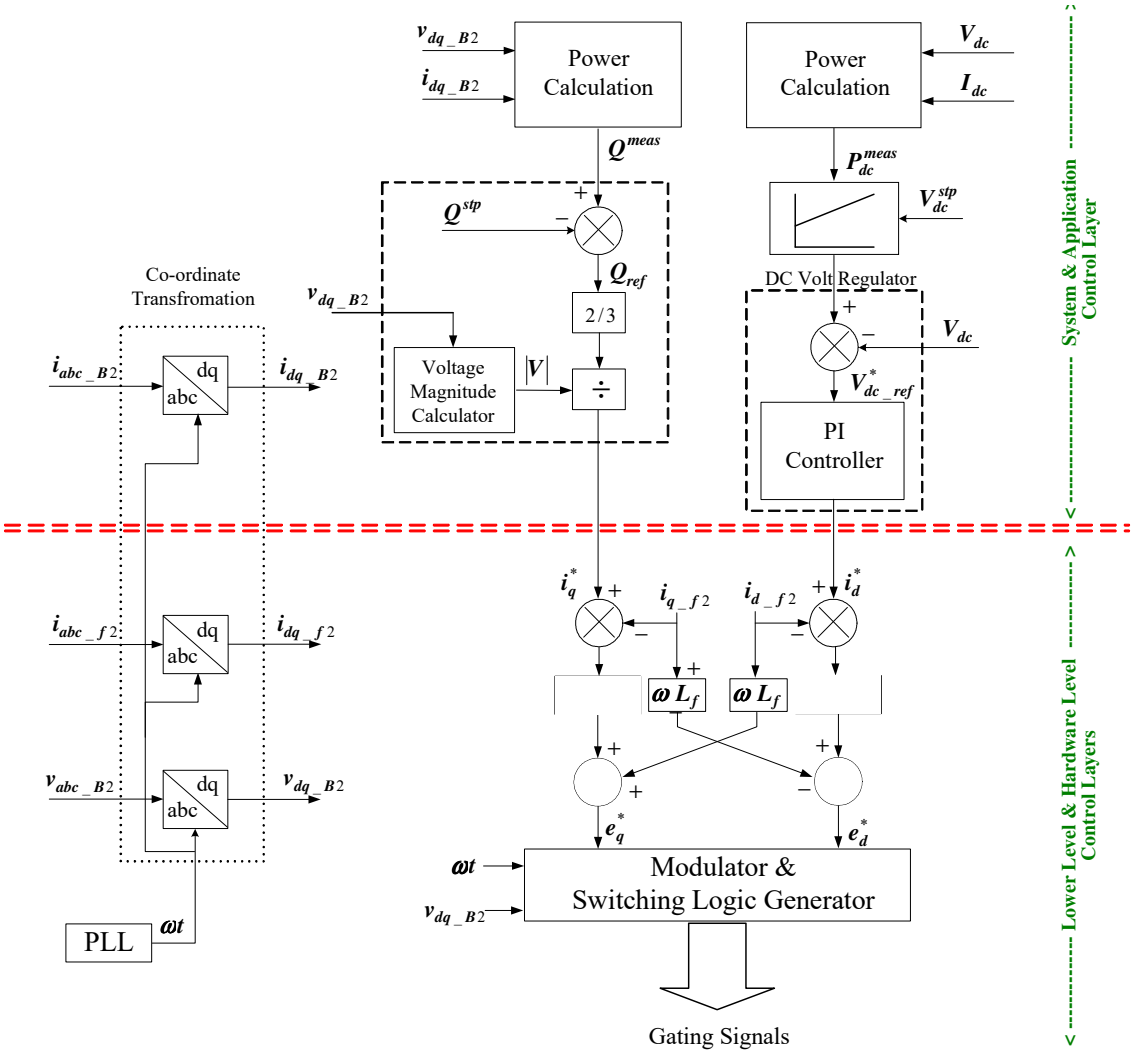


Figure 3.6 Control structure of grid-side converter.

3.2.2.2 HVDC Transmission with Two Stage Three-Phase VSC

A DC feeder transmission power system concept developed by ABB is considered, that is based on HVDC Light technology with a 6-pulse bipolar VSC for one bipolar unit [31] as shown in Figure 3.7. It consists of AC filters, transformers, converters, phase reactors, DC capacitors and DC cable. In this type of application a doubly-fed induction generator is used to convert mechanical power to electrical power.

Input-side Control Structure: The main target of input-end control structure is to implement a control scheme that provides voltage control depending on the available wind speed and frequency set point [28]. This controller converts the generator voltage to a DC voltage by maximizing the power production through the use of variable voltage/frequency for the wind turbine/farm despite low wind speeds. The wind turbine generator delivers active power and absorbs reactive power according to the wind speed [34]. The voltage stability is dependent on the demand for reactive power [35] and the reference for voltage control is obtained by using V-Q droop characteristics. Figure 3.8 shows a variable speed operation control structure for the wind turbine.

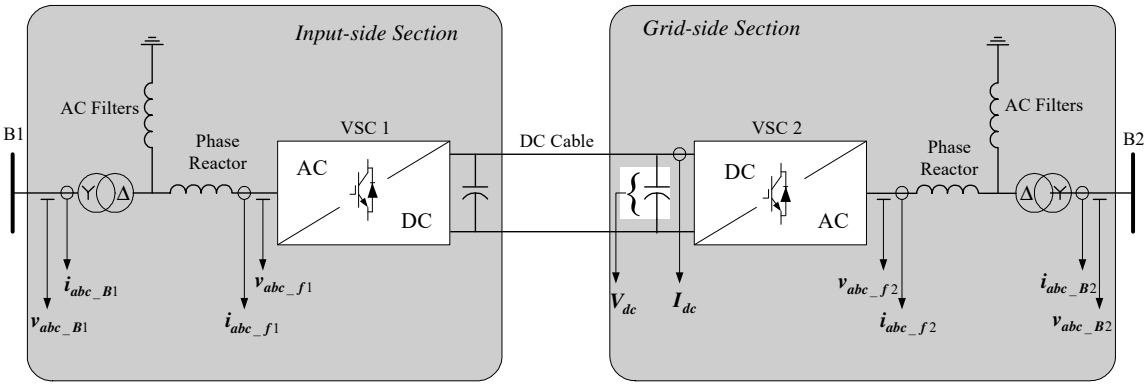


Figure 3.7 Power system diagram for the HVDC Light transmission system.

Grid-side Control Structure: For this application the control structure is similar to the one shown in Figure 3.6.

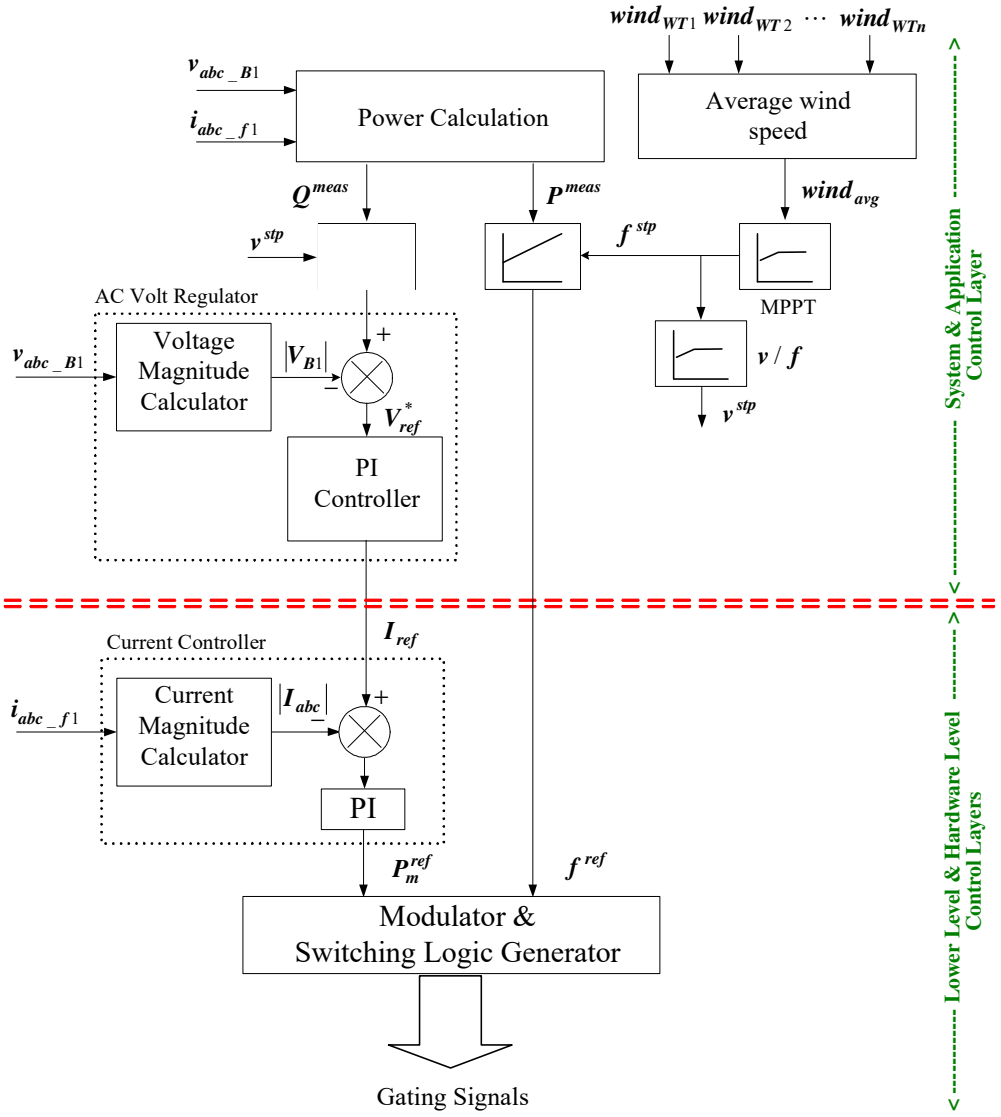


Figure 3.8 Control structure of input-side converter.

3.2.3 Active Rectifiers

Active rectifiers are very similar to the control structure of the STATCOM in VAR control mode with the exception that the DC voltage regulator is tuned to regulate the DC bus for conditions of active power transfer equal to the converter rating as opposed to supplying active power to balance losses. This is also nearly the same control structure as the grid side converter of a Mini-DC link application and some of the subsystems found in the STATCOM. For most active rectifier application the reactive current is regulated at zero to maximize power factor. The simplified control structure for an active rectifier is shown in Figure 3.9.

3.2.4 Vector Controlled Motor Drives

Two types of motors are considered for the motor drive study: induction motor drives and permanent magnet synchronous motor drives. For both of these drive systems, vector control is considered [53]. The motor side converter for an induction motor drive with the application and system layer separated from the lower layers is shown in Figure 3.10, and a permanent magnet synchronous motor drive is shown in Figure A.5. Both drives contain an outer control loop for speed regulation that provides a logical point for the separation of the system control and application control layers. From the viewpoint of the application layer control the converter is simply a current source and the application requires particular current components decomposed and/or scaled at the application layer. At the system control layer the machine operating conditions are translated into torque and flux references that govern the operation of a motor drive system.

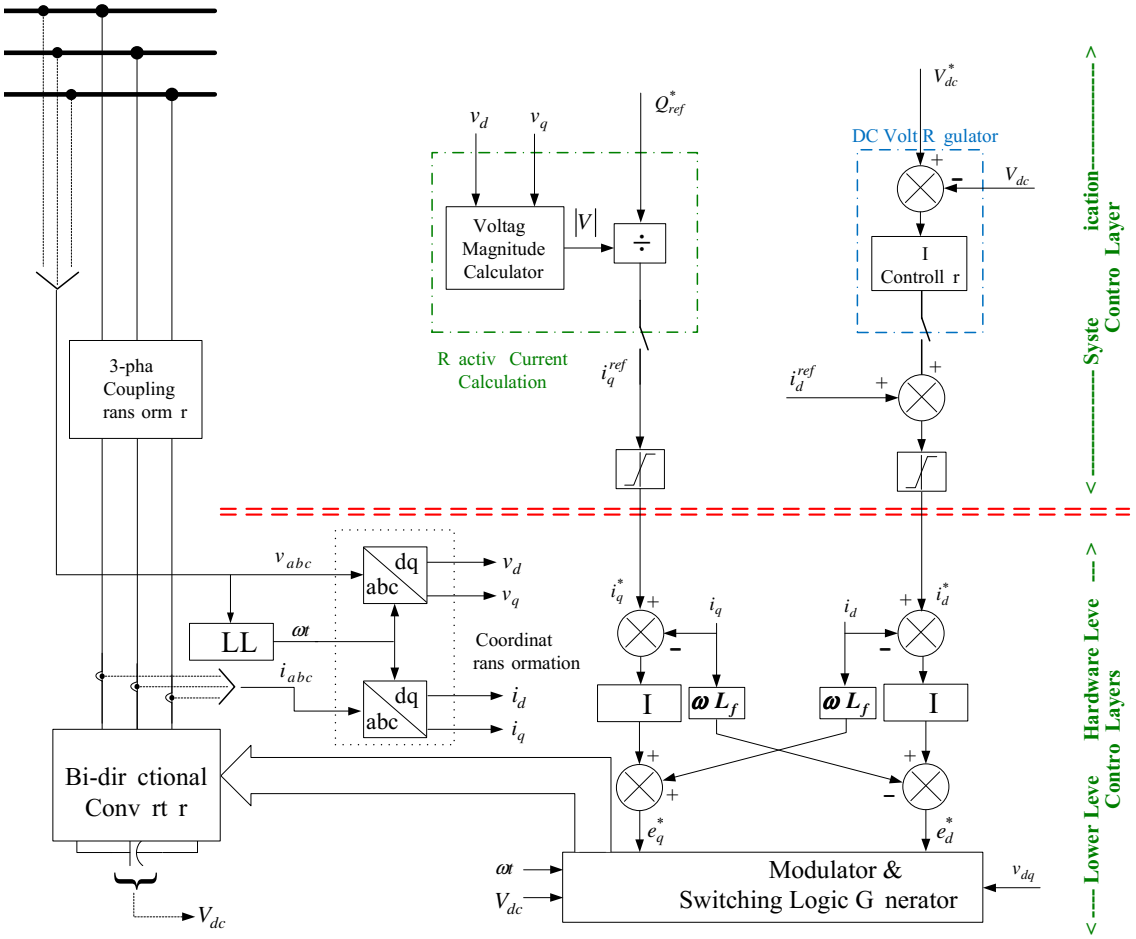


Figure 3.9 Control structure of an active rectifier.

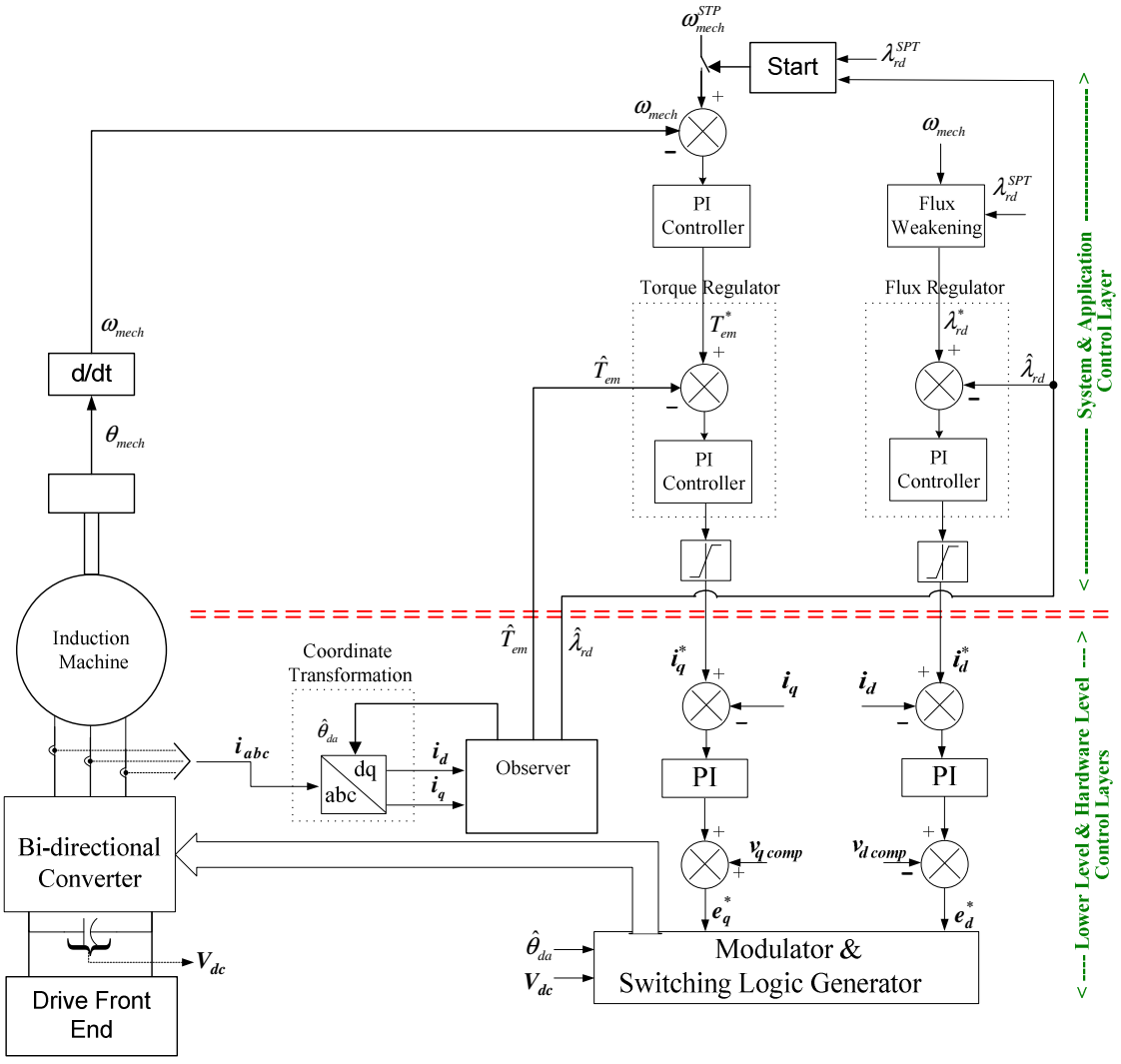


Figure 3.10 Rotor flux orientation vector control induction motor drive.

3.2.5 Active Filter Application and System Control

Shunt connected active filters, also sometimes referred to as active power filters and active compensators; inject a compensating component to cancel undesirable components of the current. A very large number of control algorithms have been proposed for use in active filter systems [40]-[51]. A more detailed description of these control algorithms is provided in Appendix A.3 and can be generalized as shown in Figure 3.11. It is the load current component extraction algorithm that determines the components of the current to be compensated at the cross section of the system where the active filter is connected based on measurements taken on the load side of the connection point. The reference signal is modified based on the output of the DC voltage regulator. Therefore, the extraction of the application and system control layers is made based on the reference outputs of the component extraction algorithm and DC voltage regulator as shown by the double dashed line.

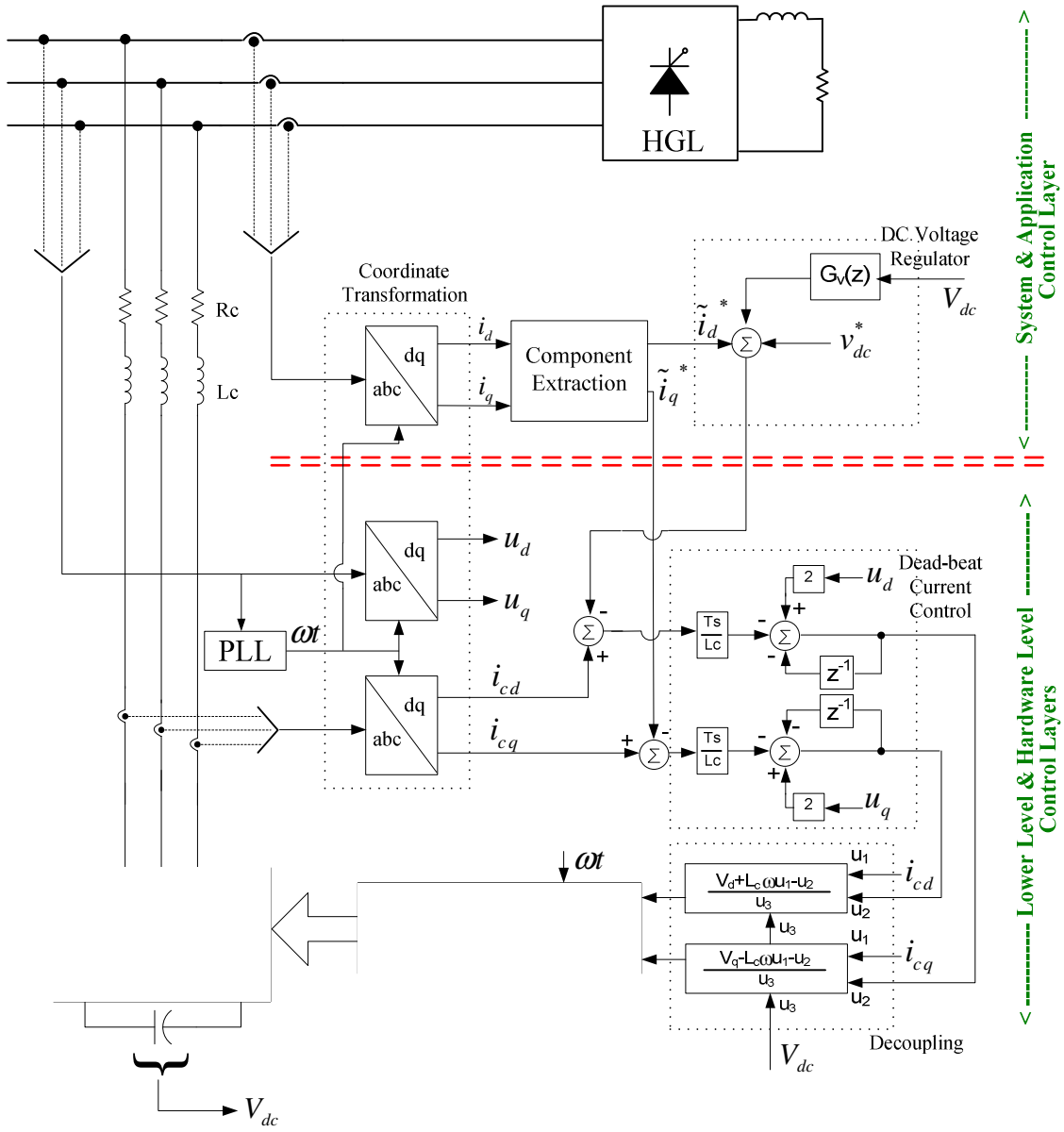


Figure 3.11 Typical active compensator control functions with division between lower functions and application plus system functions.

CHAPTER IV

SYSTEM CONTROL LAYER TO APPLICATION CONTROL LAYER PARTITIONING

After the group of application and system control layer functions are identified and separated from lower layers, the location of their boundary needs to be investigated to determine the partitioning that yields the best interface between the system and application control layers. The investigation of partitioning options and the resulting interface requirements is performed using the following steps:

1. *Partition options:* This step involves defining various functions that need to be handled in the system control and application control layers. For example the system control layer manages system level functions, such as transmission line Voltage Regulation, Stability Enhancement, Power Quality Improvement and Load Flow. Whereas the application control layer function is characterized through its active or/and reactive power control functions, voltage and current relationship.

2. *Functional analysis:* Detailed analysis of both the system control layer and application control layer functions and components has to be performed for all typical shunt connected converter applications.

3. *Temporal Study:* This step involves the determination of the interface signals and their bandwidth requirements for communication at the system and application layer partitioning as a function of switching frequency, affected current or voltage components and DC bus capacitor size [36].

In addition to performing partitioning based on the above steps (Application Control Layer to Converter Control Layer Partition), signals that cross any defined boundaries must be considered. Control signals crossing the layer boundaries have been divided into three broad categories: Primary Signals, Measurement Inputs, and Auxiliary Signals. Primary Signals refer to the signals associated with the main task of the layer. Measurement signals are any signal that must pass into an analog-to-digital converter or produced at the output of an analog-to-digital converter. Auxiliary Signals refer to those signals associated with the state of the converter system or that are passed through a layer boundary without being utilized within the receiving layer. It is expected that pass-through will be needed if the control structure is to be strictly hierarchical. If measurements are used in the layers below the application layer then they are considered to be passed upward from the lower hardware layers where the A/D converters are generally located. However, for some systems, the measurements may go directly to the application and system layers if they are not used in lower layers at all. In those cases there is an option that must be considered regarding pass-though. Auxiliary signals are not considered in the formulation of the partitions since they are not real-time signals in the sense that their timing is non-deterministic and, thus, they do not affect the temporal requirements of a boundary. However, various common auxiliary signals will be listed.

4.1 Partitioning Options for Individual Applications

In order to a develop partition criterion for system to application partitioning, generalized control structures for particular applications, derived from the review of the control architectures as discussed in Chapter III, are considered. In each case, the controls are simplified as much as possible while attempting to keep key elements distinct. Also, there are many advanced control techniques that may be found in the literature on various converter applications. In order to form a conservative partition study, the more simple controllers have been selected. In many cases, these controllers are PI controllers. Finally, the design approach is to translate controllers designed in the continuous time domain into the discrete domain using the bilinear transformation. This approach yields a conservative sampling rate since controllers realized directly in the discrete domain using more advanced techniques often achieve the same or even better performance with a lower sampling rate [60]. The sampling theorem is applied to any digital filters in the control subsystems. Using this approach enables the specification of a control interface that will accommodate systems with basic PI controllers as well as those with more advanced controllers. The detailed functional analysis and temporal requirement will be discussed more in Chapter V.

4.2 Generalized STATCOM Application and System Control

The four modes of operation correspond to various system missions while all control blocks within each mode subsystem work to relate those mission objectives into an expression of reactive current. Common summation points involving multiple modes can be considered as the most appropriate points for partitioning of the system and

application control layers. In STATCOM operation, the Transient Stability Enhancement Mode functions and Oscillations Damping Mode control subsystems require only system level measurement inputs. The final partition choice will be made based on the bandwidth requirements of the AC Voltage Regulator subsystem in comparison with a high pass filter with the time constant $\boldsymbol{T_W}$, along with the tradeoffs for the other ShCC applications in Table 2.1. The abbreviated signal list for the two partitioning options, summation points V_{ref}^{*} and i_q^{ref} , are compiled in Table 4.1 and Table 4.2 and shown in Figure 4.1 and Figure 4.2.

Table 4.1 Signal list for STATCOM applications – partition at V_{ref}^{*} summation

System Layer-Application Layer Boundary Signals	From System to Application Layer	From Application to System Layer
Primary Signals	1. Voltage reference into the voltage regulator for the coupling point voltage V_{ref}^{*}	1. Q_c, or quantity corresponding to reactive power at the fundamental frequency present in the converter phase legs 2. P_{sys}, or quantity corresponding to active power at the fundamental frequency present in the system
Auxiliary Signals	1. Mode selection data 2. Application control layer control parameter provisioning data 3. Converter control layer parameter provisioning data (pass-through)	1. Operating mode data 2. Application control layer parameter data 3. Converter control layer parameter data (pass-through)
Measurement Signals	None	None

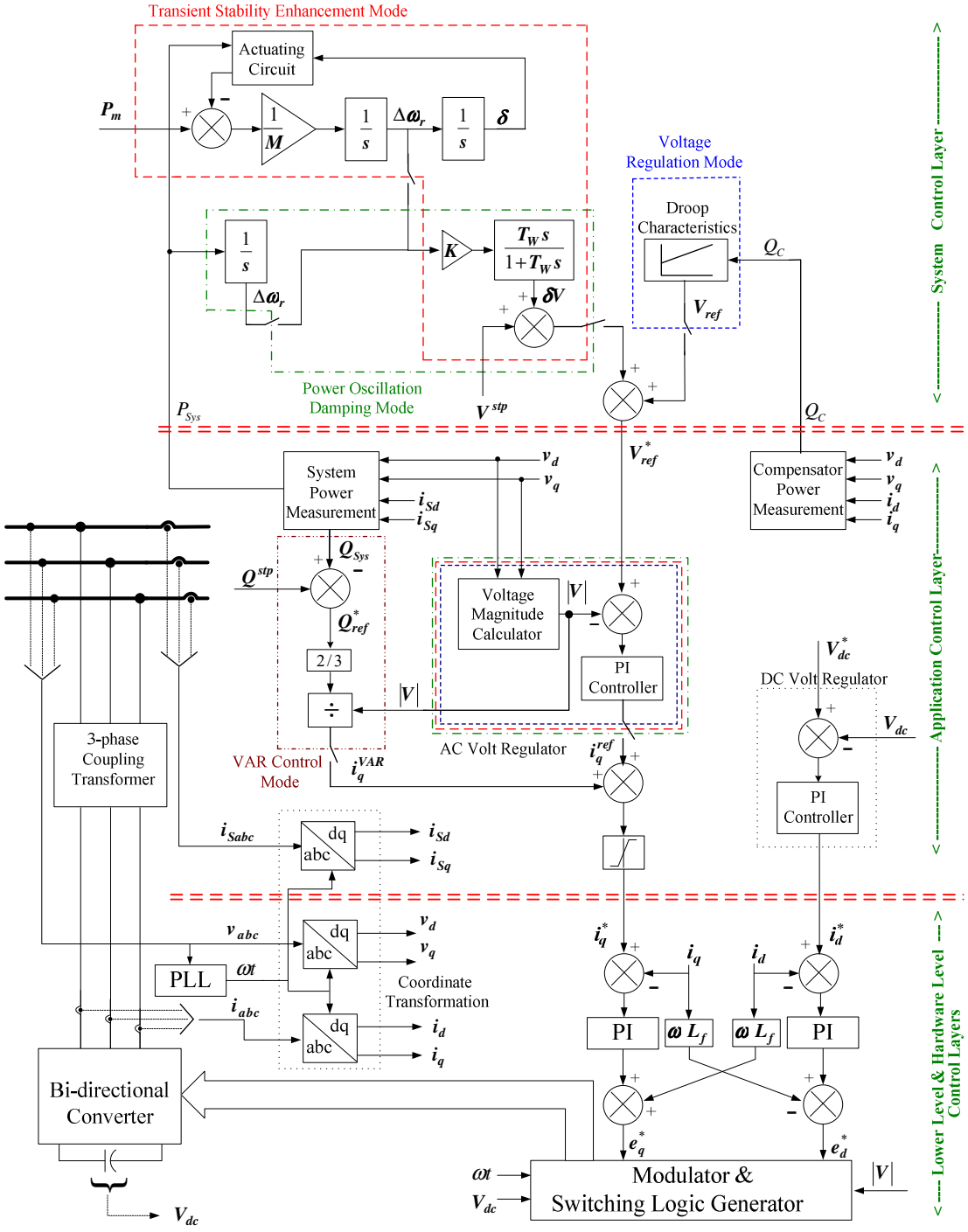


Figure 4.1 Generalized STATCOM control structure with system to application control layer partition at V_{ref}^{*}.

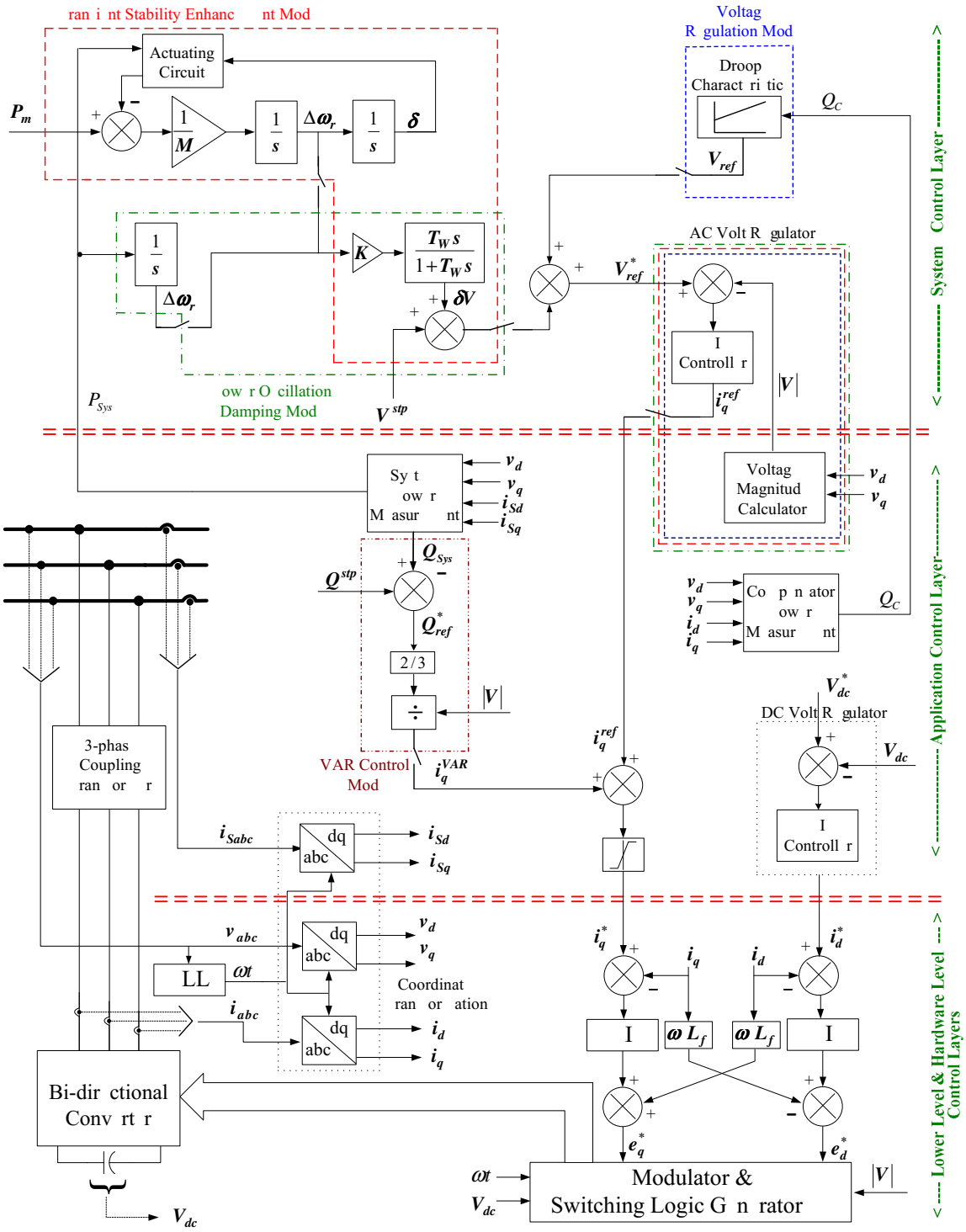


Figure 4.2 Generalized STATCOM control structure with system to application control layer partition at i_q^{ref} .

Table 4.2 Signal List for STATCOM applications – partition at i_q^{ref} summation

System Layer-Application Layer Boundary Signals	From System to Application Layer	From Application to System Layer
Primary Signals	1. Current Reference out of the AC voltage regulator i_q^{ref}	1. Q_c, or quantity corresponding to reactive power at the fundamental frequency present in the converter phase legs 2. P_{sys}, or quantity corresponding to active power at the fundamental frequency present in the system 3. $\lvert V \rvert$, or voltage magnitude at the point of converter connection.
Auxiliary Signals	1. Mode selection data 2. Application control layer parameter provisioning data 3. Converter control layer parameter provisioning data (pass-through)	1. Operating mode data 2. Application control layer parameter data 3. Converter control layer parameter data (pass-through)
Measurement Signals	None	None

4.3 Mini-HVDC Control Partition Options

The control system for any Mini-HVDC application with a converter attached to a fixed-frequency grid is shown in Figure 3.6. The main function of a Mini-HVDC system is to provide interconnection between two AC nodes and to control the active and reactive power flow independently.

In HVDC applications, reactive power can be controlled separately in each converter by the required AC voltage and the active power flow is controlled by

monitoring the DC voltage. The control system for a HVDC application with a converter attached to a fixed-frequency grid is shown in Figure 4.4. Note that it is essentially the same as the STATCOM with only the VAR control model. The difference is due to the use of a DC voltage regulator to manage active power flowing on the DC-link while the STATCOM DC voltage regulator simply counteracts the losses in the converter system to maintain a constant DC bus voltage. Mini-HVDC, as discussed in Section 3.2.2 can also be used to connect a wind farm to an AC grid to solve some potential problems, such as control of reactive power transfer between the DPGS and the grid, control of DC-link voltage and the grid synchronization.

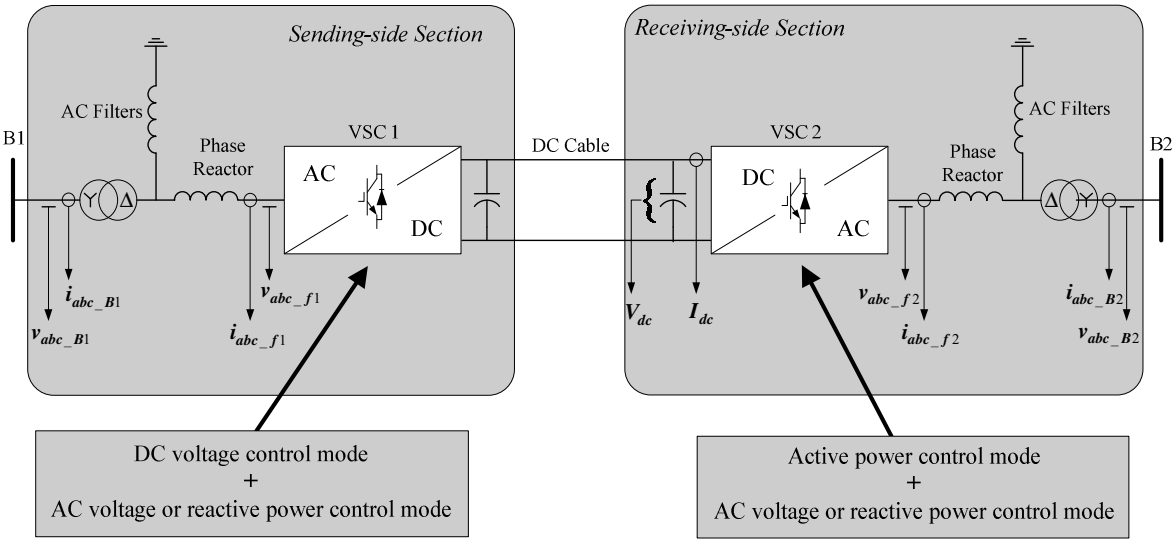


Figure 4.3 Overall system control of the VSC-HVDC power transmission system.

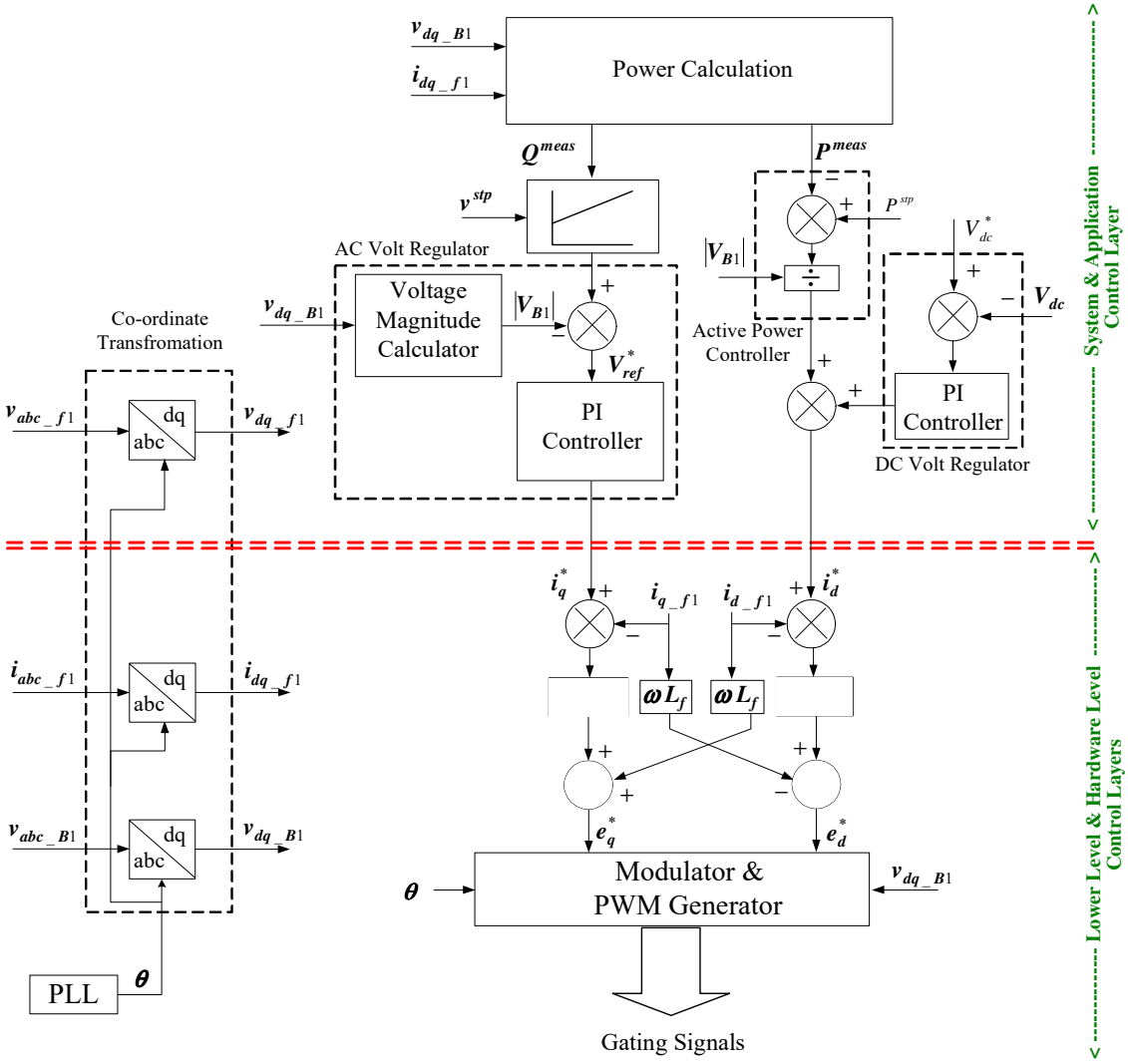


Figure 4.4 Control system of a grid connected converter.

In the layered converter control of the VSC-HVDC system, the lower-level control layers consist of a faster vector controller and the frequency controller (Grid Synchronization Controller). Furthermore, the lower-level controller is completed by additional system and application layer controllers, which supply the references for the lower-level layers. The additional layer controllers include the DC voltage controller, the AC voltage controller, the active power controller, and the reactive power controller. For example, as shown in Figure 4.3, either side of the link can choose between an AC voltage controller and a reactive power controller. Each of these application layer controllers will generate a reference value for the lower-level layer vector controller.

Obviously, not all application controllers can be used at the same time. Different applications require different choices of the control strategy. For example, the VSC-HVDC can control frequency and AC voltage if the load is a passive system. It can also control AC voltage and active power flow if the load is an established AC system. However, since the active power flow into the DC-link must be balanced, the DC voltage controller is necessary in order to achieve active power balance. Active power out of the DC-link must equal the active power into the DC-link minus the losses in the DC-link. Any difference would result in a rapid change of the DC voltage.

For separation of the system and application control layers, the common summation points are considered. The abbreviated signal list for two partitioning options, V_{ref}^{*} summation and i_q^{ref} summation, are compiled in Table 4.3 and Table 4.4 and shown in Figure 4.5 and Figure 4.6.

Table 4.3 Signal list for HVDC applications – partition at V_{ref}^{*} summation

System Layer-Application Layer Boundary Signals	From System to Application Layer	From Application to System Layer
Primary Signals	1. Voltage reference into the voltage regulator for the coupling point voltage V_{ref}^{*}	None
Measurement Signals	1. Quantity corresponding to reactive power set-point, Q^{stp} 2. Quantity corresponding to active power set-point, P^{stp}	1. Q_c, or quantity corresponding to reactive power at the fundamental frequency present in the converter phase legs

Table 4.4 Signal list for HVDC applications – partition at i_q^{ref} summation

System Layer-Application Layer Boundary Signals	From System to Application Layer	From Application to System Layer
Primary Signals	1. Current Reference out of the AC voltage regulator i_q^{ref}	None
Measurement Signals	1. Quantity corresponding to reactive power set-point, Q^{stp} 2. Quantity corresponding to active power set-point , P^{stp}	1. Q_c, or quantity corresponding to reactive power at the fundamental frequency present in the converter phase legs 2. $\lvert V \rvert$, or voltage magnitude at the point of converter connection.

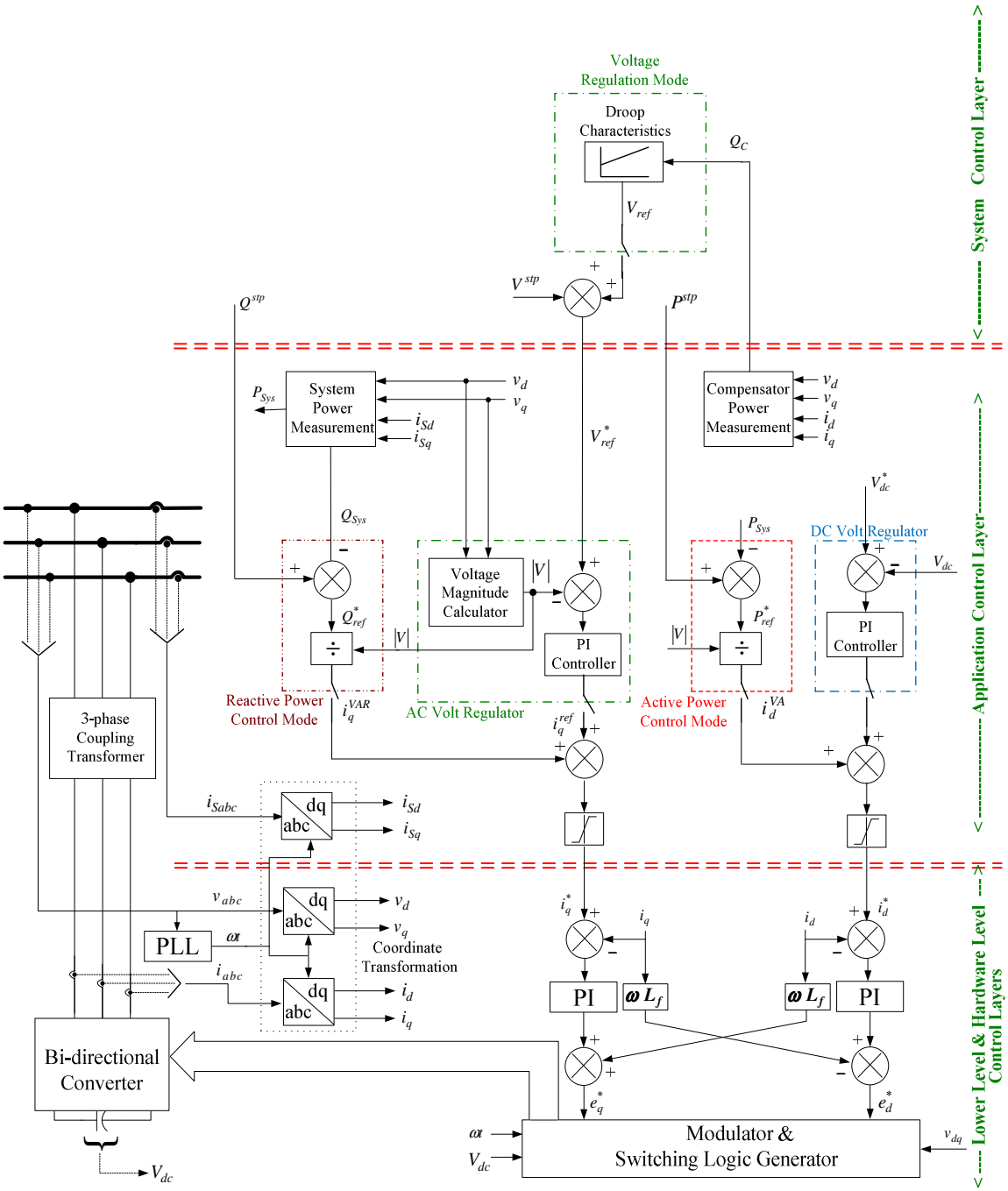


Figure 4.5 HVDC control structure with system to application control layer partition at V^*_{ref}

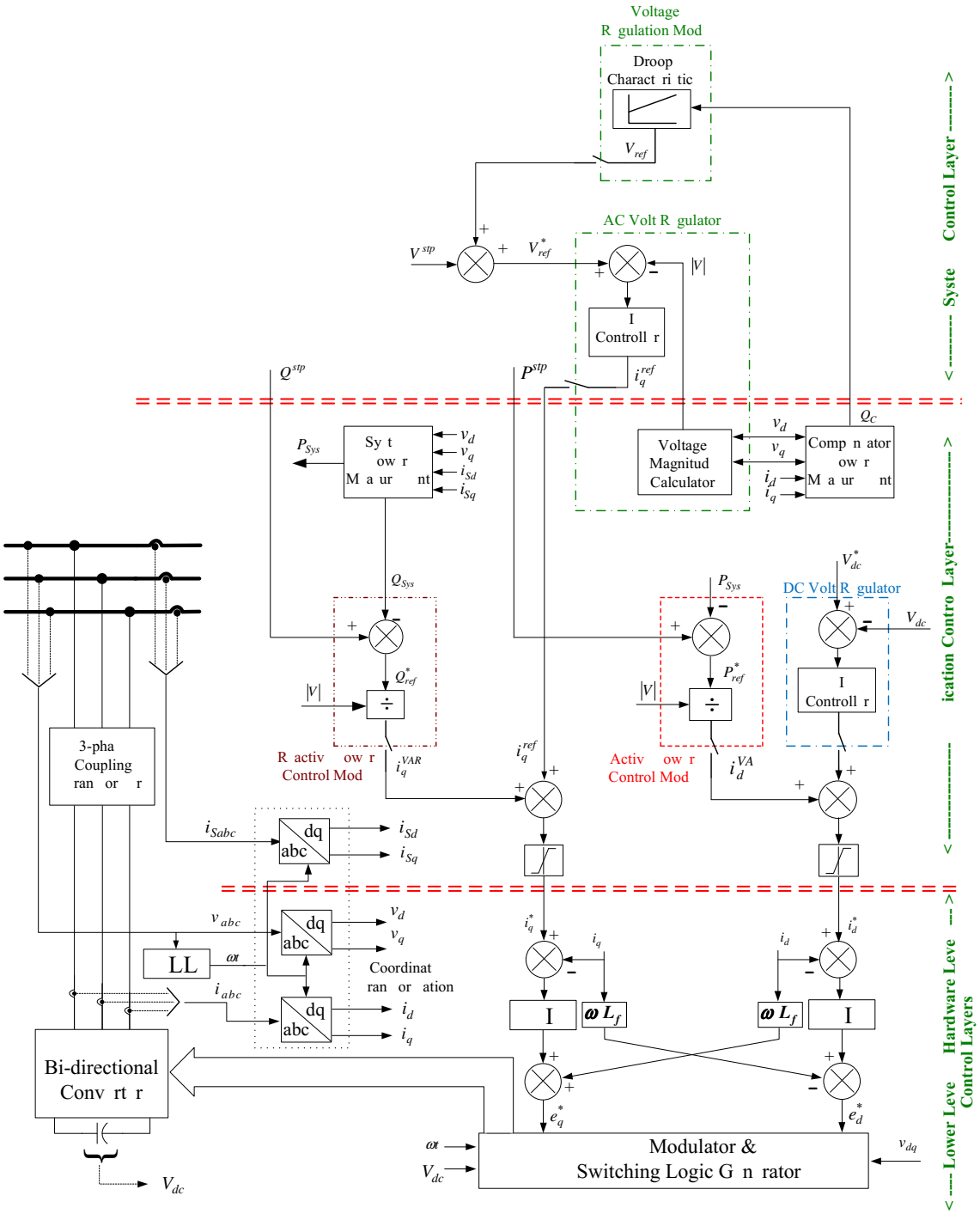


Figure 4.6 HVDC control structure with system to application control layer partition at i_q^{ref}

4.4 Active Rectifiers Control Partition Options

Active rectifiers are nearly the same as the grid side converter of Mini-HVDC application. In this case the boundary requirements are simple, as there is only one primary signal, the reactive power reference (Q^*_{ref}) at the system layer, which is fed into the application layer to regulate it at a set value. The reactive power reference is typically zero to maximize power factor. The control structure for an active rectifier is shown in Figure 4.7.

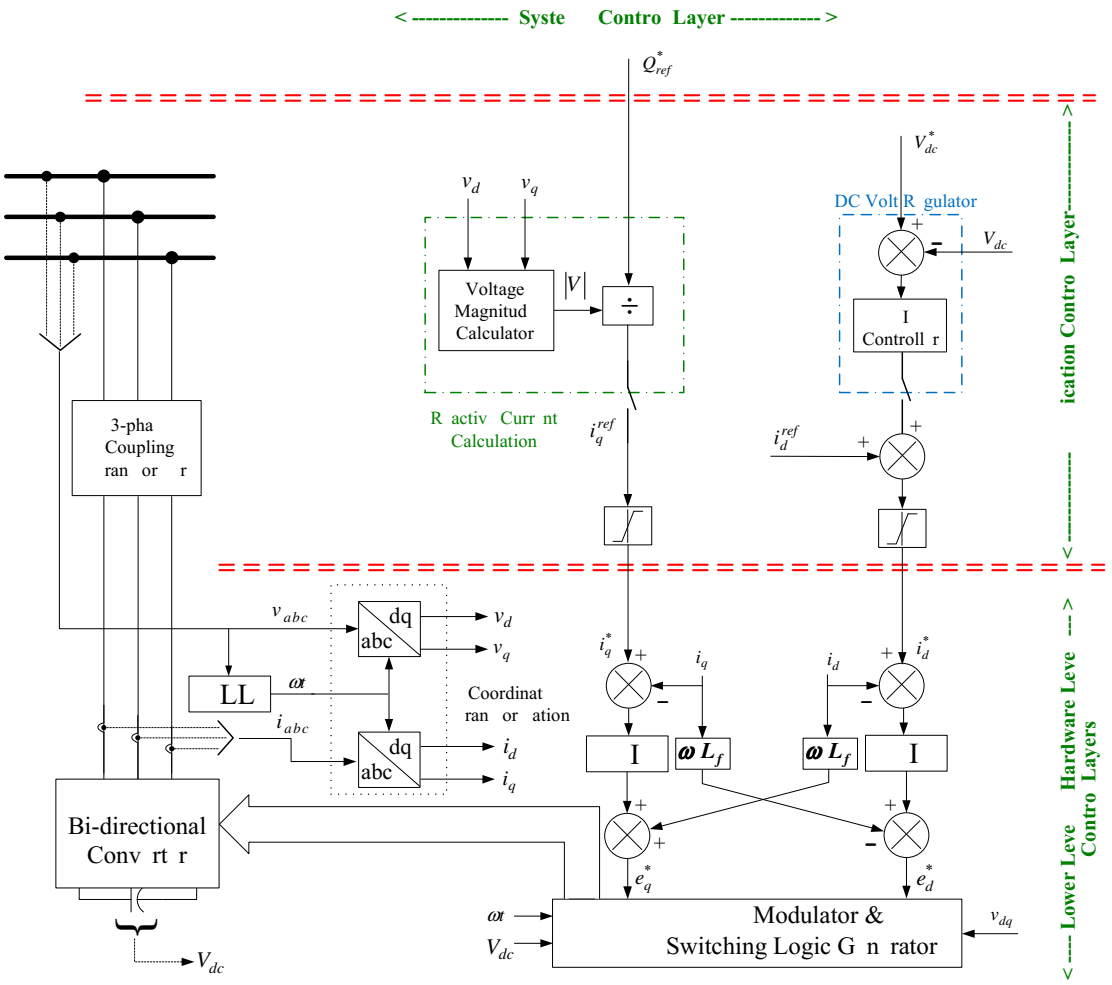


Figure 4.7 Control structure of an active rectifier.

4.5 Vector Controlled Motor Drive

A generalized diagram of a partitioned vector control drive system with the most promising draft partition is shown in Figure 4.8, although based on the flux and torque computation or estimation scheme some of the measurements shown may not be required. The partition of the DC permanent magnet drive is not shown here, since it is logical to partition it at the same point after the speed control loop. The signal list for vector drive applications is compiled in Table 4.5.

Table 4.5 Signal list for vector drive applications – partition at T_{em}* summation

System Layer-Application Layer Boundary Signals	From System to Application Layer	From Application to System Layer
Primary Signals	1. Torque Reference out of the speed regulator T_{em}^* 2. Flux Reference out of flux weakening function λ_{rd}^*	1. Estimated Flux $\hat{\lambda}_{rd}$
Auxiliary Signals	1. Mode selection data 2. Application control layer parameter provisioning data 3. Converter control layer parameter provisioning data (pass-through)	1. Operating mode data 2. Application control layer parameter data 3. Converter control layer parameter data (pass-through)
Measurement Signals	None	1. Speed measurement ω_{mech} (passed through application layer)

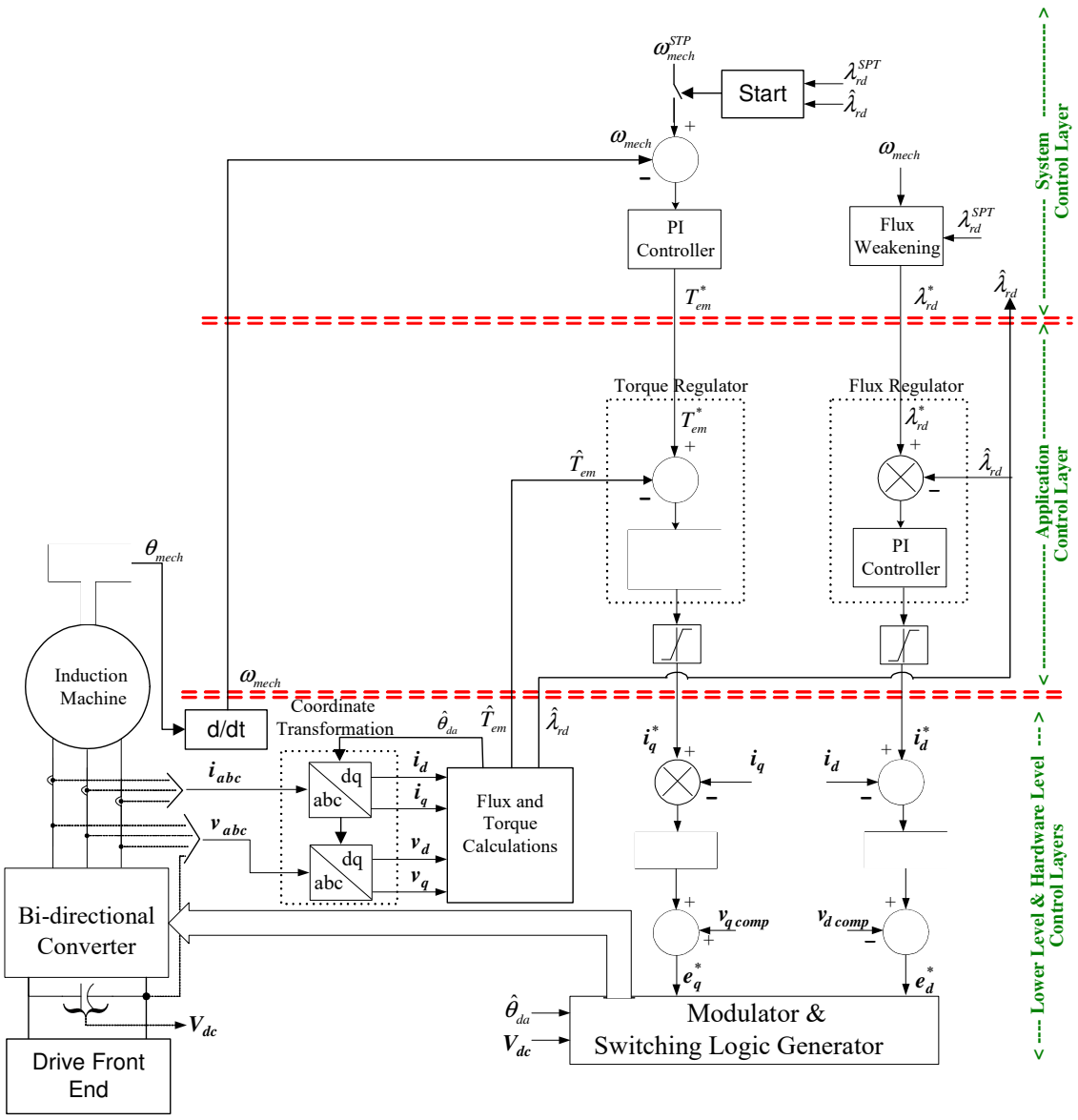


Figure 4.8 Rotor flux orientation vector control induction motor drive.

4.6 Active Filter Application and System Control

Active filter applications typically are fixed with respect to function so that the initial partitioning between the system and application control functions places the DC voltage regulator and component extraction algorithm within the application layer. In this case, the boundary requirements are simple, as there are no primary signals at the system level. Auxiliary signals are needed to provision the DC bus voltage set-point, filter coefficients, and current and voltage controller coefficients. Measurements of the load current, DC voltage and in some cases system voltage are used in the application layer but do not need to be passed to the system layer. The abbreviated signal list is compiled in Table 4.6 for a fixed function active filter system. The active filter is included here since other applications incorporate some of the active filter functions. For example, the D-STATCOM and some active rectifiers attempt to address power quality issues. Thus, some of the active filter subsystems will be included in the control partitioning of other ShCC applications. Also, compensation systems for applications with time varying power quality requirements are addressed by the multi-functional ShCC and will require Primary Signals at the interface [8].

Table 4.6 Signal list for typical fixed-function active filter applications

System Layer-Application Layer Boundary Signals	From System to Application Layer	From Application to System Layer
Primary Signals	None	None
Auxiliary Signals	1. Mode selection data 2. Application control layer parameter provisioning data 3. Converter control layer parameter provisioning data (pass-through)	1. Converter operating mode data 2. Application control layer parameter data 3. Converter control layer parameter data (pass-through)
Measurement Signals	None	None

CHAPTER V

PARTITION TEMPORAL REQUIREMENTS

This chapter summarizes partition options and makes observations based on the analysis performed in Chapter IV. Also, the temporal study of control functions based on switching frequency, time constants and control bandwidth is performed in order to define interface characteristics for each partition option. Although there can exist different criteria for an optimal partition, the most important feature of the partitioning should be the application independence. The objective of this chapter is to determine a minimum set of interface signals and their bandwidth requirements for communication at the system and application layer partition so that they are compatible across all applications discussed so far.

5.1 Partitioning Observations

Based on the analysis performed in Chapter IV, some underlying observations are summarized. In some cases, although the current components affected are the same, the method for the determination of the magnitude is different by application and may include multiple modes. A good example of this is the STATCOM. Both the STATCOM and the active filter affect reactive current while the active filter affects other components as well. However, the STATCOM uses reactive current to accomplish different overall system goals depending on the model of operation.

Application layer functions for active filters or active compensators are more complex while the system level functions are very basic. For example, the reference signal generator is complex with high sampling rate and bandwidth requirements for harmonic extraction. Many current components are affected, however, from the system point of view it does only one job. The STATCOM is the reverse, handing only one current component at the fundamental frequency while performing several different system level missions. Therefore, the application layer is very simple while the system control is complex. Both STATCOM and active filter applications do not involve the manipulation of active power. For Mini-HVDC applications the main objective is the transfer of active power from one AC system to another, however, the control structure is nearly identical to that of the STACOM VAR Control mode with regard to partitioning options. Active rectifiers, although they feed a DC bus are also nearly the same as the STATCOM VAR control mode with the exception of the DC control loop. Here the DC control regulates active power flow into the DC bus by maintaining the DC bus voltage within a specified range. Thus, the required DC control loop response is different from that of the STATCOM. Motor drive converters that utilize vector control with VSCs fit into the ShCC applications, since the converter control layer and lower layers act like a source of active and reactive current. Therefore, the torque and flux commands produced at the application and system control layers have similar partitioning requirements as the STATCOM and Active Rectifier for indirect rotor flux orientation control of an induction machine or indirect vector voltage control of permanent magnet synchronous machines.

Many of the control architectures are similar as can be seen by the separation and grouping that has been presented in Chapter III and Chapter IV. Most of the apparent differences arise from different reference frames and measurement quantities such as power or current components. Each control subsystem for the entire example set of applications has been mapped into the orthogonal current reference frame in order to eliminate apparent differences.

5.2 Temporal Study

The temporal study of the potential boundaries identified in Chapter IV is critical in determining the bandwidth requirements of the application layer to system layer interface. The interface bandwidth requirement for any converter system application is determined by the required sampling frequency of the slower layer, in this case the system layer, for that application. Thus, the temporal requirements of the layers with respect to their sampling frequencies must be determined. Controllers realized directly in the discrete domain using more advanced techniques often achieve the same or even better performance with a lower sampling rate as compared to converted continuous domain designs [60]. Therefore, as mentioned in the beginning of Section 4.1, controllers are designed in the continuous time domain and translated into the discrete domain using the bilinear transformation in order to determine a conservative sampling rate requirement. The sampling theorem is applied to determine the sampling rate requirement for digital filters in the control subsystems based on the maximum input signal bandwidth.

The following criteria for determining the temporal requirements of the layers have been developed:

1. The minimum possible sampling frequency of a layer is bounded by the control subsystem within that layer with the highest sampling frequency requirement of all layer control subsystems that receive a signal coming into the layer.
2. The maximum possible sampling frequency of a layer is bounded by the sampling frequency of the next lower (faster) layer. However, the sampling frequency should in general not be higher than the highest subsystem sampling frequency for all layer control subsystems that send a signal out of the layer.

5.2.1 STATCOM Control Partition Temporal Requirements

The temporal aspect of the partitioning options must be considered by quantifying the required sampling rates of each control subsystem. The various time constants and corresponding sampling rates are described below:

Signal Washout Block: Serves as a high-pass filter with time constant high enough to allow signals associated with the oscillations in rotor angle speed to pass unchanged. It corresponds to Transient Stability and Oscillation Damping modes. For this block, the bandwidth is determined by considering the time constant and the sampling period of highest frequency component involved in the input. Here, we may choose a sampling frequency of 6.0 Hz (by Nyquist Sampling Theorem) corresponding to the highest frequency, i.e. 3 Hz, component of the input signal based on the small signal stability analysis [20].

Droop Characteristics Block: In STATCOM voltage regulation mode, the voltage reference value for the reactive power compensation is calculated using the droop characteristics such as the voltage droop coefficient. The STATCOM operates in voltage regulation mode if there is any step change in the voltage reference of the system. The voltage regulation should meet the minimum settling time, typically a value of 5-6 cycles of the fundamental frequency [9], [37], of the given system, depending on the magnitude of the eigenvalues of the system and the bus voltage magnitude [20], [37]. This gives the required sampling frequency corresponding to Voltage Regulation Mode as 24Hz.

AC Voltage Regulator: The AC Voltage Regulator parameters are obtained from the minimum bandwidth requirement at the common summation point involving Oscillation Damping Mode, Transient Stability Enhancement Mode and Voltage Regulation Mode i.e. at system voltage reference point. In practical applications, proportional–integral (PI) controller is typically used to control the voltage response of the STATCOM [12], [13], [38]. From the above analysis, the PI control system was designed for a desired settling time of 6 cycles (0.1 seconds) corresponding to the Voltage Regulation Mode and the desired voltage set point is the initial voltage value of the terminal voltage bus. The PI controller gains were chosen accordingly to meet all specifications [60].

The given specifications (maximum overshoot, = 9.5%, and the settling time = 0.1sec) results in unit step response with undamped natural frequency of 57.16 rad/sec and the damped frequency of 45.75 rad/sec which results in oscillation damping period of 0.1373 sec. It is desirable to have at least eight samples per period (from analog to digital

conversion a conservative analysis) [60] in a digital controller implementation. Thus, a sampling frequency of 60Hz is sufficient.

DC Voltage Regulator: The bandwidth requirement of the DC Voltage Regulator primarily depends on the ratings of the DC-link capacitor bank of a voltage source converter [36]. A detailed examination of determining the size of the capacitor based on reactive power requirements of the converter and the highest allowed ripple current in the DC-link has been provided in Appendix B. In the present analysis the maximum sampling frequency requirement for the DC Voltage Regulation block is approximated to meet the minimum settling time of 1-2 cycles of fundamental frequency. The corresponding PI controller with required specifications as given above gives the required sampling frequency of 300Hz.

Summary of the sampling frequency requirements of various control subsystems for the STATCOM partition options is presented in Tables 5.1 and 5.2.

Table 5.1 Summary for determining the bandwidth – partition at V_{ref}^{*} summation

System Control Layer			
Operation Mode/ Subsystem	**Limiting Subsystem**	**Limiting Criteria**	**Sampling Frequency**
Oscillation Damping Mode	Signal Washout Block	Highest Frequency Component of input signal	6Hz
Transient Stability Mode	Signal Washout Block	Highest Frequency Component of input signal	6Hz
Voltage Regulation Mode	PI Controller	Settling time	24Hz
Application Control Layer			
AC Voltage Regulator	PI Controller	Settling time	60 Hz
DC Voltage Regulator	PI Controller	DC-link Capacitor Sizing	300 Hz

Table 5.2 Summary for determining the bandwidth – partition at i_q^{ref} summation

System Control Layer			
Operation Mode/ Subsystem	**Limiting Subsystem**	**Limiting Criteria**	**Sampling Frequency**
Oscillation Damping Mode	Signal Washout Block	Highest Frequency Component of input signal	6Hz
Transient Stability Mode	Signal Washout Block	Highest Frequency Component of input signal	6Hz
Voltage Regulation Mode	PI Controller	Settling time	60Hz
Application Control Layer			
DC Voltage Regulator	PI Controller	DC-link Capacitor Sizing	300 Hz

5.2.2 Mini-HVDC Control Partition Requirements

A study of the sampling requirements for VSC-HVDC application case and its partitioning options was similar to the STATCOM with VAR control model. The details of the sampling requirements of various control subsystems and partition options are presented in Tables 5.3 and 5.4.

Table 5.3 Summary for determining the bandwidth requirement– partition at V_{ref}^* summation

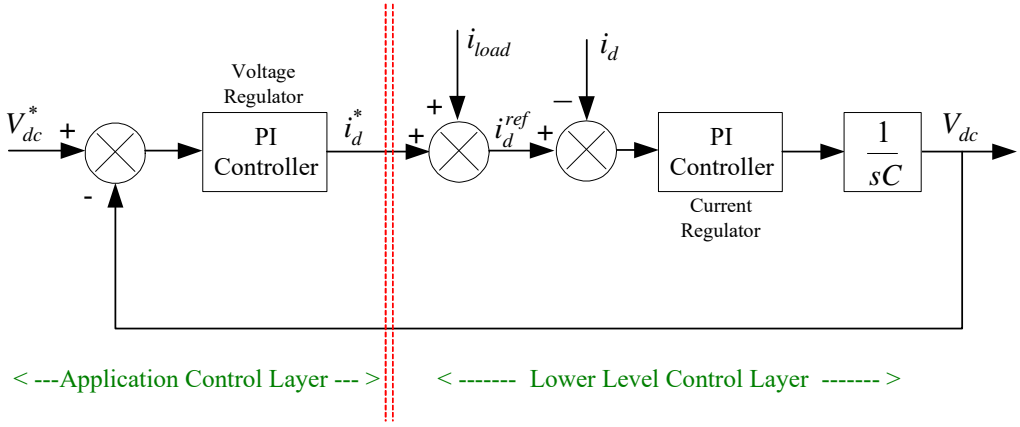
System Control Layer			
Operation Mode/ Subsystem	**Limiting Subsystem**	**Limiting Criteria**	**Sampling Frequency**
Voltage Regulation Mode	PI Controller	Settling time	24Hz
Application Control Layer			
AC Voltage Regulator	PI Controller	Settling time	60 Hz
DC Voltage Regulator	PI Controller	DC-link Capacitor Sizing	300 Hz

Table 5.4 Summary for determining the bandwidth requirement – partition at i_q^{ref} summation

System Control Layer			
Operation Mode/ Subsystem	**Limiting Subsystem**	**Limiting Criteria**	**Sampling Frequency**
AC Voltage Regulator	PI Controller	Settling time	60 Hz
Application Control Layer			
DC Voltage Regulator	PI Controller	DC-link Capacitor Sizing	300 Hz

5.2.3 Active Rectifiers Control Partition Requirement

Active rectifiers are nearly the same as the grid side converter of the Mini-HVDC application. For most active rectifier applications the reactive current is regulated at zero to maximize power factor. In some of the active front-ends for motor drives or active rectifiers, a feed-forward control strategy is employed in addition to feedback of the DC bus voltage regulator in order to achieve dynamic voltage regulation on the DC bus. Additionally, the feed-forward action makes it possible to obtain very rigid control of the DC-link voltage, even under extreme step load variations.



i_{load} = Feed-forward signal (DC-bus load current of the converter)

i_d = Active current component of converter current

Figure 5.1 The control block diagram of voltage loop.

This idea is based on the fact that the system response in the minor loop (current loop) is faster than the outer loop (voltage loop) and in the presence of a feed-forward signal, a minor current loop responds faster for unbalanced power on the DC bus, thus providing improved voltage regulation of DC-link voltage. Then, we can consider that the minor loop has reached the steady-state when proceeding with the outer loop. The control block diagram of the DC bus voltage regulator is depicted in Figure 5.1.

Sampling Requirements for the Feed-Forward Signal:

In the absence of a controller action, the time dependence of the voltage across the capacitor is given by following exponential equations:

$$V_{dc}(t) = V_{dc}(t_0)e^{-\frac{t}{\tau}} \qquad \text{(Capacitor discharging)} \quad (5.1)$$

$$V_{dc}(t) = V_{dc}(t_0)\left(1 + e^{-\frac{t}{\tau}}\right) \qquad \text{(Capacitor charging)} \quad (5.2)$$

Where, $V_{dc}(t_0) = V_{dc}^{*}$ = Magnitude of DC bus voltage at steady state, and τ = time constant corresponding to the load variation (dynamic load time constant).

For a given value of DC bus capacitance, C, and a load variation of Δi_{load} the dynamic load time constant τ is given as:

$$\tau = \frac{V_{dc}(t_0)}{\Delta i_{load}} C \qquad (5.3)$$

In the presence of a controller action, the depth/peak value of $V_{dc}(t)$ depends on following conditions:

1). Without the feed-forward signal: The depth/peak value of $V_{dc}(t)$ depends on the response time of the voltage regulator and sampling rate of the application control layer (the rate at which i_d^{ref} is updating).

2). With feed-forward signal: The depth/peak value of $V_{dc}(t)$ depends on the response time of the current regulator, sampling rate of lower level control layer and the additional time delay introduced on i_{load} (Feed-forward signal).

The performance of the feed-forward signal on the DC bus voltage regulation will be least effective if it's time delay is of the order of the application control layer's sampling rate and most effective if its time delay is of the order of lower level control layer's sampling rate.

Thus the sampling rate for the feed-forward signal will be chosen in accordance with the desired depth/peak value of $V_{dc}(t)$. Accordingly the signal will be passed either through the application control layer or the lower level control layer and it will never cross the system to application partition boundary. The sampling requirements of various control subsystems and partition options are similar to Mini-HVDC control partition requirements.

5.2.4 Motor Drive Control Partition Temporal Requirements

In general, only a subset of motor drives that do not require precise position control or very high-speed operation can fit into the same temporal partitioning as grid connected converter systems. Larger machines (hundreds of kW to several MW) do typically fit into the same temporal partitioning as the grid connected converter

applications. For example, permanent magnet motors having a 15 Nm peak transient torque and with a base speed of 1000 rpm and maximum speed of 3000 rpm can have an acceleration time to base speed of 7 – 10 ms and to maximum speed of 40-50 ms [52]. Furthermore, modern induction machines can have a peak transient torque build up in 2 – 5 ms at standstill with the flux already present in the machine [52]. These time ranges indicate that the application control layer would require a sampling time on the order of a few milliseconds while the system layer would require a sampling time in the 10's of milliseconds range.

In order to determine the range of sampling time of the system control layer the current control (or torque control) loop must be considered. Then the system control layer containing the speed controller can be set at least one order of magnitude slower. For a simple PI controller the sampling time of the torque control loop is determined by the electrical time constant of the machine as determined by the stator parameters. Also, in modern drives that do not require high precision there is often a state observer to estimate the flux and torque based on stator current measurements. If the flux and torque calculation control subsystem is located in the system control layer then the temporal requirements are much higher for that layer for reasonable magnitudes of torque ripple.

5.2.5 Active Power Filter Temporal Requirements

As mentioned in Section 4.6, there are no Primary Signals that will pass through at the system level to application level and vice versa. For addressing the power quality issues such as reactive-power compensation and balancing of three-phase systems, the temporal requirement is very similar to STATCOM and active rectifiers. But, the most

common popular filters are those which compensate for the reactive-power and harmonic currents in order to maintain the supply current completely free of harmonics and in phase with the supply voltage. The requirement for harmonic compensation in active filter applications will drastically increase the application layer temporal requirements. The requirements primarily depend on the highest order harmonic component that has to be compensated. For example, the application layer sampling requirement can be as high as 3000 Hz for a highest order compensating harmonic component, if it is the 25th order harmonic component of fundamental frequency.

5.3 Summary of Partition Options and Requirements

A summary of partition interface signals along with their required sampling frequencies for possible grid connected and vector controlled motor drives that do not require precise position control or very high speed operations applications are given in Table 5.5. The conventions for the input and output signals at the system to application interface are given in Figure 5.2.

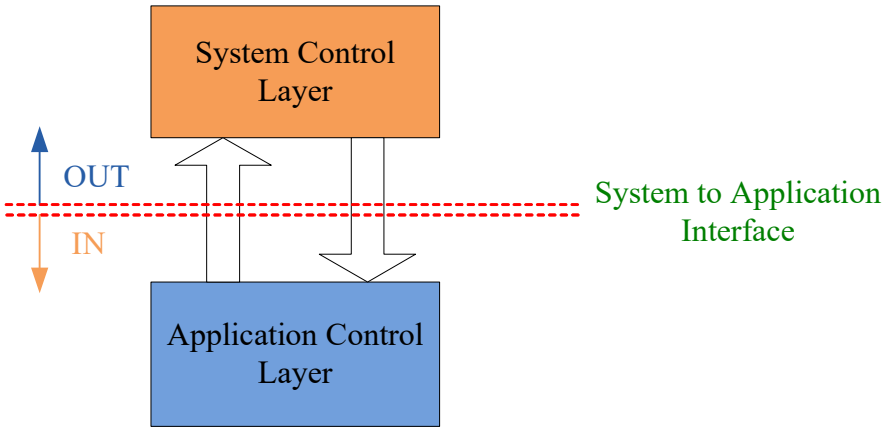


Figure 5.2 Signal convention at the system to application partition interface.

Table 5.5 Partitioning interface signals list with system and application layer sampling requirement.

Individual Application	Primary Signals In	Primary Signals Out	Measured Signals In	Measured Signals Out	System Layer Sampling Req.	Application Layer Sampling Req.
STATCOM Partitioning at V_{ref}^{*}	V_{ref}^{*}	None	None	Q_C , P_{sys}	30 Hz	300Hz
STATCOM Partitioning at i_q^{ref}	i_q^{ref}	None	None	Q_C , P_{sys} , $\lvert V \rvert$	60 Hz	300Hz
HVDC Partitioning at V_{ref}^{*}	V_{ref}^{*}	None	Q^{stp} , P^{stp}	Q_C	30 Hz	300 Hz
HVDC Partitioning at i_q^{ref}	i_q^{ref}	None	Q^{stp} , P^{stp}	Q_C , $\lvert V \rvert$	60 Hz	300 Hz
Active Rectifier/Drive Front End	None	None	Q_{ref}^{*}	None	30Hz	300 Hz
Drive Back End	T_{em}^{*} , λ_{rd}^{*}	None	None	ω_{mech} , $\hat{\lambda}_{rd}$	100 Hz	1000 Hz

CHAPTER VI

MODELING AND SIMULATIONS FOR PARTITION REQUIREMENT VALIDATION

The objective of this Chapter is to validate the system and application layer sampling requirements summarized in Table 5.5 through modeling and simulation in MATLAB/Simulink.

6.1 STATCOM Simulation Model and Results

Figure 6.1 shows the power system representation applicable to a generation station consisting of four 555 MVA, 60 Hz units [20]. The network reactances shown in Figure 6.1 are in per unit on 2220 MVA, 24kV base (referred to the LT side of the step-up transformer). The system resistances are assumed to be negligible.

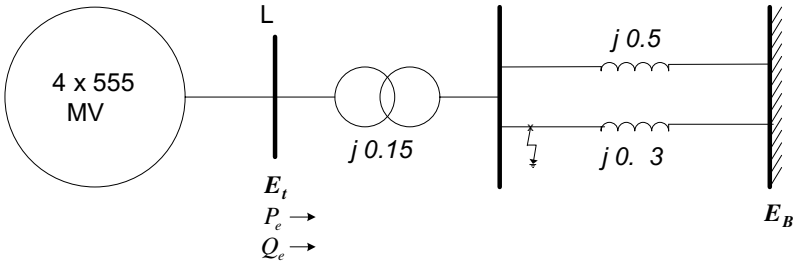


Figure 6.1 Power system representation consisting of four 555 MVA, 24 kV, 60 Hz units.

A reference signal is extracted from this system which can be used in the STATCOM controller to enhance the system stability limits. The detailed simulation model of this system is explained in Appendix C.1. The initial system-operating condition in per unit on 2220 MVA and 24 kV base, is as follows:

$P_e = 0.9$, $Q_e = 0.436$, $E_t = 1.0 \angle 28.34^0$, $E_B = 0.90081 \angle 0^0$, $X_d^{'} = 0.3$, $H = 3.5$ MW.s/MVA and $K_D = 0$,

where, P_e is real power flow into the transmission system, Q_e is reactive flow into the transmission system, E_t and E_B are the terminal and bus voltages respectively, H is the inertia constant of generation unit, $X_d^{'}$ generator transient reactance, and K_D is the damping torque coefficient.

The objective of this example is to extract stability characteristics of the system with respect to generator rotor angle variation. The rotor angle oscillations and line currents are obtained using following equations:

The active power (P_e) and the reactive power (Q_e) at the E_t end are given by:

$$\begin{aligned} P_e &= E_t(E_B \sin\delta)/X \\ Q_e &= E_t(E_t - E_B \cos\delta)/X \end{aligned} \tag{6.1}$$

Similarly the active and reactive components of the current at E_t end are:

$$\begin{aligned} i_d &= E_B \sin\delta / X \\ i_q &= (E_t - E_B \cos\delta)/X \end{aligned} \tag{6.2}$$

STATCOM control functions partitioned into two possible partitioning options between the application and system layers along with the lower level control functions have been modeled and implemented in MATLAB/Simulink using Simulink's sample-time colors feature to display the relative sampling rates of subsystems involved. Figure

6.2 shows the implementation of basic STATCOM transfer block control functions with the partition between the application and system functions at the V_{ref}^{*} summation. Figure 6.3 shows the implementation of basic STATCOM transfer block control functions with the partition between the application and system functions at the i_q^{ref} summation.

In the simulation model, the power system is implemented in the continuous time domain and the controllers in the discrete domain. The system measurements are passed to different layers based on their respective sampling frequency requirements. The simulation results are presented in the following subsections for all four STATCOM application modes with the partition between the application and system functions at V_{ref}^{*} and i_q^{ref} summation points. In system realization, the modeling and simulation was done to demonstrate the developed partitioning criteria not to study the stability, voltage regulation and VAR control analysis.

6.1.2 Oscillation Damping Mode

Power Oscillation damping generally requires the variation of voltage at the terminal of the compensator in proportion to the rate of change of the effective rotor angle speed $\Delta\omega_r$ [9]. A signal corresponding to the change in rotor angle speed is added to the fixed voltage signal V_{ref} . The added signal causes the voltage to oscillate around the fixed operating point so as to aid system damping. The terminal voltage increases when $\Delta\omega_r$ is positive (in order to increase the transmitted electrical power and thereby to oppose the acceleration of the generators) and decreases when $\Delta\omega_r$ is negative (to reduce

the transmitted electrical power and thereby oppose the deceleration of the generators). Figure 6.4 and 6.5 shows the simulation results of the variation of voltage at the terminal (E_t) of the compensator in proportion to change in the rotor angle speed $\Delta\omega_r$. Here, the magnitude of the rotor angle speed is scaled to show the variation of the terminal voltage in proportion to the rotor angle speed.

6.1.3 Transient Stability Enhancement Mode

A STATCOM performs Transient Stability Enhancement by improving the first swing stability limit of a power system. The control scheme used here improves the stability limit initially by maximizing the deceleration area and later fully utilizing it in counter balancing the acceleration area [21]. This requires continuing operation of the STATCOM at fully capacitive rating until the machine speed reaches a reasonable negative value during the first return journey. Afterwards, the control can be switched to continuous type to improve system damping in subsequent swings. This model structure is similar to that presented in Section 6.1.2 for oscillation damping mode. In addition, limits on system variables are modeled using an actuating circuit control block. Here, the variation of terminal voltage in proportion to change in the rotor angle speed is of primary interest, related to the stability of the system.

Figures 6.6 and 6.7 depict the simulation results showing the variation of voltage at the terminal (E_t) of the compensator in proportion to change in the rotor angle speed $\Delta\omega_r$, where during the first swing the STACOM operates at full capacitive rating and afterwards it operates in continuous oscillation damping mode.

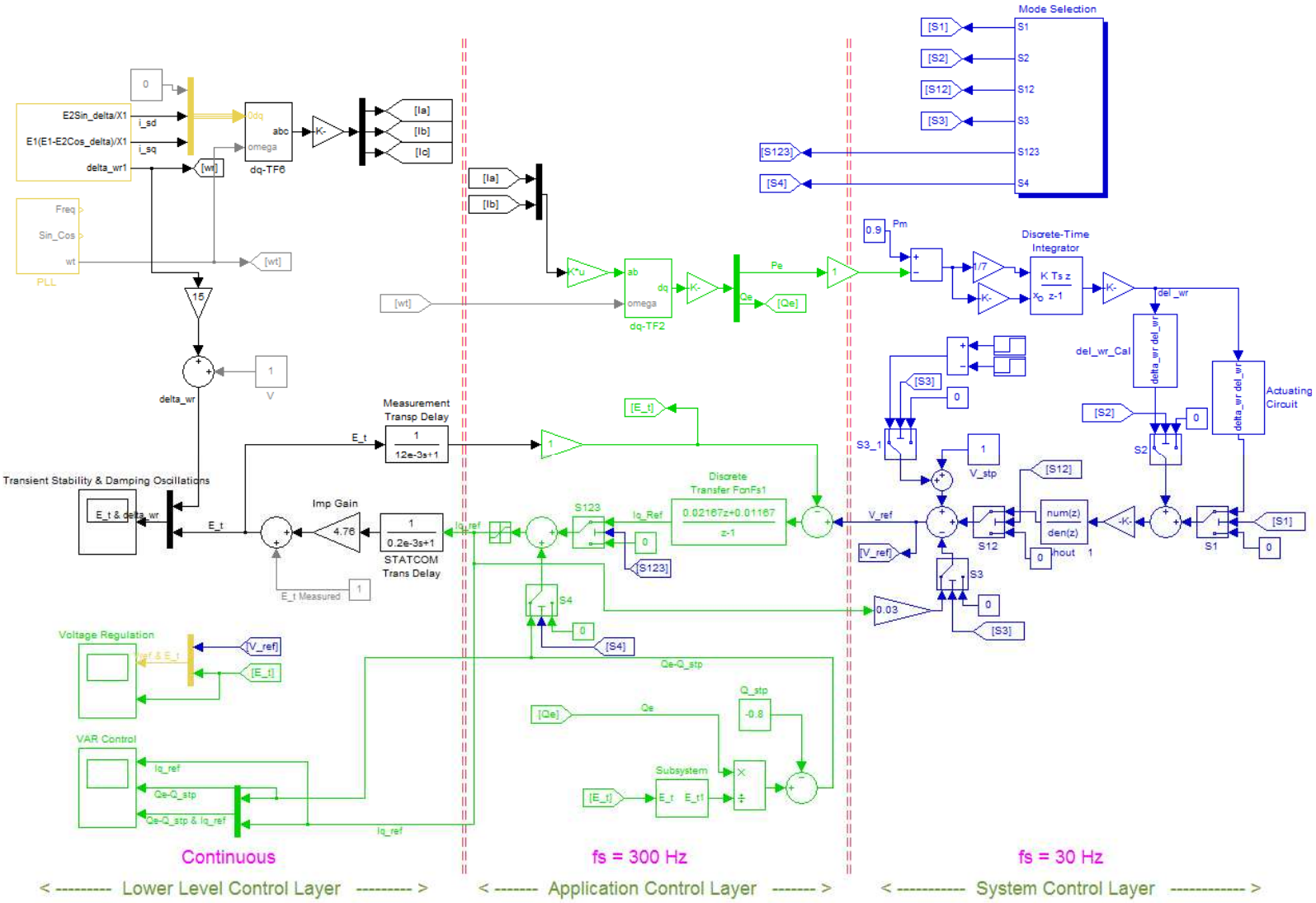


Figure 6.2 Simulink implementation of basic STATCOM transfer block control functions with partition at V_{ref}^{*} summation

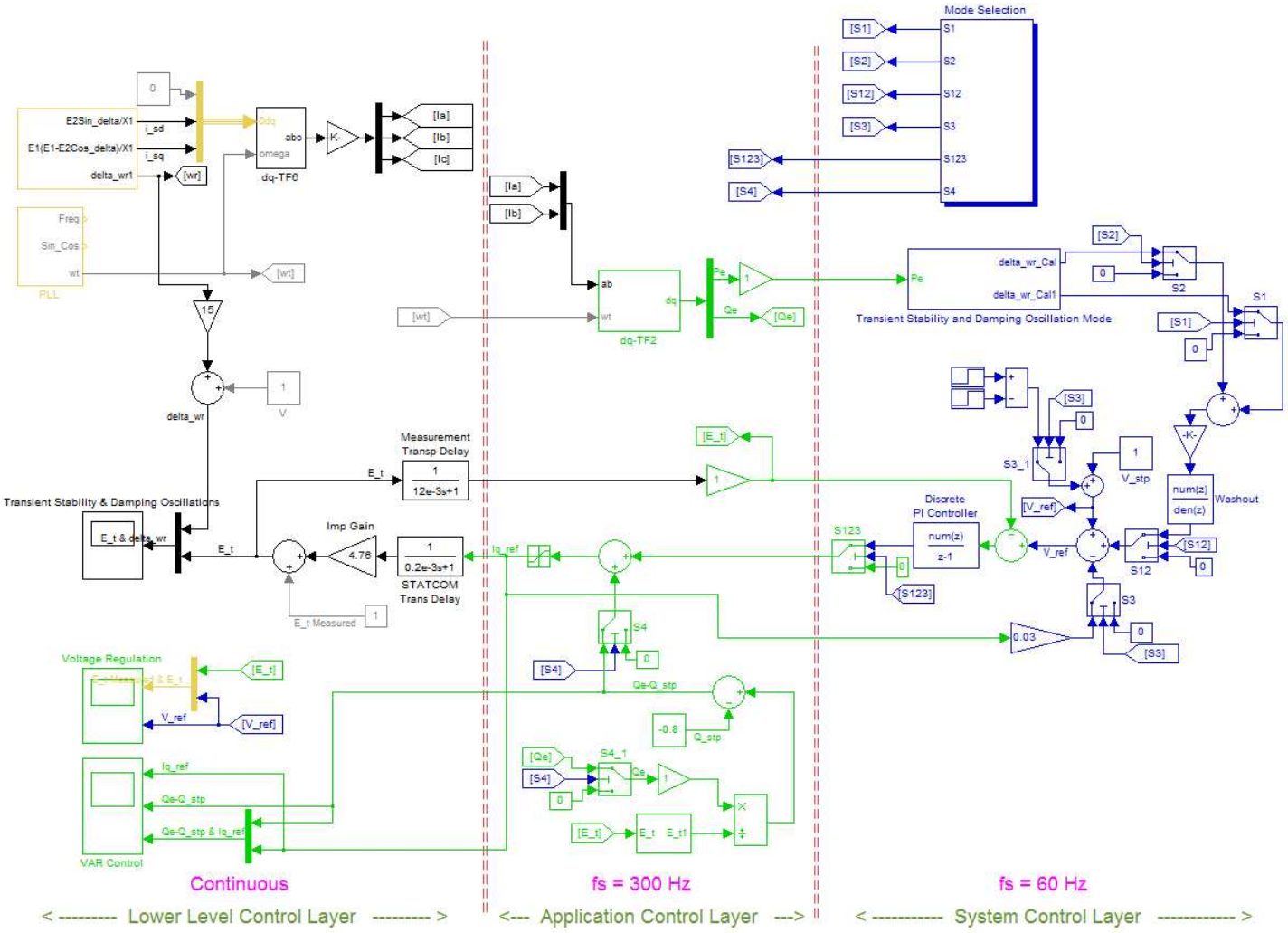


Figure 6.3 Simulink implementation of basic STATCOM transfer block control functions with partition at i_q^{ref} summation.

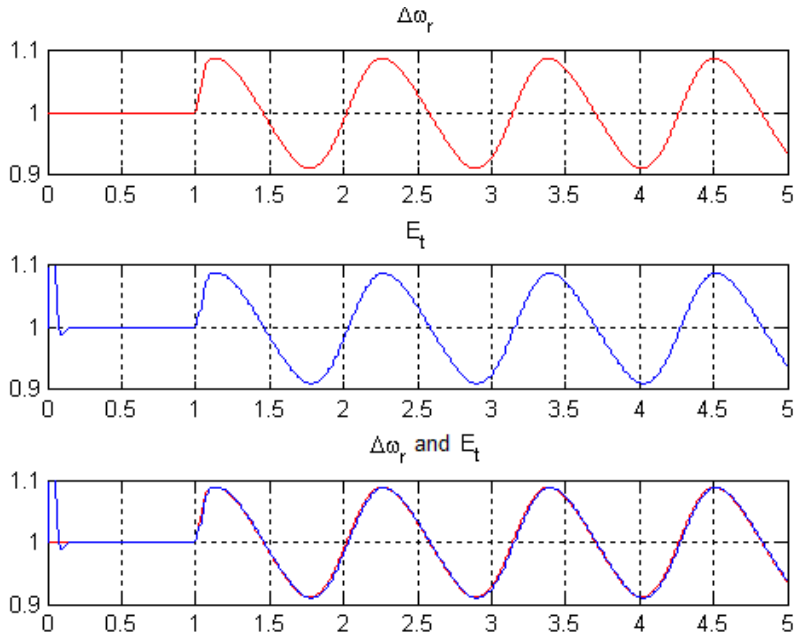


Figure 6.4 Variation of terminal voltage (E_t) in proportion to the rotor angle variation in STATCOM oscillation damping mode - V_{ref}^{*} partition

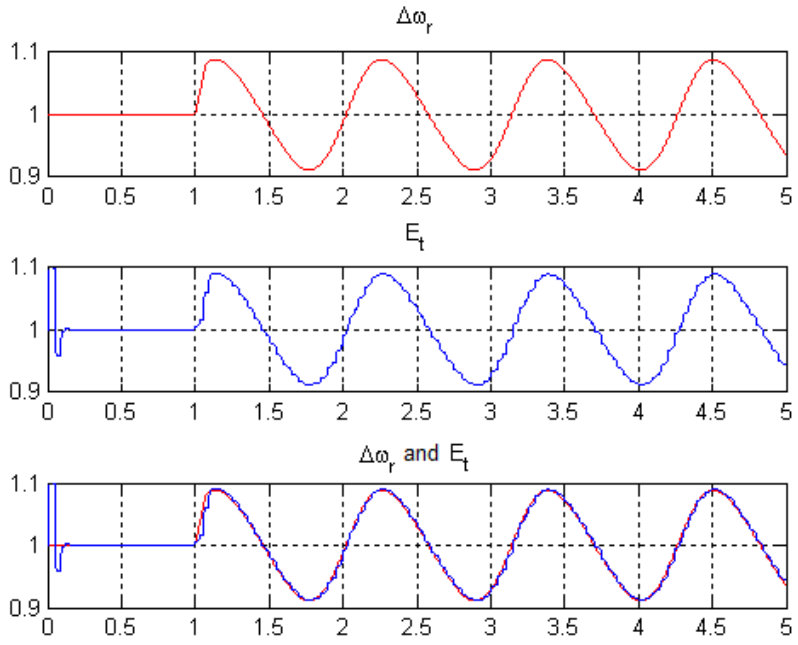


Figure 6.5 Variation of terminal voltage (E_t) in proportion to the rotor angle variation in STATCOM oscillation damping mode - i_q^{ref} partition

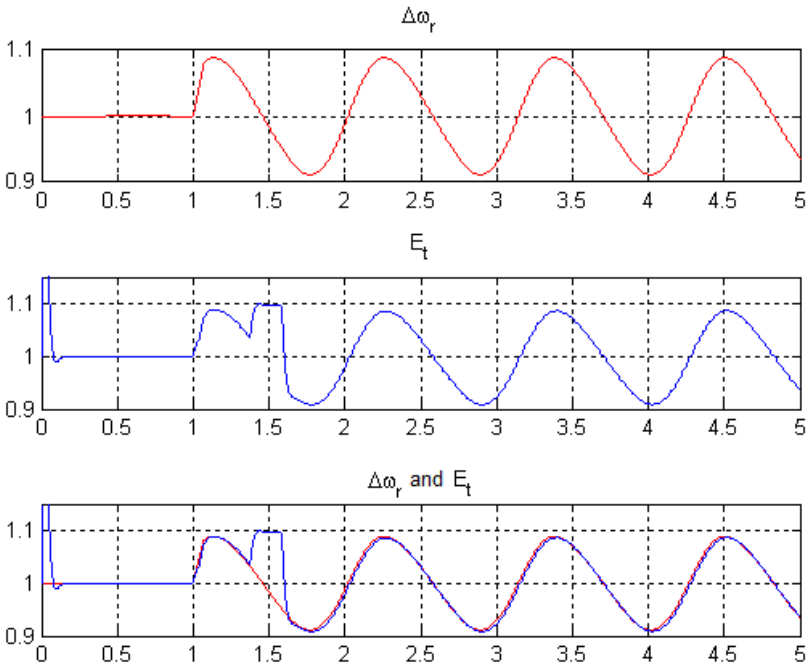


Figure 6.6 Improvement of first swing stability limit with STACOM Transient Stability Enhancement - V_{ref}^{*} partition.

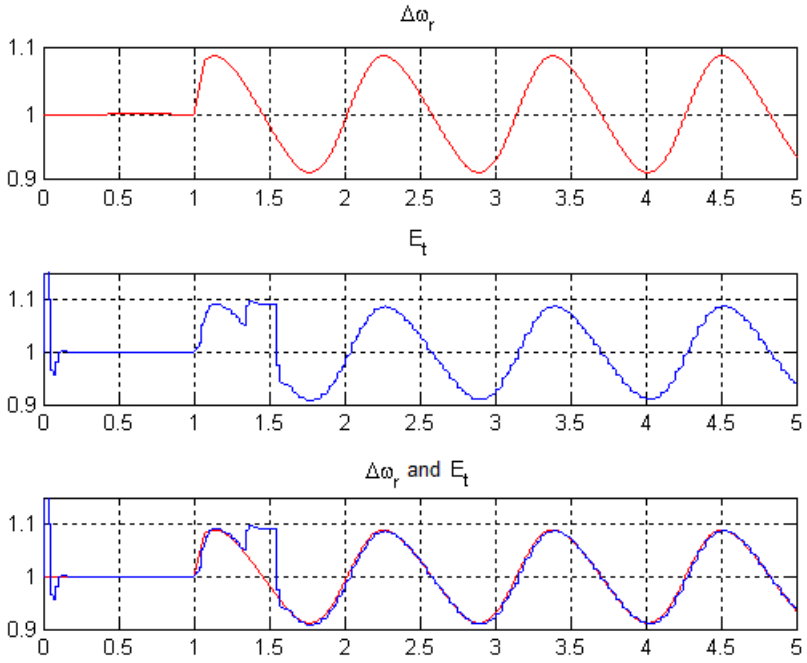


Figure 6.7 Improvement of first swing stability limit with STACOM Transient Stability Enhancement - i_q^{ref} partition.

6.1.4 Voltage Regulation Mode

While a STATCOM is operating in Voltage Regulation mode, the value of the terminal voltage E_t will be governed by the value of the reference voltage V_{ref}. The regulation of the voltage at selected load terminals of the transmission system limits voltage variation and prevents voltage instability. Figures 6.8 and 6.9 show that, when the voltage reference signal is stepped from 1.0 pu to 1.04 pu it will also change the terminal voltage with the expected response time.

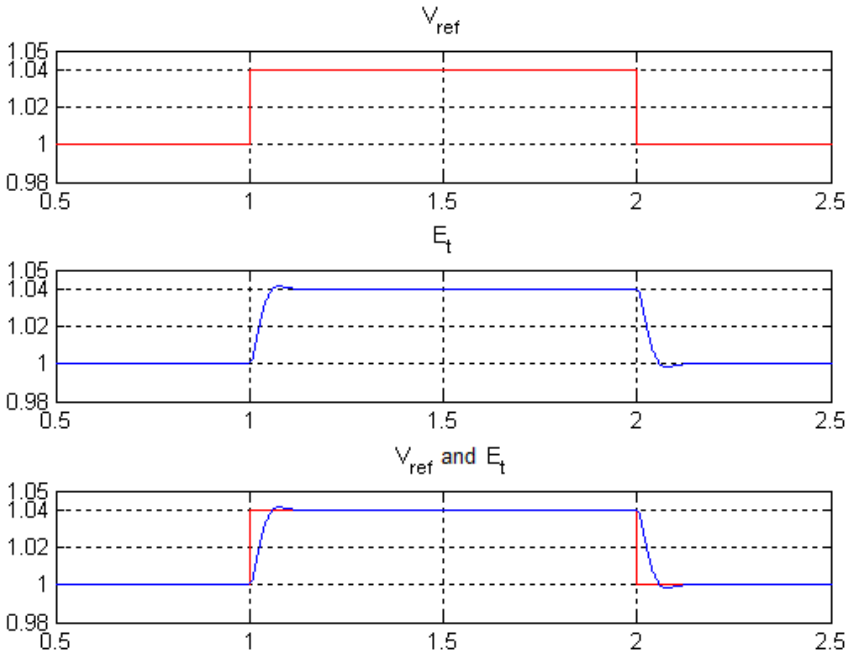


Figure 6.8 Response of the STATCOM terminal voltage E_t to a change in voltage reference value V_{ref} while operating in Voltage Regulation Mode - V_{ref}^{*} partition.

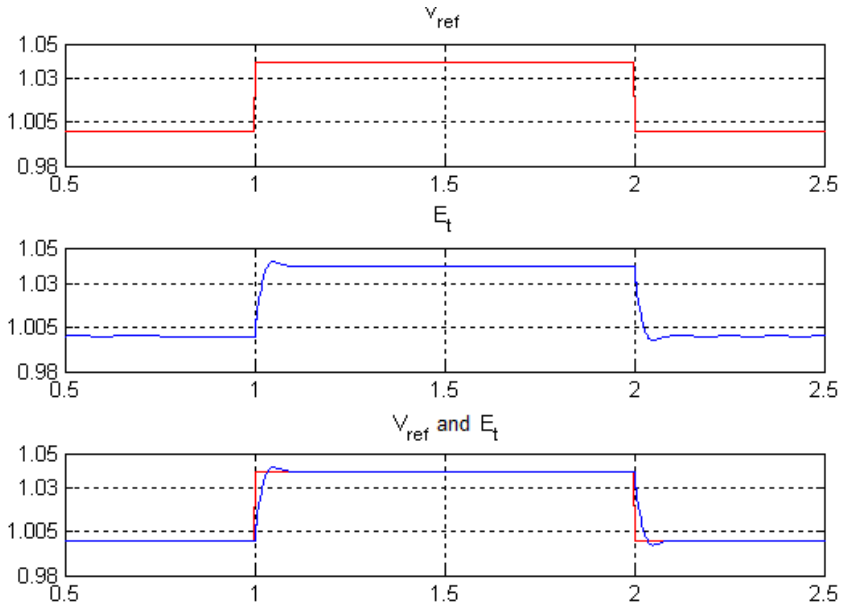


Figure 6.9 Response of the STATCOM terminal voltage E_t to a change in voltage reference value V_{ref} while operating in Voltage Regulation Mode - i_q^{ref} partition.

6.1.5 VAR Control Mode

In VAR Control mode the STATCOM steady state reactive power output is limited by a given reactive power reference value Q_{setpt}. In this mode of operation the STATCOM reactive current reference value will change in proportion with an error signal ($\Delta Q = Q_e - Q_{setpt}$), the difference in system reactive power Q_e and reference reactive power Q_{setpt}, forcing the compensator to increase/decrease the output current i_q^{ref} accordingly. Figures 6.10 and 6.11 show the simulation results while the STATCOM is operating under VAR control mode.

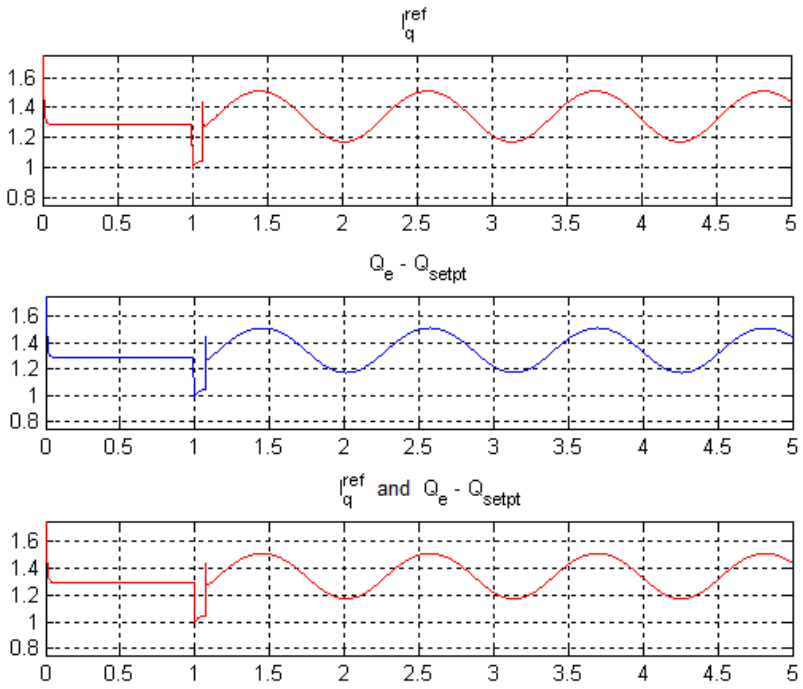


Figure 6.10 STATCOM Simulation results while operating under VAR Control mode- V_{ref}^{*} partition.

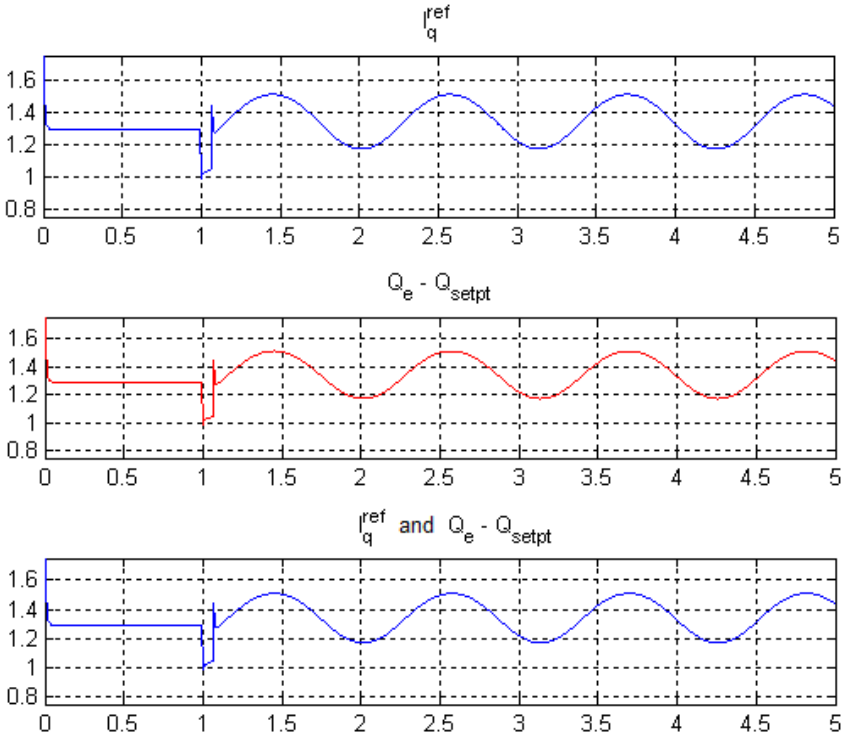


Figure 6.11 STATCOM Simulation results while operating under VAR control mode - i_q^{ref} partition.

6.2 Mini-HVDC

The studied Mini-HVDC system is shown in Figure 4.3 and the system parameters are listed in Appendix C.2. The following control strategy is implemented to evaluate the performance:

Strategy:

Converter 1 (sending side) controls the DC voltage/active power and AC voltage. Converter 2 (receiving side) controls the active power/DC voltage and supplies a constant reactive power.

The two controller partitioning options between system and application layers of the HVDC converter system are modeled and implemented in MATLAB/Simulink. Figure 6.12 shows the implementation of HVDC converter control subsystems with partitioning option at the V_{ref}^{*} summation also featuring the relative sampling rates of subsystems involved. Figure 6.12 shows the implementation with partitioning option at the i_q^{ref} summation.

Performance during step changes of active and reactive power

Step changes in reactive power and active power are performed by activating the AC voltage regulator and changing the direction of transmitted power respectively. The responses of the system are shown in Figures 6.13 and 6.15. First the AC voltage regulator of converter 1 is activated at t = 5/60 sec, and the voltage at the filter-bus1 (v_{abc_f1}) i.e. $V_{a\text{-}f1}$ returns to the reference value V_{ref} as the q-component of the current (i_q^{*}), $i_{q\text{-}ref1}$, reaches a steady state value. Then, step changes in active power are performed by

changing the direction of the transmitted power across the DC-link at t = 10/60 sec, with the response of the system shown by the d-component of the currents (i_d^*) i.e. $i_{d\text{-}ref1}$ and $i_{d\text{-}ref2}$. The DC voltage is changed when a step is applied and then returns to the reference value due to the DC voltage controller.

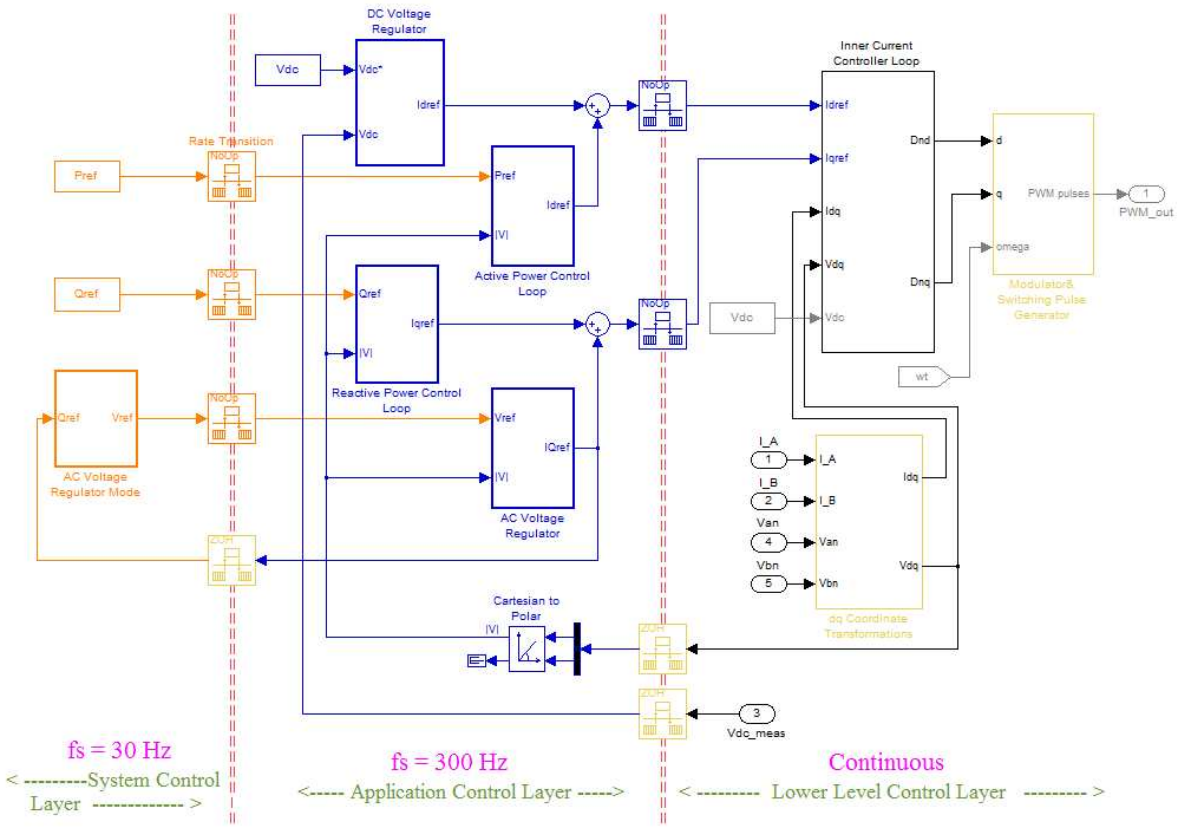


Figure 6.12 MATLAB/Simulink Simulation Control Structure for HVDC partitioning at V_{ref}^* .

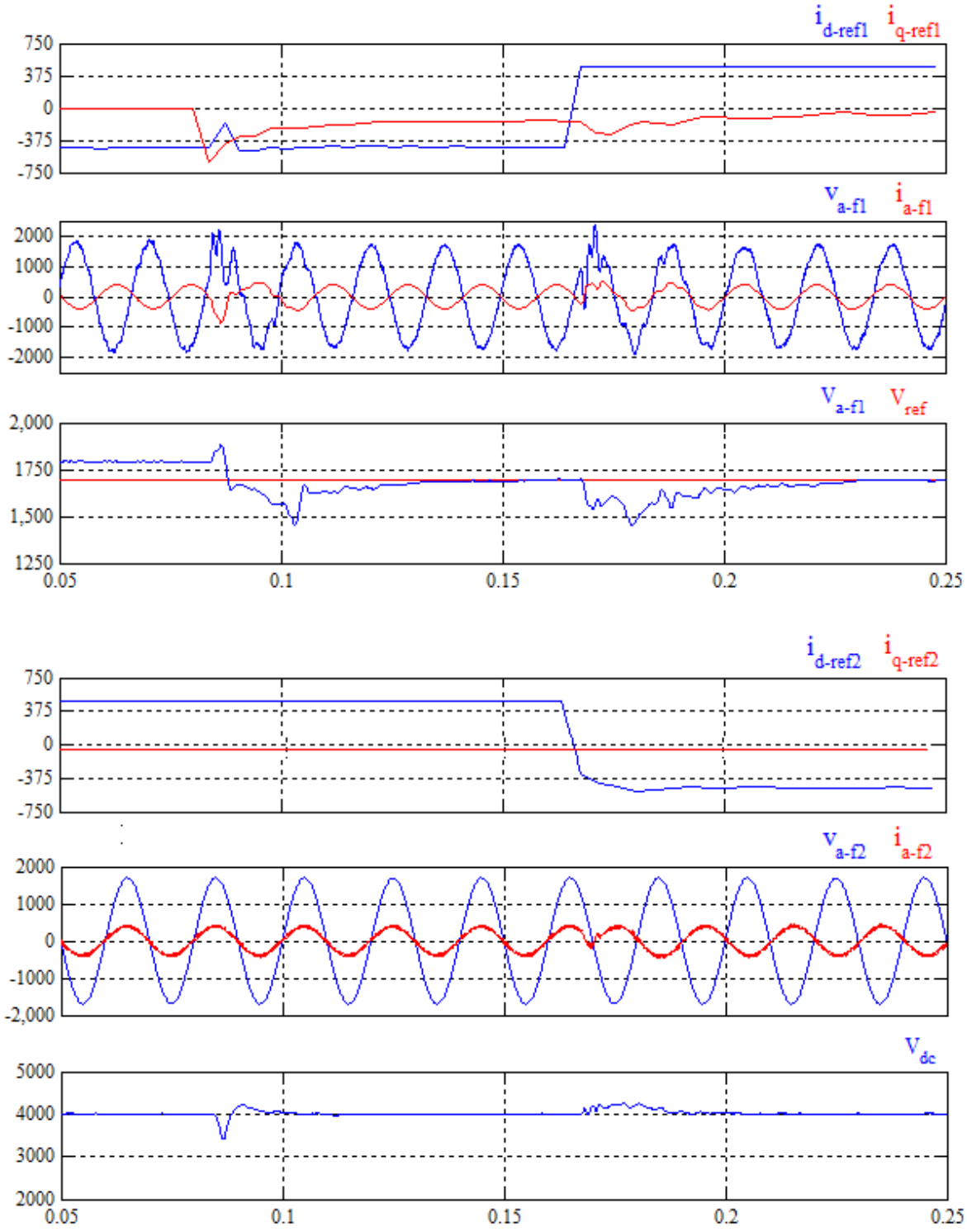


Figure 6.13 MATLAB/Simulink Simulation results for HVDC partitioning at V_{ref}^{*} .

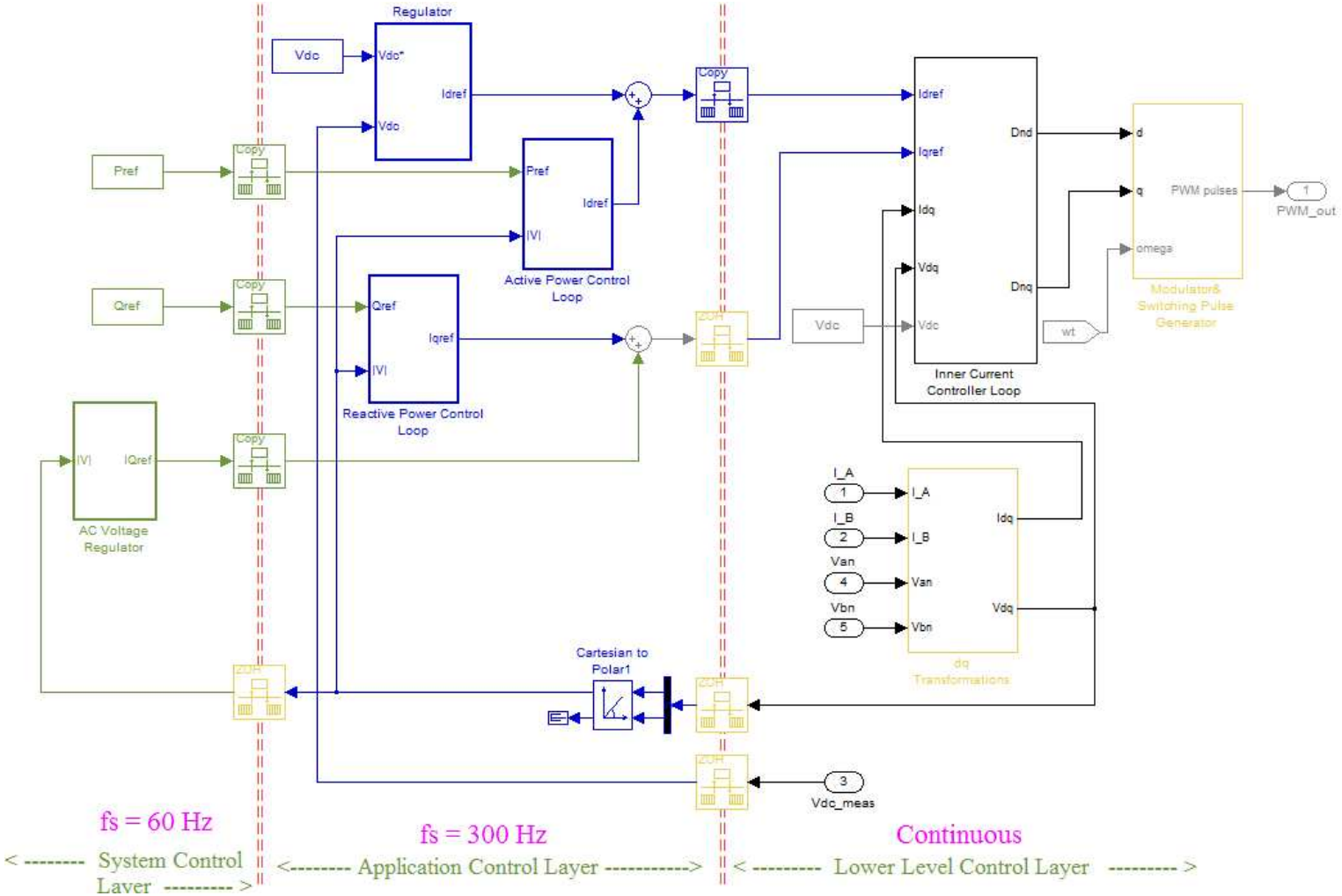


Figure 6.14 MATLAB/Simulink Simulation Control Structure for HVDC partitioning at i_q^{ref}

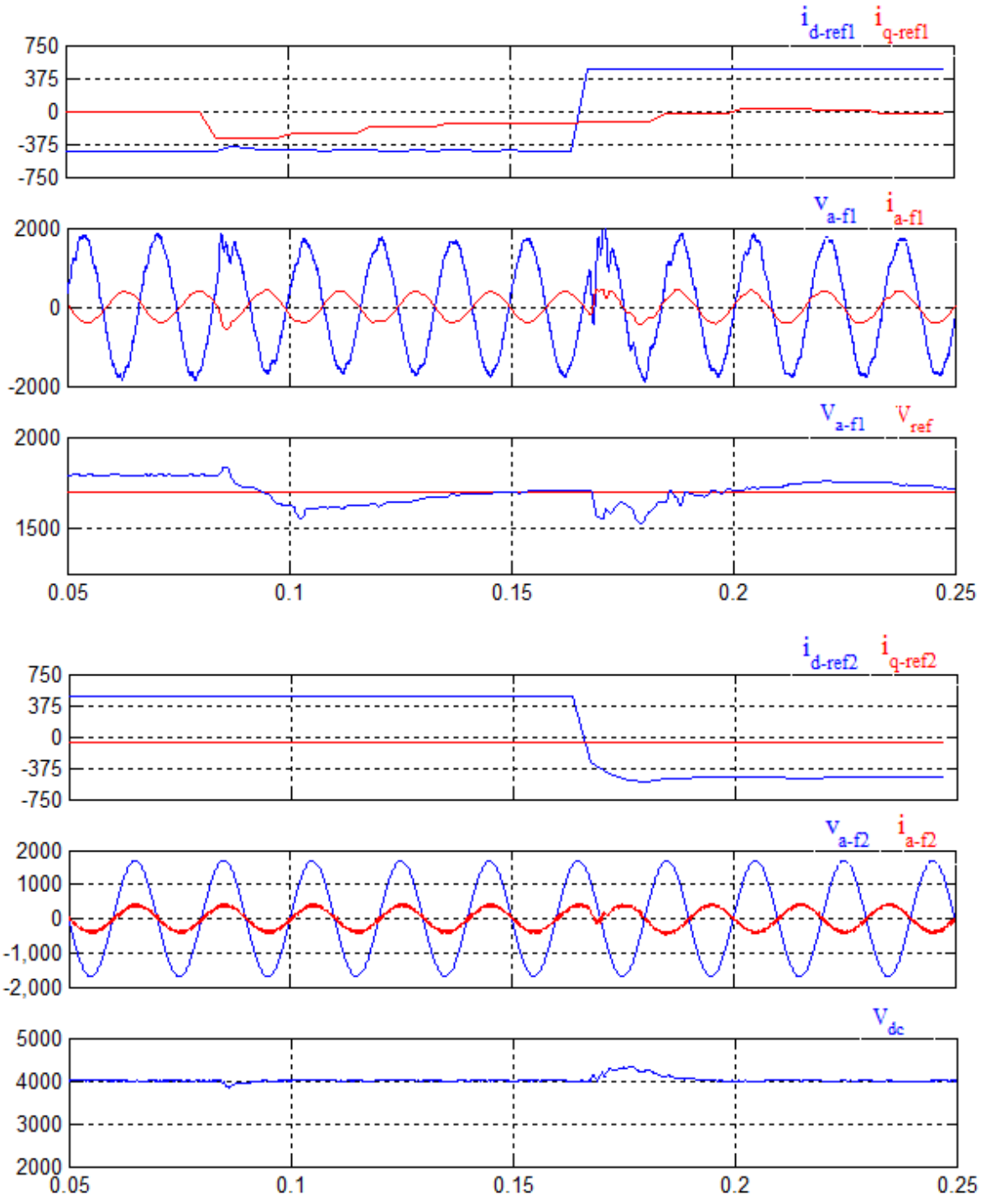


Figure 6.15 MATLAB/Simulink Simulation results for HVDC partitioning at i_q^{ref}

6.3 Active Rectifiers

Active rectifiers offer distinct advantages for variable speed drive and energy storage applications. These advantages include unity power factor and rigid control of the rectified DC-link voltage, even under extreme step load variations. Figures 6.16 and 6.17 show MATLAB/Simulink block diagram of an active rectifier implementation to control the DC voltage, while maintaining a unity input power factor for the AC supply. The controller will also have an option to control the reactive power with a reference value.

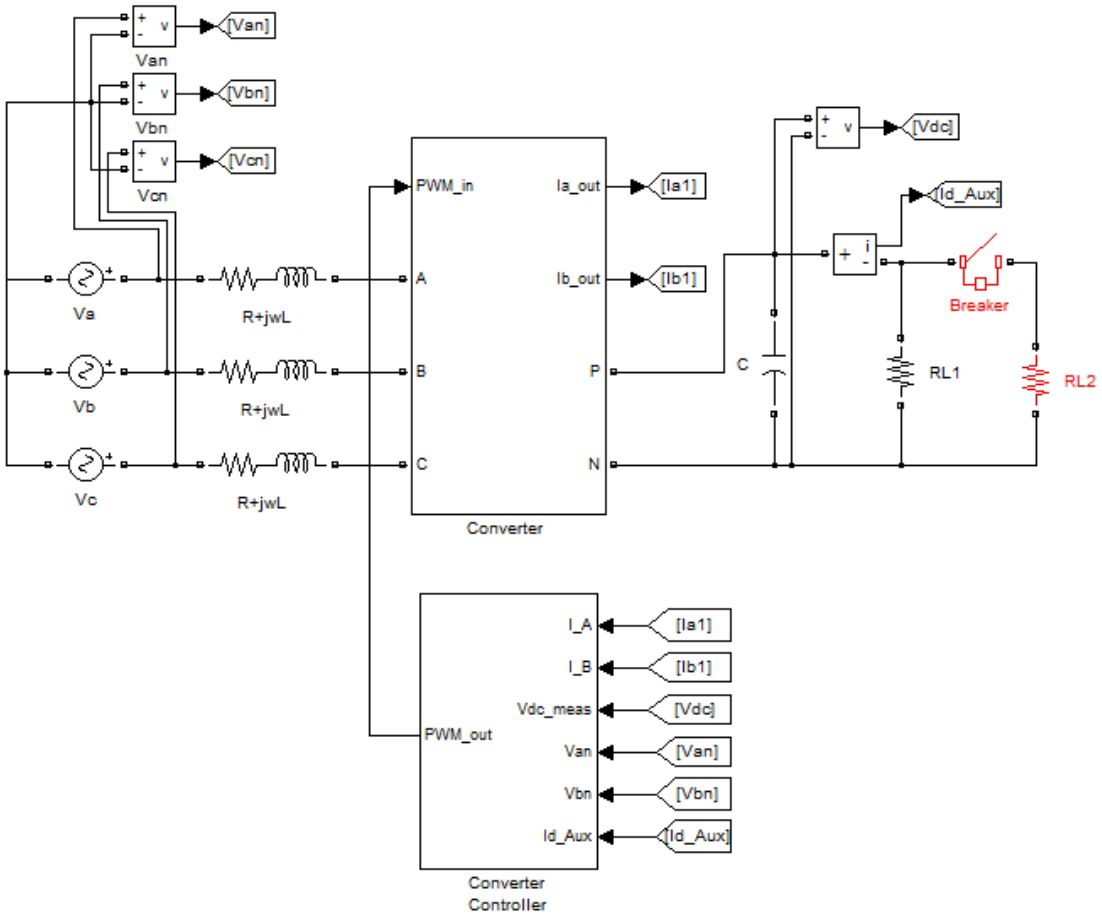


Figure 6.16 Simulink block diagram of active rectifier implementation.

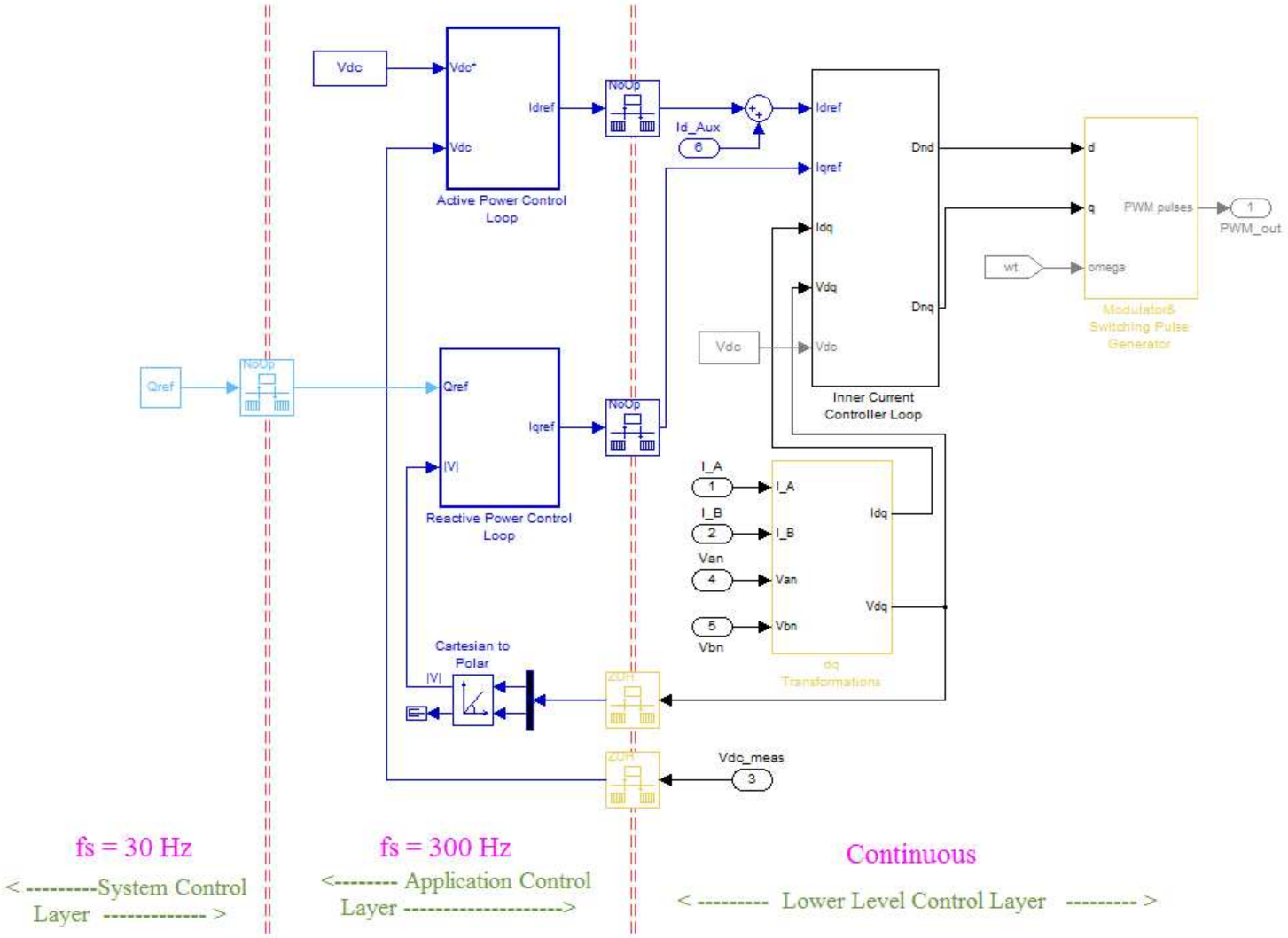


Figure 6.17 Simulation Control Structure for an active rectifier.

The simulation results are shown in Figure 6.18. At t=100 ms, a load is switched-in. The dynamic response of the DC regulator to this sudden load variation restores the DC voltage to the initial reference value and the unity power factor on the AC side is also maintained.

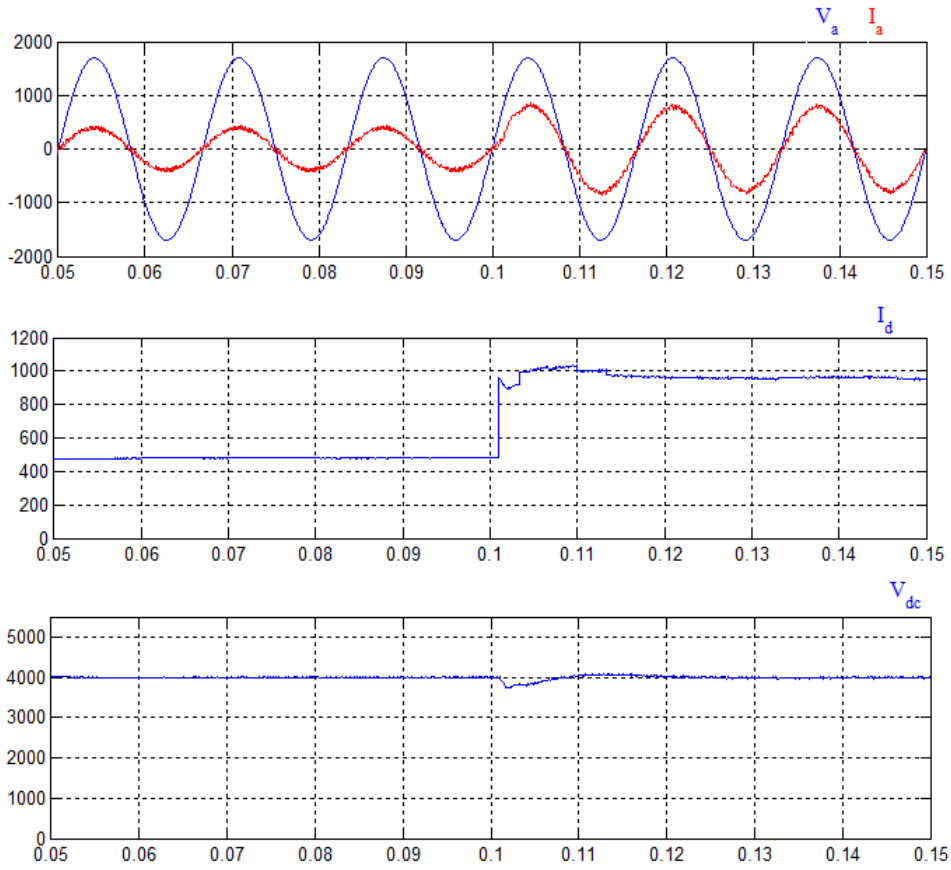


Figure 6.18 MATLAB/Simulink Simulation results for an active rectifier.

6.4 Vector Controlled Motor Drives

Vector controlled motor drive partitioning is explored using a partitioned MATLAB/Simulink drive system model derived from the models developed in [53]. The digital control subsystems are partitioned using fixed-rate subsystem blocks or Rate Transition blocks.

The simulation model parameters are provided in Appendix C.3. Figure 6.19 shows the simulation block diagram and the speed and torque outputs are shown in Figure 6.21. Although the dynamic performance and tracking are acceptable the torque ripple is approximately 4.5%. That may be considered too high for most applications. The torque and flux computations should be located in the application control layer or lower as shown in Figure 6.20. The results shown in Figure 6.22 indicate that the performance for a very slow system layer is acceptable with the shown partition. Also, the torque ripple is negligible at less than 0.1%. The reason for the torque ripple is the precision of the estimated rotor field angle. If the angle varies more than a couple of degrees per sampling interval, then the torque ripple will become unacceptably large. Therefore, the estimation of the rotor field angle should occur in the lower control layers for the same reason that the phase-locked-loop is located in the lower control layers for a grid connected converter application.

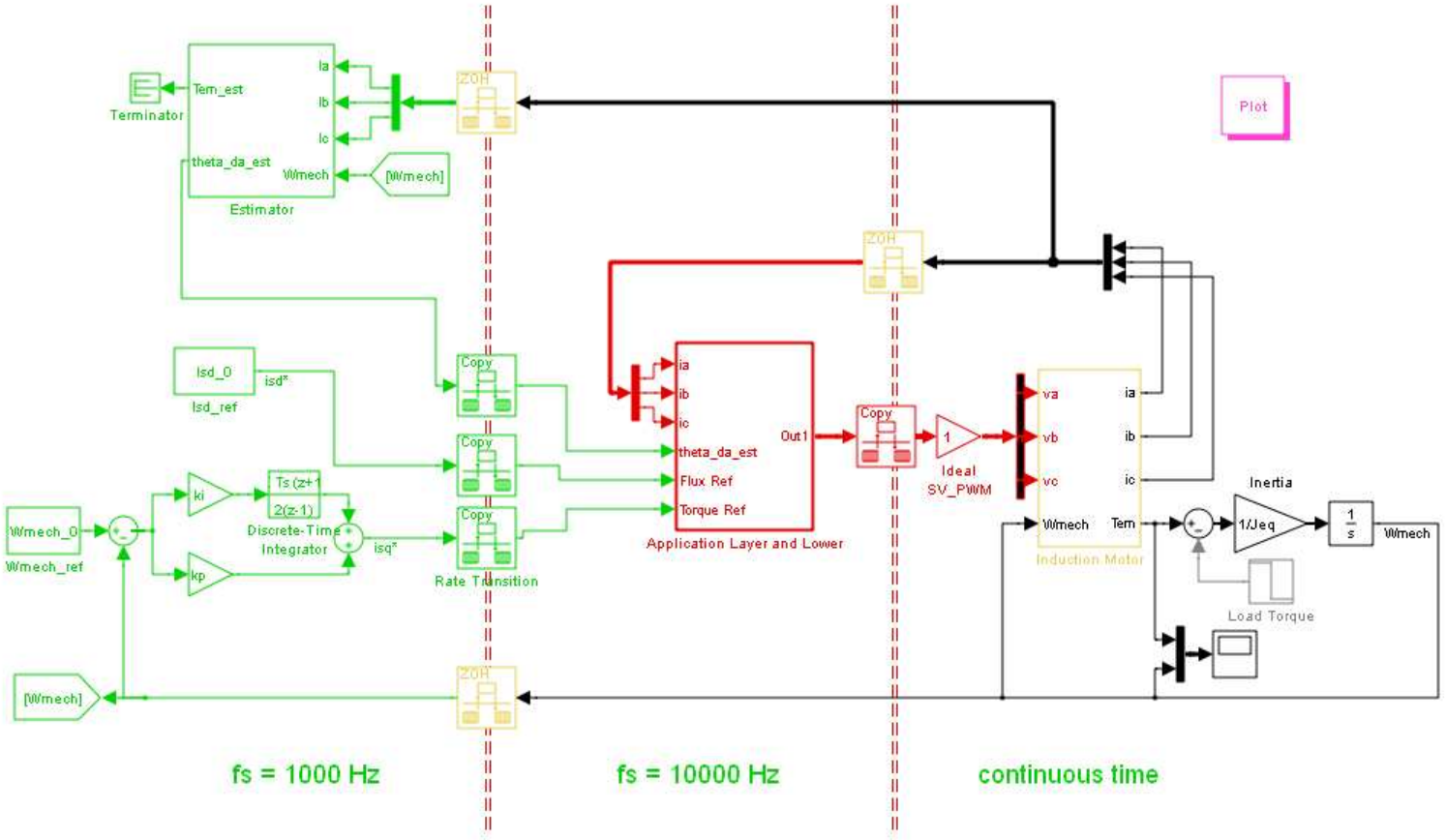


Figure 6.19 Partitioned model of a vector controlled motor drive with estimation in the system control layer.

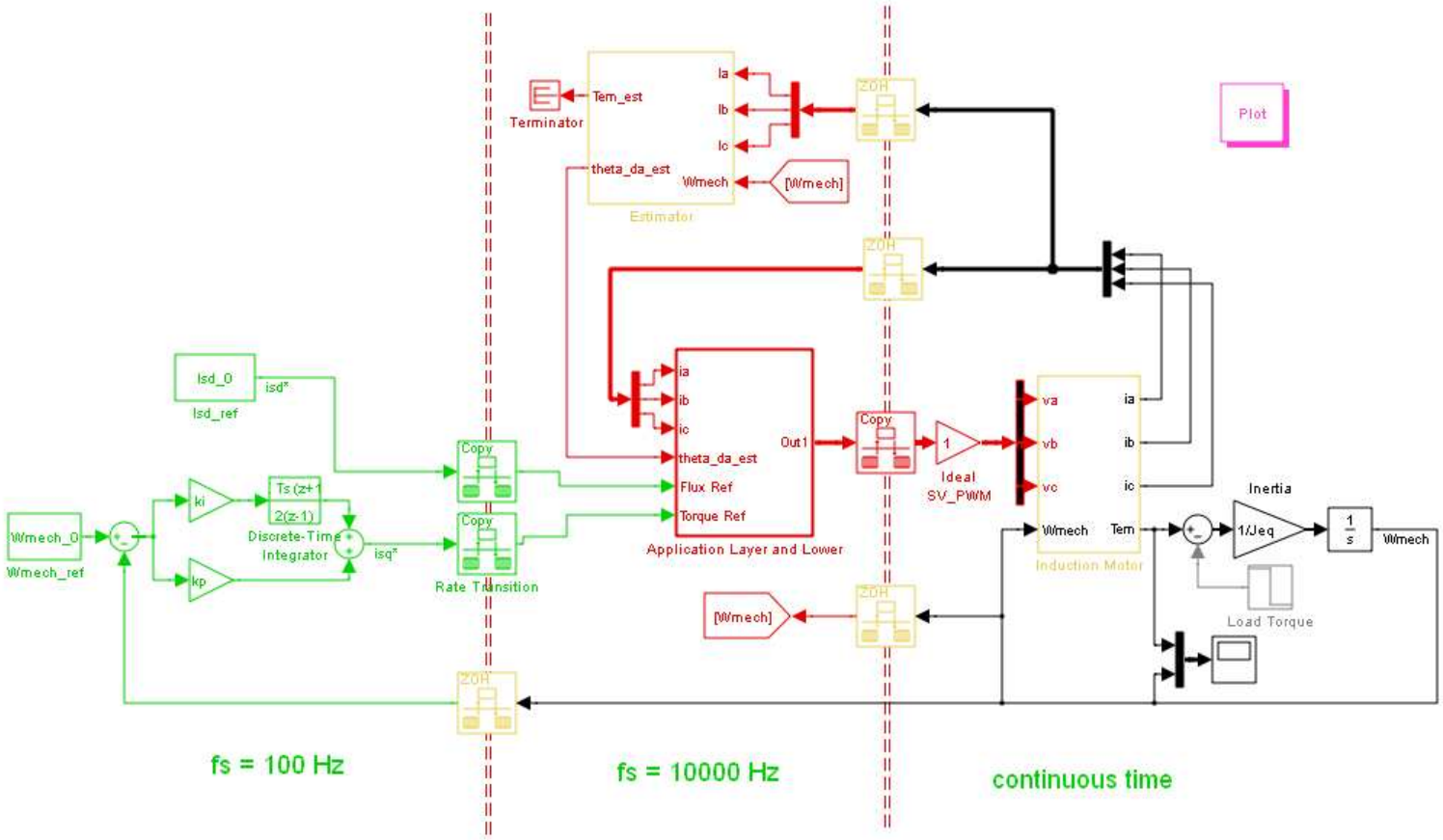


Figure 6.20 Partitioned model of a vector controlled motor drive with estimation below the system control layer.

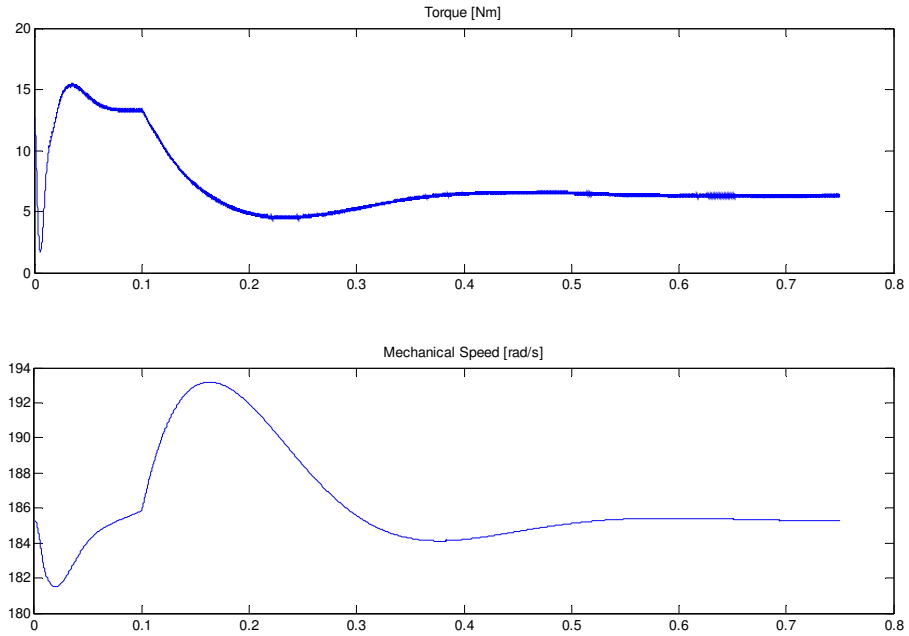


Figure 6.21 Torque and speed for the partition and sampling times shown in Figure 6.19.

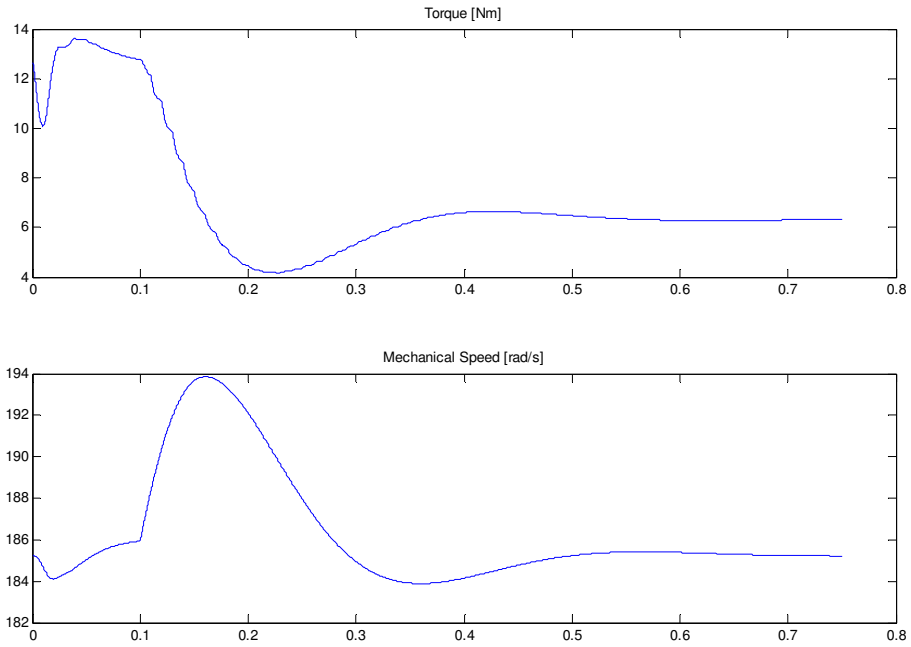


Figure 6.22 Torque and speed for the partition and sampling times shown in Figure 6.20.

6.5 Summary

The simulation models for the various grid connected converter controllers along with the partitioning requirements summarized in Table 5.5 were developed. From the MATLAB/Simulink simulations it can be found that the performance, of typical shunt connected current controller applications, during transients and steady state are satisfactory for the outlined sampling requirements given in Table 5.5. The sampling requirement for the system control layer in the grid connected converters is adjusted to be 30 Hz as compared to 24 Hz. This is because the application control sampling frequency has to be an integer multiple of sampling frequency requirement of the system control layer and to have a standardized synchronization throughout the controller.

CHAPTER VII

SYSTEM TO APPLICATION CONTROL LAYER INTERFACE DEFINITION

Chapter VI summarized partition options based on the temporal study of control functions. This chapter will quantify the control interface communication requirements with respect to primary and measurement signals so that the minimum set of system to application layer control interface is compatible across all power electronic controllers.

7.1 Analysis of Shunt Connected Converter Control Structures

Based on the previous analysis, it is possible to define a single partition between system to application control layer which can accommodate common control functions and similar interface signals for all applications summarized. The goal of this analysis is to find an optimum interface to split the system and application controllers regardless of the application.

Figure 7.1 shows a generalized grid-connected converter control structure, where different subsystems can be assembled and reconfigured easily to form a wide range of applications. The possible potential partitioning options for system to application control layer are shown, along the double dashed lines 2-2' (at V_{ref}^{*}) and 2-2" (at i_q^{ref}). By also considering vector controlled motor drive partitioning, shown in Figure 4.8, the

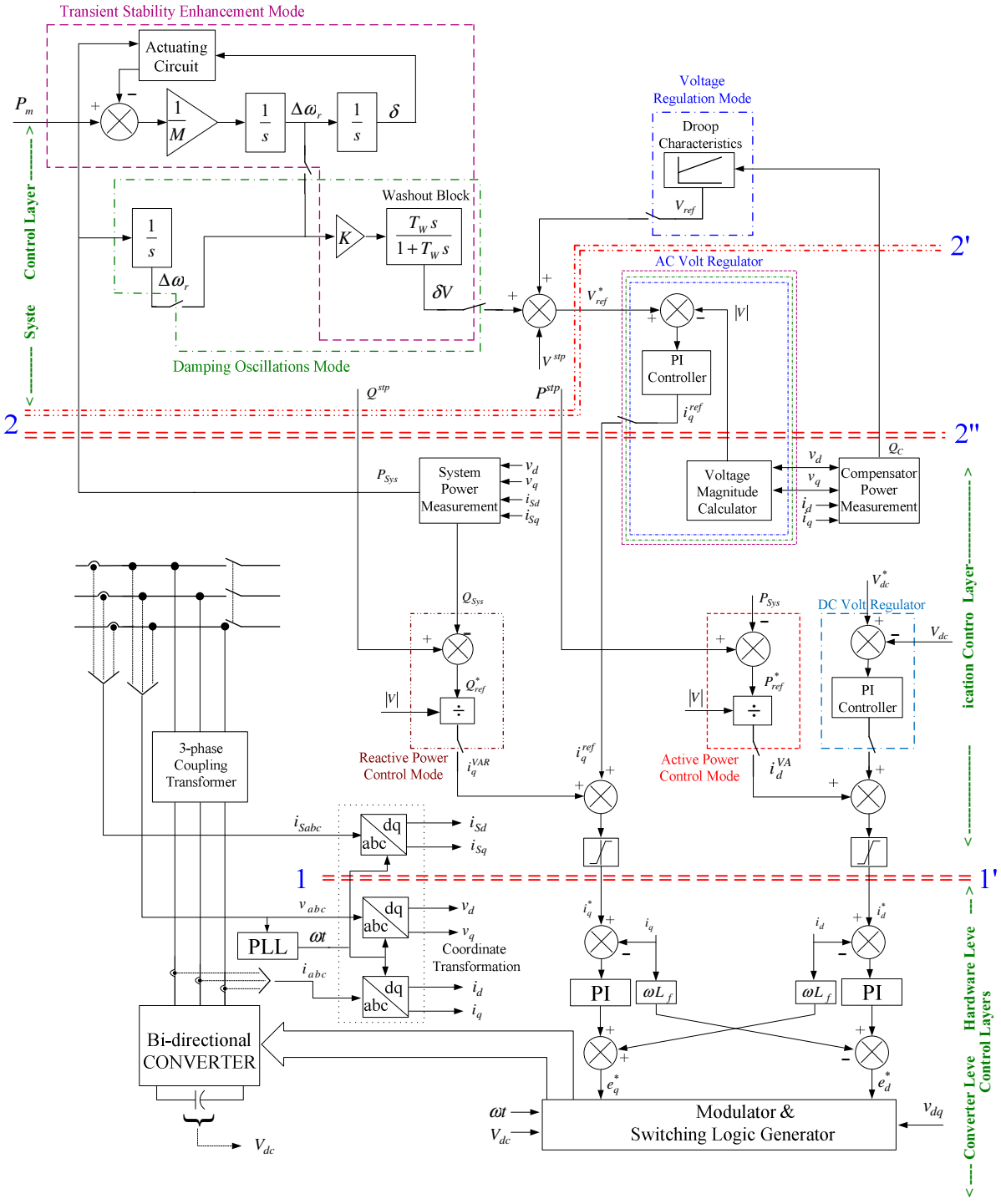


Figure 7.1 Generalized grid connected converter control structure.

partitioning option along the 2-2' (at V_{ref}^{*}) will result in more functional commonality by accommodating two PI control subsystems in the application control layer. By tracking error signals from the converter layer, these controls generate the required reference current signals from the measured quantities. The generated reference signals are then fed into the converter layer that enables the power electronic converter to behave as a controlled current source. While the complexity of system level control functions varies greatly, depending on the controller's overall objective, the interface signals remain consistent for the chosen partitioning option.

Based on the suggested partitioning option (at V_{ref}^{*}), an application control layer and system control layer definition is formulated. The suggested definitions for the system and application control layers are:

Application Control Layer –

Perform the decomposition of measured quantities to generate reference signals containing those components affected by the converter system as well as track error signals of those components in order to meet the mission determined by the system control.

System Control Layer –

Determines the overall converter mission using measured quantities and by coordinating the application layer controllers.

7.2 Communication Requirement for System to Application Control Interface

As the signals that cross this interface are purely sampled-data, all the signals are communicated in a digital form through the interface. The required channel bandwidth (*CB*) for sampled-data digital signals for lower level control interfaces are expressed as [6]:

$$CB = NK_d f_{SW} n_x \tag{7.1}$$

where K_d is defined as the ratio between the sampling period and transmission time, f_{SW} is defined switching frequency, n_X is the number of bits used to describe the measured variable, and N is the number of signals communicated through the interface.

A modified definition similar to Equation 7.1 is used here to define the channel bandwidth requirements for the system to application control interface. Where, the switching frequency (f_{SW}) used in the Equation 7.1 will be redefined with the sampling frequency requirements of system control layer, i.e. the rate at which the sampled-data will update through the system to application control interface. Thus, the required channel bandwidth for the system to application control interface is given as:

$$CB = NK_d f_{SSF} n_x \tag{7.2}$$

where f_{SSF} is the required sampling frequency of system control layer.

For the suggested partitioning option (at V_{ref}^*) and from the criteria for determining the temporal requirements of the layers developed in Section 5.2, using signal convention given in Figure 5.2, Table 7.1 summarizes the characteristics of the data that is being communicated through the system to application control interface.

Table 7.1 System to application communication requirements.

System to Application Layer	Signal Type	Name	# of signals	System Layer Sampling Req.
IN	Primary	V_{ref}^{*} or T_{em}^{*}, λ_{rd}^{*}	2	100 Hz
	Measured	Q^{stp} or Q_{ref}^{*}, P^{stp}	2	100 Hz
OUT	Primary	None	0	100 Hz
	Measured	P_{sys} or ω_{mech}, Q_C or $\hat{\lambda}_{rd}$	2	100 Hz

By considering the primary signals, and measurement signals, and using the parameters: f_{SSF}=100 Hz; n_X = 16 bits; N =6; K_d =2 the required channel bandwidth for the suggested system to application control layer interface will be 19.2 Kbits/sec.

A 16-bit processor is assumed for bit resolution measurement and other values for internal control signals and transmission rate were adopted according to standard values given in [11].

CHAPTER VIII

CONCLUSIONS AND FUTURE WORK

This dissertation presents the development of a methodology of characterizing the control interface between the system and application control for power electronic converter systems. By analyzing the current component affected by a converter, where each component or group of components is associated with a power-converter application, a common functionality is observed at the application control layer that contributes toward the partitioning requirements of the system to application control layer.

The research has addressed several aspects, including control function temporal requirements of system and application control layers, investigation into their appropriate control interface and partitioning, and, finally, modeling and simulation in order to validate the suggested interface requirements in MATLAB/Simulink environment.

An appropriate partition and the resulting interface requirements between the system and application control layers for power electronic converters has been determined so that the minimum set of system layer to application layer control interfaces is compatible across all power electronic controllers. Among the two possible potential partitioning options, the option that accommodates more functional commonality across

the application control layer was chosen. Based on the determined partitioning option, the application control layer and system control layer definitions were formulated and the communication requirements for the system to application control interface were also defined.

A subset of vector controlled motor drives that do not require precise position control or very high speed operation were shown to fit into the same temporal partitioning as grid connected converter systems. This inclusion of motor drive applications has marginally increased the interface temporal requirements in the overall generalization of the modular control architecture.

8.1 Future Work

This has dissertation mainly focused on developing the methodology for shunt connected current control applications. As series connected voltage controllers also have the same power electronic converter structure, and the only difference is in the components of the voltage affected by the converter system, this methodology can be extended to accommodate this class as well in the analysis. This will further improve the interface characteristics between the system and application control layers to adapt all power electronic converter systems.

Defining the communication protocols for the suggested system to application control interface will provide a consistent data communication environment for different manufacturers. The important aspects of the communication protocol for the system to application control interface are synchronization, jitter, transmission latency, controller computational time and the cost of the network medium. Therefore, defining

communication protocols based on widely accepted Ethernet technology for the system level control network would be a cost effective solution. At the same time this would allow integration of system level control in a wider internet information structure.

Finally, the proposed work was aimed at the analytical studies that were verified by MATLAB/Simulink models. Implementing the suggested methodology by using the latest digital control hardware for all power electronic converter systems along with the implementation of communication protocol for the interface will provide a further validation of the developed interface, and may help to refine it further, since all system details cannot be included in simulation based studies.

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APPENDIX A

SHUNT CONNECTED CURRENT CONVERTER

CONTROL ARCHITECTURES

STATCOM Control Functions

STATCOM control topologies for various (VAR control, reactive power compensation, power oscillation damping and transient stability enhancement) applications are summarized in Figure A.1 through Figure A.4.

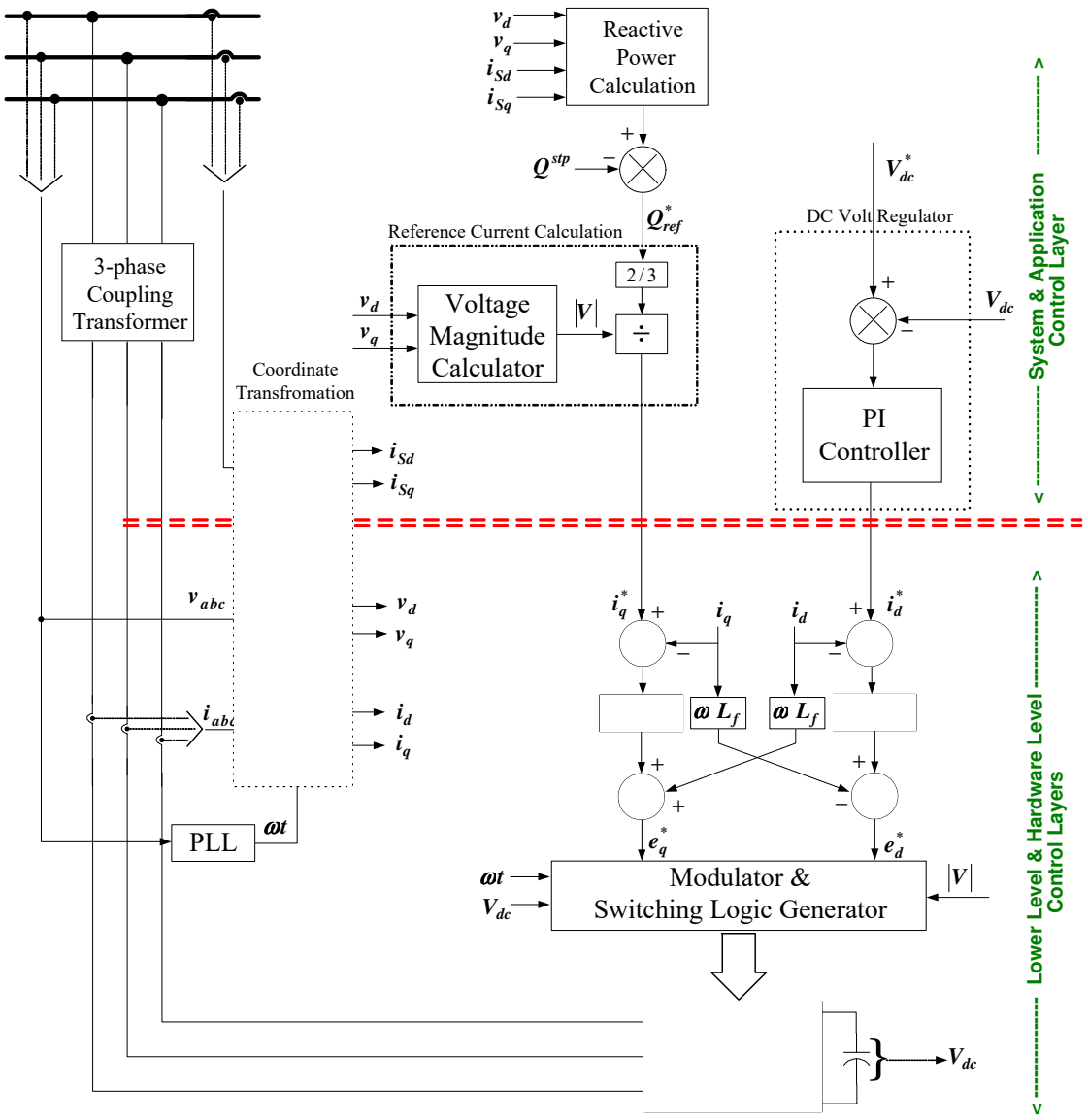

Figure A.1 STATCOM control structure for VAR control.

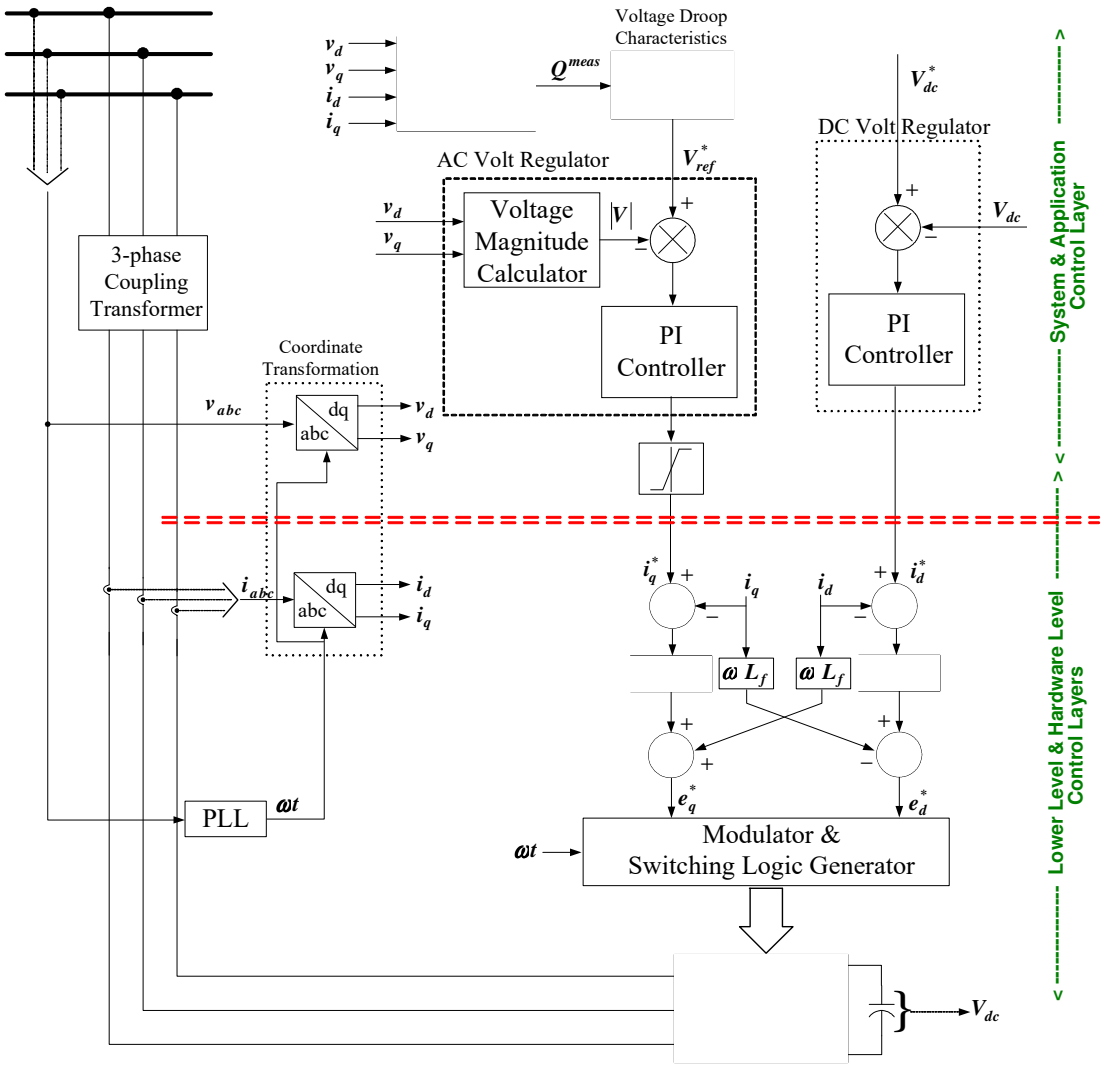

Figure A.2 STATCOM control structure for voltage regulation.

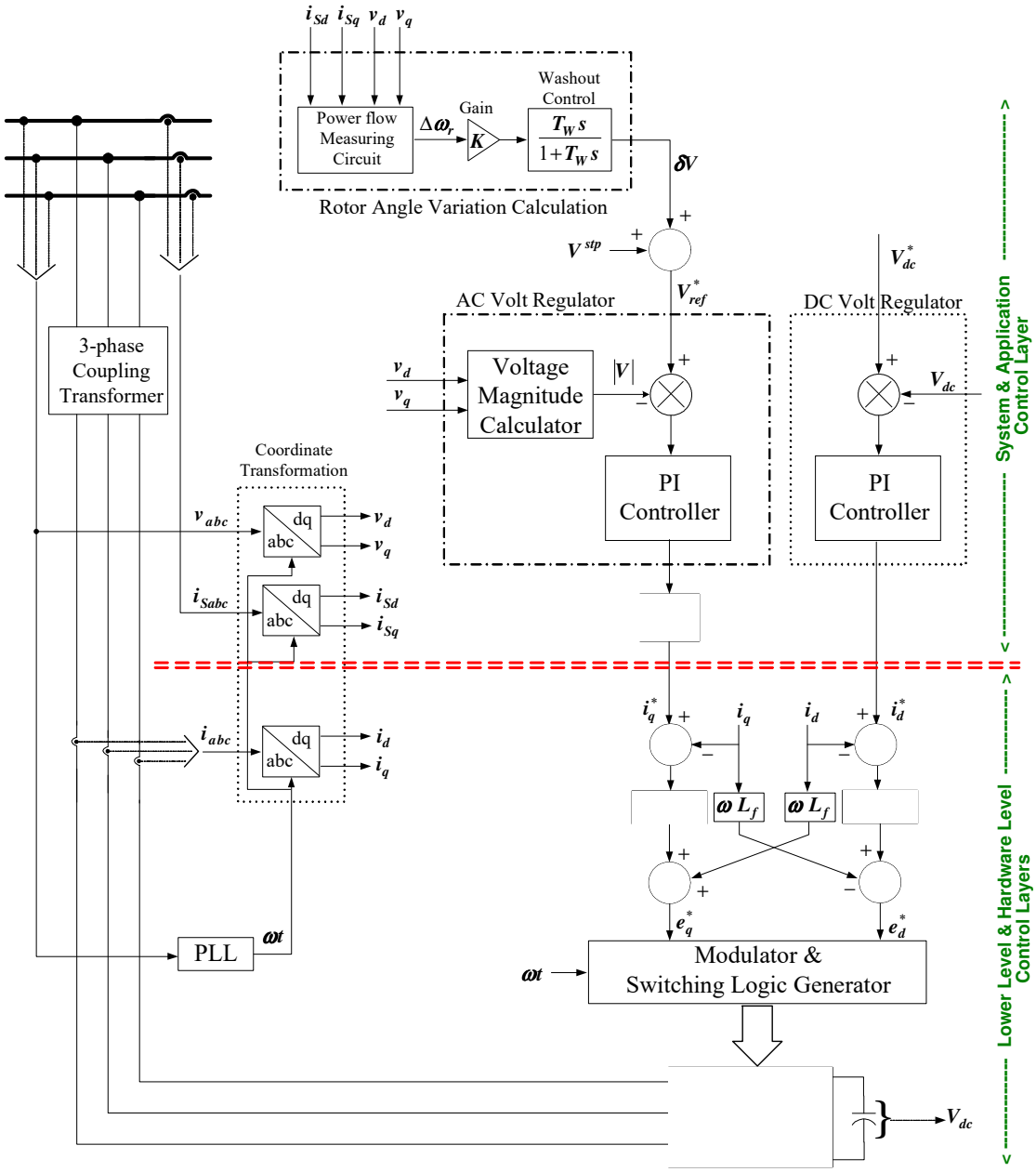

Figure A.3 STATCOM control structure for power oscillation damping.

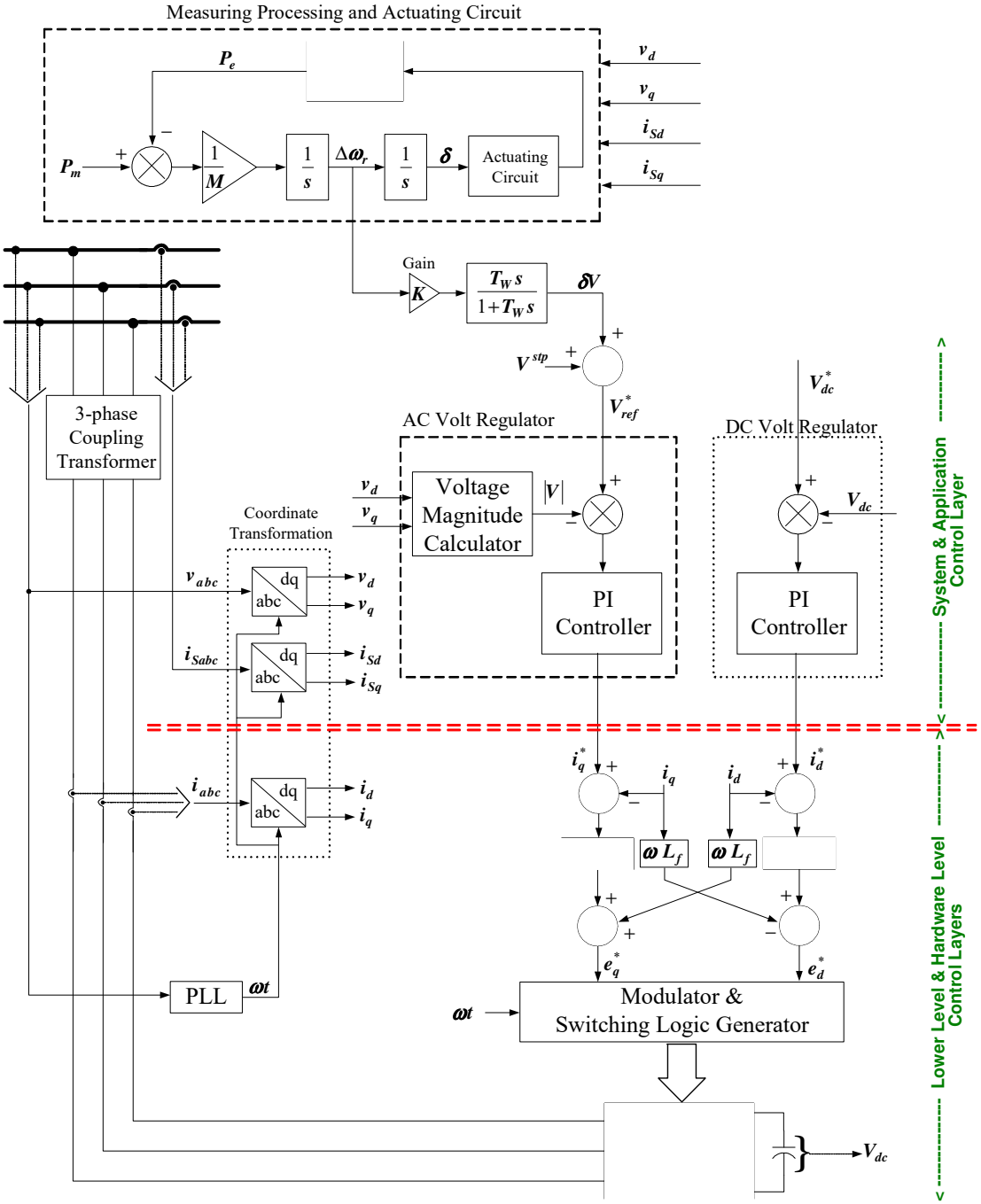

Figure A.4 STATCOM control structure for transient stability enhancement.

Vector Motor Drive Control Functions

A permanent magnet synchronous motor drive is shown in Figure A.5. It contains an outer control loop for speed regulation that provides a logic point for the separation of the system control and application control layers. From the viewpoint of the application control layer the converter is simply a controlled current source.

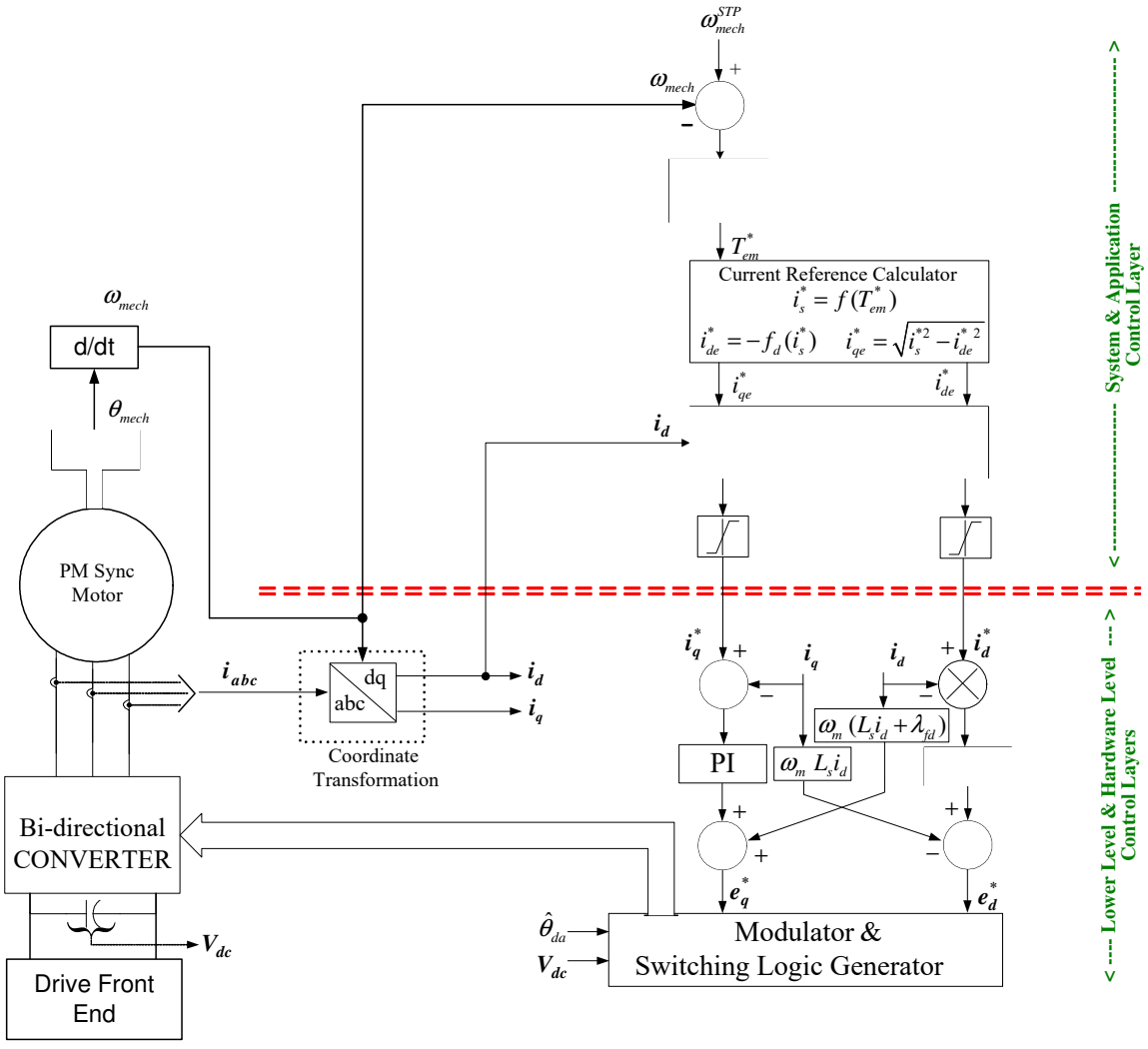

Figure A.5 Indirect vector control permanent magnet synchronous motor drive.

Active Filter Control Functions

Time-domain methods, such as the instantaneous reactive power theory, or *p-q* theory and its variants, have been used extensively in the development of methods for compensator control [8], [40]-[51]. A variation of the method known as the synchronous reference frame method or *d-q* method is also widely used. Both of these methods utilize filters to extract the desired current components. Frequency domain methods based on computationally efficient Fourier analysis have been far less prevalent, although some have been used [8], [46]-[51]. The maturity of development in the area of active filters is evidenced by the large body of literature, and in recent years comparisons of the various proposed methods of reference signal generation for active filters [46]-[58]. All of these methods are used to generate control reference signals that are sent to the feedback current control in the converter control layer. Active filters are often designed to remove all current components except the active component of the fundamental from the supply current, although, in some cases, an active filter is designed to remove only a sub-set of the unwanted components of the current. In general the unwanted components targeted for compensation are not on-line adjustable. A control architecture using the time-domain based d-q method with digital IIR filters is shown in Figure A.6, and an architecture using a frequency-domain based RDFT extraction method is shown in Figure A.7.

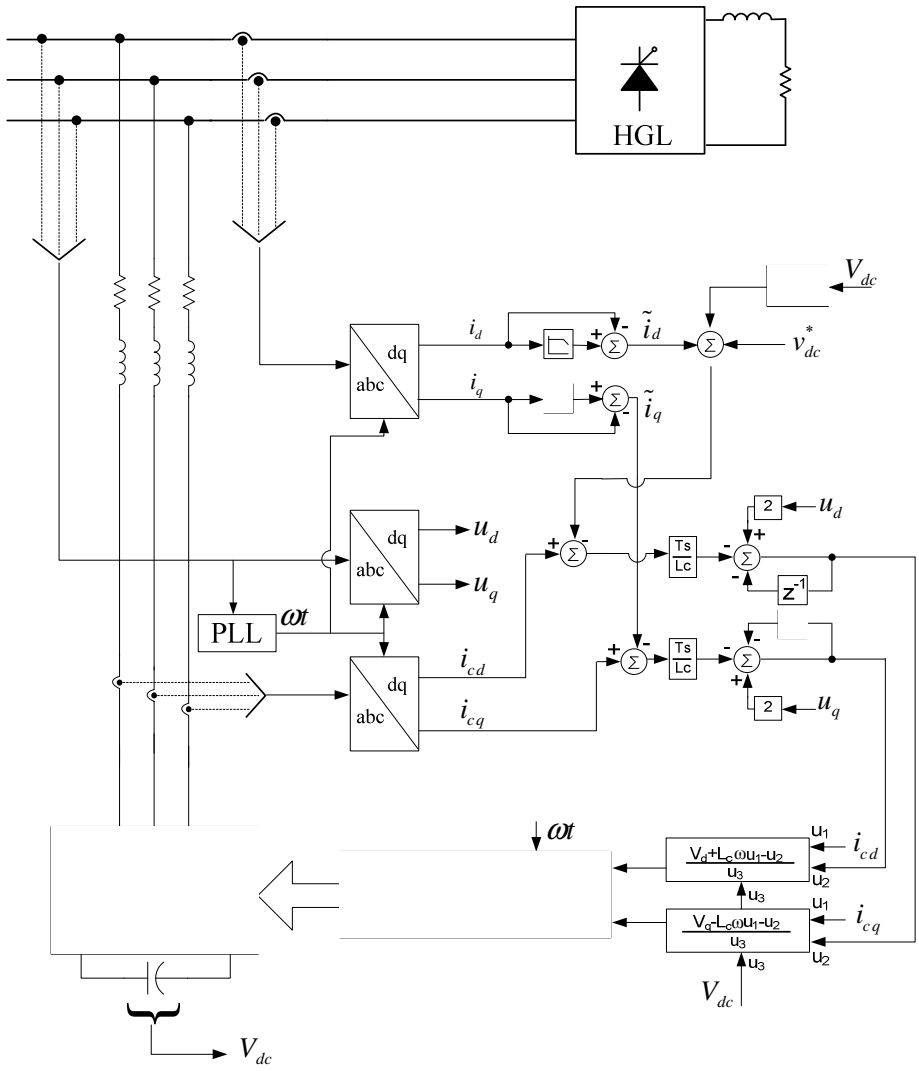

Figure A.6 Active filter application using the digital IIR filter harmonic extraction method in the d-q reference frame.

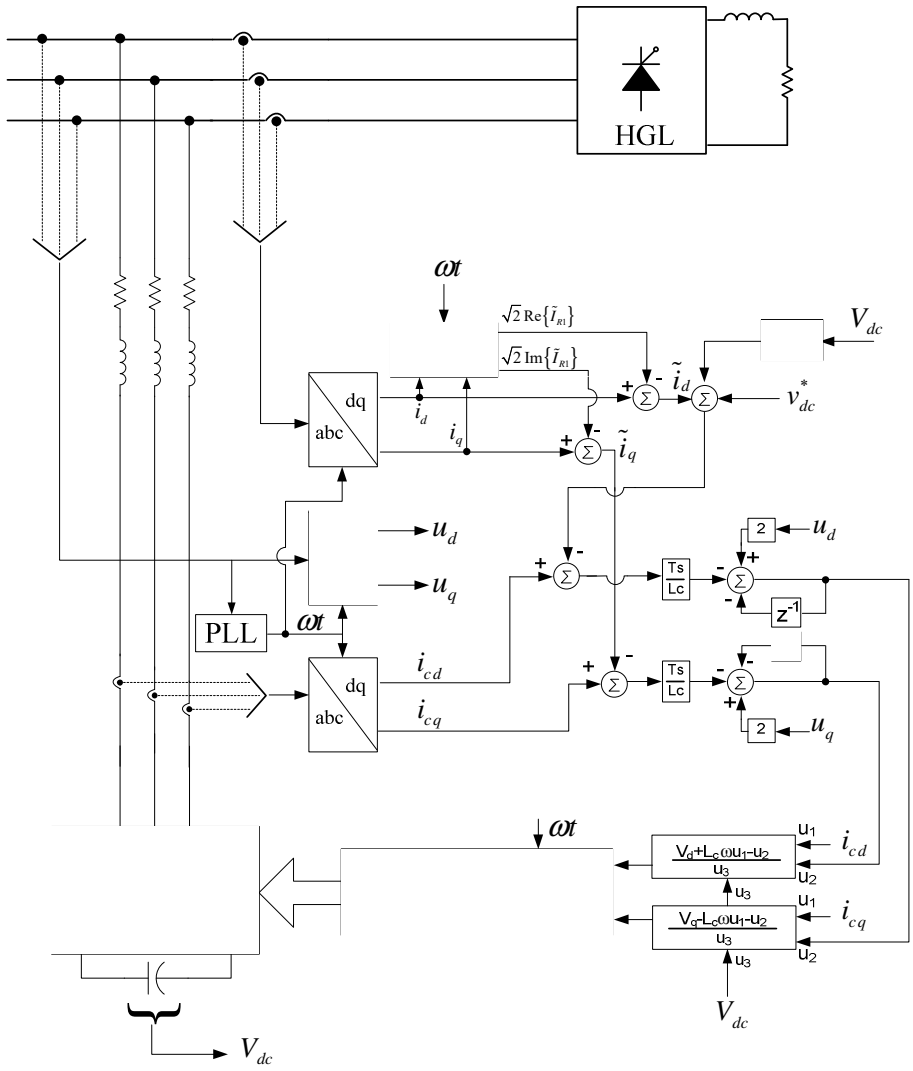

Figure A.7 Active filter application using the frequency domain RDFT harmonic extraction method in the d-q reference frame.

APPENDIX B

CAPACITOR SIZING CALCULATION

Selection of the Energy Storage Capacitor

Multilevel converters have been mainly used in medium or high power systems applications, such as static reactive power compensation and adjustable speed drives. Due to limitations on voltage rating of current available commercial high-power semiconductor technology, multilevel concept is usually the unique alternative because it provides voltage and/or current sharing between power semiconductor switches and also is based on low frequency switching.

Combining large numbers of semiconductor devices to achieve a high VA rating is well established. Choosing an arrangement where all devices are individually controlled provides more control opportunities to set things like voltage magnitude and suppress harmonics. In multilevel converter line-switching remains to be of most interest in FACTS implementations. PWM methods can be employed to give good sine-wave representation if such high switching frequency can be accommodated.

Multilevel Inverter Topologies

Several topologies are available to implement multilevel converters. Here, short reviews of the most common topologies are presented.

A. Multipulse Converter

Simple six-pulse converter units producing three-phase quasi-square wave voltages (or currents) are combined via phase-shifting isolation transformers [55]. Each unit provides a fraction of the VA rating of the overall circuit.

B. Multipoint-Clamped Converter (MPC)

MPC is also known as a diode-clamped multilevel (M -level) inverter (DCMLI). A multipoint-clamped converter typically consists of ($M-1$) capacitors on the DC bus and produce M levels on the phase voltage [54]. The DC bus consists of M capacitors, for a DC bus voltage V_{dc}, the voltage across each capacitor is V_{dc}/M, and each device voltage stress is limited to one capacitor voltage level V_{dc}/M through clamping diodes.

C. Chain Converter

Chain converter is also known as Cascaded Multilevel Inverter. A Chain converter multilevel inverter consists of a series of H-bridge (single phase, full-bridge) inverter units [56]. The general function of this multilevel inverter is to synthesize a desired voltage from several separate DC sources, which may be obtained from capacitors, batteries, fuels cells, or solar cells. Each separate DC sources is connected to an H-bridge inverter with each phase leg having an identical structure. The AC terminal voltages of different level inverters are connected in series.

D. Nested-Cell Converter

The nest cell converter is also known as the flying capacitor multilevel inverter. Each cell consists of a pair of switches (one upper and one lower operated as complements) and a capacitor that is not referenced to the DC bus [59]. The capacitors are charged to a multiple of E that is one different from the adjacent cells. The contribution of each cell to the output voltage is E when upper switch is on and zero when the lower switch is on. Each phase leg has an identical structure. Assuming that

each capacitor has the same voltage rating, the series connection of the capacitors indicates the voltage level between the clamping points.

Selection and Comparison of Topologies

A list of basic characteristics and respective priorities was defined as presented in Table B.1.

Table B.1 Multi level inverter topologies characteristics

ID	Inverter Characteristic	Priority
M1	Mainly based on low-frequency switching	Mandatory
M2	Bi-directional (4-quadrant operation)	Mandatory
M3	Suitable to implement high-resolution multilevel waveform	Mandatory
M4	Capable of feed loads with DC level Component	Mandatory
A1	Single source input	Additional
A2	Input-output isolation	Additional

According to Table B.1, the characteristics of all previously presented topologies are summarized in Table B.2.

Table B.2 Summary: Multilevel inverter topologies characteristics.

Topology	M1	M2	M3	M4	A1	A2
Multipulse	Y	Y	Y	Y	Y	Y
MPC	Y	Y	—	—	Y	—
Chain Cell	Y	Y*	Y	Y	—	—
Nested-Cell	Y**	Y	—	Y	Y	—

"Y": Yes, available. "—": Not available. "Y*": require extra controller.
"Y**": Low switching frequency makes clamping capacitors large.

As can be seen in Table B.2, the topologies with multipulse and chain cell meets all mandatory characteristics. While multipulse topology will also meets all additional

characteristics. The only disadvantage with multipulse topology is that for higher pulse numbers, the structure of the phase shift transformer becomes complex and its implementation appears difficult and expensive.

Capacitor Sizing

Rating of the DC-link capacitor bank of a voltage source converter may have a significant impact on the cost and physical size of a FACTS controller. The capacitor is sized for a specified ripple voltage, typically 5-10% of the nominal voltage. Among all modes of operation the STATCOM mode of operation (i.e., current and voltage in quadrature) yields the highest ripple current in the capacitor and hence the highest voltage ripples. Design Criteria like DC-link voltage ripple and DC-link capacitor stored energy play important roles in sizing the DC-link Capacitor [54].

Capacitor sizing for Multipulse and MPC

In the control structure of the compensator, we assume that the system AC voltage is sinusoidal and symmetrical at the point of common connection. For multipulse and MPC topologies, the main factor for determining DC-link capacitor size is 2^{nd} order energy oscillations caused by the negative sequence compensation currents [55]-[56]. These oscillations cause a ripple on the capacitor voltage, and the capacitor must be of sufficient size that the ripples do not adversely affect the performance.

The power-oscillating component which the compensator must supply in order to perform load balancing is therefore:

$$\tilde{p}(t) = 3U_1 \left| I_2 \right| \cos(2\omega t + \phi) \tag{B.1}$$

Note that only the magnitude and frequency of these oscillations are important, so the phase 'ϕ' will be omitted from further calculations.

The formula for energy stored (W) in the capacitor (size C) at a given voltage (E) is calculated using the time-integral of the real power.

$$W(t) = \frac{C V_d(t)^2}{2} = \int \tilde{p}(t)\, dt \tag{B.2}$$

This expression is then rearranged in terms of $V_d(t)$, with the oscillating power expression substituted for $\tilde{p}(t)$ and then integrated using (B.1) and (B.2)

$$V_d(t) = \sqrt{\frac{2}{C}\int \tilde{p}(t)\, dt} = \sqrt{\frac{3U_1|I_2|}{\omega C}\sin(2\omega t) + k} \tag{B.3}$$

It can be seen that 'k', the constant of integration, is the nominal DC-link capacitor voltage, squared.

$$V_d(t) = E_{nom}\sqrt{\frac{3U_1|I_2|}{\omega C(E_{nom})^2}\sin(2\omega t) + 1} \tag{B.4}$$

The following mathematical approximation can be used to simplify the preceding expression:

$$\sqrt{\delta + 1} \cong 1 + \frac{\delta}{2}, \qquad \text{where } \delta << 1$$

$$V_d(t) \cong E_{nom} + \frac{3U_1|I_2|}{2\omega C(E_{nom})^2}\sin(2\omega t) \tag{B.5}$$

Now, given the maximum allowed ripple amplitude ($\frac{\Delta E}{E_{nom}}$); it is possible to calculate a minimum required capacitor size:

$$C_{\min} \geq \frac{3U_1 \left| I_{2\max} \right|}{\omega E_{nom} \Delta E} \tag{B.6}$$

Chain converter

Chain converter topology consists of $(M-1)/2$ single-phase H-bridge units connected in cascade to generate an M-level output voltage over one half of the fundamental cycle [57]. Each H-bridge inverter has its own DC source. Since each phase has its own separate DC capacitors, calculation of the required capacitance of each H-bridge unit's DC capacitor is straightforward and automatically covers both positive-sequence and negative-sequence reactive power. The required capacitance can be formulated as [58]:

$$C_i = \frac{\Delta Q_i}{\Delta E} = \frac{\int_{\theta_i}^{T/4} \sqrt{2} I_1 \cos \omega t . dt}{\Delta E} = \frac{\sqrt{2} I_1 (1 - \sin \theta_i)}{\omega \Delta E} \tag{B.7}$$

Here, I_1 is the current rating of the inverter (rms value of the line current) and θ_i is calculated off-line to minimize the harmonics for each modulation index (*MI*) corresponding to respective DC output level. To generate $\pm Q_{\text{var}}$ reactive power, *MI* would change between MI_{min} and MI_{max}. For $MI=MI_{max}$, θ_i becomes minimum, and $MI=MI_{min}$ for θ_i becomes maximum. $\theta_i\big|_{MI=MI_{\max}}$ in Eq. (B.7) is used to calculate the

required capacitance so that the DC voltage ripple will not be larger than the given regulation factor, for all loads. Thus the required minimum capacitor size can be calculated as:

$$C_{\min} \geq \frac{\sqrt{2} I_1}{\omega \Delta E} \tag{B.8}$$

NOTE: For VAR support and for harmonic compensation, all DC capacitors (in H-bridge configuration) should have an equal capacitance because of pulse rotation among the H-bridge units instead of fixed pulse patterns. In addition, the required capacitance should be determined in the worst case (i.e. θ_i=0). Also, the harmonics have little contribution to the capacitor‘s charge because of their higher frequency, but the reactive current may dominate voltage ripples of the DC capacitor at the fundamental frequency [58].

Nested-Cell Converter

1. *Selecting DC-link capacitor*

The DC-link voltage ripples of the Nested-Cell converter become maximum when negative-phase-sequence current flows through the DC capacitor [59]. Thus the expression for the minimum required capacitor size is given by Eq. (B.6)

$$C_{\min} \geq \frac{3U_1 \left| I_{2\max} \right|}{\omega E_{nom} \Delta E}$$

2. *Selecting the Flying capacitor*

The flying capacitor of a Nested-Cell converter is a very important issue for the design. Here, the minimum required capacitance is calculated by defining the maximum

current of the flying capacitor. The voltage ripple of the flying capacitor depends on the load current and the time interval of the switching state. The time interval of the switching state is defined as:

$$T = \frac{2\pi}{(M-1)\omega_s} \tag{B.10}$$

where M is the number of levels and ω_s is the switching frequency.

Thus, the maximum voltage ripple can be defined as follows.

$$\Delta E = \frac{1}{C}\int_0^T \hat{I}_1 \, dt = \frac{\sqrt{2} I_1 \, 2\pi}{(M-1)\,\omega_s C} \tag{B.11}$$

The capacitance can be expressed as:

$$C_{\min} \geq \frac{\sqrt{2} I_1 \, 2\pi}{(M-1)\omega_s \Delta E} \tag{B.12}$$

A summary of the minimum required capacitances for each of the topologies is provided in Table B.3. Here, the value of C_i (size of capacitor) for DC bus control operation is given based on the controller design for the corresponding topology.

Table B.3 Summary for required capacitance.

Topology	M_c **(# of capacitors)**	C_i **(Size of Capacitor) for DC bus control**
Multi-Pulse	1	$C_{\min} \geq \frac{3U_1\lvert I_{2\max}\rvert}{\omega E_{nom}\,\Delta E}$
MPC	$(M-1)$	$C_{\min} \geq \frac{3U_1\lvert I_{2\max}\rvert}{\omega E_{nom}\,\Delta E}\times(M-1)$
Chain-Cell	3/2 x $(M-1)$	$C_{\min} \geq \frac{\sqrt{2}I_1}{\omega\Delta E}$
Nested-Cell	$(M-1)$ (DC-link Capacitor)	$C_{\min} \geq \frac{3U_1\lvert I_{2\max}\rvert}{\omega E_{nom}\,\Delta E}$
	3/2 x $(M-1)$ x $(M-2)$ (Flying/Balancing Capacitor)	$C_{\min} \geq \frac{\sqrt{2}I_1\,2\pi}{(M-1)\,\omega_s\Delta E}$

NOTE: In designing capacitor size considering $I_{2\max}$ will give the value for the worst possible scenario, however, as in most of the practical design applications, converter current rating is usually considered instead of $I_{2\max}$ for calculating the capacitor size.

APPENDIX C

SIMULATION CASE STUDIES

Continuous Simulation Model of Power System:

The generators are modeled as a single equivalent generator represented by classical model [20]. Figure C.1 shows the MATLAB/Simulink implementation of given system model.

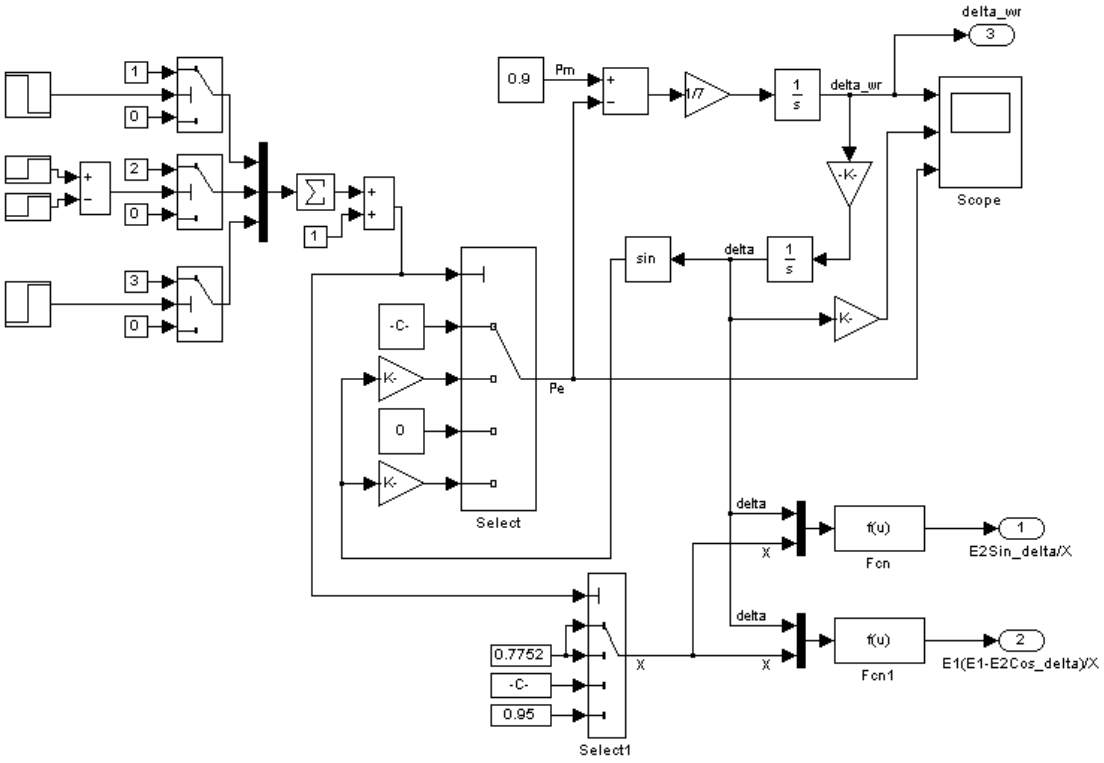

Figure C.1 Simulink power system model for all three-system conditions: a) prefault, b) during fault, and c) postfault.

Figure C.2 show the system response to a three-phase fault near bus E_t. The fault is cleared by isolating the faulted circuit in 0.07 seconds. It shows that the system with oscillatory mode of response without damping the oscillations. Using these rotor angle

oscillations and *dq-abc* coordinate transformation line currents are obtained as shown in Figure C.3. The following equations are used to obtain the dq components of currents.

The active power and the reactive power at the E_t end are given by:

$$\begin{aligned} P_e &= E_t(E_B \sin\delta)/X \\ Q_e &= E_t(E_t - E_B \cos\delta)/X \end{aligned} \tag{C.1}$$

Similarly the active and reactive components of the current at E_t end are:

$$\begin{aligned} i_d &= E_B \sin\delta / X \\ i_q &= (E_t - E_B \cos\delta)/X \end{aligned} \tag{C.2}$$

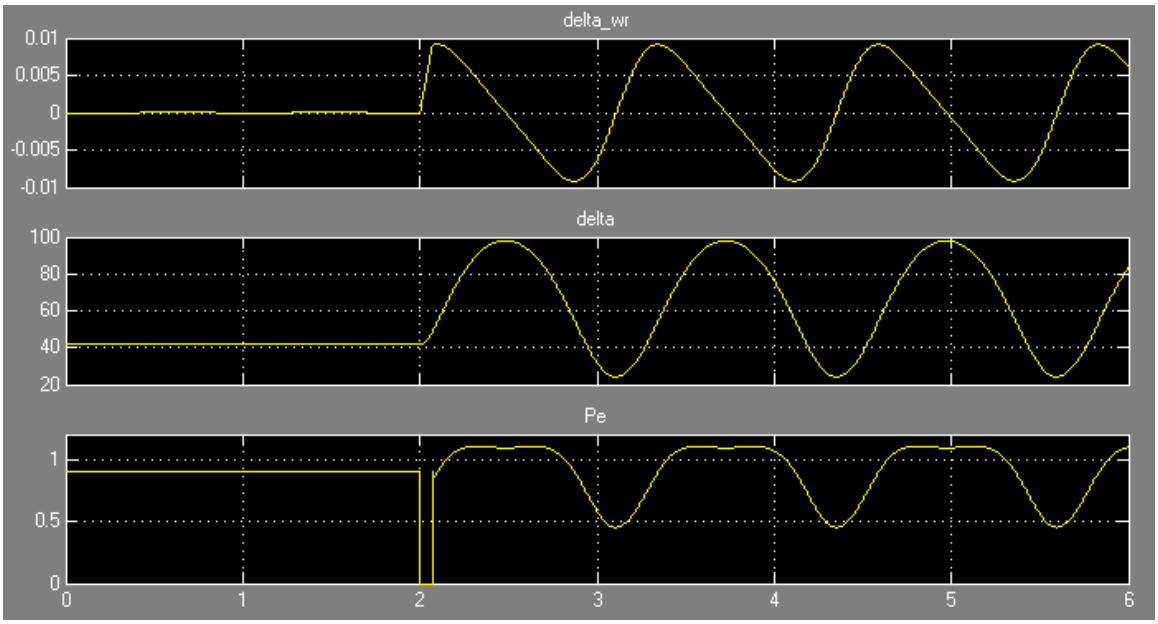

Figure C.2 Rotor angle speed (delta_wr, $\Delta\omega_r$), rotor angle (delta, δ), and active power flow (P_e) for a clearing time of $t_c = 0.07$ sec.

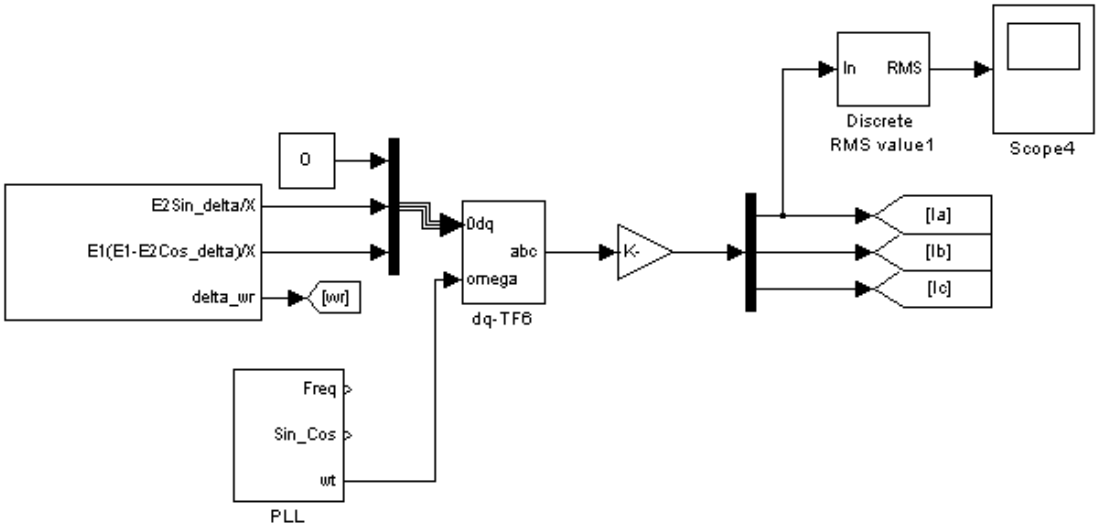

Figure C.3 Extracting line currents from current orthogonal components.

Obtaining Rotor Angular Speed from the line currents:

A mathematical formula has been developed to obtain the variations in rotor angular speed, and it is given by Equation (C.3). Equation (C.3) requires current orthogonal components, i_d and i_q, whose values are calculated using the *abc-dq* coordinate transformation.

$$\Delta\omega_r = \frac{1}{P_e}\frac{dQ_e}{dt} = \frac{1}{i_d}\frac{di_q}{dt} \tag{C.3}$$

Figure C.4 and Figure C.5 shows the MATLAB/Simulink implementation of obtaining Rotor Angular Speed variation ($\Delta\omega_r$) from line currents.

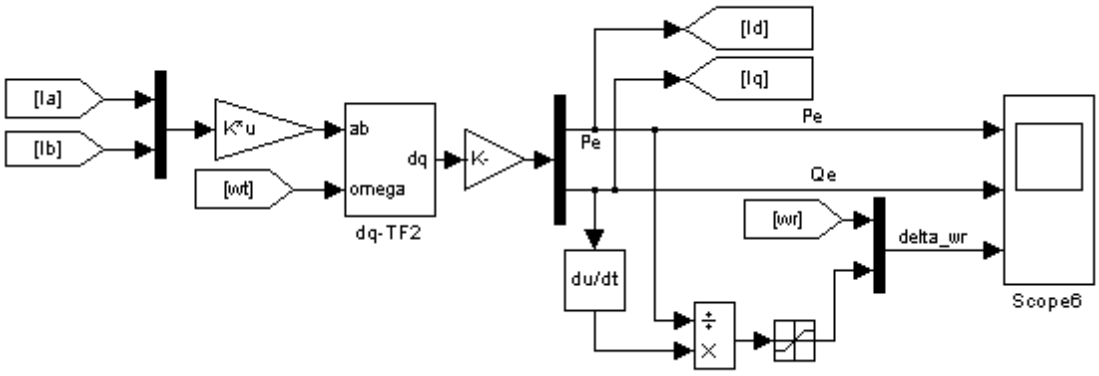

Figure C.4 Obtaining rotor angular speed variation (delta_wr, $\Delta\omega_r$) from line currents.

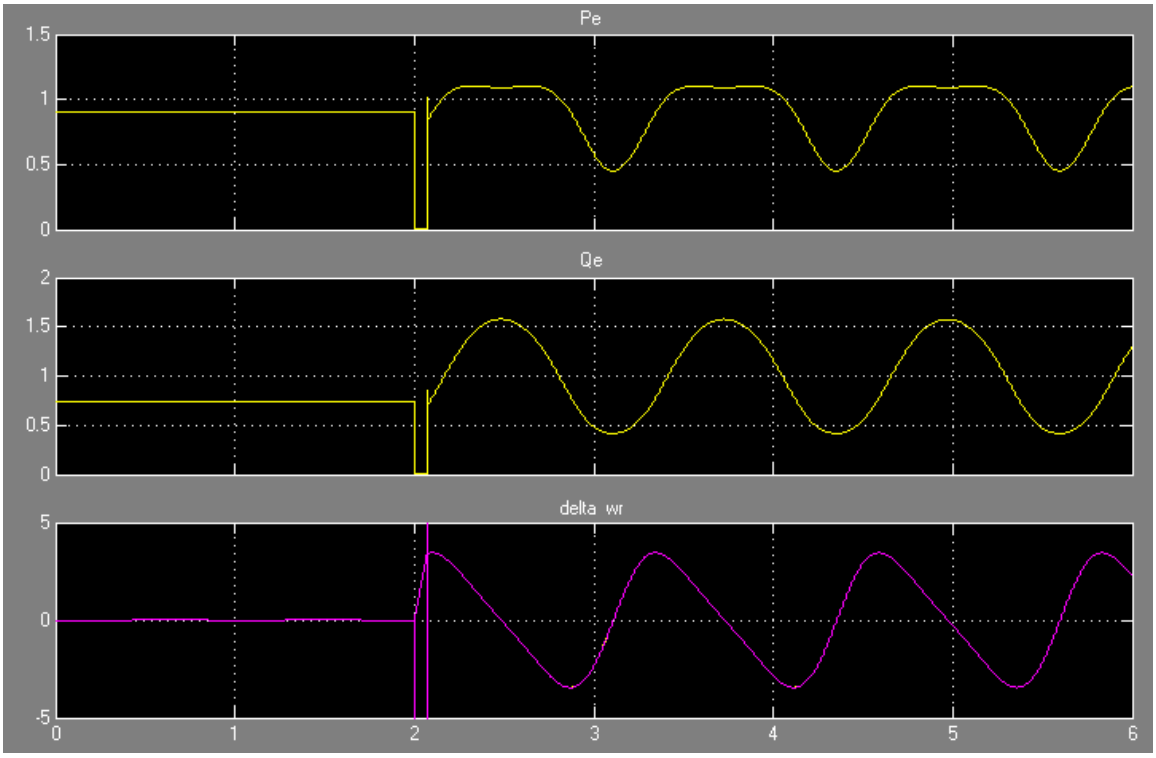

Figure C.5 Active power flow (P_e), reactive power flow (Q_e), variation in rotor angle speed (delta_wr, $\Delta\omega_r$) obtained from the formula.

AC Voltage Regulator:

The gains K_P and K_I are the proportional and integral parts of the controller respectively. The PI control system was designed for a desired settling time of 0.1 seconds. The desired voltage setpoint is the initial voltage value of 1.0 pu. The PI controller gains were chosen to be $K_P = 0.005$ and $K_I = 10$. The Unit step response for a PI-controller with desired settling time of 0.1 second is shown in Figure C.6.

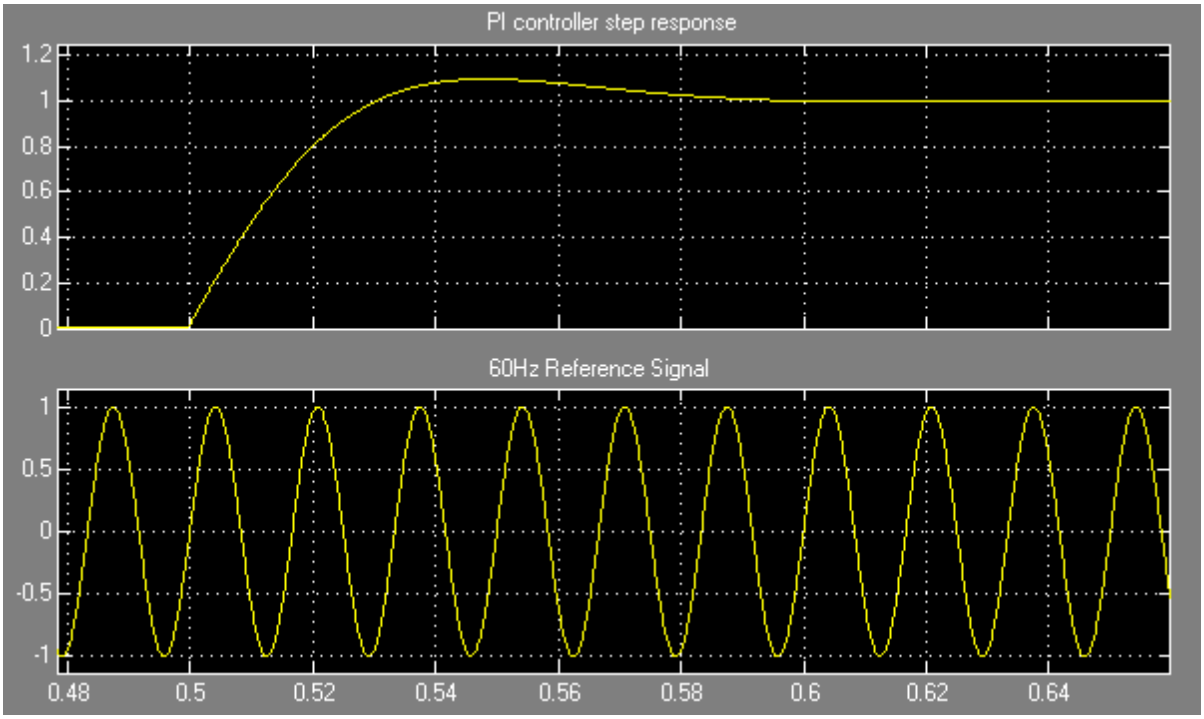

Figure C.6 PI-controller unit step response for a desired settling time of 0.1second.

STATCOM Dynamic Performance:

The dynamic behavior of the compensator in the normal compensating range can be characterized by a basic transfer function block diagram [9] as shown in Figure C.7.

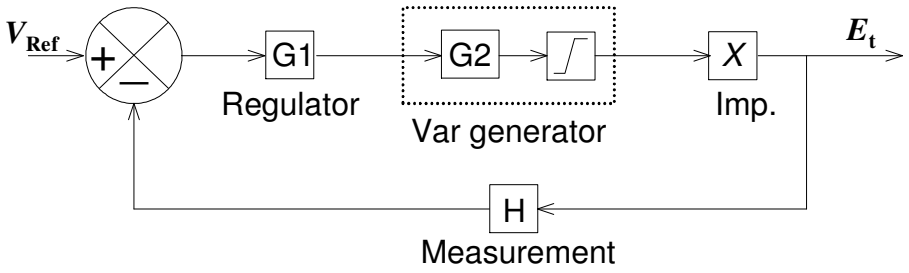

Figure C. 7 Basic transfer function block diagram of the STATCOM.

In Figure C.7, $G_1 = \dfrac{1/k_v}{1+T_1 s}$, $G_2 = e^{-T_d s}$, $H = \dfrac{1}{1+T_2 s}$ and T_1 = main time constant of the PI controller, T_2 = amplitude measuring circuit time constant, T_d = transport lag of the STATCOM, X = reactive part of the system impedance, k_v = regulation slope.

The implementation of the basic transfer block diagram is shown in Figure C.8. The response of the bus voltage magnitude with the variation of rotor angular speed is shown Figure C.9.

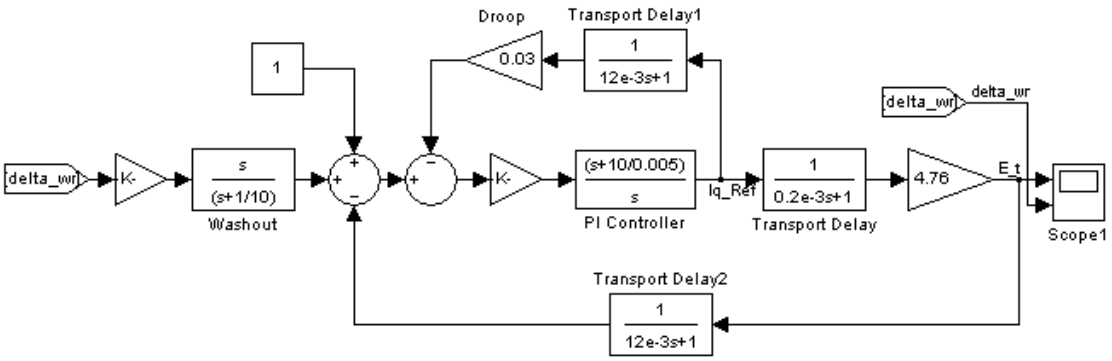

Figure C.8 MATLAB/Simulink implementation of basic transfer block diagram including an AC voltage regulator.

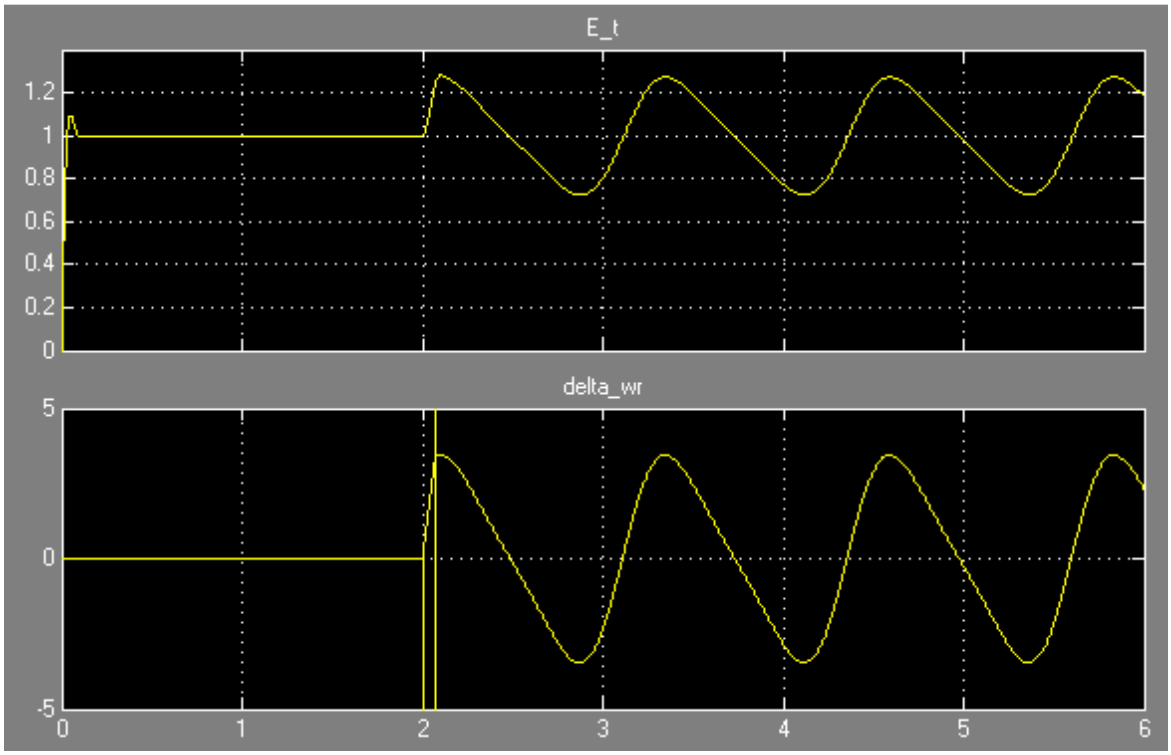

Figure C.9 Variation in the terminal voltage (E_t, E_t) with variation of rotor angular speed (delta_wr, $\Delta\omega_r$).

Mini-HVDC System Parameters

The system parameters for mini-HVDC system are listed as follows:

$v_{abc\_B1} = v_{abc\_B2} = 1.2\sqrt{3}$ kV ($V_{L\text{-}L}$, rms)

$V_{DC} = 4\,\text{kV}$

Rated Power = 1.5 MW

Per Phase Reactor Inductance = 2 mH

Per Phase Reactor Resistance = 0.01 Ω

DC Capacitor = 1000 μ F

System Frequency:

Bus B1 = 60 Hz

Bus B2 = 50 Hz

Induction Motor Parameters

The specifications for the motor are as follows [53]:

Name Plate Data:

Power:	3 HP/2.4 kW
Voltage:	460 V ($V_{L\text{-}L}$, rms)
Frequency:	60 Hz
Phases:	3
Full Load Current:	4 A
Full Load Speed:	1750 RPM
Power Factor:	88.5%
Number of Poles:	4

Per Phase Motor Circuit Parameters:

$R_s = 1.77\Omega$

$R_r = 1.34\Omega$

$X_{ls} = 5.25\Omega$ (at 60 Hz)

$X_{lr} = 4.57\Omega$ (at 60 Hz)

$X_m = 139.0\Omega$ (at 60 Hz)

$J_{eq} = 0.025\, kg.m^2$

Full-Load Slip = 1.72%