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Power supply noise reduction in 90 nm using active decap

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POWER SUPPLY NOISE REDUCTION IN 90 NM

USING ACTIVE DECAP

By

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On-chip supply voltage fluctuations are known to adversely affect performance parameters of VLSI circuits. These power supply fluctuations reduce drive capability, causes reliability issues, decrease noise margin and also adversely affect timing. Technology scaling further aggravates the problem as IR and Ldi/dt noise sources increase with each device generation. Current method used to reduce power supply variations uses an on-chip decoupling capacitors (decaps). These MOS capacitors utilize significant die area with about 15%-20% common for high-end microprocessors [4]. They also consume a considerable amount of power due to leakage and are prone to oxide breakdown during an ESD event because of reduced oxide thickness, making MOS capacitors unsuitable for technologies 90 nm and below. To improve the effectiveness of decap and reduce decap's area, a new active decap design is proposed for 90 nm technology.

DEDICATION

To my Parents for their support, their unconditional love and unfailing belief in me.

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I wish to express my heart-felt gratitude to Dr. Robert Reese who has been all that a mentor could be and more. Many thanks for all the guidance, support, encouragement and for support during the entire course of my study. I also express my sincere gratitude to Dr. Yaroslov Koshka for his inspiration through hard work, dedication and goodwill.I do believe I learnt my lessons and values for life from him. I also would like to express my gratitude to Dr. Ray Winton for imparting me with design knowledge during his course which has helped in my research. Last but not the least; I thank all the faculty, administrators and advisory committee of Electrical and Computer Engineering for giving me an opportunity to pursue graduate studies in the United States and for all the wonderful experiences I had here that will be part of my memories and I will cherish for life.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER I

INTRODUCTION

1.1 Motivation

Technology scaling is used to obtain higher gate density in integrated circuits in order to reduce cost. As the technology scales, the maximum clock frequency over which it can operate increases since the time required for charge carriers to cross the channel decreases. This increase in operating frequency leads to large transient currents drawn during a period of a few hundred picoseconds at clock edges that results in appreciable inductive voltage drop and causes power supply fluctuations. The major reason for these power supply fluctuations is the package inductance. The package inductance determines the maximum current that the power supply can handle over the switching period so that the voltage variation between the supply lines remains within the permissible noise budget, which is normally 10% of the supply voltage [10]. Furthermore, decreasing feature sizes result in reduced supply voltage which makes design of the power supply distribution network much more difficult. The International Technology Road map predicts supply voltage to be as low as 0.5 V by the year 2016 [1]. These constraints confirm the importance of noise issues and make the design of the power supply distribution network more challenging.

1.2 Noise Origin and Components

The power supply grid provides VDD and VSS throughout the chip, and experiences noise from various noise sources. The noise at any point on the power supply grid can be considered as the sum of various independent noise sources. Some of the major noise sources are described in the following sections.

1.2.1 Thermal Noise

Thermal noise or *Johnson noise* is noise generated in a conductor or a semiconductor due to random movement of charge carries when subjected to any temperature above 0 K. Thermal noise is known to have a power spectral density spread throughout the frequency spectrum and a Gaussian distribution for amplitude. This noise is unpredictable in nature, and cannot be compensated for, but the root mean square value of its current is modeled and considered during circuit design, especially when resistance is a critical component in the design.

1.2.2 Flicker Noise

Flicker noise or 1/f noise is the noise which has power spectral density proportional to the reciprocal of frequency. The frequency of pink noise is low, and its origin is still under research. Some researchers claim it is due to imperfections in silicon crystal.

1.2.3 Substrate Noise

Substrate noise, or *substrate coupling noise*, is the noise injected to a node from another node through the substrate. Reduced feature sizes leads to very small distances

between transistor nodes increasing the effectiveness of this noise coupling. The major substrate noise injection methods are impact ionization, capacitive coupling and noise coupling [14].

Impact ionization occurs in the saturation region of operation for MOS devices when a high electric field near the drain causes some charge carriers to get agitated enough to emit the attained energy to another charge carrier causing further ionization [14]. The electron hole pairs that are generated causes current to flow between drain and substrate; resulting in substrate voltage variations.

Capacitive coupling noise occurs when voltage fluctuations in source or drain terminals couple through their corresponding reverse biased junction capacitance to the substrate [14]. Substrate noise coupling is very similar to capacitive coupling but it is normally related to noise injected from the clock signal, power supply lines and analog device blocks. The major problem due to substrate noise, especially in analog circuits, is its effect on the transistor threshold voltage. The effect of substrate voltage on the threshold voltage can be explained by the following equation:

$$V_T = V_{TO} + \gamma(\sqrt{V_{SB} + \phi_F} - \sqrt{\phi_F}) \qquad [11]\ (1.1)$$

In equation 1.1, V_T is the threshold voltage with substrate bias, V_{SB} is the substrate bias, ϕ_F is the surface potential, V_{TO} is the threshold voltage at zero substrate bias and γ is the body effect parameter.

1.2.4 Switching Noise

Switching noise is the noise caused due to transistor switching. This noise is a major component of the noise that causes most of the voltage fluctuation on the supply line. The basic operation of a digital circuit is switching, which is the transition of transistor operation from one region of operation to another. During switching, the resistance in the channel changes thus causing a sudden change in current demand, which triggers various voltage fluctuations. The various elements that cause this voltage fluctuation due to switching are discussed in this section.

A typical power supply network is illustrated in Figure 1.1 [2], which depicts current flow in the grid during switching. When the inverter at the far end of the power supply switches, the capacitance at its output connects to the power supply line through the source drain resistance of the MOSFET.

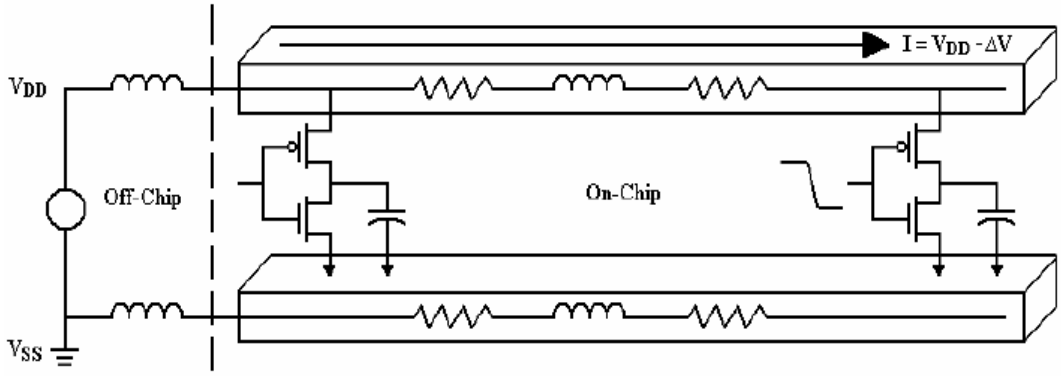

Figure 1.1 Power Supply Noise (V_{DD} droop) [2]

In the case that the inverter input is switched from high to low, the reduction in PMOS resistance and increase in NMOS resistance causes current proportional to this total resistance to flow from VDD to ground, which is called *crossbar current*. The

crossbar current is highest when the resistance sum of the PMOS and NMOS transistors is its smallest. This current flow is restricted by two power grid parameters, namely the power supply resistance and inductance. This causes a voltage drop ΔV, which is the sum of the resistance (R) voltage drop and the voltage drop due to the inductance L that resists the rate of change of current.

$$\Delta V = IR + L^* dI/dt \quad [2] \ (1.2)$$

Similar noise occurs in the ground line when the inverter input switches from low to high, causing a rise in the ground line that is commonly known as *ground bounce*.

The crossbar current that flows when both NMOS and PMOS remain conducting increases the current demand during switching. This noise due to transistor switching varies across the chip and its value depends on the switching activity in the region and the distance from the off-chip power supply.

The resistance component responsible for voltage drop arises from the resistivity of the conducting metal being used and its dimensions.

$$R = \rho^* L/A \quad (1.2)$$

In equation 1.2, R is the total resistance, ρ is the resistivity of the metal, L is the length and A is the area of cross section. Grid resistance can be reduced by lowering resistivity; such as replacing aluminum metal interconnects with copper metal interconnects. This process is known as the *copper damascene* process [3]. Long traces also increase resistance, which can cause a substantial voltage drop. This is the reason that hot spots occur normally in the center of the chip in dual inline packages since the

off-chip supply voltage is further away from the center. In the case of a ball grid array package, the problem of long supply traces is reduced significantly.

Inductive voltage drop arises due to the rate of current change through the inductor. An inductor is a passive electrical component capable of storing energy in the form of a magnetic field created by the current flowing through it.

$$V=L*dI/dt \qquad [2]\ (1.3)$$

In equation 1.3, V is the voltage potential, L is inductance of supply lines and dI/dt is the rate of current.

The voltage supply grid interconnects act as inductors because of the current loop it creates between layers. Clock frequency in modern ASIC's have considerably increased, which implies that noise due to inductance and compensation methods plays a crucial role in modern power distribution system.

Power supply noise is often compensated by adding a capacitor in parallel with the power supply lines, commonly known as a *decoupling capacitor* (decap). The capacitor connected across the power supply near the switching element provides the instantaneous current demand, which reduces power supply noise considerably. The effectiveness of these passive decaps depends on their proper value selection and placement. The decoupling capacitor is normally constructed as an NMOS capacitor, which has the drawback of high leakage current. The present passive decap design can occupy a very large area with about 15-20% of the die used in the case of high-end microprocessors [10]. This results in increased leakage power, which is undesirable. Another problem with passive decap is its reliability, which decreases with oxide

thickness because of the lower voltage level needed for oxide breakdown. This reduced oxide thickness also leads to an increase in gate leakage due to gate tunneling.

1.3 Research Objective

This thesis focuses on discussing the present noise suppression techniques, their drawbacks and the design of a distributed active decap that is used to suppress local supply noise and provides reduction in decap area over conventional passive decap. The design also takes into account the possibility of breakdown due to electro static discharge.

1.4 Organization of the Thesis

This section explains the organization of the remaining chapters in this thesis and brief review of their content.

Chapter II: Previous Noise Suppression Techniques

This chapter explains the present noise suppression techniques, their working principles, their drawbacks and also evaluates the need for a more efficient noise suppression technique.

Chapter III: Proposed Active Decap Design

This chapter deals with the design objectives and issues related to active decap design in 90 nm and the theoretical verification of the design. It also explains some limitations of the design.

Chapter IV: Simulation Setup & Results

In this chapter the simulation setup used to test the design is explained and the results obtained are presented.

Chapter V: Conclusion & Future Work

This chapter summarizes the results obtained, provides conclusions and discusses future research possibilities.

CHAPTER II

PREVIOUS NOISE SUPPRESSION TECHNIQUES

2.1 Introduction

The most common method used to design decoupling capacitors uses MOS transistors, but many factors such as ESD risk and high gate leakage makes it obsolete in 90 nm and below. This chapter provides a brief overview of the commonly used design methodologies for decap design and discusses their advantages, disadvantages and suitability for use in 90 nm technology.

2.2 Passive Decap

Decoupling capacitors are normally used in designs to reduce supply noise. The most common methods for incorporating decoupling capacitors are the use of passive decaps because of its simple construction and integration in the design. Passive decaps are normally implemented using NMOS transistors and are so named because its capacitance value does not change during operation. The basic layout and design of an NMOS decap is illustrated in Figure 2.1 [4]. The basic working of an NMOS decap is the same as the MOS capacitor working in strong inversion region. The strong inversion region of operation important as it offers constant capacitance and low series resistance.

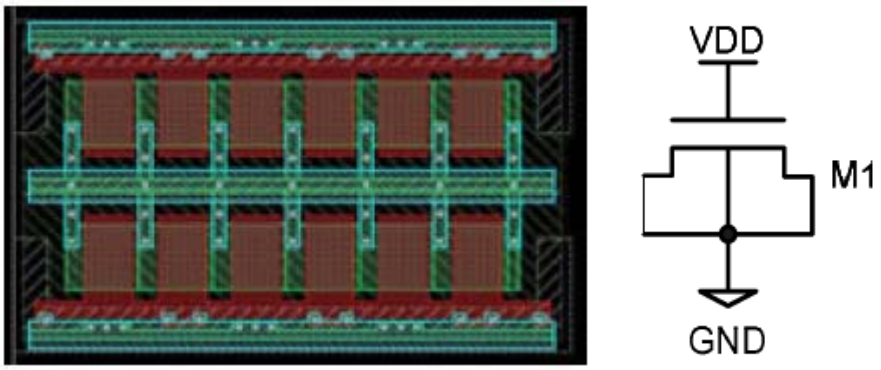

Figure 2.1 NMOS decap Layout and Design [4]

The simplest and most effective way for modeling a decap is to use a resistor, (Re) in series with a capacitor (C).

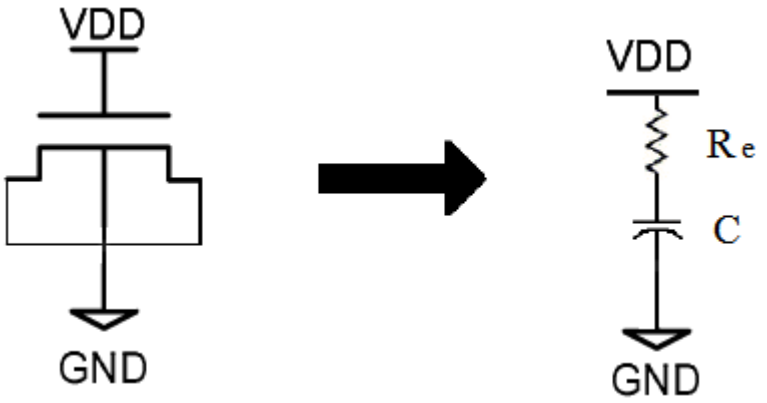

Figure 2.2 NMOS Decap equivalent circuit [13]

The effective capacitance and resistance of a decap at low frequency is given by equation 2.1 and equation 2.2

$$C = C_{OX}WL + (C_{OLGS} - C_{OLGS})\,W \qquad (2.1)\ [13]$$

$$Re = L/6\ \mu C_{OX}W\ (V_{GS} - V_T) \qquad (2.2)\ [13]$$

Passive decaps are often used in white spaces between blocks but it is preferable if used inside blocks, as the effectiveness of the capacitor decreases with increase in distance between switching element and capacitor. Decap cells can be added to a standard cell library for automatic placement of the capacitors within blocks.

The standard N+P configuration used within a standard cell block is shown in Figure 2.3[13].

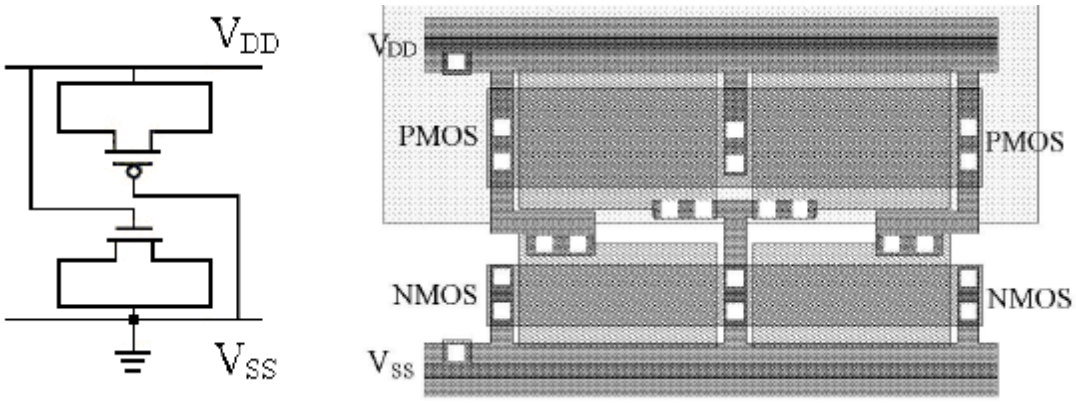

Figure 2.3 Standard N+P decap configuration and layout [13]

The disadvantages of the above discussed decap approach are its area, ESD and leakage. Leakage in MOSFETs can be from source to body, drain to body, gate to body and source to drain. Normally gate to body leakage is ignored since it is negligible but as the technology scales the oxide thickness decreases, thus increasing gate tunneling leakage. The reduced oxide thickness also makes the capacitor prone to *Electrostatic Discharge* (ESD). Electrostatic discharge is the sudden increase in current due to the introduction of a high voltage potential into the system that may be caused by an electrically charged human body or a conductor. ESD was not an issue in 180 nm and

above technologies since the oxide thickness was large enough to withstand a sudden current surge but in 90 nm and below ESD consideration during the design is crucial. An alternate decap design known as *cross-coupled* decap is used at 90 nm and below to account for ESD.

Figure 2.3 illustrates the layout and schematic of a standard cross coupled decap employed to reduce the possibility of oxide breakdown due to ESD.

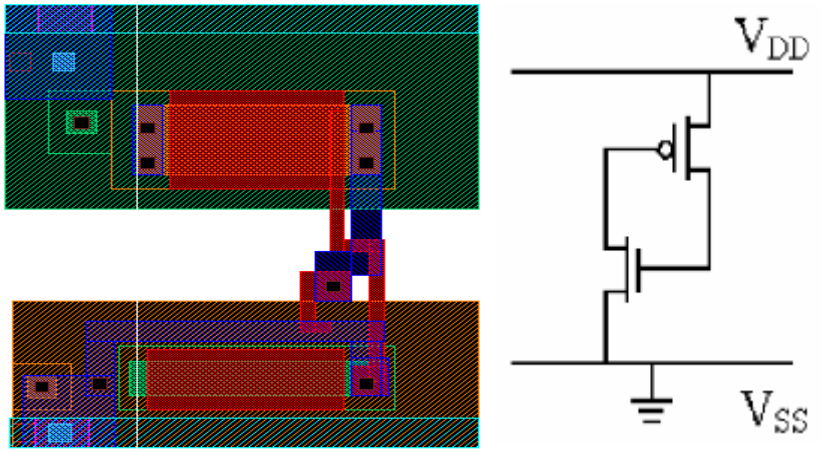

Figure 2.4 Layout and Schematic [13] of Standard Cross coupled Decap

The standard cross coupled decap uses a PMOS and NMOS transistor similar to a standard N+P decap configuration, but here the gate of one transistor is connected to the drain of the other thereby increasing the series resistance involved,[13] which improves ESD tolerance. But, this increase in series resistance adversely affects transient response due to larger RC delay.

We should also note that the gate leakage involved is unaltered in this case. Many alternate versions of the cross coupled decap have been studied [13] to improve transient

response, ESD protection and gate leakage but each improvement cannot be made without affecting the other parameters. Trade-offs between these parameters were studied and cross coupled decap for specific needs were suggested in [13].

One other type of decap used to solve the ESD problem is the thick oxide decap, which uses the thicker oxide layer provided for I/O cells as a way of increasing the oxide breakdown voltage. A similar effect can also be achieved by connecting normal decaps in series but the problem with this method is the large decap area required. If two decaps are used in series, the breakdown voltage and the area consumed for a given decap value is doubled.

2.3 Other Passive Decap Involving Process Changes

Previously we discussed only the common methods used for decap design that does not involve any extra process steps. In this section, we will discuss two of the commonly used process steps for enhancing the decap efficiency in both area and leakage.

One such method is usage of an oxide with a high dielectric constant for reducing leakage. Oxide capacitance is one of the process parameters that define the physical properties of a MOS transistor. Oxide capacitance per unit area (Cox) is the ratio of oxide permittivity to oxide thickness.

$$Cox = \varepsilon ox / tox \qquad [11]\ (2.3)$$

In equation 2.3, εox is εo (permittivity of free space)*k (dielectric constant) and tox is the oxide thickness. Oxide capacitance per unit area defines the area consumed to create decap for a given value of capacitance. An MOS transistor requires a high gate

capacitance to form and maintain a channel during its operation. Shrinking feature sizes reduces gate area, thus requiring a reduction in oxide thickness in order to maintain oxide capacitance. This reduction in oxide thickness leads to an increase in gate leakage. To overcome this problem without changing oxide thickness a high–K dielectric can be used. Some of the high-K dielectrics used instead of silicon dioxide (k=3.9) are hafnium oxide (k=20), zirconium oxide (k=23) and silicon nitride (k=6.5-7.5) [3]. These gate oxides are applied using metallo-organic chemical vapor deposition process or sputtering [3].

The other method is the use of *Metal Insulator Metal* (MIM) capacitors. They are capacitors formed by two metal layers separated by an insulator. The problem with the basic metal-insulator-metal capacitor is its low capacitance per unit area. The introduction of alumina or tantalum pentoxide as the insulating medium can be used to increase the capacitance per unit area [3]. Since the distance between the metal layers is large in comparison to the gate oxide thickness they have much less leakage and high ESD tolerance.

2.4 Gated Decap

Gated decap is a method suggested to reduce gate leakage by incorporating a control transistor that can be turned on or off as required.

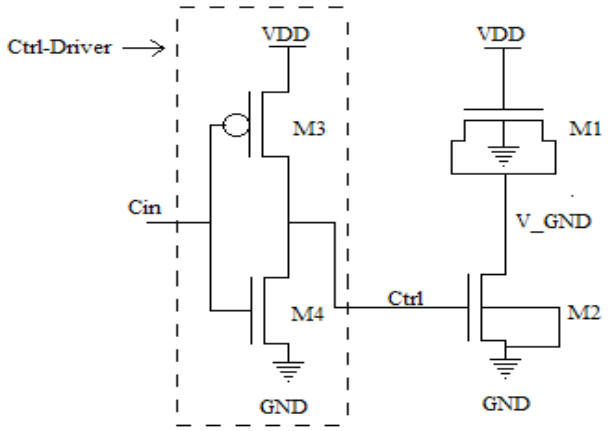

Figure 2.5 Schematic of Gated Decap [4]

The gated decap structure in Figure 2.5 [4] shows a control transistor and an inverting driver used for driving the control transistor. The gated decap operation can be divided into *active* and *power saving* modes. Active mode is when the control transistor is driven high connecting the bottom plate of the decap to ground. In this mode, the decap reduces noise in the power supply lines. In power saving mode, most of the leakage current associated with the decap is removed since its path to ground is eliminated except for gate to body leakage.

Gated decap relies on the fact that most switching occurs near the clock edge and not throughout the clock cycle. This was found to be true in most cases except in critical path or near-critical paths where switching occurs for most of the clock cycle. One study in 70 nm technology showed that a power savings of up to 99.4% [4] with a very slight increase in area. The problem with gated decap is that it can introduce unnecessary oscillations into the system when switching between operation modes. Furthermore,

gated decap requires an active control strategy to effectively minimize power supply noise. This design is not favorable if area is a major constraint in the design.

2.5 Active Decap Techniques

Until now we discussed passive decaps with a constant capacitance value. In this section, we discuss techniques that allow the capacitance value to change during operation to increase the decap efficiency.

Nearly all active decap techniques relies on the idea of current injection into the supply lines when the circuit experiences high current demand in order to reduce voltage fluctuations [5] [6]. This current injection reduces the total current amount as well as the rate of current required by the switching components from the power supply. Many efforts have been made in the past to achieve reduction in noise and area without the use of additional process steps. In the following sections, we discuss two methods of active decap design that involves varying decap capacitance during operation.

2.5.1 Switched Decoupling Capacitor

A switched decoupling capacitor involves two capacitors connected in parallel that can be switched to be connected in series, thus increasing the voltage across its terminal during voltage droop conditions. Figure 2.6 [5] below illustrates switched decap operation.

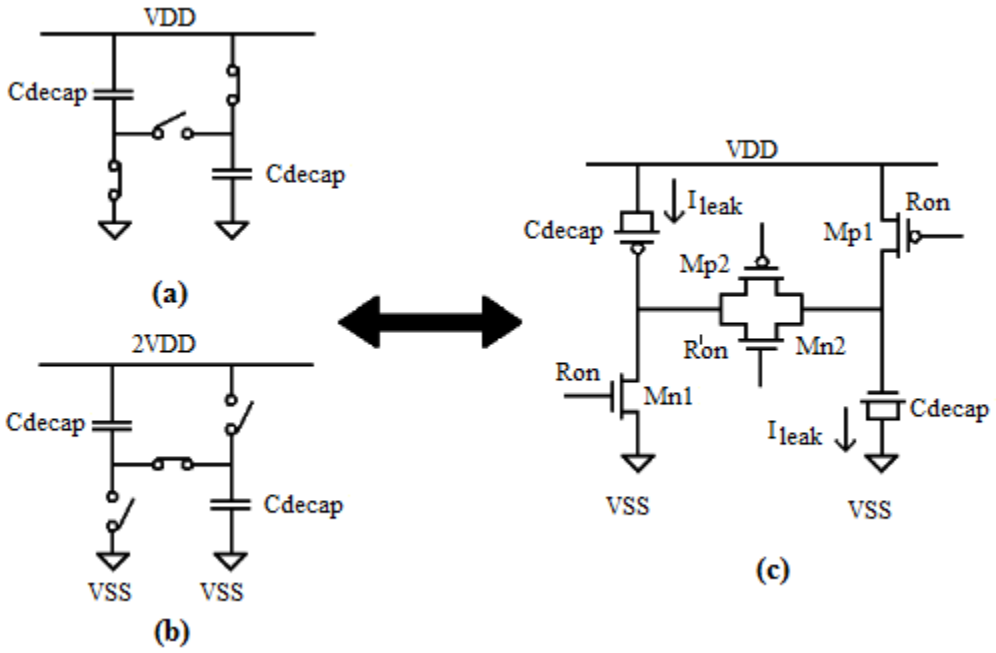

Figure 2.6 a) Decap in parallel during stand by b) Decap in series during operation c) MOS implementation of switched decap [5]

During standby mode, two capacitors are connected in parallel as shown in Figure 2.6(a) [5] that acts like two normal passive decap with equivalent capacitance of 2*Cdecap [16]. The total charge stored in the decap is $Q=2*Cdecap*V_{DIFF}$ [16] where Cdecap is the capacitance of the decap and V_{DIFF} is the voltage difference between VDD and VSS. When the control transistors are switched the capacitors are connected in series as in Figure 2.6(b) [5], with the effective capacitance of the circuit reduced to 0.5*Cdecap. The charge that was previously stored in the capacitor is subjected to a lower effective capacitance. This leads to a voltage increase across its terminal to uphold the law of charge conservation. The new voltage across its terminals in the ideal case is $4*V_{DIFF}$ neglecting the resistance of the MOS transistors [16]. However, this case can be never achieved because of non idealities of the decap circuit [16]. The switching of the

capacitor from series to parallel and vice versa can be used to decrease or increase V_{DIFF} by a factor of 2 [5]. Figure 2.6(c) [5] depicts the MOS implementation of a switched decoupling capacitor.

The major design issues that we need to consider for proper operation is the design of a MOS transistor with low on-resistance. Decap's ideal operation is restricted by the voltage drop across the on resistance of the transistors, which reduces the effective voltage across the capacitor. On resistance in the order of a few tens of ohms [5] can be obtained only if the MOS transistor size is in the order of 5000 times the feature size. However, such large transistors require a strong signal to drive them, which indicates the necessity of designing a large driving circuit that will consume significant power. The large area required for the switching transistor and driving circuit makes this design unsuitable for decap distribution within blocks.

The main advantage of this design is that it does not require any external supply for operation. There are many different control circuitry implementations used for switching between standby and active modes, one such implementation [5] is discussed in this section.

Figure 2.7 shows the control method for a switched decoupling capacitor based on an active decoupling capacitor [5]. In [5], the author uses three stages for controlling the switched decap. The first stage is reference voltage generation, where a reference voltage of VDD/2 is generated. This stage also has an enable switch for turning on or off the active decap. The second stage is a high pass filter for reducing the low frequency noise component in the signal.

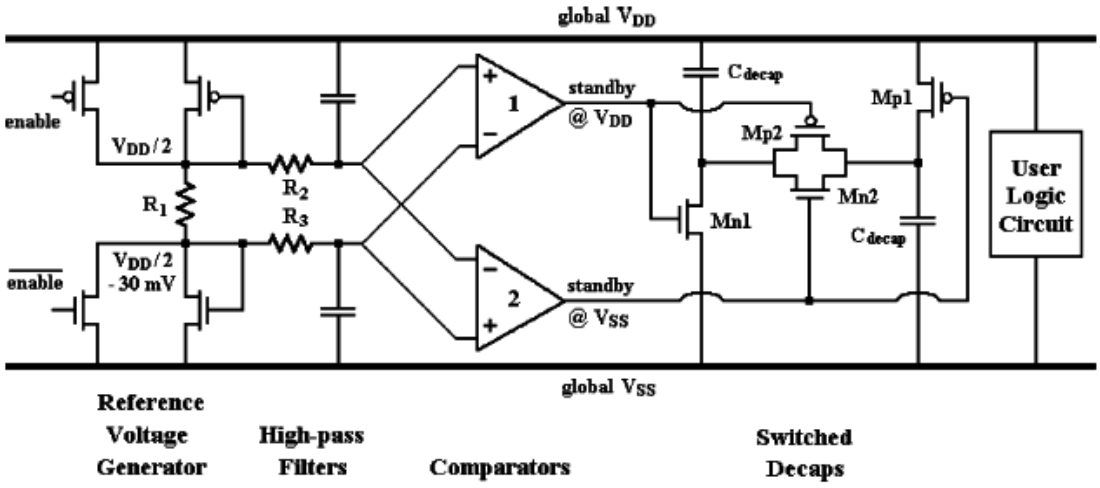

Figure 2.7 Active Decap Architecture for switched coupling capacitor [5]

The third stage involves the use of a comparator for turning on or off the 700 pF [5] decap based on the noise level in the supply. This comparator uses a preset sensitivity level of 10-15 mV and has a max dc gain of 48 db with a unity gain frequency of 1 GHz. The frequency response and power consumed by this stage determines the efficiency of the decoupling capacitor. This work introduced hysteresis voltage of 4.2 mV into the comparator design to avoid unwanted switching [5]. The static power consumed by the switching circuit was reported as 2.8 mW [5].

Feature size scaling has increased device operating frequencies, which has subsequently led to an increase in noise frequency well above the global resonance frequency. The unity gain frequency of 1 GHz in the above design is not sufficient to effectively suppress supply line noise. Other problem with this design is its unsuitability to be distributed within blocks and an ideal decap gain that is limited to only two. These limitations lead to an alternate design that involves active decap using negative feedback.

2.5.2 Active Decap using Negative Feedback

Negative feedback techniques are commonly used in systems for improving stability by reducing the error signal. The principle involved can be easily explained by the basic capacitor equation.

$$\text{Capacitor Current, } I = C * dV/dt \tag{2.4}$$

In equation (2.4) I is the current through capacitor, C is the capacitance and dV/dt is the rate of voltage change. Voltage fluctuations or noise due to switching is due to sudden change in current demand. The capacitor injects current proportional to the voltage fluctuation, thus reducing effective current demand and reducing voltage fluctuations. The effective capacitor current can be increased without altering capacitance in a circuit by increasing the rate of voltage change across the capacitor. This is achieved using by a negative feedback amplifier connected to a capacitor.

The same principle can also be explained by using *Miller effect*. Miller effect is the increase in total input capacitance of the inverting voltage amplifier due to amplification of the load capacitance.

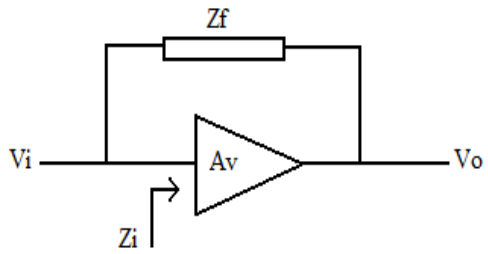

Figure 2.8 Miller Effect [15]

Miller effect in the amplifier above is due to the feedback impedance, Zf, which can be calculated as follows. Let us consider an ideal non-inverting voltage amplifier with voltage gain of Av. Considering an ideal voltage amplifier with infinite input impedance,

$$\text{Input current, } I_i = (V_i - V_o)/Z_f \quad [15]\ (2.5)$$

$$\text{Effective input impedance, } Z_i = V_i/I_i \quad [15]\ (2.6)$$

$$= (V_i * Z_f)/(V_i - V_o) \quad [15]\ (2.7)$$

$$\text{If } Z_f \text{ is purely capacitive, } Z_f = 1/j\omega C \quad [15]\ (2.8)$$

$$\rightarrow Z_i = 1/j\omega C(1-A_v) \text{ since } A_v = V_o/V_i \quad [15]\ (2.9)$$

$$\text{If we use inverting amplifier, } Z_i = 1/j\omega C\,(1+A_v) \rightarrow C_{eff} = (1+A_v)\,C \quad [15]\ (2.10)$$

The above equation proves that negative feedback through an amplifier increases the input capacitance to C*(1+Av). This approach towards increasing effective capacitance is presented in [6]. In this paper, the author utilizes a capacitor coupled input to improve frequency response and also uses pass transistors to provide the required bias voltage at the input of the differential amplifier. Figure 2.9 gives the schematic of the active decap proposed in [6].

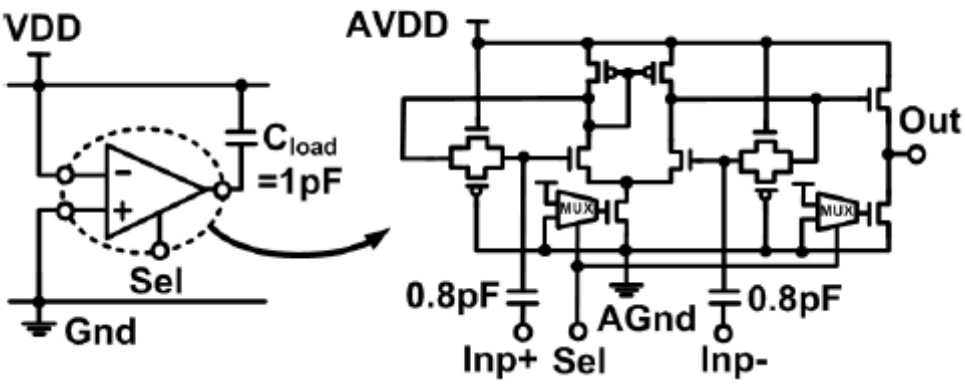

Figure 2.9 Schematic of Active Decap [6]

The schematic also shows the use of select lines for switching active decap between standby and active operation modes. The design was fabricated on a test chip 2.7 mm X 1.9 mm in a 0.18 um, 1.8 V, 6-metal process [6] with eight 16-bit Linear Feedback Shift Registers (LFSRs) and noise injection circuits in order to verify its effectiveness. The performance parameters obtained by the author are tabulated below in Table 2.1.

Table 2.1 Performance parameters of the active decap [6]

Performance Parameter	Value
DC gain	9.5
Bandwidth	535 MHz
Unity gain frequency	2.7 GHz
Maximum gain	19.9 dB

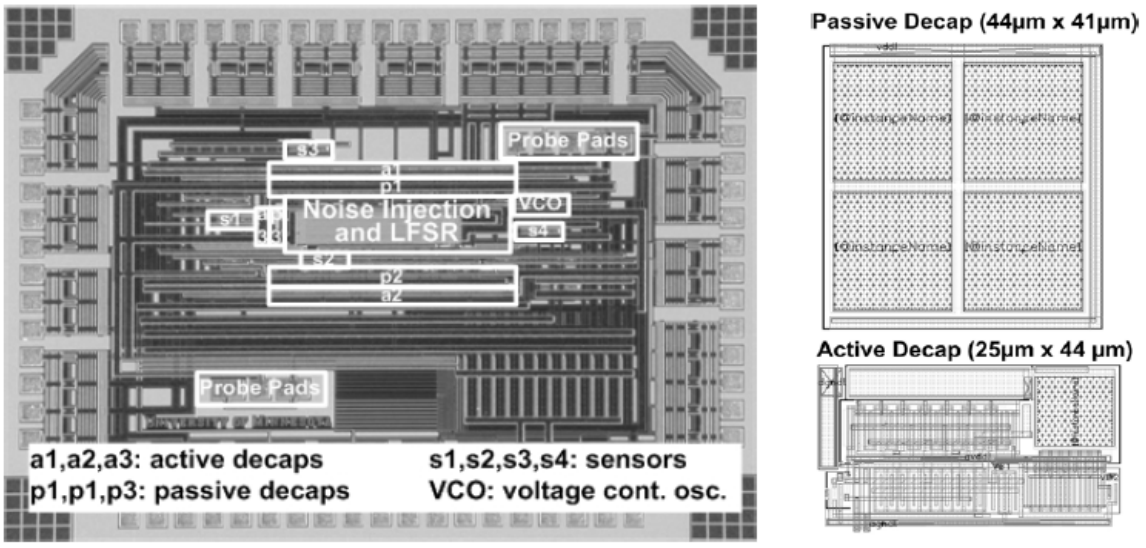

Figure 2.10 Micrograph of test chip and layout comparison of active decap and equivalent 10pF passive decap [6]

In Figure 2.10, the layout of the 1 pF active decap with its equivalent 10 pF passive decap is shown for comparison. The active decap promises a 40% reduction in area when compared to the equivalent passive decap [6]. However, the current consumed is 3.8 mA during normal operation [6].

In comparison to switched decaps, this method is much better because it provides a higher decap gain and consumes far less decap area. This decap is also suitable for block distribution because of its size when compared to a switched decap architecture. The only disadvantage of this design is that it requires an external power supply. This design can further be refined and made suitable for 90 nm by considering gate leakage, ESD and improving decap area saving.

CHAPTER III

PROPOSED ACTIVE DECAP DESIGN

3.1 Active Decap Design Considerations in 90 nm

Active decap in 90 nm and below requires certain issues to be addressed in order to achieve a practical design. The design of active decap in 90 nm must be ESD tolerant and also must consider gate leakage which until now was considered negligible.

Electrostatic Discharge (ESD) in 90 nm and below is an important issue owing to reduced oxide thickness on the order of 1–2 nm which corresponds to an oxide breakdown voltage of 5-10 V [7]. ESD is a sudden current flow that can arise due to static electricity from human contact or from any object with high voltage potential. There are many models that can be used to test device tolerance for ESD. One such model known as the *Human Body Model* is used this design [7] [8].

The Human Body Model is the most commonly used model to test for tolerance of an electronic device to electrostatic discharge. In MIL-STD-883G, the charged human body is modeled using a 100 pF capacitor and a 1.5 KΩ discharging resistance as shown in Figure 3.1 [7] [8]. During testing, the fully charged capacitor is discharged through the resistor connected in series to the device under test. The threshold voltage when the failure will occur is set and checked if the device has failed.

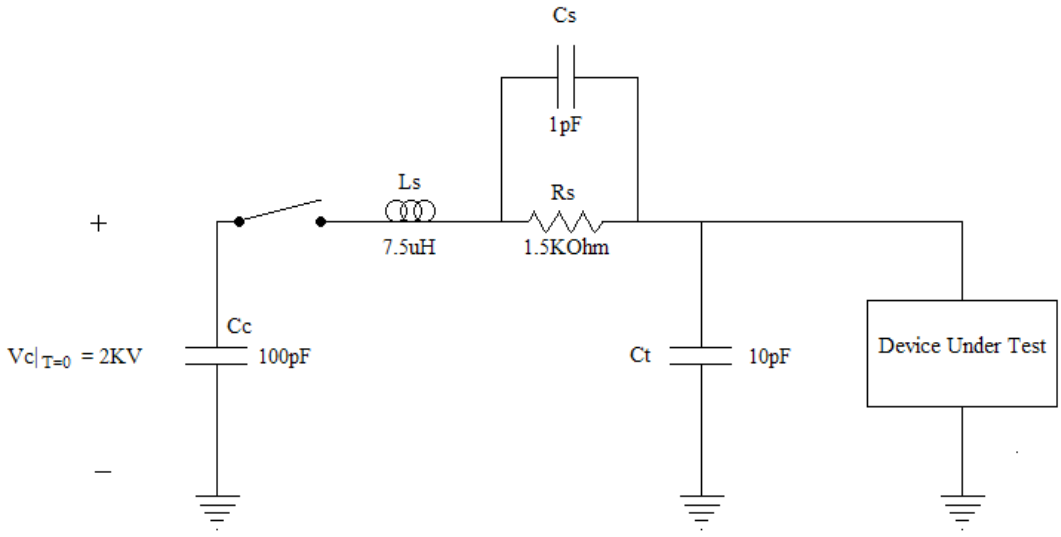

Figure 3.1 Circuit Schematic for ESD testing with stray inductance, Cs and board capacitance, Ct [7] [8]

In 90 nm and below, gate leakage is significant. As such, gate leakage should be considered in decap design because it directly contributes to static power and is dependent on the voltage bias, which is maximum in the case of decaps. The use of PMOS decap instead of NMOS is known to reduce leakage [3] but at the expense of frequency response. Gate leakage can be incorporated in design flow by using the BSIMv4 mosfet model which models both gate tunneling leakage and gate to substrate leakage [9].

3.2 Proposed Active Decap Circuit

In this section, the designed active decap is presented. Basic operation of active decap was previously discussed in chapter 2; here the design is analyzed in more detail.

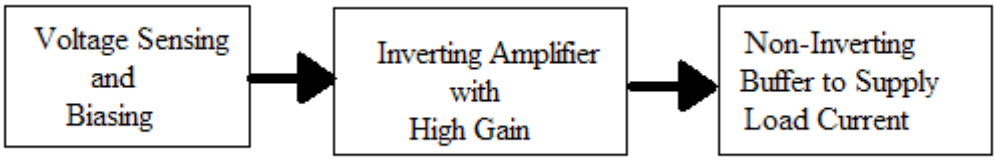

Figure 3.2 Stages in Active Decap

The stages involved in the proposed design are shown in Figure 3.2. The first stage of active decap is voltage sensing and biasing where the input voltage from VDD and VSS are voltage shifted to an appropriate input voltage for the next stage. In our case, a capacitor coupled input stage is used with a voltage divider to provide the bias voltage. A capacitor coupled input stage is very efficient in removing any DC component in the input and acts like a high pass filter reducing unwanted amplification of very low frequency noise.

The voltage divider is a simple way to provide the bias voltage, and occupies a smaller area when compared to the conventional method of using a current source for biasing. The input stage used is depicted in Figure 3.3.

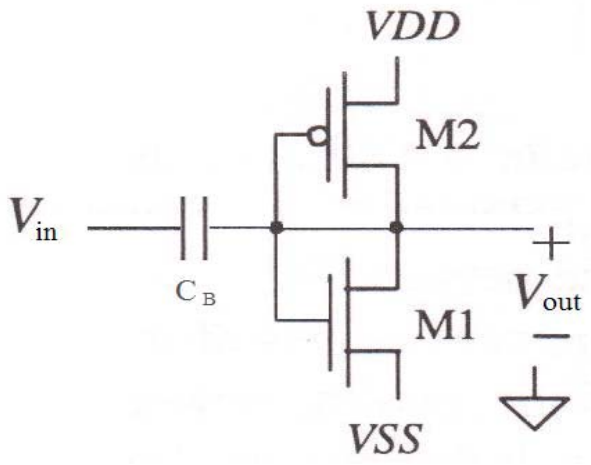

Figure 3.3 Input Stage of active decap [11]

The design of the input stage is very simple, the bias voltage is determined by the following equation (3.1) [11].

$$V_{out} = \frac{VDD - V_{THP} + \sqrt{\frac{\beta_1}{\beta_2}}(VSS + V_{THN})}{\sqrt{\frac{\beta_1}{\beta_2}} + 1} \qquad \text{[11] (3.1)}$$

In equation (3.1) above V_{THP} and V_{THN} are the threshold voltages of the PMOS and NMOS transistors, β1/ β2 is the width ratio of the PMOS and NMOS transistors considering equal gate length, and VDD and VSS are supply voltages.

The value of the biasing capacitor (C_B) determines the noise bandwidth that is amplified by the next stage; a higher C_B value implies a larger bandwidth. It is important to note that it only determines the lower frequency limit of the response and not the upper frequency limit.

The second stage of the active decap is the source coupled differential amplifier. A differential amplifier topology is a good candidate for an inverting amplifier due to its high noise rejection. During design, the slew rate required for operation above 3 GHz is considered when sizing transistor M6; sizing other transistors was done iteratively to obtain required the gain. Figure 3.4 [11] shows the schematic of a simple differential amplifier with current source load.

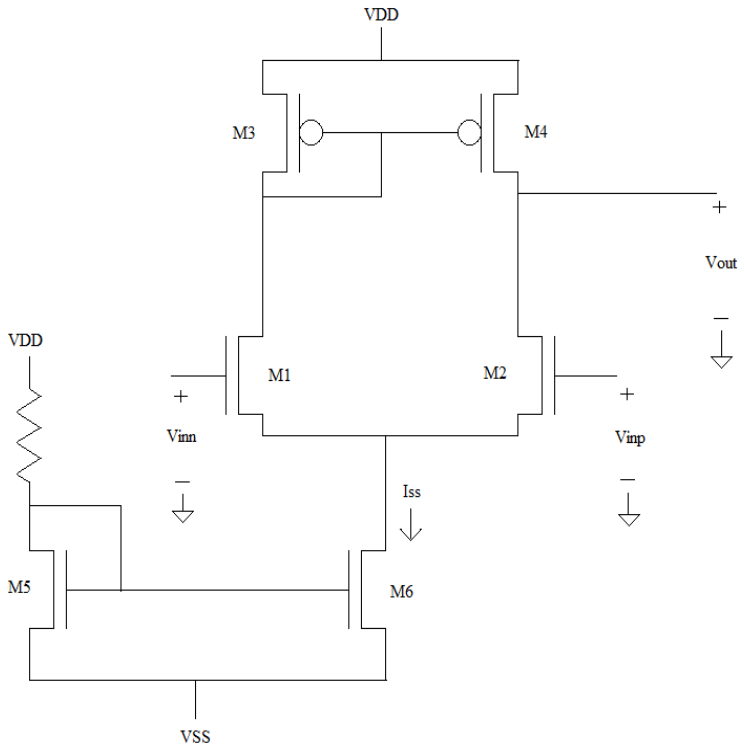

Figure 3.4 Differential Amplifier with current source load [11]

The gain of this single ended configuration is given by equation (3.2).

Voltage gain, Av=gm.*(ro2||ro4) (3.2)

In equation (3.2) gm is the transconductance of M2, and ro2 and ro4 are the output resistances of M2 and M4 respectively. The final stage is the buffer stage for providing the current requirement of the load. The final stage is implemented as an NMOS voltage follower. The final stage connects the feedback capacitor to one of the noisy power supply lines. The final design schematic is shown below in Figure 3.5.

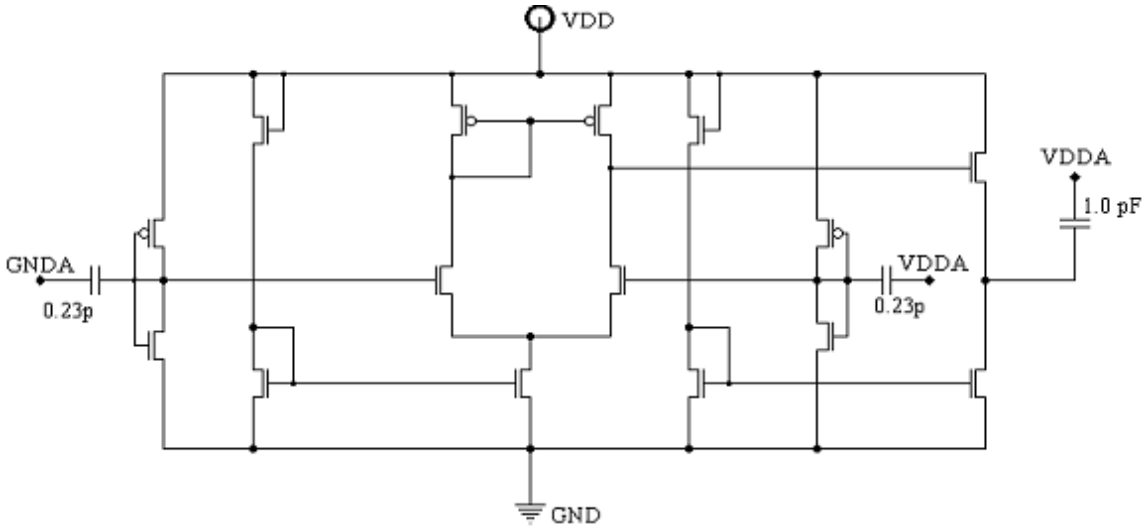

Figure 3.5 Differential amplifier schematic

The 90 nm Predictive Technology Model [12] is used for simulation as TSMC and IBM models were not available for 90 nm. Nominal corner models were used with the following technology specifications: 35nm Leff, 1 V supply voltage and a 0.15 V transistor threshold voltage.

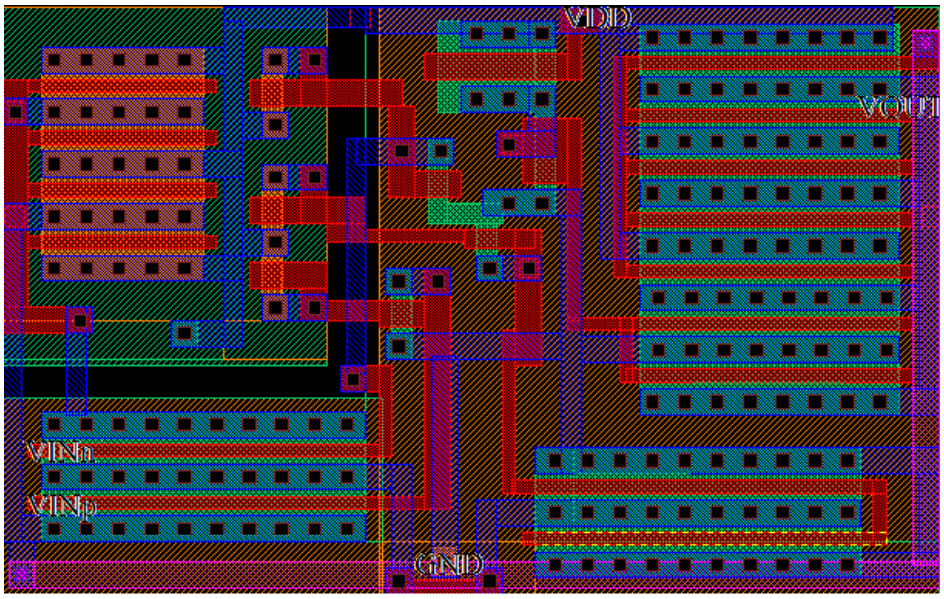

Figure 3.6 Layout of differential amplifier excluding capacitors (7.2 um X 4.5 um)

The layout for the differential amplifier is shown in Figure 3.5. The layout follows MOSIS design rules in an assumed twin well 1 V, 90 nm process with drawn gate length of 100 nm. It is important to note that the above layout does not include the biasing capacitor and feedback capacitor, which is 0.97 pF in this technology.

3.3 Layout and Response of Proposed Active Decap Circuit

The frequency response of the active decap obtained using HSPICE is shown in Figure 3.6 and the active decap layout with the capacitors is shown in Figure 3.7.

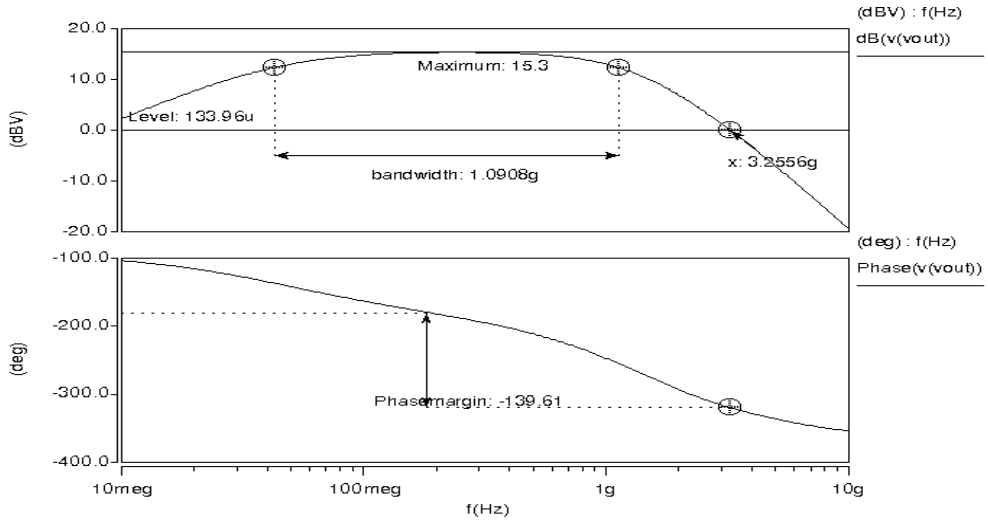

Figure 3.7 Frequency response of active decap with 1 pF feedback capacitor

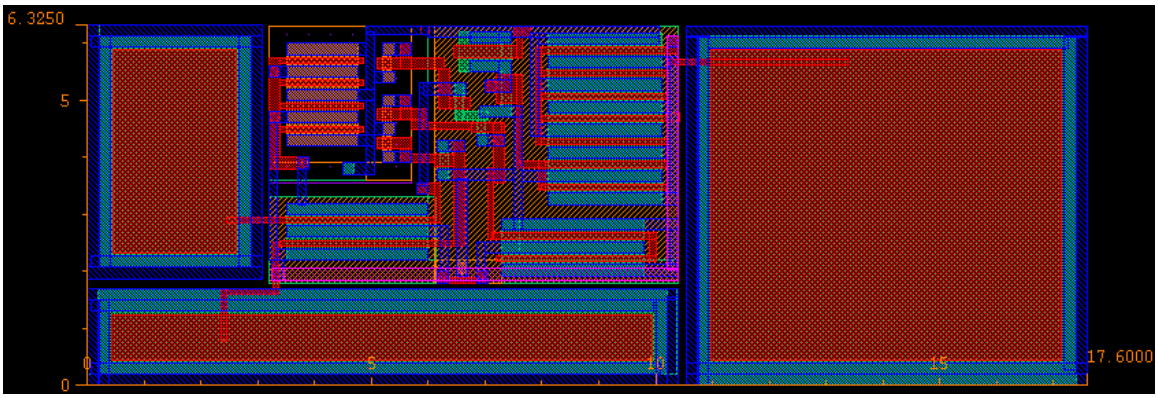

Figure 3.8 Layout of 1 pF active decap (17.6 um X 6.325 um)

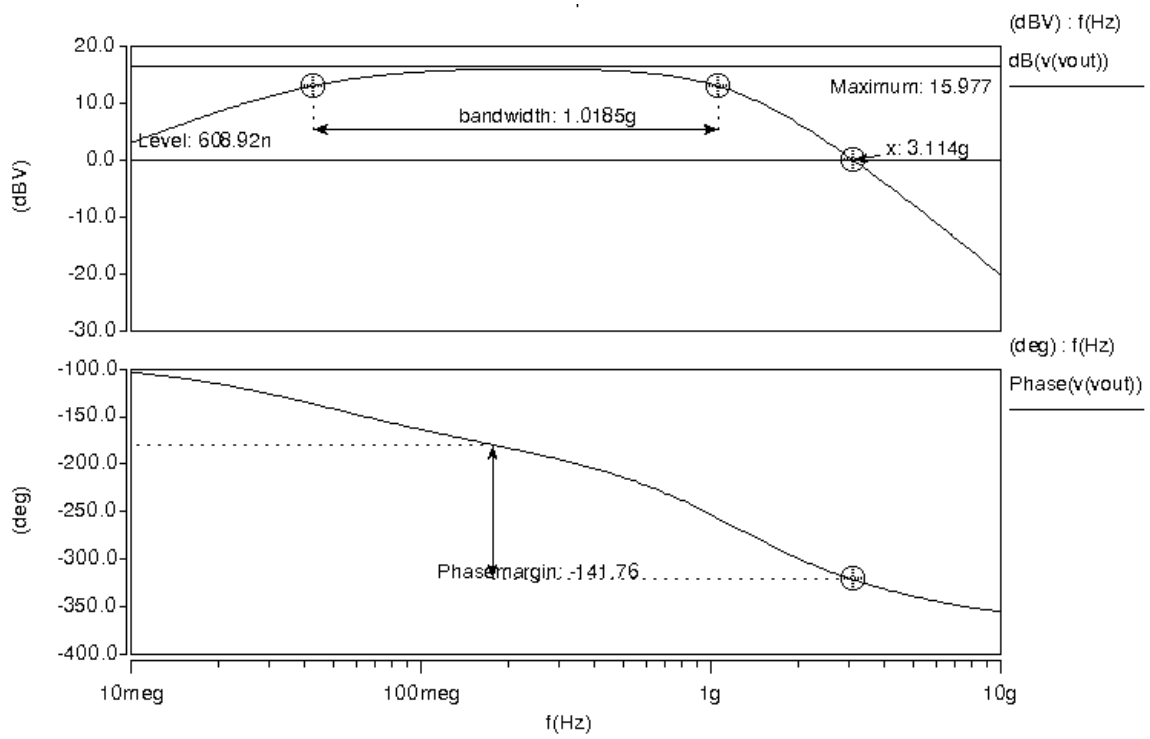

Figure 3.9 Frequency response of active decap with 1pF feedback capacitor after parasitic capacitance extraction

Table 3.1 Performance parameters of proposed active decap before and after parasitic capacitance extraction.

Performance parameter	Proposed active decap before parasitic extraction	Proposed active decap after parasitic extraction
Maximum Gain	15.3 db	15.9 db
DC gain	5.82	6.28
Bandwidth	1.09 GHz	1.01GHz
Unity gain frequency	3.25 GHz	3.11 GHz
Phase margin	41.3	38.2

From equation 2.10 and Table 3.1 the equivalent capacitance for active decap is calculated as A+1, which in our case is approximately 7. It is important to note that 7 pF is the maximum equivalent decap and is frequency dependent like voltage gain. Higher gain can be achieved by varying the transistor size at the expense of bandwidth and lower phase margin. The other reason for restricting gain of the active decap is to maintain ESD tolerance. The gain of an amplifier increases as the current through the tail of the amplifier decreases; a higher resistive path to ground for electrostatic discharge causes larger internal voltage that can cause oxide breakdown. The above design was simulated with the circuit shown in Figure 3.1 and the highest internal voltage was found to be 4.6 V which is less than 5 V, the typical oxide breakdown voltage of 1 nm oxide thickness [7].

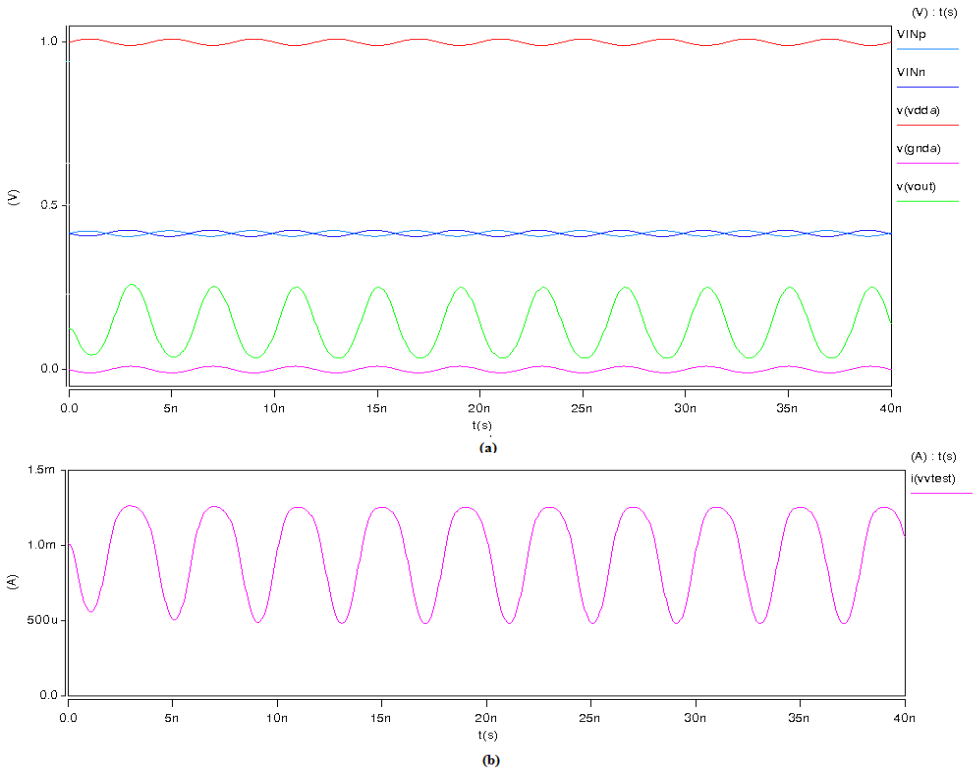

Figure 3.10 a) Transient response of active decap with 1 pF feedback capacitor b) Current waveform of active decap with 1 pF feedback capacitor

Figure 3.8a represents the output voltage that is supplied to the 1 pF feedback capacitor, when a 10 mA noise at 250 MHz is applied on both supply lines. Figure 3.8b shows current consumed by the 1 pF active decap corresponding to the previous Figure 3.8a. The average current consumed in this case is 0.95 mA. A test bench is used to analyze the performance of this decap and compare its effectiveness with passive decaps in the next chapter.

CHAPTER IV

SIMULATION SETUP AND RESULTS

4.1 Simulation Setup and Results

In this chapter, the active decap designed in the previous chapter is placed in a practical simulation test bench so that its response can be analyzed and performance compared with passive decap. Two different simulation setups are used for cross-checking and to compare its effectiveness with an equivalent passive decap.

These simulations used the BSIM4 model, which includes gate leakage [9]. However, since all capacitance parameters for 90 nm are not available, the missing parameters are taken from the 130 nm process. The simulation setup incorporates both IR and L*dI/dt losses by using a constant supply line inductance of 0.2 nH assuming a ball grid array [10] and a resistance of 0.1 Ω on both supply lines of the test circuit and the decap circuit.

The first simulation setup is shown below in Figure 4.1a and 4.1b. The setup consists of a large inverter with a minimum gate length transistor; a width of 130 um is used for PMOS and 40 um for the NMOS so that the inverter has nearly equal rise and fall time. The inverter is driven by a 200 MHz clock with 150 ps rise and fall times.

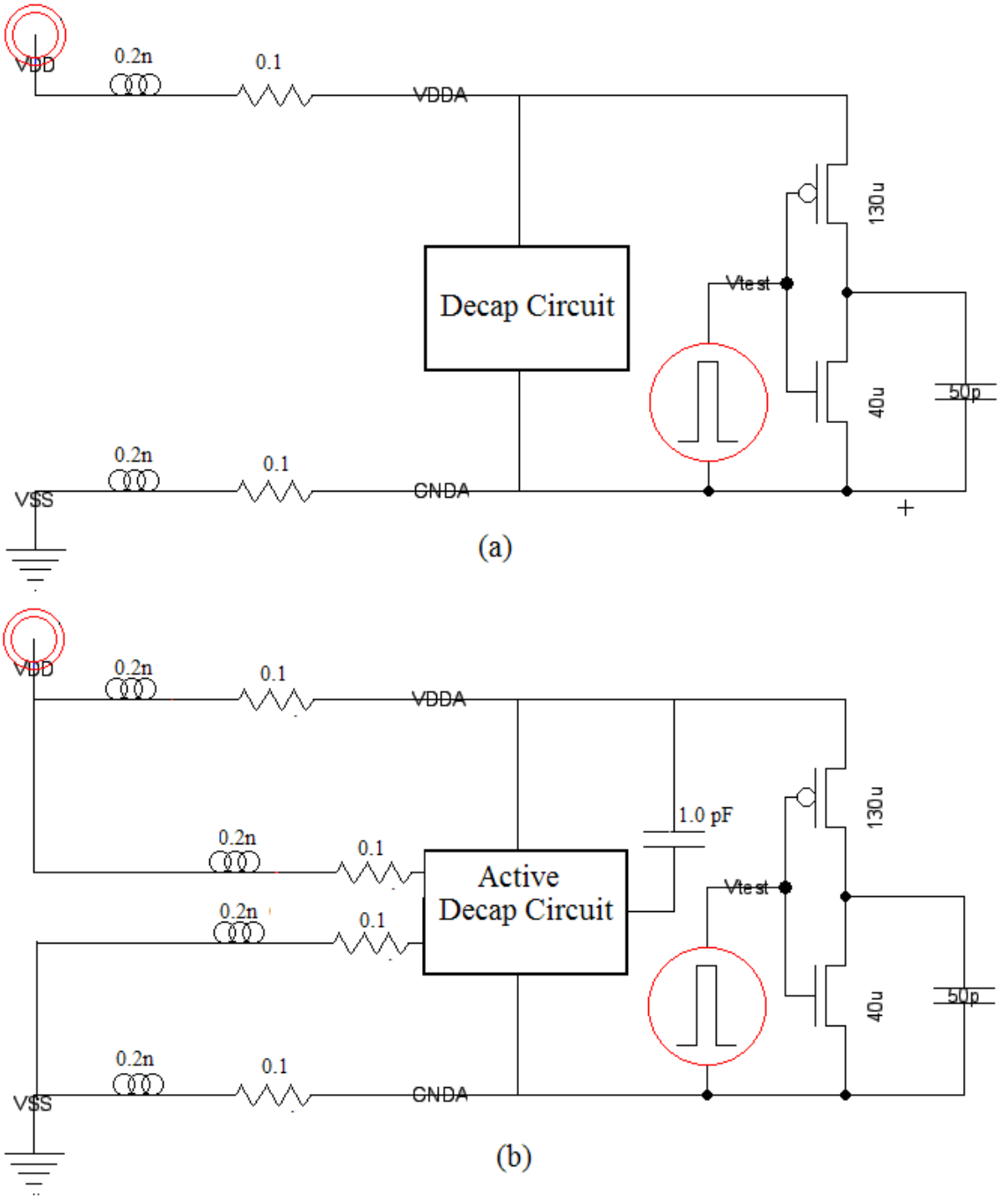

Figure 4.1 a) Passive decap test circuit using simple inverter with equal rise and fall time
b) Active decap test circuit using simple inverter with equal rise and fall time

This setup was used to confirm that a 1 pF active decap provides noise suppression higher than a passive decap occupying the same area. Figure 4.2 compares

the area of the 1 pF active decap and its equivalent 7 pF passive. The sizes of the 7 pF passive and equivalent 1 pF active decaps were 14.9 um X 17.6 um and 6.325 um X 17.6 um, respectively. The 1 pF active decap occupies the equivalent area of a 2.97 pF passive decap. This results in a 57.5% reduction in decap size in comparison to the 7 pF passive decap.

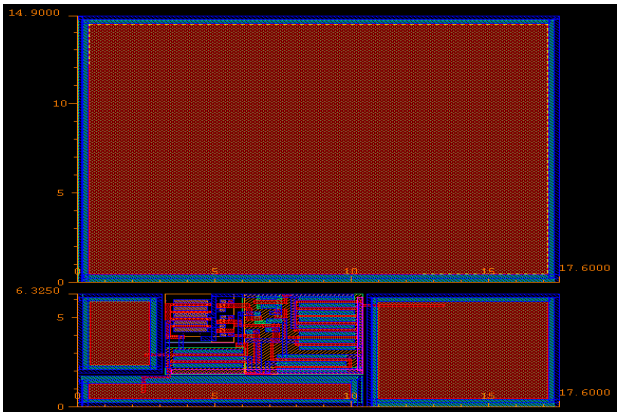

Figure 4.2 Size comparison of 1pF active and 7pF passive

Three different cases of decap are used in the test circuit.

a) 20 pF active decap

b) 60 pF passive decap

c) 140 pF passive decap

The 60 pF passive decap is chosen since it is equivalent to 20 pF active decap in terms of area and 140 pF because it is approximately seven times 20 pF, which is the maximum equivalent capacitance.

Figure 4.3 shows the differential noise between noisy voltage supply VDDA and GNDA in these three capacitance cases. The parasitic capacitance of the active decap is extracted to improve simulation accuracy.

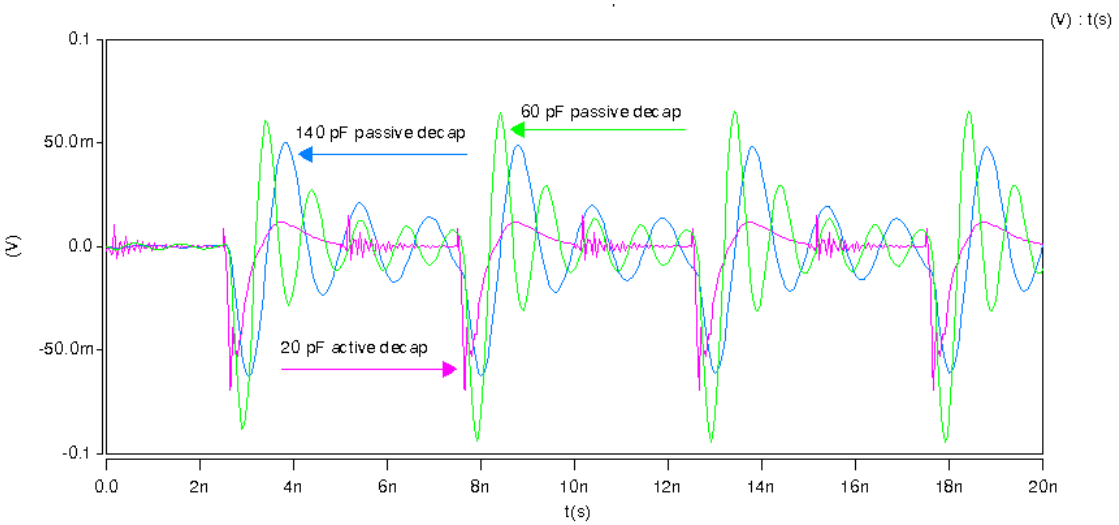

Figure 4.3 Comparison of differential noise

The HSPICE simulation of Figure 4.3 clearly shows an improvement in both average and peak noise in comparison with 60 pF passive decap. The settling time of the voltage fluctuation is also improved. In comparison to 140 pF passive decap, the 20 pF active decap has slightly high peak noise but the lack of unwanted oscillations makes active decap the better choice.

The second test circuit is a practical circuit that consists of sixteen 16-bit linear feedback shift registers (LFSRs) driven by a 500 MHz clock. The simulation circuit used is similar to the previous simulation circuit except that the inverter is replaced by the LFSRs. The layout of the sixteen 16-bit LFSR is shown in Figure 4.4.

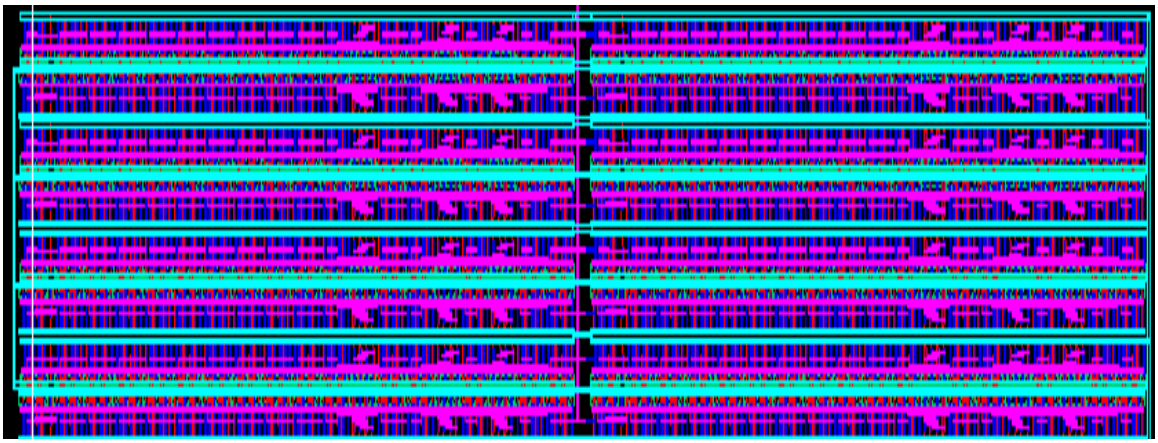

Figure 4.4 Test circuit using sixteen-16-bit LFSR (602 um x 95 um)

As with the previous simulation, we use three test cases:

a) 20 pF active

b) 60 pF passive (area equivalent of 20 pF active decap)

c) 140 pF (maximum performance which can be provided by 20 pF active decap)

This simulation was done using the Spectre simulator as it offers better convergence for this more complex circuit. The obtained results are shown in Figure 4.5.

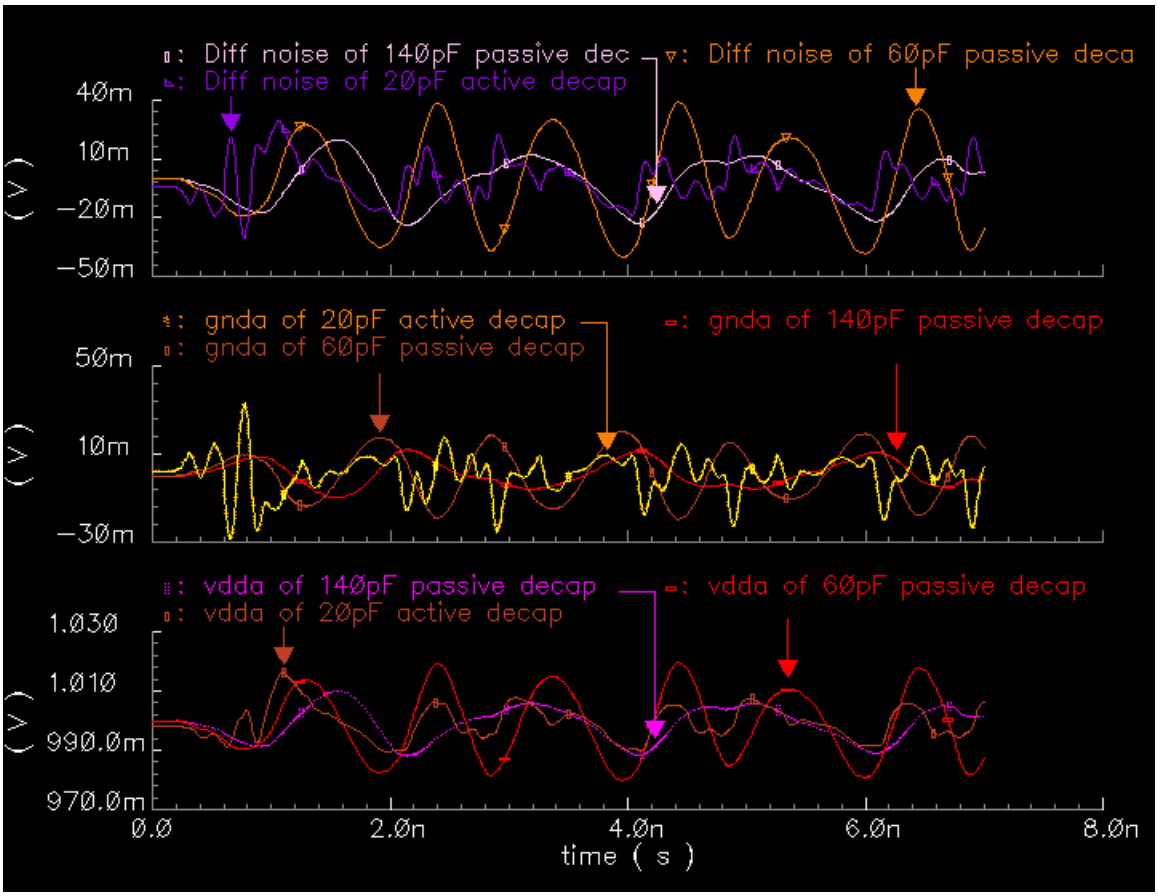

Figure 4.5 Performance Comparison between 20 pF active decap, 60 pF passive decap and 140 pF passive decap

Figure 4.5 clearly shows significant noise reduction when 20 pF active decap is compared to 60 pF passive decap. Figure 4.5 also shows that the noise reduction of the 20 pF active decap is in the same order as the 140 pF passive decap and verifies the working of the active decap in a practical test case.

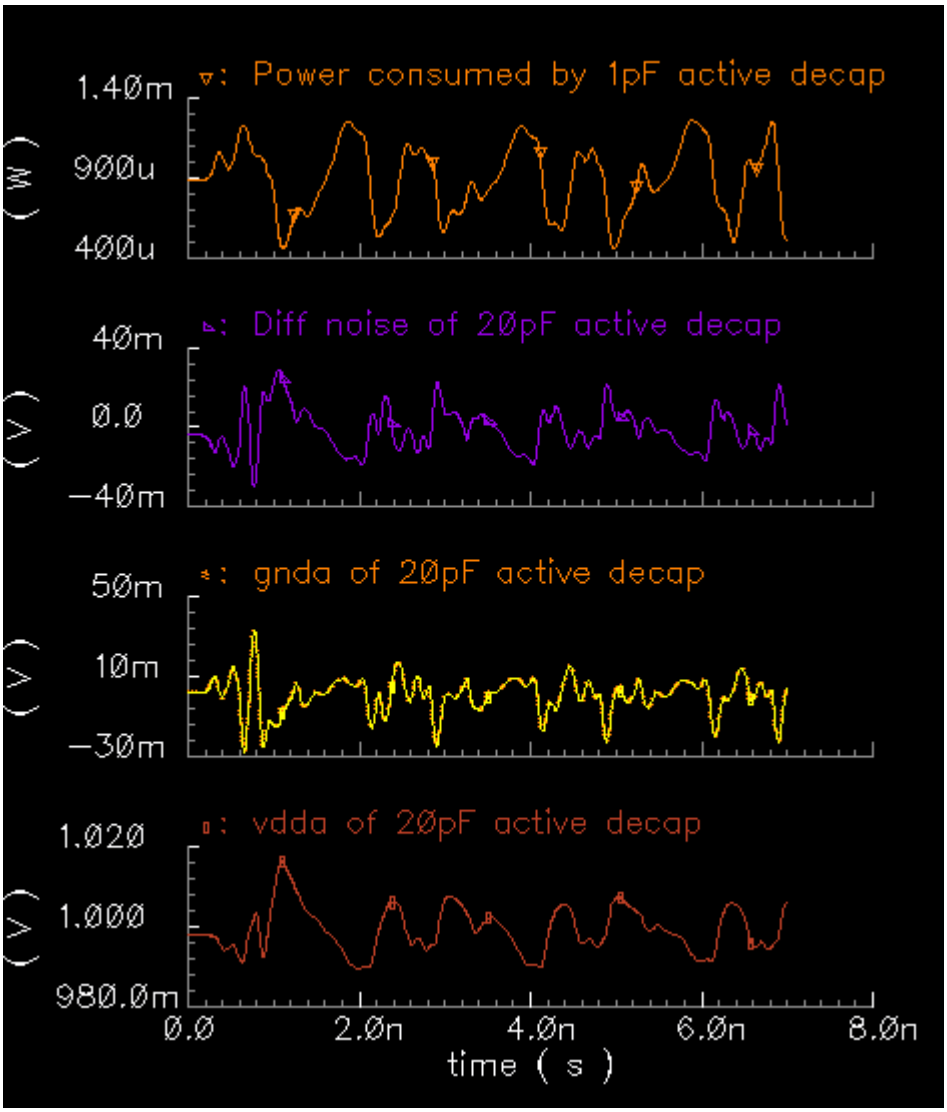

Figure 4.6 Voltage and power waveform for the active decap

Figure 4.6 gives the voltage and current waveform of the active decap, which clearly shows the relationship between power consumed and differential noise. For a decrease in differential noise, the current consumed by the active decap increases in order to compensate the current demand. The average power consumed by the 1 pF active decap in this case was found to be 0.89 mW.

4.2 Comparison of proposed design with previous designs

Table 4.1 compares the previous work [5] [6] with the proposed design. The table clearly shows the proposed design uses less power and reduced area. Since [5] is implemented in 180 nm process an exact comparison cannot be obtained but we can see that the bandwidth is nearly doubled and current consumption is reduced by a factor of 4.

Table 4.1 Performance comparison with previous works [5] [6]

	Switched Decoupling Capacitor[5] 90 nm	Active Decoupling Capacitor[6] 180 nm	.Proposed Design 90 nm
Reduction in Decap area	N/A	40%	57.5%
Bandwidth	N/A	545 MHz	1.0 GHz
Unity gain Frequency	1.0 GHz	2.7 GHz	3.1 GHz
Maximum Gain	48	20	16
Current(during Normal Operation)	2.8 mA(Stand by)	3.8 mA	0.89 mA
Phase Margin	39	42	38

CHAPTER V

CONCLUSION AND FUTURE WORK

5.1 Summary

Technology scaling has adversely affected the noise performance of modern processors. Increased clock frequency causes higher current to be drawn in a smaller time interval that is on the order of a few hundred picoseconds and this high rate of change in current causes a high inductive voltage drop. This voltage drop results in reduced voltage headroom for designers. Apart from reduced voltage headroom, this voltage drop also causes timing issues and reduces chip reliability. Current methods used for reducing these voltage variations such as passive decap are found to be insufficient as they suffer from low ESD tolerance, large area and gate leakage.

To address these issues, active decaps were proposed [5] [6]. Active decaps are designs that involve varying decap capacitance during operation to improve noise reduction. Two active decap design discussed in chapter 3 were switched decoupling decap and negative feedback decap. Switched capacitor based decap [5] was found to provide a maximum capacitance gain of two [5] and occupies a large transistor area in order to reduce on-resistance of the switching circuitry. The main advantage of this approach is the ability to control gate leakage of the MOS capacitor, while its disadvantage is its large size, making it unsuitable for usage within blocks.

The other method is the use of negative feedback for reducing voltage fluctuations. In this method, noise from the supply lines are amplified after inversion and fed back to the supply using a capacitor. This method was used in [6] and the design was implemented in 180 nm. This design provides a maximum decap gain of 11, has an area reduction of 40%, and operates up to 2.7 GHz [6]. The main advantage is its small size, which allows it to be easily distributed within blocks. Decoupling capacitor distribution is very beneficial because it improves capacitor effectiveness by reducing resistive distance between the switching element and the capacitor.

The proposed design uses the same principle as in [6] with some modification to take into account issues such as ESD tolerance and gate leakage. The maximum voltage gain of the design is 6.29, which can be increased at the expense of bandwidth. This design provides a maximum decap gain of 7 that results in a reduction of area by 57.5%, and operates up to 3.11 GHz. The high area reduction provided by this design allows easy distribution of the active decap within blocks.

Thus, a practical active decap that provides good ESD reliability, reduced gate leakage, and small area has been presented

5.2 Future Work

The current design addresses most of the issues in 90 nm but future scaling requires more design effort, such as the use of high-k dielectric for the active decap in order to increase ESD tolerance and capacitance per unit area. It is also important to remember that active decap improves noise reduction at the expense of power. Hence, an optimal trade off could be made between passive and active decap approaches in order to maximize noise reduction efficiency. The placement of the active decaps is also an issue that must be addressed, as this also has an impact on efficiency.

The current design can also be modified by adding a multiplexer to the biasing circuitry, which would allow gating of active decap. Active decap gating helps to reduce standby power when its operation is not required.

The decap performance in this paper has been evaluated via simulation, but obviously a manufactured test chip would be better in order to verify the simulation results.

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