DESIGN OF A HIGH GAIN AND POWER EFFICIENT OPTICAL RECEIVER FRONT-END IN 0.13 μm RF CMOS TECHNOLOGY FOR 10 GBPS APPLICATIONS

Diseño de front-end de receptor óptico de alta ganancia y eficiencia de potencia en 0.13 μm de tecnología CMOS de RF para aplicaciones de 10GBPS

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ABSTRACT

In this paper, two versions of a complete RF frontend for a 10 Gbps optical receiver are presented. The RF frontend consists of a transimpedance amplifier and a limiter amplifier. Two versions of the TIA amplifiers are proposed. The first topology has 54 dB transimpedance gain, 11.5 GHz bandwidth and has an input current noise density of only 6.8 pA/√ Hz. The second topology is composed by a cascade of two inverters. This topology has 48 dB transimpedance gain, 11.2 GHz bandwidth, a input current noise density of 8.9 pA/√ Hz and occupies an area of only 0.048 mm2. The limiter amplifier for both optical receivers is a five stage cherry-hooper amplifier with active inductors optimized for low power. The main amplifier has 38 dB gain, 9.8 GHz Bandwidth, 69 mW of power consumption and only 0.171 mm2 of die area. The complete RF front-end is fully integrated and has 10 GHz bandwidth. The circuits were designed in 0.13 μm RF CMOS technology.

Keywords: CMOS technology, transimpedance amplifier, limiter amplifier, optical receivers, broadband amplifiers.

RESUMEN

Este artículo presenta dos versiones de una RF frontend completa para un receptor óptico de 10Gbps. El RF frontend consiste de un amplificador de transimpedancia y amplificador limitador. Se proponen dos versiones de amplificadores TIA. La primera topología tiene una ganancia de transimpedancia de 54 dB, ancho de banda de 11.5 GHz y una salida de densidad de ruido de corriente de solamente 6.8 pA/√ Hz. La segunda topología esta compuesta de una cascada de dos invertores. Esta topología tiene una ganancia de 48 dB de transimpedancia. El amplificador limitador para ambos receptores ópticos es un amplificador de cinco etapas cherry-hooper con inductores activos optimizados para potencia baja. El amplificador principal tiene 38 dB de ganancia, 9.8 GHz de ancho de banda, 69 mW de consumo de potencia y solamente 0.171 mm2 de área muerta. Esta completa fachada de RF está integrada y tiene 10GHz de ancho de banda. Los circuitos fueron diseñados en 0.13 μm de tecnología CMOS de RF.

Palabras clave: Tecnología CMOS, amplificador de transimpedancia, amplificador limitador, receptores ópticos, amplificadores de banda ancha.

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I. INTRODUCTION

The main purpose of this paper is to describe the design of a RF front-end for a 10 Gbps optical receiver. The main blocks of the receiver chain are the transimpedance amplifier and the limiter amplifier. Figure 1 shows a typical optical receiver architecture [1].

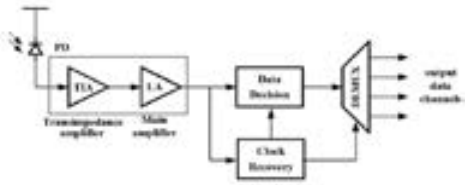

Fig. 1. Optical Receiver Architecture.

A 0.13 µm RF CMOS technology was chosen for this work, since it offers a better compromise between cost, performance and integration. The available library offers nMOS transistors with 110 GHz transition frequency, 8 metallization levels, capacitors and inductors optimized for high resonant frequency.

II. CIRCUIT LEVEL DESIGN

A. Technology Characterization and TIA Design

The transimpedance amplifier is the first block of the optical receiver chain and must be optimized for low noise and broadband frequency performance. In order to reach this goal, the layout was carefully designed and the bias point for the transistors was defined based on the density current plots. Figure 2 was used to define the optimum bias point for the circuits.

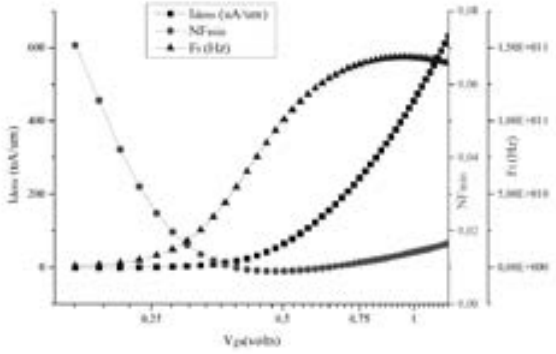

Fig. 2. Bias point optimization.

The average input-referred noise current density can be evaluated by equation 1 [3,4]:

$$\bar{I}_{n,in} = \frac{I_{n,Rx}}{\sqrt{f_{BW,S}}} \quad \left(\frac{pA}{\sqrt{Hz}}\right) \tag{1}$$

The sensitivity for a BER less than 10^{-12} can be estimated using the equation 2 [4]:

$$Sensitivity = 10\log\left\{\frac{14.1I_{n,Rx}\left(r_e+1\right)}{2\rho\left(r_e+1\right)}\times 1000\right\} \quad (2)$$

In equation 2, ρ is the photodiode responsitivity and re is the excitation ratio of the modulator.

A first fabrication run was performed to characterize the microstrip lines to be used in the TIA amplifier. Figure 3 shows the microphotograph of the shielded microstrip line. This line was designed to have a 50 Ω characteristic impedance. Figure 4 shows the S11 experimental results. S11 is bellow -20 dB up to 40 GHz.

A literature analysis showed that a common topology for the TIA circuit is the well known regulated cascode amplifier. Its main disadvantage is the high input noise current density, that reduces substantially the receiver sensitivity [5]. Based on this drawback, we proposed a double cascode amplifier optimized for low noise and high performance. Negative feedback and inductive peaking techniques were used to achieve this goal. Fig. 5 shows its basic circuit schematic and Fig. 6 the circuit microphotograph. Fig. 7 shows the S-parameters and transimpedance obtained from experimental measurements.

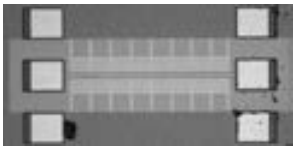

Fig. 3. 50 Ω Shielded Microtrip Line Microphotograph.

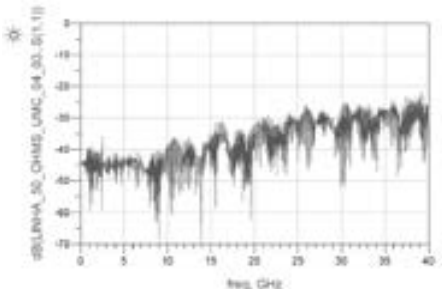

Fig. 4. Experimental S11 parameter of the Microtrip Line.

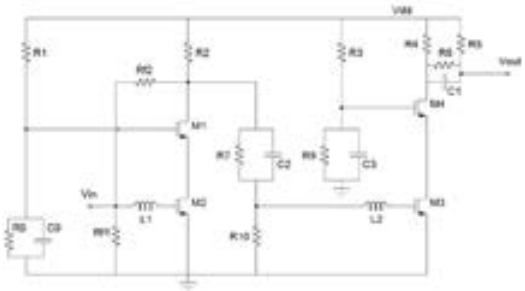

Fig. 5. Two Stage Cascode Schematics.

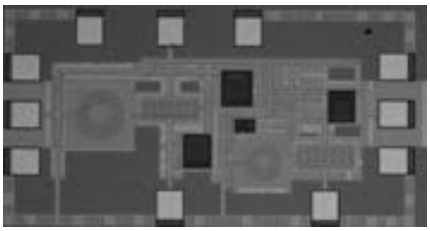

Fig. 6. Two Stage Cascode TIA Microphotograph.

The proposed double cascode circuit has an adjustable gain (S21) from 10 dB to 20 dB with different values of the bias current. Figure 8 shows the range of gain when the bias current varies from 25 mA to 50 mA. In each case, the amplifier keep the bandwidth over 7 GHz, the minimum to operate as a TIA at 10 Gbps. If we consider ρ = 0.5 A/W and re = 5 dB, equation 2 gives a sensitivity of -18.12 dBm for the double cascode TIA. This sensitivity of the proposed amplifier is the highest compared to other 10 Gbps transimpedance amplifiers reported in the literature. The second topology proposed in this work is a two stage inverter amplifier. Each stage employs negative feedback to improve de bandwidth. The proposed topology is a modified version proposed in [6]. The double inverter TIA is optimized to broadband performance, low power consumption and low noise. Figure 9 shows its basic schematic. This circuit has a 48 dB transimpedance gain, 11.2 GHz bandwidth and consumes 20.7 mW of power. It has only 0.048 mm2 of area. Figure 10 shows the post layout S-parameters for the double inverter TIA.

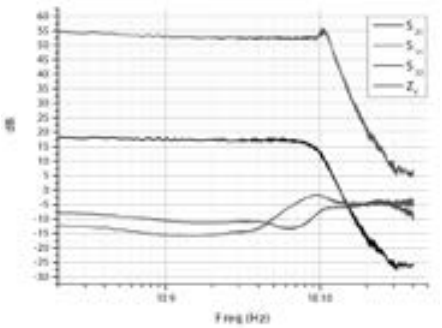

Fig. 7. Experimental S – parameters and ZT of two stage cascode.

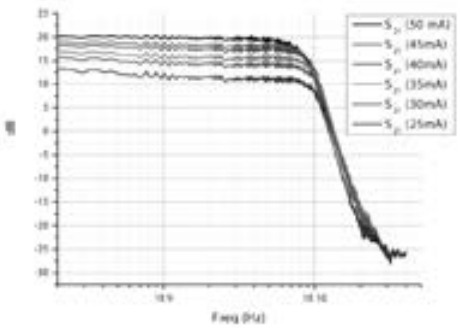

Fig. 8. Two Stage Cascode S21 for Different Bias Currents.

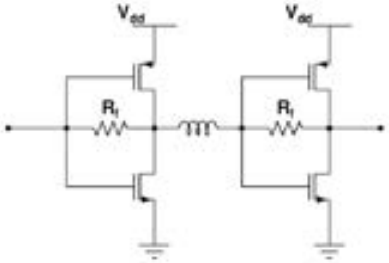

Fig. 9: Two Stage Inverter TIA Schematics.

Table 1 shows a complete comparison with other designs.

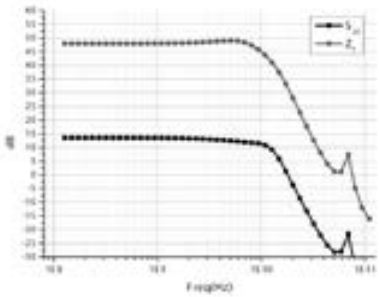

Fig. 10: Two Stage Inverter S-parameters Post-layout results.

TABLE 1. 10 GBPS TIA SUMMARY.

Ref.	[5]	[7]	[8]	[9]	[10]	This work	
	0.13 µm (C)	0.18 µm (C)	0.18 µm (C)	0.18 µm (B)	90 nm (C)	0.13 µm (C)	
Transimpedance (ΩT)	52.9	53	75	54	54	54	48
Supply (V)	1.2	1.8	1.8	2.5	1.0	1.5	
Bandwidth (GHz)	14.3	8.0	7.2	9.2	13.4	11.5	11.2
Noise (pA/$\sqrt{Hz}$)	39	33.4	19	17	28	6.8	8.9
Sens. (dBm)	-10.1	-12	-14.7	-14.6	-11.6	-18.1	-17.8
Power (mW)	2.7	35	91.8	138	2.2	45	20.7

III. MAIN AMPLIFIER DESIGN

The main function of the limiter amplifier is to improve the amplitude of this signal to a required level for the CDR circuit. The limiter amplifier core is a modified version of Cherry-Hooper amplifier [12]. The modification proposed in this work is to use an pMOS active inductor as load for the amplifier. This technique is very effective to improve the frequency response and to save chip area. Figure 11 shows the schematic of the proposed amplifier. Each stage has 8 dB gain, 13 GHz bandwidth and 13.8 mW of power consumption.

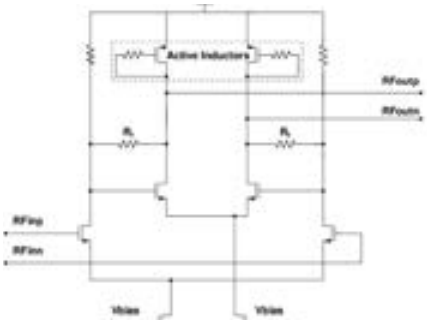

Fig. 11. Modified Cherry-Hooper Amplifier Schematics.

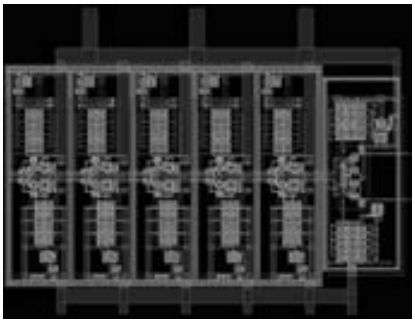

Fig. 12. Complete Limiter Amplifier Layout.

The architecture of the limiter amplifier is composed by 5 identical modified Cherry-Hooper amplifiers. The overall gain is 38 dB. The circuit has 9.8 GHz bandwidth, 69.4 mW of power consumption and occupies only 0.171 mm2 of area. This is one of the lowest power consumption and lowest area from other 10 Gbps amplifiers reported in literature. The FOM (figure of merit, expressed in Gain.BW/power units) of this circuit is 12.66. The complete limiter amplifier layout is shown in figure 12. Figure 13 shows the post-layout S21 result for the limiter amplifier.

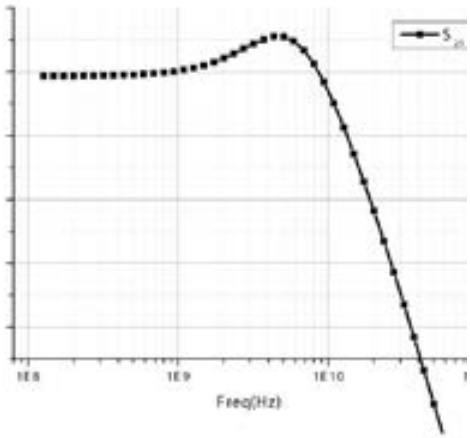

Fig. 13. Limiter Amplifier S21 parameter from Post-Layout Simulations.

Table II shows a complete comparison with other limiter amplifiers.

TABLE II: 10 GBPS LIMITER AMPLIFIER PERFORMANCE SUMMARY

Reference	[13]	[14]	[15]	[16]	[17]	This work
	40nm CMOS	180nm CMOS	180nm CMOS	180nm CMOS	180nm CMOS	130nm CMOS
Differential Gain (S_{21})	45	44.5	42	40	45.6	39
Supply (V)	1.0	1.8	1.8	1.8	1.8	1.5
Number of Stages	9	12	3	5	4	5
Bandwidth (GHz)	6.5	10.3	8.6	8.4	8.9	9.8
Power (mW)	14.4	226	72	-	165	69
Area (mm^2)	0.15	0.56	0.168	1.012	0.21	0.171
FOM (Gain.BW/mW)	80.27	7.65	15.04	-	10.4	12.66

A. Complete EO Receiver

In this section, we show two complete versions of the optical receiver. Figure 14 shows the layout of the first version. This version uses the first TIA shown in section 1 that was already fabricated and characterized. Figure 15 shows the expected performance from post-layout simulations.

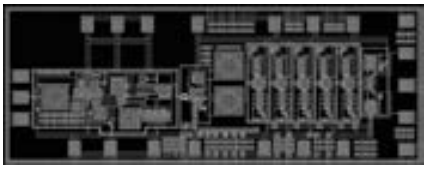

Fig. 14. Version 1 of the Complete Optical Receiver.

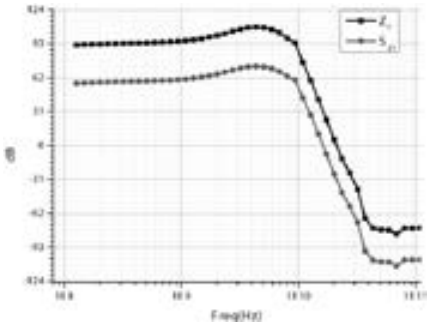

Fig. 15: Post-Layout S21 and ZT results for the Receiver 1.

The second version has the two stage inverter TIA as the first block of the complete chain. Figure 16 shows its complete layout. The expected performance from post-layout simulations is shown in figure 17.

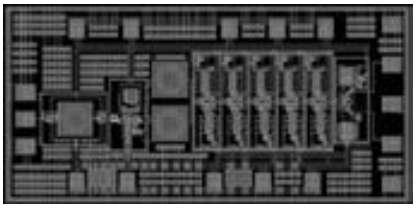

Fig. 16: Version 2 of the Complete Optical Receiver.

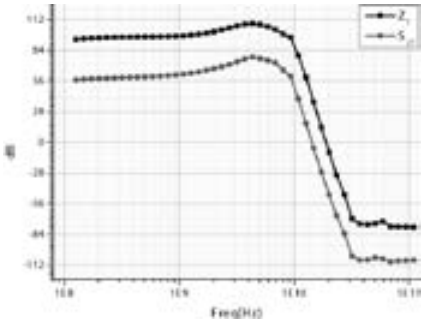

Fig. 17: Post-Layout S21 and ZT results for the Receiver 2.

IV. CONCLUSION

The design and optimization of two complete optical receivers have been described in this work. Both receivers were optimized for high gain and lonoise performance. The proposed optical receivers have higher sensitivity, lower area and lower power consumption compared to other designs reported in literature. Since the TIA is the first block of the receiver chain, the design must be optimized to very low noise. The two versions have the lowest input noise current density compared to other 10 Gbps transimpedance amplifiers.

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