Charge Balance Circuit for Constant Current Neural Stimulation with Less than 8 nC Residual Charge

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***Abstract*— Charge balancing is a major concern in functional electrical stimulation. Any excess charge accumulation over time leads to electrolysis with the electrode dissolution and tissue destruction. Therefore, charge balance circuits are used for mitigating the effects of charge accumulation in tissues. This work introduces an active synchronous charge balance circuit for constant current neural stimulators that operates without requiring negative supply for remaining charge detection. The charge balance circuit detects the residual charge by monitoring the electrode voltages just before the stimulation. If the voltage difference between the electrodes is above a certain threshold, a balance current is generated to achieve net zero charge at the electrode. Balancing current and the main stimulation current are injected simultaneously, preventing any interference in other electrodes. The charge balance circuit is dynamically disabled to reduce the system power when the charge detection is not active. The circuit can operate for the stimulation currents up to 1.4 mA and hold the electrode charge under 8 nC/phase while consuming only 6.36 µW power.**

Keywords—Charge Balance Circuit, Current Mode Neural Stimulation, FES

I. Introduction

Functional electrical stimulation (FES) is one of the most widely used techniques in biomedical engineering. FES enables stimulation of the nerves with electrical signals. Cochlear implants and retinal prostheses are the notable products of the FES technology which help to recover hearing and vision, respectively [1] [2] .

Switched-capacitor stimulation (SCS), voltage-controlled stimulation (VCS) and constant current stimulation (CCS) are the commonly used implementation methods for FES. VCS is the most efficient method among the three; however, the injected charge is not controllable as it depends on tissue impedance. Although SCS technique can control the amount of transferred charge, it comes with large area overheads due to the utilized capacitors. With its high injected charge controllability and relatively small area, CCS is the most preferred technique for FES applications [3].

In CCS, a biphasic current pulse is applied to the neurons. The procedure consists of two cycles: In the source cycle, the charge is injected to the tissue. In the sink cycle, the tissue is discharged by changing the direction of the applied current. The microelectronic process non-idealities and mismatches may lead to nonzero net charge which is harmful for the tissues and the nerves. The typical mismatch between sink and source cycles can be around 1-2%, which is above the safety region for tissue destruction [4]. The acceptable charge value for a cochlear implant is around 15 nC/phase or 100 nA DC current error between sink and source cycle [5].

Charge balance circuits which can be passive or active are used to keep the net charge after stimulation in safe limits. The blocking capacitor [6] [7] and the electrode shorting [8] methods are the most widely used passive charge balance techniques. These techniques suffer from either huge area requirement due to large blocking capacitors or being harmful to tissues because of the high current ratings. Active charge balance technique on the other hand, limits the current rating at a smaller chip area. Active charge balancing can be done by a high precision current source/sink [4], by measuring charge error [9], or by using bridge networks [6]. Active charge balance circuits should operate synchronously for multi-channel and continuous stimulation to prevent interference between electrodes.

In this work, an active charge balance circuit for a positive supply CCS is proposed in order to minimize charge accumulation with low power consumption and small chip area. The charge balance circuit monitors the electrode voltages and applies the synchronous balancing current without disturbing the stimulation. The organization of this paper is as follows: The proposed circuit design is briefly described in Section II. Section III presents charge balance circuit test results. Finally, conclusions are summarized in Section IV.

II. Circuit Description

Fig. 1 shows block diagram of the proposed charge balance circuit. The circuit observes the electrode voltage before the stimulation and arranges the stimulation current with respect to the voltage difference between the electrodes to get zero net charge. By observing the electrode voltage difference, the capacitor charge and its sign can be measured. If the electrode voltage is higher than the common electrode voltage, the generated current is activated in source cycle. If the voltage is lower, generated current is activated in sink cycle. Amplitude of the generated current is proportional to the voltage difference. Synchronous operation ensures that the main stimulation timing and current shape are not affected by the charge balance circuit.

The circuit contains three main parts (Fig. 1). The sensing part is used for sampling the voltages on the electrodes.

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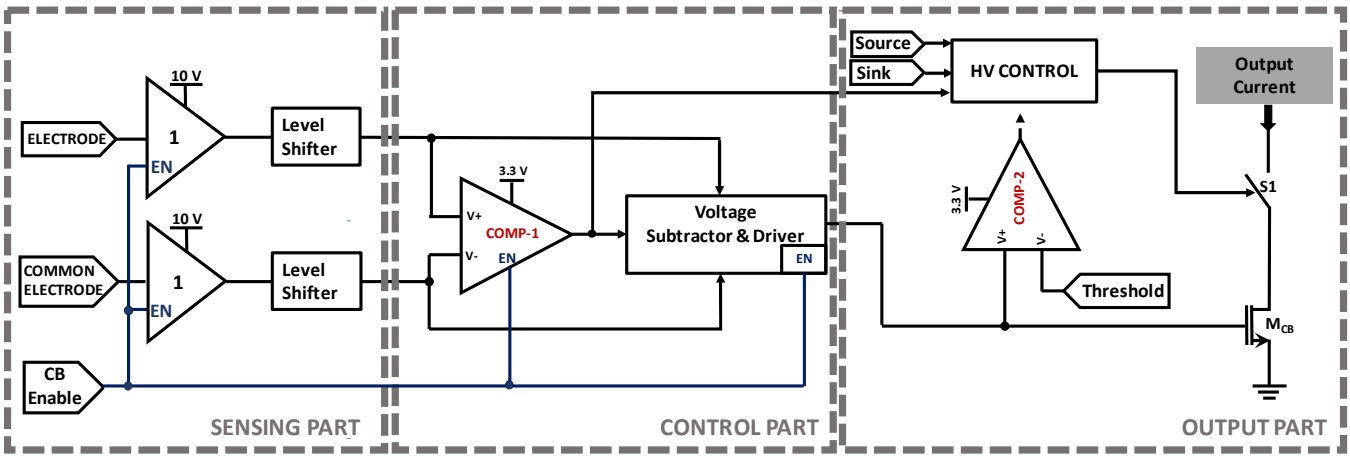

Fig. 1. Charge balance system architecture and die micrograph.

Electrode node voltages vary from 0 to 10 V in accordance with the stimulation current level. The input buffers must be suitable for the rail to rail operation to capture the wide range electrode voltage variation. Therefore, the buffers are designed with folded cascode structure. At the output of the buffers, level shifters are used to decrease the voltage level lower than 3.3 V since the rest of the circuit is designed with 3.3 V supply for minimizing power consumption. Level shifters consist of two series resistors that divide the output by three.

The control part consists of a comparator, a driver and a voltage subtractor circuit. The comparator and driver circuits are utilized for arranging the voltage subtractor inputs since the voltage subtractor circuit is not suitable for subtracting high voltage from low voltage. The comparator "COMP-1" determines the higher input and the driver circuit arrange the voltage subtractor inputs according to the output of the comparator using CMOS pass logic gates.

The output part is used for generating the stimulation current. Without the comparator "COMP-2", the circuit always generates current even if the voltages of electrode nodes are

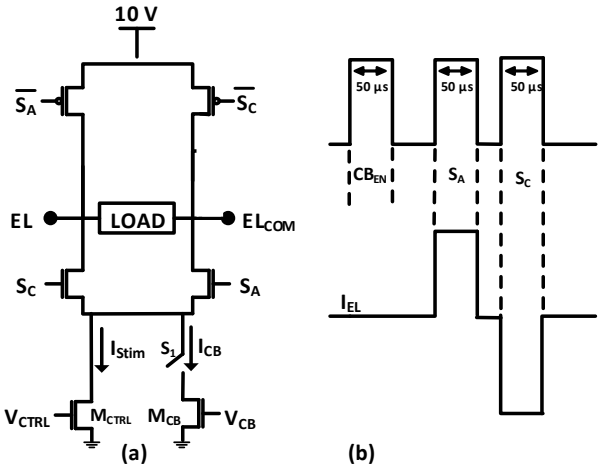

Fig. 2. (a) Single supply CCS circuit (b) control signals and generated biphasic stimulation current.

equal. However, with the help of "COMP-2", a threshold can be set for stimulation. High Voltage Control Block determines when the stimulation occurs. The operation principle of this block is as follows: If the "Common Electrode (ELCOM)" voltage is higher than "Electrode (EL)" voltage, the output current should be operated at the sink cycle. If it is not, the output current should be operated at the source cycle. Operation cycles are determined with "S_A (sink)" and "S_C (source)" inputs. The M_{CB} transistor is used to control the current level of the charge balance circuit.

The power consumption of the circuit is further decreased by operating, sensing and control parts only when the charge balance enable signal is high. The output part operates while sink or source signal is high. When the charge balance enable signal is ended, the voltage subtractor and the comparator (COMP-1) outputs are stored in a 2 pF internal capacitor. For the stimulation circuit, a single positive supply constant current source is used which consists of four switches (Fig. 2). The anodic pulse is provided through S_A and $\overline{S_A}$, whereas the cathodic pulse is supplied by S_C and $\overline{S_C}$. The stimulation current level is controlled by the gate voltage (V_{CTRL}) of the n-MOS transistor (M_{CTRL}). In the sink period, the current direction is arranged from EL_{COM} to EL by turning on S_C switches. In the source period, the current direction is reversed by turning on S_A switches while turning off S_C switches. The voltage subtractor circuit is the most challenging part of the design because it should provide the same output voltage for the constant difference value for any electrode voltage level. Fig. 3 shows the schematic diagram of the subtractor circuit. The input voltages are applied to the gate of the p-MOS transistors (M_1 & M_2) that provide the input common mode range close to low voltages. Sources of these transistors are connected to the active load transistors M_4 and M_5, which are biased through bias generator part. The gate voltages of M_4 and M_5 are calibrated according to size of the bias generator transistors, where for the input voltages close to zero the current mirrors go to the edge of saturation. When the input voltage increases, the current mirrors goes to the linear region and current of the input transistors become reversely proportional with the input voltage. The

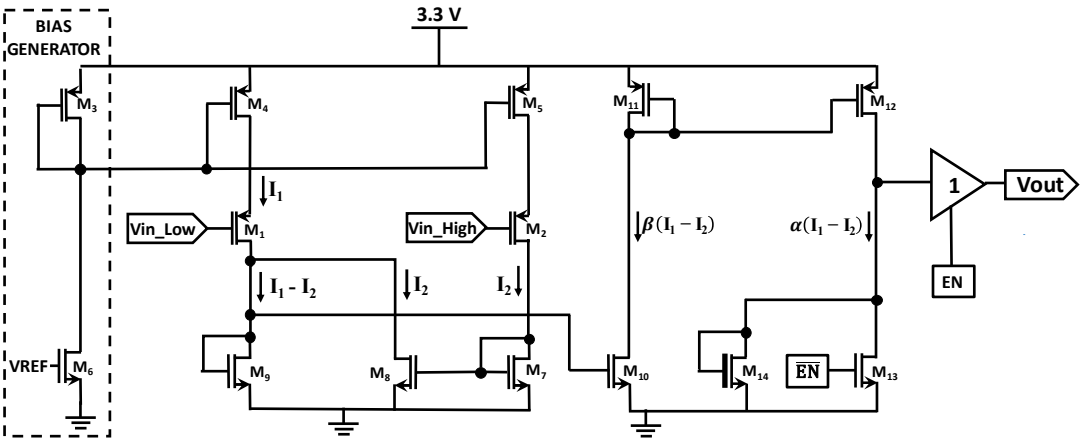

Fig. 3 The voltage subtractor circuit.

current of the M_2 is subtracted from the current of M_1 and the difference is applied to M_9. The subtracted current is amplified by M_{10} and M_{12}, and converted to the voltage by a high voltage transistor (M_{14}). The voltage on M_{14} is buffered with an op-amp and sample with the charge balance enable signal. The sampled voltage is connected to the gate of M_{CB} (Fig. 1) and thus charge balance current is generated.

III. Test Results

The proposed charge balance circuit was implemented in 180nm high-voltage CMOS technology. Die micrograph of the implemented charge balance circuit is represented in Fig 4 where the active area of the charge balance circuit occupies 540 µm x 160 µm.

The implemented chip is tested for various stimulation current levels where electrical model of the electrode tissue interface composed of series resistor (2 kΩ) and capacitor (100 nF) [10]were used as the load for the neural stimulation. For a constant stimulation time and known electrode capacitor, the required charge balance current rating can be calculated with respect to voltage difference as seen in (1). Therefore, the ratio between the charge balance current and the voltage difference can be calculated as 2 µA/mV for 50 µs stimulation time. Fig. 5 gives variation of the charge balance current with respect to the electrode voltage difference where slope of the curves is around 2 µA/mV for voltage difference between 1 mV to 15 mV. For higher voltage differences the charge balance current is saturated which prevents the instability at the circuit performance. Although the electrode voltages increase with increasing stimulation current level, the circuit operates linearly with regardless of the electrode voltage levels.

$$Q = C.\Delta V = I.\Delta t, \qquad \frac{I}{\Delta V} = \frac{C}{\Delta t} \tag{1}$$

Fig. 6 shows the stimulation currents integrals (charge) for different constant stimulation currents respect to time. For the test, the stimulation interval was set to 1 ms and charge balance enable, sink and source signals durations were set to the 50 µs which is the phase width of the anodic and cathodic stimulation pulses. Stimulation currents are changed from 500 µA to 1.4 mA. Without charge balance circuit, the electrode residual charge decreases with increased current because the effect of the charge injection is decreased. The residual electrode charges are decreased with charge balance circuit.

Fig. 7 shows the maximum absolute residual charge of the electrode after ten-cycle of stimulation. Without charge balance circuit, the residual charge reaches up to 80 nC at 500 µA stimulation current. It decreases with the increasing stimulation current since stimulator is less sensible to switch variations at high currents. With charge balance circuit, the maximum allowable residual charge is 8 nC which is lower than permitted safety limits (15 nC/phase).

The charge balance circuits input buffers and switch matrix were operated with 10 V and the rest of the circuit were operated

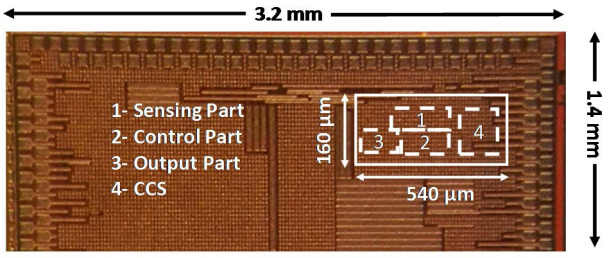

Fig. 4 Die micrograph of the charge balance circuit

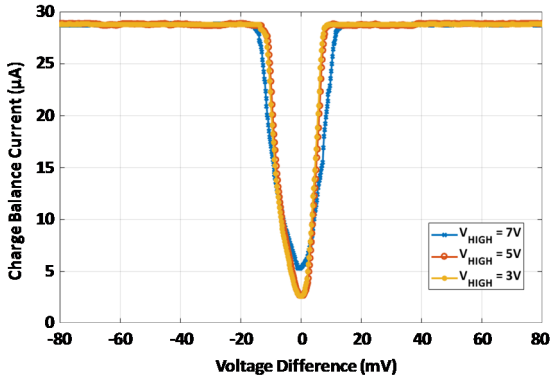

Fig. 5 Measured DC output characteristic of charge balance circuit.

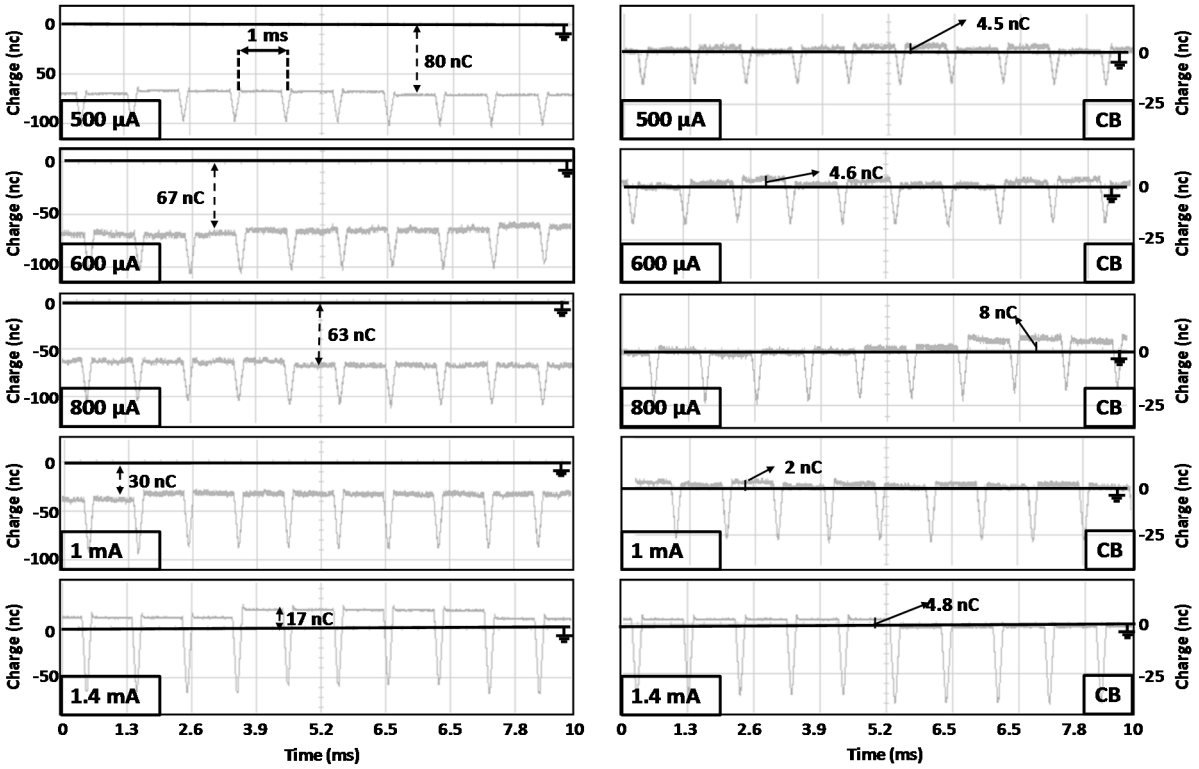

Fig. 6: Variation of the electrode residual charge with respect to time for different constant stimulation current values, left column is without charge balance circuit where right column is with the charge balance circuit.

with 3.3 V supplies. The charge balance circuit consumes low power due to its operation cycle. The total power consumption is 6.36 µW (from 10 V supply is 2.47 µW and from 3.3 V supply is 3.89 µW) which is obtained by clock gating the charge balance circuit with enable signal for 50 µs in 1 ms stimulation period. Moreover, the circuit provides small chip area since it does not use any large blocking capacitor. Due to its small size and ultra-low power consumption the chip is suitable for the implantable neural stimulators. Table I summarizes the performance comparison of the charge balance circuits. The proposed design has the lowest power consumption with a controllable safety window. The presented circuit uses synchronous charge balance technique, which enables the multichannel operation.

IV. CONCLUSION

In this paper, an active charge balance circuit, which observes the electrode voltage and generates charge balance current, has been presented. The generated current balances the electrode charge at the next cycle. This prevents any disturbance in the stimulation, and enables multi-channel operation with proper timing, which will be investigated in a future work. The proposed circuit provides stimulation currents up to 1.4 mA with maximum residual electrode charge of 8 nC. The power dissipation of the charge balance circuit is 6.36 µW.

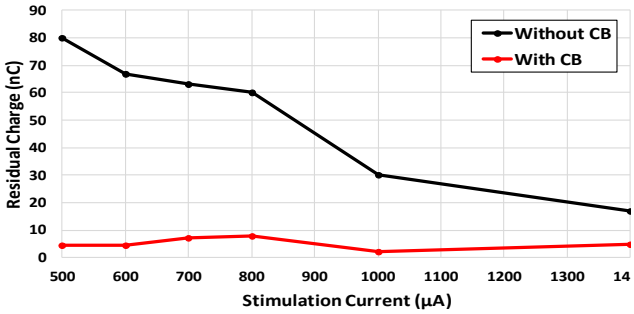

Fig. 7: Variation of the residual charge with the stimulation current.

ACKNOWLEDGMENTS

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TABLE I. COMPARISION WITH OTHER CHARGE BALANCE CIRCUITS

Reference	[11]	[4]	[9]	[7]	This Work
Process	0.35 µm	0.7µm	PCB	0.35 µm	0.18 µm
Electrode Voltage Compliance	22 V	15 V	30 V	4.2V	10 V
Safety Window	<0.1 V	<6nA	<0.1 V	N/A	<20 mV
CB Method	IPCC	DCB	SPI	CM and BC	SCB
Precision	<20 mV	<0.4%	<0.1 V	<22 mV	<12 mV(1)
Power (µW)	56	47	N/A	N/A	6.36

IPCC: Inter-Pulse Charge Control, DCB: Dynamic Current Balancing, SPI: Short Pulse Injection, CM: Charge Monitoring, BC: Blocking Capacitor (Passive), SCB: Synchronous Charge Balance.
(1)Calculated from 100 nF capacitance

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