An Adaptable Interface Circuit for Low Power MEMS Piezoelectric Energy Harvesters with Multi-Stage Energy Extraction

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***Abstract*— This paper presents a self-powered interface circuit to extract energy from ambient vibrations for powering up microelectronic devices. The system uses a MEMS piezoelectric energy harvester to scavenge power in 5 µW to 400 µW range. Synchronous electric charge extraction (SECE) technique is utilized to transfer harvested energy to output storage with the help of a novel multi-stage energy extraction (MSEE) circuit. The circuit is optimized in 180nm HV CMOS technology to operate with minimum power losses at the lowest allowable input power, and adjusts well to higher input power due to the MSEE circuit. The circuit operation was validated for a wide piezoelectric frequency range from 20 Hz to 4 kHz. Power efficiency between 62% and 81% has been achieved for the input power range of 5 µW to 173 µW at 198 Hz input vibration. MSEE provides up to 15% efficiency improvement compared to traditional SECE to keep power efficiency as high as possible for the full input power range.**

Keywords—Self-powered, vibration, piezoelectric energy harvester, IC, MSEE, power efficiency.

I. INTRODUCTION

Energy harvesting is developing into a leading technology as the number of machine-to-machine (M2M) interfaces increase exponentially. Piezoelectric energy harvester (PEH) has recently attracted interest as a solution for self-powered microelectronic devices such as fully implanted cochlear implants, micro-devices and wireless sensor networks (WSNs), since piezoelectric transducers provide higher power density than their electrostatic and electromagnetic counterparts [1]. PEHs can supply power from µW to mW, using ambient vibrations. For example, a MEMS piezoelectric harvester has been utilized to generate rms output power range up to 160 µW under different vibration levels [2].

PEHs supply AC power with significant output impedance; consequently, an interface circuit (IC) is required to efficiently extract and convert piezoelectric AC voltage to usable DC voltage. Besides standard rectifying techniques [3-4], switching approaches based on non-linear processing of the voltage across PEH are used to enhance the extracted power. Synchronous electric charge extraction (SECE) [5] is an efficient approach among switching techniques for facilitating charge delivery and achieving load matching at the same time. The main challenge in switching approaches is extracting maximum power for a wide input power and frequency range. In SECE technique, energy extraction and transfer in several successive charge packages enables reduction in the size of off-chip electromagnetic components and increased power efficiency [6]. The circuit implemented in [6] is efficient only for mechanical frequency range below 50Hz, and depends on digital inputs for establishing critical time constants related to input piezoelectric clamped capacitance and output load capacitance, to determine extraction and transfer durations. Therefore, this IC is not applicable for MEMS harvesters and implantable micro-devices. Unlike previous studies, the IC presented here is optimized through a novel multi-stage energy extraction circuit for efficient operation across a wide input power and frequency range. In the following section, the approach and implemented circuit are described in detail. Section III summarizes test setup and experimental results. Finally, the paper is concluded in Section IV.

II. INTERFACE CIRCUIT DESIGN

A. Operation Principle

The proposed circuit comprises of three stages including a Negative Level Shifter (NLS), active extraction circuit, and energy storage with start-up circuit as shown in Fig. 1. The NLS provides only positive voltage by shifting negative voltage peak to zero, like an active diode. The storage capacitor, $C_{Storage}$, is first charged by the piezoelectric harvester through a diode and a control switch at wake-up. The startup circuit decouples the supply voltage of the control unit (V_{DD}) and storage voltage (V_{stor}) as long as $V_{stor}<V_{trig}$, and powers up the active components in the control unit using the storage voltage ($V_{DD}=V_{stor}$) when $V_{stor}>V_{trig}$. The power extraction stage is designed based on synchronous electric charge extraction (SECE) technique. Active power extraction is realized through four phases managed by switch control circuitry as shown in Fig. 2. In the first phase, all switches in Fig. 1 are turned OFF to bias the PEH at open circuit condition until its output peaks. After peak detection, energy stored on the PEH clamped capacitor is transferred to the inductor through Cp-L resonant circuit by turning ON S_1 and S_3. The third phase is entered when PEH voltage reduces to zero. At this point, S_1 and S_3 are turned OFF, S_2 and S_4 switches are ON, and the stored energy on the inductor is transferred to the storage capacitor, C_S. Charging of the capacitor continues until the inductor current reaches zero.

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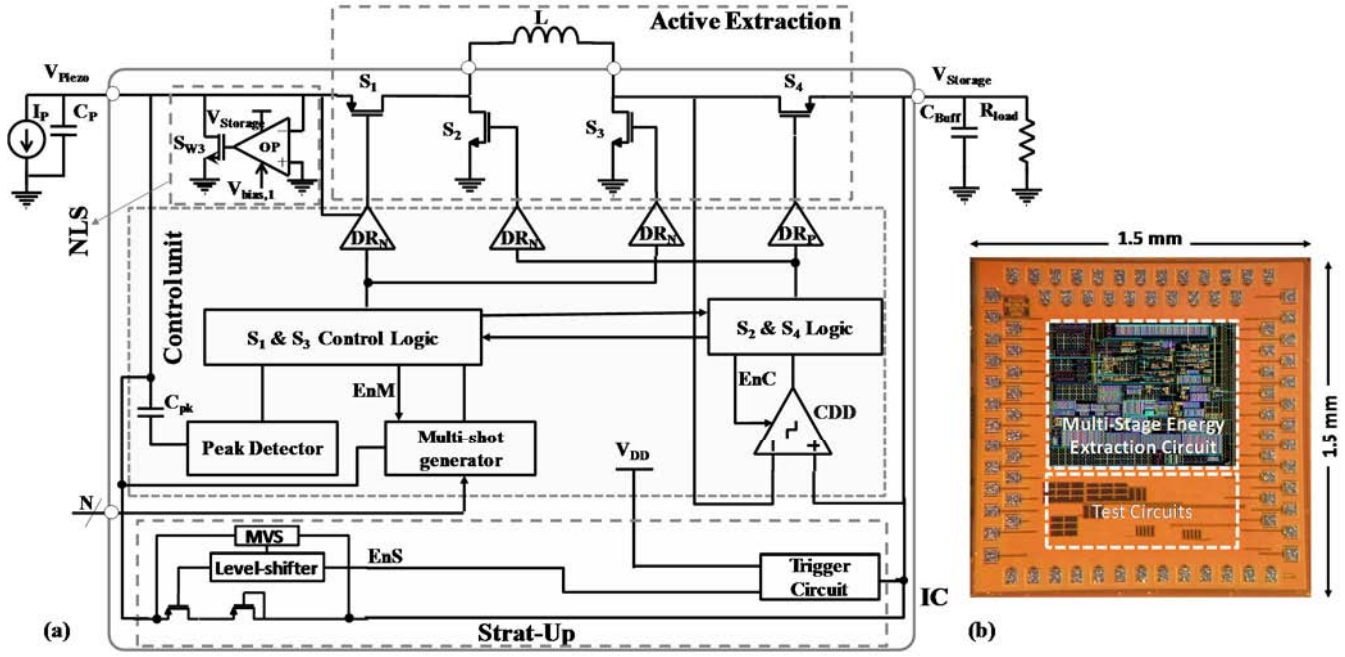


Fig. 1. (a) System architecture of the integrated PEH interface circuit, and (b) Die micrograph of implemented interface circuit.

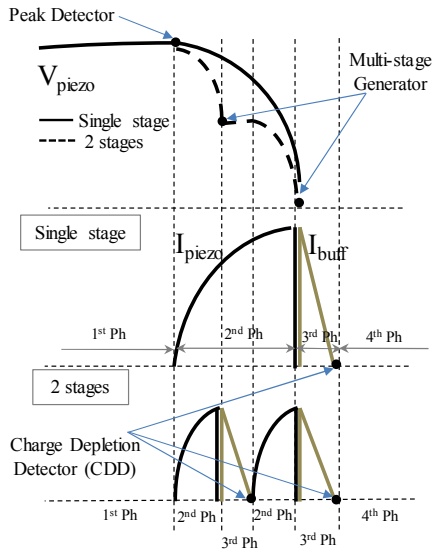


Fig. 2 Extraction phases and critical switching points of the SECE in time domain for single and two-stage transfers.

The fourth phase starts by turning switches OFF, and entering NLS mode. The circuit goes back to the first phase, and starts a new cycle by turning OFF S_{W3} when PEH voltage is positive. In the case of the multi-stage extraction, the second and third phases are repeated in sequence according to the defined stage number, N, as shown in Fig. 2.

B. Power Optimization

There are four sources of power dissipation in the switching circuit: Resistive conduction losses in the inductors and MOSFET switches; charge redistribution losses at MOSFET parasitic capacitances during phase changes, capacitive switching losses at the gates of power switches, and leakage current associated with any MOSFET in OFF state. After thorough investigation of losses, within 180nm HV CMOS, the power switch (S_1-S_4) sizes have been optimized as W=4 mm for a minimum power loss of 1.7 µW at the lowest allowable PEH voltage. This optimization improves power efficiency for the low input power scenario, and controls the efficiency of the higher input power levels through multistage energy extraction.

The charge on the piezoelectric harvester is delivered in N successive energy packages in highly charged cases to constrain switching current on inductor, as shown in Fig. 2. The presented multistage extraction has been designed to transfer the harvested energy over a relatively low-profile inductor (100 µH-3.3 mH).

C. Control unit

Peak detector, multi-stage generator, and charge depletion detector (CDD) in the control unit sequence the switch drivers according to the phases described in the previous section, in order to realize the multi-stage synchronous charge extraction.

1) Peak Detector: The proposed peak detector, shown in Fig. 3, is designed to operate at PEH voltages higher than supply voltage, V_{DD}. The circuit operates in current mode with internal negative feed-back. The input voltage is converted to a current, I_S, by a series capacitor, C_{PK}. Node X is charged until its voltage exceeds M_{N0} MOSFET threshold due to negative feed-back action on M_{N0} and M_{P0}. As PEH voltage peaks, I_S reduces to zero, and consequently voltage drop over M_{P0} causes M_{N0} to turn OFF. As M_{N0} is turned OFF, the gate of common source amplifier goes high by mirroring reference current through the node. Digital inverters in the output stage deliver a high edge rate. Upper limit of the input frequency determines the reference current value, while the minimum detectable amplitude determines the value of the series capacitor, C_{PK}.

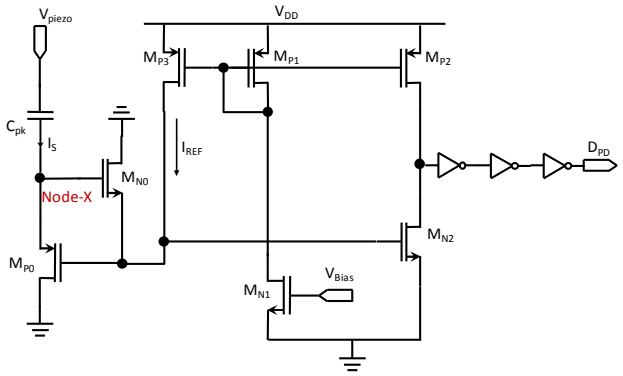
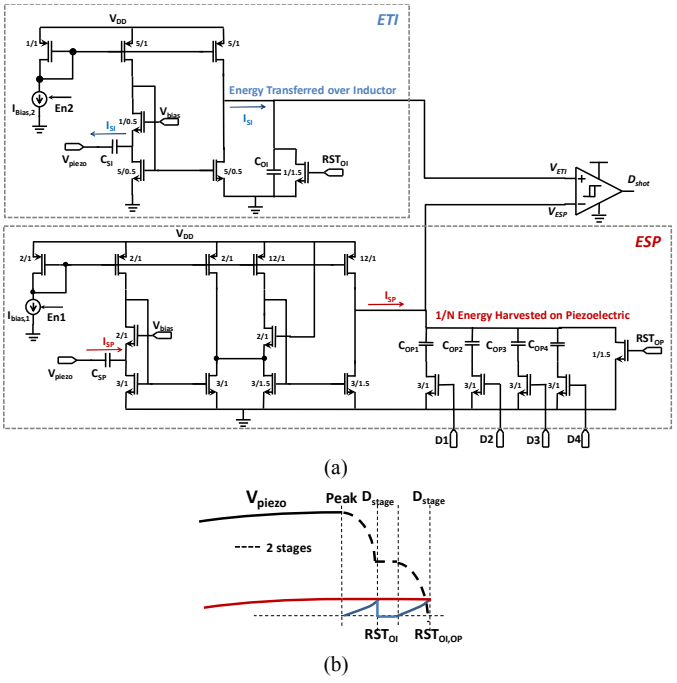


Fig. 3. Schematic of the implemented Peak Detector.

2) Multi-stage generator circuit: The multi-stage generator, depicted in Fig. 4(a), relies on energy drain without any calibration requirement. The *energy stored in piezoelectric* (ESP) capacitor is measured in the first phase, and regenerated over C_{OP} capacitor with voltage downscaling. The number of extraction steps (N) is determined by the capacitors connected in parallel to divide stored energy by N. When PEH voltage peaks in the second phase, ESP circuit is disabled in order to hold the measured voltage. As the IC enters the second phase, energy transferred to the inductor is measured through *energy transferred on inductor* (ETI) circuit, and is compared with ESP through hysteresis comparator to determine the end of energy extraction. Multi-stage output signal initiates energy transfer to buffer capacitance in the third phase, and C_{OI} is reset for next extraction. The operation principle and related signals are illustrated in Fig. 4(b). The number of extraction stages is controlled through $D_{1\text{-}4}$, generated from 2 digital bits (labeled N in Fig. 1) and a decoder.



(a)

(b)

Fig. 4. (a) Implemented Multi-stage generator: (b) Operation principle and related signals.

3) Charge depletion detector (CDD): Depletion of stored energy in the inductor to storage capacitance is controlled by a charge-depletion comparator with a relatively high bandwidth. The comparator monitors the voltage across S_4 switch to detect the end of inductor discharging. The CDD is only activated in the fourth phase to save the power.

III. Experimental Results

The maximum operation frequency of the MSEE is determined by the Peak detector. A delay in detecting peak instant may cause significant energy loss as the energy transfer is initiated at lower piezoelectric voltage. The accuracy of implemented peak detector has thus been experimentally evaluated as a function of the input frequency. The difference between actual peak and detected peak value has been illustrated in Fig. 5 up to 4,000 Hz, which is the maximum design frequency of the MSEE circuit. Peak point is detected with less than 12 mV difference for excitation frequency range of 20 to 4,000 Hz with reference current of 50 nA. High accuracy of the peak detector lessens degradation of the power efficiency due to peak detection latency. Beyond 4,000 Hz, the peak instant is detected late. The peak point can be detected with higher precision and operation frequency range can be extended by increasing the reference current.

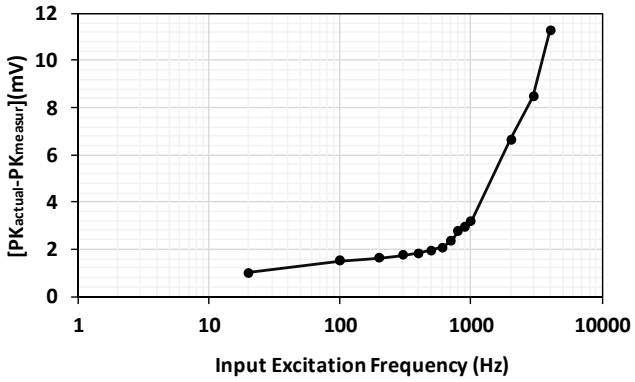


Fig. 5. The accuracy of the peak detector vs. input excitation frequency with input peak voltage of 4.5 V; the accuracy is defined as difference between actual peak (PK_{actual}) and measured peak (PK_{measur}).

The performance of the interface circuit has been measured with an MEMs piezoelectric harvester with C_P=4 nF attached to a shaker table . An inductor (L=3.3 mH/8.97 Ω) is connected to the chip to charge a 2.2 µF storage capacitance in parallel with a variable load resistance. Minimum piezoelectric peak voltage of 700 mV is required for operating start-up of the circuit. Fig. 6 represents operation of the circuit for an excitation frequency of 198 Hz with 14.4 µW input power, and 470 kΩ load resistance. The storage capacitance is initially charged through the start-up circuit. Then energy is extracted from PEH in three-stages (N=3). The voltage waveform during charging the storage capacitor in three stages is shown in Fig. 6. Fig. 7 illustrates measured piezoelectric voltage and inductor current waveforms when different number of stages are used in the circuit. The magnitude of the current passing through inductor and switches is divided by the square-root of the number of stages. Consequently, conduction power loss is decreased with the current reduction. Fig. 8 depicts power-conversion efficiency of

the circuit ($\eta=P_{OUT}/P_{IN}$) as a function of the piezoelectric open-circuit voltage. The input power is obtained through measured input voltage and current of the harvester connected to the proposed circuit. The power efficiency is calculated as ratio of average power delivered to the storage over average input power:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{\frac{1}{T}\int V_{stor}^2/R_{load}.dt}{\frac{1}{T}\int V_{piezo}.I_{piezo}.dt} \quad (1)$$

It is expected that multi-stage power extraction will improve power efficiency with increasing input power. The maximum power efficiency was measured at 81.2%. As it stands, the optimum stage number can be determined through input power or corresponding open circuit piezoelectric voltage. The stage number, N can be adjusted automatically through input power measurement at the end of the first phase of the extraction. The power efficiency can consequently be maximized for all input power levels in an autonomous manner.

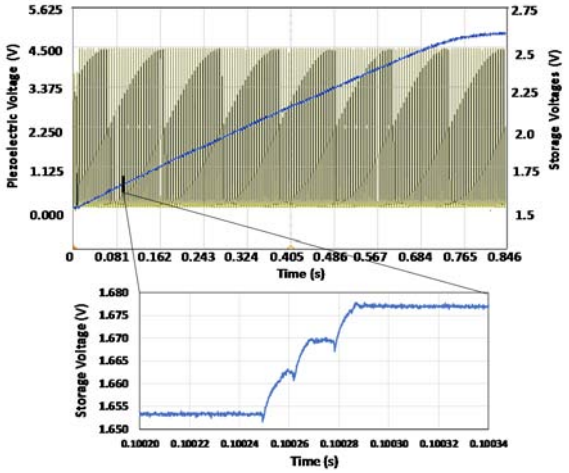


Fig. 6. Measured input-output waveforms during multi-stage extraction (N=3).

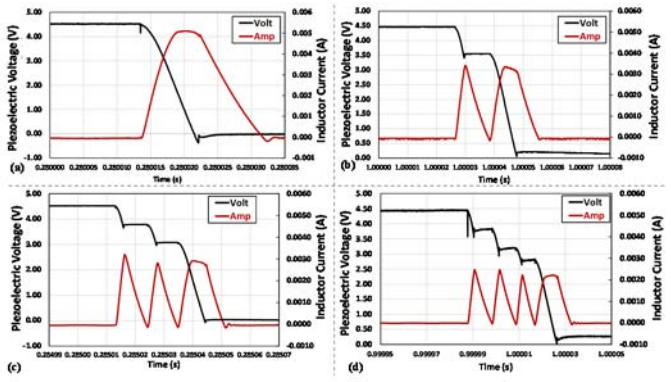


Fig. 7. Experimental piezoelectric voltage and inductor current waveforms using the multi-stages method: (a) Single stage, (b) two stages, (c) three stages, (d) four stages.

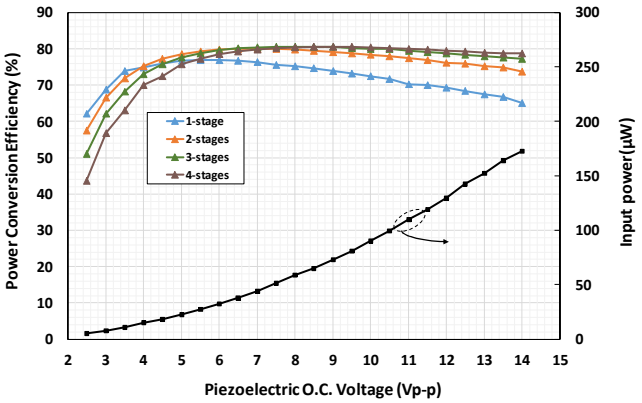


Fig. 8. Experimental power-conversion efficiency of the IC for four different stage numbers vs. Piezoelectric O.C. voltage and corresponding extracted power.

IV. Conclusion

An autonomous CMOS interface circuit has been designed and fabricated for efficient utilization of PEH resources. A novel multi-stage energy extraction circuit has been presented to enhance the adaptability of the circuit to the input power range. The performance of the IC has been experimentally evaluated. The circuit provides accurate peak detection up to 4 kHz. The power efficiency of the IC is kept above 62% for a minimum input power of 5µW, while the maximum efficiency is recorded as 81.2%. Most of the applications encompass periodic and semi-periodic vibrations. Nevertheless, randomness of an environmental energy is a great challenge in energy harvesting devices. The presented PEH interface IC delivers the means to supply power to the microelectronic devices more efficiently, regardless of the variation in the available PEH energy.

Acknowledgment

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