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Efficient, High Power Density, Modular Wide Band-gap Based Converters for Medium Voltage Application

Hadi Moradisizkoohi
Florida International University, hmora041@fiu.edu

FLORIDA INTERNATIONAL UNIVERSITY

Miami, Florida

EFFICIENT, HIGH POWER DENSITY, MODULAR WIDE BAND-GAP BASED CONVERTERS FOR MEDIUM VOLTAGE APPLICATION

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by

Hadi Moradisizkoohi

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To: Dean John Volakis
College of Engineering and Computing

This dissertation, written by Hadi Moradisizkoohi, and entitled Efficient, High Power Density, Modular Wide Band-Gap Based Converters for Medium Voltage Application, having been approved in respect to style and intellectual contents, is referred to you for judgment.

We have read this dissertation and recommend that it be approved.

Sakhrat Khizroev

Mohammed Hadi

Raj Pulugurtha

Osama A. Mohammed, Major Professor

Date of Defense: November 12, 2020

The dissertation of Hadi Moradisizkoohi is approved.

Dean John Volakis
College of Engineering and Computing

Andrés G. Gil
Vice President for Research and Economic Development
and Dean of the University Graduate School

Florida International University, 2020

DEDICATION

This dissertation is dedicated to My Parents, who instilled in me the virtues of perseverance and commitment and relentlessly encouraged me to strive for excellence.

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ABSTRACT OF THE DISSERTATION

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Miami, Florida, USA

Professor Osama A. Mohammed, Major Professor

Recent advances in semiconductor technology have accelerated developments in medium-voltage direct-current (MVDC) power system transmission and distribution. A DC-DC converter is widely considered to be the most important technology for future DC networks. Wide band-gap (WBG) power devices (i.e. Silicon Carbide (SiC) and Gallium Nitride (GaN) devices) have paved the way for improving the efficiency and power density of power converters by means of higher switching frequencies with lower conduction and switching losses compared to their Silicon (Si) counterparts. However, due to rapid variation of the voltage and current, di/dt and dv/dt, to fully utilize the advantages of the Wide-bandgap semiconductors, more focus is needed to design the printed circuit boards (PCB) in terms of minimizing the parasitic components, which impacts efficiency.

The aim of this dissertation is to study the technical challenges associated with the implementation of WBG devices and propose different power converter topologies for MVDC applications. Ship power system with MVDC distribution is attracting widespread interest due to higher reliability and reduced fuel consumption. Also, since the charging time is a barrier for adopting the electric vehicles, increasing the voltage level of the dc bus

to achieve the fast charging is considered to be the most important solution to address this concern. Moreover, raising the voltage level reduces the size and cost of cables in the car. Employing MVDC system in the power grid offers secure, flexible and efficient power flow.

It is shown that to reach optimal performance in terms of low package inductance and high slew rate of switches, designing a PCB with low common source inductance, power loop inductance, and gate-driver loop are essential. Compared with traditional power converters, the proposed circuits can reduce the voltage stress on switches and diodes, as well as the input current ripple. A lower voltage stress allows the designer to employ the switches and diodes with lower on-resistance $R_{DS(ON)}$ and forward voltage drop, respectively. Consequently, more efficient power conversion system can be achieved. Moreover, the proposed converters offer a high voltage gain that helps the power switches with smaller duty-cycle, which leads to lower current and voltage stress across them. To verify the proposed concept and prove the correctness of the theoretical analysis, the laboratory prototype of the converters using WBG devices were implemented. The proposed converters can provide energy conversion with an efficiency of 97% feeding the nominal load, which is 2% more than the efficiency of the-state-of-the-art converters. Besides the efficiency, shrinking the current ripple leads to 50% size reduction of the input filter inductors.

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PV	Photovoltaic
EV	Electric Vehicle
MV	Medium Voltage
LV	Low Voltage
HCC	Hysteresis Current Controller
MF	Medium Frequency
HF	High Frequency
CHF	Cascaded High Frequency
ESS	Energy Storage System
MPPT	Maximum Power Point Tracker
RMS	Root Mean Square
C_{dc}	Capacitor connected to the LV dc bus
V_{DC}	Voltage of the LV dc bus of the station
GaN	Gallium Nitride
SiC	Silicon Carbide
Si	Silicon
SC	Switched-Capacitor
SL	Switched-Inductor

Chapter 1 Introduction

1.1 Background

There is an increasing worldwide interest in using renewable energy sources at large-scale over the past decades due to the significant environmental and economic benefits [1]-[14]. Besides, the recent developments in medium-voltage direct-current (MVDC) paved the way for economical utilization of renewable energy sources for different applications, including transportation electrification, ship power system, offshore wind farms, and so on [15]-[30]. The MVDC offers numerous merits over the conventional AC system, including:

1) A bipolar HVDC line needs only two insulated sets of conductors. Opposed to the AC lines with same power capacity, HVDC lines contribute to lower construction cost and power losses.
2) In MVDC system, the sending and receiving end frequencies are independent.
3) Power flow can be controlled thoroughly.

Interfacing between the power sources and the loads, power electronic converters are the key enabling component in the MVDC system that can provide the following advantages:

1) Mismatching the voltage level between the source bus and the load bus [31]-[35].
2) Obtaining the maximum power from a source (e.g. photovoltaic systems, wind energy turbines, fuel cells, etc.) [36]-[42].
3) offering galvanic isolation between the sources and the load [43]-[47].
4) Control the speed and torque of electric motors [47]-[50].

5) Supporting the voltage and frequency during voltage sags and contingencies, respectively, by regulating the injected active and reactive power to the grid [50]-[60].

As far as the power range is concerned, the demand for high-power power electronic converters are increasing, especially mega-watt converters. Due to the limitation in the current and voltage range of semiconductors, the power rating of an individual prototype is currently limited to 250 kW [61]-[65]. To implement a power conversion stage with higher power ratings, multiple converter modules can be interconnected in either series or parallel that paves the way for improving the power density and efficiency. Development in semiconductor devices, as well as topologies of the power converters can contribute to considerable advancements in the power rating of the system [66]-[80].

In the applications with voltage rating higher than 600V, IGBTs are among the low-cost and affordable solutions but the switches have always presented degraded performance in terms of high tail current losses at turn-off instant and slow switching speed. Since modern applications need faster switching performance to improve the total size and cost of the system, silicon-carbide (SiC) and gallium-nitride (GaN) MOSFETs seem to be a superior substitute. In the era of power semiconductor devices, wide bandgap (WBG) semiconductors provide better power efficiency, higher switching frequency, lighter weight by reducing the size of magnetic components and heat sink, lower overall cost [81]-[90]. Employing WBG is the principal contributor to the next essential step towards an energy-efficient power system. However, to fully utilize the advantages of the WBG devices, some modifications are required in the design of the converters as the gate-driver specification of WBG devices are completely different than Si-based switches. Moreover,

due to the capability to operate at higher switching frequencies, WBG-based converters need to be investigated further to develop the filter circuit for electro-magnetic interference (EMI) [91]-[100]. Also, since MVDC applications demand devices with higher rated voltage, using high voltage MOSFETs can increase the cost and power loss of system. In fact, a thick epitaxial layer is utilized in the MOSFET to customize it for high voltage uses, which increases the on-resistance. Even though paralleling the devices is considered to be a viable solution to decrease the conduction losses, due to higher input and output capacitances, it can result in slower switching performance, more gate-driving power, and more total loss. Moreover, the current rating of the high-voltage SiC-MOSFETS is limited as a junction barrier Schottky diode should be utilized in parallel with these switches because they store excessive charge when their body diode conducts [100]-[105].

In recent years, there has been an increasing amount of literature on converter topologies. There are some studies in literature that introduce deal with the structure of power converters in terms of improving the voltage gain, efficiency, and power density [106]-[120]. Some of these converters are illustrated in Figure 1.1. Investigating the main characteristics of these converters reveals that there are some differences in terms of power flow direction, i.e. unidirectional or bidirectional, soft-switching performance and galvanic isolation. There is a consensus among researchers that the dual active bridge (DAB) converter can be efficiently employed for medium-voltage, high power applications. It has conclusively been shown that DAB converter offers the power conversion with minimum voltage and current stress of the power switches, shown in Figure 1.1(a). To reduce the switching losses, a resonant tank was added so as to enhance the efficiency. In [70], a resonant switched-capacitor converter is introduced that is derived from the conventional

switched-capacitor circuit, depicted in Figure 1.1(a). The modularity of this structure gives flexibility. To increase the voltage-gain exponentially, the modular dc-dc converters can be connected in series, in which the output power can be shared among these modules [34]. A dc-link capacitor is utilized in input stage of each sub-module to ensure equal voltage sharing among the switches by regulating the capacitor voltage. This characteristic makes this topology suitable for HVDC applications. As the voltage demand of new power electronic application increases, semiconductor voltage capability must increase as well. Especially for voltage level higher than MVDC, the voltage rating of current semiconductor technology is less than the desired value; therefore, researchers have proposed some techniques, such as series connection of semiconductors or the use of multilevel converter. Moreover, the modular structure can pave the way for scaling up the voltage and power of the converter.

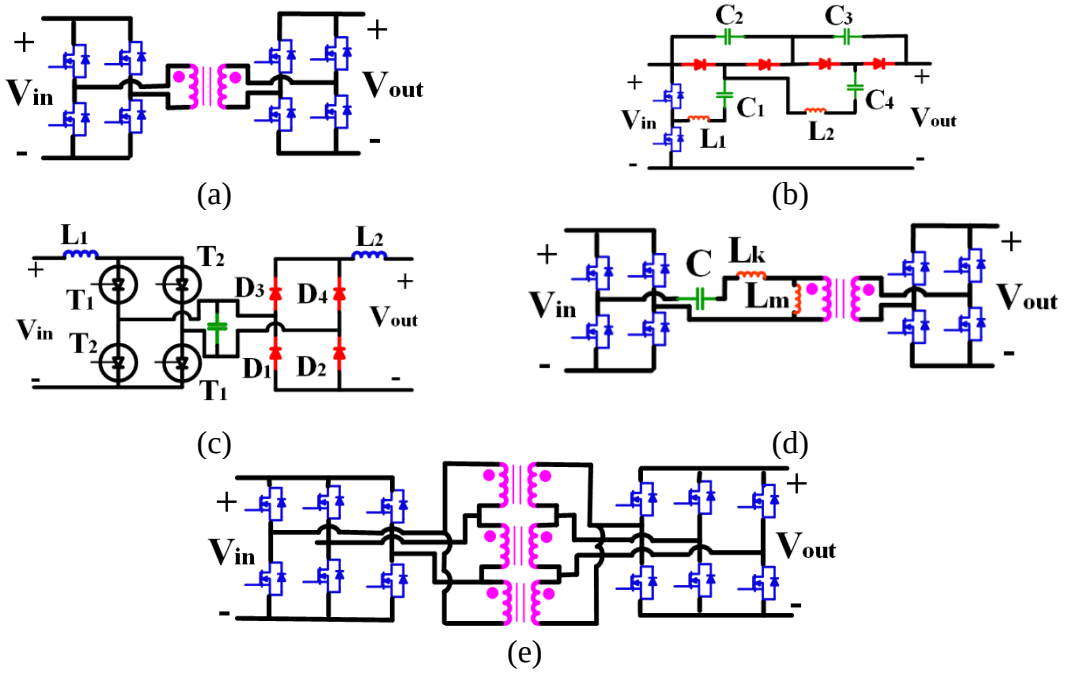


Figure 1.1: Different high step-up dc/dc converters. (a) single-phase dual active bridge (DAB1) converter. (b)Resonant switched-capacitor converter. (c) Jovcic converter. (d) LLC converter. (e) three-phase dual active bridge (DAB3) converter.

Table 1.1: Overview of different dc/dc converters for MVDC applications.

Topology	LV side (kV)	HV side (kV)	Frequency (kHz)	Rated power (MW)	Isolated	Realized	Reference
Kenzelmann-DAB1	0.075	0.225	1	0.001	Yes	Yes	[64]
DAB3	0.2	3	10	0.002	Yes	Yes	[66]
Jovcic	0.19	0.95	1.4	0.0076	No	Yes	[68]
DAB1	0.4	6.1	10	0.01	Yes	Yes	[69]
Resonant switched capacitor	0.6	10.2	7.5	0.024	No	Yes	[70]
DAB3	0.8	22	10	0.1	Yes	No	[66]
LLC	3.3	6.5	10	0.1	Yes	Yes	[72]
M2DC	0.38	3.16	1	0.25	No	No	[73]
Kenzelmann-DAB1	1.2	25.2	1	0.36	Yes	No	[64]
Kenzelmann-DAB1	1.65	13.2	1.35	10	Yes	No	[74]
Kenzelmann-DAB1	5	30	1.25	10	Yes	No	[75]
DAB3	5	5	1	5	Yes	No	[2]

1.2 Modular Power Electronics Converter

The modularity in power electronic converters is gaining more attention as it allows to simplify the analysis of the electronic circuits and offers improved performance. Reduced design cost, redundancy, and “hot swap” feature are other advantages of a modular converter. The “hot swap” characteristic enables the user to switch any faulty module with a fresh one in a few easy steps. Furthermore, if any module encounters any malfunction, it can be bypassed by implementing some intelligence in the control circuit; and thus, a continuous service can be achieved. Besides, the modularity allows stack multiple modules to increase the power rating of the converter [121]-[130].

First modular structure in power electronic converter was introduced in 1970’s by Landsman [131], which was based on the canonical switching cell, including an inductor, a capacitor, and a single pole double throw switch. As shown in Figure A (a), the block has three terminals A, B, and C, and each of them can be adopted as an input, common, and output terminal. By changing the connection of three terminals, six various converters can be synthesized, including conventional buck, boost, and buck-boost converters. This modular structure has considerably diminished the modeling and analysis complication and has provided additional merits such as improved electromagnetic interference (EMI) and ripple performance [132]-[140].

An advanced canonical cell can be formed by adding two capacitors, as shown in Figure A(b). The advanced cell offers better performance for high switching frequency. There is a direct path from the input to the output if terminal 1 or 2 is grounded and terminal 3 is considered as the output. So, this configuration is defined as the direct converter while if terminal 3 is grounded, the configuration is defined as the indirect converter since there is

no direct path between input and output. The buck converter synthesized from the canonical cell is a special case of the chopper circuit family where a low-pass filter is employed at the output of the converter. It has conclusively been shown that the boost converter and the buck converter can be implemented from more generalized bidirectional circuit. A transformation technique has been suggested in [X] to convert the isolated Ćuk converter into the buck-boost converter.

Figure 1.2: Schematic of the canonical cell. (a) basic canonical cell. (b) advanced canonical cell.

Multilevel dc-dc converter has been studied over the latest few decades because it enables the designer to build a high efficiency modular circuit, in which the bidirectional power management can be achieved [141]-[145]. More recent studies have confirmed that some switched-capacitor topologies with capacitive energy transfer technique can provide a high efficiency performance. In other words, series-parallel switched-capacitor converter contains only switches and capacitors, and it lacks any magnetic components. Figure 1.2 shows a 3-level series parallel converter, in which the series-connected capacitors get charged from input source V_{in}, and then the capacitors get discharged and transfer the energy to the output. Even though this circuit can provide a high efficiency performance,

changing the voltage conversion ratio is complicated. Also, different switches experience different voltage stress levels. Another disadvantage of this topology is that it does not allow to control the power flow as the direction of power flow depends on the voltages at the two ends, which may change. In electric vehicle applications, the battery voltage can change widely, though power transfer is needed in either direction regardless of the voltage level of two end buses. Moreover, due to charge unbalance among different capacitors, an extra circuit is required for start of charging state.

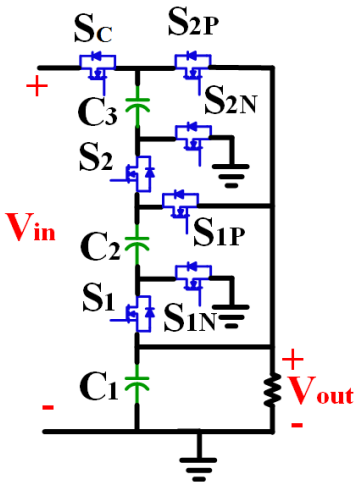


Figure 1.3: Schematic of a three level series-parallel switched capacitor converter.

The flying capacitor multilevel converter is considered the second multilevel converter widely discussed in the literature [146]-[155]. Figure 1.3 shows a schematic of 3-level flying capacitor converter, in which the high-side voltage is three times of the low-side voltage. It is noteworthy to mention that this converter is defined as a 4-level converter in the literature as he zero voltage is counted as a level. In [156], it is described that this topology can offer the maximum efficiency of 98%, and the bidirectional power flow can be established. Compared to the series-parallel switched capacitor converter, the voltage

stress of all the switches are equal. However, complicated switching pattern for different switches is the major disadvantages of this circuit. Besides, since the effective switching frequency is N times of the actual switching frequency, the high frequency noise appears at the output voltage, which makes this converter undesirable for high frequency applications.

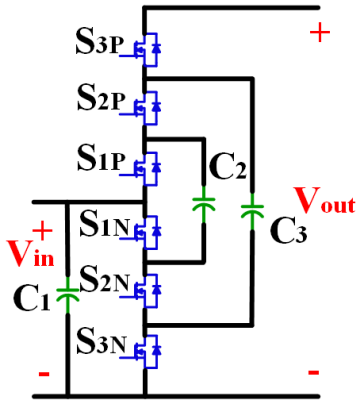


Figure 1.4: Schematic of a three-level flying capacitor converter.

The multilevel dual voltage converter is another dc-dc converter widely discussed in the literature [157]-[160]. As shown in Figure 1.4, the main element of the circuit is a modular switching cell consisting of two switches and one capacitor. The cells can be connected in a stacked manner to increase the output voltage. Also, the power can be transferred between the sources connected to the low-voltage and high-voltage sides. Lower cost is the main advantage of the converter as just one bootstrap drive circuit is required to drive the switches in each cell. Moreover, compared to the previous circuits, using individual power supplies for the gate drivers is not necessary. However, when high number of levels is needed, the circuit cannot be a commercially viable choice since for N-level converter, N(N+1) switches and N(N+1)/2 capacitors should be used; consequently, the number of

components is greater than that of the flying capacitor converter. Similar to the flying capacitor converter, the converter is not beneficial for applications where the voltages of the buses vary widely.

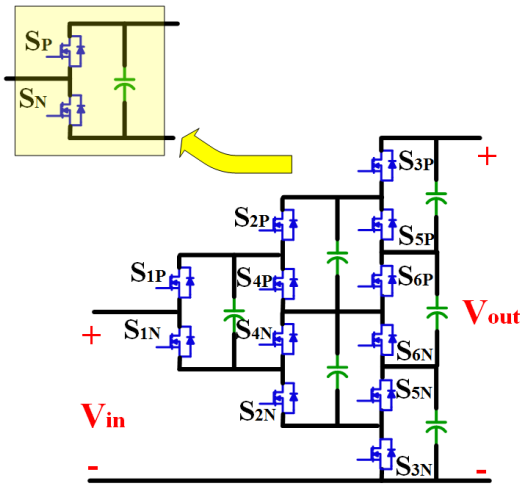


Figure 1.5: Schematic of a modular three-level multilevel converter.

Several studies have revealed that charge-pump circuit can be used for low voltage conversion ratio [161]-[165]. This circuit is derived from the flying capacitor converter and is a cascaded connection of two single ended switched-capacitor converters. Figure1.5 shows the schematic of charge-pump topology, which can provide voltage conversion ratio of 1/3 to 3. The circuit structure and switching scheme is simple as the $R_{DS(ON)}$ of the conducting switches can be controlled by changing the gate voltages to achieve any voltage gain. However, the switches count in this topology is higher than other circuits. Besides, since the switches work in saturation region, there would be much higher switching losses lead to a comparatively small efficiency (65% to 90%). The cascaded connection is the most popular technique to have floating voltage sources that can provide a higher voltage or a higher current rating [166]-[170].

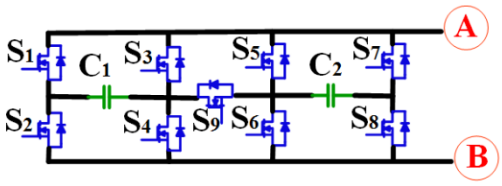


Figure 1.6: Schematic of a charge-pump converter.

Modularity is the principle feature of the cascaded-connected topologies. Compared to the multilevel circuits, there is no limitation on the number of cells as the number of levels in the output voltage increases, the less harmonic content appears in the output waveforms. A series-parallel connection of the converters is shown in Figure1.6 (a). A number of studies have found that a high voltage elevation ratio can be obtained by connecting converters in series at the output without utilizing a transformer. Also, the parallel connection at the input allows to share the input current equally among different modules, leading to lower conduction losses and smaller filter inductors. Modular structure paves the way for standardizing different phases; consequently, the cost can be reduced. As a solution to extend the operating voltage and power of the system, designer can select the number of levels so flexibly that the desired voltage and power rating can be achieved. Even though there is a limitation in the voltage rating of the semiconductors, connecting units in modular way allows employing the power semiconductors with lower voltage rating for the medium voltage applications. As the voltage of DC-link is being controlled, the series-connected switches can handle a significant higher voltage without experiencing any malfunction. In this structure, the faulty unit can be bypassed by adopting an extra switch; so, the system can operate redundantly.

1.3 Techniques to Improve the Efficiency

The power switches employed in the power electronics converters are a source of power losses which are associated with turn-on and turn-off of power devices, as well as conduction. These losses are switching losses and conduction losses, which will be briefly analyzed below [171]-[175].

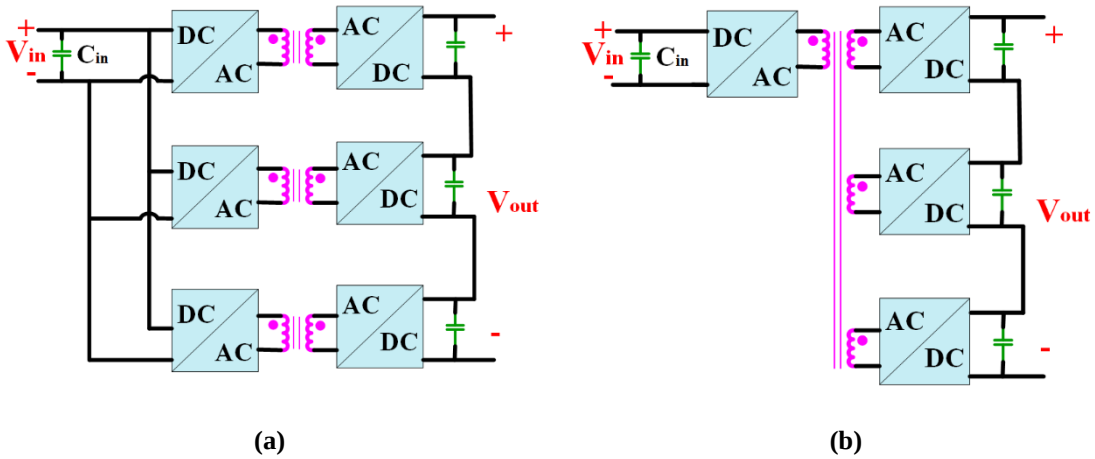


Figure 1.7: Schematic of a cascaded converters. (a) series-parallel connected converters. (b) Multi-winding transformer converter.

1.3.1 Conduction Losses

The conduction loss of a MOSFET can be defined by the following equation as MOSFET operates similar to a resistor $R_{DS(ON)}$ during on-time.

Since an IGBT during turn-on has a voltage drop of $V_{CE,sat}$, its conduction loss can be defined as follows:

1.3.2 Switching Losses

During turn-on and turn-off, a power semiconductor experiences voltage and current stresses simultaneously, which leads to power losses. In other words, the current and

voltage do not decrease instantly during turn-on and turn-off procedure. The overlapped area of the current and voltage waveforms during turn-on and turn-off is defined as the switching loss. The switching losses linearly increases in proportion to switching frequency; so, the higher switching frequency, the higher switching losses. The electromagnetic interference (EMI) noise is the significant defects of the switching process, which stems from a sharp transition of voltage and current during switching and can impact the operation of a converter and other nearby electrical devices. The current and voltage waveforms in a switching period are demonstrated in Figure 1.7. The turn-off process starts at t_0, when the gate-pulse of switch is removed, and the voltage of switch increases linearly. Note that the voltage and current do not change simultaneously. After time duration of t_{off}, the switch is fully turned-off. The turn-off loss can be calculated by the area under the power loss graph P_{off}. The turn-on process starts at t_1, where the gate pulse is applied to the switch. First, the current increases linearly from zero to the final value. Then, the voltage decreases from Vsw to zero. The area under the power loss graph P_{on} results in the turn-on switching loss.

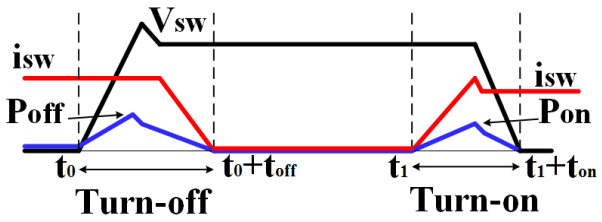


Figure 1.8: Current, voltage, and power loss during hard-switching performance.

Soft-switching techniques paves the way for reducing the switching losses and EMI issues related to hard-switching performance. In fact, in soft-switching performance, the current

or voltage are forced to be zero while the switching transition is occurring; consequently, the switching losses is reduced. Ideally, there is no overlap between the current and voltage; as a result, the switching losses are zero. Due to the gradual variation of current and voltage in soft-switching performance, EMI issue is considerably alleviated. Generally, the soft-switching techniques can be categorized into zero-voltage-switching (ZVS) and zero-current-switching (ZCS). Even though both ZVS and ZCS can be achieved for either MOSFET or IGBT, ZVS is favored for the MOSFET's turn-on performance and ZCS is preferred at IGBT's turn-off transition [176]. The equivalent model of a MOSFET is shown in Figure 1.8, which consists of a body-diode and an output capacitor across drain and source.

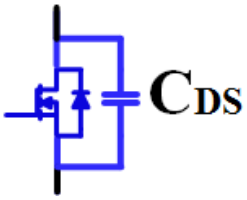


Figure 1.9: Equivalent model of MOSFET.

1.4 Research Objectives

The main research objectives of this dissertation are to design new power electronic converters with high voltage conversion ratio and high efficiency due to the soft-switching performance that make it a potential candidate for interfacing between low voltage sources, such as renewable energy sources, and medium voltage DC bus. Beside the high efficiency, the proposed topologies can provide high power density, which is an important factor for reducing cost and volume. To achieve this goal, different aspects of power converters specifications, including thermal management and electromagnetic effects have been considered in conjunction with the electrical design. In addition, the modularity of the

structures improves the flexibility of changing the number of levels resulting in changing voltage gain, fault bypass capability, and redundancy. Therefore, the proposed converters. Accordingly, the proposed new topologies offer the following advantages:

1) Providing input current with small current ripple that leads to prolong the lifetime of the input sources, especially fuel-cell source.
2) Avoid working under extreme duty-cycle values by offering a wide voltage conversion ratio, hence, high efficiency over a wide range of voltage conversion ratio can be achieved by virtue of decreasing the conduction losses.
3) The potential difference between the grounds of the ports of the converters should be constant in order to minimize the leakage currents, hence, reduce the required periodic maintenance. Modular topology provides reliable operation as a fault happens in any module, that specific module can be bypassed to guarantee an unbroken performance.

The noteworthy aspects of this study can be summarized as follow:

1) Design and develop new bipolar dc-dc converter with wide voltage gain range for interfacing ESS with DC-bus in SPS.
2) Design and develop a family of three-port three-level converters that can offer the benefits in terms of a simple control scheme, extended soft switching over a wide range of operating conditions, and reduced voltage stress across switches.
3) Design and development of an integrated interleaved dc-dc converter with ultra-high voltage gain and reduced voltage stress based on the coupled-inductors and switched-capacitor circuits for electric vehicles.

4) Development of a modular quasi-resonant inverters that can provide high voltage gain for input source without utilizing any transformer, resulting in higher power density and higher efficiency.

1.5 Original Contribution of This Thesis

The main contributions of this dissertation are the following:

1) Developing a bipolar dc-dc converter with wide voltage gain range for interfacing ESS with DC-bus in SPS. To protect the ESS against rapid discharging due to any short-circuit fault on the DC-bus, a high-frequency transformer is adopted in the proposed topology. Moreover, diode-capacitor circuits are employed in the secondary side to provide a wide voltage gain. The converter takes advantage of active clamp configuration, in terms of limiting the voltage stress of switches and providing soft-switching performance.
2) Developing a family of three-port three-level converters composed of asymmetrical bidirectional half-bridge modules is proposed, which offers the benefits in terms of a simple control scheme, extended soft switching over a wide range of operating conditions, and reduced voltage stress across switches. The proposed converters take advantage of a pulse-width-modulation plus phase-shift control technique to regulate the output voltage as well as control the power flow between different ports independently.
3) Designing a novel modular quasi-resonant bidirectional (MQRB) dc-dc converter composed of half-bridge gallium nitride modules (HBGM) with reduced switch voltage stress. By using an auxiliary capacitor, a resonant circuit is formed to shape

the current and voltage so that zero-voltage-switching (ZVS) at turn-on instant is achieved.

4) Developing a new voltage-quadrupler interleaved bidirectional DC-DC converter with intrinsic equal current sharing. The proposed converter offers a wide voltage conversion ratio, which makes it suitable for interconnecting the energy storage unit with dc-bus for electric vehicle applications. A high voltage gain and low voltage stress across switches are achieved by adopting the capacitive voltage-divider stage, which enables the designer to employ a low-voltage switch with a small on-resistance $R_{DS(ON)}$. As a result, it allows the converter to run more efficiently and cooler.
5) Design and implementation of a double-input three-level converter composed of Buck-Boost-Half-Bridge (BBHB) modules for automotive applications. The proposed converter can supply the load in the absence of FC or battery. The converter takes advantage of active clamp configuration in terms of reducing the voltage stress across switches and providing soft-switching performance. Consequently, the converter's overall performance in terms of switching losses and cost can be considerably improved.
6) Analysis and development of a novel stacked three-port three-level converter (STPTLC) using GaN switches is proposed for interfacing the renewable energy sources with load for applications that the presence of energy storage device is necessary. Derived from the asymmetrical bidirectional half-bridge converter, the proposed converter presents valuable advantages in terms of simple control

scheme, extended soft switching over a wide range of operating conditions, and reduced voltage stress across switches.

7) Design and development of an integrated interleaved dc-dc converter with ultra-high voltage gain and reduced voltage stress based on the coupled-inductors and switched-capacitor circuits, which is suitable for interfacing the low-voltage energy sources, such as fuel-cell, with a high-voltage dc bus in electric vehicle applications. Input-parallel connection of the coupled-inductors offers a reduced input current ripple and the current rating of components, as well as automatic input current sharing without a dedicated current sharing controller.
8) Development of a soft-switched boost converter including an integrated dual half-bridge circuit with high voltage gain and continuous input current for the applications requiring a wide voltage gain range, such as for the front-end of the inverter in a DC microgrid to integrate renewable energy sources (RES). In the proposed converter, two half-bridge converters are connected in series at the output stage to enhance the voltage gain.
9) Development of a modular quasi-resonant inverters that can provide high voltage gain for input source without utilizing any transformer, resulting in higher power density and higher efficiency.

1.6 Dissertation Organization

Chapter 2 gives an overview and full literature review of the bidirectional dc-dc converters for ship-power systems (SPS) with medium voltage direct current. A bipolar dc-dc converter with wide voltage gain range is proposed for interfacing energy storage system with DC-bus in SPS. To protect the energy storage system against rapid discharging due to

any short-circuit fault on the DC-bus, a high-frequency transformer is adopted in the proposed topology. Moreover, diode-capacitor circuits are employed in the secondary side to provide a wide voltage gain. The converter takes advantage of active clamp configuration, in terms of limiting the voltage stress of switches and providing soft-switching performance. Finally, a simulation in MATLAB/Simulink platform is carried out to validate the correctness of the theoretical analysis.

In chapter 3, a family of three-port three-level converters composed of asymmetrical bidirectional half-bridge modules is proposed, which offers the benefits in terms of a simple control scheme, extended soft switching over a wide range of operating conditions, and reduced voltage stress across switches. The proposed converters take advantage of a pulse-width-modulation plus phase-shift control technique to regulate the output voltage as well as control the power flow between different ports independently. The feasibility of the proposed concept and effectiveness of the design approach are validated based on the experimental results of a 1 kW, 100 kHz prototype using gallium nitride switches.

In chapter 4, a modular quasi-resonant bidirectional dc-dc converter composed of half-bridge gallium nitride modules with reduced switch voltage stress is proposed in this chapter. By using an auxiliary capacitor, a resonant circuit is formed to shape the current and voltage so that zero-voltage-switching (ZVS) at turn-on instant is achieved. Since the switching loss dominates the power losses in high-frequency dc-dc converters, the soft-switching performance leads to a noticeable reduction in the total loss; so, the operating temperature will decrease, and consequently, size of the heatsink will be reduced. Finally, a 1 kW, 600 V laboratory prototype operating at 100 kHz, along with some simulation scenarios, are carried out to validate the proposed concept of modularity.

In chapter 5, A modular multi-level bi-directional diode-clamped DC-DC converter based on eGaN High Electron Mobility Transistor (HEMT) is proposed as a plugin charger for electric vehicles (EVs). The eGaN HEMT can switch efficiently even in hard switching, but their problem is that they cannot tolerate voltage stresses higher than 650V. The proposed multilevel topology reduces the voltage stress across the switches which enables utilizing eGaN HEMT technology in the powertrain of the EVs. Simulations were carried out in PSpice environment using the eGaN equivalent circuit provided by the manufacturer.

In chapter 6, a voltage-quadrupler interleaved bidirectional DC-DC converter with intrinsic equal current sharing is presented. The proposed converter offers a wide voltage conversion ratio, which makes it suitable for interconnecting the energy storage unit with dc-bus for electric vehicle applications. A high voltage gain and low voltage stress across switches are achieved by adopting the capacitive voltage-divider stage, which enables the designer to employ a low-voltage switch with a small on-resistance $R_{DS(ON)}$. As a result, it allows the converter to run more efficiently and cooler. Moreover, a built-in equal current sharing is achieved for two interleaved phases without using a current-sharing control scheme. Finally, to verify theoretical analysis, a 2 kW scaled-down laboratory prototype of the proposed converter using Gallium-Nitride switches is implemented.

In chapter 7, a double-input three-level converter composed of Buck-Boost-Half-Bridge modules is proposed for automotive applications. The proposed converter can supply the load in the absence of FC or battery. The switching scheme doubles the effective switching frequency, which, in turn, reduces the size of the boost inductors to enhance power density. The operational characteristics of the converter and comparison with state-of-the-art

converters are given in this chapter. Finally, a 4 kW, 100 kHz prototype using GaN switches is implemented to validate the proposed concept.

In chapter 8, a stacked three-port three-level converter using GaN switches is proposed for interfacing the renewable energy sources with load for applications that the presence of energy storage device is necessary. The soft switching for all switches at turn-on instant is guaranteed thanks to active clamp configuration, resulting in high-efficiency performance. The experimental results of a 1 kW, 100 kHz prototype of the converter using GaN switches are given to confirm the validity of the proposed concept.

In chapter 9, an integrated interleaved dc-dc converter with ultra-high voltage gain and reduced voltage stress based on the coupled-inductors and switched-capacitor circuits is proposed, which is suitable for interfacing the low-voltage energy sources, such as fuel-cell, with a high-voltage dc bus in electric vehicle applications. A promising power-density improvement technique is given, in which only one magnetic core is utilized to implement two coupled-inductors that can provide the filter functionality as well as transformer behavior. Finally, experimental results of a 1 kW, 100 kHz prototype are provided to confirm the validity of the proposed concept.

In chapter 10, a soft-switched boost converter including an integrated dual half-bridge circuit with high voltage gain and continuous input current is introduced that can be suitable for the applications requiring a wide voltage gain range, such as for the front-end of the inverter in a DC microgrid to integrate renewable energy sources (RES). In the proposed converter, two half-bridge converters are connected in series at the output stage to enhance the voltage gain. Additionally, the balanced voltage multiplier stage is employed at the output to increase the voltage conversion ratio, as well as distribute the

voltage stress across semiconductors; hence, switches with smaller on-resistance $R_{DS(on)}$ can be adopted resulting in an improvement in the efficiency. A 1-kW laboratory prototype was built using gallium nitride (GaN) transistors and silicon carbide (SiC) diodes to confirm the effectiveness of the proposed topology.

In chapter 11, a Modular Quasi-Resonant Inverters (MQRIs) is proposed that can provide high voltage gain for input source without utilizing any transformer, resulting in higher power density and higher efficiency. In the proposed family of MQRIs, a resonant circuit is employed not only to achieve soft switching for all switches but to limit the inrush current during start-up.

In chapter 12, a conclusion of this dissertation and an insight on recommended future work are given.

Chapter 2 A Bipolar DC-DC Converter with Wide Voltage-Gain Range for Energy Storage Integration in Ship Power Systems

2.1 Introduction

Ship Power System (SPS) with medium voltage direct current (MVDC) is attracting widespread interest due to higher reliability and reduced fuel consumption. Energy storage system (ESS) is recognized as being the critical part of the MVDC distribution power system, enabling peak shaving, zero emission operation, and optimal scheduling of generators. In this chapter, a bipolar dc-dc converter with wide voltage gain range is proposed for interfacing ESS with DC-bus in SPS. To protect the ESS against rapid discharging due to any short-circuit fault on the DC-bus, a high-frequency transformer is adopted in the proposed topology. Moreover, diode-capacitor circuits are employed in the secondary side to provide a wide voltage gain. The converter takes advantage of active clamp configuration, in terms of limiting the voltage stress of switches and providing soft-switching performance. The extension of the proposed concept for application with multiple loads, detailed analysis of the steady-state operation of the converter, and battery discharge limiting capability are given in this chapter. Finally, a simulation in MATLAB/Simulink platform is carried out to validate the correctness of the theoretical analysis.

2.2 Proposed Isolated Bipolar Converter

The circuit diagram of the proposed converter is shown in Figure 2. 1 (a). The converter is composed of a half-bridge converter with active-clamp circuit at the input stage, including inductor L_B and switches S_1 and S_2, to provide the soft-switching performance

and limit the voltage stress across switches. To improve the voltage conversion ratio and decrease the voltage stress across switches and output diodes, three diode-capacitor cells are connected in a way that the capacitors are charged in parallel and discharged in series. Figure 2.1(b) shows the equivalent circuit of the proposed topology, where the transformer is replaced by a magnetizing inductance L_m, leakage inductance L_k, and an ideal transformer with turns-ratio n ($n = N_S/N_P$). Moreover, R_{o1} and R_{o2} represent the load resistances. The duty cycle D of main switch S_1 is the control variable to regulate the output voltage, and the switches are driven complementary.

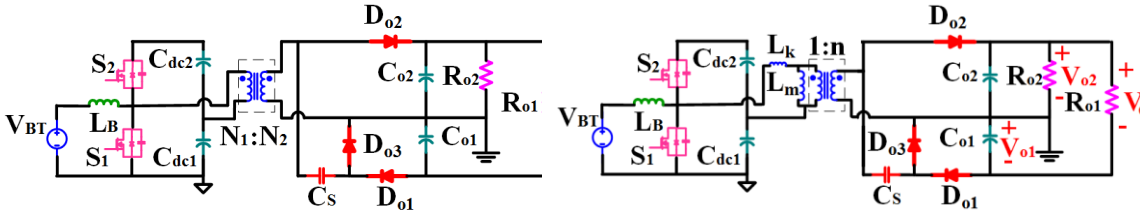


Figure 2.1: Proposed isolated converter and its equivalent circuit. (a) Circuit diagram of proposed isolated converter. (b) Equivalent circuit.

2.3 Operating Principles of the Proposed Circuit

The operation of the proposed converter in one switching period can be divided into five intervals, as shown in Figure 2. 2. Also, the key waveforms are plotted in Figure 2. 3. For the sake of simplification, it is assumed that the output capacitors C_{o1} and C_{o2} and capacitor C_s are large enough that operate like a voltage source. Furthermore, inductance L_B is so large that can be considered as a current source.

2.3.1 Interval 1 [t_0-t_1]

Before t_0, switch S_2 is turned on and the diodes D_{o2} and D_{o3} are conducting the current. The gate pulse of switch S_2 is removed at t_0. So, the output capacitors of switches S_1 and S_2 are

being discharged and charged, respectively. This process stops when the voltage of the output capacitor of switch S_1 reaches zero. After that, the body diode of switch S_1 starts to conduct the current. Therefore, to realize soft-switching performance for switch S_1, its gate-pulse can be applied before the current becomes zero.

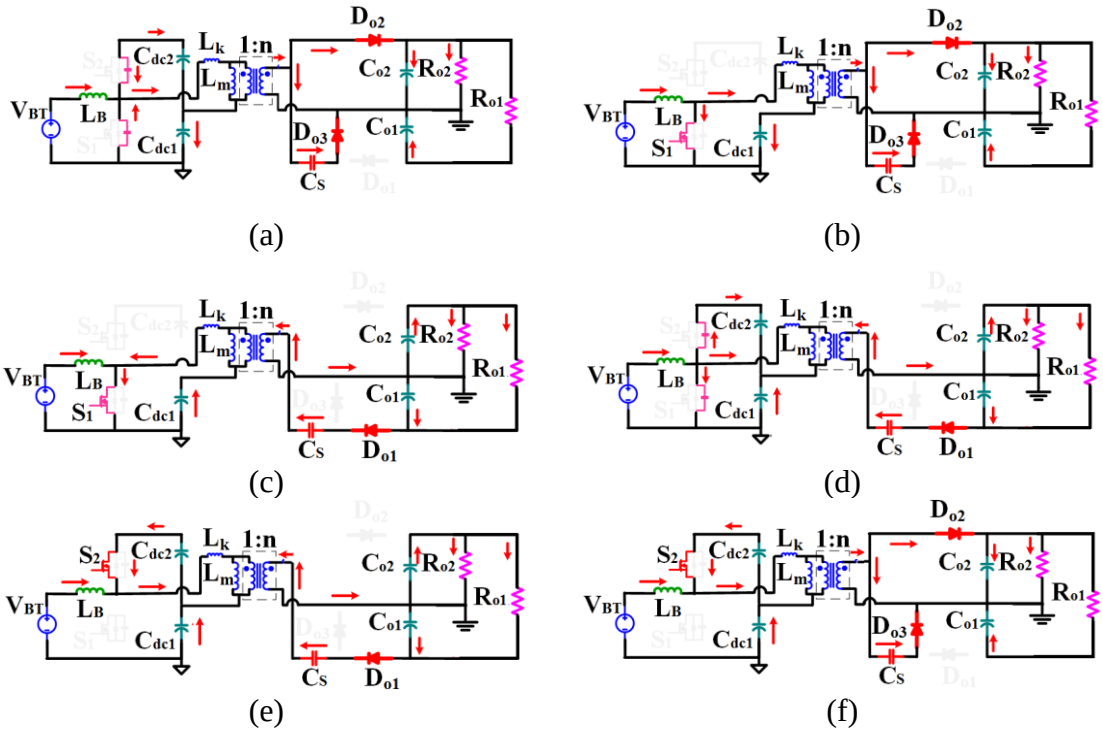


Figure 2.2: Operation intervals of the bipolar DC-DC converter. (a) Interval 1. (b) Interval 2. (c) Interval 3. (d) Interval 4. (e) Interval 5. (f) Interval 6.

2.3.2 Interval 2 [t_1-t_2]

At t_1, the gate-pulse of switch S_1 is applied and the current goes through the switch. The inductor L_B is charged by the input source V_{BT}. Meanwhile, at the secondary side, the capacitors C_{o2} and C_s are being charged. This mode ends when the secondary side becomes zero. The following equations describe this operation mode.

$$I_{Lk,P} = \frac{(V_{Co2}/n) + V_{DC1}}{L_k} d_1 T_s \tag{2-1}$$

$$t_2 - t_0 = d_1 T_s \tag{2-2}$$

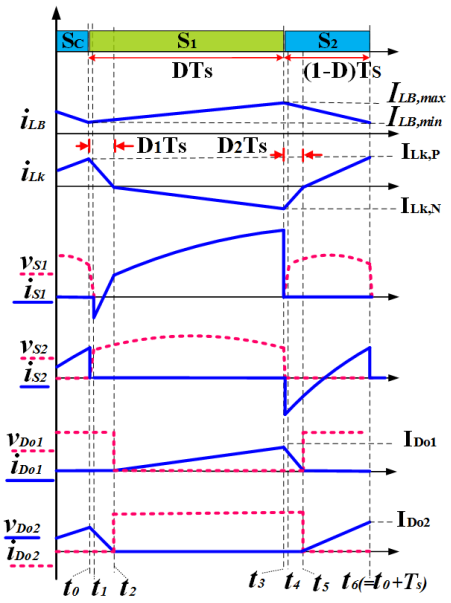


Figure 2.3: Key waveforms.

2.3.3 Interval 3 [t_2-t_3]

At t_2, the current of transformer changes and the diodes D_{o2} and D_{o3} are turned-off and the current flows through diode D_{o1}. As shown in Figure 2.3, the current of inductor L_B increases linearly controlled by source V_{BT}. Meanwhile, at the secondary side, the capacitors C_{o2} and C_s are being discharged. This mode ends when the secondary side becomes zero. The equations determining this mode are given as follows:

$$i_{Lk}(t) = \frac{(V_{o1} - V_{Cs})/n - V_{DC1}}{L_k} (t - t_2) \tag{2-3}$$

$$t_3 - t_2 = (D - d_1 - d_2) T_s \tag{2-4}$$

2.3.4 Interval 4 [t_3-t_4]

At t_3, the gate-pulse of switch S_2 is removed and the output capacitors of switches S_1 and S_2 are being charged and discharged, respectively. This process stops when the voltage of the output capacitor of switch S_2 reaches zero. After that, the body diode of switch S_2 starts to conduct the current. Therefore, to realize soft-switching performance for switch S_2, its gate-pulse can be applied before the current becomes zero.

2.3.5 Interval 5 [t_4-t_5]

At t_4, the gate-pulse of switch S_2 is applied and the current goes through the switch. The inductor L_B is discharged by the voltage difference between the input source V_{BT} and V_{DC2}. This mode ends when the secondary side becomes zero. The equations describing this mode are given as follows:

$$i_{Lk}(t) = \frac{(V_{o1} - V_{Cs})/n + V_{DC2}}{L_k}(t - t_4) \tag{2-5}$$

$$t_5 - t_4 = d_2 T_s \tag{2-6}$$

2.3.6 Interval 6 [t_5-t_6]

At t_5, the current of transformer changes and the diodes D_{o1} is turned-off and the current flows through diode D_{o1}. The inductor L_B is discharged by the voltage difference between the input source V_{BT} and V_{DC2}. This mode ends when the secondary side becomes zero. The equations describing this mode are given as follows:

$$i_{Lk}(t) = \frac{V_{o2}/n + V_{DC2}}{L_k}(t - t_5) \tag{2-7}$$

$$t_6 - t_5 = (1 - D - d_1)T_s \tag{2-8}$$

2.4 Steady-State Analysis

To simplify the analysis, it is assumed that the capacitors C_{o1}, C_{o2}, and C_s are large enough that can be considered a voltage source. Also, the output capacitors and clamp-capacitors are identical, i.e., $C_{DC1} = C_{DC2} = C_{DC}$ and $C_{o1} = C_{o2} = C_o$.

2.4.1 Voltage Conversion Ratio

By applying the voltage-second balance to the inductor L_B, the following equation can be obtained.

$$V_{DC1} + V_{DC2} = \frac{V_{BT}}{1 - D} \tag{2-9}$$

Where D is the duty-cycle of main switch S_1. Similarly, if the voltage-second balance is applied to the inductor L_m, the voltages V_{DC1} and V_{DC2} can be defined by

$$V_{DC1} = V_{BT} \tag{2-10}$$

$$V_{DC2} = \frac{D}{1 - D} V_{BT} \tag{2-11}$$

The average current of capacitors are zero in steady-state; therefore, the average current of leakage inductor can be written by

$$\langle i_{Lk} \rangle = 0 \tag{2-12}$$

From Figure 2. 3 and (12), the relation between the maximum current $I_{o1,peak}$ and $I_{o2,peak}$ can be defined as follows:

$$\frac{(1 - D - d_2 + d_1) I_{DO2}}{2} = \frac{(D + d_2 - d_1) I_{DO1}}{2} = I_{out} \tag{2-13}$$

From (12) – (13), d_1 and d_2 can be calculated by

$$d_1 = \alpha D \tag{2-14}$$

$$d_2 = \alpha (1 - D) \tag{2-15}$$

$$\alpha = 0.5(1 - \sqrt{1 - \frac{8nL_k V_{Out}}{R_o V_{BT} D T_s}}) \tag{2-16}$$

From (1), (5), and (7) – (16), the voltage conversion ratio can be determined by

$$M = \frac{V_{Out}}{V_{BT}} = \frac{nD(1+D)(1-2\alpha)}{(D(1-2\alpha)+\alpha)(1-\alpha-D(1-2\alpha))} \tag{2-17}$$

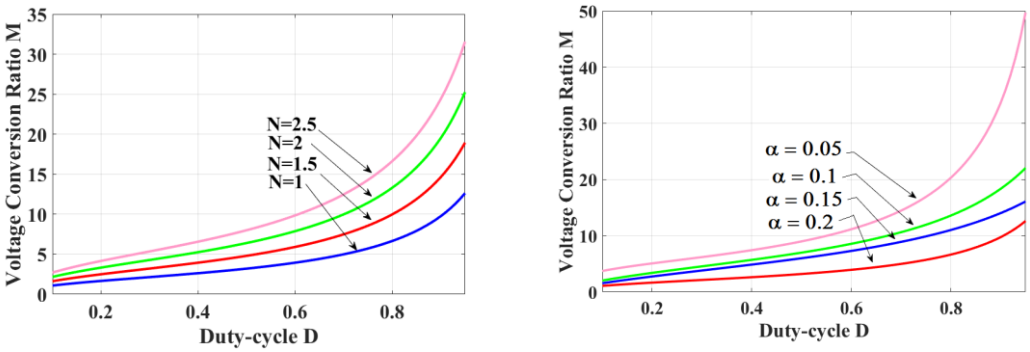
In ideal case, when the leakage inductance is zero, the voltage across the output capacitor can be written as follows:

$$M = \frac{V_{Out}}{V_{BT}} = \frac{V_{O1} + V_{O2}}{V_{BT}} = \frac{nD(1+D)}{(1-D)} \tag{2-18}$$

$$M_1 = \frac{V_{O1}}{V_{BT}} = \frac{n}{(1-D)} \tag{2-19}$$

$$M_2 = \frac{V_{O2}}{V_{BT}} = \frac{nD}{(1-D)} \tag{2-20}$$

The voltage conversion ratio (M) of the proposed converter under different turns-ratio and α values is depicted in Figure 2. 4. As shown in Figure 2. 4(a), the voltage gain increases as turns-ratio n increases. So, turns-ratio can help the designer to achieve higher voltage gain while working in lower duty-cycle values resulting in lower losses. In Figure 2. 4(b), the voltage gain is plotted as a function of duty-cycle and α. When α increases, the voltage gain decreases. Figure 2.5 helps the designer to obtain the values of L_k, n, and D for a given voltage conversion ratio for feeding specific load.



(a) (b)

Figure 2.4: Voltage gain as a function of turns-ratio and α. (a) Voltage gain under different turns-ratio (α =0.1). (b) Voltage gain under different α (ν=1).

2.4.2 Soft-switching Performance

According to Figure 2. 2(a) and (d), to realize soft-switching for switches S_1 and S_2, the gate pulse of the switches should be applied while their body-diodes are conducting the current. So, following conditions should be met to ensure zero-voltage switching at turn-on for switches:

$$\frac{1}{2}L_{Lk}I_{S1,ZVS}^2 > \frac{1}{2}C_{oss,Tot}(\frac{V_{BT}}{1-D})^2 \quad (2\text{-}21)$$

$$\frac{1}{2}L_{Lk}I_{S2,ZVS}^2 > \frac{1}{2}C_{oss,Tot}(\frac{V_{BT}}{1-D})^2 \quad (2\text{-}22)$$

$$C_{oss,Tot} = C_{oss,S1} + C_{oss,S2} \quad (2\text{-}23)$$

Where $I_{s1,ZVS}$ and $I_{s2,ZVS}$ are defined by

$$I_{S1,ZVS} = I_{BT} - I_{LK,P} \quad (2\text{-}24)$$

$$I_{S2,ZVS} = I_{BT} + I_{LK,N} \quad (2\text{-}25)$$

It can be seen that the soft-switching condition for switch S_2 is always satisfied. On the other hand, if the leakage inductance L_{Lk} is very small or the boost inductor L_B is very large, condition (21) may not be satisfied, implying soft-switching performance is

controversial for switch S_1. Figure 2. 5 shows the marginal curve of soft-switching condition of main switch S_1 under different output power, battery voltage, and duty-cycle for various values of $C_{oss,Tot}$.

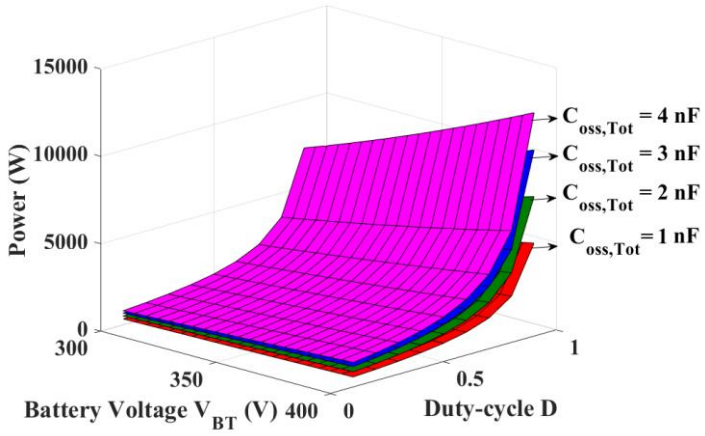


Figure 2.5: Soft-switching condition of main switch S_1 under different output power, battery voltage, and duty-cycle for various values of $C_{oss,Tot}$.

2.4.3 Voltage Stress of Semiconductors

As shown in Figure 2. 2, the voltage stress of the switches is limited to the summation of voltage of capacitors C_{DC1} and C_{DC2}. So, the voltage stress of switches are defined by

$$V_{S1} = V_{S2} = \frac{V_{Out}}{(1+D)n} \tag{2-26}$$

The voltage stress of the output diodes can be obtained by

$$V_{Do1} = V_{Do3} = V_{O1} = \frac{nV_{BT}}{1-D} \tag{2-27}$$

$$V_{Do2} = V_{O2} = \frac{nDV_{BT}}{1-D} \tag{2-28}$$

It can be seen that the voltage stress of the switches decreases with increase of turns-ratio. Therefore, switches with lower ON-resistance $R_{DS(ON)}$ can be selected leading to improvement in the efficiency. Moreover, the voltage stress of the output diodes is equal

to half of the output voltage. So, diodes with lower forward voltage-drop can be chosen, resulting in less switching loss.

2.4.4 Battery Discharge Limiting Characteristics

Monitoring the distribution system, responding to faults within milliseconds to restrict the current from the battery bank from fast discharge, and isolating it from feeding power to the fault is critical for electric ships. The proposed converter offers the isolation of battery from DC-bus as well as limiting fast battery discharge. Since a high frequency transformer is utilized in the proposed topology, it can pave the way for stopping power transfer through the transformer in order to prevent the discharge of the battery. At the fault-time instant, the control scheme sends the turn-off commands to the switches S_1 and S_2. So, after turning-off the switches, the voltage across the primary winding of transformer becomes zero. Therefore, the power will not flow through the transformer and the current drawing from battery decay to zero.

2.4.5 Extension of the proposed Concept

An extended version of the proposed concept is shown in Figure 2.6, in which n diode-capacitor cells are connected to feed the different loads with different voltage levels. In this topology, the input stage works as simple as a conventional boost converter. Also, the output capacitors C_{o3}, C_{o4}, …, and $C_{o(k+1)}$ are stacked on the output capacitor C_{o1} to provide different voltage levels. The voltage of output capacitors and the voltage stress of switches are defined by

$$V_{RNk} = \frac{k \times n}{1 - D} V_{BT} \tag{2-29}$$

$$V_{S1} = V_{S2} = \frac{V_{RNk}}{k \times n} \tag{2-30}$$

where k is number of diode-capacitor modules and V_{RNk} is the voltage across the load in k module with negative voltage.

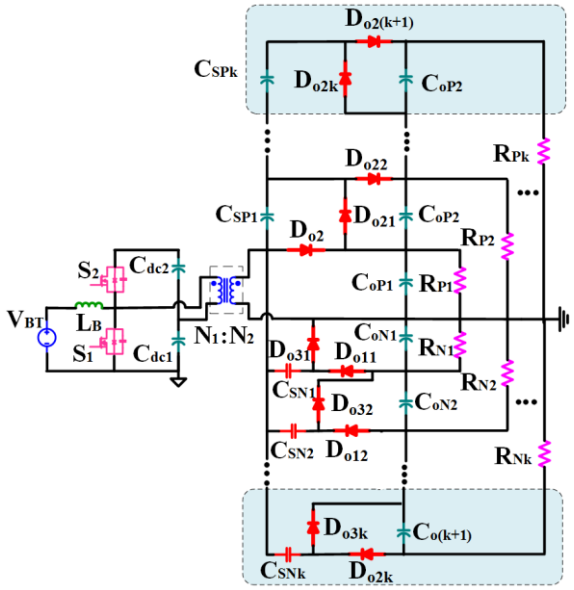
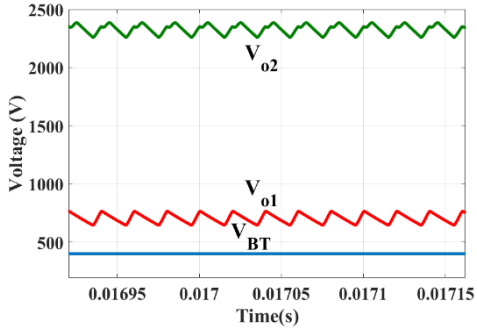


Figure 2.6: Extended version of the proposed isolated converter.

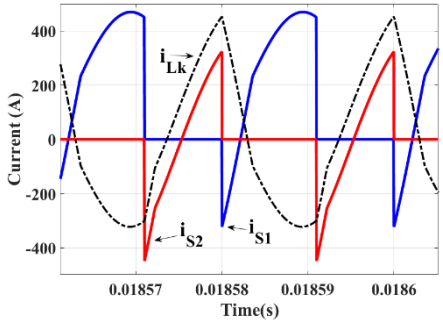
2.5 Simulation Results

To verify the theoretical analysis, a simulation has been carried out for battery voltage 400 V, DC-bus voltage 1500 V, switching frequency 50 kHz, and output power 50 kW. Two different loads are connected to the output ports with different voltage and power levels. Voltage and nominal power of load 1 are 50 kW and 2400 V, and voltage and nominal power of load 2 are 25 kW and 750 V. The simulation results of steady-state performance are shown in Figure 2.8. The battery voltage and voltage V_{o1} and V_{o2} are illustrated in Figure 2.7 (a). It can be seen that the voltage levels are following the theoretical equation. Figure 2. 7(b) demonstrates the current of switches and the leakage inductor current i_{Lk},

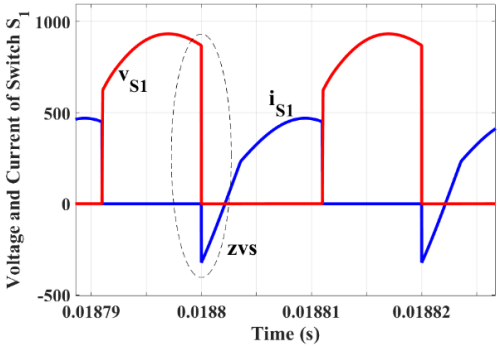
which are changing linearly according to analysis given in Section III. To investigate the ZVS performance of switches S_1 and S_2, the drain-source voltage and current are given in Figure 2.7 (c) and Figure 2.7 (d), respectively. It is clear that the soft switching is realized in the switches. In fact, the voltage across the switches becomes zero before they start conducting the current, implying the turn-on loss becomes zero. Figure 2.7 (e) and Figure 2.7 (f) show the voltage and current of diodes D_{o1} and D_{o2}, respectively. It can be seen that the current of diodes during turn-off process is changing linearly controlled by the leakage inductance, which results in lower reverse-recovery loss.



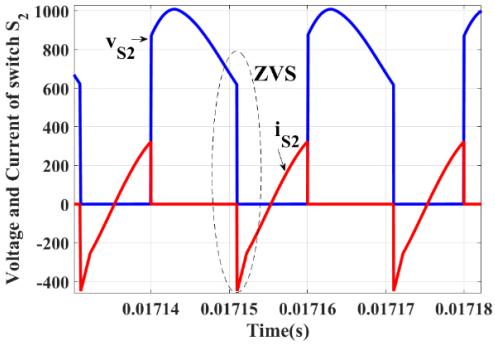
(a)



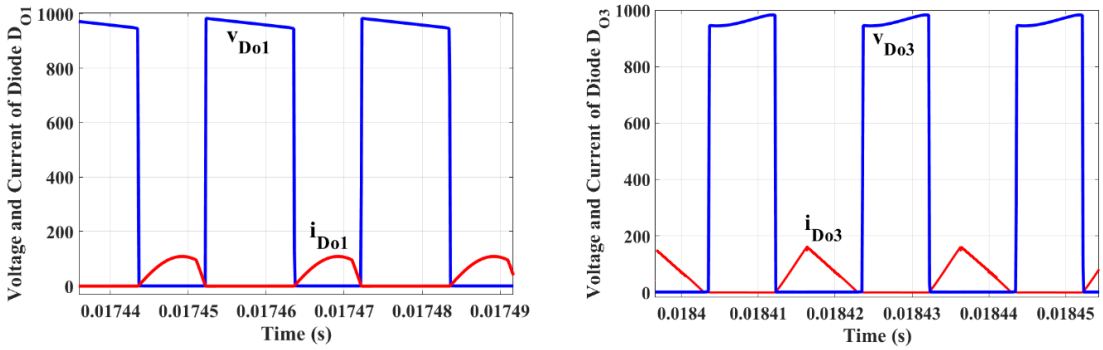
(b)



(c)



(d)



(e) (f)

Figure 2.7: Simulation results. (a) battery voltage and output voltage levels V_{o1} and V_{o2}. (b) Current of switches and the leakage inductor current i_{Lk}. (c) voltage and current of switch S_1. (d) voltage and current of switch S_2. (e) voltage and current of diode D_{o1}. (f) voltage and current of diode D_{o2}.

The converter performance during the short circuit fault between the positive and negative poles is investigated in Figure 2.8. The battery current and leakage inductor current i_{Lk} are shown in Figure 2. 8(a) and (b), respectively. It can be seen that the protection scheme is working effectively and reduces the battery current to zero after 2 ms, implying the energy storage doesn't supply the fault. The current of switches and output diodes are depicted in Figure 2. 8(c) and (d), respectively. It can be observed that the control technique prevents the power flow through the transformer.

2.6 Conclusion

Recent development in power electronics have led to the growth of medium voltage DC distribution systems in ship power system due to their higher efficiency, power quality, and higher reliability. Especially, the energy storage systems play a critical role by keeping the balance between power generation and consumption. In this chapter, an extendable isolated bipolar dc-dc converter is proposed for MVDC distribution system in marine vessels, which is derived from the conventional half-bridge circuit.

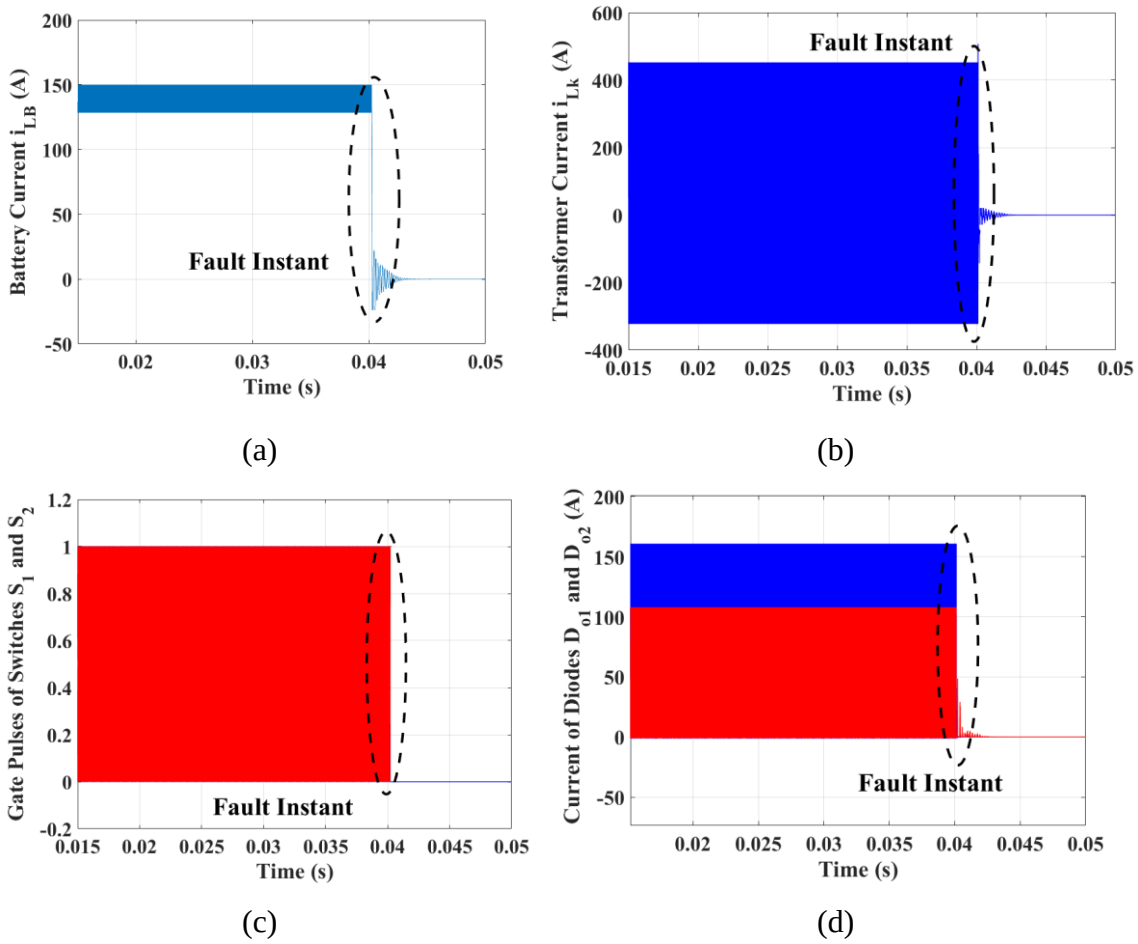


Figure 2.8: Simulation results when there is a pole to pole short circuit fault. (a) battery current i_{LB}. (b) leakage inductor current i_{Lk}. (c) current of switches S_1 and S_2. (d) current of diodes D_{o1} and D_{o2}.

The active clamp circuit is adopted in the proposed converter not only to limit the voltage stress of switches but also to provide the soft-switching performance. The voltage conversion ratio is improved considerably due to employing the diode-capacitor cells. Since the short circuit fault is inevitable in the ship power system, the proposed converter can protect the system by isolating the battery side from DC-bus. Finally, a bipolar dc-dc converter working with switching frequency of 50k Hz and feeding two different loads (25 kW and 50 kW) is simulated with the Simulink platform to verify the theoretical analysis.

Chapter 3 A Family of Three-Port Three-Level Converter Based on Asymmetrical Bidirectional Half-Bridge Topology for Fuel-Cell Electric Vehicle Applications

3.1 Introduction

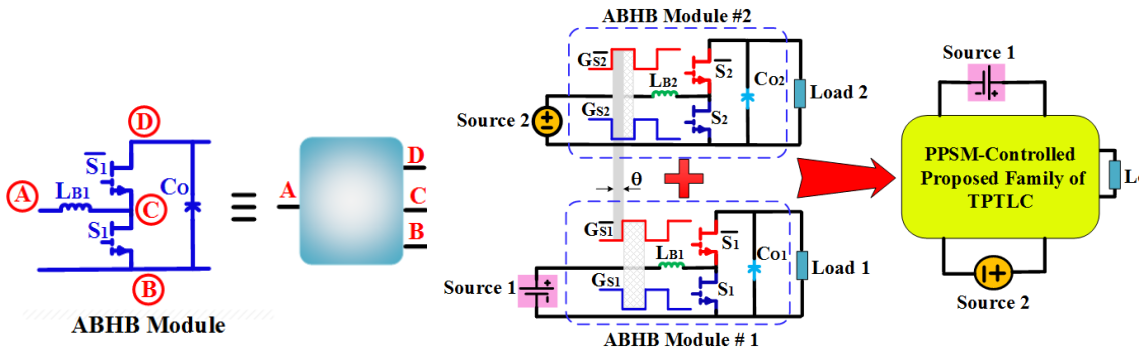
In this chapter, a family of three-port three-level converters (TPTLC) composed of asymmetrical bidirectional half-bridge modules is proposed, which offers the benefits in terms of a simple control scheme, extended soft switching over a wide range of operating conditions, and reduced voltage stress across switches. The proposed converters take advantage of a pulse-width-modulation plus phase-shift control technique to regulate the output voltage as well as control the power flow between different ports independently. A stacked TPTLC is taken as an example to be introduced in detail to gain a thorough insight into the proposed family of converters. The stacked TPTLC can provide a high voltage-gain along with a wide voltage-gain range without using any transformer, resulting in the improvement in the power density. In order to minimize the conduction loss and reduce the current stress of switches, the root-mean-square current of the inductor and the boundary condition of the phase-shift controller in different operation scenarios are studied. Finally, the feasibility of the proposed concept and effectiveness of the design approach are validated based on the experimental results of a 1 kW, 100 kHz prototype of the stacked TPTLC using gallium nitride switches.

3.2 Derivation Methodology of The TPTLC Topologies

3.2.1 The idea of TPTLC Topologies

The cornerstone of a TPC is the output port should be highly regulated to connect to

DC/AC converter while the input port is connected to an RES, such as FC. Concerning the volatility of RES, the presence of an energy storage element is necessary to supply the mismatched power. As depicted in Figure 3.1(a), ABHB module is capable of bidirectional power flow control and includes one switching leg that is comprised of two switches, S_1 and $\overline{S_1}$, an input filter inductor L_{B1}, and an output capacitor C_o. In Figure 3.1(a), the symbol "–" stands for the complementary gate pulse of the switch with the same index. For instance, two switches S_1 and $\overline{S_1}$ are driven complementary. Essentially, the input and output ports can be connected to either an energy storage element or an RES, such as FC. Generally, to construct a TPC with a minimum component number, two modules can be merged. The general structure of TPC is illustrated in Figure 3.1(*b*). Referring to Figure 3.1*(b)*, two duty-cycle controlled ABHB modules can be connected in a way that a three-port converter with a PPSM control scheme is synthesized. In fact, the second module can be integrated into the first module to provide three ports with bidirectional power flow capability, supply the load from two sources, and regulate the output voltage. Regarding the voltage and power regulation, the output port of each module is regulated by the duty-cycle, D, and the phase shift controls the power flowing between the modules 1 and 2. Nevertheless, to synthesize partially-isolated TPC, a transformer can be employed to generate a high-frequency ac voltage. Then, a rectifier stage is employed to provide the dc-voltage.



(a) (b)

Figure 3.1: Topology derivation of the proposed family of three-port three-level DC/DC converters from ABHB modules: (a) Duty cycle controlled ABHB module. (b) PWM plus phase-shift modulated TPTLC composed of ABHB modules.

3.2.2 Different Topologies of TPTLCs

A technique for synthesizing different TPTLC topologies is inspired by combining ABHB modules in various forms to make them suitable for a wide variety of applications. There are nine various circuit topologies in this family of TPTLCs, which can be categorized as non-isolated and partially-isolated as illustrated in Table 3.1 and Table 3.2, respectively. The main advantage of non-isolated TPTLC is that a high voltage gain can be attained without using a transformer. Compared to the classical solutions, the proposed nonisolated TPTLCs can directly charge and discharge the battery while the power is not required to pass through the transformer; so, a more compact power conversion system with higher efficiency is ensured. Since these topologies are derived from integrating the concept of multilevel converter and active-clamp circuit, the voltage stress across the switches is reduced compared with other state-of-the-art TPCs. Consequently, the designer can employ the low-voltage rating switches, thereby, reducing the conduction and switching losses. All the switches in the proposed family of TPTLC can be switched at zero voltage, which is

achieved without additional auxiliary circuit that leads to improvement in the system performance. In the proposed family of TPTLCs, all three ports are capable of bidirectional power flow. Besides, both sources can feed the load separately, and the power between the two sources can be regulated simultaneously. It is noteworthy to mention that for renewable energy applications, such as FC, the power can only go to the load or energy storage element port since FC cannot absorb the power. Generally, the power flow is controlled by the phase shift between ABHB modules, and the duty-cycle of switching legs regulate the output voltage. This control scheme paves the way for a seamless transition between different operation scenarios due to its symmetrical switching pattern.

For non-isolated configurations, the inductor L_{B1} is used to reduce the input current ripple. Note in *Non-Isolated Interleaved TPTLC* and *Floated Non-Isolated TPTLC*, the function of the inductor L_{B2} is similar to that of the inductor L_{B1}. Regarding the role of the inductor L_{B2} in other non-isolated converters, it transfers the power from the input stage to the output stage. As far as the current ripple is concerned, an interleaved TPTLC is an excellent solution to reduce the current ripple while improving the power density, which is constructed by symmetric connection of two ABHB modules at the low-voltage side (LVS) of TPTLCs. For example, in nonisolated interleaved TPTLC and isolated interleaved TPTLC, the phase legs operate in an interleaving way such that each of the phase-leg only handles a portion of the total power. As depicted in Table 3.1, an effective way to decrease the voltage stress of semiconductors and increase the voltage gain is to cascade the ABHB modules with a merit of minimum components count. In order to remove the disadvantages of multilevel converters, i.e., sizeable current spike and no voltage regulation, a “Multilevel Modular TPTLC” is derived from the conventional switched-capacitor converter. To

improve the power density, the proposed multilevel modular TPTLC employs the switched-capacitor concept to increase the voltage gain without using a transformer, while the major issues of the multilevel switched-capacitor converter are solved by using a small inductor. Moreover, the bidirectional power transferring is realized in this converter by transferring the energy between adjacent serial capacitors. Taking the stacked TPTLC as an example, the detailed analyses of its performance and characteristics are studied in the next section.

As shown in Table **3**.**2**, with a high-frequency transformer, the partially-isolated TPTLCs are appropriate for applications featuring isolation and high voltage gain. At the output side of the TPTLCs topologies, three-level rectifier based on the ABHB modules are used to decrease the voltage stress across switches while increasing the voltage gain. To hybridize two different type of input sources, i.e., current-fed and voltage-fed source, a full-bridge converter can be paralleled with a half-bridge converter by adopting a mutual dc-bus, named *Integrated Half-Bridge TPTLC*. This type of TPTLC is beneficial for hybrid renewable energy systems. The idea of "*Hybrid Half-Bridge and Full-Bridge TPTLC*" stems from the fact that the PWM pattern of both full-bridge and half-bridge converters are identical. To avoid transformer saturation caused by an asymmetrical operation in the full-bridge circuit, the dc-blocking capacitor C_b is added in series with the primary winding of transformer T_2. The capacitors in the secondary side fulfill this duty in the other converters. The inductance L_{B1} in *Full-Bridge TPTLC* and both inductance L_{B1} and L_{B2} in *Integrated Half-Bridge TPTLC* can be directly integrated into the transformer in the form of its leakage inductance.

3.3 Detailed Analysis and Design Consideration of the Stacked TPTLC

In this section, the proposed stacked TPTLC is thoroughly studied. Stacking structure such as that depicted in Figure **3.2** aims at improving the efficiency and voltage gain without requiring any transformer. The clamp circuit limits the voltage stress of switches; hence switches with smaller on-resistance $R_{DS(ON)}$ can be used, leading to lower conduction loss. Compared to other TPTLCs, stacked TPTLC needs less number of switches and inductors to achieve high voltage gain and offers the soft-switching for a wide range of power. Symbols are defined as follows: filter inductors L_{B1}, L_{B2}, power switches S_1, S_2, S_3, S_4, auxiliary capacitor C_{aux}, clamp capacitor C_C, and output capacitor C_O. V_{out} denotes the voltage of high-voltage port, which is equal to the summation of the voltage of clamp capacitor and the output capacitor, $V_{Cc}+V_{Co}$. In Figure **3.2**, the battery is emulated by a voltage source V_{BT}. In this figure, the fuel cell is modeled as an ideal voltage source V_{FC}. Since the FC cannot be charged, a diode D_{FC} is used in series with voltage source V_{FC}.

Also, R_{out} is the equivalent resistance of load representing the equivalent power feeding an inverter. The voltage across switches S_2 and S_3 are symbolized by V_{ab} and V_{cb}, respectively. The inductor L_{B1} is adopted as a filter to reduce the battery current ripple, and the inductor L_{B2} is used to form a resonant circuit to realize ZVS performance and confine the peak current of switches. While no extra voltage stress is added across the switches, an auxiliary capacitor is added to the circuit to extend the range of soft-switching performance, which forms a resonant tank with the inductor L_{B2}. This auxiliary capacitor stores the magnetic energy of inductor L_{B2} and then releases it to the output capacitor C_o. The main switches S_1 and S_3 can transfer the power from FC to the battery and the load, respectively. The gate pulse of switches S_2 and S_4 are complementary to that of switches S_1 and S_3, respectively.

Table 3.1: Non-isolated three-port three-level DC/DC converters comprised of ABHB modules.

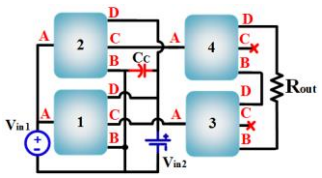
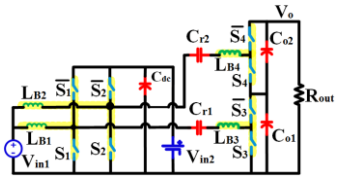
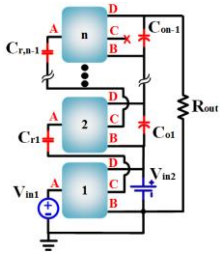
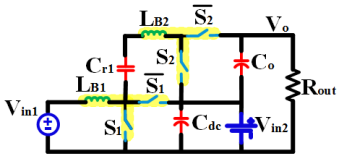
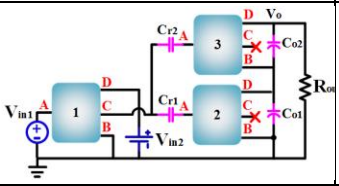
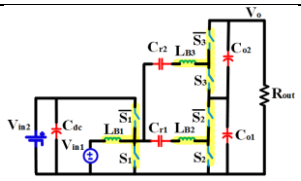
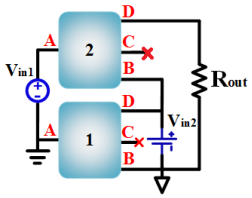
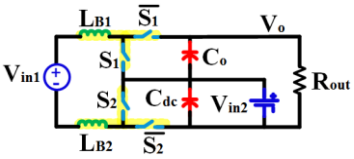
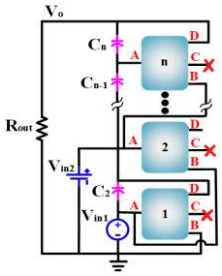
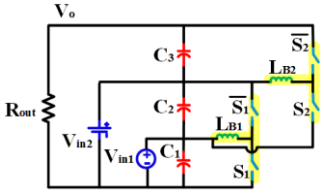
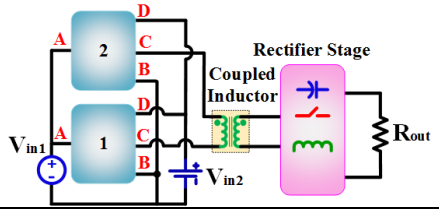
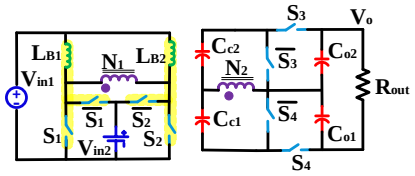
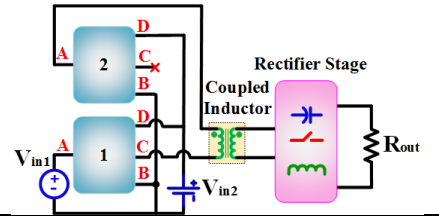
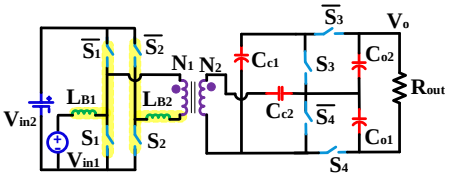
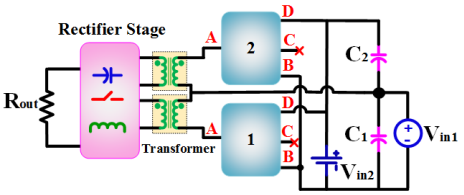
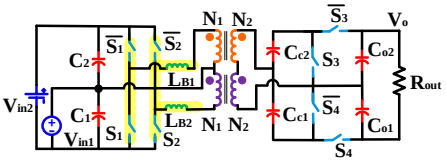
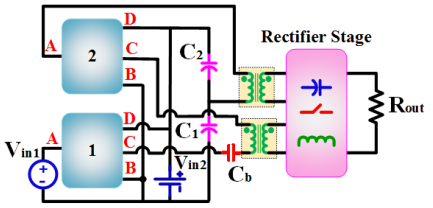
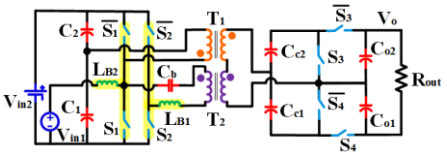
Topology	General Model	Example
Nonisolated Interleaved TPTLC		
Stacked TPTLC		
Cascaded TPTLC		
Floated non-isolated TPTLC		
Multi-level Modular TPTLC		

Table 3.2: Partially-isolated three-port three-level DC/DC converters derived from ABHB modules.

Topology	General Model	Example
Isolated Interleaved TPTLC		
Full-Bridge TPTLC		
Integrated Half-Bridge TPTLC		
Hybrid Half-Bridge and Full-Bridge TPTLC		

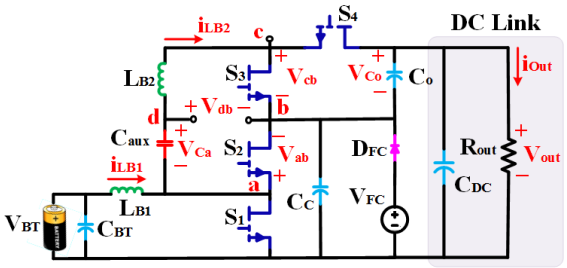


Figure 3.2: Proposed stacked TPTLC for FCEV applications.

3.3.1 Operation Modes Analysis

Based on the generated power of FC and the power demanded by the load, possible scenarios of power flow in different ports include: 1) Scenario I, when the power of FC is not enough to supply the load. 2) Scenario II, when the generated power of FC P_{FC} is more than the power demand, i.e.,$P_{FC} > P_{out}$; so, the battery absorbs the extra power generated by FC so that the output voltage is regulated at a constant value. 3) Scenario III, when the battery can be charged from the motor through an inverter during decelerating, which is named also regenerative-braking scenario. 4) Scenario IV, when the load is disconnected, i.e.,$P_{out} = 0$, and the battery is charged by the generated power of FC.

The operating principle and characteristics of proposed converter are demonstrated with the following assumptions: 1) the capacitors C_C, C_O, C_{aux} are sufficiently large such that they can be taken as constant voltage sources; 2) All switches S_1-S_4 are considered to be ideal.

1) Scenario I: In this scenario, the FC cannot meet the load power demand, i.e.,$\boldsymbol{P_{FC} < P_{out}}$, the converter operates as a double-input converter. In this condition, the battery is discharged and helps to supply the load so that the output voltage is controlled at a constant value. According to the assumptions, the proposed converter operation during one switching period can be divided into four intervals. The corresponding equivalent circuits and the key waveforms during one switching period are depicted in Figure 3.3.

Interval I [t_0-t_1]: At time t_0, switches S_1 and S_4 are on, and the battery current is going through the inductor L_{B1}; so, the inductor is being charged. Figure 3.3 (a) illustrates the current flow path for this interval. The voltage across inductor L_{B2} is negative, therefore its current decreases linearly, demonstrated in Figure **3.4**. As a result of adopting active-

clamped circuit, the voltage stress of switches S_2 and S_3 are limited to the voltage of capacitors C_C and C_O, respectively.

$$\begin{cases} L_{B1}\dfrac{di_{LB1}}{dt} = v_{BT} \\ L_{B2}\dfrac{di_{LB2}}{dt} = v_{Ca} - v_{Cc} - v_{Co} \\ C_a\dfrac{dv_{ca}}{dt} = -i_{LB2} \\ C_c\dfrac{dv_{Cc}}{dt} = i_{LB2} - \dfrac{v_{Cc} + v_{Co}}{R_o} \\ C_o\dfrac{dv_{Co}}{dt} = i_{LB2} - \dfrac{v_{Cc} + v_{Co}}{R_o} \end{cases} \quad (3\text{-}1)$$

Interval II [t_1-t_2]: At time t_1, switch S_4 is turned off and S_3 is turned on. The current flow path for this interval is depicted in Figure 3.3 (b). As shown in Figure **3.4**, the current of inductor L_{B1} increases, but the current of L_{B2} changes depending on the voltage of V_{Cc} and V_{Ca}**.**

$$\begin{cases} L_{B1}\dfrac{di_{LB1}}{dt} = v_{BT} \\ L_{B2}\dfrac{di_{LB2}}{dt} = v_{Ca} - v_{Cc} \\ C_a\dfrac{dv_{Ca}}{dt} = -i_{LB2} \\ C_c\dfrac{dv_{Cc}}{dt} = i_{LB2} - \dfrac{v_{Cc} + v_{Co}}{R_o} \\ C_o\dfrac{dv_{Co}}{dt} = -\dfrac{v_{Cc} + v_{Co}}{R_o} \end{cases} \quad (3\text{-}2)$$

Interval III [t_2-t_3]: At time t_2, switches S_1 is off and S_2 is on. Figure 3.3 (c) shows the current flow path for this interval. The current of inductor L_{B1} and L_{B2} decreases and increases linearly, respectively.

$$\begin{cases} L_{B1}\dfrac{di_{LB1}}{dt} = v_{BT} - v_{Cc} \\ L_{B2}\dfrac{di_{LB2}}{dt} = v_{Ca} \\ C_a\dfrac{dv_{Ca}}{dt} = -i_{LB2} \\ C_c\dfrac{dv_{Cc}}{dt} = i_{LB1} - \dfrac{v_{Cc}+v_{Co}}{R_o} \\ C_o\dfrac{dv_{Co}}{dt} = -\dfrac{v_{Cc}+v_{Co}}{R_o} \end{cases} \tag{3-3}$$

Interval IV [t_3-t_4]: At time t_3, switches S_3 is turned off and S_4 is turned on. Figure 3.3 (d) shows the current flow path for this interval. The current waveform of inductor L_{B2} varies depending on the voltage of V_{Cc} and V_{Ca}. As shown in Figure **3.4**, for the equal value of V_{Cc} and V_{Ca}, the current will be "flat".

$$\begin{cases} L_{B1}\dfrac{di_{LB1}}{dt} = v_{BT} - v_{Cc} \\ L_{B2}\dfrac{di_{LB2}}{dt} = v_{Ca} - v_{Co} \\ C_a\dfrac{dv_{Ca}}{dt} = -i_{LB2} \\ C_c\dfrac{dv_{Cc}}{dt} = i_{LB1} - \dfrac{v_{Cc}+v_{Co}}{R_o} \\ C_o\dfrac{dv_{Co}}{dt} = i_{LB2} - \dfrac{v_{Cc}+v_{Co}}{R_o} \end{cases} \tag{3-4}$$

2) Scenario II: During this scenario, the generated power of FC is more than the load demand, so the battery is charged by the extra power. The converter works as a dual-output converter in this condition. The operation intervals and the equivalent circuits are similar to those in scenario I, except the inductor current i_{LB1} is different. Figure 3.5 shows the inductor current i_{LB1} for scenarios I and II according to the generated power of FC P_{FC} and load power P_{out}.

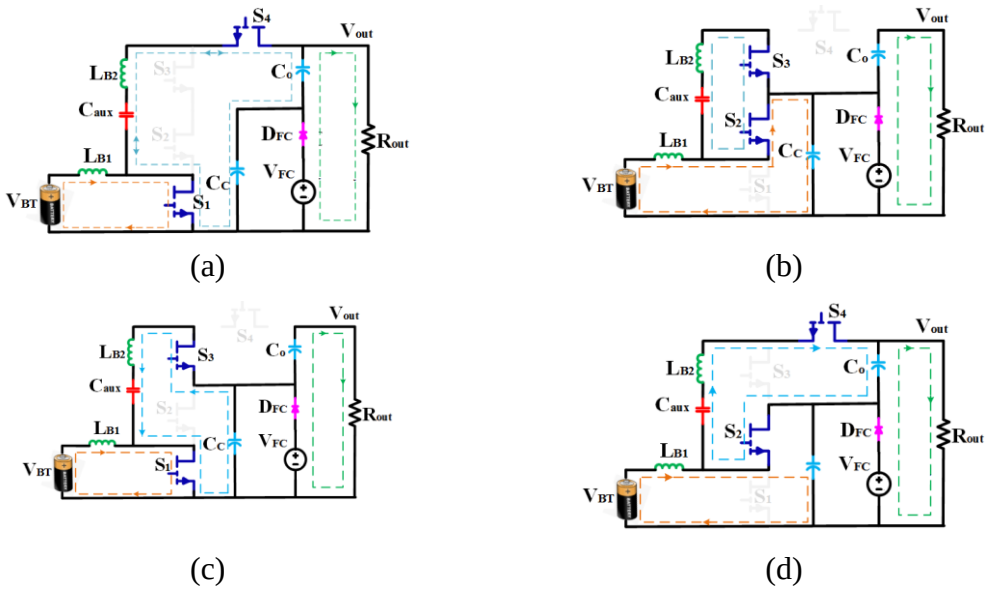


Figure 3.3: Equivalent circuits and key waveforms for scenario I. (a) Interval I. (b) Interval II. (c) Interval III. (d) Interval IV. (e) Key waveforms.

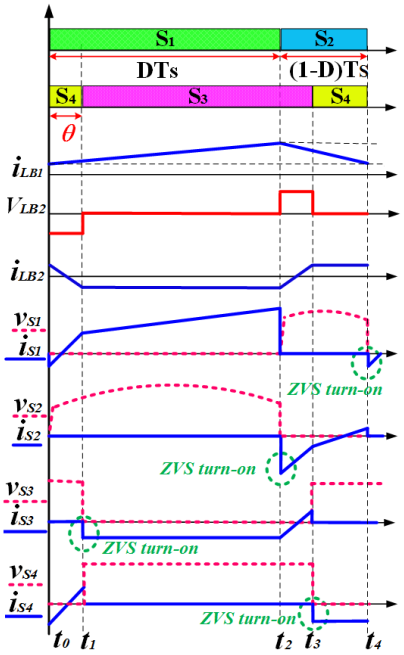


Figure 3.4: Key waveforms.

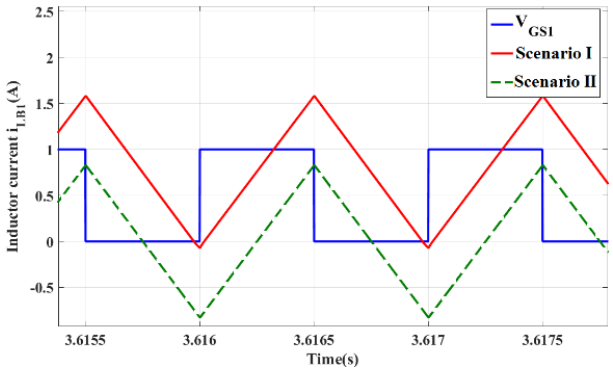
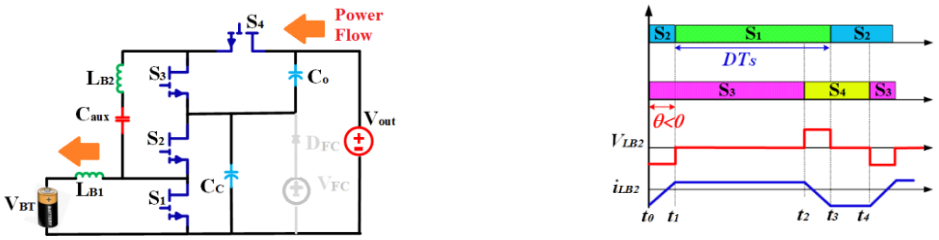


Figure 3.5: The inductor current i_{LB1} for scenarios I ($P_{FC} < P_{out}$) and II ($P_{FC} > P_{out}$).

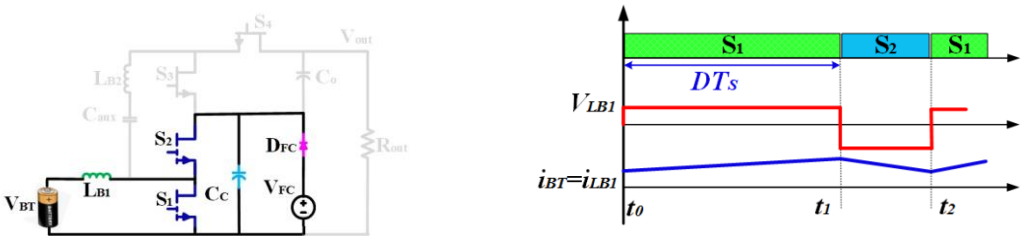
3) Scenario III: In this scenario, the motor charges the battery through an inverter, which is also named regenerative braking scenario. Whereas in the scenario I, the gate pulse of switch S_1 leads that of switch S_3, in this scenario the gate pulse of switch S_1 lags that of switch S_3 to control the power flow in the reverse direction, which means the phase shift ratio, θ, is negative. The equivalent circuit and the key waveforms in this scenario are depicted in Figure 3.6 (a) and (b), respectively. As shown in Figure 3.6 (a), the power flows from high-voltage side (HVS) to the battery in this scenario. The operation intervals in this scenario are similar to those in the scenario I with a different sequence of operation intervals. As shown in Figure 3.6 (b), the sequence of switching states in a switching period can be expressed as S_2S_3, S_1S_3, S_1S_4, and S_2S_4.



(a) (b)

Figure 3.6: Equivalent circuit and key waveforms of converter in scenario III. (a) Equivalent circuit. (b) Key waveforms.

4) Scenario IV: In this scenario, the load is disconnected, and the generated power of FC charges only the battery. The principle of operation of the converter in this scenario is similar to that of a conventional ABHB converter. The switches S_1 and S_2 are driven complementary, and other switches are turned off. There are two intervals in one switching period. The equivalent circuit of the proposed converter during scenario IV is depicted in Figure 3.7 (a). The gate-pulse of switches S_1 and S_2 and the current of the battery are depicted in Figure 3.7 (b).



(a) (b)

Figure 3.7: Equivalent circuit and key waveforms of the proposed converter in scenario IV. (a) Equivalent circuit. (b) key waveforms.

3.3.2 Voltage Conversion Ratio

As shown in Figure **3.2**, in the proposed stacked TPTLC two switches S_1 and S_3 share the gate-control signals with the same duty-cycle D but a phase-shift ratio θ, which are complementary to gate-control signals of S_2 and S_4, respectively. From assumptions as mentioned earlier in Section A, the relation between the voltage of HVS port and LVS port in different scenarios can be obtained. From Figure 3.2, it is apparent that the output voltage is equal to the summation of the voltage of capacitors C_C and C_O.

$$V_{out} = V_{FC} + V_{Co} \tag{3-5}$$

By applying the volt-sec balance on the inductor L_{B1}, V_{FC} can be expressed by

$$V_{FC} = \frac{V_{BT}}{1 - D} \tag{3-6}$$

Based on the circuit shown in Figure **3.2**, an equivalent circuit of the HVS of proposed stacked TPTLC is obtained, as shown in Figure **3.8**, which helps to derive the relation between V_{db} and the voltage across capacitor Co. From Figure **3.8** and the volt-sec balance on the inductor L_{B2}, V_{Co} can be obtained by

$$V_{Co} = \frac{V_{db}}{1 - D} \tag{3-7}$$

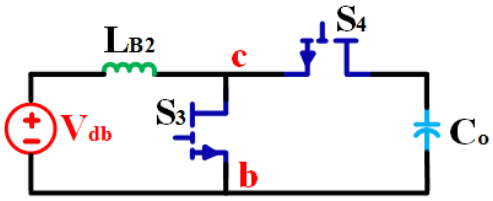


Figure 3.8: Equivalent circuit of HVS of proposed stacked TPTLC.

From Figure **3.2** and voltage-second balance principle across the inductor, the relation of voltages on two side of inductor L_{B1} can be defined as follows:

$$V_{BT} + V_{Ca} = V_{db} + V_{FC} \tag{3-8}$$

From (5) – (8), the output voltage V_{out} can be calculated as follows:

$$V_{out} = \frac{2V_{BT}}{1 - D} + \frac{V_{Ca} - V_{FC}}{1 - D} \tag{3-9}$$

From current-second balance principle on the capacitor C_{aux}, the relationship between the inductor current i_{LB2} at t_0 and t_3 can be derived by

$$\int_0^{T_s} i_{Ca}(t)dt = \int_0^{T_s} i_{LB2}(t)dt = 0 \tag{3-10}$$

$$i_{LB2}(t_0)(1-D)T_S + i_{LB2}(t_3)DT_S = 0 \tag{3-11}$$

From operation modes and Figure **3.3** (a), the inductor current i_{LB2} at t_3 can be expressed by

$$i_{LB2}(t_3) = i_{LB2}(t_0) - \frac{V_{Co} + V_{FC} - V_{Ca}}{L_{B2}}\theta T_S \tag{3-12}$$

From current-second balance principle on the capacitor C_O, the average current of switch S_4 can be written by

$$\int_0^{T_s} i_{S4}(t)dt = I_{out} = \frac{V_{out}}{R_{out}} \tag{3-13}$$

Substituting for i_{LB2} from (10) – (11) into (13) and integrating the result, the output voltage can be expressed by

$$V_{out} = \frac{(2\theta D - 2\theta D^2 - \theta^2 - 4\theta D^2 + 4\theta D^3 + 2D\theta^2)R_{out}T_S}{2L_{B2} - (2\theta D^2 - 2\theta D^3 - \theta^2 D)R_{out}T_S}V_{FC} \tag{3-14}$$

3.3.3 Analysis of Inductor Current and Transferred Power

In order to keep the output voltage regulated and control the power flow, the PPSM scheme is proposed for the proposed stacked TPTLC. Firstly, the relationship of transferred power with the phase-shift ratio (θ) and duty cycle (D) needs to be derived. As illustrated in Figure 3.9, depending on the values of D and θ, there are eight possible operating cases: 1) case I, when $\theta < 1 - D < 0.5$; 2) case II, when $1 - D < \theta < 0.5$; 3) case III, when $\theta < D < 0.5$; 4) case IV, when $D < \theta < 0.5$. In Figure 3.9, "Scenario I" represents the power flow from low-voltage side to high-voltage side, which is defined as Forward operation, i.e., P>0 and $\theta > 0$. In Backward operation, P<0 and $\theta < 0$, which is defined as in "Scenario III" in Figure 3.9, the power the power flows from high-voltage side to low-voltage side.

Note Cases I-IV in Scenario III are represented with prime values, named cases I'-IV'. For instance, I represents *Case I* in *Scenario I*, while I' represents *Case I* in *Scenario III*.

Case 1 [θ < (1-D) < 0.5] [see Figure 3.10 (a)]:

The key waveforms for this case are shown in Figure 3.10 (a). From (10)-(14) and the current-second balance principle on the capacitors C_{aux} and C_o, the output power can be calculated by

$$P = \frac{V_{out}^2 T_S}{4L_{B2}}(2D - 2D^2 - |\theta|)|\theta| \tag{3-15}$$

From (15) it is obvious that the transferred power is inversely related to the switching frequency f_s and inductance L_{B2}. The maximum power can be obtained at the maximum phase-shift ratio (θ_{max}) as follows:

$$\frac{dP}{d|\theta|} = \frac{V_{out}^2 T_S}{4L_{B2}}(2D - 2D^2 - 2|\theta_{max}|) = 0 \tag{3-16}$$

$$|\theta_{max}| = D - D^2 \tag{3-17}$$

$$P_{max} = \frac{V_{out}^2 T_S}{4L_{B2}}(D - D^2)^2 \tag{3-18}$$

The maximum transferred power as a function of switching frequency f_s and inductance L_{B2} is presented in Figure 3.10 (a), demonstrating the effect of the switching frequency and the inductance L_{B2} on the maximum transferred power P_{max}, which is derived from the equation (18) when V_{out}= 400 V and D=0.5. As shown in this figure, the maximum transferred power increases exponentially if the inductance L_{B2} decreases below 1uH. It can be seen that the maximum transferred power decreases with increase of either the switching frequency or inductance.

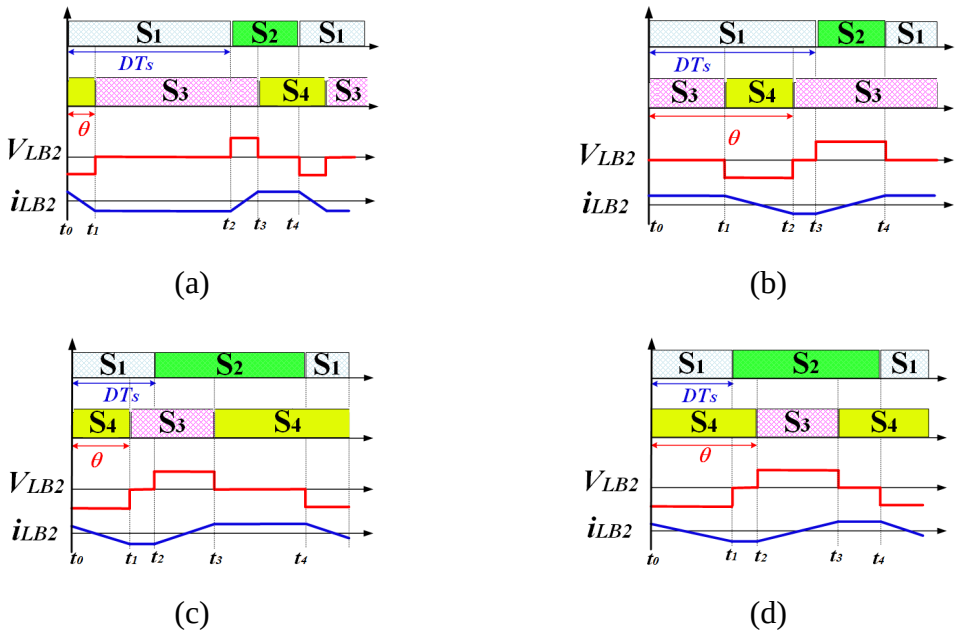


Figure 3.9: Different operation modes according to different values of duty-cycle and phase shift ratio. (a) Case 1. (b) Case 2. (c) Case 3. (d) Case 4.

Case 2 [(1-D) < θ < 0.5] [see Figure 3.10 (b)]:

Figure 3.10 (b) shows the current and voltage waveforms for operating case 2. Employing the similar derivation procedure, the output power can be obtained by

$$P = \frac{V_{out}^2 T_S}{4L_{B2}}(1-D)^2(1-2|\theta|) \tag{3-19}$$

Case 3 [θ < D < 0.5] [see Figure 3.10 (c)]:

The current and voltage waveforms for this case are depicted in Figure 3.10 (c).

With the same analysis method, the output power in this case is completely similar to *Case 1*, which is a function of the phase-shift ratio (θ) and duty cycle (D) and can be determined by

$$P = \frac{V_{out}^2 T_S}{4L_{B2}}(2D-2D^2-|\theta|)|\theta| \tag{3-20}$$

Case 4 [D < θ < 0.5] [see Figure 3.10 (d)]:

The key waveforms for this case are shown in Figure 3.10 (d). Applying the similar mathematical derivation, the output power is a function of the phase-shift ratio (θ) and duty cycle (D), which is given by

$$P = \frac{V_{out}^2 T_S}{4L_{B2}} D^2(1 - 2|\theta|) \tag{3-21}$$

Figure 3.11 (b) shows the normalized delivered power as function of duty cycle and phase-shift ratio for different operation modes, in which the transferred power is normalized by

$$P_{base} = \frac{V_{out}^2 T_S}{4L_{B2}} \tag{3-22}$$

Note the negative power refers to a power flowing from HVS to LVS. As depicted in Figure 3.11 (b), the direction of power flow can be changed seamlessly because the proposed converter has a unified operation for various values of phase-shift ratio; so, similar equations are valid for a negative phase-shift ratio. It is important to note that zero delivered power does not imply zero current. In essence, when the phase-shift ratio is zero (θ=0), there is reactive power going through the switches contributing to the power losses. Further examinations show that the transferred power curve is symmetric around the axis D=0.5, and it enhances with the rise of the duty cycle (D) for D ≤ 0.5 and the decrease of D for D > 0.5. The transferred power curve when the duty cycle is fixed is analogous to the sinusoidal wave. The maximum transferred power in Scenario I and Scenario III are identical to each other, happening at D=0.5 and θ = ±0.25.

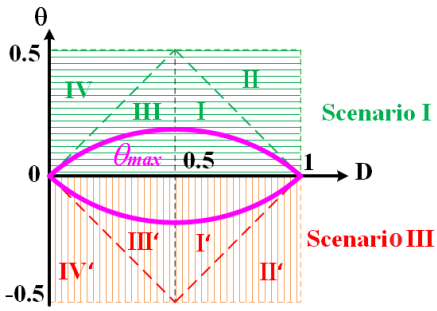
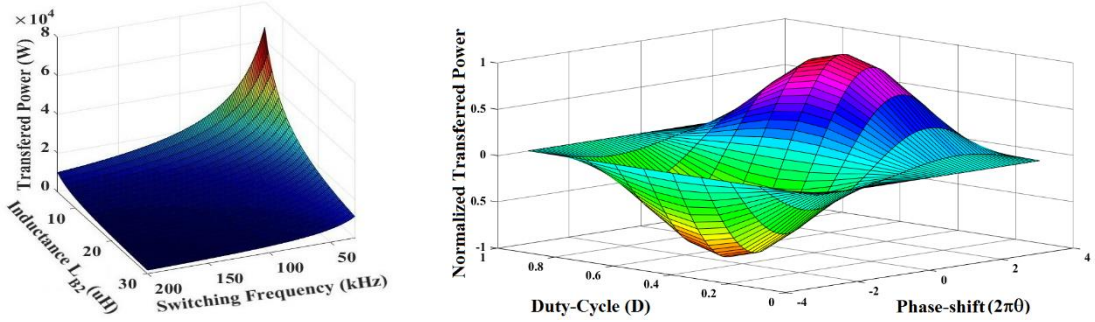


Figure 3.10: Operating cases for different values of phase shift ratio θ versus duty-cycle D.



(a) **(b)**

Figure 3.11: Maximum power transferred and normalized transferred output power; (a) Maximum power transferred as a function of switching frequency f_s and inductance L_{B2}. (b) Normalized power transferred versus different phase-shift ratio and duty cycle.

3.3.4 Current and Voltage Stress of Switches

In order to calculate the current stress of switches, first, the current of inductor L_{B2}, i_{LB2}, should be thoroughly analyzed. From the explanation given in "Operation Mode Analysis" section, the inductor current i_{LB2} can be calculated, which is given in Table 3.3. It can be seen that the inductor current is a function of phase shift ratio θ and duty cycle D, indicating that any change in operation point can lead to a change of the peak current and RMS current of switches. Therefore, the determination of a proper phase-shift ratio and the duty cycle is

vital in minimizing the switching and conduction losses. The root-mean-square (RMS) current of inductor L_{B2} for different operating cases is given in Table **3.4**.

Table 3.3: Current of inductor L_{B2} for different values of duty cycle and phase-shift ratio.

Condition	$\|\theta\| < (1-D) < 0.5$	$(1-D) < \|\theta\| < 0.5$	$\|\theta\| < D < 0.5$	$D < \|\theta\| < 0.5$
$i_{LB2}(t=t_0\text{-}t_1)$	$\frac{V_{out}T_s}{2L_{B2}}(\theta\mathrm{D} - \frac{t}{T_s})$	$\frac{V_{out}T_s}{2L_{B2}}(1 - \theta)(1-D)$	$\frac{V_{out}T_s}{2L_{B2}}(\theta\mathrm{D} - \frac{t}{T_s})$	$\frac{V_{out}T_s}{2L_{B2}}(\theta\mathrm{D} - \frac{t}{T_s})$
$i_{LB2}(t=t_1\text{-}t_2)$	$-\frac{V_{out}T_s}{2L_{B2}}\theta(1-D)$	$\frac{V_{out}T_s}{2L_{B2}}(\theta\mathrm{D} - \frac{t}{T_s})$	$\frac{V_{out}T_s}{2L_{B2}}(\theta\mathrm{D} - \frac{t}{T_s})$	$-\frac{V_{out}T_s}{2L_{B2}}D(1-\theta)$
$i_{LB2}(t=t_2\text{-}t_3)$	$\frac{V_{out}T_s}{2L_{B2}}[-\theta(1-D) - D + \frac{t}{T_s}]$	$-\frac{V_{out}T_s}{2L_{B2}}\theta(1-D)$	$\frac{V_{out}T_s}{2L_{B2}}[-\theta(1-D) - D + \frac{t}{T_s}]$	$\frac{V_{out}T_s}{2L_{B2}}[-D(1-\theta) - \theta + \frac{t}{T_s}]$
$i_{LB2}(t=t_3\text{-}t_4)$	$\frac{V_{out}T_s}{2L_{B2}}\theta D$	$\frac{V_{out}T_s}{2L_{B2}}[-\theta(1-D) - D + \frac{t}{T_s}]$	$\frac{V_{out}T_s}{2L_{B2}}\theta D$	$\frac{V_{out}T_s}{2L_{B2}}\theta D$

Figure 3.12 shows the normalized RMS current for different values of duty cycle and phase-shift ratio, in which the base inductor current i_{LB2}, named $I_{LB2,base}$, is defined as follows:

$$i_{LB2,base} = \frac{V_{out}T_S}{L_{B2}} \tag{3-23}$$

From the inductor current i_{LB2} given in Table **3.4**, the maximum current of switches can be expressed as follows:

$$\begin{aligned} i_{s1,max} &= i_{LB1}(t_2) - i_{LB2}(t_2) \\ &= \frac{V_{out}T_s}{2L_{B2}}\frac{\theta(1-\mathrm{D}^2-\theta)}{1-D} + \frac{V_{out}T_s}{2L_{B1}}\frac{(1-D)D}{2} \end{aligned} \tag{3-24}$$

$$i_{s2,max} = -i_{LB1}(t_4) + i_{LB2}(t_4)$$
$$= \frac{V_{out}T_s}{2L_{B2}}\frac{\theta(\mathrm{D}^2 - \mathrm{D} + \theta)}{1-D} + \frac{V_{out}T_s}{2L_{B1}}\frac{(1-D)D}{2} \quad (3\text{-}25)$$

$$i_{s3,max} = i_{LB2}(t_3) = \frac{V_{out}T_s}{2L_{B2}}\theta D \quad (3\text{-}26)$$

$$i_{s4,max} = -i_{LB2}(t_0) = \frac{V_{out}T_s}{2L_{B2}}\theta \mathrm{D} \quad (3\text{-}27)$$

Table 3.4: RMS Current of inductor LB2 for different operating cases.

Operating Case	**Condition**	**RMS Current of inductor L_{B2}**
Case 1	$\lvert\theta\rvert < (1-D) < 0.5$	$I_{LB2,rms} = \frac{V_{out}T_s}{2L_{B2}}\sqrt{\frac{\theta^2(3D - 3D^2 - \theta)}{3}}$
Case 2	$(1-D) < \lvert\theta\rvert < 0.5$	$I_{LB2,rms} = \frac{V_{out}T_s}{2L_{B2}}\sqrt{\frac{(1-D)^2(3\theta - 3\theta^2 + D - 1)}{3}}$
Case 3	$\lvert\theta\rvert < D < 0.5$	$I_{LB2,rms} = \frac{V_{out}T_s}{2L_{B2}}\sqrt{\frac{\theta^2(3D - 3D^2 - \theta)}{3}}$
Case 4	$D < \lvert\theta\rvert < 0.5$	$I_{LB2,rms} = \frac{V_{out}T_s}{2L_{B2}}\sqrt{\frac{D^2(3\theta - 3\theta^2 - D)}{3}}$

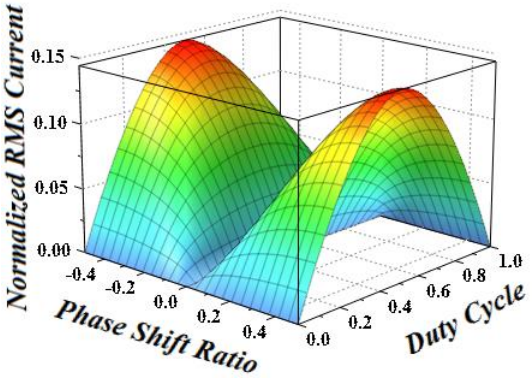


Figure 3.12: Normalized RMS current versus different phase-shift ratio and duty cycle.

From Figure **3.3**, it is apparent that the LVS and the HVS switches should withstand the voltage of clamp capacitor V_{Cc} and V_{Co}, respectively. Therefore, the voltage stress of power switches can be obtained from Figure **3.3** and (6) as follows:

$$V_{s1} = V_{s2} = V_{Cc} = \frac{V_{BT}}{1 - D} \tag{3-28}$$

$$V_{s3} = V_{s4} = V_{out} - V_{Cc} \tag{3-29}$$

3.3.5 ZVS Performance

Aside from the conduction loss, the switching loss is another concern to find the high-efficiency operation region. ZVS soft-switching performance can be realized owing to the PPSM control algorithm. As discussed in section B, case 1 is recognized as the low inductance current region, which can be seen in Figure **3.13**. In this part, the soft switching performance in this region during scenario I is discussed. Note the ZVS soft-switching performance in the scenario I is quite similar to that in scenario II, III, IV, and V. The results and analytical procedure derived in this section are valid for the proposed converter regardless of the operation modes.

The conditions to obtain ZVS performance of switches S_1-S_4 can be expressed by

$$i_{s1}(t_0) = (i_{LB1}(t_0) - \frac{V_{out}T_s}{2L_{B2}}\theta\mathrm{D}) < 0 \tag{3-30}$$

$$i_{s2}(t_2) = (i_{LB1}(t_2) - \frac{V_{out}T_s}{2L_{B2}}\theta(1 - \mathrm{D})) > 0 \tag{3-31}$$

$$i_{s3}(t_1) = (-\frac{V_{out}T_s}{2L_{B2}}\theta(1 - \mathrm{D})) < 0 \tag{3-32}$$

$$i_{s4}(t_3) = (\frac{V_{out}T_s}{2L_{B2}}\theta\mathrm{D}) > 0 \tag{3-33}$$

The maximum and minimum inductor current i_{LB1} happens at t_0 and t_2, respectively, which can be calculated by

$$i_{LB1}(t_0) = \frac{P_{BT}}{V_{BT}} - \frac{V_{BT}DT_s}{2L_{B1}} = \frac{V_{out}T_s}{2L_{B2}}\frac{\theta(2\mathrm{D} - 2\mathrm{D}^2 - \theta)}{1-D} - \frac{V_{BT}DT_s}{2L_{B1}} \tag{3-34}$$

$$i_{LB1}(t_2) = \frac{P_{BT}}{V_{BT}} + \frac{V_{BT}DT_s}{2L_{B1}} = \frac{V_{out}T_s}{2L_{B2}}\frac{\theta(2\mathrm{D} - 2\mathrm{D}^2 - \theta)}{1-D} + \frac{V_{BT}DT_s}{2L_{B1}} \tag{3-35}$$

According to (30), (31), (34), and (35), the soft-switching condition of switches S_1 and S_2 is more rigorous than that of switches S_3 and S_4 due to the DC current injection of the inductor L_{B1}. Thus, ZVS turn-on performance of all switches can be satisfied once the following conditions are met.

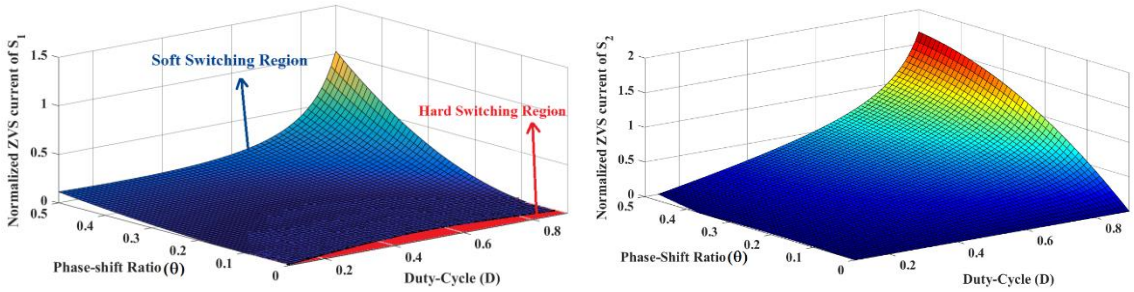
$$i_{s1}(t_0) = \frac{V_{out}T_s}{2L_{B2}}\frac{\theta(D - D^2 - \theta)}{1-\mathrm{D}} - \frac{V_{BT}DT_s}{2L_{B1}} < 0 \tag{3-36}$$

$$i_{s2}(t_2) = \frac{V_{out}T_s}{2L_{B2}}\frac{\theta(4D - 3D^2 - \theta)}{1-\mathrm{D}} > 0 \tag{3-37}$$

From (36) and (37), it is apparent that the ZVS performance depends on the duty cycle, the phase-shift ratio, the output voltage, the inductor L_{B2}, and switching frequency. Defining the base ZVS current $I_{ZVS,base}$ as $(V_{out}*T_s)/L_{B2}$, Figure 3.13 (a) and (b) show the normalized ZVS current of switches S_1 and S_2, respectively. Note since the inductor L_{B1} is employed to filter the input current ripple, it is assumed that the inductor L_{B1} is larger than the inductor L_{B2}, so L_{B1}= 10 L_{B2}. Another condition to achieve the ZVS performance is that the energy stored in the inductance L_{B2} should discharge the output capacitor of switch S_1 to zero. Thus, the detailed ZVS condition of switch S_1 can be derived as:

$$(i_{LB2}(t_0))^2 > \frac{2C_{oss}V_{Cc}^2}{L_{B2}} + (i_{LB1}(t_0))^2 \tag{3-38}$$

It can be seen that that the larger inductance L_{B2} and the smaller battery power P_{BT}, the easier switch S_1 can obtain ZVS. As a conclusion, ZVS can be implemented for all the switches for a wide operating range in this mode. It is noteworthy that the soft-switching performance of switches in other modes can be ensured similarly.



(a) (b)

Figure 3.13: Normalized ZVS current of switches versus different phase-shift ratio and duty cycle. (a) Switch S_1. (b) Switch S_2.

3.3.6 Passive Component Selection

In this section, the design guide to choosing the inductors L_{B1} and L_{B2}, and capacitors C_{aux}, C_{BT}, C_O, and C_C are illustrated. The inductor L_{B1} works as a filter in the boost converter to limit the battery current ripple, so it can be obtained as follows:

$$L_{B1} = \frac{DT_S V_{BT}}{(\Delta I_{LB1})} \tag{3-39}$$

The design of inductor L_{B2} is of paramount importance for the proposed converter since it plays a critical role in the soft switching, the conduction losses, and the maximum transferred power; so, more attention should be given to its selection. According to (36) and (38), to realize the soft switching, the inductor L_{B2} should meet the following conditions:

$$L_{B2} > \frac{\theta(D - D^2 - \theta)V_{out}}{(1 - \mathrm{D})\mathrm{D}V_{BT}} L_{B1} \tag{3-40}$$

$$L_{B2} > \frac{2C_{oss}V_{Cc}^2}{\frac{V_{out}T_S\theta^2}{2L_{B2}}\left(D^2 - \left(\frac{(2\mathrm{D} - 2\mathrm{D}^2 - \theta)}{1 - D} - \frac{DL_{B2}}{\theta L_{B1}}\right)^2\right)} \tag{3-41}$$

It can be understood that the larger inductance L_{B2} is selected, the more possible soft-switched turn-on operation can be realized. Nevertheless, according to (18), increasing L_{B2} shrinks the maximum transferred power.

Regarding the design of capacitors, it is assumed that the capacitors serve as a dc voltage source and the voltage ripple on the capacitors should be limited in a reasonable range. The capacitors can be determined by

$$C_O > \frac{V_{out}DT_S}{R_{out}\Delta V_{Co}} \tag{3-42}$$

$$C_C > \frac{V_{out}(1 + D)T_S}{(1 - D)R_{out}\Delta V_{Cc}} \tag{3-43}$$

$$C_{aux} > \frac{V_{out}T_S}{R_{out}\Delta V_{Caux}} \tag{3-44}$$

$$C_{BT} > \frac{\Delta I_{BT}T_S}{8\Delta V_{BT,pp}} \tag{3-45}$$

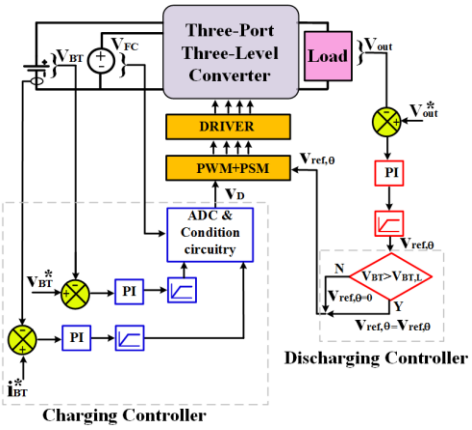
Where T_S is the switching period, ΔV_{Co} is the voltage ripple on capacitor C_O, ΔV_{Cc} is the voltage ripple on capacitor C_C, $\Delta V_{BT,pp}$ is the voltage battery ripple, ΔV_{Caux} is the voltage ripple on capacitor C_{aux}, ΔI_{BT} is the ripple current of the battery.

3.3.7 Control Scheme

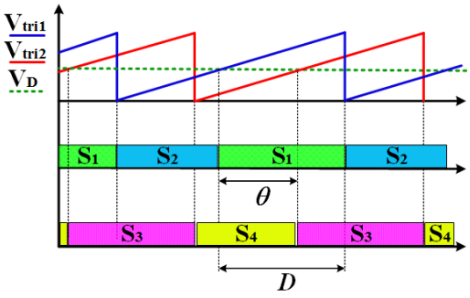
As previously discussed, keeping the balance between the battery and FC while maximizing the utilization of FC power is the main aim of the power management of the proposed FC-battery system. The block diagram of designed control scheme is depicted in

Figure **3.14** (a), including battery charging and discharging control and load voltage control. As exhibited in Figure **3.14** (b), utri1 and u_{tri2} represent the two carrier signals, D is the duty-cycle of switches S_1 and S_3 and regulated by control voltage V_D, and θ is the phase shift ratio between V_{tri1} and V_{tri2}, and T_S is the switching period. To balance the power and voltage between battery and FC, duty-cycle D is applied as one of the control freedoms, while the phase shift ratio θ is employed as the second control freedom to regulate the voltage and power between FC and load. Based on the operation principles of stacked TPTLC, the equivalent circuit between the battery and FC is an ABHB converter, and the equivalent circuit between the FC and load is a noninverting bidirectional buck-boost converter. In other words, the FC resembles the output of the ABHB converter and input of noninverting bidirectional buck-boost converter, implying the load and the battery is decoupled by the FC.

The modulation scheme depicted in Figure **3.14** (b) allows the independent control of ABHB converter and noninverting bidirectional buck-boost converter. Since the battery voltage is constant, the output voltage can be regulated by a voltage-mode control loop. The sign of phase-shift ratio θ indicates the power flow direction. The positive and negative values indicate the power flow from LVS to HVS and from HVS to LVS, respectively. Due to the symmetrical performance of converter in Scenarios I and III, seamless power flow can be obtained by adopting PPSM. Battery charging and discharging control is designed such that constant current and constant voltage charging are implemented. To avoid over discharging the battery, a discharge controller is used to cease operating the load by adjusting the phase shift ratio to be zero.



(a)



(b)

Figure 3.14: Control scheme: (a) control block diagram of proposed converter, (b) modulation scheme.

3.4 Comparison of The Proposed Stacked TPTLC and Other Converters

While considering the state-of-the-art TPC topologies, a close look at the proposed converter and comparing it with other converters is of great importance because it provides invaluable information on different aspects of TPCs for various applications. A comparison between the proposed stacked TPTLC, nonisolated converters introduced in [18], [20], [24], partially-isolated converter introduced in [6], and isolated converter introduced in [11] is presented in Table 3.5. It is noteworthy to mention that each TPC DC-DC converter topology has its own merits and demerits; therefore, there are no specified selection criteria to choose any specific topology for any particular application. However, these topologies can be compared under particular characteristics, such as the number of components including the switch, diode, inductor, and transformer, control technique, voltage stress of switches, and efficiency. The comparison is made only on the bases of simple synthesized topology. Control schemes and extra cells added to achieve additional benefits are not taken into account in this comparison.

Regarding the soft switching operation, all the switches in these converters can achieve it, except the non-isolated converters cited in [20] that suffers from hard switching operation of the switch and reverse-recovery problem of the diode, leading to high switching losses. The proposed converter offers the soft-switching performance for a wide range of operation points. Among these converters, the partially-isolated converter introduced in [6] has the least number of switches. However, since the diode rectifier is employed in the output stage, the power cannot flow from the output to the sources; so, operating in scenario III is not possible.

Looking at the recent works, the classic PWM is used in the most nonisolated converters such as converters introduced in [18], [20], and [24]; but, the duty cycle is the only parameter to regulate the voltage and power flow, which imposes challenges on the independent control of power and voltage. In the partially-isolated converter introduced in [6], a combination of pulse frequency modulation (PFM) and PWM is used to provide the independent voltage regulation of output and battery. Nevertheless, the design of passive components is an implementation hurdle due to the interdependence of their impedance and frequency. Moreover, the voltage regulation range for this converter is narrow. Adopted in the proposed converter and the isolated converter introduced in [11], PPSM control scheme is an attractive solution for hybrid renewable energy systems that enables control of power and voltage by employing phase-shift ratio and duty-cycle, respectively. Nevertheless, a high number of switches in the isolated converter introduced in [11] complicates the control scheme, diminishes the overall system efficiency, and increases the cost. Even though the total semiconductor count in both proposed converter and the nonisolated converter introduced in [20] is the same, the bidirectional power flow for all

three ports is feasible only in the proposed converter. To sum up, compared to other converters, the proposed converter offers the main features of TPCs with a smaller number of semiconductors as well as the fewer magnetic cores; therefore, it can be a preeminent option for applications that size is a critical parameter. The stacked configuration provides high voltage gain with reduced voltage stress across the switches, providing the conditions to employ the switches with smaller on-resistance $R_{DS(ON)}$ that results in higher efficiency.

Table 3.5: Comparison study between the proposed converter and other TPCs.

Specification	**Non-isolated Converter [18]**	**Non-isolated Converter [24]**	**Partially-isolated converter [6]**	**Isolated converter [11]**	**Proposed Converter**
No. of switches	3	6	2	14	4
No. of diodes	3	0	4	0	0
No. of transformer	0	0	1	2	0
No. of inductors	4	2	1	2	2
Boost voltage gain (V_o/V_{in1})	2/(1-D)	1/(1-D)	N/(1-D)	$\frac{ND(1-D)R_L}{L_f f_S}$	2/(1-D)
Voltage stress of switches	$0.5V_{out}$	V_{out}	V_{out}	$\frac{V_{out}L_f f_S}{ND(1-D)R_L}$	$0.5V_{out}$
Control technique	PWM	PWM	PWM+ PFM	PPSM	PPSM
No. of ports with bidirectional power flow capability	1	3	2	3	3
Soft switching	Yes	Yes	Yes	Yes	Yes

3.5 Loss Analysis and Experiment Verification

In this section, the experimental verification of a 1kW prototype of the stacked TPTLC PWM plus phase-shift modulated converter are given to prove the theoretical analysis and operation principle of the proposed converter. The design specifications for the prototype are illustrated in Table 3.6.

Table 3.6: Design specifications.

Parameters	Value
Battery voltage V_{BT}	50-100 V
Output voltage V_{out}	400 V
Output power P_{out}	1000 W
Switching frequency f_s	100 kHz
Switches	GS66516T (650 V, 60 A, $R_{DS(ON)}$ of 25 mΩ)
Inductor L_{B1}	300 uH
Inductor L_{B2}	10 uH
Auxiliary capacitor C_{aux}	DCP4I052006JD2KSSD (WIMA, 20 uF, 600 V)
Battery port capacitor C_{BT}	C4AEGBW6100A3NJ (KEMET, 100 uF, 450 V)
Output capacitor (C_C and C_O)	DCP4I052006JD2KSSD (WIMA, 20 uF, 600 V) in parallel with C5750X6S2W225K250KA (TDK, 2.2 uF, 450 V)

3.5.1 Loss Analysis of the Proposed Stacked TPTLC

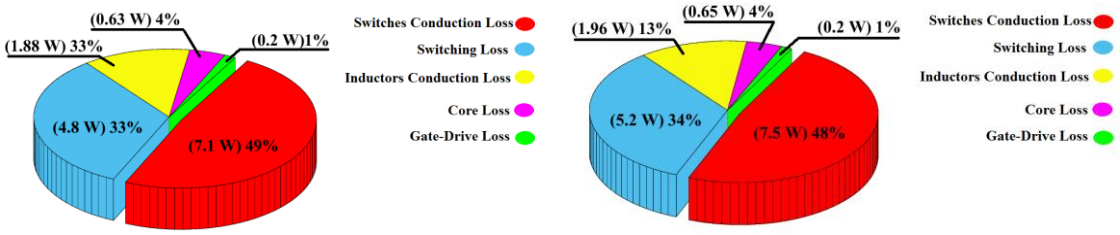
Referring to Figure **3.3** (e) and [33], the equations for calculating the loss can be obtained. Table 3.7 gives the loss equations for key components, including the switching and conduction losses of switches, core and conduction losses of magnetic cores.

Since all cores have been selected from Micrometal Inc. with relative permeability of μ_r=35, the core loss of the inductors can be calculated by multiplying core volume V_e with core loss density P_e. For this permeability, core loss consumed in unit volume P_{cv} has been provided by Micrometal Inc. with the equation given in Table 3.7 [34]. In Table 3.7, f_s is the switching frequency, Q_{gate} is the total gate charge and V_d is the drive voltage, which in case of SI8261BAC is 6.8V, B is the peak AC flux density, R_{ESR} is the equivalent series resistance of the inductor, and the coefficients a, b, c and d can be derived from datasheet. In this equation, four coefficients (a, b, c, and d) needed to describe the material, determined by "best fitting" measured data from core loss graph given by manufacturer. This model in this equation will be referred to as the Oliver model [35]. In this study, due to ZVS performance, the capacitive switching loss as well as the loss of capacitor is not considered. To calculate the switching loss for GaN devices, simulation using LTSpice model by the manufacturer is beneficial. The double pulse simulation model can precisely estimate the turn-on and turn-off losses. The turn-on loss and the turn-off loss under different drain-source voltages for GaN eHEMT GS66516T from GaN Systems can be obtained.

Table 3.7: Loss equations for key components.

Parameters		**Value**
Switches (S_1-S_4)	Conduction loss	$P_C = R_{DS(on)} I_{S,rms}^2$
	Switching loss	By integrating the product of the voltages and currents using double pulse test circuit
	Gate drive loss	$P_G = V_d Q_{gate} f_s$
Inductors (L_{B1} and L_{B2})	Core loss	$P_v = \frac{f_S}{\frac{a}{B^3} + \frac{b}{B^{2.3}} + \frac{c}{B^{1.65}}} + d * (f_S^2 B^2)$
	Winding loss	$P_W = R_{ESR} I_{L,rms}^2$

For the purpose of clarification, the loss breakdown for two scenarios I and III feeding full load using the equations given in Table 3.7 is presented in Figure **3.15**. The theoretical efficiency for scenario I and III during feeding full load are 98.5 % and 98.4%, respectively. It can be concluded that, due to using GaN switches and ZVS performance, the switching and conduction loss in the proposed converter is decreased compared to its hard-switched silicon-based counterparts. So, smaller heat-sink can be used for the proposed converter leading to higher power density.



(a) (b)

Figure 3.15: Loss breakdown for different scenarios under full-load condition. (a) Full-load P_{out}=1 kW, V_{BT}=100 V, θ=0.05 and D=0.53 in scenario I. (b) Full-load P_{out}=1 kW, V_{BT}=100 V, θ= –0.1 and D=0.53 in scenario III.

3.5.2 Experimental Results

A 1 kW prototype of proposed TPTLC converter was implemented to verify the theoretical analysis and simulation results. The design specifications and the components used in the prototype are given in Table 3.6. Developments in wide band-gap semiconductor devices, especially GaN switches, have enabled the power converters operation at a higher frequency, higher efficiency, temperature, and voltage. Due to the attractive characteristics of GaN devices such as small on-resistance $R_{DS(ON)}$, zero reverse recovery charge, high switching frequency, and high temperature operation, they are the most promising

competitors to replace different silicon-based DC/DC converters. Many EV manufacturers are migrating their converter designs to GaN to take advantage of this new semiconductor. In the experimental setup, the FC source was emulated by XR375-15.9 Programmable DC MAGNA power supply, and a HO 50-S current sensor is used for measuring the FC current.

In this part, to evaluate the voltage regulation and steady-state performance of the proposed converter, some experimental results for different scenarios I –IV are presented, shown in Figure 3.16-Figure 3.20, respectively. The results of converter performance at full load 1 kW for scenario I are shown in Figure 3.16. The output voltage V_{out}, battery voltage, and voltage across capacitors C_c and C_o are shown in Figure 3.16 (a). It can be seen that the voltage ripple of V_{out} and V_{Cc} and V_{CO} is small enough confirming the design of related capacitors. The gate-source pulses of the switches are illustrated in Figure 3.16 (b). There is no voltage ringing caused by parasitics in the gate pulses, implying the design of gate driving circuit in PCB layout is carried out correctly. To study ZVS performance, the gate signals and voltage stress across switches S_1, S_3, S_4, and S_2 are shown in Figure 3.16 (c), (d), (e), and (f), respectively. The voltage stress of all switches is 200 V, which is half of the output voltage, thus enabling use of low voltage switches with low conduction resistance $R_{DS(ON)}$. The voltage spike on switch S_2 is more than other switches, which is 20 V (about 10%), meaning that low parasitic inductance is achieved by optimizing the PCB layout design. The converter performance at battery voltage 100 V and output power 1 kW is investigated from an efficiency viewpoint. As discussed in Section III, the soft-switching condition of switches S_1 and S_2 is more rigorous than that of switches S_3 and S_4. So, the soft-switching performance of switches S_1 and S_2 is evaluated in this part. Figure 3.16 (c) and (f) illustrate the detailed turn-on instant for the switch S_1 and S_2 at full load,

demonstrating the voltage across the switch becomes zero before the gate pulse is applied that implies ZVS is realized. Also, soft-switching performance of switches S_3 and S_4 is presented in Figure 3.16 (d) and (e). The results of converter performance for battery voltage 50 V at different loads 100, 500, and 1000 W are depicted in Figure 3.17 (a), (b), and (c), respectively, including the inductor current i_{LB1} and i_{LB2}, and the voltage across switches V_{ab} and V_{cb}. Figure 3.17 (d), (e), and (f) show the current and voltage waveforms for battery voltage 75 V at different loads 100, 500, and 1000 W, respectively.

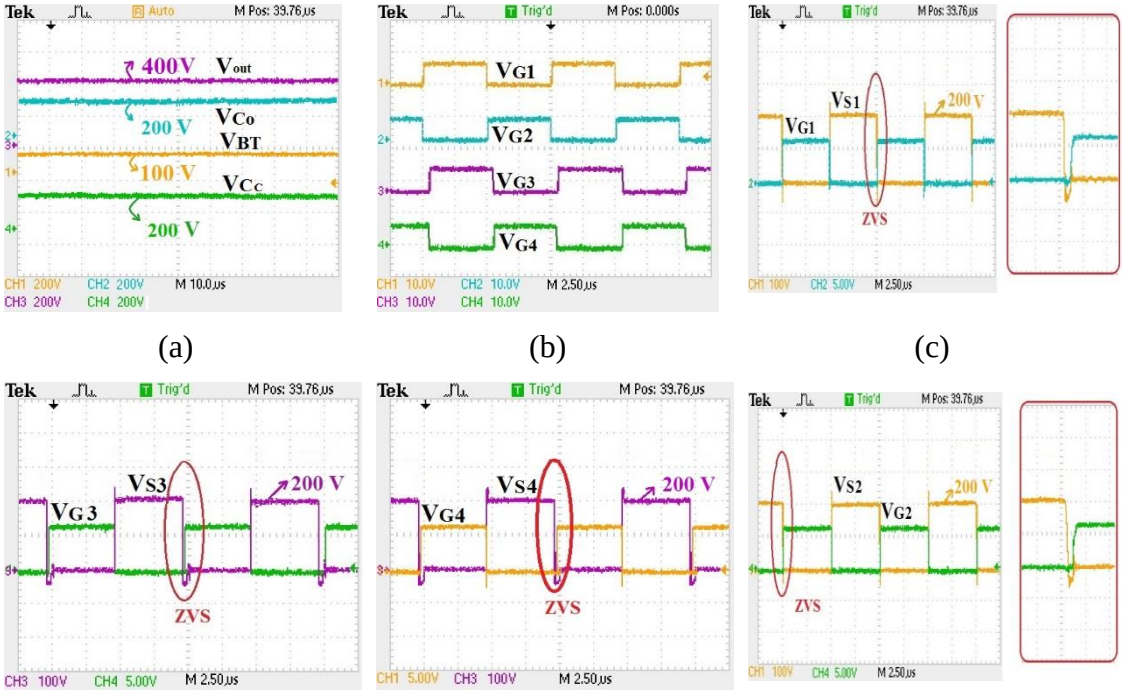


Figure 3.16: Experimental results during scenario I at full-load condition when V_{BT} = 100 V, V_{out} = 400 V, P_O = 1 kW, θ=0.05, and D=0.53. (a) Gate-source voltage of switches. (b) drain-source voltage of switches S_1 and S_2 (c) gate-source and drain-source voltage of switch S_1. (d) gate-source and drain-source voltage of switch S_4. (e) gate-source and drain-source voltage of switch S_4. (f) gate-source voltage of switch S_1 and inductor current i_{LB1} and i_{LB1}.

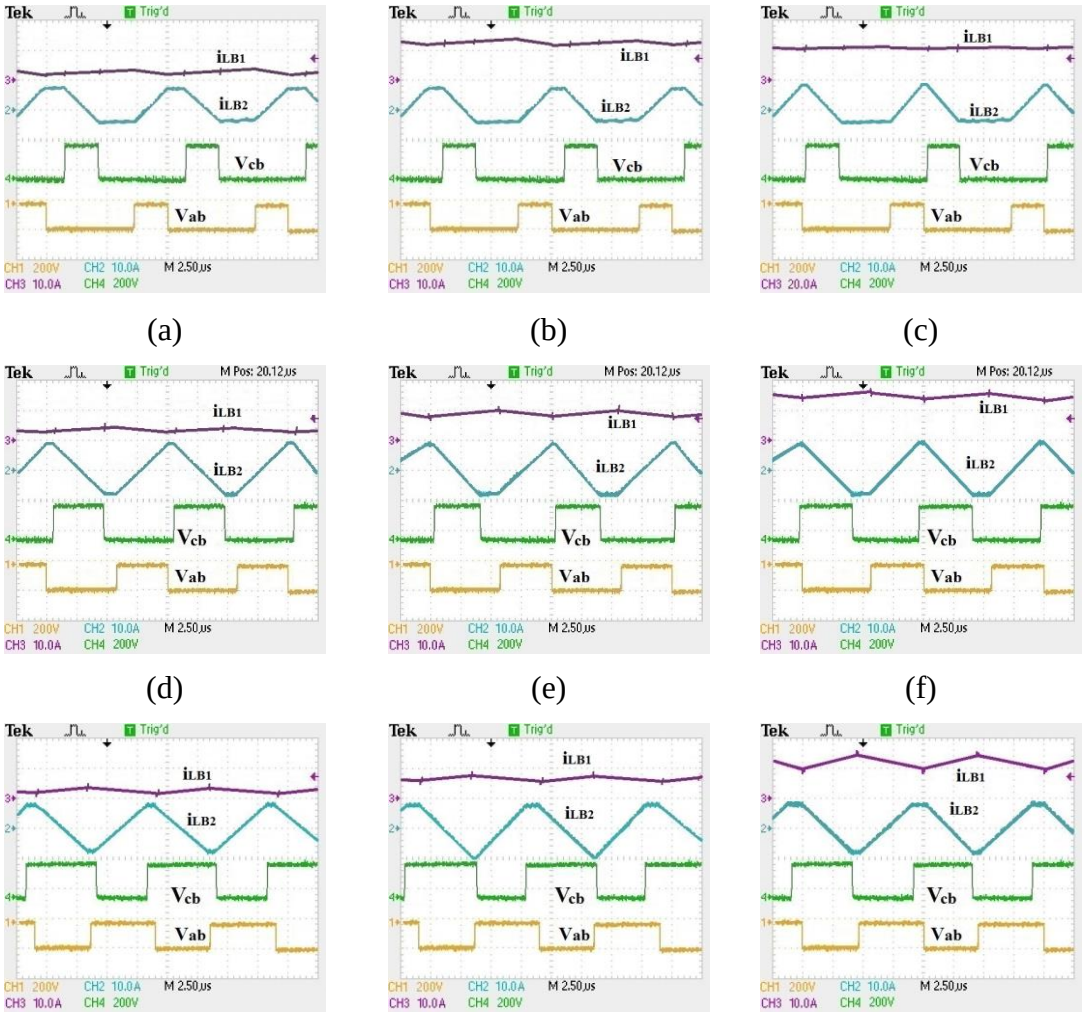


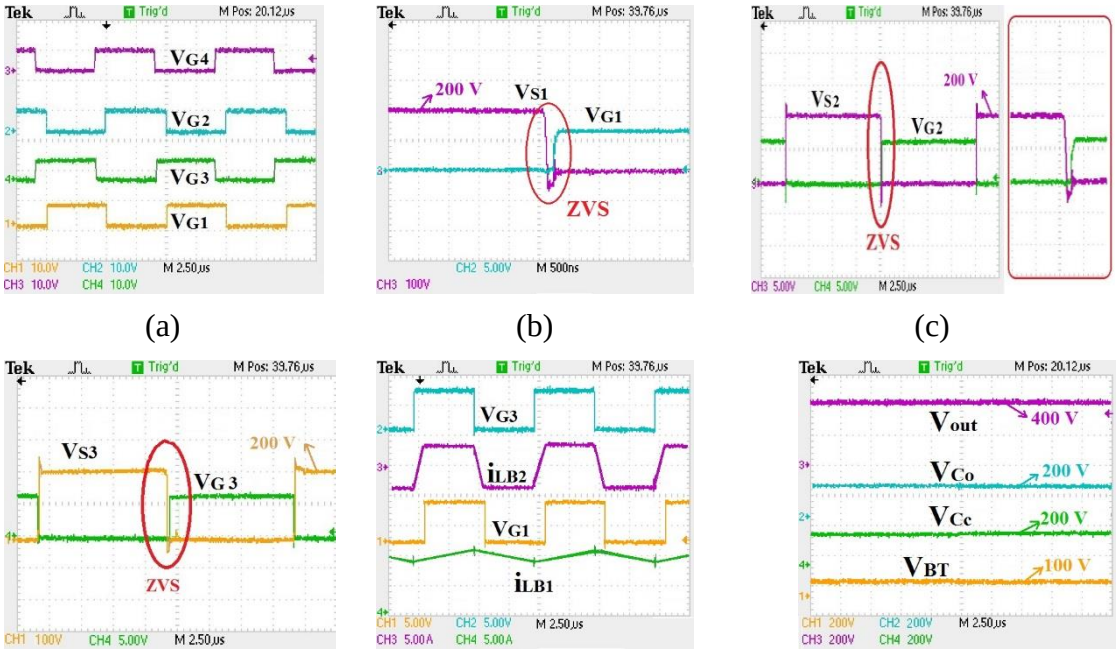
Figure 3.17: Experimental results during scenario I for different battery voltage and output power V_{FC} = 175.7 V and V_{out} = 400 V. (a) V_{BT} = 50 V and P_{out} = 100 W. (b) V_{BT} = 50 V and P_{out} = 500 W (c) V_{BT} = 50 V and P_{out} = 1000 W. (d) V_{BT} = 75 V and P_{out} = 100 W. (e) V_{BT} = 75 V and P_{out} = 500 W. (f) V_{BT} = 75 V and P_{out} = 1000 W. (g) V_{BT} = 100 V and P_{out} = 100 W. (h) V_{BT} = 100 V and P_{out} = 500 W. (i) V_{BT} = 100 V and P_{out} = 1000 W.

The results of converter operation for battery voltage 100 V at different loads 100, 500, and 1000 W are illustrated in Figure 3.17 (g), (h), and (i), respectively. As shown in Figure **3.2**, the voltages V_{ab} and V_{cb} imply the voltage stress across switches. When the gate-pulse of switch S_1 is applied, V_{ab} should be equal to $-V_{FC}$, which is about 180 V shown in Figure

3.17. Otherwise, the voltage V_{ab} is zero. During the conduction of switch S_3, V_{cb} is zero, and during the conduction of switch S_4, V_{cb} should be equal to V_{Co}, which is about 220 V as shown in Figure 3.17. It is noteworthy to mention that the current ripple of battery is in the acceptable range confirming that the design of inductor L_{B1} is precise. The operation of proposed converter under full-load condition in scenario III is shown in Figure 3.18, which is in the line with the theoretical analysis. Figure 3.18 (a) depicts the gate pulses of switches, indicating the phase-shift between the gate pulse of switches S_1 and S_3 is 1us and the duty-cycle is 0.53. The gate pulse and voltage stress across the switches S_1, S_2, and S_3 are shown in Figure 3.18 (b), (c), and (d), respectively. These figures provide evidence that the soft switching at turn-on instant is achieved in scenario III. The inductor current i_{LB1} and i_{LB2}, and the gate signal of switch S_1 and S_3 are shown in Figure 3.18 (e). There is perfect agreement between the theoretical analyses discussed in the previous section and the experimental results shown in Figure 3.18 (e). As expected, the experimental results shown in Figure 3.18 (e) prove that the inductor current i_{LB2} is flat since the voltage of capacitors C_C, C_O, and C_{aux} are equal. The battery voltage V_{BT}, the voltage of output capacitors V_{Co} and V_{Cc}, and output voltage V_{out} are demonstrated in Figure 3.18 (f). The results of converter performance during scenarios II and IV are demonstrated in Figure 3.19. The gate pulse, drain-source voltage of switch S_1 and the inductor current i_{LB1} are depicted in Figure **3.19** (a). As shown in Figure **3.19** (a), the voltage stress of switch S_1 is 176 V, which is equal to the FC voltage. The generated power of FC stack (P_{FC}=1020 W) is more than the power demanded by load (P_{out}=1000 W); so, the battery is charged by the surplus power. Figure **3.19** (b) shows the gate voltage of switch S_1 and S_3, and the battery voltage V_{BT} =70 V when the FC voltage is V_{FC} = 176 V and the duty cycle is 0.62. The

voltage stress of switches is limited to the voltage of clamp capacitor. The experimental results also clearly substantiate that the control scheme is working properly in all operating scenarios.

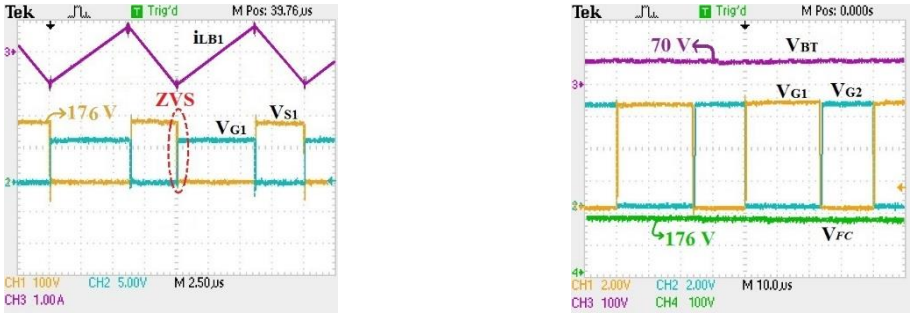
To evaluate the dynamic behavior of stacked TPTLC, a test was conducted. The battery voltage, the output voltage, and current i_{LB1} under power flow change are illustrated in Figure 3.20. A lithium iron phosphate battery with nominal voltage of 100 V is connected to the LVS port to test the performance of the converter in transition between scenario I and III. From Figure 3.20 (a) and (b), it can be concluded that the power flow change is carried out smoothly from scenario I to III and vice versa.



(a) (b) (c)

(d) (e) (f)

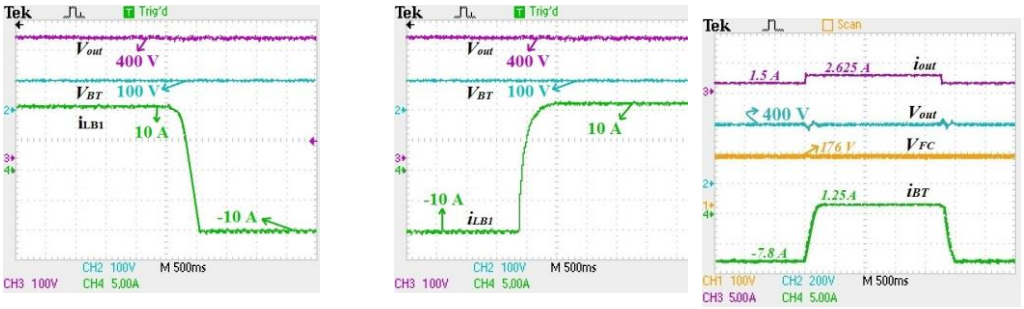
Figure 3.18: Experimental results during scenario III at full load when D=0.53, θ= –0.1, V_{BT} = 100 V, V_{DC} = 400 V, P_O = 1000 W. (a) Gate pulse of switches. (b) gate-source and drain-source voltage of switch S_1. (c) gate-source and drain-source voltage of switch S_2. (d) gate-source and drain-source voltage of switch S_3. (e) gate-source of switches S_1 and S_3, inductor current i_{LB1} and i_{LB1}. (f) Battery voltage, output voltage, voltage across capacitors C_{o1} and C_{o2}.



(a) (b)

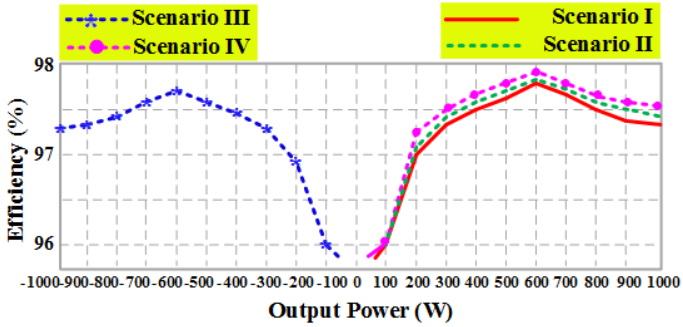
Figure 3.19: Experimental results during scenario II and IV (V_{BT} = 70 V, V_{FC} = 175.7 V, P_O = 1000 W, and D=0.6). (a) Gate-source voltage of switches. S_1 and S_2 and inductor current i_{LB1} during Scenario II when P_{FC}=1020 W. (b) Battery voltage and gate-source voltage of switches S_1 and S_3 during scenario IV.

Figure 3.20 (c) shows the transient characteristics during a step increase in the load while the battery voltage is 50 V. It can be seen that at the instant of the step increase in load, I_{out}, V_{out} dropped in response to abrupt increase in I_{out}. Before the load variation, the converter was working in *Scenario II*. After the step variation in the load, the converter enters *Scenario I*. It can be observed from figure that the output voltage is maintained at 400 V while the load is changed. The measured efficiency for different scenarios is depicted in Figure 3.21 (a). The maximum experimental efficiency happens at 600 W during Scenario IV, which is 97.9%. The experimental efficiency at full load condition in scenarios I-IV are 97.5%, 97.6%, 97.5%, and 97.7%, respectively. The efficiency comparison among the proposed converter working in scenario I, converter in [11], converter in [14], and converter in [18] are given in Figure 3.21 (b). By providing fewer passive components involving in the power conversion, the proposed converter provides higher efficiency. The developed prototype is shown in Figure **3.22**.

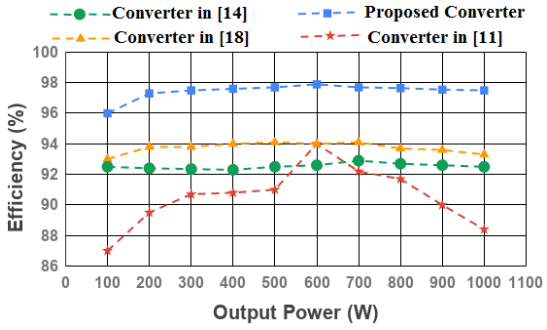


(a) (b) (c)

Figure 3.20: Experimental results under transition when V_{out}= 400 V and P_{out}= 1000 W. (a) Transition from scenario I to scenario III (V_{BT}=100 V). (b) Transition from scenario III to scenario I (V_{BT}=100 V). (c) Measured transient response characteristics during the stepped load change conditions. (V_{FC} =175.8, P_{FC}= 990 W, and V_{BT}=50 V).



(a)



(b)

Figure 3.21: Efficiency curves. (a) efficiency curves for different scenarios. (b) Efficiency comparison between the proposed converter and other recent TPCs.

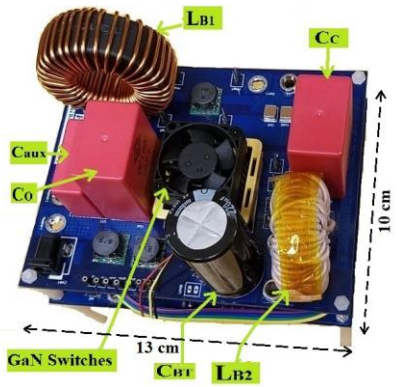


Figure 3.22: Laboratory prototype of the Stacked TPTLC.

3.6 Conclusion

A multiport converter is recognized as being a key enabling technology for fuel cell electric vehicle to interface the renewable energy source with the load and the battery. In this chapter, a family of TPTLC for hybridizing of renewable energy sources is introduced which features simple topology, low voltage stress across switches, and ZVS performance for wide load variation. It also inherits the salient advantages of the conventional ABHB converter in terms of the lower number of components, small size, and weight. The proposed stacked TPTLC is taken as an example to investigate the correctness of the proposed concept, which has different operation scenarios based on the output power of FC and the state of the charge of battery. In the stacked TPTLC, a high voltage gain is achieved without using the transformer, which results in significantly reduced cost and size of the system. The RMS current of inductance and the boundary condition of the phase-shift controller in different operation scenarios are analyzed to find the low-conduction-loss operation mode. A control system comprised of PWM and phase-shift controlled algorithm is proposed, which provides a solution to simultaneously regulate the voltage of different ports and control the power flowing between ports. Finally, a laboratory prototype

of proposed stacked TPTLC using GaN switches was developed to validate the proposed concept experimentally.

Chapter 4 Design and Implementation of a GaN-Based, Modular, PWM-Controlled Quasi-Resonant, Bidirectional DC/DC Converter Using GaN Switches for EV Application

4.1 Introduction

A modular quasi-resonant bidirectional (MQRB) dc-dc converter composed of half-bridge gallium nitride modules (HBGM) with reduced switch voltage stress is proposed in this chapter. The suggested configuration takes advantage of enhancement-mode gallium nitride (eGaN) switches regarding their small on-resistance $R_{DS(on)}$, low gate charge, and fast switching speed to improve both efficiency and power density. By using an auxiliary capacitor, a resonant circuit is formed to shape the current and voltage so that zero-voltage-switching (ZVS) at turn-on instant is achieved. Since the switching loss dominates the power losses in high-frequency dc-dc converters, the soft-switching performance leads to a noticeable reduction in the total loss; so, the operating temperature will decrease, and consequently, size of the heatsink will be reduced. The main performance issue of adopting GaN switches in the bidirectional dc-dc converter is the high voltage stress of GaN devices, which is handled by connecting the HBGM in the active-clamped stacked configuration, as well as optimizing printed circuit board (PCB) layout design. Finally, a 1 kW, 600 V laboratory prototype operating at 100 kHz, along with some simulation scenarios, are carried out to validate the proposed concept of modularity.

4.2 Proposed converter and its Operation Principle

The basic unit of proposed MQRB dc/dc converter is comprised of the half-bridge GaN module, which is shown in Figure 4.1. Symbols are defined as follows: filter inductors L_B,

resonant inductor L_r, C_{in} the energy storage/filter capacitor of the battery side, power switches S_M, S_C, S_L, S_H, resonant capacitor C_r, and output capacitors C_{O1} and C_{O2}.V_{DC} denotes the voltage of DC-link, which is equal to the summation of the voltage of output capacitors, $V_{Co1} + V_{Co2}$. In Figure 4.4.1, the battery is emulated by a voltage source V_{BT}. Also, the DC-link is modeled as an ideal voltage source V_{DC}. Indeed, two HBGMs are connected by an auxiliary capacitor C_r forming a resonant circuit with inductor L_r. The output capacitors C_{O1} and C_{O2} work as the clamp capacitors to confine the voltage stress of switches. In the battery side, a filter inductor L_B is used to decrease the current ripple. i_{LB} and i_{Lr} are the currents through filter inductor and resonant inductor, respectively. In this converter, the duty cycle D of switches S_M and S_L is the same, which is the control variable to adjust the voltage of battery and DC-link, and it can vary from 0 to 1. Asymmetrical complementary PWM switching technique is used for switch S_C and S_H.

Figure 4.4.2 shows the generalized structure of proposed MQRB dc/dc converter for high-power and high-voltage applications. This topology is composed of "P" groups of HBGMs connected in parallel at the battery side to reduce the input current ripple, and "S" groups of HBGMs that are placed in series at the DC-link side to increase the output voltage.

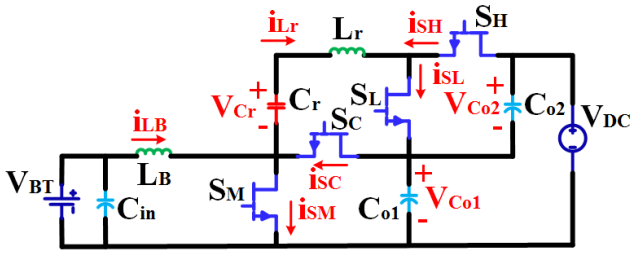


Figure 4.1: The single-phase version of proposed MQRB converter as a building block for multiphase MQRB converter.

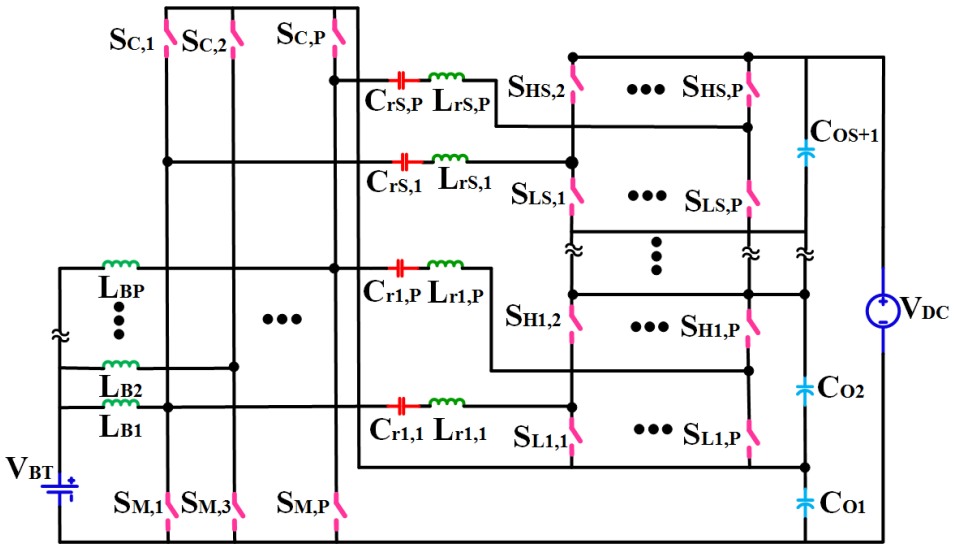


Figure 4.2: General configuration of the proposed MQRB converter for high-voltage and high-power applications.

To reduce the current stress of series-connected modules, each of the S groups of HBGMs also is composed of "P" parallel connected HBGMs. Modular characteristic gives the designer flexibility in selection of switches according to the desired output power and voltage level.

Fundamentally, there are two performance modes in EV application according to the power flow direction: forward mode and backward mode. To simplify the analysis of the converter operation modes, the following reasonable assumptions are made:

1) The power switches are considered ideal, and their anti-parallel diodes and parasitic capacitors are overlooked.
2) The capacitors C_{in}, C_{o1}, and C_{o2} are so large that the voltage of these capacitors can be estimated constant throughout the switching period.

4.2.1 Forward Mode

The operation intervals and the key waveforms during forward mode are shown in Figure 4.4.3 and Figure 4.4.4, respectively. R_o represents the resistive load in forward mode. As shown in Figure 4.4.4, there is time delay between the rising edge of driving signal of switches S_M and S_L, which is defined as D_1T_S. Also, the time-delay between the gate pulse of switches S_C and S_H is defined as D_2T_S. As shown in Figure 4.4, there are four operation intervals during one switching period T_S, which are thoroughly explained as follows.

Interval 1 (t_0-t_1): In this interval, switch S_M is conducting the current in the negative direction. Indeed, the anti-parallel diode is conducting the current; so, the ZVS soft switching can be achieved when the gate pulse is applied before the current of S_M gets positive, shown in Figure 4.3 (a). Also, the inductor current i_{Lr} is flowing through anti-parallel diode of switch S_H. The output capacitors C_{O1} and C_{O2} limit the voltage stress of switch S_C and S_L owing to the clamp circuit. Meanwhile, the battery energy is being stored in the filter inductor L_B during this interval.

$$i_{LB}(t) = \frac{V_{BT}}{L_B}(t - t_0) + i_{LB}(t_0) \tag{4-1}$$

$$i_{Lr}(t) = \frac{V_{Cr,min} - V_{CO1} - V_{CO2}}{L_r}(t - t_0) + i_{Lr}(t_0) \tag{4-2}$$

Interval 2 (t_1-t_2): This interval begins when the gate pulse of switch S_L is applied. It should be noted that ZVS performance of switch S_L is realized naturally since the current was flowing through its antiparallel diode. As depicted in Figure 4.3 (b), a resonant circuit including the resonant inductor L_r and auxiliary capacitor C_r is established. The current and voltage during this mode are defined by the following equations:

$$i_{Lr}(t) = \frac{V_{Cr} - V_{CO1}}{Z_r}\sin(\omega_r(t - t_1)) \quad (4\text{-}3)$$

$$v_{Cr}(t) = (V_{Cr,min} - V_{Co1})\,[\cos(\omega_r(t - t_1)) - 1] + v_{Cr}(t_1) \quad (4\text{-}4)$$

Where

$$v_{Cr}(t_1) = V_{Cr,min} - V_{CO1}, \quad , Z_r = \sqrt{\frac{L_r}{C_r}} \qquad and, \omega_r = \frac{1}{\sqrt{C_r L_r}}$$

Interval 3 (t_2-t_3): This interval begins when the gate signal of switch S_M ends. Since the inductor current cannot change suddenly, it goes through the anti-parallel diode of switch S_C, illustrated in Fig3(c). As a result, ZVS performance of switch S_C is ensured. The energy stored in the boost inductor L_B is transferred to the output capacitor C_{O1}. Similar to the second interval, a resonant circuit composed of auxiliary capacitor C_r and inductor L_r is formed.

$$i_{LB}(t) = \frac{V_{BT} - V_{CO1}}{L_B}(t - t_2) + i_{LB}(t_2) \quad (4\text{-}5)$$

$$i_{Lr}(t) = \frac{V_{Cr,max} - V_{CO2}}{Z_r}\sin(\omega_r(t - t_3)) \quad (4\text{-}6)$$

$$v_{Cr}(t) = (V_{Cr,max} - V_{CO2})\,[\cos(\omega_r(t - t_3)) - 1] + v_{Cr}(t_3) \quad (4\text{-}7)$$

Interval 4 (t_3-t_4): This interval starts when the switch S_L turns off, and the gate signal of switch S_H is applied. As depicted in Figure 4.3 (d), the current of resonant inductor i_{Lr} is positive, and the ZVS performance at turn-on instant is realized for switch S_H. The voltage stress of switches S_M and S_L are limited to the voltage of V_{CO1} and V_{CO2}, respectively.

4.2.1 Backward Mode

The operation intervals of backward mode are similar to those of forward mode, except there is a delay between the switches S_M and S_L, which is defined as D_3T_S. The operation

intervals and the key waveforms are shown in Figure 4.5 and Figure 4.6, respectively. The backward mode includes four operation intervals in one switching period T_S, which are thoroughly described as follows.

Interval 1 (t_0-t_1): This interval starts when the gate pulse of switches S_C and S_H are removed, and the current flows through the switches S_M and S_L in the negative direction.

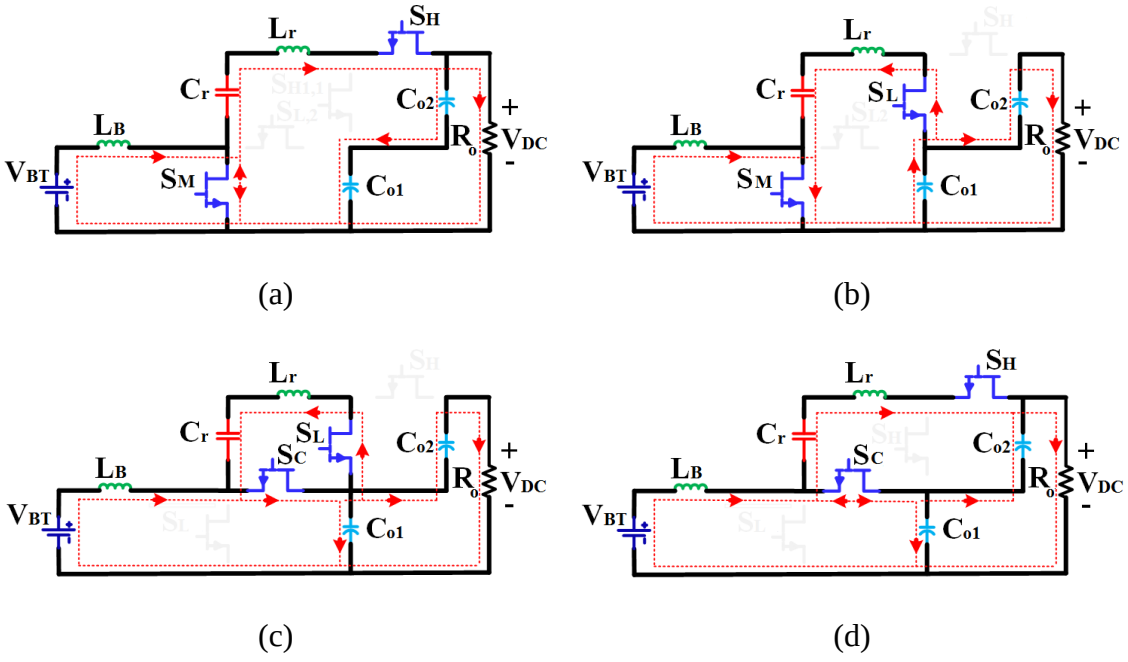


Figure 4.3: Different operation intervals during forward mode. (a) Interval 1; (b) Interval 2; (c) Interval 3; (d) Interval 4.

The ZVS soft switching can be obtained when the gate pulse is applied before the current of S_M gets positive, shown in Figure 4.5 (a). Also, the inductor current i_{Lr} is going through anti-parallel diode of switch S_L. Meanwhile, the battery has been charged by the energy stored in the filter inductor L_B during this mode.

Interval 2 (t_1-t_2): In this interval, the resonant inductor current reverses while it is flowing through the switches S_M and S_L. To obtain the ZVS performance of switch S_L, the gate

pulse should be applied before this interval. As depicted in Figure 4.5 (b), a resonant circuit including the resonant inductor L_r and auxiliary capacitor C_r is established.

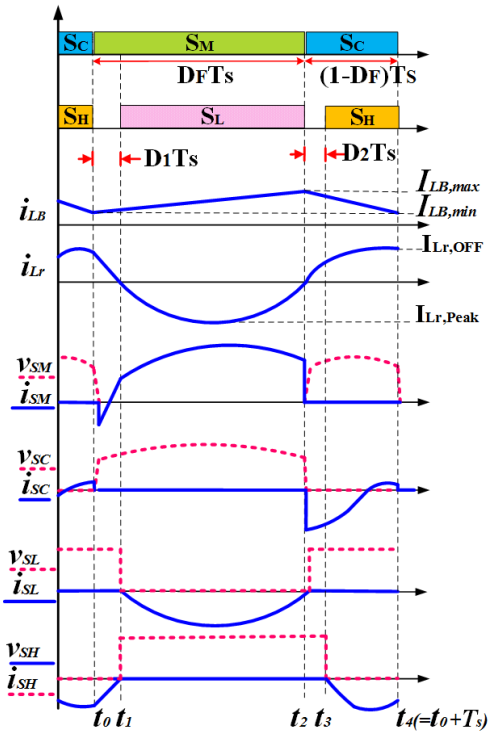


Figure 4.4: The key waveforms in forward mode.

Interval 3 (t_2-t_3): As shown in Figure 4.5 (c), this interval begins when the gate signal of switches S_M and S_L are removed. Since the inductor current cannot change suddenly, it goes through the anti-parallel diode of switches S_M and S_H. As a result, ZVS performance of switch S_H can be ensured as long as its gate pulse is applied before reversal of inductor current i_{Lr}. The energy stored in the boost inductor L_B is transferred to the battery.

Interval 4 (t_3-t_4): At the beginning of this interval, the gate pulse of switch S_C is applied, displayed in Figure 4.5 (d). It indicates that the ZVS performance at turn-on instant is obtained for switch S_C. The voltage stress of switches S_M and S_L are limited to the voltage

of V_{CO1} and V_{CO2}, respectively. Similar to the second mode, a resonant circuit composed of auxiliary capacitor C_r and inductor L_r is created.

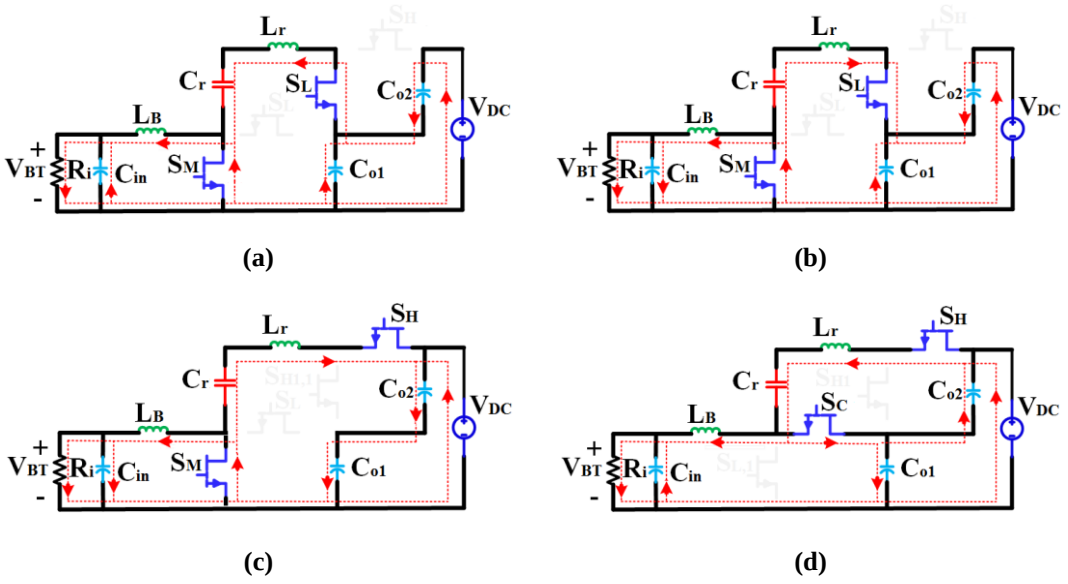


Figure 4.5: Different operation intervals during backward mode. (a) Interval 1; (b) Interval 2; (c) Interval 3; (d) Interval 4.

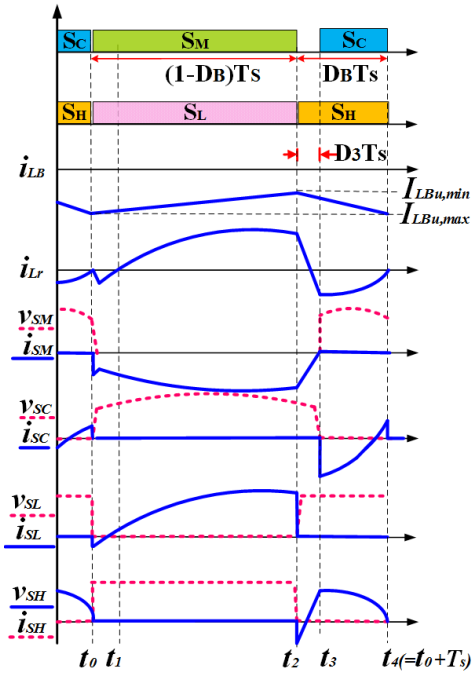


Figure 4.6: The key waveforms in backward mode

4.3 Steady-State Analysis

Since the capacitance C_{in}, C_{o1} and C_{o2} are large enough, the input and output voltage can be regarded as constant in the steady-state analysis.

4.3.1 Voltage Gain (M)

The DC-link voltage is defined by:

$$V_{DC} = V_{Co1} + V_{Co2} \tag{4-8}$$

Regarding the voltage-second balance on the inductor L_B, the output voltage V_{Co1} can be expressed by

$$V_{Co1} = \frac{1}{1 - \mathrm{D_F}} V_{BT} \tag{4-9}$$

Where D_F is the duty cycle of main switch S_M. By applying the voltage-second balance on the inductor L_r, the dc-link voltage can be obtained by

$$\mathrm{V_{DC}} = \frac{2}{1 - \mathrm{D}_F + \mathrm{D_1} + \mathrm{D_2}} \mathrm{V_{BT}} \tag{4-10}$$

Indeed, $(D_F\text{-}D_1\text{-}D_2) \times T_S$ is the time interval that the output capacitors are being charged by the inductor current i_{Lr}. The DC-link voltage can be rewritten as

$$\mathrm{V_{DC}} = \frac{2}{1 - \mathrm{D}_F} \mathrm{V_{BT}} - \Delta V \tag{4-11}$$

From (8), (9) and (11), the output voltage V_{Co1} and V_{Co2} can be defined by

$$V_{Co2} = \frac{1}{1 - D} V_{BT} - \Delta V \tag{4-12}$$

Since the average currents of output switches S_L and S_H are equal with the output current, the DC-link current can be written as follows:

$$I_{SL,avg} = I_{SH,avg} = \frac{V_{DC}}{R_o} = \frac{2}{T_S}\int_0^{\frac{T_r}{4}} \left(V_{C_{r,min}} - V_{CO1}\right)\frac{\sqrt{C_r}\sin(\omega_r t)}{\sqrt{L_r}}.dt \quad (4\text{-}13)$$

Where R_o represents the resistive load in forward mode. From (13), the maximum and minimum voltage of auxiliary capacitor can be calculated by

$$V_{C_{r,min}} \approx V_{Co1} - \frac{V_{DC}}{2f_S R_o C_r} \quad (4\text{-}14)$$

$$V_{C_{r,max}} \approx V_{Co1} + \frac{V_{DC}}{2f_S R_o C_r} \quad (4\text{-}15)$$

Where f_s is the switching frequency. Regarding the voltage-second balance on the inductor L_r, the duty cycle $D_1 + D_2$ can be defined by

$$D_1 + D_2 = \frac{2(1-D_F)(\frac{f_S}{\omega_r})\sin(\omega_r/2f_S)\cos\left((D_F - 0.5)\omega_r/f_S\right)}{2C_r R_o f_S\left(\frac{V_{BT}}{V_{DC}}\right) + (1-D_F)} \quad (4\text{-}16)$$

From (10) and (16), the relation between the battery voltage and DC-link voltage in forward-mode can be written as follows:

$$M = \frac{V_{DC}}{V_{BT}} = \frac{A(1-C) + \sqrt{(A(1-C)^2 + 4ABC(A + 2(\frac{f_S}{\omega_r})\sin(\frac{\omega_r}{2f_S})}}{AB(A + 2(\frac{f_S}{\omega_r})\sin(\frac{\omega_r}{2f_S})} \quad (4\text{-}17)$$

Where A=1-D_F, B= $\cos\left((0.5 - A)\frac{\omega_r}{f_S}\right.$, and C=$C_r R_o f_S$

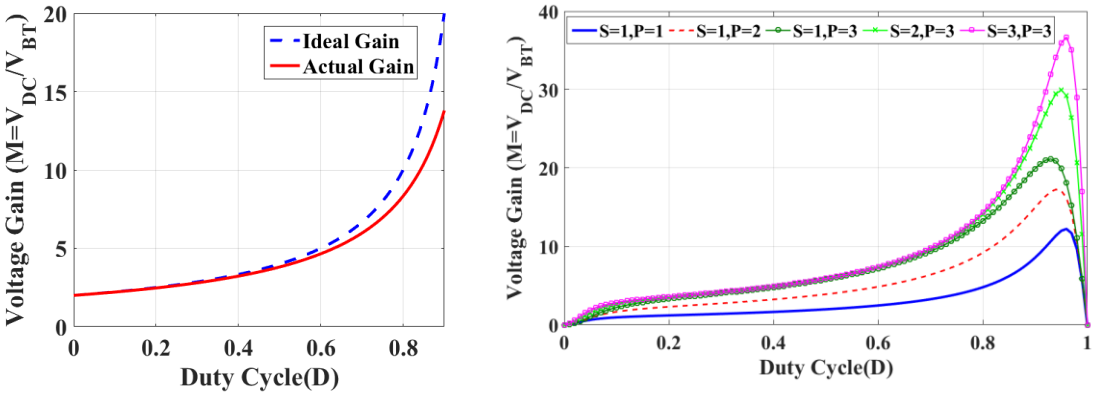
The ideal and actual voltage gain of the single-phase MQRB is illustrated in Figure 4. 7(a). The ideal voltage gain of the MQRB converter shown in Figure 4. 3 can be defined by

$$M = \frac{V_{DC}}{V_{BT}} = \frac{S+1}{1-D_F} \quad (4\text{-}18)$$

Where S is the number of series connected HBGMs. Figure 4. 7(b) shows the voltage gain of the MQRB converter in forward mode as a function of the duty-cycle (D_F) with different values of P and S. It can be seen that the voltage gain increases with the increase in P and S. The voltage stress of switches for the structure shown in Figure 4. 3 can be obtained by

$$V_{stress} = \frac{V_{DC}}{S+1} \tag{4-19}$$

From (18), it is clear that as the number of series modules (S) increases the voltage gain of proposed converter increases. The proposed converter can increase the voltage gain without using any transformer, resulting in higher power density. Aside from voltage gain, the proposed configuration helps to reduce the voltage stress of switches, which enables the designer to employ switches with smaller drain-source resistance $R_{DS(on)}$ leading to higher efficiency.



(a) (b)

Figure 4.7: Voltage gain characteristics for different number of modules and duty-cycle. (a) Voltage gain of single-phase MQRB. (b) Voltage gain of MQRB.

4.3.2 Voltage and current stress of switches

Due to the active clamp configuration, the voltage across switches is limited to the voltage of output capacitors C_{O1} and C_{O2}; so, the voltage stress can be defined by (19).

Turn-off current, maximum current, and root-mean-square (RMS) current of each switch are given in Table 4.1. The RMS current of switches for different duty-cycle and the resonant ratio (T_r/T_s) is presented in Figure 4.8. Interestingly, for the same resonant ratio, the RMS current decreases as duty-cycle increases; therefore, the conduction loss decreases with increasing the duty-cycle.

4.3.3 ZVS performance of proposed MQRB converter

The turn-on operation of switch S_C considering the dead-time between the gate-pulse of switches S_M and S_C is explained in Figure 4.9. As shown in Figure 4.4(a) and (b), before turn-on of S_C, the current i_{Lr} is negative, and the voltage across switches S_M and S_C are equal to 0 and V_{Co1}, respectively. The corresponding equivalent circuit is depicted in Figure 4. 9 (a). After the gate pulse of switch S_M is removed, the parasitic capacitance of switch S_M, C_{oss1}, charges from zero to V_{Cc} and parasitic capacitance of switch S_C, C_{oss2}, discharges from V_{Cc} to zero, as shown in Figure 4. 9(b). After the voltage across switch S_C reaches zero, its antiparallel diode starts conducting the current and the difference of the current of the inductors L_B and L_r freewheels through the antiparallel diode of switch S_C, shown in

Table 4.1: RMS current, turn-off current, and maximum current of switches.

Item	RMS Current	Turn-off Current	Maximum current
S_M	$I_{in}\sqrt{\frac{4(1-D_F)}{6}+\frac{\pi(1-D_F)^2T_s}{72\sqrt{L_rC_r}}}$	I_{in}	$I_{in}(1+\frac{(1-D_F)T_s}{2\sqrt{L_rC_r}})$
S_C	$I_{in}\sqrt{(1-D_F)+\frac{4I_{Lr,off}^2}{I_{in}^2}\left(\frac{(1-D_F)}{2}-\frac{\sin(2\omega_r(1-D_F)T_s)}{4\omega_rT_s}\right)-\frac{4I_{Lr,off}}{I_{in}\omega_r}(1-\cos(\omega_r(1-D_F)T_s))}$	$I_{Lin}(1-\frac{4\omega_r(1-D)I_{in}}{K})$	I_{in}
S_L	$I_{Lr,off}\sqrt{\frac{\sqrt{L_rC_r}\pi}{2T_s}}$	0	$I_{Lr,peak}=\frac{(1-D_F)I_{in}}{4\sqrt{L_rC_r}f_s}$
S_H	$\sqrt{\frac{1}{T_s}(\frac{1-D_F+D_1}{2}-\frac{\sin2\,(1-D_F+D_1)\omega_rT_s)}{4\omega_r})}I_{Lr,off}$	0	$\frac{\omega_r(1-D_F)I_{in}}{K}$

*$K=4(1-\cos(\omega_r(1-D)T_s))+2D_1T_s\omega_r$

Figure 4.9 (c). While the switch S_C is conducting the current, the gate pulse of switch S_C is applied; so, the switch S_C turns on at zero voltage, as depicted in Figure 4.9 (d). In a similar way, the ZVS operation of other switches can also be visualized. As illustrated in the operating principle of the converter and Figure 4. 4, the ZVS performance at turn-on instant is always guaranteed for switches S_C, S_L and S_H since the energy stored in the boost inductor is perpetually higher than the energy stored in the output capacitance of switches. Similarly, to satisfy ZVS condition at turn-on instant for switch S_M, the energy stored in the boost inductor should be greater than the energy stored in the output capacitance of switches S_M and S_C at t_0. However, the value of current flowing through the switch at this interval depends on the difference of the boost inductor current I_{LB} and resonant inductor current at t_0.

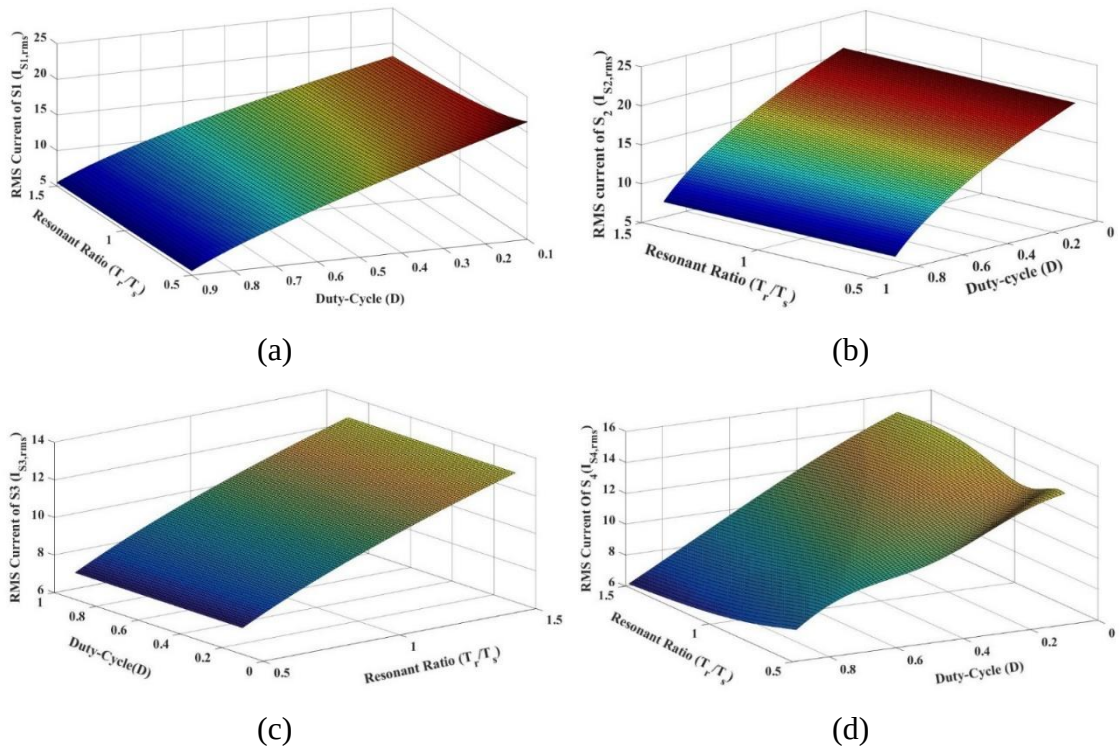


Figure 4.8: RMS current of switches for different duty-cycle (D) and resonant-ratio (T_r/T_s). (a) Switch S_M. (b) Switch S_C. (c) Switch S_L. (d) Switch S_H.

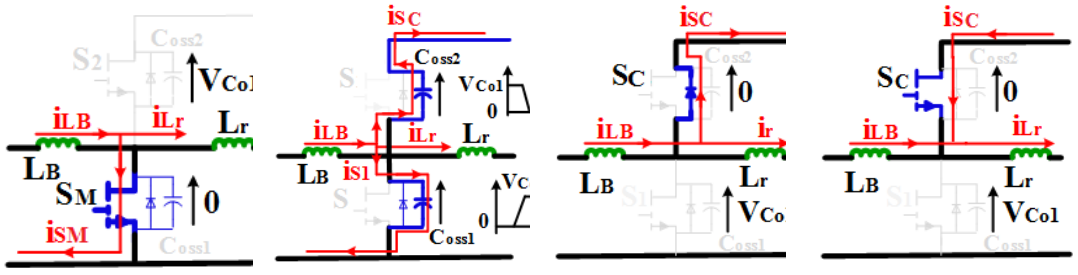


Figure 4.9: ZVS turn-on of switch S_C. (a) Before turn-on instant. (b) Charging and discharging of output capacitor C_{oss1} and C_{oss2}. (d) Antiparallel diode freewheeling. (d) Flowing current in reverse direction.

The average value and the ripple of the battery current can be calculated by,

$$I_{BT,avg} = \frac{1}{P}\frac{V_{DC}^2}{V_{BT}R_{out}} \tag{4-20}$$

$$\Delta I_{BT} = \frac{V_{BT}D_F T_S}{P L_{B1}} \tag{4-21}$$

The positive and negative maximum currents of inductors L_B and L_r can be calculated by,

$$I_{LB,max} = \frac{1}{P}\frac{P_o}{V_{BT}} + \frac{V_{BT}D_F T_S}{2P L_{B1}} \tag{4-22}$$

$$I_{LB,min} = \frac{1}{P}\frac{P_o}{V_{BT}} - \frac{V_{BT}D_F T_S}{2P L_{B1}} \tag{4-23}$$

$$I_{Lr,+max} = \frac{\omega_r T_s \sin(\omega_r(1-D_F)T_s)}{2P}\frac{P_o}{V_{DC}} \tag{4-24}$$

$$I_{Lr,-max} = \frac{2}{D_F P}\frac{V_{DC}}{R_o} + \frac{(1-D_F)D_F}{D_F^2 + (1-D_F)^2}\frac{V_{BT}T_S}{L_r} \tag{4-25}$$

Where P_o is the output power delivered to the DC-link. It is obvious from (22) and (23) that the positive and negative maximum values of inductor current decrease when number of paralleled cells, P, increases. The current of lower switch to realize ZVS is determined by

$$I_{SM,ZVS} = I_{Lr,+max} - I_{LB,min}$$

$$= \frac{\omega_r T_s \sin(\omega_r (1 - D_F) T_s)}{2P} \frac{P_o}{V_{DC}} - \frac{1}{P} \frac{P_o}{V_{BT}} + \frac{V_{BT} D_F T_S}{2P L_B} \quad (4\text{-}26)$$

The current of upper switch to realize ZVS can be determined by

$$I_{SC,ZVS} = I_{Lr,-max} + I_{LB,max}$$

$$= \frac{2}{D_F P} \frac{V_{DC}}{R_{out}} + \frac{(1 - D_F) D_F}{D_F^2 + (1 - D_F)^2} \frac{V_{BT} T_S}{L_r} + \frac{1}{P} \frac{P_o}{V_{BT}} + \frac{V_{BT} D_F T_S}{2P L_B} \quad (4\text{-}27)$$

So, the desire condition to achieve ZVS can be expressed as follows:

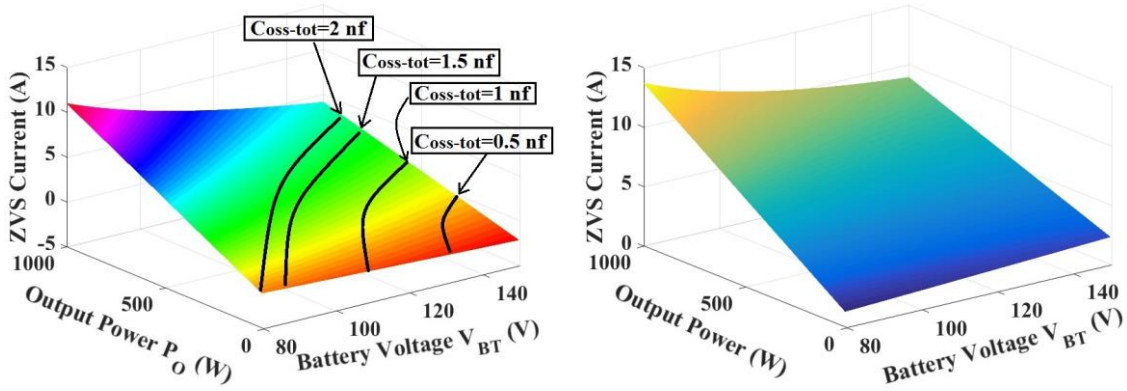
$$\frac{1}{2} \mathrm{L}_B (I_{LB}(\mathrm{t}_0) - \mathrm{I}_{Lr}(\mathrm{t}_0))^2 > \frac{1}{2} (\mathrm{C}_{oss1} + \mathrm{C}_{oss2}) \mathrm{V}_{CO1}^2 \quad (4\text{-}28)$$

Where C_{oss1} and C_{oss2} are the output capacitances of the main and clamp switches, respectively. Figure 4. 10 (a) and (b) show the ZVS current of main and clamp switches S_M and S_C as a function of output power and battery voltage, respectively. It can be clearly understood that the ZVS performance of clamp switch S_C is guaranteed for different power and voltage. It is noteworthy to mention that ZVS current of the main switch increases with increasing power P_o, implying the soft-switching operation is easily possible at higher output power. Moreover, the smaller the output capacitance, the wider ZVS operation range, because a smaller current is required to discharge the output capacitor of GaN switch, which implies that soft-switching performance would be more probable for GaN switch in comparison with its silicon counterpart. From (26), to extend the soft-switching capability of the converter, either the boost inductance L_B could be reduced, or the resonant inductance L_r could be increased. But, reducing the boost inductance leads to an increase

in the current rating of the switches due to large current ripple, and enlarging the resonant inductance contribute to the more considerable duty-cycle loss. Thus, making a compromise between ZVS capability and cost is necessary for design.

Another requirement for realizing the ZVS at turn-on instant is that the dead-time between the gate pulses applied to two switches S_M and S_C should be longer than the time for discharging the output capacitor of switch C_{oss1} from voltage V_{CO1} to 0 V. Equation (29) illustrates the relationship between the minimum current and minimum dead-time.

$$i \geq \frac{2C_{oss1}\Delta v}{\Delta t} \tag{4-29}$$



(a) (b)

Figure 4.10: ZVS current for switches S_M and S_C. (a) switch S_M. (b) switch S_C.

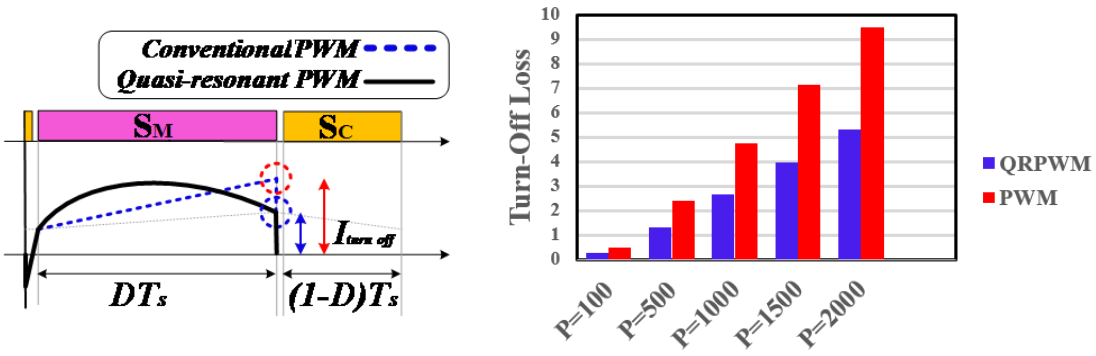
4.3.4 The effect of resonant frequenvscy on the current waveform of switch $S_{L,1}$

The proposed converter can work in two resonance operations modes according to the variation of resonant frequency: the quasi-resonant PWM (QRPWM) and conventional PWM. Equations (30) and (31) defines the resonant frequency for above-resonance operation. To achieve zero-voltage-switching in the series resonant converter, the converter

should work in the above-resonance operation mode; so, the switching frequency should be higher than the resonant frequency. Figure 4.11 (a) illustrates the effect of resonant frequency on the current waveforms of switch S_M. Regarding the turn-off current of switch S_M, QRPWM operation shows better performance compared to PWM technique, leading to lower turn-off loss. As illustrated in Figure 4.11 (b), the turn-off losses are considerably reduced due to the quasi-resonant operation.

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{4-30}$$

$$f_r > \frac{f_S}{2D} \tag{4-31}$$



(a) (b)

Figure 4.11: QRPWM performance versus conventional PWM performance. (a) Current waveform (b) Turn-off losses.

4.3.5 Interleaving MQRB converter for high-power applications

As depicted in Figure 4.3, P groups of HBGMs are interleaved in the battery side to reduce the current ripple, which is the critical issue in high power applications. Each leg is interleaved with a phase difference of $2\pi/P$. From (20), it is clear that the average current of battery increases as P decreases. Eq. (21) reveals that the frequency of input current

ripple becomes P times of the switching frequency f_S due to the interleaved operation, resulting in significantly smaller input inductors.

4.4 Loss Analysis

Major losses in a bidirectional DC/DC converter can be divided into three main parts: switch losses, inductor losses and capacitor loss. Switch loss includes conduction loss, driving loss, body-diode loss, and switching loss.

4.4.1 Conduction loss

Similar to other switches, the conduction losses in the GaN devices can be computed by the following equation. The RMS current of switches are estimated by equations given in Table 4.1.

$$P_{cond} = R_{DS(ON)} I_{rms}^2 \tag{4-32}$$

4.4.2 Driving loss

Drive loss of switches can be evaluated from the following equation

$$P_{drive} = V_d Q_{gate} f_s \tag{4-33}$$

Where f_s is the switching frequency, Q_{gate} is the total gate charge and V_d is the drive voltage, which in case of SI8261BAC is 6.8V.

4.4.3 Body-diode loss

Compared to the MOSFET, there is a higher reverse-conduction voltage drop in GaN device, results in a higher loss. The reverse conduction loss can be obtained by:

$$P_{BD} = V_{DS} . I_{DS} . t_{dead} . f_s \tag{4-34}$$

Where t_{dead}, V_{DS}, and I_{DS} are the dead-time, current, and voltage of switch, respectively.

4.4.4 Switching loss for hard-switching operation

The switching loss, one of the notable losses in the high-frequency circuits, is impossible to measure due to the small size of the GaN device and impact of parasitic elements in the PCB layout. To calculate the switching loss for GaN devices, the E_{oss} curve resulted from the experiment can be used. However, this is time-consuming and is not readily achievable for the employed switch; therefore, simulation using LTSpice model by the manufacturer is beneficial. The double pulse simulation model can precisely estimate the turn-on and turn-off losses. The turn-on loss and the turn-off loss under different drain-source voltages for eGaN HEMTs GS66508T from GaN Systems are depicted in Figure 4. 12 (a) and (b), respectively. Both turn-on and turn-off losses can be calculated based on the integration of device current I_{DS} and V_{DC} during switching transient. These data are derived based on the assumption that the switch is working in the hard-switching mode. There is some energy stored in the output capacitance C_{oss} defined as E_{oss}, which is stored in the capacitance of device during turn-off and then later will be recovered because of ZVS performance. So, for soft switching performance, taking E_{oss} away from the hard-switching E_{off} can provide an accurate estimation of the switching loss, as follows:

$$E_{off,soft\_switching} = E_{off} - E_{oss} \tag{4-35}$$

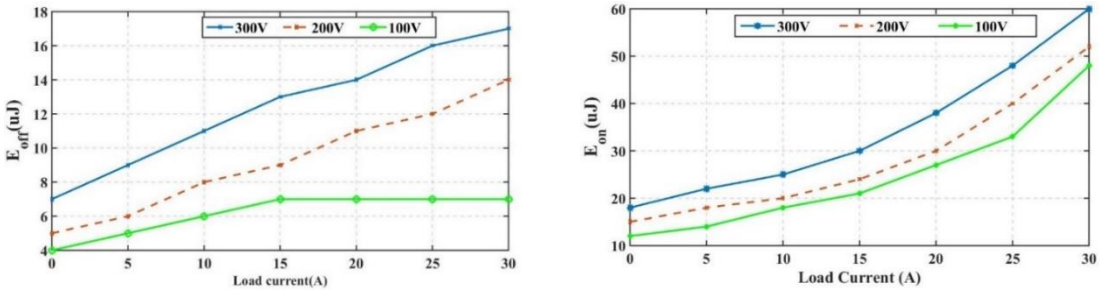
Since the output capacitance is non-linear, output charge should be considered to analyze the capacitive switching loss. The output charge can be defined as follows:

$$Q_{oss} = \int_0^V C_{oss}(v)dv \tag{4-36}$$

Where C_{oss} and v are the output capacitance and voltage across the device, respectively. The output charge can be estimated by using the graph given by the manufacturer for different C_{oss} and V_{DS}.

4.4.5 Inductors' losses

There are two factors causing inductor power loss including copper loss and the core loss. The copper loss is totally because of dc and low-frequency current, and the core loss comes from the high-frequency current. For the input inductor L_B, a lower permeability core material can be employed to improve the performance of the converter since the total losses are dominated by core loss rather than a copper loss. So, powder Iron T175-8 core and T126-8 from Micrometal is selected for the filter L_B and L_r, respectively.



(a) (b)

Figure 4.12: Turn-on loss and the turn-off loss under different drain-source voltages. (a) Turn-on loss under different drain-source voltages. (b) Turn-off loss under different drain-source voltages.

The equations for calculating the core loss and copper loss can be received from datasheet given by manufacturer as follows:

$$P_{core} = \frac{f_S}{\frac{a}{B^3} + \frac{b}{B^{2.3}} + \frac{c}{B^{1.65}}} + (df_S^2 B^2) \tag{4-37}$$

$$P_{cu} = R_{DC} I_{rms}^2 \tag{4-38}$$

Where B is the peak AC flux density, f_S is the switching frequency, R_{DC} is the equivalent series resistance of the inductor, the coefficients a, b, c and d can be derived from datasheet given by the manufacturer.

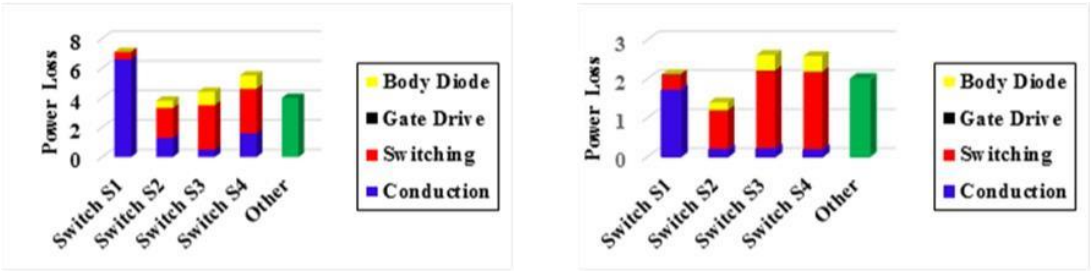
4.4.6 Capacitors' losses

The losses in the capacitors can be estimated by

$$P_{cond} = R_{ESR} I_{rms}^2 \tag{4-39}$$

Where R_{ESR} is the equivalent series resistance of the capacitor.

The total loss breakdown under full-load and half-load condition is depicted in Figure 4. 13. It is clear that the conduction loss of main switch is one of the main contributor to the power losses.



(a) (b)

Figure 4.13: Loss breakdown under full load and half-load condition. (a) Full load. (b) Half-load.

4.5 Comparison with the State-of-the-Art Converters

Helping in understanding the advantages and disadvantages of different BDC converters, a thorough comparison has been performed among the nonisolated bidirectional converters, including switched-capacitor converter [19], non-inverting buck-boost converter [26], nonisolated converter using coupled-inductor [27], three-level converter [28], and proposed converter in terms of efficiency, power rating, frequency, number of

switches and coupled inductor, voltage stress of switches, cost and soft-switching scheme. Fewer switches count along with reduced voltage stress is the chief merit of the proposed converter, leads to smaller driver size, lower gate losses and decreased cost compared to converter introduced in [19].

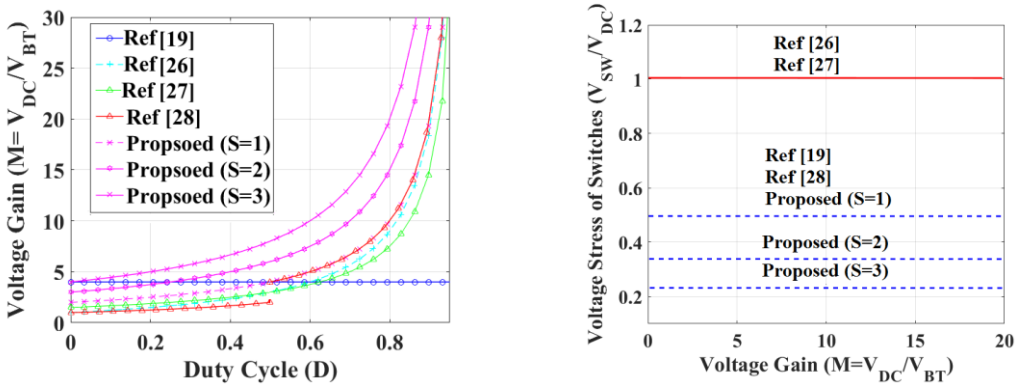
Regarding the cost of the converter, the utilization factor of semiconductors, as well as the number of components, can give a thorough insight into the expected cost of different topologies [29]. The utilization factor (U) is defined by

$$U = \frac{P_{out}}{qV_{pk}I_{pk}} \tag{4-40}$$

Where q is the number of switches, V_{pk} and I_{pk} are the maximum voltage and current of the switches. It is apparent from Table 4.2 that the proposed converter transfers the power from the battery to DC-link with the highest utilization factor, implying cheaper power conversion can be obtained using the proposed topology. Concerning the number of components, all the converters have the same number of active switches, except the converter introduced in [19]. However, the proposed converter does not require a bulky transformer to achieve high voltage gain; therefore, its cost is less as compared to other converters. Even though the switched-capacitor converter [19] lacks any inductor or transformer, its output voltage is weakly regulated, which impedes its utilization in EV application. Therefore, it can be concluded that the cost of the proposed circuit is lower than the others.

Regarding the control algorithm, the frequency modulation is used in converters [19] and [28] that brings about a wide range of current and voltage harmonics and complicates the design of inductor and capacitor because of the variable switching frequency; while simple,

easy-to-implement PWM control scheme is used in the proposed converter, converter introduced in [26], and converter introduced in [27]. As far as switching loss is concerned, the proposed converter can ensure ZVS turn-on for all switches that reduce the turn-on loss, which is a major loss in the bidirectional dc/dc converters. The soft-switching performance in other converters can be realized for several switches at specific operating points. Since it is vital that the size of the converter be as small as possible for EV application, using GaN switches in the proposed converter paved the way for high-frequency, high-efficiency operation. Employing GaN switches, the proposed converter provides advantages over Si-based counterparts with lower reverse recovery charge and smaller conduction resistance $R_{DS(on)}$, resulting in lower switching and conduction losses. Meanwhile, the switching losses in the current eGaN switches can be so small that the magnetic components are now the significant contributor to losses in the BDC converter, implying the proposed transformerless converter can lead to a noticeable improvement in the efficiency.



(a) (b)

Figure 4.14: Performance comparisons regarding the voltage gain and voltage stress of switches. (a) voltage gain. (b) voltage stress of switches.

Table 4.2: Performance comparison (V_{BT}= 150 V, V_{DC}= 600 V, P_{out}= 1 kW, and f_s= 100 kHz).

Item	Reference [19]	Reference [26]	Reference [27]	Reference [28]	Proposed Converter (P=S=1)
No. of Switches	8	4	4	4	4
No. of coupled inductor	0	0	1	0	0
No. of capacitors	5	2	4	3	4
Power (kW)	0.45	0.1	0.2	1	1
Frequency (kHz)	100-125	85	50	100	100
Efficiency (%)	96.4	-	95.44	93.2	97.5
V_{pk} (V)	300	600, 600, 150, 150	600, 600, 200,200	300	300
I_{pk} (A)	8,6,8,6,2,2,4,4	9,7,9,6	8,8,6,4	11,11,8,8	9, 8, 4, 7
U	0.083	0.084	0.109	0.087	0.119
Soft switching	ZCS at turn-off and turn-on for all switches	ZVS for narrow load range	ZVS at turn-on for all switches	ZVS at turn-on for two switches	ZVS at turn-on for all switches
Voltage regulation	Weakly regulated	Highly regulated	Highly regulated	Highly regulated	Highly regulated
Power Control	Frequency Modulation	PWM	PWM	Frequency Modulation	PWM

Figure 4.14 (a) and (b) show the voltage gain and voltage stress of switches under the different number of series-connected modules (S) for different BDC converters, respectively. The voltage gain of converter introduced in [19] entirely depends on the number of switched-capacitor stages, independent of the duty cycle that narrows the voltage regulation capability of the converter for a wide range of battery voltage. The

voltage gain of converter introduced in [26] and [27] is considerably lower than that of the proposed converter. It is noteworthy to mention that the voltage gain increases with increasing the number of series-connected modules in the MQRB converter. In converter introduced in [28], the voltage gain definition for duty-cycle values less than 0.5 is different than that of duty-cycle higher than 0.5. Therefore, the control scheme would be more complex to regulate the DC-link voltage.

4.6 Simulation and Experimental Results

4.6.1 Simulation Results

In this section, the simulation results of a 1 kW, 100 kHz prototype are given to prove the theoretical analysis and operation principle of the proposed modular converter. The specifications of the laboratory prototype are summarized in Table 4.3. The simulation is performed using LT Spice software and a model of GaN switches provided by GaN Systems Inc. Furthermore, the parasitic components of the switches are included in the simulation, which are derived from PCB layout using Q3D Extractor.

To demonstrate the potential of the proposed converter and its suitability for high-power and high-voltage applications, three case studies are investigated in this section: 1) Case study I: single-phase MQRB converter with battery voltage V_{BT}=122 V, P_{out}=1 kW, V_{DC}=600 V, D=0.6, and P=S=1. 2) Case study II: MQRB converter with battery voltage V_{BT}=53 V, P_{out}=1 kW, V_{DC}=600 V, D=0.6, and S=4. 3) Case study III: MQRB converter with battery voltage V_{BT}=120 V, P_{out}=1 kW, V_{DC}=600 V, D=0.63, and P=4 and S=1.

2) **Case Study I (single-phase MQRB converter with battery voltage V_{BT}=122 V, P_{out}=1 kW, V_{DC}=600 V, D=0.6, and P=S=1):**

Figure 4. 15 shows the simulation results for the single-phase MQRB converter as a building block of the proposed multiphase converter. The battery voltage, voltage across the output capacitors, and DC-link voltage are demonstrated in Figure 4. 15(a).

Table 4.3: Parameters of the prototype.

Parameters	Value
Input Voltage	80-150
Output Voltage	600V
Output Power	1 kW
Frequency	100 kHz
Output capacitors C_{O1} and C_{O2}	20 uF
Auxiliary Capacitor C_r	1 uF
Switches	GS66508T (650 V, 30 A, $R_{DS(on)}$ of 50 mΩ)
Input Inductor L_B	300 uH
Resonant Inductor L_r	3.5 uH

The current of boost inductor and resonant inductor are shown in Figure 4.15 (b). The voltage stress of switches S_M and S_C are depicted in Figure 4.15 (c). Figure 4.15 (d) shows the voltage stress of switches S_L and S_H. It is clear that the voltage stress is 300V, and voltage spikes are less than 10% which are acceptable; so, the clamp circuit works effectively to limit the voltage stress. Figure 4.15 (e), (f), (g), and (h) exhibit the soft-switching performance during turn-on operation for all switches S_M, S_C, S_L, and S_H, respectively. It is evident that the switches are conducting the current before the corresponding gate-pulse is applied. So, the soft-switching performance at turn-on instant is guaranteed for all switches at the full-load condition.

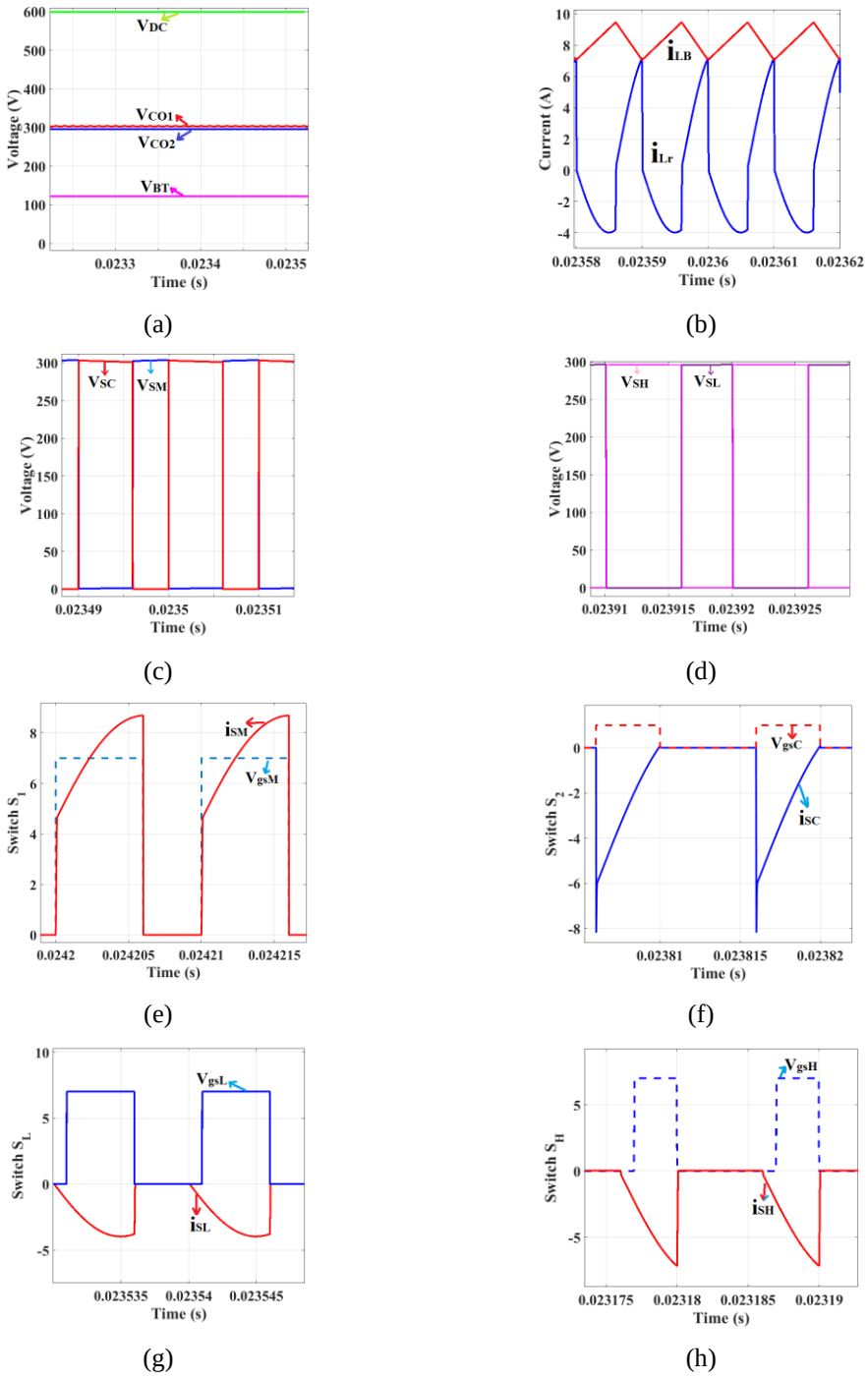


Figure 4.15: Simulation results for case I (battery voltage V_{BT}=122 V, P_{out}=1 kW, V_{DC}=600 V, D=0.6, and P=S=1). (a) Voltage of battery, DC-link, and output capacitors. (b) Current of inductors i_{LB} and i_{L4}. (c) Voltage stress of switches S_M and S_C. (d) Voltage stress of switches S_L and S_H. (e) gate-source voltage and current of main switch S_M. (f) gate-source voltage and current of clamp switch S_C. (g) gate-source voltage and current of switch S_L. (h) gate-source voltage and current of switch S_H.

3) Case Study II (MQRB converter with battery voltage V_{BT}=53 V, P_{out}=1 kW, V_{DC}=600 V, D=0.58, and S=4):

The simulation results for case study II are presented in Figure 4.16 to verify that the current and voltage stress are distributed equally among different modules shown in Figure 4.3. In this case, four modules (S=4) are connected in series to increase the voltage gain which is desired for high-voltage applications. The voltages of output capacitors C_{o1}-C_{o5} are shown in Figure 4.16 (a). It is obvious that the control circuit is working correctly to distribute the DC-link voltage V_{DC} equally among the output capacitors. Moreover, due to the use of active clamp configuration, the voltage stress of switches would be equal to the voltage of the output capacitor in each module. For instance, the voltage stress of switches in module 4 and 5 are shown in Figure 4.16 (b) and (c), respectively. It can be concluded that the voltage stress of each switch is limited, which paves the way for utilizing the switches with small on-resistance $R_{DS(on)}$. The current of resonant inductors i_{Lr1}, i_{Lr1}, i_{Lr1}, and i_{Lr1} are shown in Figure 4.16 (d). It is clear that the maximum values of the current of the resonant inductors are equal, implying the power processed by different modules is identical. The current of switches S_{L1}, S_{L2}, S_{L3}, and S_{L4} are illustrated in Figure 4. 16 (e), confirming the current stress of lower switches in all the modules are the same. The current of switches S_{H1}, S_{H2}, S_{H3}, and S_{H4} are presented in Figure 4. 16 (f) as well, which are approximately identical. To investigate the current sharing capability for different modules, the RMS values of the current of the resonant inductors, the current of lower switches, and the current of upper switches are given in Table 4.4. It can be clearly understood that the RMS current values of all the switches and inductors are the same in different modules.

So, the similar components can be employed to synthesize MQRB converter for any applications requiring a specific voltage and power level.

4) **Case Study III (MQRB converter with battery voltage V_{BT}=120 V, P_{out}=1 kW, V_{DC}=600 V, D=0.63, and P=4 and S=1):**

Figure 4.17 illustrates the simulation results for case study III when battery voltage is 122 V, the duty-cycle D=0.6, the output power P_{out}=1 kW, DC-link voltage V_{DC}=600 V, and the number of paralleled modules in Figure 4.3 is equal to P= 4. The main aim of this case study is to investigate the current sharing capability of the converter among different modules. The current of input boost inductors L_{B1}-L_{B4} are shown in Figure 4.17 (a). The maximum and minimum values of the boost inductor current are equal, implying the same boost inductors can be used in different modules. The current of resonant inductors i_{Lr1}, i_{Lr2}, i_{Lr3}, and i_{Lr4} are shown in Figure 4.17 (b). It is evident that the maximum values of the resonant inductors' current are equal, implying the power processed by different modules is identical. Figure 4.17 (c) and (d) present the current of main switches S_{M1}-S_{M4} and clamp switches S_{C1}-S_{C4} in different modules, respectively. The current of switches S_{L1}, S_{L2}, S_{L3}, and S_{L4} are illustrated in Figure 4. 16 (e), confirming the current stress of lower switches in all the modules are the same in this scenario. The current of switches S_{H1}, S_{H2}, S_{H3}, and S_{H4} are presented in Figure 4. 16 (f) as well. To investigate the power-sharing capability for the various number of modules, the RMS values of the resonant currents, the current of lower switches, and current of upper switches are given in Table 4.5. It can be clearly understood that the RMS current values of all the switches and inductors are the same in different phases. Therefore, the similar components, including the switches and inductors,

can be employed to synthesize MQRB converter for any applications requiring a specific voltage and power level.

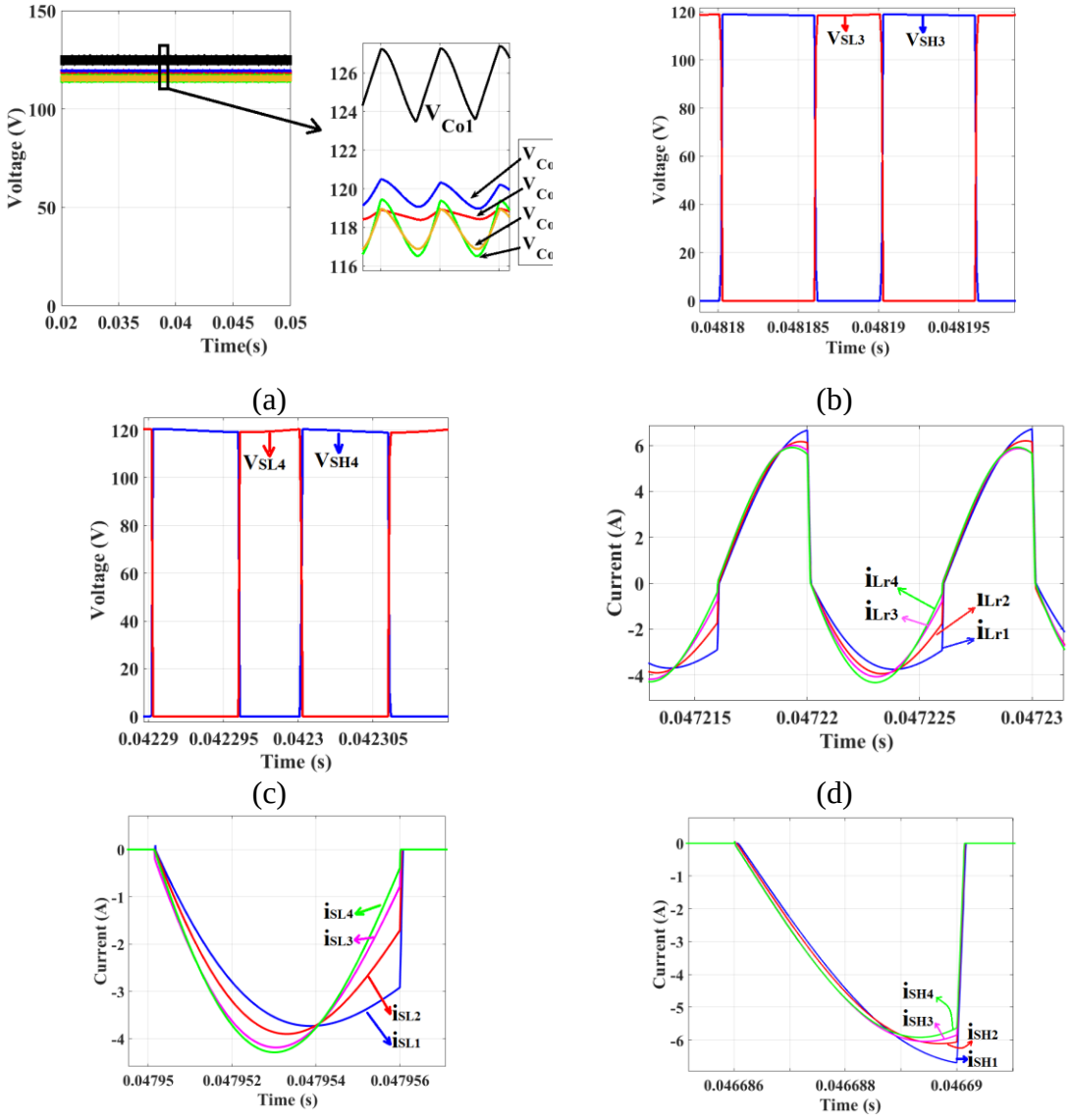


Figure 4.16: Simulation results for case study II (battery voltage V_{BT}=53 V, P_{out}=1 kW, V_{DC}=600 V, D=0.58, and S=4). (a) Voltage of output capacitors C_{o1}-C_{o5}. (b) Voltage stress of switch S_{L3} and S_{H3}. (c) Voltage stress of switch S_{L4} and S_{H4}. (d) Inductor current i_{Lr1}-i_{Lr4}. (e) Current of lower switches in each module i_{SL1}- i_{SL4}. (f) Current of upper switches in each module i_{SH1}- i_{SH4}.

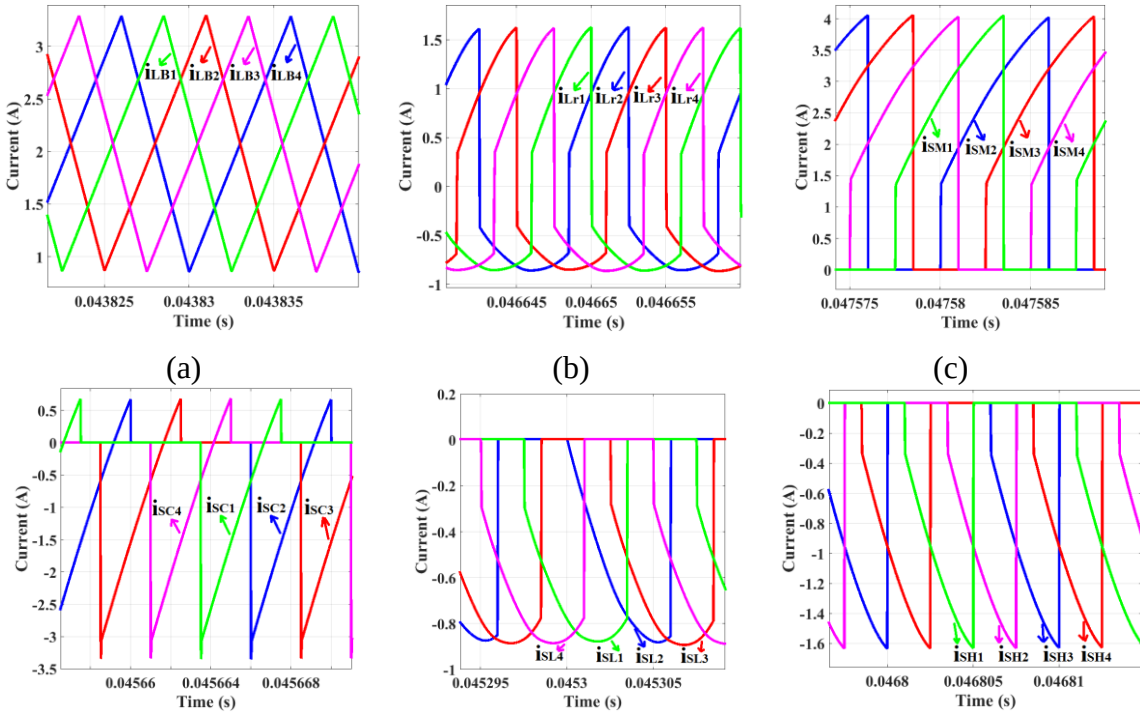


Figure 4.17: Simulation results for case study III (battery voltage V_{BT}=120 V, P_{out}=1 kW, V_{DC}=600 V, D=0.63, and P=4). (a) current of main switches i_{SM1}- i_{SM4}. (b) current of clamp switches i_{SC1}- i_{SC4}. (d) Inductor current i_{Lr1}-i_{Lr4}. (e) Current of lower switches in each module i_{SL1}- i_{SL4}. (f) Current of upper switches in each module i_{SH1}- i_{SH4}.

Table 4.4: RMS current of switches in case study II (battery voltage V_{BT}=53 V, P_{out}=1 kW, V_{DC}=600 V, D=0.58, and S=4).

Component	**Lower Switches**				**Upper switches**			
	i_{SL1}	i_{SL2}	i_{SL3}	i_{SL4}	i_{SH1}	i_{SH2}	i_{SH3}	i_{SH4}
Values (A)	1.665	1.653	1.676	1.665	1.665	1.655	1.678	1.666

4.6.1 Experimental Results

A laboratory prototype with specifications given in Table 4.3 is implemented to validate the performance of MQRB converter shown in Figure 4.2 and confirm that noteworthy gains in efficiency and power density can be made.

The control circuit is implemented by a TMS320F28377S microcontroller. The power switches GS66508T E-HEMTs (650 V, 30 A, $R_{DS(on)}$ of 50 mΩ) are employed in the prototype. Controlling the voltage and current variation, di/dt and dv/dt, are the main challenge of using eGaN HEMTs, requiring adherence to particular PCB design regarding the parasitic elements. Previous studies have illustrated that to reach optimal performance in terms of low package inductance and high slew rate of switches, designing a PCB with low common source inductance, power loop inductance, and gate-driver loop are principal [1-2].

Table 4.5: RMS current of inductors and switches in case II (battery voltage V_{BT}=120 V, P_{out}=1 kW, V_{DC}=600 V, D=0.63, and P=4).

Component		RMS Value
Resonant Inductors	i_{Lr1}	0.8753
	i_{Lr2}	0.8753
	i_{Lr3}	0.8751
	i_{Lr4}	0.8756
Main Switches	i_{SM1}	1.76
	i_{SM2}	1.756
	i_{SM3}	1.757
	i_{SM4}	1.759
Clamp switches	i_{SC1}	0.5016
	i_{SC2}	0.5003
	i_{SC3}	0.5008
	i_{SC4}	0.5012
Lower Switches	i_{SL1}	0.4414
	i_{SL2}	0.4413
	i_{SL3}	0.4418
	i_{SL4}	0.4419
Upper Switches	i_{SH1}	0.4339
	i_{SH2}	0.4338
	i_{SH3}	0.4339
	i_{SH4}	0.4334

Both common source inductance and power loop inductance cause huge overshoot on the drain-source voltage. But the power loop inductances are the most crucial that can increase the voltage spikes across the drain-source of the switch. So, of great importance is that the power loop inductances be as low as possible. Also, to avoid false turn-on and turn-off, common source inductance should be minimized by connecting the ground pin of the driver directly to the source pin of the switch, which results in alleviation of the impact of power path on the driver circuit. As far as adopting GaN switches is concerned, placement of components on PCB plays an essential role in reducing these parasitic inductances.

In this chapter, to minimize the parasitic inductance, all switches S_M, S_C, S_L, and S_H are mounted on the top layer of PCB, and decoupling capacitors are placed on the bottom-side, shown in Figure 4.18 (a) and (b). Moreover, a 4-layer structure of PCB paves the way to crease the parasitic inductance by putting the cooper polygon in parallel in 4 layers and placing the switches very close to each other. As shown in Figure 4.18 (c), the current paths are stretched into the large planes in all layers, acting like an interleaved configuration; therefore, the parasitic inductance considerably will be small. As a practical solution to lower the gate driver loop inductance, the driver circuits are mounted precisely beneath the switches to lessen the length of the driving loop. By making the gate loop perpendicular to the power loop, the parasitic elements are minimized in this design.

The converter performance at full load 1 kW during forward mode is shown in Figure 4.19. The gate signals for forward mode is shown in Figure 4.19 (a), indicating the duty-cycle is about 0.72.

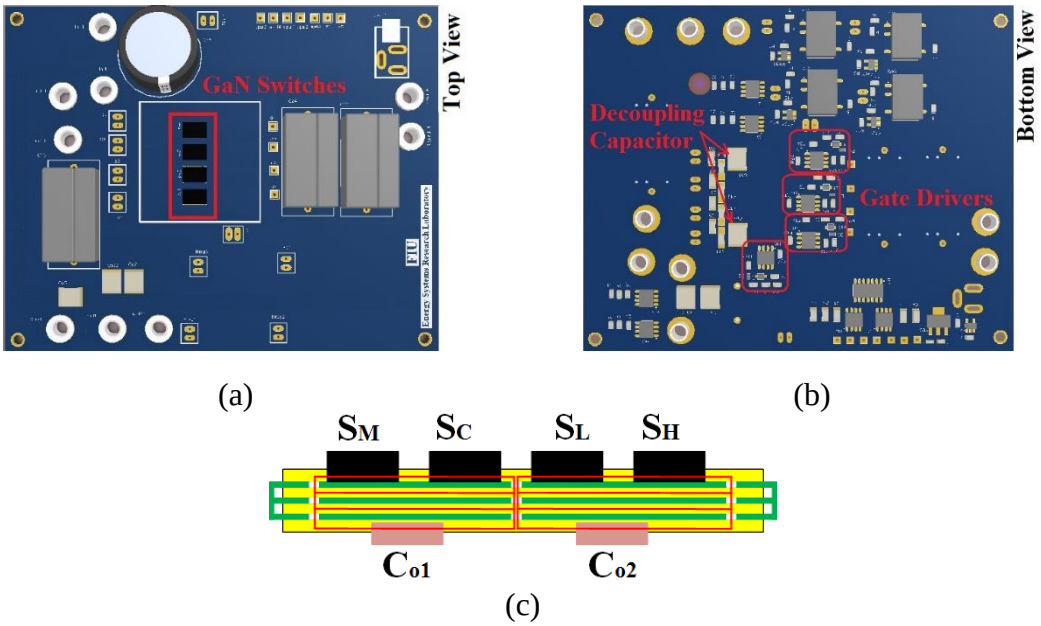


Figure 4.18: Layout of single-phase MQRB converter; (a) Top view. (b) Bottom view. (c) Side view.

Figure 4.19 (b) indicates that the clamp circuit is reducing the voltage stress of switches S_M and S_C. Figure 4.19 (c), (d), and (e) show the gate pulse and voltage stress on the switches S_M, S_C, and S_H, respectively. As it is clear ZVS soft-switching performance is achieved for all switches. The inductor current I_{LB} and the gate signal of switch S_M are illustrated in Figure 4.19 (f). Since the conventional DC/DC converters lose the soft-switching performance at light load, the converter performance at light load is investigated from an efficiency viewpoint. So, a test is made for output power 100 W, shown in Figure 4.20. The battery voltage V_{BT}, the voltage of output capacitors V_{CO1} and V_{CO2}, and DC-link voltage V_{DC} are shown in Figure 4.20 (a). It is clear the voltage of output capacitors is balanced, and the control circuit is working correctly. The gate pulses of switches in boost mode are shown in Figure 4.20 (b), in which duty-cycle is 0.5. There is no voltage ringing caused by parasitics in the gate pulses, implying the design of gate driving circuit in PCB layout is carried out correctly. The gate signals and voltage stress across switches S_M, S_C,

S_L, and S_H are shown in Figure 4.20 (c), (d), (e), and (f), respectively. The voltage stress of all switches is 300 V, which is half of the output voltage. Thus, low voltage switches with low conduction resistance $R_{DS(on)}$ can be used. The voltage spike on switch S_C is more than other switches, 40 V, which is less than 15%, which implies the effectiveness of the PCB layout design using the interleaving method. Figure 4.20 (c) depicts the detailed turn-on instant for the switch S_M at 100 W, illustrating ZVS is realized even under light load condition.

The backward mode operation results are presented in Figure 4.21. Figure 4.21. (a) represents the gate pulses of switches. The delay between the gate pulse of switches S_C and S_H is 2us. The gate pulse and voltage stress across the switches S_M, S_C, S_L, and S_H are shown in Figure 4.21 (b), (c), (d), and (e), respectively. These figures provide evidence that the soft switching at turn-on instant is achieved in buck mode. The experimental results also suggest that the control scheme is working properly in both operation modes, forward and backward. Considering that the size of switches is very small and adding any component for measurement can increase the parasitics in the PCB layout, figuring current waveforms is impractical. Monitoring the temperature of switches by taking an infrared thermal photo is the efficient way to analyze their performance. The FLIR ONE Pro thermal imaging camera with a thermal resolution of 160x120 is used to observe the thermal operating point of the proposed converter.

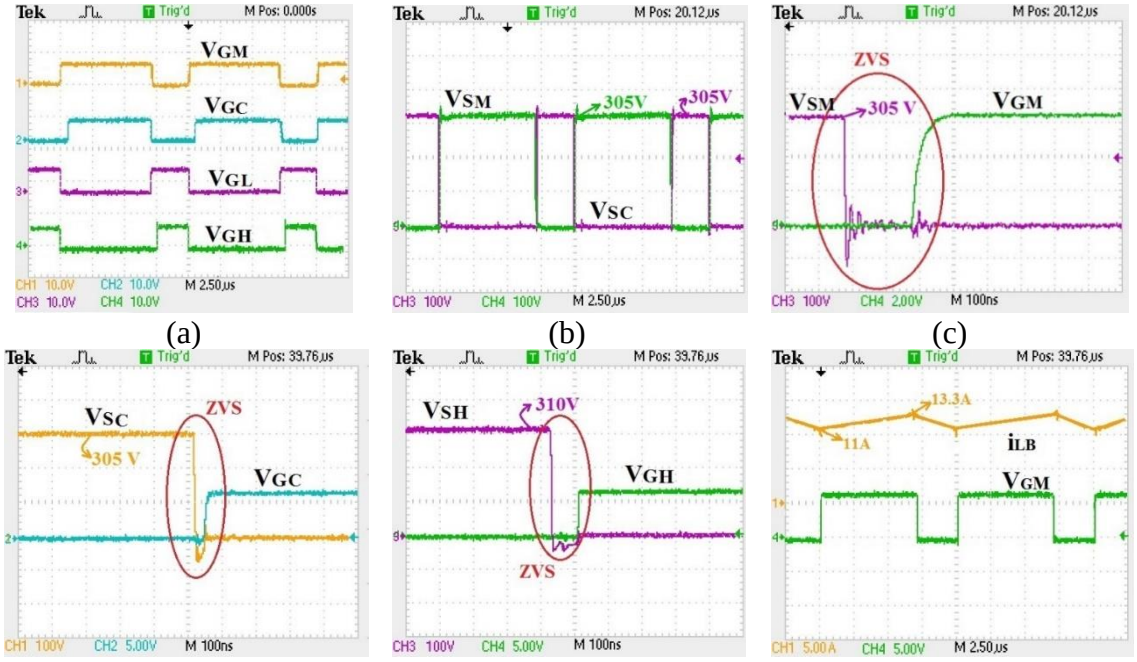
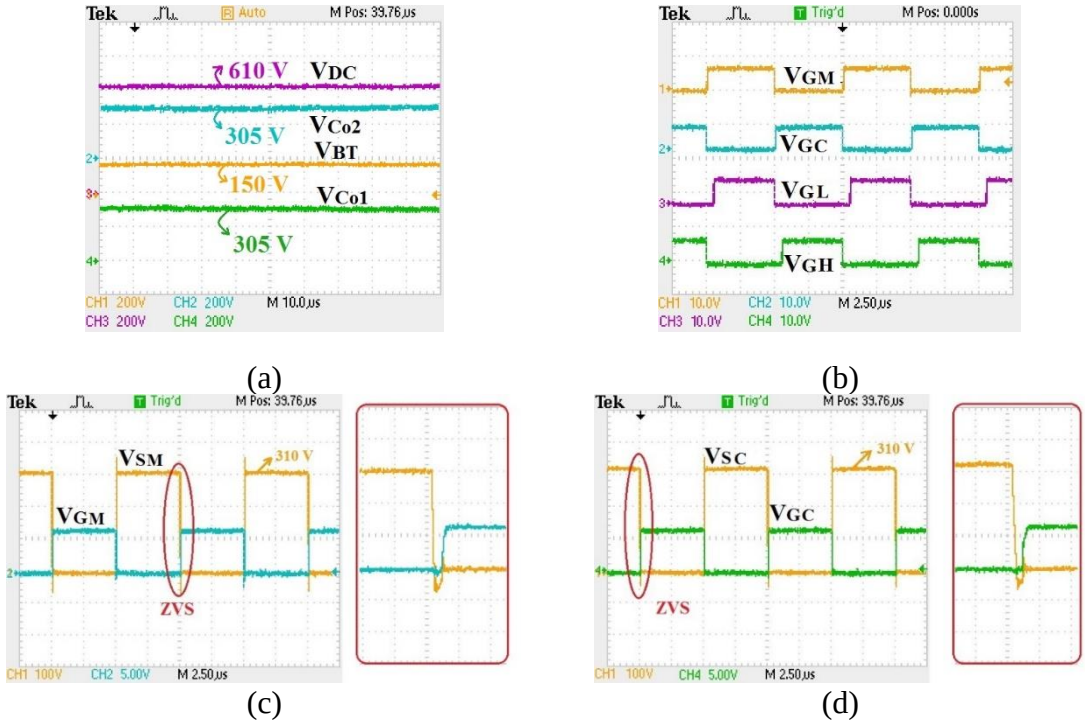
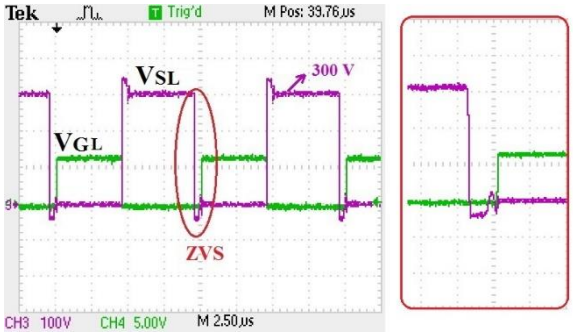
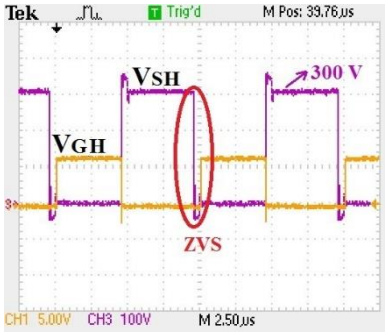


Figure 4.19: Experimental results of forward mode at full load condition when D=0.72 (V_{BT} = 85 V, V_{DC} = 600 V, P_O = 1 kW). (a) Gate-source voltage of switches. (b) Drain-source voltage of switches S_M and S_C (c) Gate-source and drain-source voltage of switch S_M. (d) Gate-source and drain-source voltage of switch S_C. (e) Gate-source and drain-source voltage of switch S_H. (f) Gate-source voltage of switch S_M and inductor current i_{LB}.



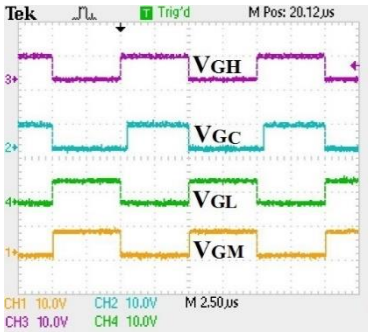


(e)

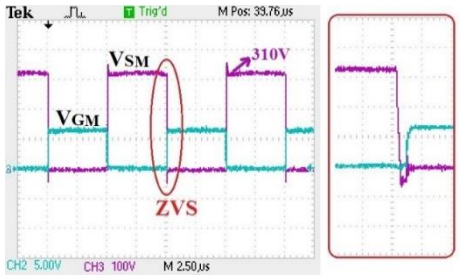


(f)

Figure 4.20: Experimental results of forward mode at light load when D=0.5 (V_{BT} = 150 V, V_{DC} = 600 V, P_O = 100 W). (a) Battery voltage, High-side voltage, voltage across capacitors C_{O1} and C_{O2}. (b) Gate-source voltage of switches. (c) gate-source and drain-source voltage of switch S_M. (d) gate-source and drain-source voltage of switch S_C. (e) gate-source and drain-source voltage of switch S_L. (f) gate-source and drain-source voltage of switch S_H.



(a)



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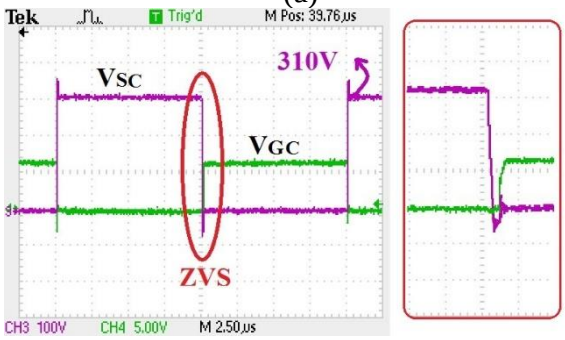
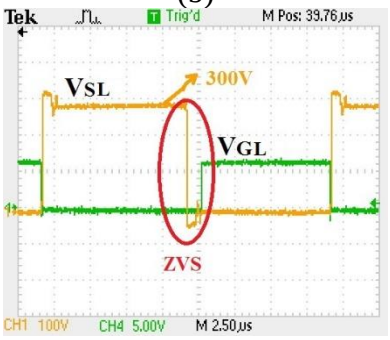


(c)



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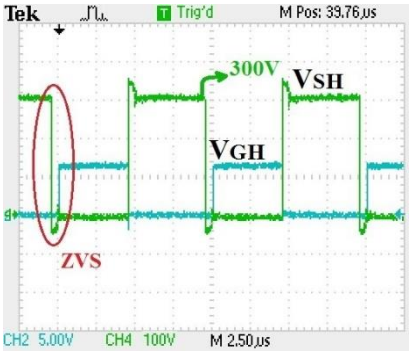
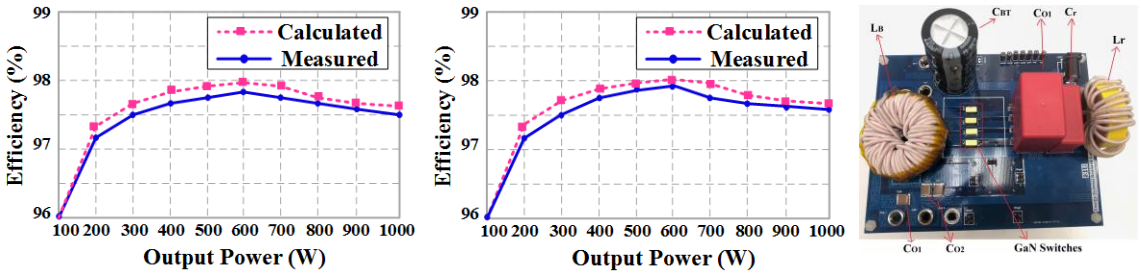


(e)

(f)

Figure 4.21: Experimental results of backward mode at full load when D=0.5 (V_{BT} = 150 V, V_{DC} = 600 V, P_O = 1000 W). (a) Gate-source voltage of switches. (b) Gate-source and drain-source voltage of switch S_M. (c) Gate-source and drain-source voltage of switch S_C. (d) Gate-source and drain-source voltage of switch S_L. (e) Gate-source and drain-source voltage of switch S_H. (f) Thermal image of the converter.

Figure 4.21 (f) shows the IR image of eGaN devices at full load condition, indicating that maximum temperature is 72 °C and the switches are working in acceptable condition. The calculated efficiency and the experimental efficiency curves for forward mode and backward mode are given in Figure 4. 22 (a) and (b), respectively. The calculated and experimental efficiency in forward mode under full load condition is 97.7 % and 97.5 %, respectively. The maximum calculated and experimental efficiency in forward mode is achieved at 600 W, which are 97.9 % and 97.7 %, respectively. The calculated and experimental efficiency in forward mode under full load condition is 97.8 % and 97.6 %, respectively. The maximum calculated and experimental efficiency in forward mode is achieved at 600 W, which are 98.0 % and 97.7 %, respectively. The prototype of the single-phase MQRB converter is shown in Figure 4. 22 (c).



(a) (b) (c)

Figure 4.22: Efficiency curves and a photograph of the converter. (a) Calculated and measured efficiency in forward mode. (b) (a) Calculated and measured efficiency in backward mode. (c) A photograph of laboratory prototype.

4.7 Conclusion

In this chapter, a modular, quasi-resonant bidirectional dc/dc converter has been presented as an interface between the battery and high-voltage bus in EV system. The steady-state operation of the converter in both boost and buck mode has been presented. To show the effectiveness of the proposed configuration, a thorough comparison has been made with other competitive candidates for EV applications. A 1 kW, 100 kHz, 600 V prototype has been implemented to verify the proposed modular concept. Analysis of the experimental results show the following: 1) the voltage stress of switches is reduced in proportion to the number of modules; so, switches with lower drain-source resistance can be used. 2) A resonant circuit is formed that enables the soft-switching performance even under light load condition. 3) Modularity of proposed topology helps the designer to employ the modules in such a way that different needs of various applications can be met. 4) Due to the small package, zero reverse-recovery, fast switching speed, and small gate charge, use of GaN switches brings about reduction in the losses and the size of the converter.

Chapter 5 A Multilevel Bidirectional Buck-Boost Converter with Distributed Voltage Stress Using eGaN HEMTs

5.1 Introduction

A modular multi-level bi-directional diode-clamped DC-DC converter based on enhancement Gallium Nitride (eGaN) High Electron Mobility Transistor (HEMT) is proposed as a plugin charger for electric vehicles (EVs). The eGaN HEMT can switch efficiently even in hard switching, but their problem is that they cannot tolerate voltage stresses higher than 650V. The proposed multilevel topology reduces the voltage stress across the switches which enables utilizing eGaN HEMT technology in the powertrain of the EVs. Simulations were carried out in LTSpice environment using the eGaN equivalent circuit provided by the manufacturer. The simulation results prove that the performance of the proposed converter complies with the theoretical analysis.

5.1 Proposed converter and its Operation Modes

5.1.1 The Proposed Converter

The proposed modular converter is shown in Figure 5.1, where the GaN HEMTs utilized are modeled as in Figure 5.2. The proposed converter operates like a conventional bi-directional buck/boost converter with a neutral point clamped leg. The configuration of the converter has a filter inductance L_B to reduce the current ripple at the Low Voltage (LV) port. Also, the High Voltage (HV) port consists of a number of *n* switched-capacitor cells to increase the output voltage level to *n*+1. Therefore, this modular converter allows the designer to manage the voltage stress across the semiconductor devices systematically.

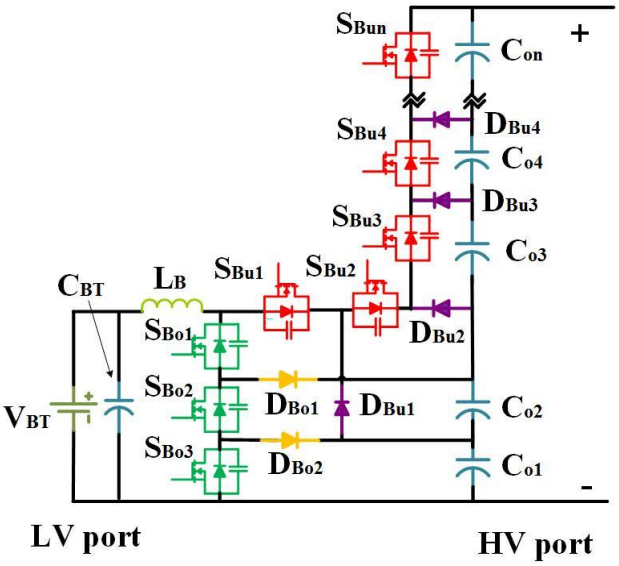


Figure 5.1: Circuit diagram of the Proposed Modular Converter

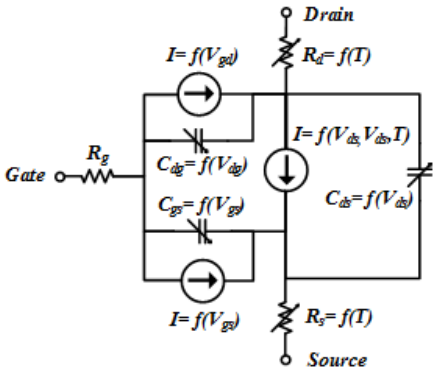
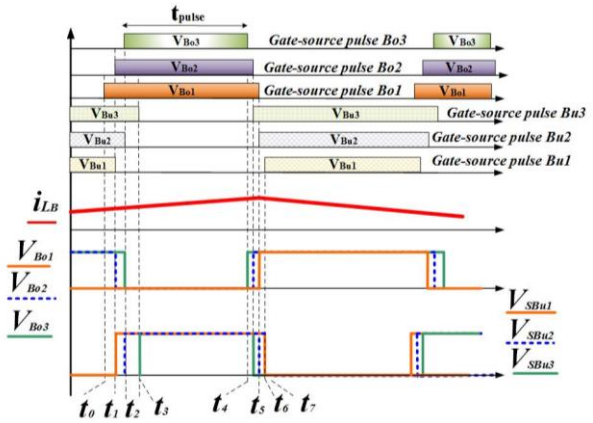


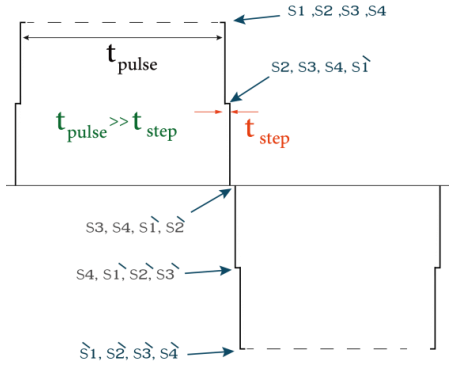
Figure 5.2: GanSys Model GS66508P PSpice equivalent model.

The operation of the proposed converter is similar to the conventional bidirectional buck-boost converter. The boost mode is related to the traction of the EV. The buck mode is for battery energy injection which can occur in two cases: regenerative braking on the motor or connecting the battery to the power source (utility grid). The steady-state operation

waveforms including the gate pulses of switches, the input inductor current $i_{LB,}$ and the voltage stress of switches are shown in Figure 5. 3(a).



(a)



(b)

Figure 5.3: Steady-state waveforms. (a) the gate pulse sequence. (b) the switching sequence of the neutral point clamped leg.

5.1.2 Operation Intervals

Interval 1 (t_0-t_1): Before t_0, the buck switches S_{Bu1}, S_{Bu2}, and S_{Bu3} are conducting the current. As depicted in Figure 5. 4(a) and Figure 5. 3(a), the gate pulse of the boost switch S_{Bo1} is applied and the voltage stress of boost switches S_{Bo2} and S_{Bo3} is limited to the voltage of the output capacitors C_{o1}+C_{o2}. During this interval, the input energy has been stored in the inductor.

Interval 2 (t_1-t_2): After a short-time delay, the boost switch S_{Bo2} turns on and the voltage stress of boost switches S_{Bo3} are limited to the voltage of output capacitor C_{o1}. Figure 5. 4(b) shows the current path during this interval.

Interval 3 (t_2-t_3): After a short-time delay, the boost switch S_{Bo3} turns on. During this mode, all of the input energy would be stored in the inductor. As shown in Figure 5. 4(c), this operation mode is similar to the conventional boost converter except that the voltage stress is distributed amongst switches.

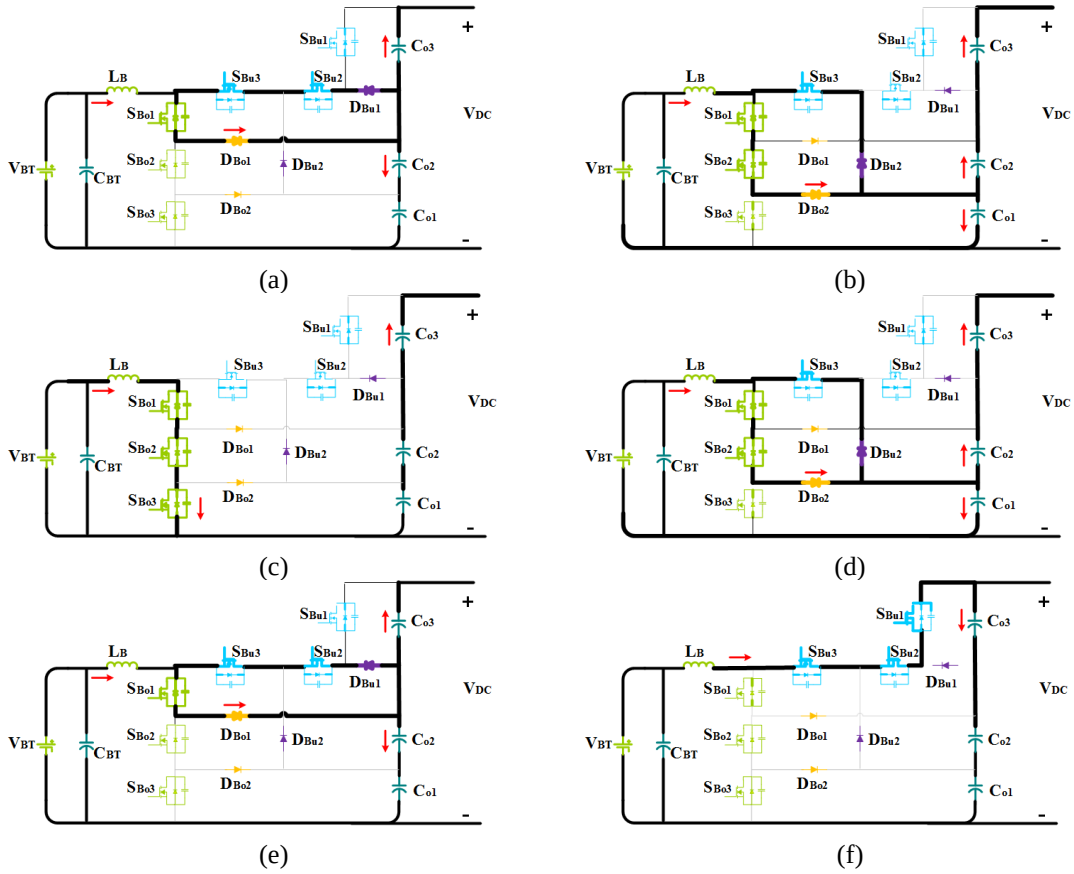


Figure 5.4: Boost Operation Modes. (a) mode1; (b) mode2; (c) mode 3 and (d) mode4; (e) mode 5; (f) mode 6.

Interval 4 (t_3-t_4): As depicted in Figure 5. 4(d), after a short time delay the boost switch S_{Bo3} will turn off and the buck switch S_{Bu3} will turn on. Similar to what happened during Interval 2, the voltage stress of switch S_{Bo3} is limited to the voltage of output capacitor C_{o1}.

Interval 5 (t_3-t_4): After a short-time delay, the boost switch S_{Bo2} will turn off and the buck switch S_{Bu2} will turn on. In this mode, the diode D_{Bu1} starts to conduct the current. Figure 5. 4(e) shows the current path during this interval.

Interval 6 (t_3-t_4): As shown in Figure 5. 4(f), after a short time delay, all boost switches will turn off and all buck switches conduct the current. In turn, the inductor will release the stored energy to the output capacitors.

5.2 Control Algorithm

A design example of a 5-level neutral point clamped leg is shown in Figure 5. 5. For this leg, five voltage levels can be realized, namely: $-V_{DC}$, $-V_{DC}/2$, 0, $V_{DC}/2$ and V_{DC}. The switching sequence associated with each voltage level is shown in Figure 5. 3(b). t_{pulse} is the time of $V_{DC}/2$ or $-V_{DC}/2$ realization (= DT_s), and t_{step} is the time that separates the two consecutive levels. This time is extremely small (in the range of 10 ns to 100 ns) as compared to t_{pulse}. The square-wave voltage with fine stepping requires a dedicated circuit to provide the gate pulses for the 8 power switches of the NPC inverter.

The proposed control scheme is shown in Figure 5. 5. The circuit provides the fine stepping by means of monostable timers. The firing circuit is fed with a reference square waveform (P) where negative and positive edge detectors fire short pulses at each edge of P. These short pulses are then fed to monostable timers. $V_{DC}/2$ and $-V_{DC}/2$ have two designated monostable timers, one which fires a high pulse at the edge of P with a pulse width of ($2t_{\text{step}}+t_{\text{pulse}}$) and the other firing a low pulse at the edge of P with a pulse width of $2t_{\text{step}}$.

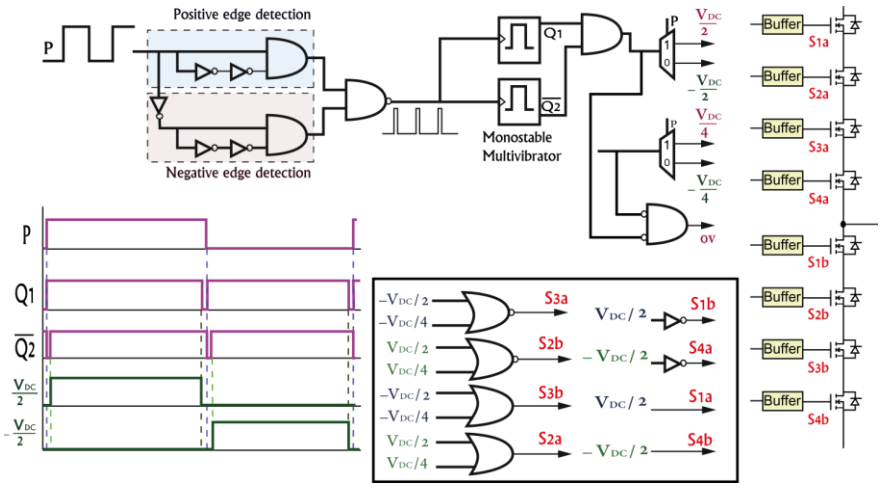


Figure 5.5: The proposed control scheme of the 5-level NPC leg.

Passing the output of the two monostable timers through an AND gate produces the reference pulse width of $V_{DC}/2$ or $-V_{DC}/2$. A demultiplexer is used to select whether the reference pulse generated is for $V_{DC}/2$ or $-V_{DC}/2$. The same technique is used to generate the reference pulses of $V_{DC}/4$ or $-V_{DC}/4$. There are another two monostable timers designated for these voltage levels, one of which fires a high pulse at the edge of P with a pulse width of $(3t_{step}+t_{pulse})$ and the other fires a low pulse at the edge of P with a pulse width of t_{step}. Passing the output of both timers through an AND gate generates the reference pulses for $V_{DC}/4$ or $-V_{DC}/4$. A demultiplexer selects whether the generated pulses are to be for a $V_{DC}/4$ or $-V_{DC}/4$ reference.

The reference for the 0 V voltage level exists whenever the reference of $-V_{DC}/2$, $V_{DC}/2$, $-V_{DC}/4$, or $V_{DC}/4$ does not exist. Combinational logic circuits, as shown in Figure 5. 5 use the reference pulses for each level of the NPC inverter to trigger the power switches associated with each voltage level. The buffer circuit has two functions: the first is to provide galvanic isolation between the control circuit and the power switches. The second

function is to translate the triggering pulses of the control circuit to the adequate voltage level required by the power switches.

5.3 Design Specification

There are some design parameters which affect the converter operation in terms of cost and reliability as well as other factors. To design a new converter with different input voltage and power, the following parameters should be considered.

5.3.1 Voltage Stress of the Switch

As was shown previously in Figure 5.4, the voltage stresses of the switches are effectively limited to the voltage of output capacitors which can be defined by:

$$V_{sw} = \frac{V_{DC}}{3} \tag{5-1}$$

Thus, for an *n* level modular converter which has *n*-1 output capacitors, the voltage stress equates to:

$$V_{sw} = \frac{V_{DC}}{n-1} \tag{5-2}$$

where V_{sw} is the voltage stress of the switches and V_{DC} is the voltage of DC-link.

5.3.2 Voltage Gain

For an *n* level modular converter, the voltage gain can be defined as:

$$M = \frac{V_{DC}}{V_{BT}} = n - 1 \tag{5-3}$$

5.3.3 Input Inductance L_B

Input inductance operates like a filter to reduce the input current ripple. The value of this inductor can be calculated using the following equation:

$$L_B = \frac{V_{BT} D T_s}{0.2 I_{in}} \tag{5-4}$$

where the input current ripple is assumed to be 20%.

5.4 Simulation Results

To verify the theoretical analysis given in the previous section, a simulation is performed following the specifications of the GaNSys GS66508P given in Table I. The simulations are conducted in PSPICE where the PSPICE equivalent model is shown in Figure 5.2. The model consists of voltage controlled current sources with V_{gs} and V_{ds} dependence, parasitic capacitances (C_{dg}, C_{gs}, C_{ds}), temperature-dependent series resistances at the source (Rs) and drain (R_d), a gate resistance R_g, and alternate current sources to account for leakage currents. To verify the operation, the simulation results are shown in Figure 5.6.

The gate pulse of the boost switch S_{BO3}, buck switch S_{Bu3}, and current through the inductor are shown in Figure 5.6(a). In this figure, it should be noted that the pulses where implemented sequentially (with a very small delay in-between them) to limit the voltage stress on the main switches. Also, the inductor current shows linear behavior as was expected from the average model in (4). Figure 5.6(b) shows the battery voltage V_{BT}, DC-link voltage V_{DC} and gate pulse of switches S_{Bu3} and S_{Bo3} during the boost mode operation. In this mode, the voltage stress of all switches are half of the battery voltage. The voltage stress of buck switch S_{Bu1}, S_{Bu2}, and S_{Bu3} the boost switches S_{Bo1}, S_{Bo2}, and S_{Bo3} are shown in Figure 5. 6(c) and Figure 5. 6(d), respectively. Shown in the figure, all switches experience voltage stress lower than the output voltage at around 200 V, thus enabling the usage of GaN HEMT devices with lower ON-resistance and gate capacitance. Moreover, the modularity allows the designer to increase the output voltage for specific applications.

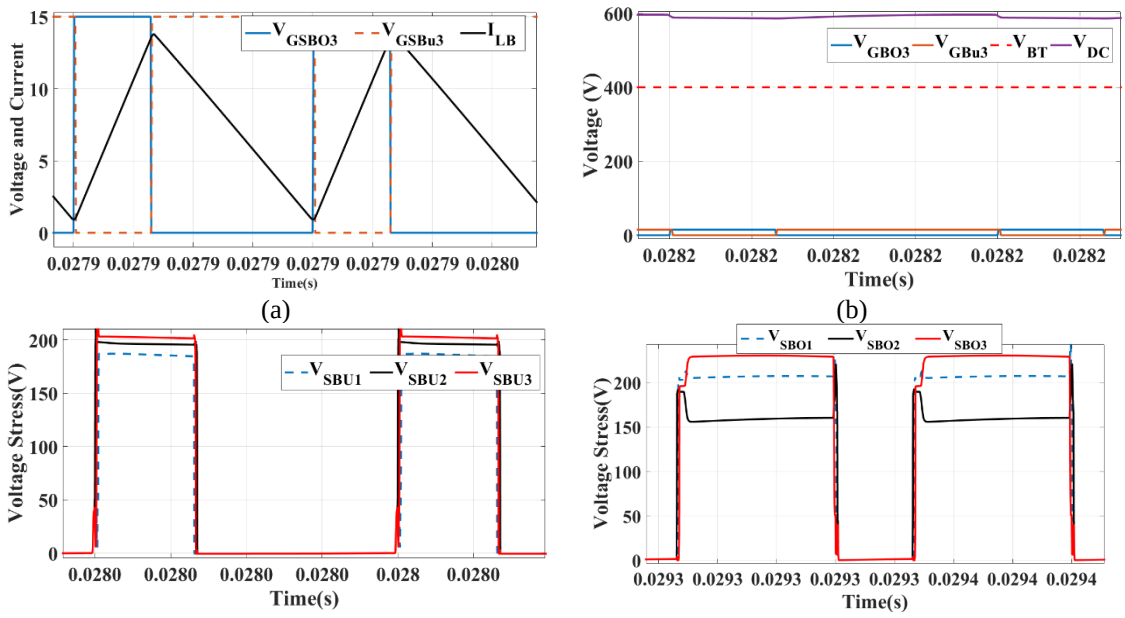


Figure 5.6: Simulation. (a) gate pulse of boost switch S_{BO3}, buck switch S_{Bu3}, and current of filter inductor I_{LB}; (b) gate pulse of boost switch S_{BO3}, buck switch S_{Bu3}, battery voltage and dc-link voltage; (c) voltage stress of buck switches S_{Bu1}, S_{Bu2}, and S_{Bu3}; (d) voltage stress of boost switches S_{Bo1}, S_{Bo2}, and S_{Bo3}.

5.5 Conclusion

A proposed structure for a bi-directional diode-clamped DC/DC converter based on GaN devices was presented. The converter is based on the switched capacitor topology which effectively reduces voltage stress on the switches in this work. To deal with both concerns about low efficiency and power density in an EV application, GaN HEMT switching devices were used. A driving algorithm complements the proposed structure revealing the effectiveness of the converter. A simulation using PSPICE has been done for a 2 kW model using real GaN equivalent circuits obtained from the manufacturer. The simulation results confirm the correctness of theoretical analysis and its driver-circuit performance.

Chapter 6 A Voltage-Quadrupler Interleaved Bidirectional DC-DC Converter with Intrinsic Equal Current Sharing Characteristic for Electric Vehicle Applications

6.1 Introduction

A voltage-quadrupler interleaved bidirectional DC-DC converter with intrinsic equal current sharing is presented in this chapter. The proposed converter offers a wide voltage conversion ratio, which makes it suitable for interconnecting the energy storage unit with dc-bus for electric vehicle applications. A high voltage gain and low voltage stress across switches are achieved by adopting the capacitive voltage-divider stage, which enables the designer to employ a low-voltage switch with a small on-resistance $R_{DS(ON)}$. As a result, it allows the converter to run more efficiently and cooler. An interleaved connection at the low-voltage side paves the way for reducing the current ripple, which reduces the filter size and increases the power-density. Moreover, a built-in equal current sharing is achieved for two interleaved phases without using a current-sharing control scheme. The operating principle, steady-state characteristics including the current and voltage stress of the switches, and comparison with other state-of-the-art bidirectional converters are carried out in detail. Finally, to verify theoretical analysis, a 2kW scaled-down laboratory prototype of the proposed converter using Gallium-Nitride switches is implemented.

6.2 Structure and Operating Principles of the Proposed Converter

6.2.1 Circuit Structure of the Proposed Topology

The schematic of the SGIBC is depicted in Figure 6.1. The proposed topology consists of an interleaved stage (L_1, L_2, S_1, and S_2), and the voltage quadrupler stage (C_{C1}, C_{C2}, C_{H1} and C_{H2}, S_3, S_4, S_5, and S_6), and LVS filter capacitor C_L. Meanwhile, the capacitors C_{H1} and C_{H2} operate as high-voltage side filter capacitors. The proposed circuit can work either in the forward or backward mode, which allows the U_C connected to the LVS and dc-bus interchange the power. To simplify the analysis, it is assumed that all components are ideal, so the on-resistance $R_{DS(on)}$ of the switches and equivalent series resistance R_{ESR} of passive components can be neglected. Moreover, the capacitors can be considered as a voltage source since their capacitance are high.

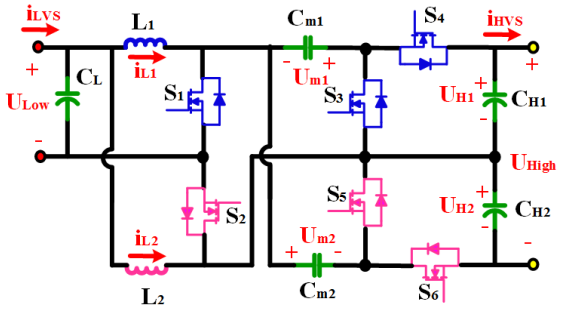


Figure 6.1: The schematic of the proposed converter.

6.2.2 Operation in Forward Mode

In this mode, the energy flows from LVS to high-voltage side (HVS), and the converter increases the voltage of UC to the desired level of dc-bus of EV (800 V). The equivalent circuits of the converter in different intervals with associated current paths are illustrated in Figure 6.2. The key waveforms of the converter in forward mode are shown in Figure 6.3 (a). Regarding the interleaved operation, switches S_1 and S_2 are driven by the gate

pulses with the same duty-cycle of d_F and a phase-shift of 180º. The gate pulse of switches S_3 and S_6 are complementary to that of switch S_1. Similarly, the gate pulse of switches S_4 and S_5 are complementary to that of switch S_2. High step-up gain characteristics of the proposed topology is favorable for EV application with UC, which can be realized when the converter is working in continuous-conduction-mode (CCM); therefore, the steady-state analysis is carried out based on this assumption that the duty-cycle is greater than 0.5. The operation intervals are described as follows.

Interval 1 [t_0~t_1]: Before this interval, switch S_2 is turned ON and the switch S_1 is turned OFF. At t_0, the gate pulse of switch S_1 is applied. The current flow paths in interval 1 is depicted in Figure 6.2(a). During this interval, both inductors L_1 and L_2 are charged by UC connected to LVS. Meanwhile, the load is supplied by the HVS capacitors C_{H1} and C_{H2}.

$$\frac{di_{L1}(t)}{dt} = \frac{di_{L2}(t)}{dt} = \frac{U_{Low}}{L} \tag{6-1}$$

$$\frac{dv_{CH1}(t)}{dt} = \frac{dv_{CH2}(t)}{dt} = -\frac{U_{High}}{R_{LF}} \tag{6-2}$$

$$\frac{dv_{Cm1}(t)}{dt} = \frac{dv_{Cm2}(t)}{dt} = 0 \tag{6-3}$$

Interval 2 [t_1~t_2]: At t_1, the gate pulse of switches S_4 and S_5 are applied. Concurrently, switch S_2 is turned OFF. Figure 6.2 (b) shows the equivalent circuit for this interval. The load and output capacitor C_{H1} are supplied by the energy stored of inductor L_2 and capacitor C_{C1}. At the same time, the capacitor C_{C2} is charged by energy stored of L_2.

$$\frac{di_{L1}(t)}{dt} = \frac{U_{Low}}{L} \tag{6-4}$$

$$\frac{di_{L2}(t)}{dt} = \frac{U_{Low} - U_{m1}}{L} \tag{6-5}$$

$$\frac{dv_{Cm1}(t)}{dt} = \frac{i_{Cm2} - i_{L2}}{C_{m1}} \tag{6-6}$$

$$\frac{dv_{Cm2}(t)}{dt} = \frac{i_{Cm1} + i_{L2}}{C_{m2}} \tag{6-7}$$

$$\frac{dv_{CH1}(t)}{dt} = -\frac{U_{High}}{R_{LF}} \tag{6-8}$$

$$\frac{dv_{CH2}(t)}{dt} = i_{Cm2} - \frac{U_{High}}{R_{LF}} \tag{6-9}$$

Interval 3 [t_2~t_3]: At the beginning of this interval, the gate pulse of switch S_2 is applied. Also, the switches S_4 and S_5 are turned off in this interval. Similar to Interval 1, the energy of UC charges the inductors L_1 and L_2. The current flow paths during this interval is similar to interval 1, shown in Figure 6.2 (a).

Interval 4 [t_3~t_4]: At t_3, the gate pulse of switches S_3 and S_6 are applied. Also, the switch S_1 is turned OFF. As illustrated in Figure 6.2 (c), load and output capacitor C_{H2} are supplied by the energy stored of inductor L_1 and capacitor C_{C2}. Meanwhile, the capacitor C_{C1} is charged by energy stored of L_1.

$$\frac{di_{L1}(t)}{dt} = \frac{U_{Low} - U_{m2}}{L} \tag{6-10}$$

$$\frac{di_{L2}(t)}{dt} = \frac{U_{Low}}{L} \tag{6-11}$$

$$\frac{dv_{Cm1}(t)}{dt} = \frac{i_{Cm2} + i_{L1}}{C_{m1}} \tag{6-12}$$

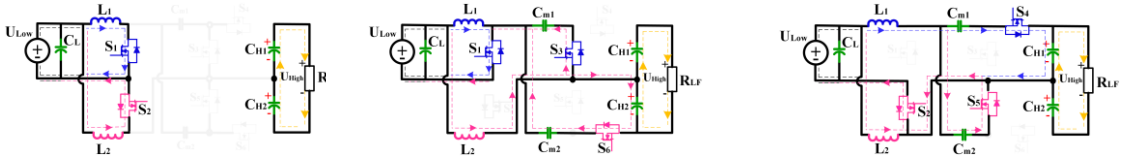
$$\frac{dv_{Cm2}(t)}{dt} = \frac{i_{Cm2} - i_{L2}}{C_{m2}} \tag{6-13}$$

$$\frac{dv_{CH1}(t)}{dt} = i_{Cm1} - \frac{U_{High}}{R_{LF}} \tag{6-14}$$

$$\frac{dv_{CH2}(t)}{dt} = -\frac{U_{High}}{R_{LF}} \tag{6-15}$$

6.2.1 Operation in Backward Mode

In this mode, the energy flows from HVS to LVS, and the converter operates similar to a buck converter, decreasing the voltage of dc-bus to the desired level of ESU connected to LVS. The equivalent circuits of the converter in different intervals with the current paths are illustrated in Figure 6.4.



(a) (b) (c)

Figure 6.2: Equivalent circuit of the proposed converter in forward mode. (a) Interval 1 and 3. (b) Intervals 2. (c) Interval 4.

The key waveform of the converter in backward mode is shown in Figure 6.3(b). The interleaved gating pulses with the same duty-cycle of d_B and a phase-shift of 180º are applied to switches S_3-S_6. The gate pulse of switch S_1 is complementary to that of switches S_3 and S_6. Likewise, the gate signal of switch S_2 is complementary to that of switches S_4 and S_5. Since the proposed converter can achieve a high step-down ratio when the duty-cycle d_B is less than 0.5 and the converter is working in CCM, the operation intervals and analysis are illustrated only for this case. The operation intervals are described as follows.

Interval 1 [t_0~t_1]: As shown in Figure 6.4 (a), switches S_1, S_4, and S_5 are turned on in this interval. The part of load is supplied by energy stored of inductor L_1. Meanwhile, the energy stored of capacitor C_{m2} is transferred to the inductor L_2 and load. It can be seen that

the capacitor C_{H1} is transferring the energy to the capacitor C_{m2}, the inductor L_2, and load as well. The equations (4)-(9) are valid for this interval.

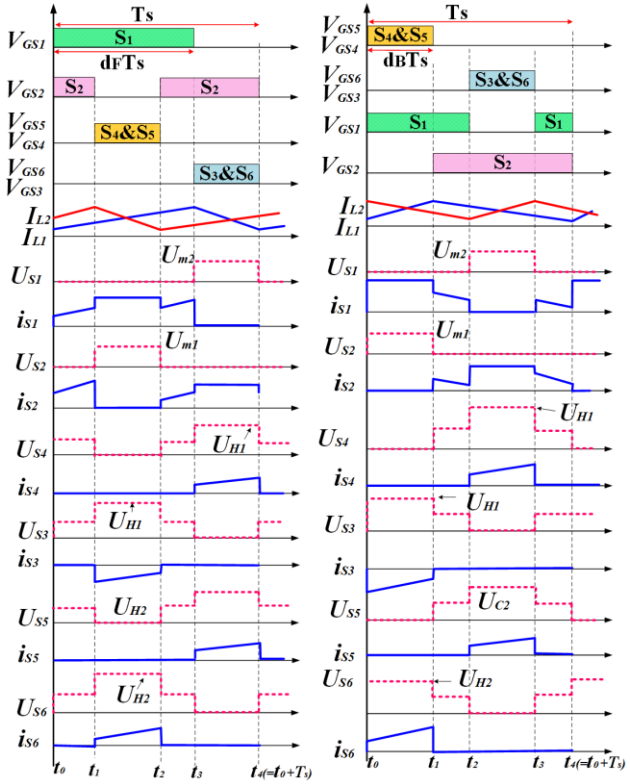


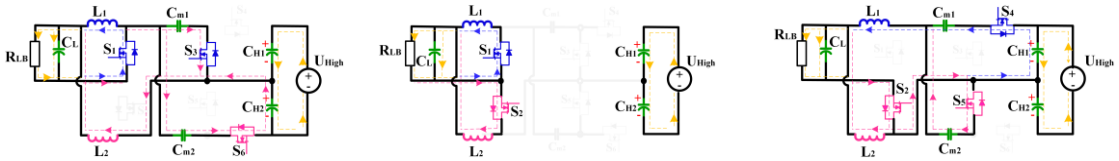
Figure 6.3: Key waveforms of the proposed converter. (a) forward mode. (b) backward mode.

Interval 2 [t_1~t_2]: At the beginning of this interval, the switches S_4 and S_5 get turned-off. Figure 6.4 (b) shows the equivalent circuit of the converter in this interval. It can be seen that the inductors L_1 and L_2 are supplying the load. The equations (1)-(3) are valid for this interval.

Interval 3 [t_2~t_3]: In this interval, the switches S_2, S_3, and S_6 are conducting the current. The corresponding equivalent circuit is depicted in Figure 6.4 (c). It can be seen that the inductor L_2 is releasing the energy to LVS to supply the load. At the same time, the energy

stored of capacitor C_{m1} is transferred to the inductor L_1 and load. Also, the capacitor C_{H2} is transferring the energy to the capacitor C_{m1}, the inductor L_1, and load as well. The equations (10)-(15) are valid for this interval.

Interval 4 [t_3~t_4]: At t_3, the switches S_1 and S_2 are turned on. The equivalent circuit of the converter is the same as that of Interval 2, illustrated in Figure 6.4 (b). It is clear that the inductors L_1 and L_2 are supplying the load.



(a) (b) (c)

Figure 6.4: Equivalent circuit of the proposed converter in backward mode. (a) Interval 1 and 3. (b) Intervals 2. (c) Interval 4.

6.3 Steady-State Analysis of the Proposed Converter

To simplify the analysis, it is assumed that the voltage ripple of capacitors are so negligible that they act like voltage source. Also, the switches are considered ideal.

6.3.1 Voltage Conversion Ratio

1) Forward Mode: The steady-state characteristics of the proposed converter can be obtained by applying the voltage-second balance principle across inductors L_1 and L_2. According to Figure 6.2(a)-(c), the equations describing forward mode operation can be written as follows:

$$\begin{cases} d_F.U_{Low} + (1-d_F).(U_{Low} - U_{m1} + U_{H1}) = 0 \\ d_F.U_{Low} + (1-d_F).(U_{Low} - U_{m2} + U_{H2}) = 0 \end{cases} \quad (6\text{-}16)$$

Where d_F is the duty cycle of switches S_1 and S_2 in the forward mode. According to Figure 6.3 (a)-(c) and applying Kirchhof Voltage Law to the circuit, the HVS voltage U_{High} can be defined by

$$\begin{cases} U_{High} = U_{H1} + U_{H2} \\ U_{H1} = U_{m1} + U_{m2} \\ U_{H2} = U_{m1} + U_{m2} \end{cases} \quad (6\text{-}17)$$

So, the voltage across the capacitors can be obtained by simplifying (16) and (17), given as follows:

$$\begin{cases} U_{m1} = U_{m2} = \dfrac{U_{Low}}{1 - d_F} \\ U_{H1} = U_{H2} = 2U_{m1} = \dfrac{2U_{Low}}{1 - d_F} \\ U_{High} = 2U_{H1} = \dfrac{4U_{Low}}{1 - d_F} \end{cases} \quad (6\text{-}18)$$

The voltage conversion ratio of the proposed converter in forward mode can be defined as

$$M_F = \frac{U_{High}}{U_{Low}} = \frac{4}{1 - d_F} \quad (6\text{-}19)$$

2) Backward Mode: According to Figure 6.4 (a)-(c) and the voltage-second balance principle across inductors L_1 and L_2, the stead-state characteristics of the proposed converter in backward mode can be obtained as follows:

$$\begin{cases} d_B.(U_{Low} - U_{m2}) + (1 - d_B).U_{Low} = 0 \\ d_B.(U_{Low} - U_{m1}) + (1 - d_B).U_{Low} = 0 \end{cases} \quad (6\text{-}20)$$

Where d_B is the duty cycle of switches S_3 – S_6 in the forward mode. According to Figure 6.4 (a)-(c) and applying Kirchhof Voltage Law to the circuit, the voltage across capacitors can be defined by

$$\begin{cases} U_{m1} = U_{m2} = \dfrac{U_{Low}}{d_B} \\ U_{H1} = U_{H2} = 2U_{m2} = \dfrac{2U_{Low}}{d_B} \\ U_{Low} = \dfrac{d_B U_{H1}}{2} = \dfrac{d_B U_{High}}{4} \end{cases} \tag{6-21}$$

The voltage conversion ratio of the proposed converter in forward mode can be defined as

$$M_B = \frac{U_{Low}}{U_{High}} = \frac{d_B}{4} \tag{6-22}$$

6.3.2 Voltage Stress on Switches

The voltage stress across switches S_1-S_6 in forward mode can be calculated by

$$\begin{cases} U_{S1} = U_{S2} = U_{m1} = \dfrac{U_{Low}}{1 - d_F} \\ U_{S3} = U_{S4} = U_{S5} = U_{S6} = U_{H1} = \dfrac{2U_{Low}}{1 - d_F} \end{cases} \tag{6-23}$$

The voltage stress across switches S_1-S_6 in backward mode can be calculated by

$$\begin{cases} U_{S1} = U_{S2} = U_{m2} = \dfrac{U_{Low}}{d_B} \\ U_{S3} = U_{S4} = U_{S5} = U_{S6} = U_{H1} = \dfrac{2U_{Low}}{d_B} \end{cases} \tag{6-24}$$

6.3.3 Current Ripple

In the forward mode, the current ripples as a function of the duty cycle can be defined by

$$\begin{cases} \Delta i_{L1} = \Delta i_{L2} = \dfrac{d_F \times (1 - d_F) \times U_{High}}{4L \times f_s} \\ \Delta i_{Low} = \dfrac{(1 - d_F) \times (2d_F - 1) \times U_{High}}{4L \times f_s} \end{cases} \tag{6-25}$$

Where Δi_{L1}, Δi_{L2}, and Δi_{Low} are the current ripples of i_{L1}, i_{L2}, and i_{Low}. For simplicity, it is assumed that L_1=L_2=L.

In the backward mode, the current ripples can be derived as follows:

$$\begin{cases} \Delta i_{L1} = \Delta i_{L2} = \dfrac{d_B \times (1 - d_B) \times U_{High}}{4L \times f_s} \\ \Delta i_{Low} = \dfrac{d_B \times (1 - 2d_B) \times U_{High}}{4L \times f_s} \end{cases} \tag{6-26}$$

6.3.4 Built-in Equal Current Sharing Capability

The built-in equal current sharing is a characteristic of the proposed converter to divide the input current equally between two phases without using extra circuitry. This is an important step toward realizing a truly interleaved converter, where the input current can be shared equally between two phases, which leads to the symmetrical performance in two phases. From operation analysis of the converter in forward and backward mode, the averaged-state equations can be obtained by using the state space averaging method, given by (27)-(32), where $C_{eq1} = C_{H1}C_{m1} + C_{H1}C_{m2} + C_{m1}C_{m2}$ and $C_{eq2} = C_{H2}C_{m1} + C_{H2}C_{m2} + C_{m1}C_{m2}$. Also, i_{L1}, i_{L2}, v_{m1}, v_{m2}, v_{H1}, and v_{H2} represent the average state variables, I_{L1}, I_{L2}, U_{m1}, U_{m2}, U_{H1}, and U_{H2} denotes the dc values of average state variables. For the sake of simplicity, it is assumed that $C_{H1} = C_{H2} = C_H$ and $C_{m1} = C_{m2} = C_m$. Since the derivative of the average state variables are equal to zero in the steady-state, the following relation can be derived from (27)-(32).

$$I_{L1} = I_{L2} = \left(\frac{2}{(1 - D_F)} + \frac{D_F C_m}{(1 - D_F) C_H}\right) \frac{U_{High}}{R_{LF}} \tag{6-33}$$

From (33), it is obvious that the proposed topology has the built-in equal current sharing characteristic.

6.4 Design Considerations

6.4.1 Inductors

The inductors play an important role in the proposed converter by reducing the current ripple. So, they should be selected accurately. Their values can be defined from (25), where the current ripple of the LVS should be 20 %.

6.4.2 Switches

The voltage rating of switches can be determined from (23)- (24), which provide an estimation for the voltage range. However, a safety margin of 150 % is considered to take into account the effect of the parasitic elements.

6.4.3 Capacitors

The value of the capacitance should be selected based on the assumption made in the previous sections that the capacitors work as a voltage source.

$$C_{H1} = C_{H2} = \frac{D_F \times U_{High}}{\Delta v_{CH1} \times R_{ESR} \times f_s} \tag{6-34}$$

$$C_L = \frac{(1 - D_F) \times U_{High}}{4 \times \Delta v_{CL} \times R_{ESR} \times f_s} \tag{6-35}$$

$$C_{m1} = C_{m2} = \frac{D_F \times U_{High}}{\Delta v_{Cm1} \times R_{ESR} \times f_s} \tag{6-36}$$

Where Δv_{CH1}, Δv_{CL}, and Δv_{Cm1} are the voltage ripples of capacitors C_{H1}, C_L, and C_{m1}.

6.4.4 Efficiency Analysis

The power losses in a bidirectional DC-DC converter includes five major components: 1) switching loss of switches, 2) conduction losses of switches, 3) conduction loss of inductors, 4) core loss of inductors, and 5) conduction losses of capacitors. The proposed converter losses can be approximated by the equations given in Table 6.1, where R_{L1}, R_{L2},

R_{Cc1}, R_{Cc2}, R_{CH1}, and R_{CH2} are the equivalent series resistance of the inductors L_1, L_2, and capacitors C_{C1}, C_{C2}, C_{H1}, and C_{H2}, respectively. Also, t_{fi}, t_{ri}, C_{OSSi} refer to the fall time, rise time, and the parasitic output capacitance of switch S_i, respectively. In equation describing core losses of inductors, a, b, and c are fitting parameters that can be found in the datasheet of the core. Also, l_{L1}, l_{L2}, A_{L1}, and A_{L2}, ΔB_1, and ΔB_2 are the magnetic flux path lengths, the cross-sectional areas, and ac magnetic flux density of the inductors L_1 and L_2, respectively. The loss breakdown at full load for forward and backward modes are shown in Figure 6. 8. As illustrated in Figure 6.12, the total losses of the converter in forward mode are 58.3 W, in which the major losses come from power switches and inductors. The conduction loss of switches accounts for 64% of the total losses.

The total loss can be calculated by

$$P_{loss} = P_{L\_cond} + P_{L\_core} + P_{C\_cond} + P_{S\_cond} + P_{S\_sw} \tag{6-37}$$

Table 6.1: Loss equations for key components.

Parameters		**Value**
Switches (S_1-S_6)	Conduction loss	$P_{S-cond} = R_{DS(on)}\left[\frac{I_{LVS}^2}{36}(77-41D) + \frac{D(1-D)U_{Low}^2}{3L^2f_s^2}\right]$
	Switching loss	$P_{Si-sw} = f_s(0.5V_{Si}I_{Si}(t_{ri}+t_{fi}) + 0.5V_{Si}^2C_{OSSi})$
Inductors (L_1 and L_2)	Core loss	$P_{L-core} = l_{L1}A_{L1}(a\Delta B_1^b f_s^c) + l_{L2}A_{L2}(a\Delta B_2^b f_s^c))$
	Winding loss	$P_{L-cond} = (R_{L1}+R_{L2})\left[\frac{I_{LVS}^2}{4} + \frac{DU_{Low}^2}{12L^2f_s^2}\right]$
Conduction loss of Capacitors		$P_{C-cond} = (R_{Cc1}+R_{Cc2})\frac{I_{LVS}^2}{8}(1-D) + (R_{CH1}+R_{CH2})\frac{I_{LVS}^2}{16}D^2(1-D)$

The conduction and core losses of the three inductors can be calculated using (6-38) and (6-39), where R_{L1}, R_{L2}, R_{L3}, l_{c1}, l_{c2}, l_{c3}, A_{c1}, A_{c2}, A_{c3}, ΔB_1, ΔB_2, and ΔB_3 are the equivalent series resistances of the three inductors, the magnetic flux path lengths of the three inductors' cores, the cross sectional areas of the three inductors' cores, and ac magnetic flux density of the three inductors.

$$P_{L\_cond} = \sum_{i=1}^{i=3} I_{Li}^2 \, R_{Li} \tag{6-38}$$

$$P_{L\_core} = \sum_{i=1}^{i=3} l_{ci} \, A_{ci} \, (a \, \Delta B_i^b \, f_s^c) \tag{6-39}$$

Equation (19), is the empirical Steinmetz equation, and *a*, *b*, and *c* are fitting values and can be extracted from the core manufacturer datasheet. The conduction loss of the capacitors can be extracted via (20), where $R_{C1} \rightarrow R_{C6}$ are the equivalent series resistances of the six capacitors.

$$P_C = \frac{\Delta i_{L1}^2}{12} R_{C1} + \frac{d_1}{1-d_1} I_H^2 (4R_{C2} + R_{C3} + 4R_{C4} + R_{C5} + R_{C6}) \tag{6-40}$$

The conduction losses of the switches can be derived using (21), where $R_{S1} \rightarrow R_{S4}$ are the on resistances of the switches. The switching loss of the switches can be calculated by (22) and (23), noting that the switching loss is only considered for the main switches for the considered mode of operation and discarded for the synchronous rectifiers (because they realize ZVS during turn-on and turn-off transitions). Equation (23) is used to calculate the switching loss for any of the four switches, where t_{ri}, t_{fi}, and C_{OSSi} are the rising and falling times, and the parasitic output capacitance of switch Q_i.

$$P_{Q\_cond} = I_H^2 \left(\left(\frac{3\sqrt{d_1}}{1-d_1} \right)^2 R_{S1} + \left(\frac{R_{S2}+R_{S3}+R_{S4}}{1-d_1} \right) \right) \quad (6\text{-}41)$$

$$P_{Q\_sw} = \begin{cases} P_{Q1\_sw} & \text{(Step-up mode)} \\ P_{Q2\_sw} + P_{Q3\_sw} + P_{Q3\_sw} & \text{(Step-down mode)} \end{cases} \quad (6\text{-}42)$$

$$P_{Qi\_sw} = f_s(0.5V_{Qi}i_{Qi}(t_{ri} + t_{fi}) + 0.5{V_{Qi}}^2 C_{OSSi}) \quad (6\text{-}43)$$

Finally, the efficiency η can be calculated using (24):

$$\eta = \begin{cases} \frac{V_L\, I_L}{V_L\, I_L + P_{Loss}} & \text{(Step-up mode)} \\ \frac{V_H\, I_H}{V_H\, I_H + P_{Loss}} & \text{(Step-down mode)} \end{cases} \quad (6\text{-}44)$$

6.5 Performance Comparison

To show the effectiveness of the proposed converter, a comparison is given in this section. Table 6.1 summarizes the passive and active components count, voltage conversion ratio, voltage stress of switches, and the maximum measured efficiency for SGIBC and recent BDCs. In Table 6.1, M_F and M_B denote the voltage gain in forward and backward mode, respectively. By employing the voltage quadrupler stage, SGIBC outperforms other circuits regarding the voltage conversion ratio, as depicted in Figure 6.5. The voltage gain of different converters in forward mode are shown in Figure 6.5 (a), implying that the voltage conversion ratio of the SGIBC notably is higher than that of other converters. Even though the voltage gain of the converter in [26] exceeds that of the SGIBC for duty cycle (d_F) more than 0.82, which corresponds to the voltage gain of 22 that is not in the operating range. Moreover, the converter in [26] utilizes more semiconductors and passive components than other BDC counterparts, suffering from reduced power density and efficiency. As shown in Figure 6.5(b), the proposed converter provides lowest voltage

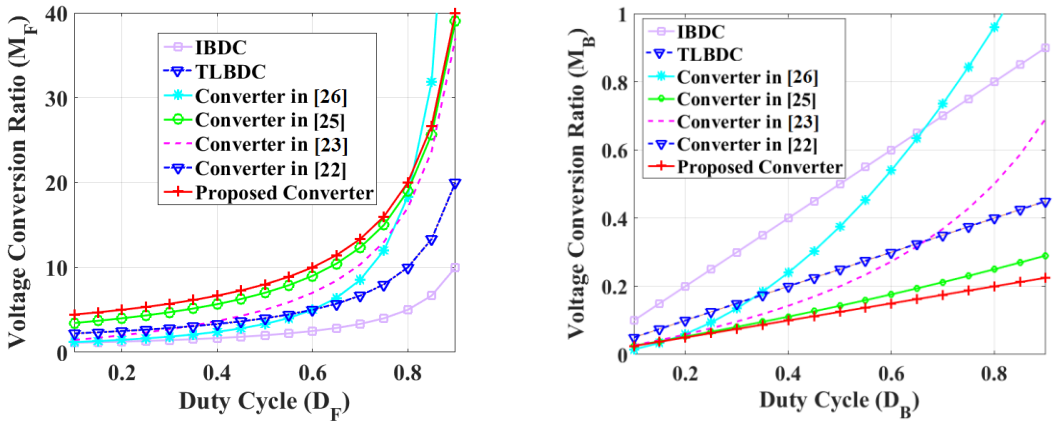
conversion ratio in backward mode. Regarding the voltage stress of switches, SGIBC offers much lower voltage stress compared to other BDCs, which enables the designer to utilize a switch with smaller on-resistance $R_{DS(ON)}$ resulting in higher efficiency.

Since the cost of switches dominates the other components costs in a BDC, a comparison of cost of the switches is carried out, which evaluates the converters by comparing the voltage and current stress imposed on the switches.

TABLE 6.2: COMPARISON BETWEEN THE PROPOSED CONVERTER AND OTHER BIDIRECTIONAL CONVERTERS

Topology		**Conventional IBDC**	**TLBDC [6]**	**Converter [23]**	**Converter [25]**	**Converter [26]**	**SGIBC**
Number of Components	**Switch**	4	4	4	5	7	6
	Inductor	2	2	3	2	5	2
	Capacitor	2	3	4	4	6	5
Voltage conversion ratio	***Forward Mode (M_F)***	$\frac{1}{1-d_F}$	$\frac{2}{1-d_F}$	$\frac{1+3d_F}{1-d_F}$	$\frac{3+d_F}{1-d_F}$	$\frac{3-d_F}{3(1-d_F)^2}$	$\frac{4}{1-d_F}$
	Backward mode (M_B)	d_B	$\frac{d_B}{2}$	$\frac{d_B}{4-3d_B}$	$\frac{d_B}{4-d_B}$	$\frac{3d_B^2}{2}$	$\frac{d_B}{4}$
Voltage stress (U_S/U_{Low})		M_F	$\frac{M_F}{2}$	$\frac{3+M_F}{2}$	$\frac{1+M_F}{4}$	$M_F(1-X_S)^*$	$\frac{M_F}{4}$
				$\frac{3+M_F}{4}$	$\frac{1+M_F}{2}$	$\frac{M_F-2}{2}(1-X_S)$	$\frac{M_F}{2}$
Rated output power		1 kW	0.5 kW	0.2 kW	0.2 kW	0.2 kW	2 kW
Maximum efficiencies	***Forward Mode***	94.3	-	96.8	η=97.1	97.0	97.3
	Backward Mode	94.5	-	-	-	94.5	97.4

$^*X_S = \frac{1+\sqrt{(6M_F-1)^2-36M_F(M_F-1)}}{6M_F}$



(a) (b)

Figure 6.5: Comparison of the voltage conversion ratio. (a) Forward mode. (b) Backward mode

This comparison is carried out between SGIBC and other BDCs with lowest voltage stress, namely converter introduced in [22] and TLBDC. According to [30], the total switch stress gives a rough estimate for the cost of the switches of a converter, which is defined by

$$S = \sum_{j=1}^{k} V_j I_j \tag{6-45}$$

Where k is the number of switches. In (10), V_j and I_j represent the maximum voltage and current stress of switch j, respectively. The total switch stress of SGIBC, TLBDC, and converter introduced in [22] are expressed by (20)-(22). To simplify these formulas, it is assumed that the converter is designed to work at a single operating point with switching frequency f_s, HVS power P_H, and HVS voltage U_{High}. Figure 6.6 (a) illustrates the total switches stress for different converters. It can be seen that the proposed converter operates more efficient than other converters in spite of using more semiconductor devices., except for the converter introduced in [26]. Therefore, the proposed converter offers a high-efficiency power conversion with lower cost.

$$S_{TLBDC} = \frac{P_H U_{High}}{2U_{Low}} + \frac{U_{High}U_{Low}}{4Lf_s}(1 - \frac{2U_{Low}}{U_{High}}) \quad (6\text{-}46)$$

$$S_{Converter\,[22]} = P_H\left(\frac{3U_{High}}{4U_{Low}} + \frac{U_{Low}}{U_{High}}\right) + \frac{3U_{High}U_{Low}}{4Lf_s}(1 - \frac{2U_{Low}}{V_H}) \quad (6\text{-}47)$$

$$S_{SGIBC} = P_H\left(\frac{U_{High}}{4V_L} + \frac{7U_{Low}}{8U_{High}}\right) + \frac{U_{High}U_{Low}}{8Lf_s}(1 - \frac{4U_{Low}}{U_{High}}) \quad (6\text{-}48)$$

Note to find the inductance L, the current ripple can be calculate using (6). According to (6), the maximum of current ripple happens when d_F = 0.75. Correspondingly, the maximum inductor current ripple can be defined as

$$\Delta i_{Low_{max}} = \frac{U_{High}}{32L \times f_s} \quad (6\text{-}49)$$

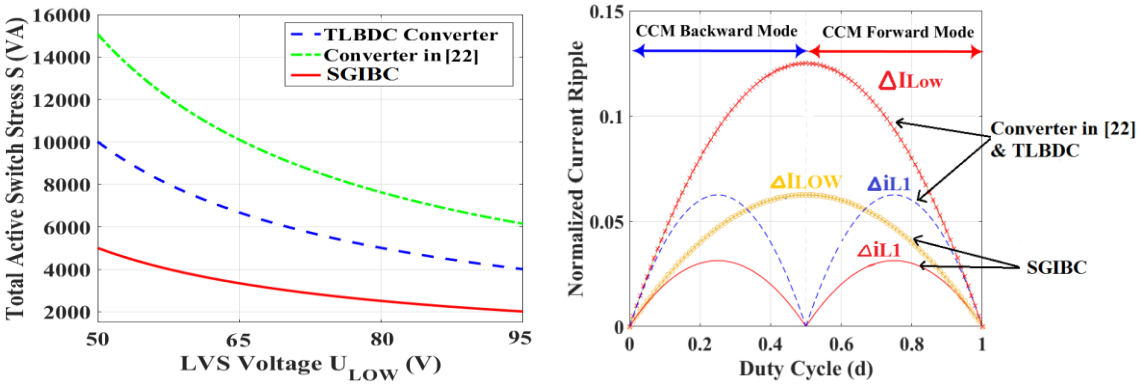
According to (6-14), the inductance L can be calculated by

$$L \geq \frac{U_{High}}{32\Delta i_{Low_{max}} \times f_s} \quad (6\text{-}50)$$

From (6-50) and Figure 6.6(b), it is clear that the inductance L of SGIBC is half of the inductance of the converter introduced in [22] and TLBDC for the same switching frequency and the current ripple $\Delta i_{Low_{max}}$. It implies that the volume and weight of the inductor of proposed converter is notably lower than that of other BDCs.

6.6 Analysis of The Dynamic Performance

In this section, the small-signal models of the proposed converter in forward mode is derived. It is noteworthy that the capacitor currents $i_{Cc1}(t)$ and $i_{Cc2}(t)$ are mutually coupled; so, their equivalent series resistance is taken into account to avoid the invalid state variables.



(a) (b)

Figure 6.6: Comparison of the total switch stress S and normalized current ripple. (a) Total switch stress S. (b) Current ripple.

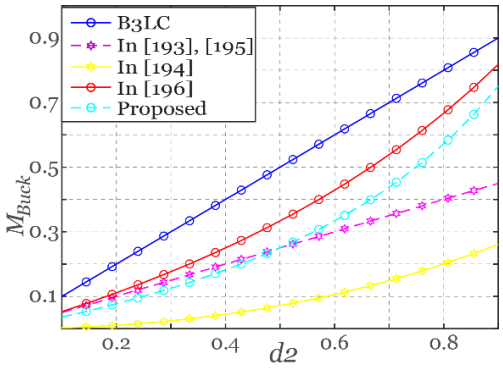


Figure 6.7: Voltage gain of the compared converters in the step-down mode versus the duty cycle.

Except for capacitors C_{C1} and C_{C2}, it is assumed that the inductors, capacitors, and the switches are ideal. With state space averaging method, the small signal AC equation can be obtained as (25).

The control-to-output transfer function in forward mode can be derived in complex frequency domain by employing the experimental parameters given in Table 6.3, which is given in (6-51). Similarly, the control-to-output transfer function in backward mode can be derived in complex frequency domain as (6-52).

$$\hat{G}_{u_H d_F} = \frac{\hat{u}_{High}(s)}{\hat{d}_F(s)} = \frac{a_1 S^5 + a_2 S^4 + a_3 S^3 + a_4 S^2 + a_5 S + a_6}{S^6 + b_1 S^5 + b_2 S^4 + b_3 S^3 + b_4 S^2 + b_5 S + b_6} \quad (6\text{-}51)$$

Where $a_1 = -2.5 \times 10^4$, $a_2 = -1.7 \times 10^{10}$, $a_3 = -1.1 \times 10^{15}$, $a_4 = -4.1 \times 10^{17}$, $a_5 = -2.5 \times 10^{25}$, $a_6 = 6.7 \times 10^{29}$, $b_1 = 7.2 \times 10^6$, $b_2 = 1.6 \times 10^{11}$, $b_3 = 3.5 \times 10^{15}$, $b_4 = 4.5 \times 10^{17}$, $b_5 = 1.5 \times 10^{22}$, and $b_6 = 8.5 \times 10^{25}$.

$$\hat{G}_{u_L d_B} = \frac{\hat{u}_{Low}(s)}{\hat{d}_B(s)} = \frac{a_1 S^5 + a_2 S^4 + a_3 S^3 + a_4 S^2 + a_5 S + a_6}{S^6 + b_1 S^5 + b_2 S^4 + b_3 S^3 + b_4 S^2 + b_5 S + b_6} \quad (6\text{-}52)$$

$$G_C(s) = K_p + \frac{K_i}{s} \quad (6\text{-}53)$$

Where $a_1 = 6.5 \times 10^8$, $a_2 = 7.6 \times 10^{12}$, $a_3 = 3.1 \times 10^{19}$, $a_4 = 2.6 \times 10^{23}$, $a_5 = 8.1 \times 10^{27}$, $a_6 = 1.7 \times 10^{31}$, $b_1 = 2.3 \times 10^5$, $b_2 = 2.6 \times 10^{11}$, $b_3 = 1.8 \times 10^{16}$, $b_4 = 9.5 \times 10^{19}$, $b_5 = 3.5 \times 10^{23}$, and $b_6 = 4.5 \times 10^{26}$.

In order to make the proposed converter achieve the better output voltage performance, As shown in Figure 6.8, an output voltage control strategy is adopted to improve the output voltage performance of the proposed converter, where $G_{u_H d_F}(s)$ denotes the transfer function of the converter, $G_m(s)$ denotes the transfer function of the pulse-width modulator, $H(s)$ refers to the feedback transfer function, and $G_c(s)$ is the voltage controller. In the adopted voltage control scheme, the transfer functions $G_m(s)$ and $H(s)$ are unitized. So, the transfer function $G_c(s)$ is designed in a way that the better closed-loop operation can be gained. The transfer function $G_c(s)$ is a proportional-integral (PI) controller, defined by (29), where values $K_{p\text{-}F} = 0.0002$, and $K_{i\text{-}F} = 0.0005$ in forward mode, and $K_{p\text{-}B} = 0.08$, and $K_{i\text{-}B} = 0.002$ in backward mode are adopted in the experiments.

6.7 Experimental Results

To validate the feasibility of the proposed converter, a laboratory prototype is implemented, shown in Figure 6.9. The specifications of the converter and component

parameters are presented in Table 6.2. In this section, two operation modes are investigated, namely: Forward mode and backward mode.

6.7.1 Forward Mode

The experimental results for forward mode are shown in Figure 6.8, where the LVS is connected to a voltage source U_{Low} = 50 V and HVS is connected to a resistive load R_{LF} = 320 Ω, and duty-cycle is 0.76. Figure 6.10 (a) illustrates the gate-source voltage of switch S_1 and S_2 and inductor currents i_{L1} and i_{L2}. It is obvious that the current ripples of inductors are consistent with the theoretical values obtained by (6). Interleaved operation paves the way for increasing the effective switching frequency, which leads to a smaller current ripple and inductors. Note that there is no voltage ringing in the gate-pulse due to correct PCB design by minimizing the parasitics inductance. The voltage of capacitors C_{m1}, C_{m2}, C_{H1}, and C_{H2} are demonstrated in Figure 6.10 (b). According to (3), the average capacitor voltages can be calculated as follows: U_{m1}=205V, U_{m2}=205V, U_{H1}=410V, and U_{H2}=410V, which are in a good agreement with the experimental results. Moreover, the voltage ripples of capacitors are small enough that confirms the correctness of the design of capacitors. The voltage stress across switches S_1, S_2, and S_3 are shown in Figure 6.10 (c). Also, the voltage stress across switches S_4, S_5, and S_6 are shown in Figure 6.10 (d). It can be seen that the voltage stresses of switches are much lower than the voltage of HVS U_{High}; therefore, switches with small on-resistance $R_{DS(ON)}$ can be employed leading to higher efficiency. The current waveforms of the switches S_1, S_2, and S_3 are shown in Figure 6.10 (e).

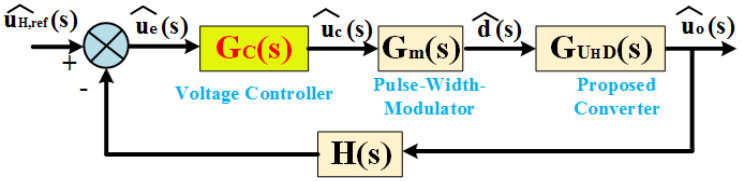


Figure 6.8: Voltage control strategy.

$$\begin{bmatrix} \frac{d\hat{\imath}_{L1}(t)}{dt} \\ \frac{d\hat{\imath}_{L2}(t)}{dt} \\ \frac{d\hat{u}_{Cc1}(t)}{dt} \\ \frac{d\hat{u}_{Cc2}(t)}{dt} \\ \frac{d\hat{u}_{CH1}(t)}{dt} \\ \frac{d\hat{u}_{CH2}(t)}{dt} \end{bmatrix}$$

$$= \begin{bmatrix} 0 & 0 & 0 & \frac{1-D}{L_1} & 0 & -\frac{1-D}{L_1} \\ 0 & 0 & \frac{1-D}{L_2} & 0 & -\frac{1-D}{L_2} & 0 \\ \frac{1-D}{kC_{c1}} & \frac{-(1-D)}{C_{c1}k} & \frac{-2(1-D)}{r_AkC_{c1}} & \frac{-2(1-D)}{r_AkC_{c1}} & \frac{1-D}{r_AkC_{c1}} & \frac{1-D}{r_AkC_{c1}} \\ \frac{-(1-D)}{C_{c2}k} & \frac{1-D}{C_{c2}k} & \frac{-2(1-D)}{r_AkC_{c2}} & \frac{-2(1-D)}{r_AkC_{c2}} & \frac{1-D}{r_AkC_{c2}} & \frac{1-D}{r_AkC_{c1}} \\ 0 & \frac{1-D}{C_{H1}k} & \frac{1-D}{C_{H1}kr_A} & \frac{1-D}{C_{H1}r_Ak} & \frac{-k-1}{RC_{H1}} & \frac{-1}{RC_{H1}} \\ \frac{1-D}{C_{H1}k} & 0 & \frac{1-D}{C_{H2}(r_Ak} & \frac{1-D}{C_{H2}r_Ak} & \frac{-1}{RC_{H2}} & \frac{-k-1}{RC_{H2}} \end{bmatrix} \begin{bmatrix} \hat{\imath}_{L1}(t) \\ \hat{\imath}_{L2}(t) \\ \hat{u}_{Cc1}(t) \\ \hat{u}_{Cc2}(t) \\ \hat{u}_{CH1}(t) \\ \hat{u}_{CH2}(t) \end{bmatrix} \quad (6\text{-}54)$$

$$+ \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{u}_{Low}(t) + \begin{bmatrix} 0 & 0 & 0 & \frac{1}{L_1} & 0 & \frac{-1}{L_1} \\ 0 & 0 & \frac{1}{L_2} & 0 & \frac{-1}{L_2} & 0 \\ \frac{-1}{kC_{c1}} & \frac{1}{C_{c1}k} & \frac{2}{r_AkC_{c1}} & \frac{2}{r_AkC_{c1}} & \frac{-1}{r_AkC_{c1}} & \frac{-1}{r_AkC_{c1}} \\ \frac{1}{C_{c2}k} & \frac{-1}{C_{c2}k} & \frac{2}{r_AkC_{c2}} & \frac{2}{r_AkC_{c2}} & \frac{-1}{r_AkC_{c2}} & \frac{-1}{r_AkC_{c1}} \\ 0 & \frac{-1}{C_{H1}k} & \frac{-1}{C_{H1}r_Ak} & \frac{-1}{C_{H1}r_Ak} & 0 & 0 \\ \frac{-1}{C_{H1}k} & 0 & \frac{-1}{C_{H2}r_Ak} & \frac{-1}{C_{H2}r_Ak} & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ U_{Cc1} \\ U_{Cc2} \\ U_{CH1} \\ U_{CH2} \end{bmatrix} \hat{d}(t)$$

$$\hat{u}_{High}(t) = [0 \quad 0 \quad 0 \quad 0 \quad 1 \quad 1][\widehat{\imath_{L1}}(t) \quad \widehat{\imath_{L2}}(t) \quad \widehat{u_{Cc1}}(t) \quad \widehat{u_{Cc2}}(t) \quad \widehat{u_{CH1}}(t) \quad \widehat{u_{CH2}}(t)]^T \quad (6\text{-}55)$$

TABLE 6.3: EXPERIMENT PARAMETERS AND COMPONENTS

Parameters and Components	Values
Rated power P_{High}	2 kW
Switching frequency f_s	100 kHz
High-side voltage U_{High}	800 V
Low-side voltage U_{Low}	50-100 V
Power Switches	GS66516B-E01-MR
Inductors L_1, L_2	100 µH
Capacitors C_{m1}, C_{m2}	10 µF
Capacitors C_{H1}, C_{H2}	220 µF
Microcontroller	TMS320f28335

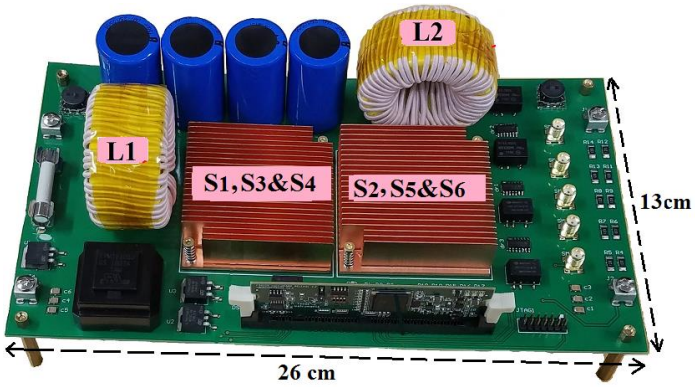


Figure 6.9: A photograph of laboratory prototype.

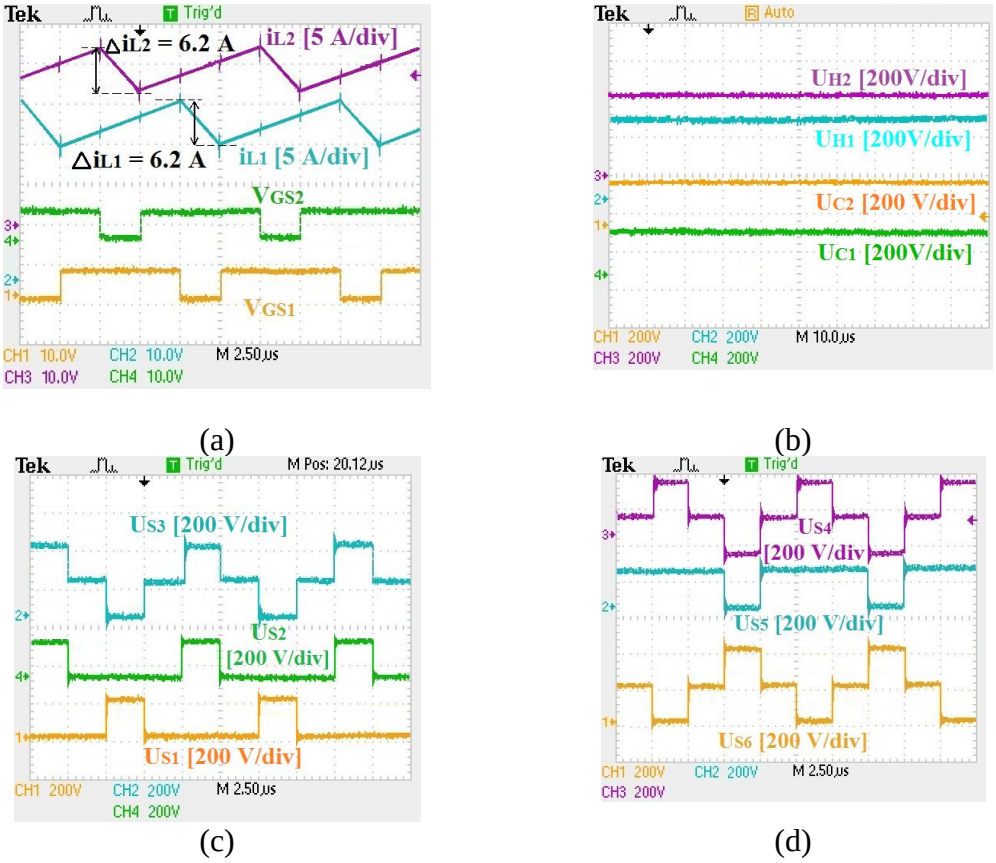


Figure 6.10: Experimental results for forward mode. (a) Gate-source voltage of switches S_1 and S_2 and Inductor currents. (b) Capacitor voltages. (c) Voltage stresses on switches S_1, S_2, and S_3. (d) Voltage stresses on switches S_4, S_5, and S_6.

6.7.2 Backward Mode

The experimental results for forward mode are shown in Figure 6.11, where the HVS is connected to a voltage source U_{High} = 800 V and LVS is connected to a resistive load R_{LB} = 3.2 Ω, and duty-cycle is 0.39. Figure 6.11 (a) illustrates the gate-source voltage of switch S_1 and inductor currents i_{L1} and i_{L2}. It is obvious that the current ripples of inductors are consistent with the theoretical values obtained by (11).

The voltage of capacitors C_{m1}, C_{m2}, C_{H1}, and C_{H2} are demonstrated in Figure 6.11 (b). According to (8), the average capacitor voltages can be calculated as follows: U_{m1} = 202V, U_{m2} = 202V, U_{H1} = 405V, and U_{H2} = 405V, which are in a good agreement with the

experimental results. Moreover, the voltage ripples of capacitors are small enough that confirms the correctness of design of capacitors. The voltage stresses across switches S_1, S_2, and S_3 are shown in Figure 6.11 (c). Also, the voltage stresses of switches S_4, S_5, and S_6 are shown in Figure 6.11 (d).

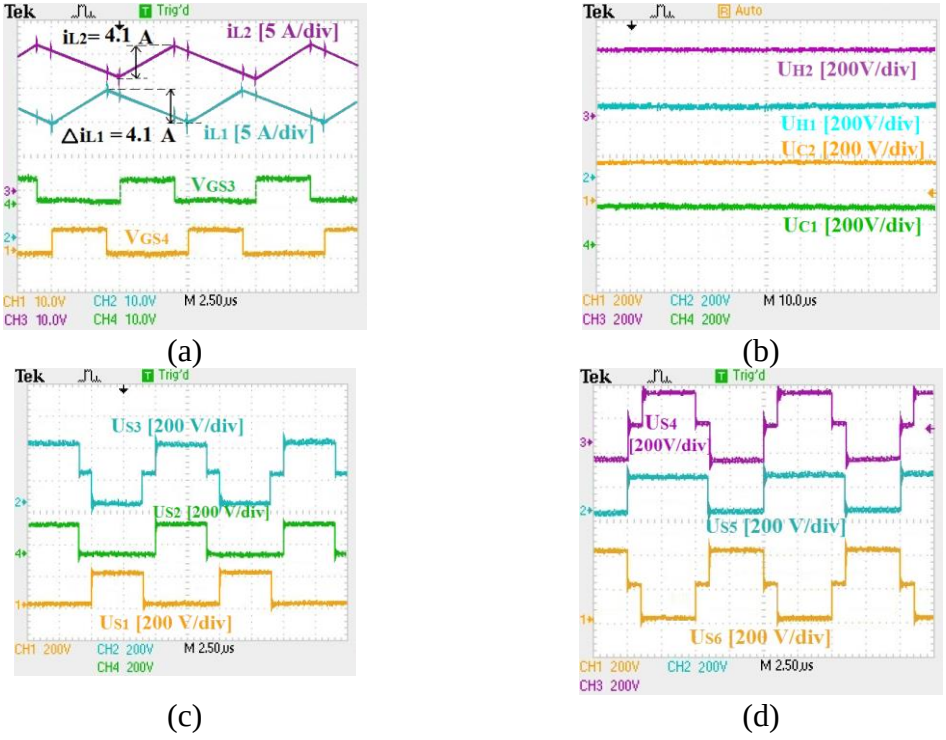


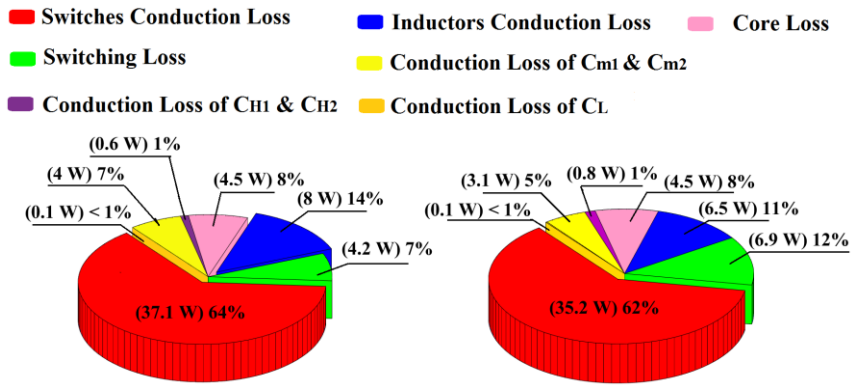
Figure 6.11: Experimental results for backward mode. (a) Gate-source voltage of switches S_1 and S_2 and Inductor currents. (b) Capacitor voltages. (c) Voltage stresses on switches S_1, S_2, and S_3. (d) Voltage stresses on switches S_4, S_5, and S_6.

It can be seen that the voltage stress of switches are much lower than the voltage of HVS U_{High}; therefore, switches with small on-resistance $R_{DS(ON)}$ can be employed that contributes to higher efficiency. The current waveforms of the switches S_1, S_2, and S_5 are shown in Figure 6.11 (e).

The loss breakdown at full load for forward and backward modes are shown in Figure 6.12. As illustrated in Figure 6. 10(a), the total losses of the converter in forward mode are 58.3

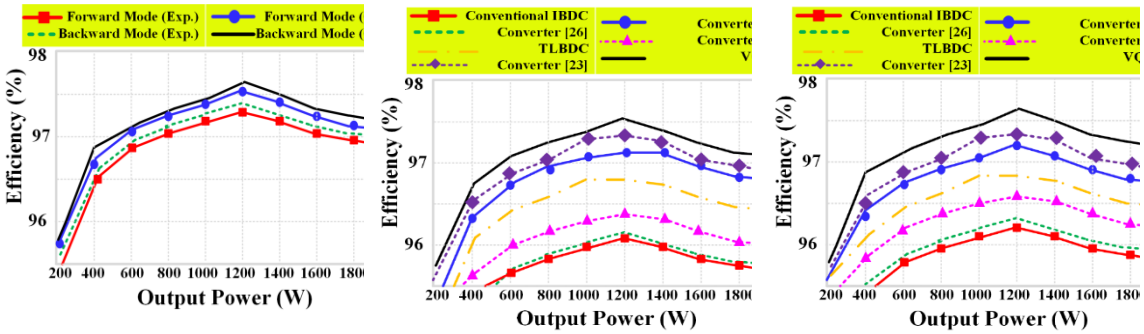
W, in which the major losses come from power switches and inductors. The conduction loss of switches accounts for 64% of the total losses. The loss breakdown in backward mode is shown in Figure 6. 10(b), where the total losses of the converter are 57.1 W. By analyzing the power loss distribution, it is evident that the conduction loss of switches is the significant loss that accounts for 62% of the total losses.

To measure the efficiency of the converter in different power levels, a power analyzer (Tektronix PA3000) was used. Figure 6.13 shows the measured and calculated efficiency curves for forward and backward modes. Form Figure 6.13 (a), it can be seen that the maximum efficiency happens at 600 W, where the maximum calculated efficiency for forward and backward modes are 97.5% and 97.6%, respectively. The maximum measured efficiency for forward and backward modes are 97.3% and 97.4%, respectively. At full load, the calculated efficiency values for forward and backward modes are 97.1% and 97.2%, respectively. Also, the values of measured efficiency at full load for forward and backward modes are 96.9% and 97%, respectively. There is a satisfactory agreement between the calculated and measured efficiency. A comparison of the efficiency of the proposed converter in forward and backward mode are given in Figure 6.13 (b) and (c), respectively. It is clear that the proposed converter offers the highest efficiency due to the low voltage stress of switches, low conduction losses of switches, and soft-switching performance.



(a) (b)

Figure 6.12: Calculated power loss distributions for the experiment. (a) forward mode. (b) backward mode.



(a) (b) (c)

Figure 6.13: efficiency curves. (a) Experimental and calculated results. (b) comparison of efficiency in forward mode. (c) comparison of efficiency in backward mode.

6.8 Conclusion

In this chapter, a steep-gain interleaved bidirectional DC-DC converter with intrinsic voltage-quadrupler and reduced total switch stress has been proposed. Charging the capacitors in parallel and then delivering the energy through different paths during the discharging process is the operating principle of SGIBC in forward mode to achieve high voltage conversion ratio. On the other hand, in backward mode, the switched capacitors are charged in series and discharged in parallel, which provides a high step-down gain. Due to the capacitive voltage divider, the voltage stress across the switches becomes smaller,

which facilitates employing lower voltage rating switches. Consequently, a significant reduction in switching and conduction losses is realized. Moreover, the proposed converter possesses the built-in equal current sharing feature without adopting extra circuitry. A 2-kW laboratory prototype using gallium-nitride switches is implemented to validate the proposed concept. It can be seen that the experimental results show agreement with the theoretical analysis. Therefore, the proposed topology is appropriate for applications demanding bidirectional power flow with a wide voltage range, such as interfacing the UC with the dc bus in EV systems.

Chapter 7 Experimental Verification of a GaN-Based Double-Input Soft-Switched DC/DC Converter for Hybrid Electric Vehicle Applications with Hybrid Energy Storage System

7.1 Introduction

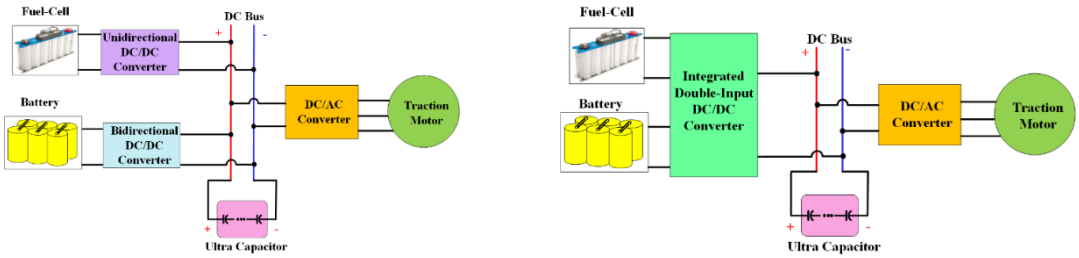
In the drivetrain of a fuel cell-powered electric vehicle (FCEV), double-input converter plays a critical role by transferring the power from battery and fuel cell (FC) to an ultra-capacitor (UC) during acceleration and from UC to the battery during braking. As battery and FC have unregulated low voltage, the converter should provide a high voltage gain as well as an efficient power conversion. In this chapter, a double-input three-level converter composed of Buck-Boost-Half-Bridge (BBHB) modules is proposed for automotive applications. The proposed converter can supply the load in the absence of FC or battery. The converter takes advantage of active clamp configuration in terms of reducing the voltage stress across switches and providing soft-switching performance. Consequently, the converter's overall performance in terms of switching losses and cost can be considerably improved. The switching scheme doubles the effective switching frequency, which, in turn, reduces the size of the boost inductors to enhance power density. The operational characteristics of the converter and comparison with state-of-the-art converters are given in this chapter. Finally, a 4 kW, 100 kHz prototype using GaN switches is implemented to validate the proposed concept.

7.2 Proposed Double-Input Three-Level DC-DC Converter

Figure 7.1(a) illustrates the general configuration of powertrain for a fuel cell-powered EV with hybrid energy storage, named parallel active hybrid. Including two DC/DC

converters, a DC/AC inverter and an electrical motor, this configuration is mainly reported in the literature. Conventional two-level bidirectional converter has been typically suggested as an effective circuit due to its simple design and ease of control. The main drawback of this topology is the high voltage stress of the switches that bring about higher switching losses and cost. Moreover, two bulky boost inductors are required that increases the volume and the weight of the converter, especially for high power applications.

In the drivetrain of a fuel cell-powered EV shown in Figure 7.1(b), the power is transferred to the DC bus from a battery via a bidirectional dc-dc converter during propulsion. During regenerative braking, the power flows from DC bus to the battery, which allows the battery to be charged. In this system, an FC stack is utilized to enhance the vehicle operating range.



(a) (b)

Figure 7.1: Block diagram of a fuel-cell-powered EV with hybrid energy storage. (a) using separate converters. (b) Proposed integrated double-input converter.

The proposed converter is shown in Figure 7.2, which consists of four switches S_1-S_4, two boost inductors L_{B1} and L_{B2}, and two DC bus capacitors C_{DC1} and C_{DC2}. Basically, the proposed double-input three-level converter is developed by merging two BBHB converters which are connected in such a way that the voltage gain is enhanced, and the voltage stress of the switches is considerably decreased.

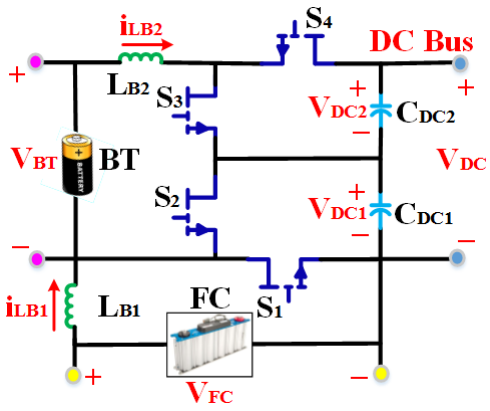


Figure 7.2: Proposed three-level double-input DC/DC converter.

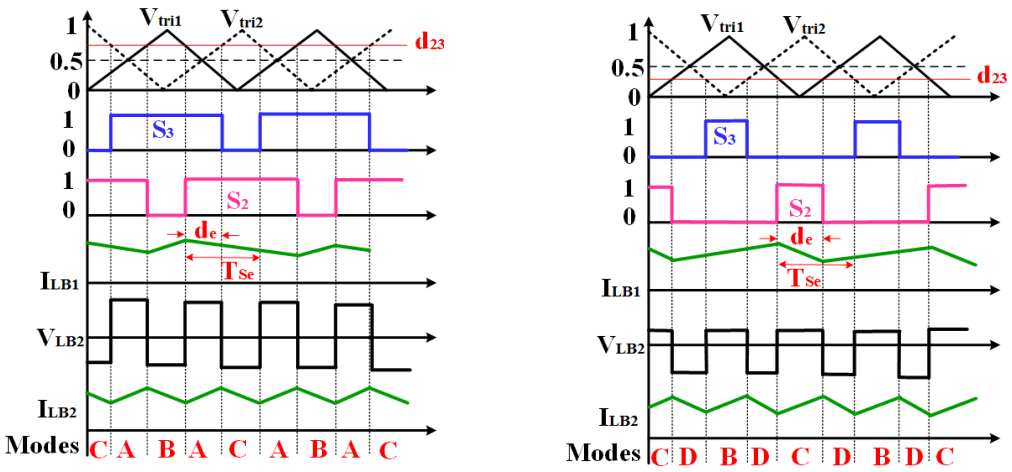
The states of the switches S_2 and S_1 are defined by a switching function $f_1(t)$ and its complementary function, respectively, which is given by (1). Similarly, the switching function $f_2(t)$ and its complementary functions determine the states of the switches S_3 and S_4, respectively. In (1), T_S is the switching period, and k is an integer.

$$f_1(t) = \begin{cases} 1, & kT_S < t \le T_S(k + 0.5d_{23}) and\ (k + 1 - 0.5d_{23})T_S < t \le T_S(k + 1) \\ 0, & (k + 0.5d_{23})T_S < t \le T_S(k + 1 - 0.5d_{23}) \end{cases}$$

$$f_2(t) \tag{7-1}$$

$$= \begin{cases} 1, & kT_S < t - \frac{T_S}{2} \le T_S(k + 0.5d_{23}) and\ (k + 1 - 0.5d_{23})T_S < t - \frac{T_S}{2} \le T_S(k + 1) \\ 0, & (k + 0.5d_{23})T_S < t - \frac{T_S}{2} \le T_S(k + 1 - 0.5d_{23}) \end{cases}$$

Figure 7.3 shows the switching scheme for the proposed converter, in which the carriers are triangular signals V_{tri1} and V_{tri2}, and d_{23} is the duty cycle of switches S_2 and S_3 (d_{s2}= d_{s3}= d_{23}). According to the value of the duty cycle d_{23} and the switching scheme, there are four different states: A, B, C, and D. The current and voltage key waveforms for d_{23}>0.5 and d_{23}<0.5 are shown in Figure 7.3 (a) and (b), respectively. The operation states for forward and backward modes are illustrated in Figure 7.4 and Figure 7.5, respectively.



(a) (b)

Figure 7.3: Different operation states for forward operation. (a) $d_{23} > 0.5$ (b) $d_{23} < 0.5$.

7.3 Operation Scenarios

According to the generated power of main source (FC), the battery state-of- charge, and the load, the operation of the converter can be divided into four scenarios which are described as follows:

7.3.1 Scenario I (FC supplies the load while the battery is not used)

This scenario happens when the main energy source (fuel cell) can solely supply the load. In this scenario, the converter works similar to a single-input single-output converter. The operation states for this scenario are illustrated in Figure 7. 4.

State A ($S_2 = S_3 = 1$): In this state, both switches S_2 and S_3 are turned-on, shown in Figure 7.4(a). So, the energy stored in the filter inductor L_{B1} is released into the capacitor C_{DC1}. The clamp capacitor C_{DC1} limits the voltage stress of switch S_1 to half of the DC-bus voltage V_{DC}.

State B (S_3=1 and S_2 =0): In this state, the inductor current i_{LB2} goes through the switches S_1 and S_3. As depicted in Figure 7.4 (b), the load is supplied by the energy stored in the capacitor C_{DC2}. Meanwhile, the inductor L_{B1} is being charged by FC.

State C (S_3=0 and S_2 =1): As shown in Figure 7.4 (c), during this mode, the energy stored in the inductor L_{B2} and capacitor C_{aux} is transferred to the clamp capacitor C_{DC2}. The clamp capacitor C_{DC2} limits the voltage stress of switch S_3 to the voltage V_{DC2}.

State D (S_3=0 and S_2 =0): If the duty cycle is less than 0.5, this operation mode happens. As shown in Figure 7.4 (d), the clamp circuit confines the voltage stress of switches S_2 and S_3 to the voltage of V_{DC1} and V_{DC2}, respectively. Meanwhile, the inductor L_{B1} is being charged by FC.

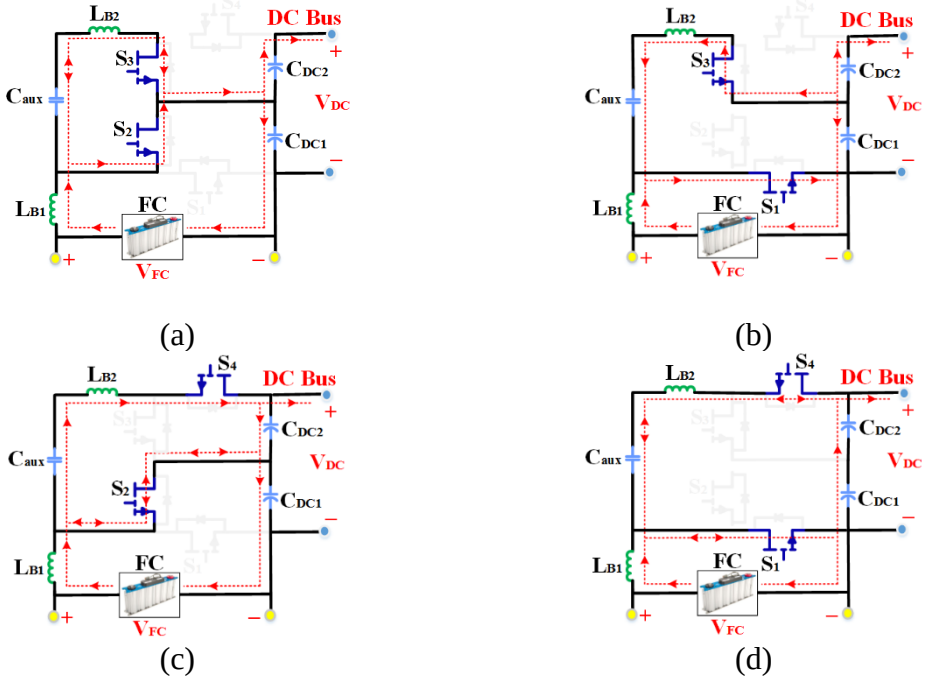


Figure 7.4: Operation states during scenario I. (a) State A. (b) State B. (c) State C. (d) State D.

7.3.2 Scenario II (FC and battery supply the load)

When the generated power of fuel cell is not enough to supply the load, the battery will discharge to feed the load. In this scenario, the converter operates like a double-input single-output converter. Based on the value of duty cycles d_1 and d_2, the converter can work in different states A, B, C, and D, which are illustrated in Figure 7.5. In special case, if the FC generated power is zero, which happens at the starting the car due to the long start-up time of the fuel cell or when the car is run out of fuel cell gas, the battery can supply the load. So, still the analyses given in this section are valid.

State A ($S_2 = S_3=1$): In this mode, both switches S_2 and S_3 are turned-on, shown in Figure 7.5 (a). So, the battery energy has been stored in the filter inductor L_{B2}. The clamp capacitor C_{DC1} limits the voltage stress of switch S_1 to half of the DC-bus voltage V_{DC}. Meanwhile, the capacitor C_{DC1} is charged by FC and the filter inductor L_{B2} during this state.

State B ($S_3=1$ and $S_2 =0$): In this state the load is supplied by the energy stored in the capacitor C_{DC2}. Also, the inductor current i_{LB2} goes through the switches S_1 and S_3. Meanwhile, the DC-bus capacitor C_{DC1} is being charged by the energy stored in the inductor L_{B2} and battery.

State C ($S_3=0$ and $S_2 =1$): As shown in Figure 7.5 (c), in this state, the energy stored in the inductor L_{B2} and battery is transferred to the clamp capacitor C_{DC2}. Also, the capacitor C_{DC1} is charged by the inductor L_{B1} and FC. The clamp capacitor C_{DC1} limits the voltage stress of switch S_3 to half of the DC-bus voltage V_{DC}.

State D ($S_3=0$ and $S_2 =0$): If the duty cycle is less than 0.5, this operation mode happens. As shown in Figure 7.5 (d), the clamp circuit confines the voltage stress of switches S_2 and S_3 to the voltage of V_{DC1} and V_{DC2}, respectively. In this state, the inductor is transferring

the battery energy to the DC-bus capacitors. Meanwhile, the inductor L_{B1} is being charged by FC.

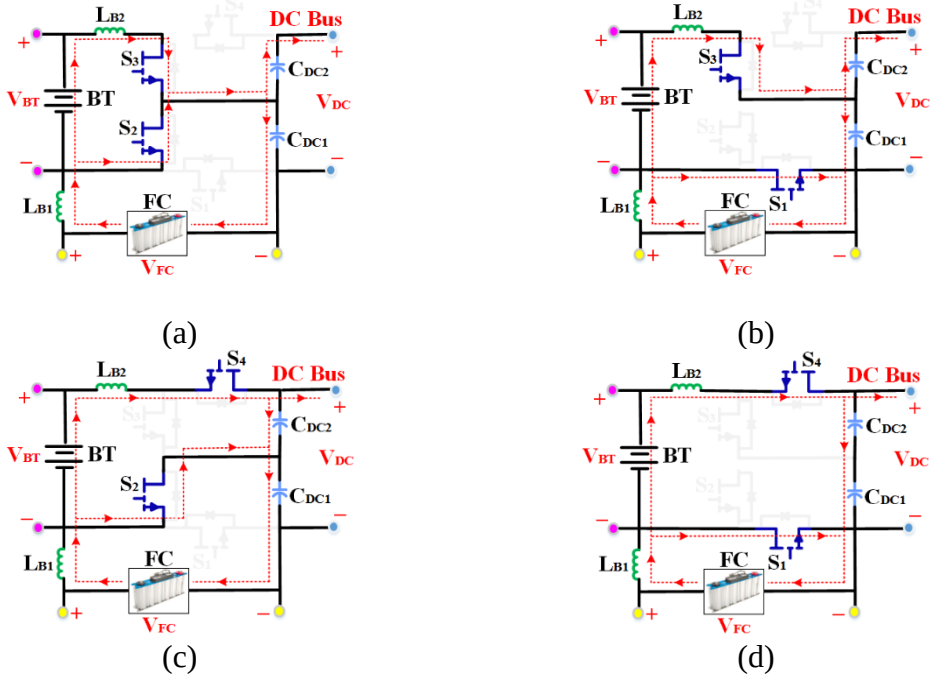


Figure 7.5: Operation states during scenario II. (a) State A. (b) State B. (c) State C. (d) State D.

To calculate the DC Bus-voltage-to-battery-voltage ratio, it is assumed that the converter works in continuous conduction mode (CCM). Moreover, the voltage across the DC bus capacitors C_{DC1} and C_{DC2} are equal ($V_{DC1} = V_{DC2} = 0.5V_{DC}$). According to Figure 7.4(a) and by applying the voltage-second balance principle to the inductor L_{B2} and analyzing its current ripple, the voltage conversion ratio can be determined as follows:

$$\frac{V_{DC}}{V_{BT}} = \frac{2}{1 - d_e} \tag{7-2}$$

Where d_e is defined by

$$d_e = (d_{s2} - 0.5) + (d_{s3} - 0.5) \tag{7-3}$$

Assuming that the duty cycle of switches S_2 and S_3 are equal, the effective duty-cycle d_e can be expressed as

$$d_e = 2d_{23} - 1 \tag{7-4}$$

Now, if $d_{23} < 0.5$, the voltage conversion ratio can be written as

$$\frac{V_{DC}}{V_{BT}} = \frac{2}{2 - d_e} \tag{7-5}$$

In this case, the effective duty-cycle d_e is defined by

$$d_e = (d_{s2} + d_{s3}) = 2d_{23} \tag{7-6}$$

7.3.3 Scenario III (FC supplies the load while battery is charged by the extra power)

In this scenario, FC can generate the power more than the power demanded by the load; so, the battery is charged by extra power. In this scenario, the converter works as a single-input double-output converter. There are four different states A, B, C, and D based on the value of duty cycles d_1 and d_2, which are shown in Figure 7.6. In this scenario, the operation states are the same as those in Scenario II, except that the inductor current i_{LB2} goes in the reverse direction.

7.3.1 Scenario IV (regenerative braking mode)

In this scenario, the motor is working in the regenerative braking mode; so, the direction of power flow changes and the battery can be charged by the energy coming from DC bus. In this scenario, the converter works similar to a single-input single-output buck converter. The operation states during this scenario are shown in Figure 7.7, in which the current is flowing from DC bus to the battery.

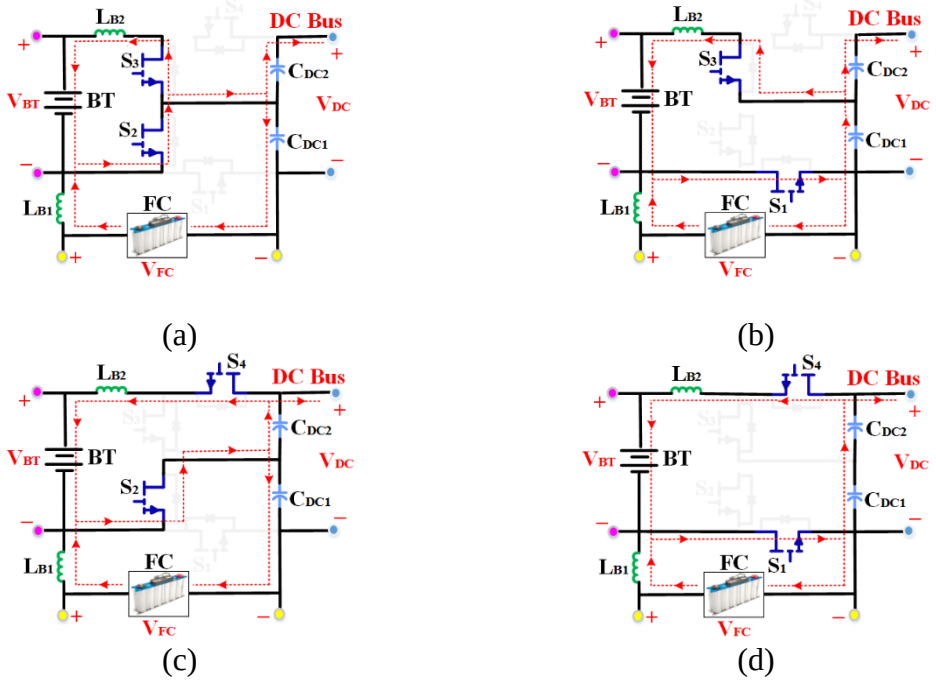


Figure 7.6: Operation states during scenario III. (a) State A. (b) State B. (c) State C. (d) State D.

State A ($S_2 = S_3=1$): This state starts when the turn-off signals are applied to the switches S_1 and S_4. In this state, the inductor current i_{LB2} will go through the switches S_2 and S_3. As depicted in Figure 7.7(a), the energy stored in inductor L_{B1} is transferred to battery, so the battery is being charged in this mode.

State B ($S_3=1$ and $S_2=0$): In this state, the switches S_2 and S_4 are turned off and the switches S_1 and S_3 conduct the current in negative direction, shown in Figure 7.7 (b). The clamp circuit confines the voltage stress of switches S_2 and S_4 to the voltage of V_{DC1} and V_{DC2}, respectively.

State C ($S_3=0$ and $S_2=1$): when the gate signal of switch S_1 is removed this state starts. As shown in Figure 7.7 (c), the battery is being charged by the total energy stored in inductor L_{B2} and capacitor C_{DC2}. The clamp capacitor C_{DC1} limits the voltage stress of switch S_1 to half of the DC-bus voltage V_{DC}.

State D (S_3 = S_2 =0): If the duty cycle is less than 0.5, this operation state happens. This state starts when both switches S_2 and S_3 are turned off. After this moment, the current goes through the switches S_1 and S_4. Meanwhile, the energy stored in both inductor L_{B2} and the DC-bus capacitors charges the battery, as illustrated in Figure 7.7 (d).

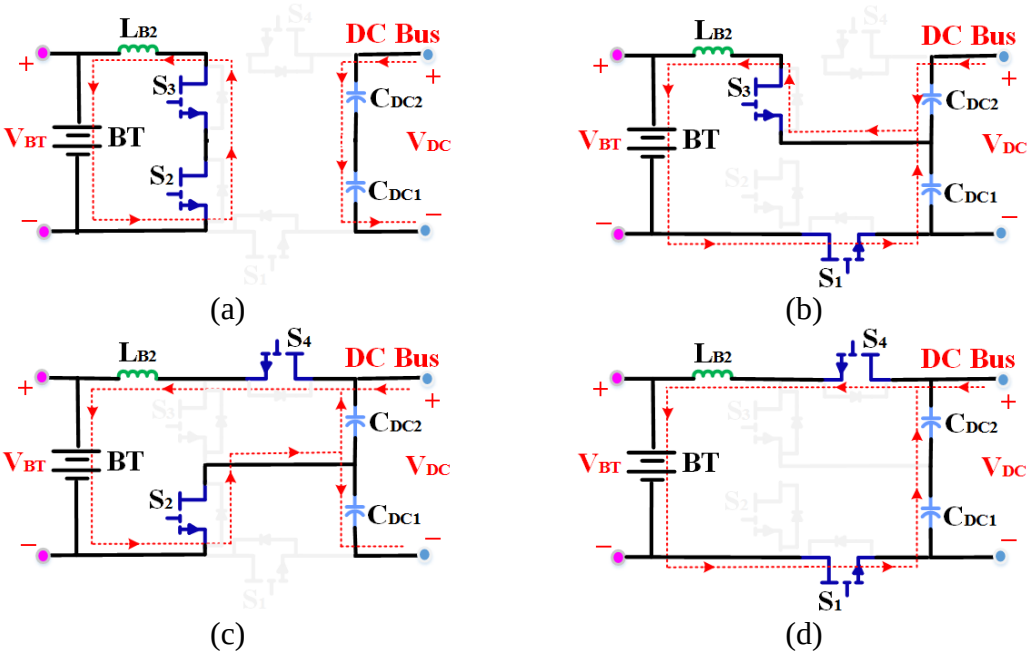


Figure 7.7: Operation states during scenario IV. (a) State A. (b) State B. (c) State C. (d) State D.

7.4 Design Considerations

7.4.1 Magnetic Inductors L_{B1} and L_{B2}

To design the inductance, three parameters should be considered: inductance, losses, and the maximum current to estimate the peak flux density.

1) Inductance L_{B1}: The inductance can be determined as a function of the battery current ripple Δi_{BT}, duty cycle, switching frequency fs, and DC bus voltage as follows:

$$\Delta i_{BT} = \begin{cases} \dfrac{V_{DC}(1-2d_{23})d_{23}}{2L_{B2}f_s}, & d_{23} \le 0.5 \\ \dfrac{V_{DC}(1-d_{23})(2d_{23}-1)}{2L_{B2}f_s}, & d_{23} > 0.5 \end{cases} \quad (7\text{-}7)$$

The maximum battery current ripple occurs at 0.25 and 0.75 duty cycles, which can be calculated by

$$\Delta i_{BT,max} = \frac{V_{DC}}{16L_{B2}f_s} \quad (7\text{-}8)$$

Accordingly, the inductance L_{B2} can be obtained by following equation:

$$L_{B2} \ge \frac{V_{DC,max}}{16\Delta i_{BT,max}f_s} \quad (7\text{-}9)$$

Where $V_{DC,max}$ is the maximum voltage of DC bus. From (8), it can be clearly understood that the required inductance for the same current ripple and the switching frequency for the proposed converter and 2LBIC is 25% of that for 2LBC.

2) Inductor Losses P_L: The inductor losses are composed of two components, copper loss P_{LCU} and core loss P_{LC}, which are defined by following equations:

$$P_{LCU} = R_{LB2}I_{LB2,rms}^2 \quad (7\text{-}10)$$

$$P_{L\_core} = \sum_{i=1}^{i=3} l_{ci}\, A_{ci}\, (a\, \Delta B_i^b\, f_s^c) \quad (7\text{-}11)$$

Where R_{LB2} is the inductor winding resistance, L_{ci} is the magnetic flux path length of the core, A_{ci} is the cross-sectional area *a*, *b*, and *c* are fitting values and can be extracted from the core manufacturer datasheet. It is noteworthy to mention that the core loss model (11) is the empirical Steinmetz equation.

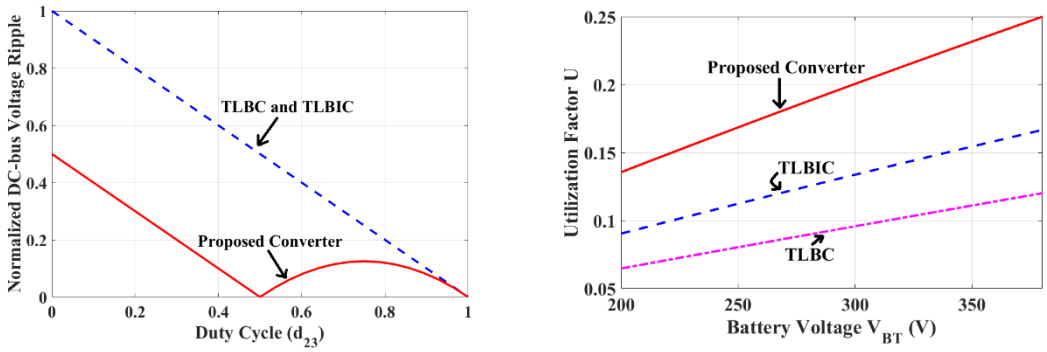
The RMS value of the inductor current $I_{LB2,rms}$ can be determined by

$$I_{LB2,rms} = \sqrt{I_{S3,rms}^2 + I_{S4,rms}^2} \tag{7-12}$$

Where $I_{s3,rms}$ and $I_{s4,rms}$ are the RMS current of switches S_3 and S_4, respectively, which can be obtained by

$$I_{S3,rms} = \sqrt{d_{23}(I_{L,min}^2 + I_{L,min}\Delta i_{BT} + \frac{\Delta i_{BT}^2}{3})} \tag{7-13}$$

$$I_{S4,rms} = \sqrt{(1-d_{23})(I_{L,max}^2 - I_{L,max}\Delta i_{BT} + \frac{\Delta i_{BT}^2}{3})} \tag{7-14}$$



(a) (b)

Figure 7.8: Normalized DC bus voltage ripple and utilization factor for different converters (P_{UC} = 50 kw, f_s = 100 kHz, and V_{UC} = 760 V). (a) Normalized DC bus voltage ripple; (b) utilization factor.

In equations (7-13)-(7-14), the inductor maximum and minimum current are defined as:

$$I_{L,max} = \frac{P_{DC}}{(1-d_{23})V_{DC}} + \frac{\Delta i_{BT}}{2} \tag{7-15}$$

$$I_{L,min} = \frac{P_{DC}}{(1-d_{23})V_{DC}} - \frac{\Delta i_{BT}}{2} \tag{7-16}$$

3) The maximum inductor current $I_{L,max}$: The maximum inductor current plays an important role in determining the size of the inductor since the peak flux density is directly related to the maximum inductor current. $I_{L,max}$ can be calculated using (7-15).

7.4.2 DC Bus Capacitors C_{DC1} and C_{DC2}

Three parameters are important in design of DC bus capacitors: the DC bus voltage ripple, RMS current, and maximum current. For this analysis, it is assumed that the DC bus capacitance are identical ($C_{DC1} = C_{DC2} = C_{DC}$). First, we calculate the DC bus voltage ripple as follows:

$$\Delta V_{DC} = \begin{cases} \dfrac{P_{DC}(1-2d_{23})}{2C_{DC}V_{DC}f_s}, & d_{23} \le 0.5 \\ \dfrac{P_{DC}(1-d_{23})(2d_{23}-1)}{2C_{DC}V_{DC}f_s d_{23}}, & d_{23} > 0.5 \end{cases} \tag{7-17}$$

Assuming the same output power P_{UC}, switching frequency f_s, and capacitance C_{DC}, a comparison of the DC-bus voltage ripple of the proposed converter with that of conventional 2LBC and 2LBIC is shown in Figure 7. 8. It can be seen that the voltage ripple of the proposed converter is much lower than that of 2LBC and 2LBIC. As a result, the DC bus capacitors C_{DC} of the proposed converter can be considerably smaller. The maximum DC bus voltage ripple occurs at duty cycle equal to $d_{23}=1/\sqrt{2}$, which can be calculated by

$$\Delta V_{UC,max} = \frac{P_{DC}(3-2\sqrt{2})}{2C_{DC}D_{DC}f_s} \tag{7-18}$$

From (18), the capacitance C_{DC} can be estimated by

$$C_{DC} \ge \max\left(\frac{P_{DC}(3-2\sqrt{2})}{2V_{DC}f_s\Delta V_{DC,max}}, \frac{P_{DC}(1-2d_{23})}{2V_{DC}f_s\Delta V_{DC,max}}\right) \tag{7-19}$$

For the sake of simplicity, it is assumed that the current ripple of inductor L_{B2} is negligible ($\Delta i_{LB2} \cong 0$). From Figure 7. 4 and Figure 7. 5, the instantaneous current of DC bus capacitors are defined by

$$\begin{aligned} i_{DC1}(t) &= i_{LB2}\big(d_{23} - f_1(t)\big) \\ i_{DC2}(t) &= i_{LB2}\big(d_{23} - f_2(t)\big) \end{aligned} \tag{7-20}$$

The maximum and the RMS current of DC bus capacitors can be estimated by

$$I_{C1,max} = I_{C2,max} = \frac{P_{DC}}{V_{UC}} \max\left(1, \frac{1}{1 - d_{23,max}}\right) \tag{7-21}$$

$$I_{C1,rms} = I_{C2,rms} = \frac{P_{DC}}{V_{DC}} \sqrt{\frac{d_{23}}{(1 - d_{23})}} \tag{7-22}$$

7.4.3 Power Switches

To choose the switches, the voltage and current stresses on the switches should be examined. In the proposed converter, the switches should withstand half the output voltage. The rms current of switches can be calculated from (13) and (14). Also, the resonance between the parasitic inductances of the circuit and the parasitic output capacitances of the switches creates a voltage spike, which necessitate choosing switches with higher voltage rating. So, a safety margin should be considered. Here, it is decided as 1.5, which dictates choosing 600-V switches. The maximum currents of the switches are equal to the maximum current of the inductors, which has been given in Table 7.1. Taking these criteria into account, the switches GS66516T from GaN Systems Inc. is selected.

7.4.4 Soft-Switching Performance

The equivalent circuit of the circuit including switch S_1 and S_2 is given in Figure7.9 (a), which operates similar to a conventional half-bridge stage. The asymmetrical pulse-width-

modulation is applied to the circuit, as shown in Figure7.9 (b). As shown in Figure7.9 (b), the current can flow in both directions for a synchronous rectifier. A special merit in half-bridge stage is that the GaN switches can conduct the freewheeling current without the need of an extra anti-parallel diode.

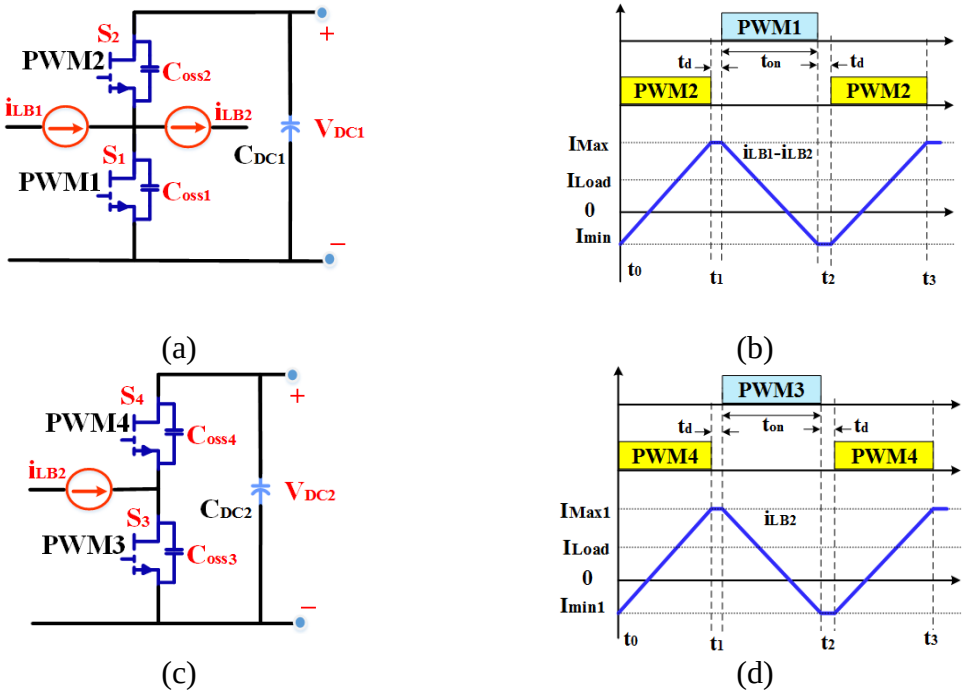


Figure 7.9: Asymmetrical PWM soft-switching operation. (a) Equivalent circuit of module including switches S_1 and S_2. (b) Gate-source pulse of switches S_1 and S_2 and inductor currents i_{LB1} and i_{LB2}. (c) Equivalent circuit of module including switches S_3 and S_4. (d) Gate-source pulse of switches S_3 and S_4 and inductor current i_{LB2}.

According to the waveforms shown in Figure 7. 9(b), at t_2, the switch S_1 is turned OFF, and its parasitic capacitance C_{oss1} is discharged. To achieve zero-voltage-switching (ZVS), parasitic capacitance C_{oss2} should discharge before applying the turn-on pulse to switch S_2. The body diode of switch S_2 starts to carry the current when the output capacitances C_{oss2} is fully discharged. Therefore, the total inductor current has to be negative. Moreover, the total energy stored in the inductors L_{B1} and L_{B2} at the switching instant must satisfy the following condition.

$$\frac{1}{2}L_{B2}(I_{LB2}-I_{LB1})^2 \geq \frac{1}{2}C_{oss1}(V_{S1})^2+\frac{1}{2}C_{oss2}(V_{S2})^2 \quad (7\text{-}23)$$

$$I_{LB2}-I_{LB1}=\frac{t_d.\Delta V_{LB2}}{L_{B2}}=\frac{t_d.(V_{DC2}-V_{BT})}{L_{B2}} \quad (7\text{-}24)$$

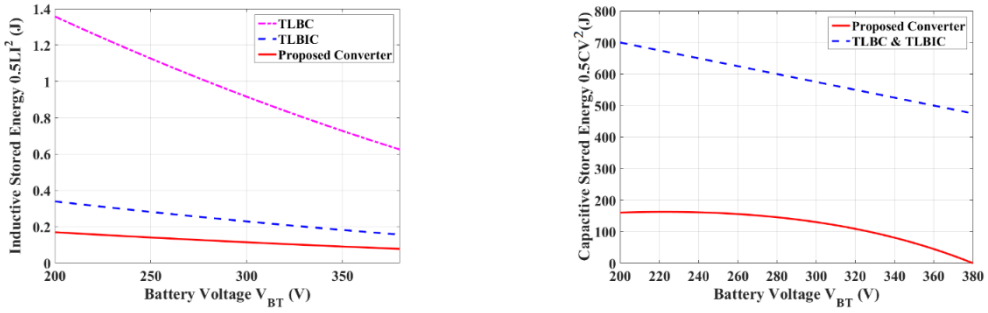
Where $E_{ind,total}$ is the total inductive energy of the inductor L_{B1} and L_{B2}, V_{s1} and V_{s2} are the voltage of switches S_1 and S_2, respectively, and C_{oss1} and C_{oss2} are the output capacitance of switches S_1 and S_2, respectively. Also, t_d represents the dead-time. the minimum dead time can be determined from (23) and (24), which is given as follows:

$$t_{d,min}=\sqrt{\frac{C_{oss,tot}.L_{B2}.V_{DC2}}{V_{DC2}-V_{BT}}} \quad (7\text{-}25)$$

Where $C_{oss,tot} = C_{oss1} + C_{oss2}$.. It can be concluded that if a specific dead-time is selected, the higher output capacitance is, the higher I_{min} is required. The similar analysis can be applied to the circuit including switches, S_3 and S_4. The equivalent circuit and gate-pulse waveforms are given in Figure 7. 9(c) and (d), respectively.

7.5 Comparison of The Proposed Converter With Other Converters

In this section, first a comparison of the proposed converter with 2LBC and 2LBIC is carried out, in terms of the magnetic component size, cost and the efficiency.



(a) (b)

Figure 7.10: Comparison of stored energy in the inductors and capacitors for different converters (P_{UC} = 50 kw, f_s = 100 kHz, and V_{DC} = 760 V). (a) Inductive stored energy; (b) Capacitive stored energy.

A thorough comparison with state-of-the-art three-port converters is made in this section.

7.5.1 Comparison with 2LBC and 2LBIC

1) Cost

The utilization factor of semiconductors can give a thorough insight into the expected cost of different topologies [25]. The utilization factor (U) is defined by

$$U = \frac{P_{DC}}{qV_{pk}I_{pk}} \tag{7-26}$$

Where q is the number of switches, V_{pk} and I_{pk} are the maximum voltage and current of the switches. Figure 7.8 (b) shows the utilization factor as a function of battery voltage for the proposed converter, 2LBC, and 2LBIC. It can be seen that the value of utilization factor of the switches for the proposed converter is higher than that for 2LBC and 2LBIC.

2) Component Size

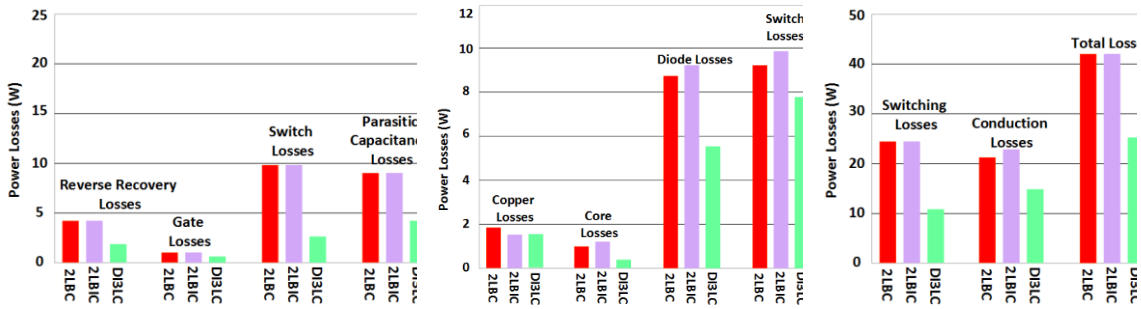
The stored energy in the passive components can give an insight into the size and weight of these elements. Therefore, the volume of converter is evaluated by measuring the stored energies in inductors and capacitors. To evaluate the size of passive components, it is assumed that the switching frequency is 100 kHz, the power is 50 kW, the DC bus voltage is 760 V, and the current ripple is 20 % of the discharging current, and the voltage ripple is 10 % of the DC-bus voltage. Figure 7.10 (a) and (b) illustrates the stored energy in the inductors and capacitors as a function of battery voltage, respectively. It is obvious that the stored energy of the inductors and capacitors of the proposed converter are much lower than those of 2LBC and 2LBIC converters.

3) Efficiency

In this section, a comparison in terms of the efficiency is carried out between the proposed double-input three-level converter (DI3LC) and the state-of-the-art bidirectional two-level dc-dc converters, namely 2LBC and 2LBIC.

The efficiency of a DC/DC converter can be estimated by analyzing the different losses, including the conduction and switching losses of switches, winding and core loss of the inductors [30]-[31].

The switching losses are composed of four components: 1) losses of switches caused by the overlap of voltage and current during turn-on and turn-off. 2) gate drive loss; 3) parasitic output capacitance loss; 4) reverse recovery losses of the body diode of switches. The core loss of the inductors can be calculated by multiplying core volume V_e with core loss density P_e, which are given by manufacturer. All cores have been chosen from Micrometal Inc. with relative permeability of μ_r =35. The loss breakdown at full load for DI3LC, 2LBC, and 2LBIC are shown in Figure 7.8. Figure 7.11(a) and Figure 7.11(b) demonstrate the switching and conduction losses, respectively.



(a) (b) (c)

Figure 7.11: Comparison of loss breakdown for the proposed converter versus 2LBC and 2LBIC. (a) Switching losses. (b) Conduction losses. (c) Total loss.

As illustrated in Figure 7. 11(a), due to the hard switching and high voltage stress across switches, the power losses of switches at switching instant is the main contributor to the switching losses. However, lower voltage stress and the soft-switching performance in the proposed converter reduce the switching losses. From Figure 7.11(b), it can be concluded that the conduction loss of switches and diodes are the significant conduction losses for all the converters. Nevertheless, the conduction losses of diodes in the proposed converter are lower in comparison with 2LBC and 2LBIC, since less count of diodes is employed in DI3LC. Figure 7.11(c) shows the total losses for the converters, in which the total loss of the proposed converter is 26.1 W, while that of 2LBC and 2LBIC are 41.9 and 42.4, respectively. By analyzing the power loss distribution, it is evident that the conduction losses are the significant losses that account for 59% of the total losses in the proposed converter. Nevertheless, in the 2LBC and 2LBIC, the switching losses account for 58% and 57% of the total losses, respectively.

Table 7.1: Comparison study between the proposed converter and other converters.

Specification	**Converter [26]**	**Converter [27]**	**Converter [29]**	**2LBC**	**2LBIC**	**Proposed Converter**
No. of switches	3	4	4	3	5	4
No. of diodes	3	4	5	1	1	0
No. of inductors	4	1	2	2	3	2
No. of capacitors	4	4	5	4	4	4
No. of input port	2	3	3	2	2	2
Boost voltage gain (V_{DC}/V_{FC})	$1/(1- d_1)$	$1/(1- D)$	$1/(1-d_2) + 1/(d_2-d_1)$	$1/(1- D)$	$1/(1- D)$	$2/(1-D)$
Max. voltage stress across switches	$0.5V_{DC}$	V_{DC}	V_{DC}	V_{DC}	V_{DC}	$0.5\ V_{DC}$
Input current	Discontinuous	Discontinuous	Discontinuous	Continuous	Continuous	Continuous
No. of ports with bidirectional power flow capability	1	3	1	1	1	3
Soft switching	Yes	No	No	No	No	Yes
Frequency (kHz)	100	0.4	30	20	74	100
Efficiency (%)	96	-	92.2	91.1	92.8	97.3
Power P_{out} (W)	1200	100	80	500	2000	4000

7.5.2 Comparison with the-state-of-the-art converters

A thorough comparison between DI3LC and other converters, including converters introduced in [26], [27], [28], [29], 2LBC, and 2LBIC is presented in Table 7.1. These converters are compared under operational characteristics, such as the number of components including the switch, diode, inductor, and capacitors, soft-switching possibility, voltage stress of switches, and power level, frequency, and efficiency.

Regarding the soft switching operation, only the converter [26] and the proposed converter can provide it, which results in lower switching losses. However, the proposed converter offers the soft-switching performance for all the switches, while only two switches in converter [26] can operate under soft-switching condition.

Since the switching losses considerably decreases with the voltage applied across the switch, the proposed converter offers lower switching loss. Especially, the switching loss of the parasitic capacitance can be remarkably lessened compared with 2LBC and 2LBIC as the voltage stress of switches is half the DC-bus voltage. In other words, due to employing low-voltage switches, the parasitic capacitance losses are expected to be even lower.

The current ripple impacts the FC system's lifetime; so, having a continuous input current with small ripple is very crucial for this application. Among these converters, 2LBC, 2LBIC, and the proposed converter offer the continuous current. Also, the total semiconductor count in the proposed converter is the minimum among the converters, and the bidirectional power flow for all three ports is possible only in the proposed converter and converter [27]. Considering all the aforementioned features, the proposed converter can be a preeminent candidate for applications that size is a critical parameter.

7.6 Dynamic Modeling and Control

In order to analyze dynamic performance of the proposed converter, modelling the converter is necessary. To obtain the average model, a one-period averaging technique is used, and to obtain a linear model, small-signal approximation is employed.

$$\langle x \rangle = \frac{1}{T_S}\int_{t}^{t+T_S} x(\tau)d\tau = X_0 + \hat{x} \tag{7-27}$$

Where T_S is the switching period, X_0 is a dc value in the steady-state, and $\hat{x}$ is a small perturbation around the dc value. Figure 7. 12(a) shows the converter equivalent circuit, in which the ideal capacitors C_{DC1} and C_{DC2} are used to represent the output filter capacitors. Resistance R_{LB1} and R_{LB2} represent the inductors resistance. The circuit performance can be defined by equations given in the following.

$$\frac{L_{B1}d\langle i_{LB1}\rangle}{dt} = \langle v_{FC}\rangle - d_1\langle v_{DC1}\rangle - R_{LB1}\langle i_{LB1}\rangle \tag{7-28}$$

$$\frac{L_{B2}d\langle i_{LB2}\rangle}{dt} = \langle v_{BT}\rangle - (1-d_1)\langle v_{DC1}\rangle - (1-d_2)\langle v_{DC2}\rangle - R_{LB2}\langle i_{LB2}\rangle \tag{7-29}$$

$$C_{DC1}\frac{d\langle v_{DC1}\rangle}{dt} = \langle i_{LB2}\rangle(1-d_1) - \frac{\langle v_{DC1}\rangle}{R_{DC1}} - \frac{\langle v_{DC2}\rangle}{R_{DC2}} \tag{7-30}$$

$$C_{DC1}\frac{d\langle v_{DC1}\rangle}{dt} = \langle i_{LB1}\rangle(-d_1) + (\langle i_{LB2}\rangle(d_1) - \frac{\langle v_{DC1}\rangle}{R_{DC1}} - \frac{\langle v_{DC2}\rangle}{R_{DC2}} \tag{7-31}$$

It is assumed that the perturbations do not oscillate significantly in switching period ($X_0 \gg \hat{x}$). Substituting (7-23) into (7-28)-(7-31) and neglecting the second-order terms, the small-signal model can be achieved. The small-signal models are described in matrix form as

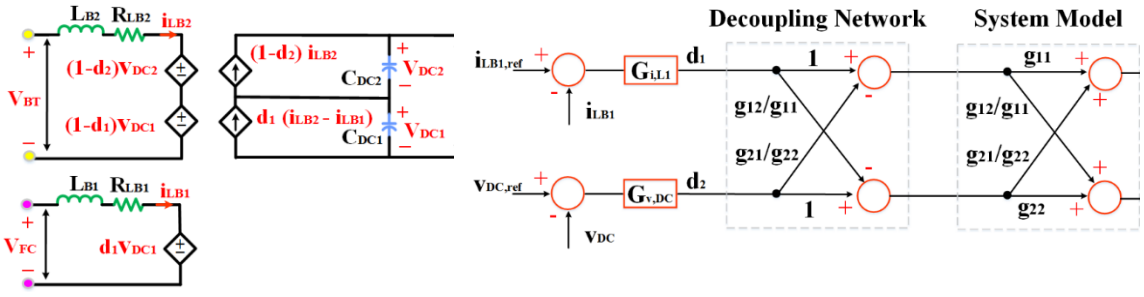
$$\begin{aligned} \dot{\hat{x}} &= A\hat{x} + B\hat{u} \\ \hat{y} &= C\hat{x} + D\hat{u} \end{aligned} \tag{32}$$

Where $\hat{x}, \hat{y}$, and $\hat{u}$ are state variable, system output vector, and control variables vector. Therefore, the matrix forms of the small-signal models can be expressed as follows:

$$\hat{x} = \begin{bmatrix} \widehat{\imath_{LB1}} \\ \widehat{\imath_{LB2}} \\ \widehat{v_{DC1}} \\ \widehat{v_{DC2}} \end{bmatrix}; \hat{u} = \begin{bmatrix} \widehat{d_1} \\ \widehat{d_2} \end{bmatrix};$$

$$A = \begin{bmatrix} \frac{-R_{LB1}}{L_{B1}} & 0 & \frac{-D_1}{L_{B1}} & 0 \\ \frac{-R_{LB2}}{L_{B2}} & 0 & \frac{D_1 - 1}{L_{B2}} & \frac{D_2 - 1}{L_{B2}} \\ 0 & \frac{1 - D_2}{C_{DC1}} & \frac{-1}{R_{DC}C_{DC1}} & \frac{-1}{R_{DC}C_{DC1}} \\ \frac{-D_1}{C_{DC2}} & \frac{D_1}{C_{DC2}} & \frac{-1}{R_{DC}C_{DC2}} & \frac{-1}{R_{DC}C_{DC2}} \end{bmatrix}; \quad (7\text{-}33)$$

$$B = \begin{bmatrix} \frac{-V_{DC}}{L_{B1}} & 0 \\ \frac{V_{DC1}}{L_{B2}} & \frac{V_{DC2}}{L_{B2}} \\ \frac{-I_{LB2}}{C_{DC1}} & 0 \\ \frac{I_{LB2} - I_{LB1}}{C_{DC2}} & 0 \end{bmatrix}; C = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$



(a) (b)

Figure 7.12: Large signal model and decoupling network accompanied with closed-loop compensators. (a) Large-signal average model of the proposed converter; (b) Decoupling network and closed-loop compensators.

In the system small-signal models, the state variables are controlled by two control variables. Accordingly, the transfer function matrix of the converter can be obtained as follows:

$$G = C(sI - A)^{-1}B + D \tag{7-34}$$

The rank of transfer function matrix represents the number of control variables. Therefore, $G_{2\times2}$-type transfer function matrix can be determined according to the number of control variables and based on (7-30).

$$\underbrace{\begin{bmatrix} y_1 \\ y_2 \end{bmatrix}}_{y} = \underbrace{\begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix}}_{G_{2\times2}} \underbrace{\begin{bmatrix} u_1 \\ u_2 \end{bmatrix}}_{u} \tag{7-35}$$

Where y and u are the system output and input vectors, and component g_{ij} represents the transfer function between y_i and u_j. In this study, the decoupling method is adopted to separately design closed-loop compensators for the coupled control loops [32]. The decoupling networks and closed -loop compensators are depicted in Figure 7.12(b). As a result of adopting the decoupling network G^* derivation, the state vector x can be expressed as $x = Gu^*$, where u^* is the modified input vector consist of duty ratios $u^* = G^*u$ [32], [33]. Therefore, $x = GG^*u$. In agreement with modern control theory, to allow each output of the matrixes be controlled by each singular input, the matrix GG^* should be a diagonal matrix [27]. According to $G^* = G^{-1}xu^{-1}$,

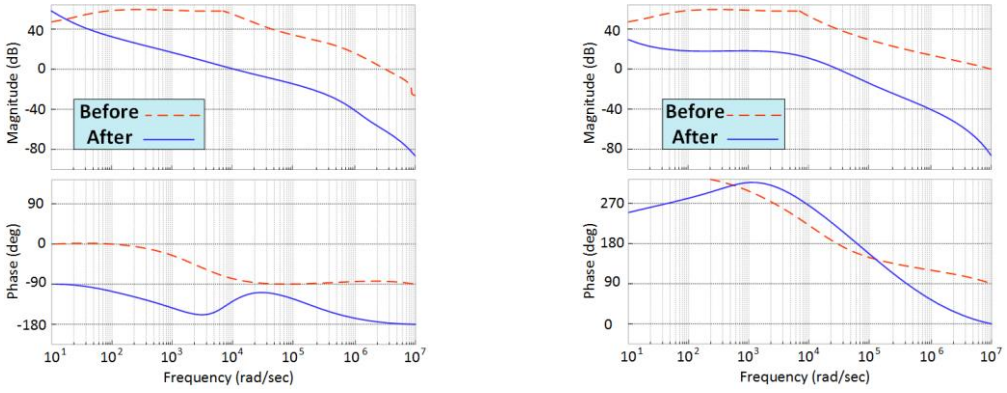
$$G^*_{2\times2} = \begin{bmatrix} 1 & -\dfrac{g_{12}}{g_{11}} \\ -\dfrac{g_{21}}{g_{22}} & 1 \end{bmatrix} \tag{7-36}$$

Using decoupling network $G^{*}_{2\times2}$ results in the cross-coupled two-loop control system $G_{2\times2}$ to be independent single-loop control for each input in two control variables systems as follows:

$$\frac{y_1}{u_1} = g_{11} - g_{12}\frac{g_{21}}{g_{22}} \tag{7-37}$$

$$\frac{y_2}{u_2} = g_{22} - g_{12}\frac{g_{21}}{g_{11}} \tag{7-38}$$

To design the system compensators, frequency-domain bode plot analysis is employed. To remove the steady-state errors of the system step responses, proportional-integral (PI) controller is used. Also, the compensator should have a lead unit in addition to the integral unit to reach the desired phase margin $60^{\circ} \leq P.M \leq 80^{\circ}$ and proper gain margin $G.M \geq 10$ db with suitable cutoff frequency. Therefore, the compensator with general form of (K_1 (1 + K_2S) / S (1 + K_3S)) is adopted. Regarding the mentioned considerations, the values of K_1, K_2, and K_3 for compensator G_{vDC} are 1853.7×10^{-5}, 3023.1×10^{-5}, 20.7×10^{-6}, and those for compensator G_{iLB1} are 42023.1×10^{-4}, 302.3×10^{-5}, 85.1×10^{-6}. The open-loop bode plot prior and pro to compensation are presented in Figure 7.13.

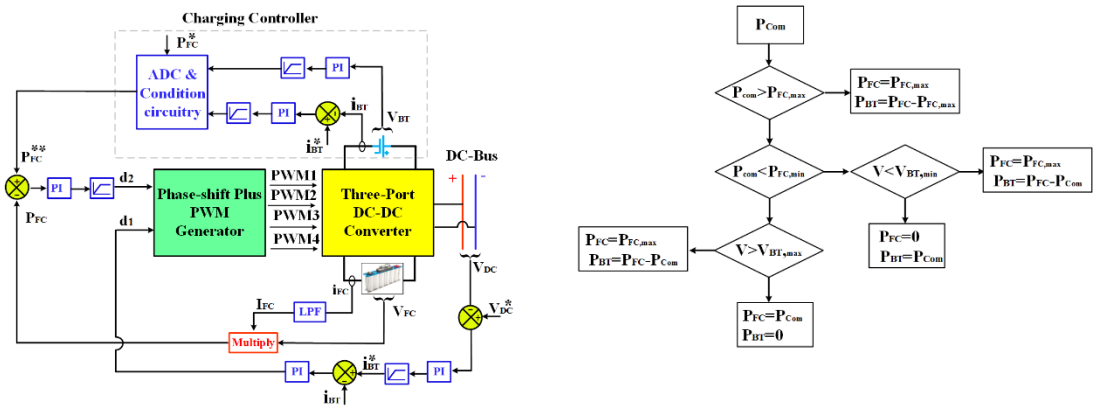


(a) (b)

Figure 7.13: Bode plots. (a) $i_{L1}(s) / d_1(s)$. (b) $v_{DC}(s) / d_2(s)$.

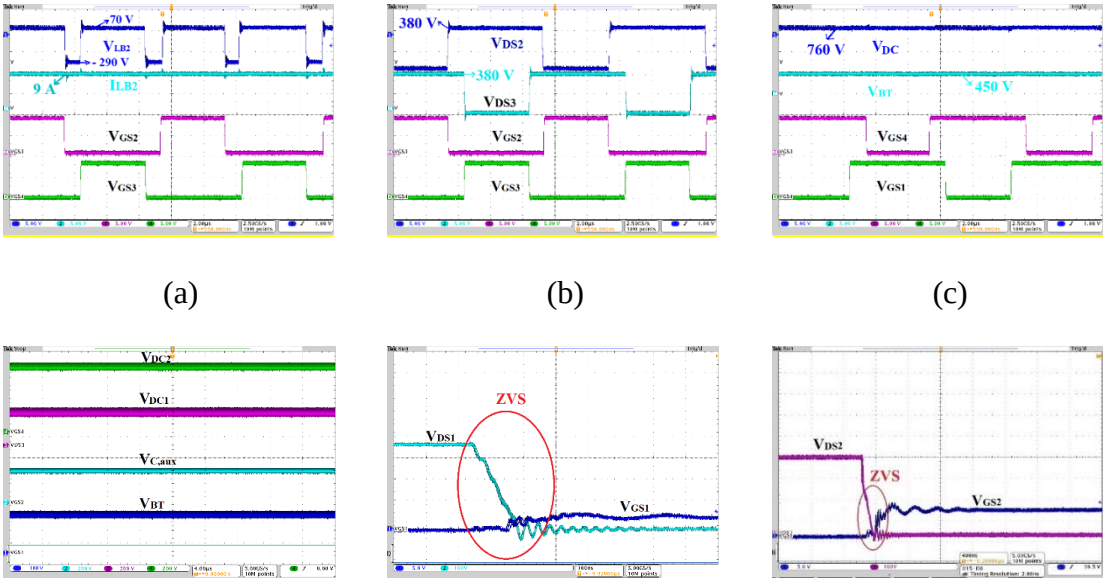
7.7 Power Management Algorithm

In the system shown in Figure 7.14(a), the proposed converter has been used this to interface a FC source at the first input port and a battery at the storage port. In this system, the FC source provides the steady-state power demanded by load connected to DC bus while the battery is utilized to feed a part of power demand during low generation of the FC source and high-load circumstances, as well as to improve the dynamic performance of the FC and startup transitions. As the transient load power is hard to predict, the power management system aims to regulate the DC bus voltage V_{DC}, set the fuel cell power level P_{FC} in its reference power, and take into account the state of charge (SOC) regulation of the battery. Accordingly, the proper operation scenario should be determined. As shown in Figure 7. 14(a), two degrees of freedom (i.e., d_1 and d_2) are available for controlling the power flow and regulating the DC bus voltage simultaneously, and two PI controllers are adopted to reach these goals. The control scheme is fully implemented using a digital signal processor (DSP). The SOC regulation for the battery enables the system to maintain the battery voltage in permissible minimum and maximum voltages $v_{BT.Min} < v_{BT} < v_{BT.Max}$. When the battery voltage goes below the minimum value $v_{BT.Min}$, the battery charging is necessary. Therefore, if the generated power of FC is more than the load, the battery charging is started while the load is supplied. The amount of power for charging the battery depends on the battery capacity. Moreover, the battery discharge can start when the battery voltage is higher than $v_{BT.Max}$, which depends on the FC power generation and load. The flowchart of the strategy is shown in Figure 7. 14(b).



(a) (b)

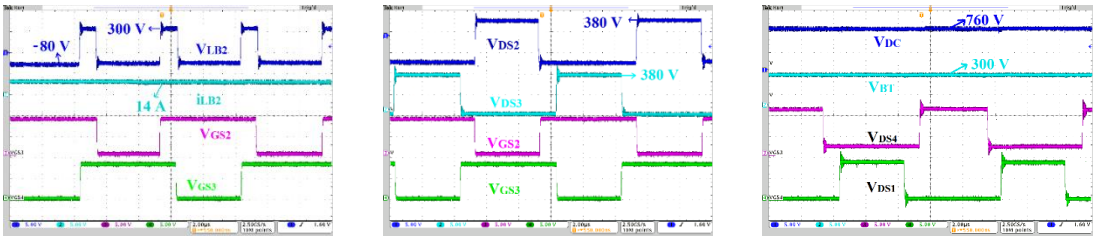
Figure 7.14: The power management scheme and its flowchart. (a) The power management scheme. (b) flowchart.



(a) (b) (c)

(d) (e) (f)

Figure 7.15: Experimental results for scenario I (V_{BT} = 450 V, P_{DC} = 4 kW and V_{DC} = 760 V). (a) Gate-source pulses of switches S_2 and S_3, current and the voltage across inductor L_{B2}. (b) Gate-source and drain-source voltage of switches S_2 and S_3. (c) Gate-source voltage of switches S_1 and S_4, DC-bus voltage, and battery voltage. (d) Voltage of capacitors C_{DC1}, C_{DC2} and C_{aux}. (e) Gate-source and drain-source voltage of switch S_1. (f) Gate-source and drain-source voltage of switch S_2.



(a) (b) (c)

Figure 7.16: Experimental results for scenario I (V_{BT} = 300 V, P_{UC} = 4 kW and V_{UC} = 760 V). (a) Gate-source pulse of switches S_2 and S_3, current and the voltage across inductor L_{B2}. (b) Gate-source and drain-source voltage of switches S_2 and S_3. (c) Drain-source voltage of switches S_1 and S_4, DC-bus voltage, and battery voltage.

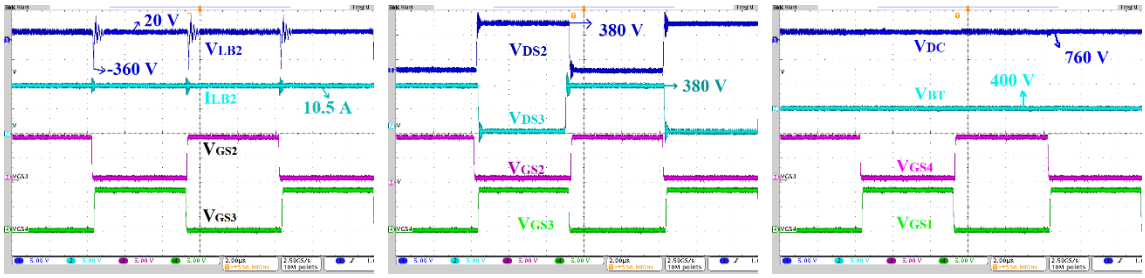
7.8 Experimental Results

To verify the theoretical analysis and operation modes of converter during different scenarios, a 4 kW prototype is implemented as the proof of concept, and the experimental results are given in Figure 7.15- Figure 7.18. Converter performance in scenario I is shown in Figure 7.15, where the battery voltage is 450 V and the converter is feeding full load. As shown in Figure 7.15 (a), the gate-source pulses of switches S_2 and S_3, current and the voltage across inductor L_{B2} are illustrated. It can be seen that the duty-cycle of switches

TABLE 7.2: MAIN EXPERIMENTAL PARAMETERS OF THE PROPOSED CONVERTER

PARAMETERS AND COMPONENTS	VALUE
BATTERY VOLTAGE (V_{BT})	250-500 V
OUTPUT VOLTAGE (V_{DC})	760 V
OUTPUT POWER (P_{DC})	4 KW
SWITCHING FREQUENCY	100 KHZ
INPUT INDUCTOR L_{B1}	300 µH
RESONANT INDUCTOR L_{B2}	100 µH
CAPACITORS C_C AND C_O	20 µF
POWER SWITCHES (S_1, S_2, S_3, S_4)	GS66516T (FROM GAN SYSTEMS)

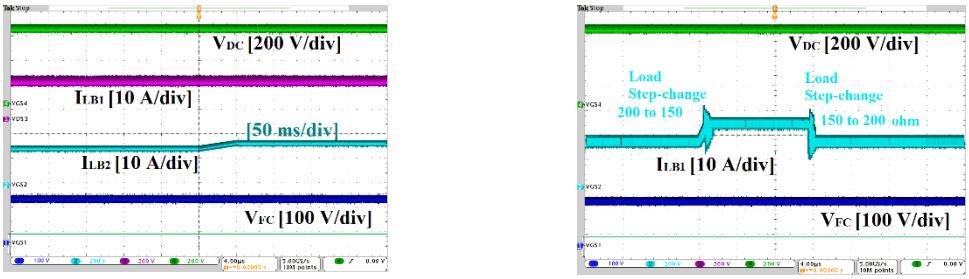
are about 0.6, which is in good agreement with the theoretical equation. The drain-source voltage of switches S_2 and S_3 are shown in Figure 7.15(b). It is clear that the voltage stress of switches are limited to half of output voltage V_{DC} due to the clamp circuit configuration, indicating the clamp-circuit suppress the voltage spikes; thus, employing the switches with small rated-voltage is possible leading to lower conduction loss. The gate-source voltage of switches S_1 and S_4, battery voltage, and DC-bus voltage V_{DC} during scenario I are given in Figure 7.15 (c), which clearly confirms the control algorithm is working correctly. The waveforms of the voltage of capacitors C_{aux}, C_{DC1}, and C_{DC2} are shown in Figure 7.15 (d). The experimental results for soft-switching performance of switches S_1 and S_2 are given in Figure 7.15 (e) an (f), respectively. It is clear that the voltage of switch becomes zero before its gate-pulse is applied, implying the overlap between the voltage and current stress of switch is negligible. The results of converter performance in scenario I, when battery voltage is 300 V, is shown in Figure 7.16. The gate-source pulses of switches S_2 and S_3, current and the voltage across inductor L_{B2} are demonstrated in Figure 7. 16 (a). The voltage stress of all switches S_1-S_4 are shown in Figure 7. 16 (b) and (c). To investigate the performance of proposed converter in scenario IV, a test is done when the output port is generating the power. Figure 7.17 shows the results of the converter performance in scenario IV. The inductor current i_{LB2} and gate-source voltage of switches during scenario IV are given in Figure 7.17 (a) while the duty-cycle is about 0.5, which proves the correctness of control algorithm. Figure 7.17 (b) and (c) illustrate the gate-source voltage of all switches and drain-source voltage of switches S_2 and S_3. It is clear that the clamp circuit is confining the voltage stress across the switches.



(a) (b) (c)

Figure 7.17: Experimental results for scenario IV (V_{BT} = 400 V, P_{UC} = 4 kW and V_{UC} = 760 V). (a) Gate-source pulse of switches S_2 and S_3, current and the voltage across inductor L_{B2}. (b) Gate-source and drain-source voltage of switches S_2 and S_3. (c) Gate-source voltage of switches S_1 and S_4, DC-bus voltage, and battery voltage.

The dynamic performance of the converter is demonstrated in Figure 7.18. Transition from scenario I to scenario II, the control scheme operates in a way that the circuit draws enough current from battery, as shown in Figure 7.18 (b). converter output is Figure 7. 18 (b) demonstrates the output voltage and the inductor current i_{LB1} while there is a step change of load between 150 Ω and 200 Ω. It is clear that the control technique keeps the output voltage constant with the load step-change. The efficiency of the converter operation under different power values for different scenarios is shown in Figure 7.19.



(a) (b)

Figure 7.18: The experimental results of dynamic performance. (a) Transitioning from scenario I to scenario II. (b) Output voltage and inductor current when load step-change between 150 Ω and 200 Ω.

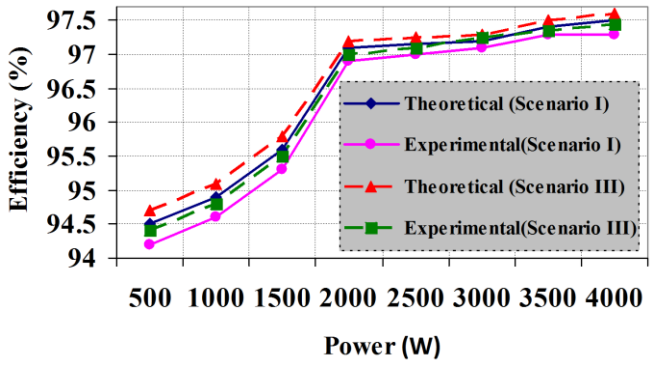


Figure 7.19: The theoretical and experimental efficiency for different power P_{DC}.

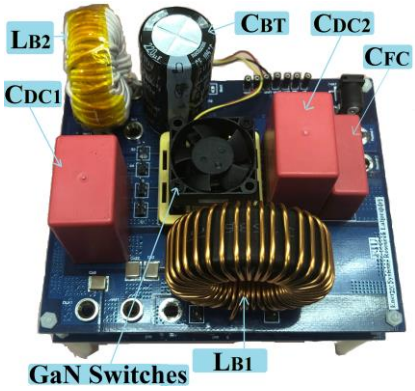


Figure 7.20: Laboratory prototype.

The maximum theoretical and experimental efficiency are obtained as 97.5 and 97.3 % at 4000 W, respectively. Figure 7. 20 shows the laboratory prototype of proposed double-input three-level dc/dc converter.

7.9 Conclusion

In this chapter, a double-input three-level dc/dc converter consisting of two buck-boost half-bridge modules is proposed. The proposed converter can supply the load in the absence of one of the sources. Moreover, it can charge the battery by the power generated from DC-bus when the vehicle is working in the braking mode. To increase both the power

density and efficiency, GaN switches are used. To decrease the voltage stress of switches, a cascaded configuration is employed which paves the way for adopting switches with small $R_{DS(ON)}$. To investigate the performance of converter during different condition, in terms of availability of power of sources, the converter is analyzed for three different operation scenarios. Finally, a 4 kW prototype is built to verify the correctness of theoretical analysis. The proposed converter offers several merits over the state-of-the-art 2LBC and 2LBIC converters in terms of voltage stress across switches, cost, and size of passive components, which make it a promising candidate for BPEV app

Chapter 8 PWM Plus Phase-Shift Modulated Three-Port Three-Level Soft-Switching Converter Using GaN Switches for Photovoltaic Applications

8.1 Introduction

Gallium nitride (GaN) high electron mobility transistors (HEMTs) are a promising technology for high-efficiency and high-power density applications. In this chapter, a stacked three-port three-level converter (STPTLC) using GaN switches is proposed for interfacing the renewable energy sources with load for applications that the presence of energy storage device is necessary. Derived from the asymmetrical bidirectional half-bridge converter, the proposed converter presents valuable advantages in terms of simple control scheme, extended soft-switching performance over a wide range of operating conditions, and reduced voltage stress across switches. The soft switching for all switches at turn-on instant is guaranteed thanks to active clamp configuration, resulting in high-efficiency performance. The pulse-width-modulation plus phase-shift control technique paves the way for decoupled regulation of the output voltage and power by presenting two control freedoms, which allows the input voltage to vary in a wide range. To diminish the current stress of switches and minimize the conduction loss, the root-mean-square (RMS) current of inductance and the boundary condition of the phase-shift controller in different operation cases are studied. Finally, the experimental results of a 1 kW, 100 kHz prototype of STPTLC using GaN switches are given to confirm the validity of the proposed concept.

8.2 Proposed STPTLC and Its Operation Analysis

8.2.1 Configuration of the Proposed Converter

A TPC is a well-established means of realizing a highly regulated dc-link bus in systems

with multiple sources. Since the input port is connected to a RES such as PV, TPC has to have the maximum power tracking capability. Due to the volatility of renewable energy sources, presence of an energy storage element is necessary to supply the mismatched power.

In this section, the proposed STPTLC is thoroughly studied. Stacking converters such as that depicted in Figure 8.1 aims at improving the efficiency and voltage gain without requiring any extra component. It is obvious that the power can transfer among three ports directly without using any transformer. The clamp circuit limits the voltage stress of switches; hence switches with smaller on-resistance $R_{DS(ON)}$ can be used, leading to lower conduction loss. Compared to other TPC, STPTLC offers the soft-switching performance for a wide range of power and input voltage and needs less number of switches and inductors to achieve high voltage gain.

Symbols are defined as follows: filter inductors L_{B1}, L_{B2}, power switches S_1, S_2, S_3, S_4, auxiliary capacitor C_{aux}, clamp capacitor C_C, and output capacitor C_O. V_{out} denotes the voltage of high-voltage port (HVP), which is equal to summation of voltage of clamp capacitor and output capacitor, $V_{Cc}+V_{Co}$. In Figure 8.1, the battery is emulated by a voltage source V_{BT}. Also, the solar panel is modeled as an ideal voltage source V_{PV} in series with a diode D_{PV}. The voltage across switches S_2 and S_3 are symbolized by V_{ab} and V_{db}, respectively. The gate pulse of switches S_2 and S_4 are complementary to that of switches S_1 and S_3, respectively. The inductor L_{B1} is adopted as a filter to reduce the battery current ripple, and the inductor L_{B2} is used to form a resonant circuit to realize ZVS performance and confine the peak current of HVP switches. The main switches S_1 and S_3 can transfer the power from PV to the battery and the load, respectively. While no extra voltage stress

is added across the switches, an auxiliary capacitor is added to the circuit to extend the range of soft-switching performance, which forms a resonant tank with the inductor L_{B2}. This auxiliary capacitor stores the magnetic energy of inductor L_{B2}, and released it to the output capacitor C_o.

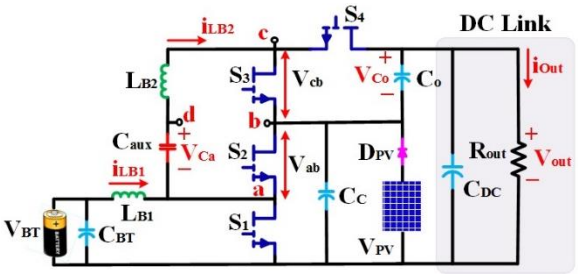


Figure 8.1: Proposed STPTLC for hybrid BT/PV applications.

8.2.2 Operation Mode Analysis

As depicted in Figure 8.2, based on the generated power of PV array and the power demanded by load, four operation scenarios can happen: 1) Scenario I, when the power of solar panel is not enough to supply the load (cloudy day or nighttime). 2) Scenario II, when the generated power of PV array P_{PV} is more than the power demand, i.e.,$P_{PV} > P_{out}$; so, the battery absorbs the extra power generated by PV so that the output voltage is regulated at a constant value. 3) Scenario III, when the battery can be charged from the utility grid through an inverter, which is possible only for grid-connected application. 4) Scenario IV, ABHB operation, when the load is disconnected, i.e.,$P_{out} = 0$, and the battery is charged by the generated power of PV array.

The operating principle and characteristics of proposed converter are demonstrated with the following assumptions: 1) the capacitors C_C, C_O, C_{aux} are large enough so that they can be taken as constant voltage sources; 2) All switches S_1-S_4 are considered to be ideal.

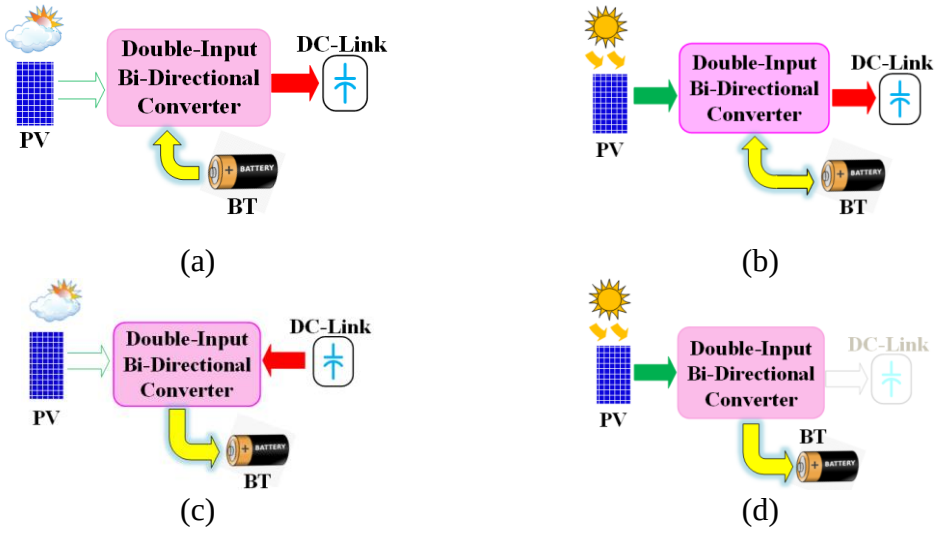


Figure 8.2: Different scenarios according to different condition of PV and load; (a) Scenario I.(b) Scenario II.(c) Scenario III.(b) Scenario IV.

5) Scenario I: Depending on the output power of PV array, the converter works as either dual-input converter (DIC) or single-input single-output converter (SISOC). If the generated power of PV is zero, i.e., $\boldsymbol{P_{PV} = 0}$, the converter operates as a SISOC and the battery supplies the load alone, and if PV cannot meet the demanded, i.e.,$\boldsymbol{P_{PV} < P_{out}}$, the converter operates as a DIC. In this condition, the battery is discharged and helps to supply the load so that the output voltage is controlled at a constant value. The operation modes for these two different cases are similar. According to the assumptions, the proposed converter operation during one switching period can be divided into four intervals. The

corresponding equivalent circuits and the key waveforms during one switching period are depicted in Figure 8.3.

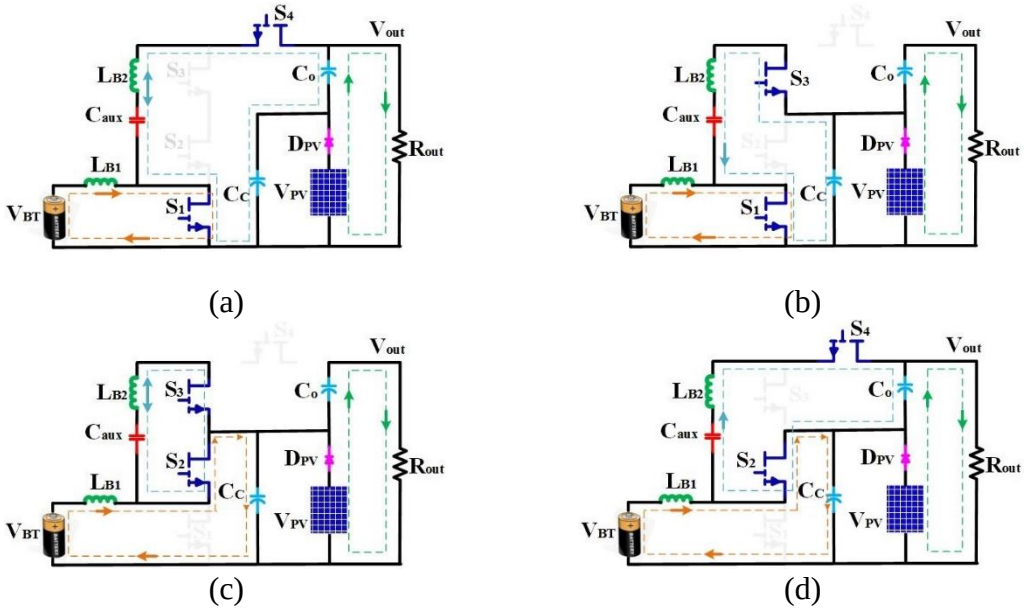


Figure 8.3: Operation modes and key waveforms for scenario I. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV.

Interval I [t_0-t_1]: At time t_0, switches S_1 and S_4 are on, and the battery current is going through the inductor L_{B1}; so, the inductor is being charged. Figure 8.3 (a) illustrates the current flow path for this interval. The voltage across inductor L_{B2} is negative, therefore its current decreases linearly, demonstrated in Figure 8.4. As a result of adopting active-clamped circuit, the voltage stress of switches S_2 and S_3 are limited to the voltage of capacitors C_C and C_O, respectively.

$$\begin{cases} L_{B1}\dfrac{di_{LB1}}{dt} = v_{BT} \\ L_{B2}\dfrac{di_{LB2}}{dt} = v_{Ca} - v_{Cc} - v_{Co} \\ C_a\dfrac{dv_{Ca}}{dt} = -i_{LB2} \\ C_c\dfrac{dv_{Cc}}{dt} = i_{LB2} - \dfrac{v_{Cc} + v_{Co}}{R_o} \\ C_o\dfrac{dv_{Co}}{dt} = i_{LB2} - \dfrac{v_{Cc} + v_{Co}}{R_o} \end{cases} \quad (8\text{-}1)$$

Interval II [t_1-t_2]: At time t_1, switch S_4 is turned off and S_3 is turned on. The current flow path for this interval is depicted in Figure 8.3 (b). As shown in in Figure 8.4, the current of inductor L_{B1} increases, but the current of L_{B2} changes depending on the voltage of V_{Cc} and V_{Ca}.

$$\begin{cases} L_{B1}\dfrac{di_{LB1}}{dt} = v_{BT} \\ L_{B2}\dfrac{di_{LB2}}{dt} = v_{Ca} - v_{Cc} \\ C_a\dfrac{dv_{Ca}}{dt} = -i_{LB2} \\ C_c\dfrac{dv_{Cc}}{dt} = i_{LB2} - \dfrac{v_{Cc} + v_{Co}}{R_o} \\ C_o\dfrac{dv_{Co}}{dt} = -\dfrac{v_{Cc} + v_{Co}}{R_o} \end{cases} \quad (8\text{-}2)$$

Interval III [t_2-t_3]: At time t_2, switches S_1 is off and S_2 is on. Figure 8.3(c) shows the current flow path for this interval. The current of inductor L_{B1} and L_{B2} decreases and increases linearly, respectively.

$$\begin{cases} L_{B1}\dfrac{di_{LB1}}{dt} = v_{BT} - v_{Cc} \\ L_{B2}\dfrac{di_{LB2}}{dt} = v_{Ca} \\ C_a\dfrac{dv_{Ca}}{dt} = -i_{LB2} \\ C_c\dfrac{dv_{Cc}}{dt} = i_{LB1} - \dfrac{v_{Cc}+v_{Co}}{R_o} \\ C_o\dfrac{dv_{Co}}{dt} = -\dfrac{v_{Cc}+v_{Co}}{R_o} \end{cases} \tag{8-3}$$

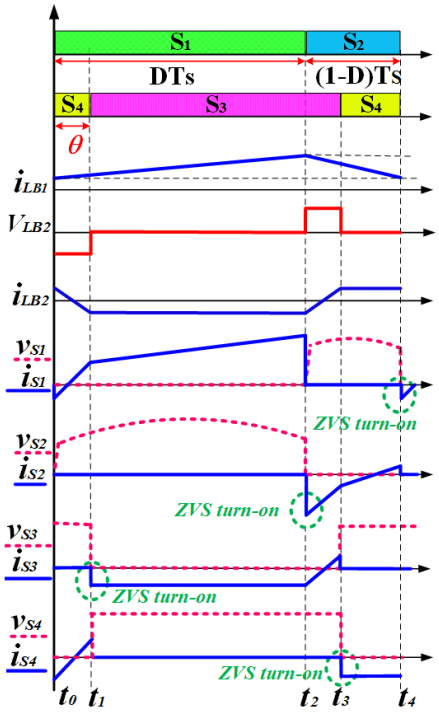


Figure 8.4: Key waveforms.

Interval IV [t_3-t_4]: At time t_1, switches S_3 is turned off and S_4 is turned on. Figure 8.3 (d) shows the current flow path for this interval. Depending on the voltage of V_{Cc} and V_{Ca}, the current waveform of inductor L_{B2} varies. As shown in Figure 8.4, for the equal value of V_{Cc} and V_{Ca}, the current will be "flat".

$$\begin{cases} L_{B1}\dfrac{di_{LB1}}{dt} = v_{BT} - v_{Cc} \\ L_{B2}\dfrac{di_{LB2}}{dt} = v_{Ca} - v_{Co} \\ C_a\dfrac{dv_{Ca}}{dt} = -i_{LB2} \\ C_c\dfrac{dv_{Cc}}{dt} = i_{LB1} - \dfrac{v_{Cc} + v_{Co}}{R_o} \\ C_o\dfrac{dv_{Co}}{dt} = i_{LB2} - \dfrac{v_{Cc} + v_{Co}}{R_o} \end{cases} \quad (8\text{-}4)$$

6) *Scenario II*: During this scenario, the generated power of PV is more than the load demand, so the battery is charged by the extra power. The converter works as a dual-output converter in this condition. The operation intervals and the equivalent circuits are similar to those in the scenario I, except the inductor current i_{LB1} is different. Figure 8.5 shows the inductor current i_{LB1} for scenario I and II according to the different condition of PV power P_{PV} and load power P_{out}.

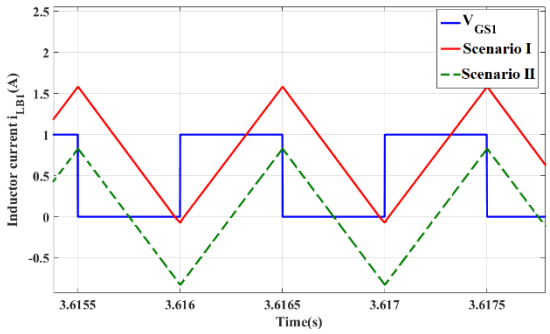
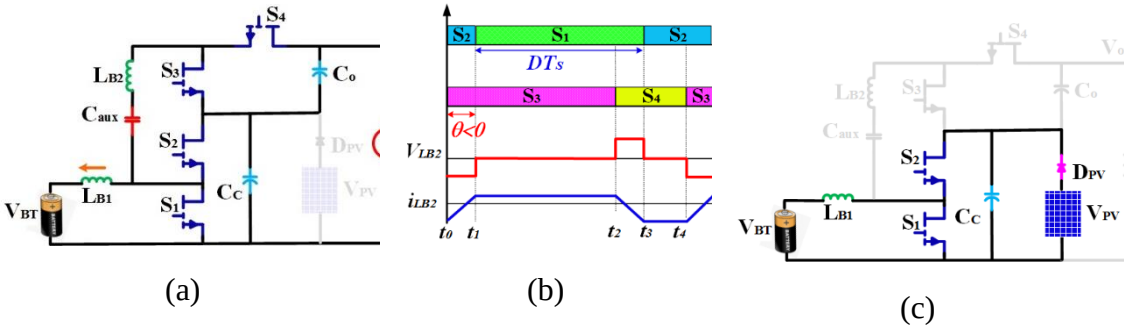


Figure 8.5: The inductor current for different scenarios I ($P_{PV} < P_{out}$) and II ($P_{PV} > P_{out}$).

7) Scenario III: In this scenario, the grid charges the battery through an inverter. Whereas in scenario I, the gate pulse of switch S_1 leads that of switch S_3, in this scenario the gate pulse of switch S_1 lags that of switch S_3 to control the power flow in the reverse direction, which means the phase shift ratio, θ, is negative. The equivalent circuit and the key waveforms in this scenario are depicted in Figure 8.5. As shown in Figure 8.6 (a), the

power flows from HVP to the battery. The operation modes in this scenario are similar to those in scenario I with different sequence of intervals. As shown in Figure 8.6 (b), the sequence of switching intervals in a switching cycle happens as follows: S_2S_3, S_1S_3, S_1S_4, and S_2S_4.

S*cenario IV:* In this scenario, the load is disconnected and the generated power of PV array charges only the battery. The principle of operation of the converter in this scenario is similar to that of a conventional ABHB converter. The switches S_1 and S_2 are driven complementary and other switches are turned off. There are two intervals in one switching period. The equivalent circuit of proposed converter during scenario IV is depicted in Figure 8.6 (c).



(a) (b) (c)

Figure 8.6: Equivalent circuit and key waveforms of converter in scenario III and IV. (a) Equivalent circuit in scenario III. (b) Key waveforms in scenario III. (c) Equivalent circuit in scenario IV.

8.2.1 Steady-State Characteristics

1) Voltage gain

From aforementioned assumptions in the Section A, the relation between the voltage of HVP port and Low-voltage port (LVP) can be obtained. From Figure 8.2, it is apparent that the output voltage is summation of voltage of capacitors C_C and C_O.

$$V_{out} = V_{Cc} + V_{Co} \tag{8-5}$$

By applying the volt-sec balance on the inductor L_{B1}, V_{Cc} can be expressed by

$$V_{Cc} = \frac{V_{BT}}{1 - D} \tag{8-6}$$

From Figure 8.1, the HVP of proposed STPTLC can be modeled as a bidirectional buck-boost converter, represented in Figure 8.5. According to Figure 87 and the volt-sec balance on the inductor L_{B2}, V_{Co} can be obtained by

$$V_{Co} = \frac{V_{db}}{1 - D} \tag{8-7}$$

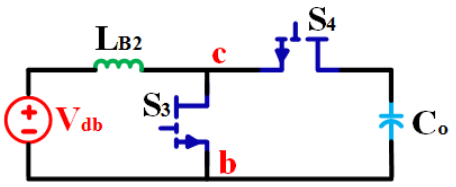


Figure 8.7: Equivalent circuit of HVP of proposed STPTLC.

As the average voltage across the inductor is zero in the steady state, the relation of voltages on two side of inductor L_{B1} in Figure 8.1 results in the following equation:

$$V_{BT} + V_{Ca} = V_{db} + V_{Cc} \tag{8-8}$$

From (5) – (8), the output voltage V_{out} can be calculated as follows:

$$V_{out} = \frac{2V_{BT}}{1 - D} + \frac{V_{Ca} - V_{Cc}}{1 - D} \tag{8-9}$$

From Figure 8.4 (e), to extend the ZVS range for switches S_3 and S_4 and to equalize the voltage rating of switches and capacitors, the voltages V_{Cc}, V_{Ca},V_{Co} should be equal. So, the relation between the voltage of HVP port and LVP port can be obtained as follows:

$$V_{out} = \frac{2V_{BT}}{1-D} \tag{8-10}$$

2) Analysis of Inductor Current and Transferred Power

In order to keep the output voltage regulated as well as control the power flow, the PPSM scheme is proposed for STPTLC. Firstly, the relationship of transferred power with phase-shift ratio (θ) and duty cycle (D) needs to be derived. As illustrated in Figure 8.8, depending on the values of D and θ, there are four operating cases that require to be studied thoroughly: 1) case I, when $\theta < 1 - D < 0.5$**;** 2) case II, when $1 - D < \theta < 0.5$; 3) case III, when $\theta < D < 0.5$; 4) case IV, when $D < \theta < 0.5$. In Figure 8.8, "Boost Mode" represents the power flow from LVP to HVP, i.e., $P > 0$ and $\theta > 0$. When $P < 0$ and$\theta <$ 0, which is defined as "Buck Mode", the power the power flows from HVP to LVP.

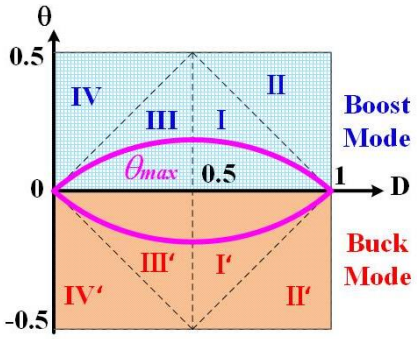


Figure 8.8: Operating cases for different values of phase shift ratio θ versus duty-cycle D.

Case 1 [θ< (1-D) < 0.5] [see Figure 8.9 (a)]:

The key waveforms for this case are shown in Figure 8.9 (a). From current-second balance principle on the capacitor C_{aux}, the relationship between the inductor current i_{LB2} at t_0 and t_3 can be derived by

$$\int_0^{T_s} i_{C,aux}(t)dt = 0 \tag{8-11}$$

$$i_{LB2}(t_0)(1-D)T_S + i_{LB2}(t_3)DT_S = 0 \tag{8-12}$$

From operation modes and Figure 8.4 (a), the inductor current i_{LB2} at t_3 can be expressed by

$$i_{LB2}(t_3) = i_{LB2}(t_0) - \frac{V_{Co} + V_{Cc} - V_{Ca}}{L_{B2}}\theta T_S \tag{8-13}$$

From current-second balance principle on the capacitor C_O, the average current of switch S_4 can be written by

$$\int_0^{T_s} i_{S4}(t)dt = I_{out} \tag{8-14}$$

From (12) - (14), the output power can be calculated by

$$P = \frac{V_O^2 T_S}{4L_{B2}}(2D - 2D^2 - |\theta|)|\theta| \tag{8-15}$$

From (15) it is obvious that the transferred power is inversely related to the switching frequency $\boldsymbol{f_s}$ and inductance $\boldsymbol{L_{B2}}$. The maximum power can be obtained at the maximum phase-shift ratio (θ_{max}) as follows:

$$\frac{dP}{d|\theta|} = \frac{V_{out}^2 T_S}{4L_{B2}}(2D - 2D^2 - 2|\theta_{max}|) = 0 \tag{8-16}$$

$$|\theta_{max}| = D - D^2 \tag{8-17}$$

$$P_{\max} = \frac{V_{out}^2 T_S}{4L_{B2}}(D - D^2)^2 \tag{8-18}$$

The maximum transferred power as a function of switching frequency f_s and inductance L_{B2} is presented in *Figure 8.10* (a). As shown in this figure, the maximum transferred power decreases with increase of either switching frequency or inductance**.**

Case 2 [(1-D) < θ < 0.5] [see Figure 8.9(b)]:

Figure 8.9(b) shows the current and voltage waveforms for operating case 2. Employing the similar derivation procedure, the output power can be obtained by

$$P=\frac{V_{out}^2 T_s}{4L_{B2}}(1-D)^2(1-2|\theta|) \tag{8-19}$$

Case 3 [θ < D < 0.5] [see Figure 8.9 (c)]:

The current and voltage waveforms for this case are depicted in Figure 8.9 (c). With the same analysis method, the output power in this case is completely similar to *Case 1*, which is a function of the phase-shift ratio (θ) and duty cycle (D), determined by

$$P=\frac{V_{out}^2 T_s}{4L_{B2}}(2D-2D^2-|\theta|)|\theta| \tag{8-20}$$

Case 4 [D <θ < 0.5] [see Figure 8.9 (d)]:

The key waveforms for this case are shown in Figure 8.9 (d). Applying the similar mathematical derivation, the output power is given by

$$P=\frac{V_{out}^2 T_s}{4L_{B2}}D^2(1-2|\theta|) \tag{8-21}$$

Figure 8.10 (b) shows the delivered power as function of duty cycle and phase-shift ratio for different operation modes, in which the negative power refers to a power transfer from HVP to LVP. As depicted in Figure 8.10 (b), the direction of power flow can be changed seamlessly because the proposed converter has a unified operation for various values of

phase shift ratio; so, similar equations are valid for a negative phase shift ratio. It is important to note that zero delivered power does not imply zero current. In essence, when the phase-shift ratio is zero (θ=0), there is reactive power going through the switches resulting in some switching losses. Further examinations show that the transferred power curve is symmetric around the axis D=0.5, and it enhances with the rise of the duty cycle (D) for D ≤ 0.5 and the decrease of D for D>0.5. The transferred power curve is analogous to the sinusoidal wave when the duty cycle is fixed. The maximum transferred power in Boost Mode and Buck Mode are identical to each other, happening at D=0.5 and θ=±0.25.

3) Current and Voltage Stress of Switches

In order to calculate the current stress of switches, first the current of inductor L_{B2}, i_{LB2}, should be thoroughly analyzed.

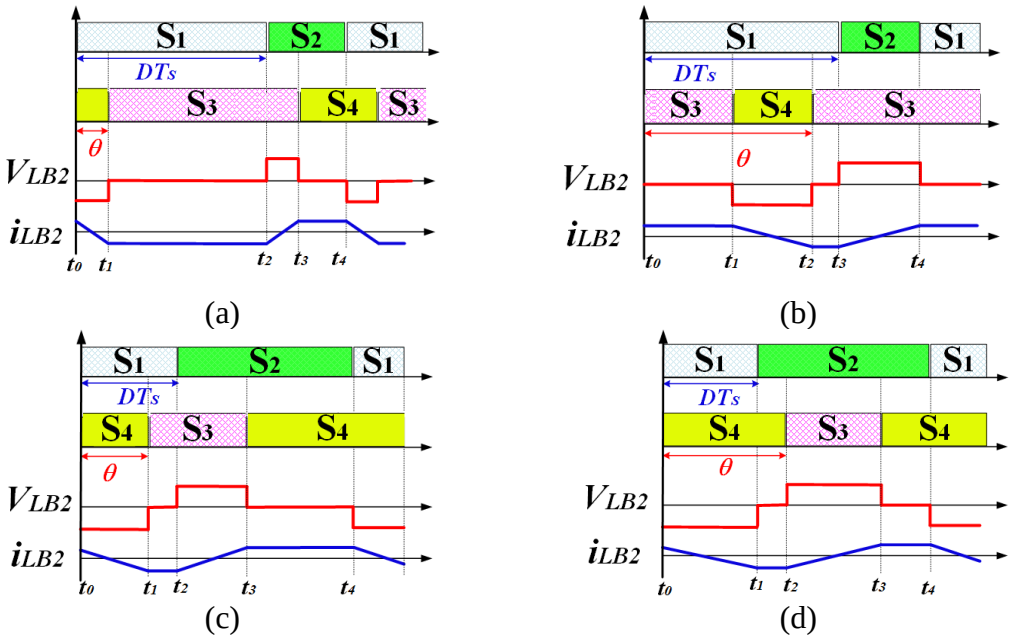
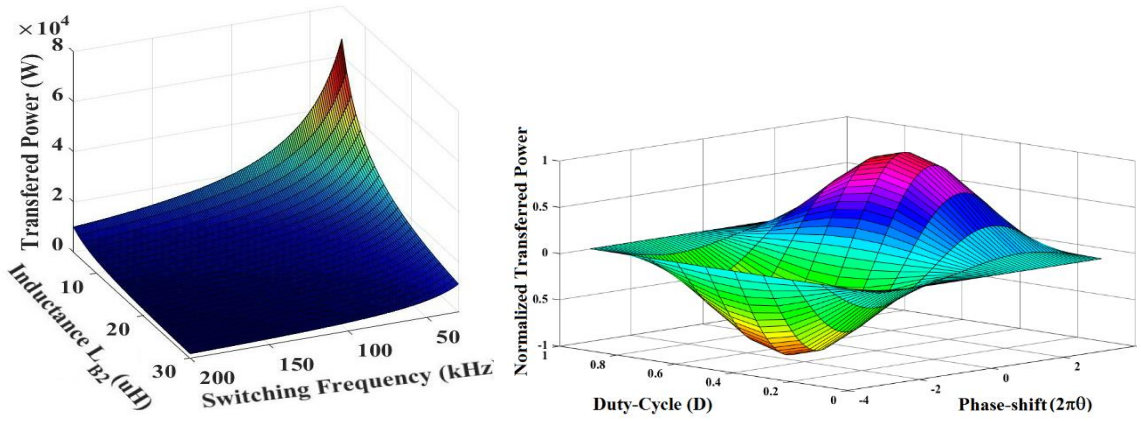


Figure 8.9: Different operation modes according to different values of duty-cycle and phase shift ratio θ. (a) Case 1. (b) Case 2. (c) Case 3. (d) Case 4.



(a) (b)

Figure 8.10: Maximum transferred power and normalized transferred power; (a) Maximum transferred power as a function of switching frequency f_s and inductance L_{B2}. (b) Normalized transferred power versus different phase-shift ratio and duty cycle.

From the explanation given in "Operation Mode Analysis" section, the inductor current i_{LB2} can be calculated, which is given in Table 8.1. The RMS current of inductor L_{B2} for different operating cases is given in Table 8.2. The inductor current is a function of phase shift ratio θ and duty cycle D, indicating that any change in operation point can lead to change of the peak current and RMS current of switches; hence choice of a proper phase-shift ratio and duty cycle is vital in minimizing the switching and conduction losses. Figure 8.11 shows the normalized RMS current for different values of duty cycle and phase-shift ratio. The base inductor current i_{LB2} is defined as $I_{LB2,base}$ as follows:

$$I_{LB2,base} = \frac{V_{out} T_S}{L_{B2}} \tag{8-22}$$

$$\begin{aligned} i_{S1,max} &= i_{LB1}(t_2) - i_{LB2}(t_2) \\ &= \frac{V_{out} T_s}{2L_{B2}} \frac{\theta(1 - D^2 - \theta)}{1 - D} + \frac{V_{out} T_s}{2L_{B1}} \frac{(1 - D)D}{2} \end{aligned} \tag{8-23}$$

$$i_{S2,max} = -i_{LB1}(t_4) + i_{LB2}(t_4) = \frac{V_{out} T_s}{2L_{B2}} \frac{\theta(D^2 - D + \theta)}{1 - D} + \frac{V_{out} T_s}{2L_{B1}} \frac{(1 - D)D}{2} \tag{8-24}$$

Table 8.1: The Current of inductor L_{B2} for different values of D and θ.

Condition	$i_{LB2}(t=t_0\text{-}t_1)$	$i_{LB2}(t=t_1\text{-}t_2)$	$i_{LB2}(t=t_2\text{-}t_3)$	$i_{LB2}(t=t_3\text{-}t_4)$
$\lvert\theta\rvert < (1-D) < 0.5$	$\frac{V_{out}T_s}{2L_{B2}}(\theta D - \frac{t}{T_s})$	$-\frac{V_{out}T_s}{2L_{B2}}\theta(1-D)$	$\frac{V_{out}T_s}{2L_{B2}}[-\theta(1-D)-D+\frac{t}{T_s}]$	$\frac{V_{out}T_s}{2L_{B2}}\theta D$
$(1-D) < \lvert\theta\rvert < 0.5$	$\frac{V_{out}T_s}{2L_{B2}}(1-D)(1-\theta)$	$\frac{V_{out}T_s}{2L_{B2}}(\theta D - \frac{t}{T_s})$	$-\frac{V_{out}T_s}{2L_{B2}}\theta(1-D)$	$\frac{V_{out}T_s}{2L_{B2}}[-\theta(1-D)-D+\frac{t}{T_s}]$
$\lvert\theta\rvert < D < 0.5$	$\frac{V_{out}T_s}{2L_{B2}}(\theta D - \frac{t}{T_s})$	$\frac{V_{out}T_s}{2L_{B2}}(\theta D - \frac{t}{T_s})$	$\frac{V_{out}T_s}{2L_{B2}}[-\theta(1-D)-D+\frac{t}{T_s}]$	$\frac{V_{out}T_s}{2L_{B2}}\theta D$
$D < \lvert\theta\rvert < 0.5$	$\frac{V_{out}T_s}{2L_{B2}}(\theta D - \frac{t}{T_s})$	$-\frac{V_{out}T_s}{2L_{B2}}D(1-\theta)$	$\frac{V_{out}T_s}{2L_{B2}}[-D(1-\theta)-\theta+\frac{t}{T_s}]$	$\frac{V_{out}T_s}{2L_{B2}}\theta D$

Table 8.2: The RMS Current of inductor L_{B2} for different operating cases.

Operating Case	Condition	RMS Current of inductor L_{B2}
Case 1	$\|\theta\| < (1-D) < 0.5$	$I_{LB2,rms} = \frac{V_{out}T_s}{2L_{B2}}\sqrt{-\frac{\theta^2(3D^2-3D+\theta)}{3}}$
Case 2	$(1-D) < \|\theta\| < 0.5$	$I_{LB2,rms} = \frac{V_{out}T_s}{2L_{B2}}\sqrt{\frac{(D-1)^2(-3\theta^2+3\theta+D-1)}{3}}$
Case 3	$\|\theta\| < D < 0.5$	$I_{LB2,rms} = \frac{V_{out}T_s}{2L_{B2}}\sqrt{-\frac{\theta^2(3D^2-3D+\theta)}{3}}$
Case 4	$D < \|\theta\| < 0.5$	$I_{LB2,rms} = \frac{V_{out}T_S}{2L_{B2}}\sqrt{\frac{D^2(3\theta-3\theta^2-D)}{3}}$

The maximum current of switches can be expressed as follows:

$$i_{S3,max} = i_{LB2}(t_3) = \frac{V_{out}T_s}{2L_{B2}}\theta D \tag{8-25}$$

$$i_{S4,max} = -i_{LB2}(t_0) = \frac{V_{out}T_s}{2L_{B2}}\theta D \tag{8-26}$$

From Figure 8.4, it is apparent that the LVP and the HVP switches should withstand the voltage of clamp capacitor V_{Cc} and V_{Co}, respectively. Therefore, the voltage stress of power switches can be obtained from (6) and (7) as follows:

$$V_{S1} = V_{S2} = V_{S3} = V_{S4} = \frac{V_{BT}}{1-D} = \frac{V_{out}}{2} \tag{8-27}$$

4) ZVS Performance

Aside from the conduction loss, the switching loss is another concern to provide the high-efficiency operation. In this section, detailed analysis of the soft-switching performance in the proposed converter is given. In the proposed converter, ZVS soft-switching performance can be realized owing to the PPSM control algorithm. Figure 8.12 shows the circuit modes when S_1 and S_2 are operating at ZVS.

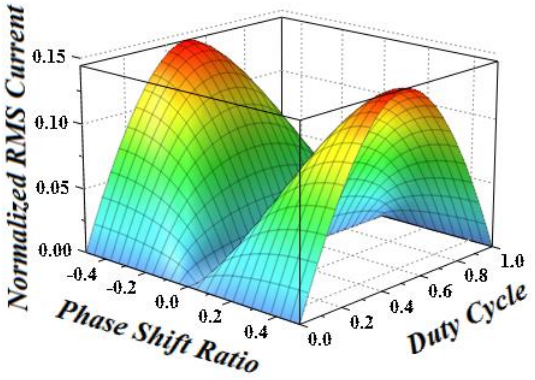


Figure 8.11: Normalized RMS current versus different phase-shift ratio and duty cycle.

In this case, before turn-on of S_2, the current i_{LB2} is negative as shown in Figure 8.5 and corresponding switching voltages are shown in Figure 8.12 (a). After turning-off of switch S_1, parasitic capacitance of switch S_2, C_{oss2}, discharges from V_{Cc} to zero and parasitic capacitance of switch S_1, C_{oss1}, charges from zero to V_{Cc}, as shown in Figure 8.12 (b). After the completion of the charging and discharging process, the difference of the current of the inductors L_{B1} and L_{B2} freewheels through the antiparallel diode of switch S_2. As switch S_2 is provided with turn-on gate signals, it starts conducting at zero voltage. In similar way, the ZVS operation of other switches can also be visualized.

In this part, the soft switching performance in this region during scenario I, the battery discharging operation, is discussed. As discussed in section B, case 1 is recognized as the low inductance current region, shown in Figure 8.11. In fact, the ZVS soft-switching performance in the scenario I is quite similar to that in scenario II, III, and IV. The results and analytical procedure derived in this section are valid for the proposed converter regardless of the operation scenario.

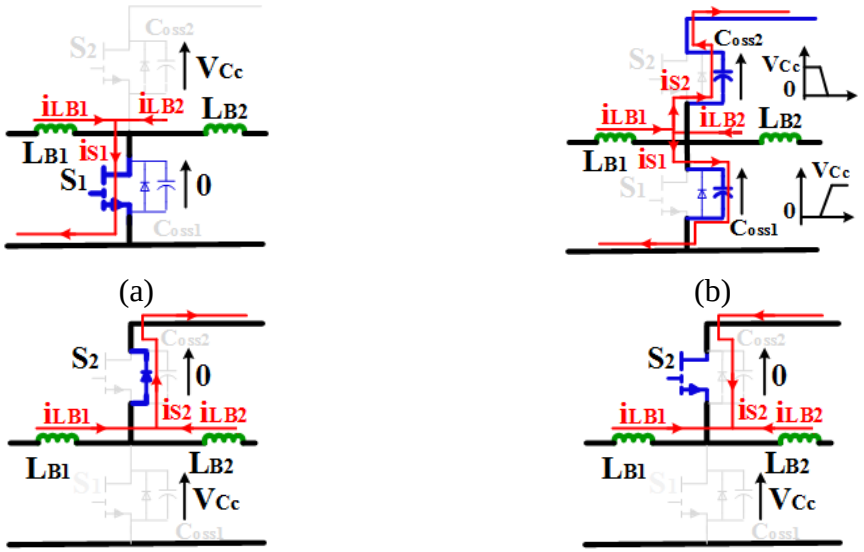


Figure 8.12: ZVS turn-on of switch S_2. (a) just before turn-on instant. (b) rapid charging and discharging of output capacitor C_{oss1} and C_{oss2}. (d) antiparallel diode freewheeling. (d) current polarity alternation.

The conditions to obtain ZVS performance of switches S_1-S_4 can be expressed by

$$i_{S1}(t_0) = (i_{LB1}(t_0) - \frac{V_{out}T_s}{2L_{B2}}\theta D) < 0 \qquad \text{For } S_1 \qquad (8\text{-}28)$$

$$i_{S2}(t_2) = \left(i_{LB1}(t_2) - \frac{V_{out}T_s}{2L_{B2}}\theta(1-D)\right) > 0 \qquad \text{For } S_2 \qquad (8\text{-}29)$$

$$i_{S3}(t_1) = \left(-\frac{V_{out}T_s}{2L_{B2}}\theta(1-D)\right) < 0 \qquad \text{For } S_3 \qquad (8\text{-}30)$$

$$i_{S4}(t_3) = \left(\frac{V_{out}T_s}{2L_{B2}}\theta D\right) > 0 \qquad \text{For } S_4 \qquad (8\text{-}31)$$

The maximum and minimum inductor current i_{LB1} happens at t_0 and t_2, respectively, which can be calculated by

$$i_{LB1}(t_0) = \frac{P_{BT}}{V_{BT}} - \frac{V_{BT}DT_s}{2L_{B1}} = \frac{V_{out}T_s}{2L_{B2}}\frac{\theta(2D-2D^2-\theta)}{1-D} - \frac{V_{BT}DT_s}{2L_{B1}} \qquad (8\text{-}32)$$

$$i_{LB1}(t_2) = \frac{P_{BT}}{V_{BT}} + \frac{V_{BT}DT_s}{2L_{B1}} = \frac{V_{out}T_s}{2L_{B2}}\frac{\theta(2D - 2D^2 - \theta)}{1 - D} + \frac{V_{BT}DT_s}{2L_{B1}} \tag{8-33}$$

According to (28) and (29), the soft-switching condition of switches S_1 and S_2 is more rigorous than that of switches S_3 and S_4 due to the DC current injection. Thus, ZVS turn-on performance of all switches can be satisfied once the following conditions are met.

$$i_{S1}(t_0) = \frac{V_{out}T_s}{2L_{B2}}\frac{\theta(D-D^2-\theta)}{1-D} - \frac{V_{BT}DT_s}{2L_{B1}} < 0 \tag{8-34}$$

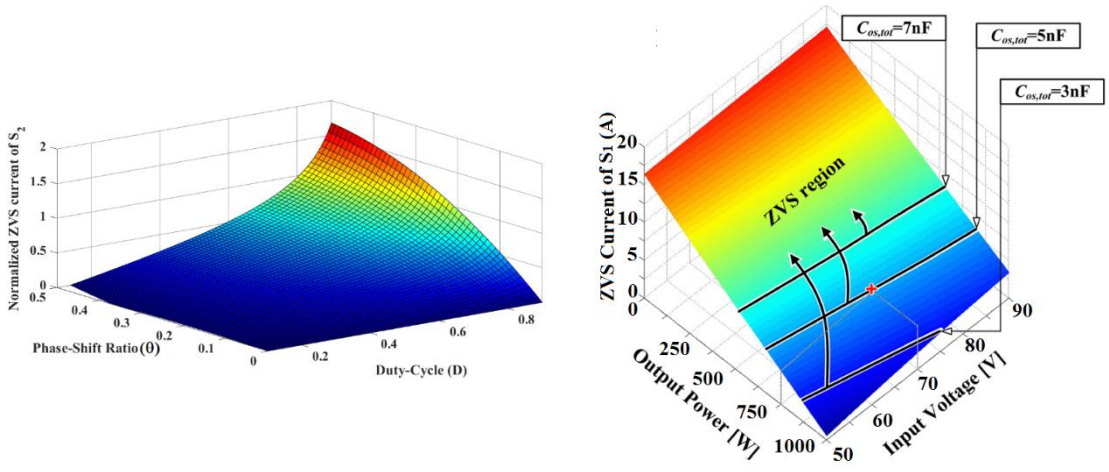
$$i_{S2}(t_2) = \frac{V_{out}T_s}{2L_{B2}}\frac{\theta(4D-3D^2-\theta)}{1-D} > 0 \tag{8-35}$$

From (34) and (35), it is apparent that the ZVS performance depends on the duty cycle, the phase-shift ratio, the output voltage, the inductance L_{B2}, and switching frequency f_s. The ZVS current of switch S_2 is shown in Figure 8.13 (a), which implies that the ZVS of switch S_2 at turn-on instant can be realized in the overall duty-cycle and phase-shift ratio. Another condition to achieve the ZVS performance is that the energy stored in the inductance L_{B2} should discharge the output capacitor of switch S_1 to zero. Thus, the detailed ZVS condition of switch S_1 can be derived as:

$$(i_{LB2}(t_0))^2 > \frac{2C_{oss}V_{Cc}^2}{L_{B2}} + (i_{LB1}(t_0))^2 \tag{8-36}$$

The soft switching range of switch S_1 is depicted in Figure 8.13 (b) as a function of battery voltage V_{BT} and output power P_{out}. It can be seen that that the larger inductance L_{B2}, the easier switch S_1 can obtain ZVS. It demonstrates that ZVS current of switch S_1 reduces when the output power increases. Additionally, it highlights that as the output capacitance of switch decreases, the soft-switching range of switch S_1 increases. So, GaN switches allows for the implementation of soft-switching performance in a wide range of output power and input voltage due to their smaller output capacitance compared to their silicon-

based counterparts. As a conclusion, ZVS can be implemented for all the switches for a wide operating range in this case. It is noteworthy that soft-switching performance of switches in other cases can be ensured similarly.



(a) (b)

Figure 8.13: ZVS current of switches S_1 and S_2. (a) Normalized ZVS current of switch S_2 versus different phase-shift ratio and duty cycle. (b) ZVS current of switch S_1 versus different battery voltage and output power.

8.2.2 Design Considerations

1) Passive Component Selection:

In this section, the design guide to choosing the inductors L_{B1} and L_{B2} and the auxiliary capacitor C_{aux} is given. The inductor L_{B1} works as a filter in the boost converter to limit the battery current ripple, so it can be obtained as follows:

$$L_{B1} = \frac{DT_S V_{BT}}{(\Delta I_{LB1})} \tag{8-37}$$

The design of inductor L_{B2} is of paramount importance for the proposed converter since it plays an indisputable role in the soft switching, the conduction losses, and the maximum transferred power; so, more attention should be given to its selection. According to (31)

and (36), to achieve the soft-switching, the inductor L_{B2} should satisfy the following conditions (38)-(39).

$$L_{B2} > \frac{\theta(D - D^2 - \theta)V_{out}}{(1 - D)DV_{BT}} L_{B1} \tag{8-38}$$

$$L_{B2} > \frac{2C_{oss}V_{Cc}^2}{(\frac{V_{uto}T_s}{2L_{B2}}\theta D)^2 - \left(\frac{V_{out}T_s}{2L_{B2}}\frac{\theta(2D - 2D^2 - \theta)}{1 - D} - \frac{V_{BT}DT_s}{2L_{B1}}\right)^2} \tag{8-39}$$

It can be observed that the larger inductance L_{B2} is selected, the more possible soft-switched turn-on operation can be. On the other hand, according to (8-18), increasing L_{B2} shrinks the maximum transferred power.

Regarding the auxiliary capacitor C_{aux}, it is assumed this capacitor acts as a voltage source; so, this capacitance should be chosen such that it is adequately large. In addition, the auxiliary capacitance is selected so large that the resonance between the auxiliary capacitor C_{aux} and inductor L_{B2} is avoided.

2) Control Scheme

As previously discussed, a PPSM scheme is implemented in the proposed STPTLC. As exhibited in Figure 8.14 (a), u_{tri1} and u_{tri2} are the two carrier signals, D is the duty-cycle of switches S_1 and S_3 and regulated by control voltage u_D, and θ is the phase shift ratio between u_{tri1} and u_{tri2}, and T_S is the switching period. Balancing the power and voltage between battery and PV, duty-cycle D is applied as one of the control freedoms, while the phase shift ratio θ is employed as the second control freedom to regulate the voltage and power between PV and load. Based on the operation principles of STPTLC, the equivalent circuit between the battery and PV is an asymmetrical bidirectional half-bridge converter, and the equivalent circuit between the PV and the load is a non-inverting bidirectional

buck-boost converter. The modulation scheme depicted in Figure 8.14 (a) paves the way for the independent control of the control of ABHB converter and noninverting bidirectional buck-boost converter. In other words, the PV resembles the output of the ABHB converter and input of noninverting bidirectional buck-boost converter, implying the load and the battery is decoupled by the PV. The block diagram of control scheme is shown in Figure 8.14 (b), including maximum power point tracking (MPPT) control of PV, battery charging control, and load voltage control. The MPPT controller is adopted for extracting maximum available power from PV module under all conditions. Since the battery voltage is constant, the output voltage can be regulated by a voltage-mode control loop. The sign of phase-shift ratio θ indicates the power flow direction. The positive and negative values indicate the power flow from LVP to HVP and from HVP to LVP, respectively. Due to the symmetrical performance of converter in Scenarios I and III, seamless power flow can be obtained by adopting PPSM. To balance the voltage of output capacitors C_O and C_C, the duty-cycle D is employed that aids in developing the ZVS range for HVP switches and equalizing the voltage stress across all switches.

3) PCB Layout Considerations

The use of GaN switches is rapidly increasing in high-efficiency, high-power density applications due to their intrinsic merits; however, special care should be taken not only for the component selection, but the PCB layout as well to take full advantage of the intrinsic capabilities of the GaN switches in the final design. Main issues to be addressed in the adoption of GaN switches in power converters are controlling the voltage and current variation, di/dt and dv/dt, which necessitates proper attention to the PCB design to minimize the parasitic elements.

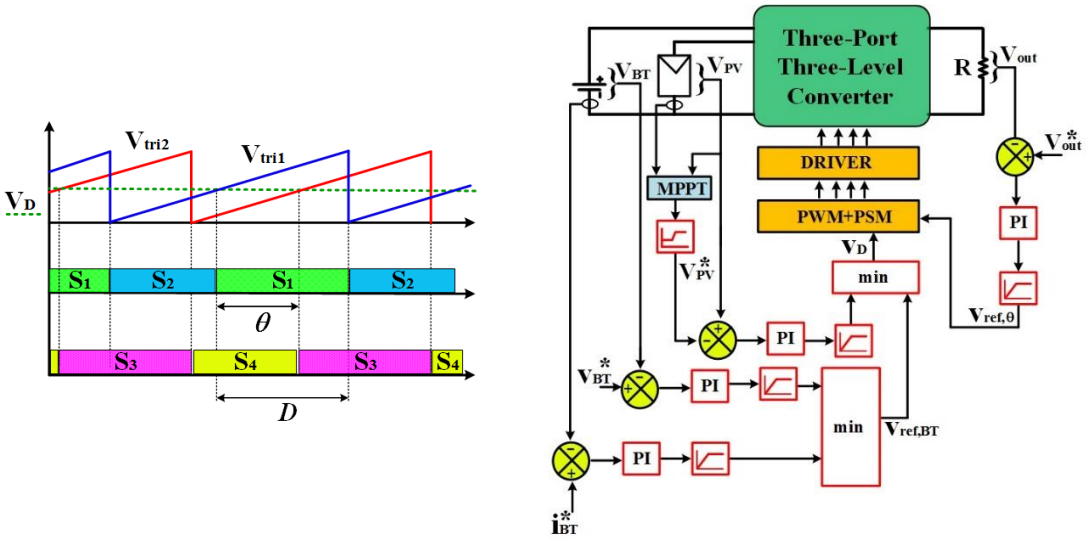


Figure 8.14: Control scheme: (a) modulation scheme, (b) control block diagram of proposed converter.

So, it is necessary to have precise simulation model to make sure that the behavior of the circuit is in accordance with the experimental design. Figure 8.15 shows the schematic diagram of STPTLC including different parasitic elements, consisting of the driving circuit and decoupling capacitors. In Figure 8.15, L_{Swi} and L_{Cwi} represent the source parasitic inductance and the common parasitic inductance, respectively. L_{Ci}, L_{Pi}, and L_{Di} represent the power loop inductance, L_{G1}, L_{S1}, and L_{Dr1} represent the gate driver loop inductance. Also, C_1 to C_8 is used to model the driving capacitors, and C_{Dec1} and C_{Dec2} show the decoupling capacitor. C_{issi}, C_{ossi}, and C_{gdi} are the input capacitance of switch S_i, output capacitance of switch S_i, and Miller capacitors, respectively. R_{Gi} and R_{Si} represent the gate resistor and parasitic gate resistor, respectively. To reach an optimal performance, designing a PCB with low common source inductance, power loop inductance, and gate-driver loop is critical [32].

Both common source inductance and power loop inductance cause huge overshoot on the drain-source voltage; however, the power loop inductances are the most crucial parameter that can increase the voltage spikes across the drain-source of the switch. So, minimizing the power loop inductances is of great importance. To ensure the power loop inductances are small, the source pin of switches S_2 and S_4 should be connected to the drain pin of switches S_1 and S_3 by the shortest path, respectively. Also, the ground pin of the driver is directly connected to the source pin of the switch to reduce the common source inductance, and consequently to avoid false turn-on and turn-off.

For this study, it was of interest to investigate the impact of placement on the parasitic inductance. In fact, a possible solution to the problem of parasitic inductances is proper placement of components on PCB. In the lateral structure, two switches of a half-bridge are placed on the same side of PCB, and conversely, in the vertical structure, two switches are mounted on the different sides resulting in small parasitic inductance [33]. In this chapter, to minimize the parasitic inductance, all switches S_1, S_2, S_3, and S_4 are mounted on the top layer of PCB and decoupling capacitors are placed on the bottom-side, shown in Figure 8.16. Moreover, to diminish the parasitic inductance, 4-layer structure of PCB is adopted by putting the polygon copper pour in parallel in 4 layers, and the switches are placed very close to each other as well, depicted in Figure 8.16 (a). From Figure 8.16(c), the current paths are stretched into the wide parallel planes in all layers, acting like an interleaved configuration, leading to small parasitic inductance.

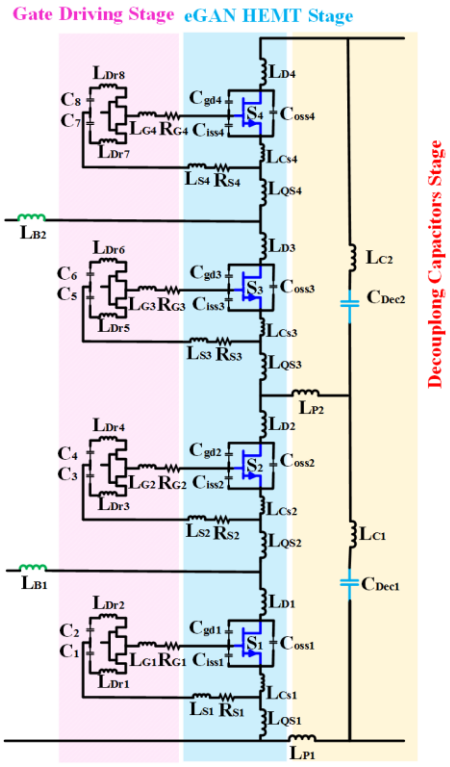
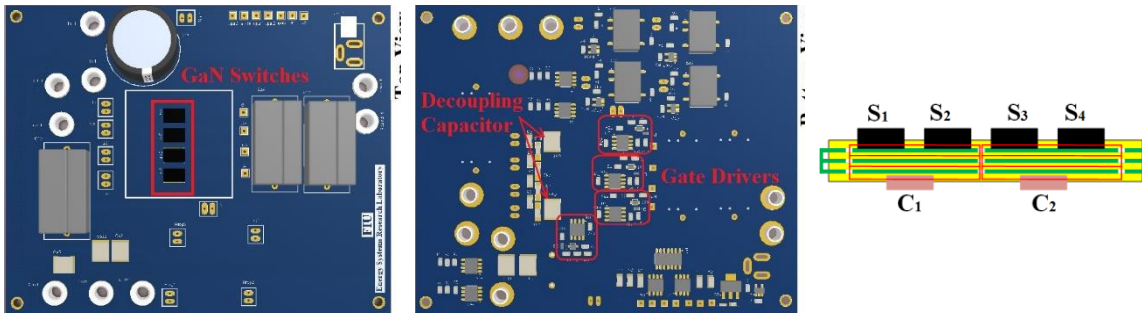


Figure 8.15: The equivalent circuit of BHB module including various parasitics.

This approach is also applied to the gate-driver circuit to decrease the gate driver loop inductance. The driver circuits are mounted exactly beneath the switches to reduce the length of the driving loop. A model is simulated in the ANSYS Q3D Extractor to estimate different parasitic components, indicates that the commutation loop inductance of proposed layout (L_{P1}, L_{P2}, L_{C1}, L_{C2}, L_{D1}, L_{D2}, L_{D3}, L_{D4}) is 1.2 nH, common parasitic inductance (L_{CS}, L_{CS2}, L_{CS3}, L_{CS4}) is 0.5 nH, the quasi-common parasitic inductance is 0.3 nH, and gate driver loop inductance is 2.2nH. Then, these values are used for the parasitics elements in the simulation to estimate the voltage spike across the switches.



(a) (b) (c)

Figure 8.16:. Layout of STPTLC; (a) Top view. (b) Bottom view. (c) Side view.

8.2.3 Comparison of The Proposed STPTLC and Other Three-Port Converters

A close look at the proposed converter and comparing it with other converters is of great importance since it provides useful information about different features of TPCs for various applications. Table 8.3 presents a number of performance parameters to compare the proposed STPTLC and new TPC topologies, including nonisolated converters cited in [17], [19], and [31], partially-isolated converter cited in [11], and isolated converter cited in [16]. Topologies are compared under certain characteristics such as number of components including switch, diode, inductor, and transformer, control technique, voltage stress of switches, and efficiency. The comparison is made only on the bases of simple synthesized topology. Control schemes and extra cells added to achieve additional benefits are not taken into account in this comparison. Regarding the soft switching operation, all of switches in these converters can achieved ZVS at turn-on, except the nonisolated converters cited in [19], in which the hard-switching operation of switch and reverse-recovery problem of diodes deteriorate the efficiency. Although the partially-isolated converter cited in [11] has the least number of switches, this converter lacks the feature of

the bidirectional power flow since the diode rectifier is employed in the output stage; so, the working scenario III is not possible with this topology.

Looking at the state-of-the-art control scheme, a classic PWM is used in the most nonisolated converters such as converters cited in [17], [19], and [31], in which a simple algorithm is adopted. The duty-cycle is the only parameter to regulate the voltage and power flow, implying the independent control of power and voltage is not feasible. One approach to regulate the voltage of three ports independently is introduced in the partially-isolated converter cited in [11], which is based on the combination of pulse frequency modulation (PFM) and PWM. Nevertheless, the interdependence of impedance and frequency complicates the design of passive components. Moreover, this control technique allows for voltage regulation for a limited operating range. The independent voltage regulation of different ports can be tackled by PPSM control scheme that provides decoupled control of power and voltage by employing phase-shift and duty-cycle, respectively. PPSM control scheme is adopted in the proposed converter for hybrid renewable energy systems with energy storage device, which can extend ZVS for a wide range of operation and decreasing the circulating current. Although PPSM control technique is applied for the isolated converter [16], high number of switches in this converter increases the complexity of the control circuit, diminishes the overall system efficiency, and increases the cost. Even though both proposed converter and the nonisolated converters [19] consist the same number of semiconductor devices, the bidirectional power flow for all three ports is possible only in the proposed converter. Compared to other converters, the proposed converter offers the main features of TPCs with a smaller number of switches and diodes as well as fewer magnetic cores. In brief,

stacked configuration offers high voltage gain with reduced voltage stress across the switches, providing the conditions to employ the switches with smaller on-resistance $R_{DS(ON)}$ that results in higher efficiency. This particular combination of high-efficiency, high-power density, and high-frequency behavior intrinsic to GaN, makes the converter attractive for applications that size is a critical parameter.

Table 8.3: **Comparison study between the proposed converter and other TPCs.**

Specification	**Nonisolated Converter [19]**	**Nonisolated Converter [31]**	**Partially-isolated converter [11]**	**Isolated converter [16]**	**Proposed Converter**
No. of switches	3	6	2	14	4
No. of diodes	1	0	4	0	0
No. of transformer	0	0	1	2	0
No. of inductors	3	2	1	2	2
Boost voltage gain (V_o/V_{in1})	1/(1-D)	1/(1-D)	N/(1-D)	$ND(1-D)R_L/(L_f f_S)$	2/(1-D)
Voltage stress of switches	$V_{in1}/(1-D)$	$V_{in1}/(1-D)$	$V_{in1}/(1-D)$	V_{in1}	$V_{in1}/(1-D)$
Control technique	PWM	PWM	PWM+ PFM	PPSM	PPSM
No. of ports with bidirectional power flow capability	2	3	2	3	3
Soft switching	Only two switches	Yes	Yes	Yes	Yes

The energy stored in inductors (E_L) and the energy stored in capacitors (E_C) provide a means for estimating the volume of a given converter. The stored energy in the inductors

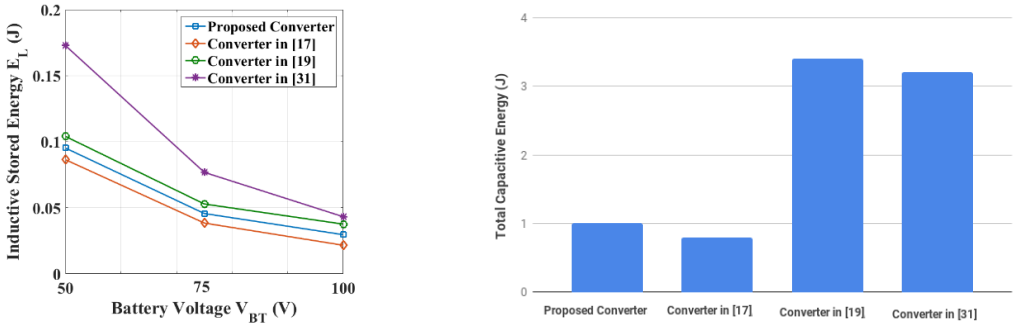
and capacitors of a converter can be calculated by (40) and (41), respectively, where I_{Li} is the dc current flowing in inductor L_i and V_{Ci} is the dc voltage of capacitor C_i.

$$E_L = \sum \frac{L_i \, I_{Li}^2}{2} \tag{8-40}$$

$$E_C = \sum \frac{C_i \, V_{Ci}^2}{2} \tag{8-41}$$

The stored energy in the inductors and capacitors for the nonisolated converters in Table III is depicted in Figure 8.17 (a) and (b), respectively, when V_o = 400V, P_o = 1 kW, f_s = 100kHz, and V_{BT} = 50~100 V. From Figure 8.17 (a), the inductive stored energy in the proposed converter is lower than that of the converters in [19] and [31], while the inductive stored energy in the proposed converter is higher than that of the converter in [17]. It implies that the estimated weight and size of the passive components for the proposed converter is lower than that of the converters in [19] and [31] and higher than that of the converters in [17]. Figure 8.17 (b) shows the total capacitive stored energy for different three-port converters. It is clear that the proposed converter has a total capacitive energy less than the converters introduced in [19] and [31] due to the employing three-level structure at the high-voltage side (HVS). Similar to the proposed converter, the converter introduced in [17] has three-level structure at HVS, offering the minimum total capacitive energy. However, compared to the proposed converter, the converter introduced in [17] only uses the inductor to transfer the energy to the HVS. In the proposed converter, the resonance between the capacitor and inductors allows the designer to control the current of the switches to reduce the turn-off losses. Moreover, even though the total number of the semiconductors in the converter introduced in [17] is more that of the proposed converter,

the operation in scenario III to transfer the power from HVS to the battery is not possible in converter [17].



(a) (b)

Figure 8.17: Comparison of the inductive and capacitive stored energy for different nonisolated TPCs. (a) Inductive stored energy. (b) Capacitive stored energy.

8.3 Experimental Results and Analysis

In this section, the experimental verification of a 1kW prototype of the PWM plus phase-shift modulated STPTLC are given to prove the theoretical analysis and operation principle of the proposed converter. The design specifications for the prototype are illustrated In Table 8.4.

Table 8.4: Design specifications.

Parameters	Value
Battery voltage V_{BT}	50-100 V
PV voltage V_{PV}	100-200 V
output voltage V_{out}	400 V
output power P_{out}	1000 W
switching frequency f_s	100 kHz
Switches	GS66508T (650 V, 30 A, $R_{DS(ON)}$ of 50 mΩ)
Inductor L_{B1}	300 uH
Inductor L_{B2}	10 uH
Auxiliary capacitor C_{aux}	DCP4I052006JD2KSSD (WIMA, 20 uF, 600 V)
Output capacitor (C_C and C_O)	DCP4I052006JD2KSSD (WIMA, 20 uF, 600 V) in parallel with C5750X6S2W225K250KA (TDK, 2.2 uF, 450 V)

8.3.1 Loss Analysis of Proposed Converter

Referring to Figure 8.5 and [1], the equations for calculating the losses in converters using GaN devices can be obtained. Table 8.5 gives the loss equations for key components, including the switching and conduction losses of switches, core and conduction losses of magnetic cores [34]. In this chapter, due to ZVS performance, the capacitive switching loss as well as the loss of capacitor is not considered. To calculate the switching loss for GaN devices, simulation using LTSpice model by the manufacturer is beneficial. The double pulse simulation model can precisely estimate the turn-on and turn-off losses.

The turn-on loss and the turn-off loss under different drain-source voltages for eGaN HEMTs GS66508P from GaN Systems Inc. can be calculated using LTSpice model. The loss breakdown under different load conditions using the equations given in Table 8.5 is presented in Figure 8.18.

Table 8.5: Loss equations for key components.

Parameters		**Value**
Switches (S_1-S_4)	Conduction loss	$P_C = R_{DS(on)} I_{S,rms}^2$
	Switching loss	By integrating the product of the voltages and currents using double pulse test circuit
	Gate drive loss	$P_G = V_d Q_{gate} f_s$
Inductors (L_{B1} and L_{B2})	Core loss	$P_v = \frac{f_S}{\frac{a}{B^3} + \frac{b}{B^{2.3}} + \frac{c}{B^{1.65}}} + d * (f_S^2 B^2)$
	Winding loss	$P_W = R_{ESR} I_{L,rms}^2$

*f_s is the switching frequency, Q_{gate} is the total gate charge and V_d is the drive voltage, which in case of SI8261BAC is 6.8V, B is the peak AC flux density, R_{ESR} is the equivalent series resistance of the inductor, and the coefficients a, b, c and d can be derived from datasheet.

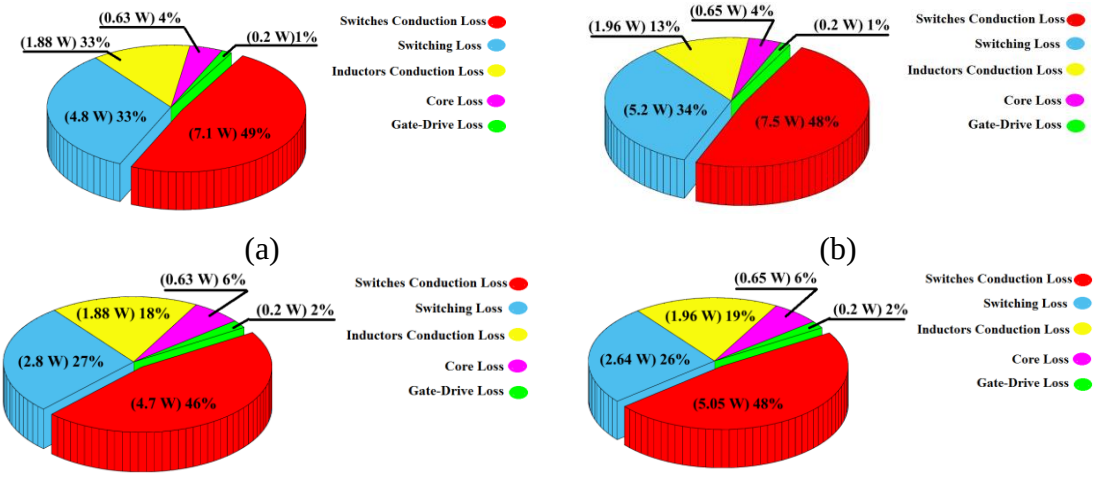


Figure 8.18: Loss breakdown for different scenarios under full-load and half-load condition. (a) Full-load P_{out}=1000W, V_{BT}=100 V, D=0.53, and scenario I. (b) Full-load P_{out}=1000W, V_{BT}=100 V, D=0.53, and scenario III. (c) Half-load P_{out}=500W, V_{BT}=60 V, D=0.75, and scenario I. (d) Half-load P_{out}=500W, V_{BT}=60 V, D=0.75, and scenario III.

The maximum theoretical efficiency for scenario I and III is 97.9 % and 97.8%, respectively. It can be concluded that, due to using GaN switches, the conduction loss in the proposed converter is decreased compared to its silicon-based counterparts.

8.3.2 Experimental Results

A 1kW prototype of proposed STPTLC converter was implemented to verify the theoretical analysis. The design specifications and the components used in the prototype are given in Table 8.4. Use of GaN switches aids in high-efficiency and high-power density due to their small on-resistance $R_{DS(ON)}$, zero reverse-recovery, and small packaging. The experimental results for different scenarios I – IV are shown in Figure 8.19 - Figure 8.22, respectively. Since the conventional TPC converters lose the soft-switching performance at light load, the converter performance at output power P_{out}=100 W is investigated from an efficiency viewpoint, shown in Figure 8.19.

The battery voltage V_{BT}, the voltage of output capacitors V_{Co} and V_{Cc}, and output voltage V_{out} are shown in Figure 8.19 (a). As it is clear the voltage of capacitors C_C and C_O are balanced, and the control circuit is working properly. The gate pulse of switches in scenario I are shown in Figure 8.19 (b), in which the duty-cycle is approximately 0.5. There is no voltage ringing caused by parasitics in the gate pulses, implying the design of gate driving circuit in PCB layout is carried out correctly.

To study ZVS performance, the gate signals and voltage stress across switches S_1, S_3, S_4, and S_2 are shown in Figure 8.19 (c), (d), (e), and (f), respectively. The voltage stress of all switches is 200 V, which is half of the output voltage. Therefore, low voltage switches with low on-resistance $R_{DS(ON)}$ can be used. The voltage spike on switch S_2 is more than other switches, which is 20 V (about 10%), meaning that low parasitic inductance is achieved by optimizing the PCB layout design. Figure 8.19 (c) and (f) illustrate the detailed turn-on instant for the switch S_1 and S_2 at 100 W, demonstrating ZVS is realized even under light load condition.

The results of converter performance at full load 1 kW for scenario I are shown in Figure 8.19. The gate signals for scenario I at full-load condition is shown in Figure 8.20 (a), indicating the duty-cycle is about 0.72. Figure 8.20 (b) clearly indicates that the clamp circuit is reducing the voltage stress of switches S_1 and S_2. Figure 8.20 (c), (d), and (e) show the gate pulse and voltage stress on the switches S_1, S_2, and S_4, respectively.

As it is clear ZVS soft-switching performance is achieved for all switches. The inductor current i_{LB1} and i_{LB2}, and the gate signal of switch S_1 are shown in Figure 8.20 (f). The current ripple of battery is in the acceptable range confirming that the design of inductor L_{B1} is precise.

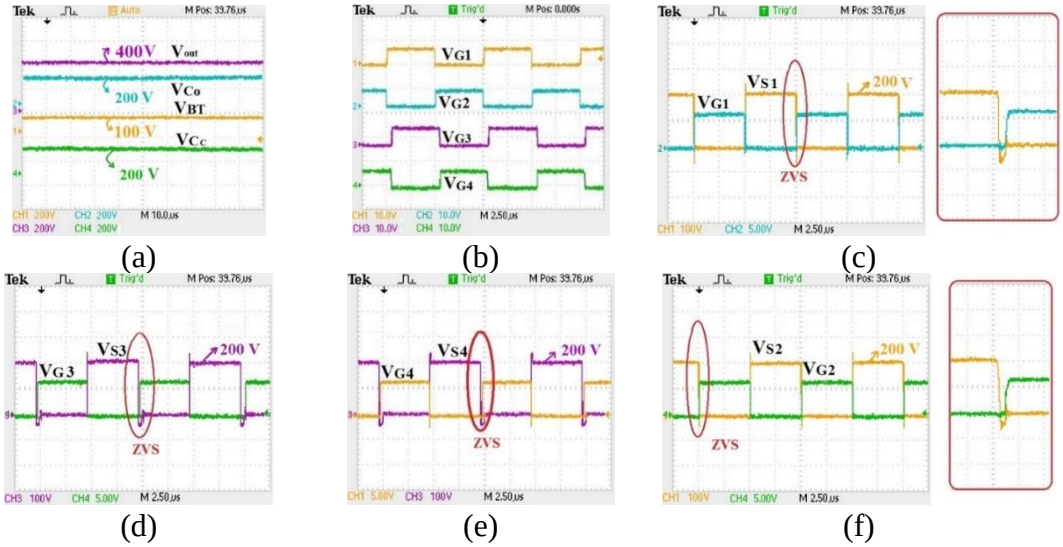


Figure 8.19: Experimental results during scenario I at light load when D=0.5 (V_{BT} = 100 V, V_{out} = 400 V, P_{Out} = 100 W). (a) Battery voltage, output voltage, voltage across capacitors C_{o1} and C_{o2}. (b) Gate-source voltage of switches. (c) gate-source and drain-source voltage of switch S_1. (d) gate-source and drain-source voltage of switch S_3. (e) gate-source and drain-source voltage of switch S_4. (f) gate-source and drain-source voltage of switch S_2.

As expected, the experimental results shown in Figure 8.20 (f) prove that the inductor current i_{LB2} is flat since the voltage of capacitors C_C, C_O, and C_{aux} are equal.

As shown in Figure 8.21, the operation of proposed converter under full-load condition in scenario III is in the line with the theoretical analysis. Figure 8.21 (a) depicts the gate pulses of switches. The phase-shift between the gate pulse of switches S_1 and S_3 is 1us and the duty-cycle is 0.53. Also, the gate-pulse of switches highlights that the adopted technique to reduce the parasitic inductance is effective and there is not any false turn-on or turn-off. The gate pulse and voltage stress across the switches S_1, S_2, and S_3 are shown in Figure 8.21 (b), (c), and (d), respectively. These figures provide evidence that the soft switching at turn-on instant is achieved in scenario III.

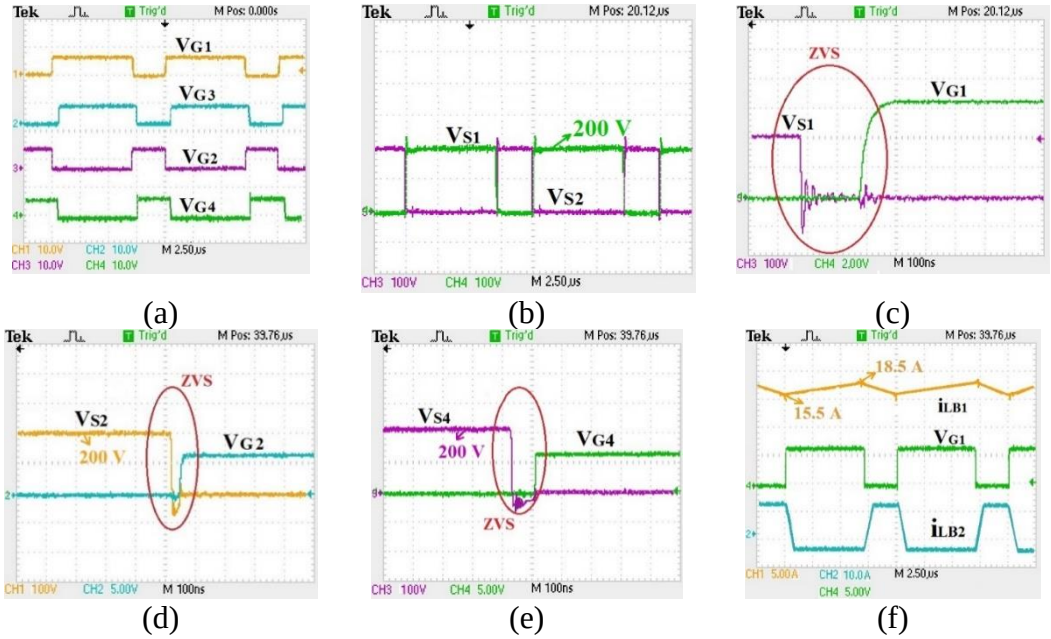
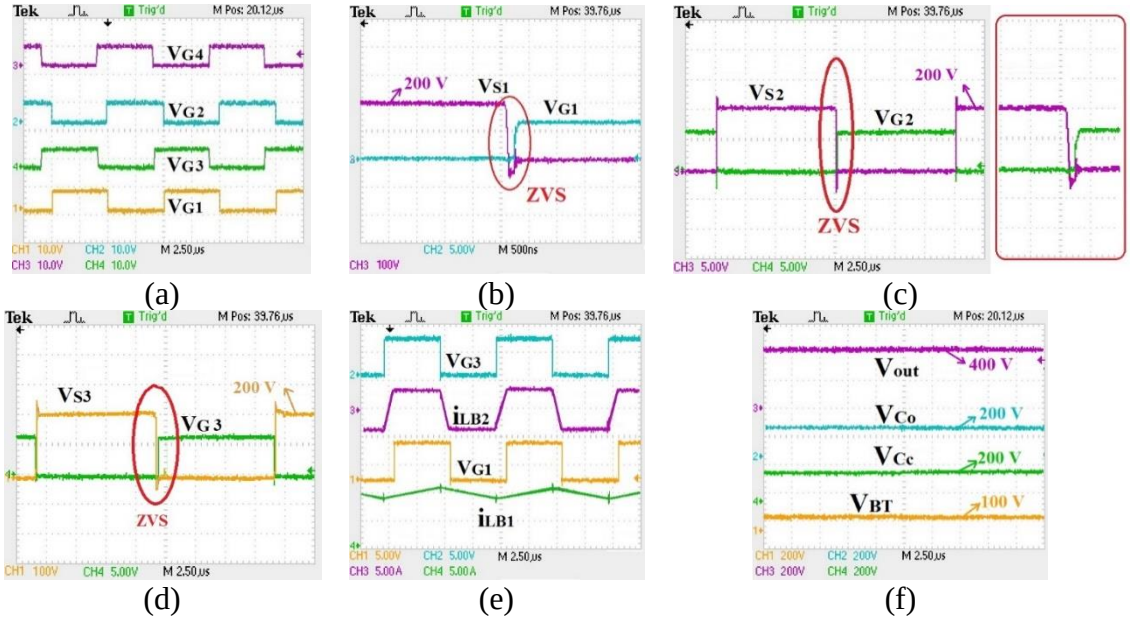


Figure 8.20: Experimental results during scenario I at full-load condition when D=0.72 (V_{BT} = 60 V, V_{out} = 400 V, P_O = 1 kW). (a) Gate-source voltage of switches. (b) drain-source voltage of switches S_1 and S_2 (c) gate-source and drain-source voltage of switch S_1. (d) gate-source and drain-source voltage of switch S_2. (e) gate-source and drain-source voltage of switch S_4. (f) gate-source voltage of switch S_1 and inductor current i_{LB1} and i_{LB1}.

The inductor current i_{LB1} and i_{LB2}, and the gate signal of switch S_1 and S_3 are shown in Figure 8.21(e). There is perfect agreement between the theoretical analyses discussed in the previous section and the experimental results shown in Figure 8.21 (e). The battery voltage V_{BT}, the voltage of output capacitors V_{Co} and V_{Cc}, and output voltage V_{out} are demonstrated in Figure 8.21(f). As predicted by (10), the experimental result proves that the voltage gain is four when duty-cycle is 0.53. The results of converter performance during scenarios II and IV are demonstrated in Figure 8.22. The gate pulse, drain-source voltage of switch S_1 and the inductor current i_{LB1} are depicted in Figure 8.22 (a).



(a) (b) (c)

(d) (e) (f)

Figure 8.21: Experimental results during scenario III at full load when D=0.53 (V_{BT} = 100 V, V_{DC} = 400 V, P_O = 1000 W). (a) Gate pulse of switches. (b) gate-source and drain-source voltage of switch S_1. (c) gate-source and drain-source voltage of switch S_2. (d) gate-source and drain-source voltage of switch S_3. (e) gate-source of switches S_1 and S_3, inductor current i_{LB1} and i_{LB1}. (f) Battery voltage, output voltage, voltage across capacitors C_{o1} and C_{o2}.

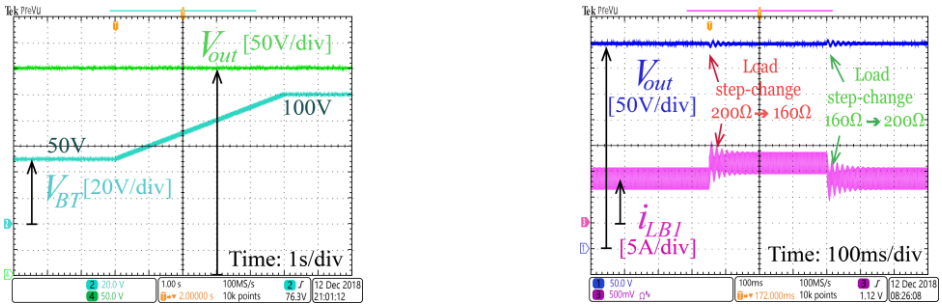
(a) (b)

Figure 8.22: Experimental results during scenario II and IV at full load when D=0.6 (V_{BT} = 80 V, V_{Cc} = 200 V, P_O = 1000 W). (a) Gate-source and drain-source voltage of switches S_1 and inductor current i_{LB1} during scenario II when P_{PV}=1020 W. (b) battery voltage and gate-source voltage of switches S_1 and S_2 during scenario IV.

The generated power of PV array (P_{PV}=1020 W) is more than the power demanded by load (P_{out}=1000 W); so, the battery is charged by the surplus power. Figure 8.22(b) shows the gate voltage of switch S_1 and S_3, and the battery voltage (V_{BT} =60 V) when the PV voltage

is 200 V and the duty cycle is 0.62. The experimental results also clearly substantiate that the control scheme is working properly in all operating scenarios.

Regarding the application of the proposed three-port converter for hybridizing renewable energy sources, the controller performance with wide-range changed battery voltage is experimentally verified. Figure 8.23 (a) shows the output voltage V_{out} when the battery voltage V_{BT} is changed gradually from 50 V to 100 V over dozens of seconds. It can be seen that the output voltage follows the reference voltage of 400 V with wide-range changed battery voltage, implying the wide voltage-gain range from 4 to 8 is achieved. To evaluate the dynamic behavior of the proposed three-port converter, a step-change of load is applied to the proposed circuit. Figure 8.23(b) demonstrates the output voltage and the inductor current i_{LB1} while there is a step change of load between 160 Ω and 200 Ω. It can be concluded that the control technique keeps the output voltage constant with the load step-change.

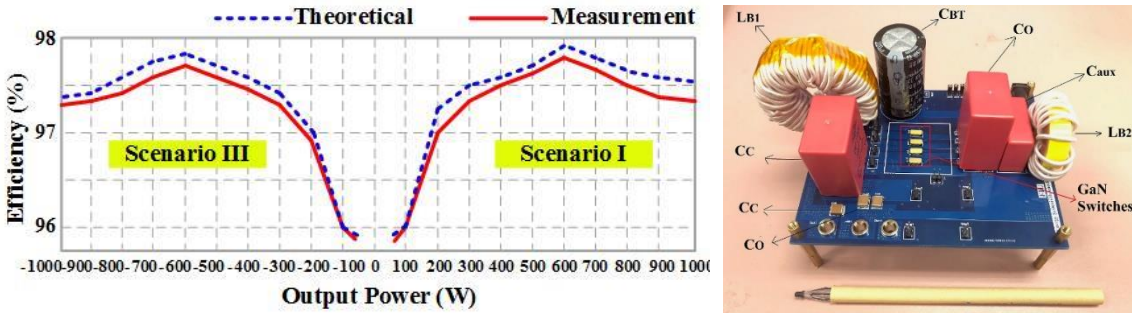


(a) (b)

Figure 8.23: Controller performance verification. (a) Output voltage with wide-range changed battery voltage from 50 V to 100V.(b) Output voltage and inductor current when load step-change between 160 Ω and 200 Ω.

The theoretical and measured efficiency during scenario I and III are depicted in Figure 8.24 (a). The maximum theoretical and experimental efficiency happens at 600 W, which are 97.9% and 97.7%, respectively. Theoretical and experimental efficiency at full load

condition are 97.5% and 97.3%, respectively. The developed prototype is shown in Figure 8.24 (b).



(a) (b)

Figure 8.24: Efficiency curves and prototype of the proposed converter. (a) Calculated and measured efficiency curves. (b) Laboratory prototype of STPTLC.

8.4 Conclusion

In this chapter, a three-port three-level converter for hybridizing of renewable energy sources is introduced which features simple topology, low voltage stress across switches, ZVS performance for wide load variation, and decoupled control of power and voltage. It also benefits the inherent advantages of the conventional ABHB converter in terms of the lower number of components, small size, and weight. The proposed STPTLC has different operation scenarios based on the output power of PV that varies with weather and daytime. The RMS current of inductance and the boundary condition of the phase-shift controller in different operation scenarios are analyzed to find the low-conduction-loss operation mode. A control system comprised of PWM and phase-shift controlled algorithm is proposed, which provides a solution to cope with the wide input voltage variation as the voltage and power are regulated independently. Finally, the performance of proposed STPTLC was verified using a 1 kW, 100 kHz experimental setup built with GaN switches.

Chapter 9 An Integrated Interleaved Ultra High Step-Up DC-DC Converter Using Dual Cross-Coupled Inductors with Built-in Input Current Balancing for Electric Vehicles

9.1 Introduction

An integrated interleaved dc-dc converter with ultra-high voltage gain and reduced voltage stress based on the coupled-inductors and switched-capacitor circuits is proposed in this chapter, which is suitable for interfacing the low-voltage energy sources, such as fuel-cell, with a high-voltage dc bus in electric vehicle applications. Input-parallel connection of the coupled-inductors offers a reduced input current ripple and the current rating of components, as well as automatic input current sharing without a dedicated current sharing controller. A promising power-density improvement technique is given, in which only one magnetic core is utilized to implement two coupled-inductors that can provide the filter functionality as well as transformer behavior. To suppress the voltage ringing resulting from the leakage inductors, the active-clamp configuration is employed that can facilitate the soft-switching performance for all switches in a wide range of output power. A voltage multiplier stage is adopted to not only boost the voltage gain but help alleviate the reverse-recovery problem of diodes. The steady-state performance, theoretical analysis, and a comparison with the state-of-the-art converters are given in this chapter. Finally, experimental results of a 1 kW, 100 kHz prototype are provided to confirm the validity of the proposed concept.

9.2 Proposed Integrated Interleaved Ultra High Step-Up DC-DC Converter with Dual Coupled-Inductors

Hybrid Electric vehicles (HEVs) have received much attention in the past decade due to environmental and economic benefits. Fuel-cell (FC)-powered HEVs are attracting considerable interest as FCs offer high-efficiency performance with the lowest emission, and they are cheap in terms of capital cost compared to other renewable energy sources [1]-[4]. General scheme of the power train of an FC-powered HEV depicted in Figure 9.1, where the voltage levels of FC (about 20-30V) are relatively low compared to that of dc-bus voltage. So, a high step-up dc-dc converter (HSUC) is recognized as being the essential power conversion unit, which is characterized by having high voltage gain, high power-density, high reliability, high efficiency, and low cost [5]-[7]. Small input current ripple is another characteristic that is a key performance indicator in FC-based power systems. In other words, the input current ripple directly impacts the lifetime of FC system [8].

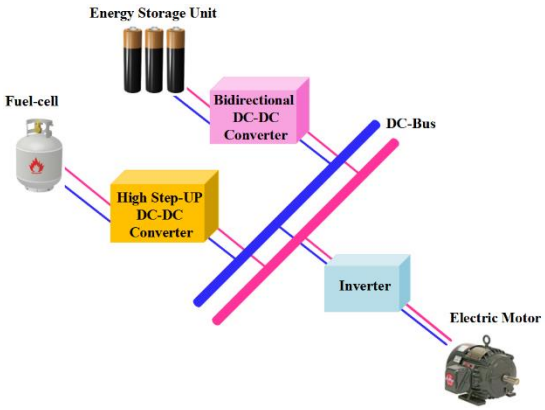


Figure 9.1: General scheme of power train of an HEV based on the fuel cell.

9.2.1 Circuit Configuration

The general layout of the proposed IIUHSC is shown in Figure 9.2 (a), which is derived from the interleaved half-bridge converter. The IIUHSC consists of a current-auto-balance integrated interleaved stage (CABIIS), a ZVS active-clamp switching stage (ACSS), and a voltage multiplier stage (VMS). CABIIS is comprised of the primary windings of two coupled inductors, connected in a way that the automatic current distribution can be realized, and the current stress of semiconductors can be reduced. ACSS paves the way for the soft-switching performance and confining the voltage stress across the switches. The high voltage conversion ratio is achieved by virtue of the VMS, which is composed of series-connection of the secondary windings of coupled inductors. The multiplier capacitors not only help increase the voltage gain but also serve as the dc-blocking capacitor. As a result, the converter operates in continuous conduction mode (CCM). As shown in Figure 9.2(a), in the proposed concept, only one magnetic core is utilized to fulfil the functions of both input filters and coupled inductors. Figure 9.2 (b) demonstrates the equivalent circuit of the proposed converter, where S_1 and S_2 represent the main switches; S_{C1} and S_{C2} denote the clamp switches; C_C is the clamp capacitor; D_{o1} and D_{o2} denote the output diodes; D_{r1} and D_{r2} represent the regenerative diodes; C_{m1} and C_{m2} denote the multiplier capacitors; V_{in}, V_{out}, and R_{out} denote the input voltage, output voltage, and the load, respectively. Also, the coupled inductors are modeled by the ideal transformers, the leakage inductors L_{k1} and L_{k2}, and the magnetizing inductors L_{m1} and L_{m2}. Note the primary inductor L_{1a} with N_{1a} turns is coupled with its secondary inductor L_{2a} with N_{2a} turns. Similarly, the primary inductor L_{1b} with N_{1b} turns is coupled with its secondary inductor

L_{2b} with N_{2b} turns. To simplify the analysis, turns-ratio is defined by $n = N_{2b} / N_{1a} = N_{2a} / N_{1a}$.

9.2.2 Operation Modes

Due to the specific connection of coupled-inductors and dc-blocking capacitor at the secondary side, the IIUHSC operates in CCM; so, the duty cycle should be more than 0.5. The duty cycles (D) of the main switches are identical and there is a phase-shift of 180° between the gate pulses of the main switches. The operation of converter during one switching period T_s can be divided into 16 modes, as illustrated in Figure 9.3. Due to the symmetry of the circuit, only 8 operation modes are analyzed in this section, which are depicted in Figure 9.4 and are explained in the following.

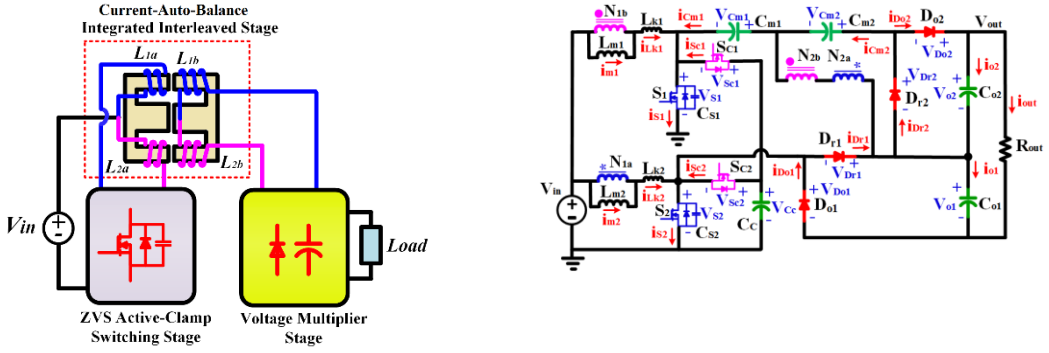


Figure 9.2: Proposed IIUHSC converter. (a) Schematic. (b) Equivalent circuit with magnetic component model.

Mode 1 [$t_0 \sim t_1$]: Prior to t_0, the main switches are ON, and the clamp switches are OFF. All the diodes are reversed-biased. During this mode, the magnetizing and the leakage inductors, L_{m1} and L_{m2}, L_{k1} and L_{k2}, are being charged by the input voltage linearly. As shown in Figure 9. 4(a), the load is being supplied by output capacitors. This mode can be described by

$$i_{Lm1,2}(t) = i_{Lk1,2}(t) = i_{Lm1,2}(t_0) + \frac{V_{in}}{L_{m1,2} + L_{k1,2}}(t - t_0) \quad (9\text{-}1)$$

Mode 2 [$t_1 \sim t_2$]: At t_1, the gate-pulse of S_1 is removed and it turns off, depicted in Figure 9.4(b). Since the parasitic capacitor of switch S_1 controls the voltage variation across the switch, the ZVS performance at turn-off can be achieved. Due to the small capacitance of parasitic capacitor, the voltage of switch S_1 charges linearly and can be expressed as

$$v_{ds1}(t) \cong \frac{i_{Lm1}(t_1)}{C_{s1}}(t - t_1) \quad (9\text{-}2)$$

At the end of this mode, the voltage of the switch reaches to the clamp capacitor voltage V_{Cc}.

Mode 3 [$t_2 \sim t_3$]: This mode starts when the antiparallel diodes of switch S_{C1} starts conducting the current. So, the voltage stress of switch S_1 is clamped to V_{Cc}, shown in Figure 9.4(c). In the meanwhile, the energy of input source is being stored in the magnetizing and leakage inductors.

Mode 4 [$t_3 \sim t_4$]: At the beginning of this mode, the diodes D_{o1} and D_{r2} turn on. In this mode, the energy stored in the magnetizing inductors is transferred to the output capacitor C_{o1}. As illustrated in Figure 9.4(d), the multiplier capacitor C_{m1} is discharged in this mode. The equations describing this mode are given as follows:

$$i_{Lm1}(t) = i_{Lm1}(t_3) + \frac{V_{in} - V_{Cc}}{L_{m1}}(t - t_3) \quad (9\text{-}3)$$

$$i_{Lk1}(t) = i_{Lk1}(t_3) + \frac{V_{o1} - V_{Cm1} - (n+1)V_{Cc}}{nL_{k1}}(t - t_3) \quad (9\text{-}4)$$

$$i_{Lk2}(t) = i_{Lk2}(t_3) - \frac{V_{o1} - V_{Cm1} - (n+1)V_{Cc}}{nL_{k2}}(t - t_3) \quad (9\text{-}5)$$

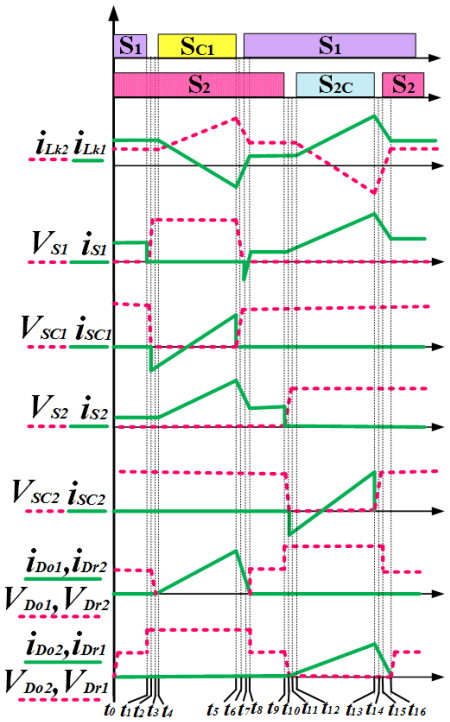


Figure 9.3: Key waveforms of the proposed converter.

Mode 5 [$t_4 \sim t_5$]: At the begging of this mode, the turn-on pulse is applied to the gate of S_{C1}. Therefore, the ZVS performance of S_{C1} is achieved. As shown in Figure 9.4(e), the equivalent circuit of converter in this mode is the same as that of the previous mode.

Mode 6 [$t_5 \sim t_6$]: At $t=t_5$, the clamp switch S_{c1} turns off. Then a resonant circuit composed of the leakage inductor L_{k1} and the parasitic capacitor of switch C_{S1} is formed. Accordingly, the current of L_{k1} changes linearly due to the small capacitance of C_{S1}, and the stored energy of C_{S1} is transferred to the leakage inductor. During this mode, the voltage of the switch S_{c1} increases linearly as well. The equivalent circuit in this mode is shown in Figure 9. (f). The voltage of switch S_1 can be defined by

$$v_{ds1}(t) \cong V_{Cc} - \frac{i_{Lm1}(t_5)}{C_{s1}}(t - t_5) \qquad (9\text{-}6)$$

Mode 7 [$t_6 \sim t_7$]: At t=t_6, the voltage of switch S_1 becomes zero and its antiparallel diode turns on. The current of diodes D_{o1} and D_{r2} decreases linearly, and its slope is controlled by the leakage inductance.

$$i_{Lk1}(t) = i_{Lk1}(t_6) - \frac{V_{o1} - V_{Cm1}}{n^2 L_{k1}}(t - t_6) \tag{9-7}$$

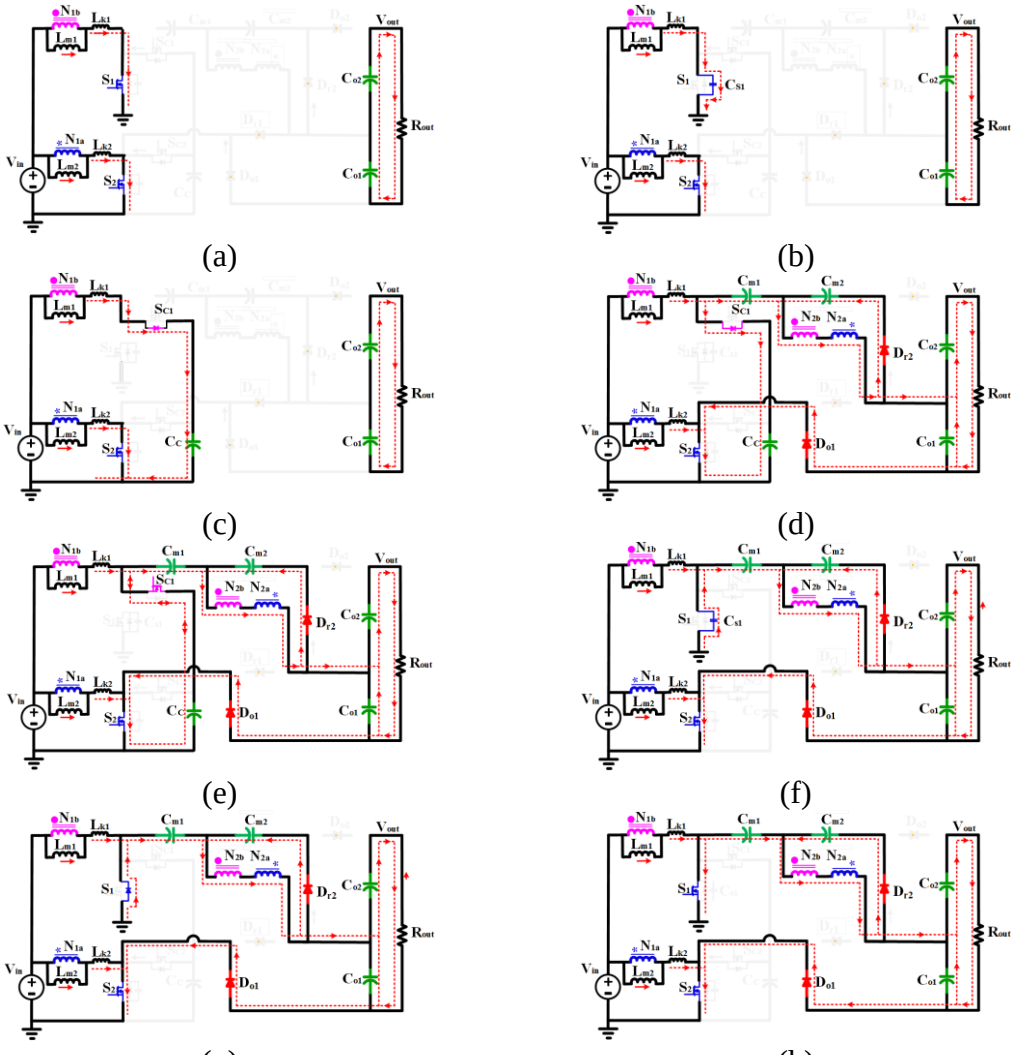


Figure 9.4: Operation modes in one switching period. (a) Mode 1 [$t_0 \sim t_1$]. (b) Mode 2 [$t_1 \sim t_2$]. (c) Mode 3 [$t_2 \sim t_3$]. (d) Mode 4 [$t_3 \sim t_4$]. (e) Mode 5 [$t_4 \sim t_5$]. (f) Mode 6 [$t_5 \sim t_6$]. (g) Mode 7 [$t_6 \sim t_7$]. (h) Mode 8 [$t_7 \sim t_8$].

Mode 8 [$t_7 \sim t_8$]: At the beginning of this mode, the turn-on pulse of switch S_1 is applied while its antiparallel diode is conducting; therefore, the switch S_1 turns ON with ZVS

operation. Moreover, the magnetizing and leakage inductors, L_{m1} and L_{k1}, are being charged by input source. Other components operate in the similar way as in mode 7. At the end of this mode, the diodes D_{o1} and D_{r2} are cut off.

As shown in Figure 9.3, in the remaining operation modes, the circuit performance is similar due to the symmetry of the converter. Indeed, in the CABIIS circuit, the operating principle of switches S_2 and S_{c2} are similar to those of switches S_1 and S_{c1}, and identical commutation process happens between the switches S_2 and S_{C2}. In the VMS, the diodes D_{o2} and D_{r1} conduct the current.

9.3 Steady-State Performance of the Proposed Converter

9.3.1 General Assumptions

In order to simplify the steady-state analysis, the parameters of coupled inductors and switches are considered identical, i.e., $L_{k1} = L_{k2} = L_k$, $L_{m1} = L_{m2} = L_m$, and $C_{S1} = C_{S2} = C_S$. Also, the VMS capacitors as well as the output capacitors are assumed to be identical due to the symmetry of converter, i.e., $C_{m1} = C_{m2} = C_m$ and $C_{o1} = C_{o2} = C_o$. Furthermore, it is estimated that the voltage of all the capacitors except the parasitic capacitance of switches is constant during one switching period since their capacitance is relatively high.

9.3.2 Voltage Gain

Similar to the conventional boost converter, the voltage of clamp capacitor can be obtained by applying the volt-second balance to the magnetizing inductors as follows:

$$V_{Cc} = \frac{V_{in}}{1 - D} \tag{9-8}$$

In (8), D denotes the duty-cycle of the main switches S_1 and S_2. From (4), the raising rate of the output diode current is defined by

$$k_{rise} = \frac{di_{Do1}}{dt} = \frac{V_{o1} - V_{Cm1} - (n+1)V_{Cc}}{4n^2 L_k} \tag{9-9}$$

From (7), the falling rate of the output diode current i_{Do1} can be determined by

$$k_{fall} = \frac{di_{Do1}}{dt} = \frac{-V_{o1} + V_{Cm1}}{4n^2 L_k} \tag{9-10}$$

From (4) and (10), the peak current and the fall time of the output diode current i_{Do1} can be calculated as follows:

$$I_{Do1,Peak} = \frac{V_{Cm1} + (n+1)V_{Cc} - V_{o1}}{4n^2 L_k}(1-D)T_s \tag{9-11}$$

$$t_{fall} = \frac{I_{Do1,Peak}}{-k_{fall}} = \frac{V_{Cm1} + (n+1)V_{Cc} - V_{o1}}{V_{o1} - V_{Cm1}}(1-D)T_s \tag{9-12}$$

Where T_s denotes the switching period. By applying Kirchhoff's Voltage Law (KVL) to the converter when switches S_1 and S_{c2} are ON and the diodes D_{o2} and D_{r1} are conducting the current (Mode 13), the voltage of multiplier capacitor C_{m1} can be written as

$$V_{Cm1} = (n+1)V_{Cc} \tag{9-13}$$

In steady state, the average current of a capacitor is zero; so, the average current of output diode D_{o1} is equal to the average output current, which can be written as

$$I_{out} = I_{Do1,avg} = \frac{V_{out}}{R_{out}} = \frac{1}{2T_s} I_{Do1,Peak}[(1-D)T_s + t_{fall}] \tag{9-14}$$

Considering (8)-(14), the voltage gain of the proposed converter can be determined by

$$M = \frac{V_{out}}{V_{in}} = \frac{4(2n+1)}{(1-D) + \sqrt{(1-D)^2 + 6k}} \tag{9-15}$$

Where $k = 8\,n^2\,(2n+1)\,L_k / (n+1)\,T_s\,R_{out}$. Figure 9.5 demonstrates the relationship between the voltage gain and the duty-cycle for different values of leakage inductance L_k, which

obviously indicates that a high voltage gain is achieved even with small duty cycle. Moreover, the voltage gain reduces as the leakage inductance increases.

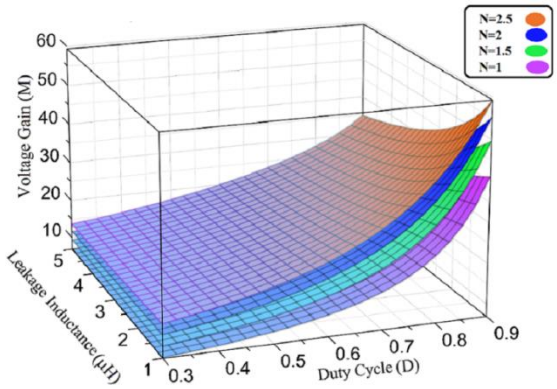


Figure 9.5: Voltage gain of the proposed converter as a function of duty cycle, turns-ratio, and leakage inductance.

9.3.3 Automatic Input Current Sharing

In this section, the effects of mismatches in the individual circuit parameters, including the magnetizing inductance and duty cycle, on the automatic current sharing capability of the converter is investigated. These mismatches happen in the practical situation. It is noteworthy to mention that the two coupled inductors are decoupled magnetically due to the short magnetic reluctance of the center leg without air gap. So, only mismatch between N_{1a}/N_{2a} and N_{1b}/N_{2b} are considered. The average magnetizing current can be written as

$$I_{Lmi,avg} = \frac{I_{in}}{2} = I_{out}\frac{2n_i + 1}{(1 - D_i)} \tag{9-16}$$

For the sake of simplicity, the parameter is defined as $\Delta I_{Lm,avg} / I_{in} = (I_{Lm1,avg} - I_{Lm2,avg}) / I_{Lm2,avg} + I_{Lm1,avg})$. From (4), the ratio of average magnetizing current $I_{Lm1,pk}$ and $I_{Lm2,pk}$ can be defined by

$$\frac{I_{Lm2,avg}}{I_{Lm2,avg}} = \frac{(1 - D_1)(2n_2 + 1)}{(1 - D_2)(2n_1 + 1)} \tag{9-17}$$

Assuming the parameters of first branch are constant, defined as D_2=D and L_{m1}=L_m, and there are variations in the parameters of first branch; defining D_1=D + ΔD and L_{m1} = L_m+ ΔL_m. Then, to simplify the analysis a function is defined as follows:

$$f(D,L) = \frac{(2n+1)}{(1-D)} \tag{9-18}$$

By applying the first order approximation, we have

$$f(D+\Delta D, L_m+\Delta L_m) \approx f(D,L_m) + \frac{\partial f}{\partial D}\Delta D + \frac{\partial f}{\partial L}\Delta L_m \tag{9-19}$$

Combining (18) and (19) and substituting into (17), the parameter $\Delta I_{Lm,pk}$ / I_{in} can be expressed as

$$\frac{\Delta I_{Lm,avg}}{I_{in}} = 0.5\frac{\Delta D}{1-D} + \frac{n}{2n+1}\frac{\Delta L_m}{L_m} \tag{9-20}$$

The similar analysis can be applied to the maximum magnetizing current, which is defined by

$$I_{Lmi,pk} = V_{out}[\frac{2n+1}{R_{out}(1-D_i)} + \frac{T_s D_i(1-D_i)}{4L_{mi}(2n+1)}] \tag{9-21}$$

To simplify analysis, the parameter is defined as $\Delta I_{Lm,pk}$ / I_{in}= ($I_{Lm1,pk}$ - $I_{Lm2,pk}$) / ($I_{Lm2,pk}$ + $I_{Lm1,pk}$). From (4), the maximum magnetizing current $I_{Lm1,pk}$ and $I_{Lm2,pk}$ can be defined by (22). Then, combining (21) and (22) and substituting into (20), the parameter $\Delta I_{Lm,pk}$ / I_{in} can be expressed as (23).

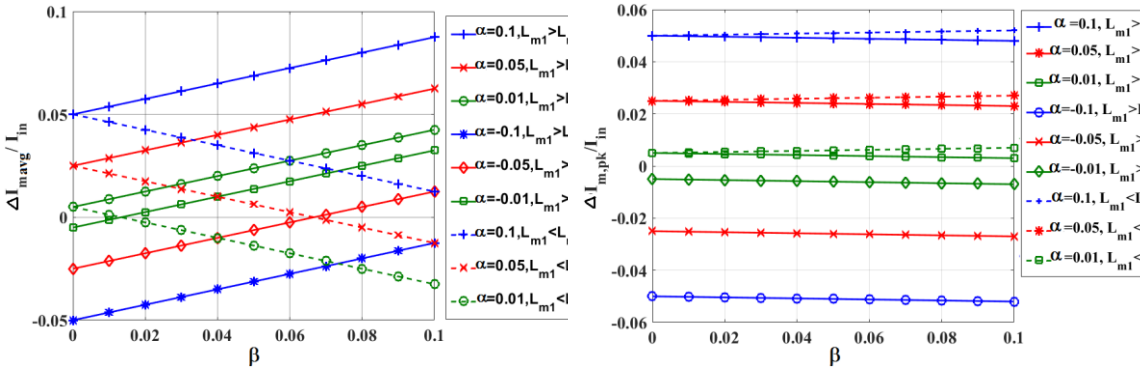
From (17), it is obvious that the magnetizing currents of two branches are equal ($\Delta I_{Lm,pk}$ = 0) if the parameters of two branches are identical, i.e., ΔD = ΔL_m = 0. Figure 9.6 (a) and (b) show the effect of the mismatches in the parameters of coupled inductors on the current sharing characteristics, in which α = ΔD / (1-D), β= ΔL / L, n= 1.5, D = 0.65, R_o = 160, T_s

= 10 μs, and L = 50 μH. It can be seen that the mismatches in the duty cycle values as well as the parameters of coupled inductors has a negligible impact on the sharing the input current between two phases.

$$\frac{I_{Lm2,pk}}{I_{Lm2,pk}} = \frac{L_{m2}(1-D_2)}{L_{m1}(1-D_1)} \frac{4L_{m1}(2n+1)^2 + R_{out}T_sD_1(1-D_1)^2}{4L_{m2}(2n+1)^2 + R_{out}T_sD_2(1-D_2)^2} \tag{9-22}$$

$$\frac{\Delta I_{Lm,pk}}{I_{in}} = \frac{4L_m(2n+1)^2 + R_oT_s(1-2D)(1-D)^2}{8L_m(2n+1)^2 + 2R_oT_sD(1-D)^2} \frac{\Delta D}{1-D} + \frac{R_oT_sD(1-D)^2}{8L_m(2n+1)^2 + 2R_oT_sD(1-D)^2} \frac{\Delta L}{L} \tag{9-23}$$

In Figure 9.6(a), the difference between the average of magnetizing currents is depicted, which clearly indicates that the current can be equally divided even with some variations in the circuit parameters. Also, the maximum magnetizing currents can be approximately equal even with presence of mismatch in the circuit parameters, as illustrated in Figure 9.6(b). From the aforementioned analysis, the current sharing characteristics of the converter is realized even with the presence of the mismatches in the different parameters of circuit resulting from the driver cell as well as fabrication of coupled inductors.



(b) (b)

Figure 9.6: Automatic current sharing performance. (a) Effect of mismatches in the parameters on the average current of magnetizing inductors. (b) Effect of mismatches in the parameters on the maximum current of magnetizing inductors.

9.3.4 Magnetic Integration

In this section, implementing the advanced magnetic integration technology as a means to improve the power density of the proposed converter is discussed. The coupled inductors are wound around outer legs, which provides the condition to decouple them magnetically as the center leg enables a low permeable magnetic path. The magnetic and electrical equivalent circuit of the coupled inductors can be established according to Figure 9. 7 (a) and (b), respectively. To simplify the analysis, it is assumed that the reluctance values of the outer legs are equal. The maximum value of the flux density can be calculated according to (24).

$$\phi_{Max} = \phi_{dc} + \left|\frac{\phi_{ac}}{2}\right| \tag{9-24}$$

The flux values flowing through outer and center legs can be expressed as

$$\phi_1 = \frac{(N_P I_{P1} + N_S I_{S1} + \alpha(N_P I_{P2} + N_S I_{S2}))}{(1+\alpha)R_o} \tag{9-25}$$

$$\phi_2 = \frac{(N_P I_{P2} + N_S I_{S2} + \alpha(N_P I_{P1} + N_S I_{S1}))}{(1+\alpha)R_o} \tag{9-26}$$

$$\phi_C = \frac{(1-\alpha)(N_P I_{P1} + N_S I_{S1} - (N_P I_{P2} + N_S I_{S2}))}{(1+\alpha)R_o} \tag{9-27}$$

Where $\alpha = R_C / (R_C + R_O)$, and I_{P1} and I_{S1} represent the current flowing through the primary and secondary windings of the inductor L_{1a} and L_{2a}, respectively. Also, I_{P2} and I_{S2} represent the current flowing through the primary and secondary windings of the inductor L_{1b} and L_{2b}, respectively. According to the analysis given in the previous sections, the average value of the current flowing through different legs can be determined by

$$I_{P1,avg} = I_{P2,avg} = 0.5 I_{in} \tag{9-28}$$

$$I_{S1,avg} = I_{S2,avg} = 0 \tag{9-29}$$

From Figure 9.7 (b), the dc analysis of the fluxes in the outer and center legs can be calculated by

$$\phi_{1,dc} = \frac{N_P I_{in}}{2R_o} = \frac{(1+\alpha)L_P I_{in}}{2N_P} \tag{9-30}$$

$$\phi_{2,dc} = \frac{N_P I_{in}}{2R_o} = \frac{(1+\alpha)L_P I_{in}}{2N_P} \tag{9-31}$$

$$\phi_{C,dc} = \phi_{1,dc} - \phi_{2,dc} = 0 \tag{9-32}$$

Where $L_{P1} = L_{P2} = L_P = N_P^2 / ((1+\alpha) R_O)$.

The ac-component of the flux in different mode can be obtained from Figure 9.7(c). In mode 1, the following equations can be written as follows:

$$\Delta\phi_{1,ac} = \Delta\phi_{2,ac} = \frac{DT_S V_{in}}{N_P} = \frac{(1+\alpha)L_m I_{in}}{2} \tag{9-33}$$

$$\Delta\phi_{C,ac} = \Delta\phi_{1,ac} - \Delta\phi_{2,ac} = 0 \tag{9-34}$$

Similarly, the ac-component of the flux in mode 2 can be expressed by

$$\Delta\phi_{1,ac} = \frac{(1-D)T_S(V_{in} - V_{Cc})}{N_P} = \frac{-DT_S V_{in}}{N_P} \tag{9-35}$$

$$\Delta\phi_{2,ac} = \frac{(1-D)T_S V_{in}}{N_P} \tag{9-36}$$

$$\Delta\phi_{C,ac} = \Delta\phi_{1,ac} - \Delta\phi_{2,ac} = \frac{-T_S V_{in}}{N_P} \tag{9-37}$$

Due to the symmetry of the circuit, the flux variation in other operation modes can be calculated similarly. Similar to Mode 2, the ac-component of the flux in the center leg is zero in mode 3.

From (24)-(37), the maximum value of the flux in different legs can be determined by

$$\phi_{1,Max} = \frac{(1+\alpha)L_m I_{in}}{2N_P} + \frac{DT_S V_{in}}{2N_P} \quad (9\text{-}38)$$

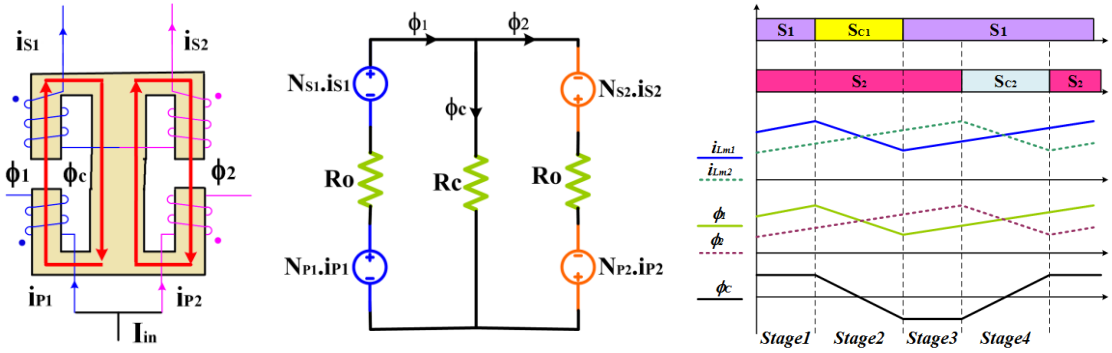
$$\phi_{2,Max} = \frac{(1+\alpha)L_m I_{in}}{2N_P} + \frac{DT_S V_{in}}{2N_P} \quad (9\text{-}39)$$

$$\phi_{C,Max} = \frac{T_S V_{in}}{2N_P} \quad (9\text{-}40)$$

The cross-section area of the core is essentially defined by the maximum the flux density so that there is no core saturation occurs when flux density reaches its peak value. According to (24) and (32), it can be concluded that there is no need to adopt an air gap in the center leg as the dc-component of the excited flux will cancel in the center leg, leading to less maximum the flux density; and consequently, lower core loss. From (34), with reduction of AC flux in the center leg, the proposed integrated coupled inductors have a lower core loss in the center leg than do conventional magnetic.

9.3.5 Soft-Switching Characteristics

As described in the section B, the ZVS performance at turn-on and turn-off is an inherent merit of the proposed converter which is enable by the energy stored in the magnetizing inductance. Regarding ZVS performance of the main switches at turn-on, as depicted in



(a) (b) (c)

Figure 9.7: The flux flow path, the electrical equivalent circuit, and flux and current waveforms during different operation modes. (a) The flux flow path. (b) the electrical equivalent circuit of the coupled-inductors. (c) flux and current waveforms during different operation modes.

Figure 9.4(c) and (g), the parasitic capacitance of the switch must be completely discharged before applying the gate pulse to the switch. In other words, the following condition should be met:

$$\frac{1}{2}L_{ki}I_{in}^2 \geq \frac{1}{2}C_{Si}V_{Si}^2 \text{ for i=1,2} \tag{9-41}$$

It is assumed the converter works in ideal lossless condition for simplification purposes. Now, from (16), the ZVS condition can be determined by

$$L_{ki} \geq \frac{C_{Si}}{(4n+2)}\frac{V_{out}^2}{I_{in}^2} \; for \; i = 1,2 \tag{9-42}$$

Figure 9. 8 shows the leakage inductance L_k versus input current I_{in} and the parasitic capacitance of switch C_s. It can be seen that if the parasitic capacitance of switch decreases, lower leakage inductance is required to realize the soft-switching performance in light load. Because of low parasitic capacitance, (42) implies that the GaN switches can offer soft-switching performance with smaller leakage inductance, leading to higher efficiency. From Figure 9.8, it can be concluded that to extend the soft-switching region, higher leakage inductance should be used. Nevertheless, it has to be taken into account, that increasing the leakage inductance will decrease the voltage gain, as shown in Figure 9.5.

9.3.6 Voltage and Current Stress of Semiconductors

Due to the active clamp circuit, the voltage stress of switches is confined to the clamp capacitor voltage.

$$V_{s1,max} = V_{sc1,max} = V_{s2,max} = V_{s2c,max} = \frac{V_{out}}{4n+2} \tag{9-43}$$

Equation (16) reveals that the voltage stress of switches is much lower than the output voltage, decreasing with increase in turns ratio. Thus, to limit the voltage stress of switches,

a proper n can be selected. As a result, a switch with small rated voltage as well as small on-resistance can be employed. The voltage stress of diodes can be achieved from (9-44).

$$V_{Do1} = V_{Do2} = V_{Dr1} = V_{Dr2} = \frac{V_{out}}{2} \tag{9-44}$$

The peak current of main switches can be obtained as follows:

$$I_{S1,peak} = 0.5I_{in,avg} + 2nI_{Dr1,peak} + I_{Dr1,peak} \tag{9-45}$$

$$I_{S2,peak} = 0.5I_{in,avg} + 2nI_{Do1,peak} + I_{Do1,peak} \tag{9-46}$$

Under the steady-state condition, the average current of diodes equals to the output current due to the capacitor current-second balance.

$$I_{Dr1,peak} = I_{Dr2,peak} = I_{Do1,peak} = I_{Do2,peak} = \frac{2I_{out}}{1-D} \tag{9-47}$$

By substituting (47) into (45) and (46), the peak current of main switches can be expressed as

$$I_{S1,peak} = I_{S2,peak} = 3(2n+1)I_{out}/(1-D) \tag{9-48}$$

The peak current of clamp switches can be derived from

$$I_{Sc1,peak} = I_{Sc2,peak} = 0.5I_{in} = (2n+1)I_{out}/(1-D) \tag{9-49}$$

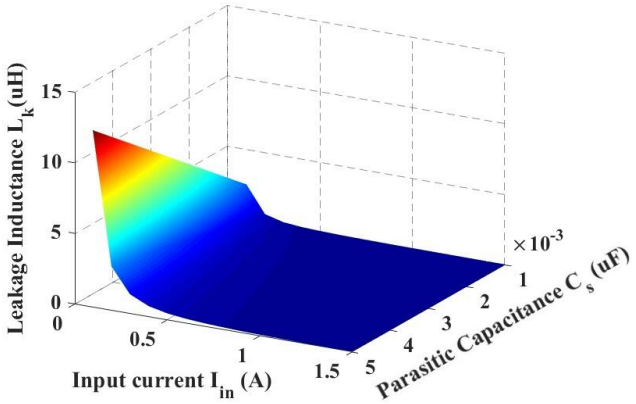


Figure 9.8: ZVS condition for the proposed converter as a function of input current (I_{in}) and parasitic capacitance (Cs) when n=1.5 and V_{out}=600 V.

9.4 Comparison of The Proposed Converter and Other HSUCs

In order to investigate the features of the proposed converter in comparison with some of the well-known nonisolated interleaved high step-up converters, the key characteristics of converters, including voltage gain, voltage stress of semiconductors, and number of passive and active components, are summarized in Table 9.1.

A comparison of the voltage gain of the proposed converter with other HSUCs for different values of the duty-cycle are given in Figure 9.9 (a)-(c). It can be seen that the proposed converter offers the desired voltage gain without working under extreme duty-cycle values. Besides, as depicted in Figure 9.9 (d), the proposed converter offers lowest voltage stress across the semiconductors, therefore, switches with lower rated-voltage and smaller on-resistance can be adopted, resulting in improved efficiency and cost.

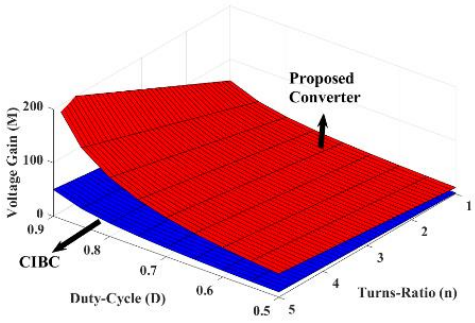
Also, as indicated in Table 9.1, the voltage stress of diodes for the proposed topology is half of the output voltage, implying that the diodes with smaller voltage drop can be used bringing about lower conduction loss. Due to use of active-clamp circuit, the number of power switches is the same in the proposed converter, converter [21], and converter [29], and CIBC. Even though the converter [24] has the least number of active switches, it suffers from the hard-switching performance that deteriorates the efficiency. Moreover, the total number of semiconductors for the proposed converter is the same as the converter introduced in [24]. It should be noted that the higher number of active switches does not increase the complexity of the control circuit because the similar asymmetrical PWM is used in the proposed converter. Due to using three-level structure in the output stage, the

TABLE 9.1: PERFORMANCE COMPARISON OF THE PROPOSED CONVERTER AND THE CONVERTER CITED IN [21], [24], [28], AND [29].

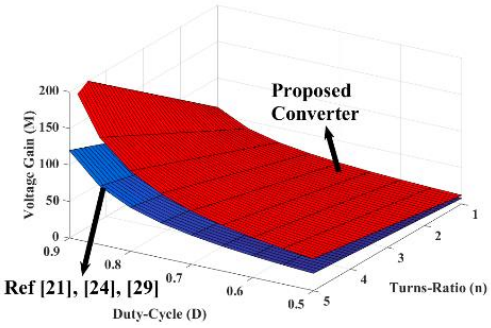
Item		**CIBC**	**Ref. [21]**	**Ref. [24]**	**Ref. [28]**	**Ref. [29]**	**Proposed converter**
Voltage gain		$\frac{n}{1-D}$	$\frac{2(n+1)}{1-D}$	$\frac{2(n+1)}{1-D}$	$\frac{2(n+2)}{1-D}$	$\frac{2(n+1)}{1-D}$	$\frac{2(2n+1)}{1-D}$
Voltage stress of switches		$\frac{V_{out}}{n}$	$\frac{V_{out}}{2(n+1)}$	$\frac{V_{out}}{2(n+1)}$	$\frac{(1+Dn)V_{out}}{2(n+1)}$	$\frac{V_{out}}{2(n+1)}$	$\frac{V_{out}}{2(2n+1)}$
Voltage stress of diodes		V_{out}	$\frac{2n+1}{2(n+1)}V_{out}$	$\frac{2n+1}{2(n+1)}V_{out}$	$\frac{(n+1)V_{out}}{n+2}$	$\frac{2n+1}{2(n+1)}V_{out}$	$\frac{V_{out}}{2}$
No. of Components	**Switch**	4	4	2	3	4	4
	Diode	4	2	6	6	6	4
	Cap.	2	3	5	4	9	5
	Cores	3	2	3	3	2	1
Soft switching		Yes	Yes	No	Yes	Yes	Yes
Automatic current sharing		No	No	No	No	Yes	Yes
Output voltage ripple		Large	Large	Large	Large	Large	Small

voltage ripple of the output capacitors in the proposed converter is lower than that of other converters.

As the magnetic cores occupy most volume of the converter, reducing the number of cores remarkably shrinks the size of the converter. According to [30], the stored energy and total apparent power gives a rough estimate for the size of the inductor and transformer, respectively. A comparison of size of the magnetic components is carried out, which evaluates the converters by comparing the total apparent power of coupled inductors. The converters have been designed and simulated under same specifications, as follows: P_{out}=1000 W, V_{in}= 30 V, V_{out}= 600 V, f_s = 100 kHz, and ΔI_{in}= 10 %. Table 9.2 presents the stored energy and total apparent power for most recent high step-up converters. The total apparent power of coupled inductors is ample support for this claim that the magnetic volume of proposed converter is less than that of the converter introduced in [21], [24], [28], and [29].



(a)



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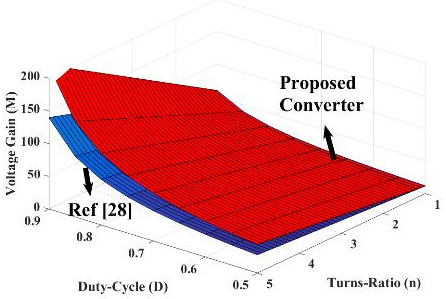
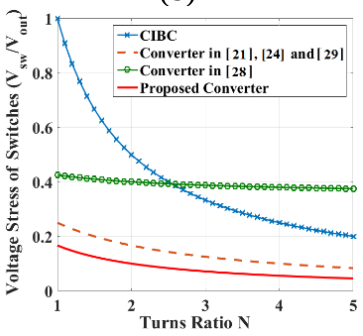




(c) (d)

Figure 9.9: Comparison of the voltage gain and voltage stress of active switches. (a) proposed converter versus CIBC. (b) proposed converter versus converter in [21], [24], and [29]. (c) proposed converter versus converter in [28]. (d) voltage stress of active switches.

TABLE 9.2: COMPARISON OF MAGNETIC COMPONENTS SIZE BETWEEN THE PROPOSED CONVERTER AND OTHER CONVERTERS. (P_{OUT}=1000 W, V_{IN}= 30 V, V_{OUT}= 600 V, F_S = 100 KHZ, AND ΔI_{IN}= 10 %)).

Magnetic Item			Topology					
			CIBC	Converter [21]	Converter [24]	Converter [28]	Converter [29]	Proposed Converter
Input Filter inductors	Inductance L		2×100 µH	-	2×100 µH	-	-	-
	Max. current I_{max}		17.7 A	-	17.7 A	-	-	-
	$\sum LI^2$(pu)		1	-	1	-	-	-
Transformer	Turn-ratio n		6.6	2.3	2.3	1.3	2.3	1.2
	Primary	V_{rms}	48	2× 34	40	2× 32	2× 35	2× 35
		I_{rms}	23.8	2× 30.2	29.2	2× 29.2	2× 29.3	2× 24.9
	Secondary	V_{rms}	440	2× 120	170	2× 110	2× 142	2× 57
		I_{rms}	2.7	2× 4.5	4.1	2× 4.1	2× 2.7	2× 7.6
	Tertiary	V_{rms}	-	-	170	2× 40	2× 142	-
		I_{rms}	-	-	4.1	2× 2.6	2×2.7	-
	$\sum VA$(pu)		2330.4 (1 pu)	3133.6 (1.34 pu)	2562 (1.10 pu)	2978.8 (1.28 pu)	3584.6 (1.54 pu)	2609.4 (1.11 pu)

TABLE 9.3: COMPARISON OF SIZE OF CAPACITORS BETWEEN THE PROPOSED CONVERTER AND OTHER CONVERTERS. (P_{OUT}=1000 W, V_{IN}= 30 V, V_{OUT}= 600 V, F_S = 100 KHZ, AND ΔV= 10 %)).

Item		Topology					
		CIBC	Converter [21]	Converter [24]	Converter [28]	Converter [29]	Proposed Converter
Output Capacitors	Capacitance	22 µF	22 µF	22 µF	2 × 10 µF	22 µF	2 × 10 µF
	Max. voltage V_{max}	600 V	600 V	600 V	300 V	600 V	300 V
	$\sum CV^2$(J)	7.9	7.9	7.9	1.8	7.9	1.8
Clamp Capacitors	Capacitance	10 µF	10 µF	2 × 10 µF	2 × 10 µF	2 × 10 µF	10 µF
	Max. voltage V_{max}	100 V	100 V	100 V	100 - 200 V	100 V	100 V
	$\sum CV^2$(J)	0.1	0.1	0.2	0.5	0.1	0.1
Switched Capacitors	Capacitance	-	10 µF	2 × 10 µF	-	2 × 10 µF	10 µF
	Max. voltage V_{max}	-	300 V	300 V	-	300 V	220 V
	$\sum CV^2$(pu)	-	0.9	1.8	-	1.8	0.484
Resonant Capacitors	Capacitance	-	-	-	-	2 × 0.1 µF	-
	Max. voltage V_{max}	-	-	-	-	100 V	-
	$\sum CV^2$(pu)	-	-	-	-	0.002	-
Total energy volume of capacitors (p.u.)		0.81	0.9	1	0.23	0.9	0.24

Compared to the converter introduced in [24], [28], and [29], less magnetic cores are utilized in the proposed converter due to applying the integrated magnetic technology, which advances the power density.

Now, a comparison of the size of capacitors is performed between the proposed converter and other recent high step-up converters. The energy volume of capacitors can give an insight into the size of capacitors [30]. So, the energy volume of capacitors for different converters are calculated and presented in Table 9.3.

9.5 Design Considerations

9.5.1 Coupled Inductors Design

1) **Turns-Ratio**

As mentioned before, the converter is working in CCM and the duty cycle of main switches should be higher than 0.5. From (15), along with ignoring the leakage inductance, the turns-ratio can be calculated from

$$n < \frac{1}{8}\frac{V_{out}}{V_{in}} - 0.5 \tag{9-50}$$

2) **Magnetizing Inductance**

Limiting the input current ripple, the magnetizing inductors operate similar to boost inductor in the conventional boost converter. So, the value of the magnetizing inductors can be determined by

$$L_{m1} = L_{m2} = \frac{2V_{in}DT_s}{kI_{in}} = \frac{D(1-D)V_{in}T_s}{k(2n+1)I_{out}} \tag{9-51}$$

Where k is the current ripple on magnetizing inductor. To ensure that the input current ripple is 15%, the minimum magnetizing inductance can be calculated by

$$L_{m1} = L_{m2} > \frac{5D(1-D)V_{in}T_s}{3(2n+1)I_{out}} \tag{9-52}$$

3) **Leakage Inductance**

According (10), the leakage inductance plays an important role in soft switching performance of semiconductors as well as the voltage gain and the falling rate of the output diodes current. To extend the ZVS range of switches and restrain the slope of diodes current in the proposed converter, higher leakage inductance is required, whereas, the voltage gain decreases. Although increasing the leakage inductance widens the ZVS region and restrains the slope of diodes current, the voltage gain decreases.

9.5.2 Capacitors Design

Based on the assumption made in the previous subsection, the capacitors should be designed so large that they operate like a voltage source during one switching period. So, the capacitors can be chosen as

$$C_{m1} = C_{m2} > \frac{I_{out}T_s}{\Delta V_m} \tag{9-53}$$

$$C_{o1} > \frac{(1-D)V_{out}T_s}{R_{out}\Delta V_{out}} \tag{9-54}$$

$$C_{o2} > \frac{DV_{out}T_s}{R_{out}\Delta V_{out}} \tag{9-55}$$

$$C_C > \frac{(2n+1)I_{out}T_s}{4\Delta V_{out}} \tag{9-56}$$

9.6 Efficiency Analysis

There are totally five major losses in the dc-dc converter: switching loss, switches conduction loss, diodes conduction loss, capacitors conduction loss, and inductor conduction loss. The switching loss can be ignored in the proposed converter due to the

ZVS performance of switches and ZCS operation of diodes. The switches conduction loss can be calculated by

$$P_S = R_{DS(on)} I_{RMS,S}^2 \tag{9-57}$$

Where $R_{DS(on)}$ is the on-resistance of switch. To simplify the current analysis, the leakage inductance is assumed to be zero. The RMS current of switches, $I_{RMS,S}$, can be obtained from

$$I_{RMS,S1} = I_{RMS,S2} = \frac{(2n+1)I_{out}}{(1-D)} \sqrt{\frac{10-7D}{3}} \tag{9-58}$$

$$I_{RMS,Sc1} = I_{RMS,Sc2} = \frac{(2n+1)I_{out}}{(1-D)} \sqrt{\frac{(1-D)}{3}} \tag{9-59}$$

The diode conduction loss can be determined by using the diode equivalent model of the forward voltage drop V_F in series with resistance R_D, which can be calculated from

$$P_D = R_D I_{RMS,D}^2 + V_F I_{D,avg} \tag{9-60}$$

Where $I_{RMS,D}$ and $I_{D,avg}$ are the RMS and average current of diodes, which can be derived from

$$I_{RMS,D} = \frac{2I_{out}}{\sqrt{3(1-D)}} \tag{9-61}$$

$$I_{D,avg} = I_{out} \tag{9-62}$$

The conduction loss due to equivalent series resistance (ESR) of capacitors can be derived by

$$P_C = R_{ESR,C} I_{RMS,C}^2 \tag{9-63}$$

Where $I_{RMS,C}$ is the RMS current of capacitors and can be derived by

$$I_{RMS,Co1} = I_{RMS,Co2} = I_{out}\sqrt{\frac{4+3D(1-D)}{3(1-D)}} \tag{9-64}$$

$$I_{RMS,Cm1} = I_{RMS,Cm2} = I_{out}\sqrt{\frac{8}{3(1-D)}} \tag{9-65}$$

$$I_{RMS,Cc} = \frac{(2n+1)I_{out}}{(1-D)}\sqrt{\frac{2(1-D)}{3}} \tag{9-66}$$

The conduction loss due to ESR of inductors can be derived by

$$P_L = (R_{ESR,p})I_{RMS,Lk}^2 + 2n(R_{ESR,s})I_{RMS,D}^2 \tag{9-67}$$

Where $R_{ESR,p}$ and $R_{ESR,s}$ are the total ESR of primary and secondary windings, respectively. RMS current of leakage inductance can be calculated by

$$I_{RMS,Lk} = \frac{(2n+1)I_{out}}{1-D}\sqrt{1+\frac{8nD}{2n+1}+\frac{16n^2(1-D^3+(1-D)^3)}{3(2n+1)^2(1-D)}} \tag{9-68}$$

The total loss in the coupled inductors can be calculated by

$$P_{L,tot} = P_L + P_{Core} \tag{9-69}$$

Where P_{Core} can be obtained from the datasheet given by the manufacturer. The efficiency of the proposed converter can be obtained from

$$\eta = \frac{P_{out}}{P_{out} + P_S + P_D + P_C + P_{L,tot}} \tag{9-70}$$

Figure 9.10 shows the efficiency of the proposed converter versus duty cycle at different values of output power, where $R_{ESR,P}$ and $R_{ESR,S}$ represent the parasitic resistance of primary and secondary winding the coupled-inductors, respectively, $R_{DS(on)}$ represents the on-resistance of the switches, R_D represent the parasitic resistance of the diodes, $R_{ESR,C}$ represent the parasitic resistance of the capacitors, and V_F is the forward voltage drop of

the diodes.

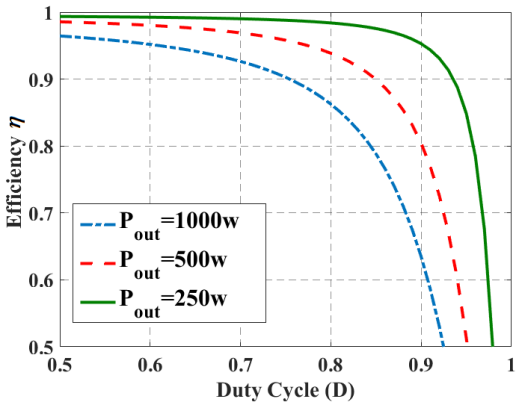


Figure 9.10: Theoretical efficiency versus duty-cycle for different values of output power. ($R_{ESR,P}$ = $R_{ESR,S}$ = 15 mΩ, $R_{ESR,C}$ = 22 mΩ, $R_{DS(on)}$= 5 mΩ, R_D = 7 mΩ, n = 1.2, V_F = 1.25, and V_{out} = 600)

9.7 Experimental Results

To validate the theoretical analysis, a 1kW prototype of the proposed topology operating at 100 kHz is implemented, shown in Figure 9.11. The parameters and components used in the prototype are listed in Table 9.4. To implement the desired coupled inductors, an EE55 ferrite core is used. A TMS320F28337S is employed to generate the signal pulses for the control scheme. To handle high current as well as reduce the conduction losses, two switches EPC2034 are connected in parallel.

The experimental results at the full-load condition for two different values of input voltage 30 V and 40 V are presented in Figure 9.12 and Figure 9.13, respectively. The gate-source pulses of all switches are shown in Figure 9.12 (a). According to (15), to achieve a voltage gain around 20, the control circuit should generate pulses with a duty cycle of 0.66. As can be seen from Figure 9.12 (a), the experimental results match the theoretical analysis

reasonably. Thereby, the operation with extreme values of duty-cycle to obtain a high voltage gain is avoided in the proposed topology.

TABLE 9.4: PARAMETERS AND COMPONENTS OF THE PROTOTYPE

Item	SPECIFICATION
Input voltage V_{in}	30-40 V
Output voltage V_{out}	600 V
Output power P_{out}	1 kW
Switching frequency f_s	100 kHz
Switches	Two EPC2034 in parallel (V_{DS} = 200 V, I_{DS} = 48 A, $R_{DS(ON)}$ =10 mΩ)
Diodes	RFN20NS6SFHTL (V_{rrm} = 600 V, I_F = 20 A, V_F = 1.25 V)
Clamp Capacitor C_C	220 µF (Electrolytic capacitor)
Output capacitors C_{o1} and C_{o2}	220 µF (Electrolytic capacitors)
Switched capacitors C_{m1} and C_{m2}	10 µF (Film capacitors)
Magnetizing inductance L_m	40 µH
Leakage inductance L_k	0.8 µH
Turns ratio N_2:N_1	12:10- EE55 ferrite core, N97 material

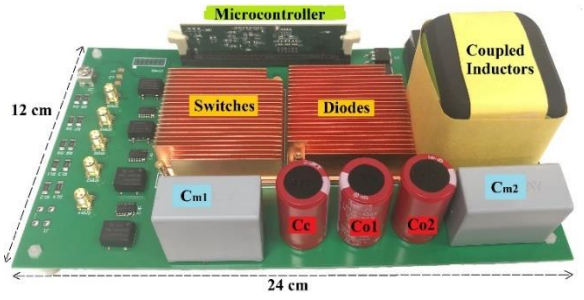


Figure 9.11: Photograph of the laboratory prototype with microcontroller.

The voltage of output capacitors C_{o1} and C_{o2}, the voltage across the clamp capacitor C_C, and the input voltage are displayed in Figure 9.12(b). It can be seen that the voltage ripple is so small, which confirms the correctness of the design of capacitors. The automatic current sharing performance is explained in Figure 9.12(c), in which the current of leakage inductors and input current are demonstrated. As can be seen, the automatic equal current sharing can be obtained without adopting any special control scheme. Also, it is clear that the magnetizing inductance of the coupled inductors acts like the input filter so as to reduce the input current ripple. The voltage stress across switches S_1 and S_{C1} are demonstrated in Figure 9.12 (d). Due to use of active-clamp technology, the voltage stress of switches is limited to the voltage of capacitor C_C, which is about 70 V. It can be concluded that the voltage stress of switches are much less than the output voltage (600 V); therefore, switches with smaller on-resistance $R_{DS(on)}$ can be adopted that leads to higher efficiency. As discussed in the previous section, the soft-switching performance of main switches S_1 and S_2 is more challenging than that of the clamp switches. So, the soft-switching operation of the main switch S_1 is considered in this section. To investigate the soft-switching performance of the switch S_1, the gate-source and drain-source voltage are shown in Figure 9.12 (e). It is obvious that ZVS at turn on for the main switch S_1 is accomplished. The voltage and current of diodes D_{O1} and D_{O2} are given in Figure 9.12 (f). As can be seen from this figure, the diodes turn off under ZCS condition due to controlling their current by the leakage inductance, alleviating the reverse recovery issue.

The experimental results of the proposed converter at input voltage 40 V are shown in Figure 9.13. The gate pulses of switches are shown in Figure 9.13(a). It can be seen that to achieve a voltage gain of 15, the duty cycle is about 0.55, which is in accordance with the

equation (15) fairly. The input voltage and voltage stress across switches S_1 and S_{C1} are demonstrated in Figure 9.13 (b). It can be observed that the voltage stress of switches (90 V) are much less than the output voltage (600 V); thus, the proposed circuit enables using switches with smaller on-resistance $R_{DS(on)}$ that results in lower conduction losses. Figure 9.13 (c) and (d) shows the gate-source and drain-source voltage of switch S_1 and S_2, respectively, where the ZVS at turn-on instant is demonstrated. The input current, the gate voltage of switch S_1, and the current of output diode D_{o1} are presented in Figure 9.13 (e), following the theoretical analysis. The waveform of voltage and current of diodes D_{O1} and D_{O2} are presented in Figure 9.13 (f), in which the current of diodes are controlled by the leakage inductance of the coupled-inductors.

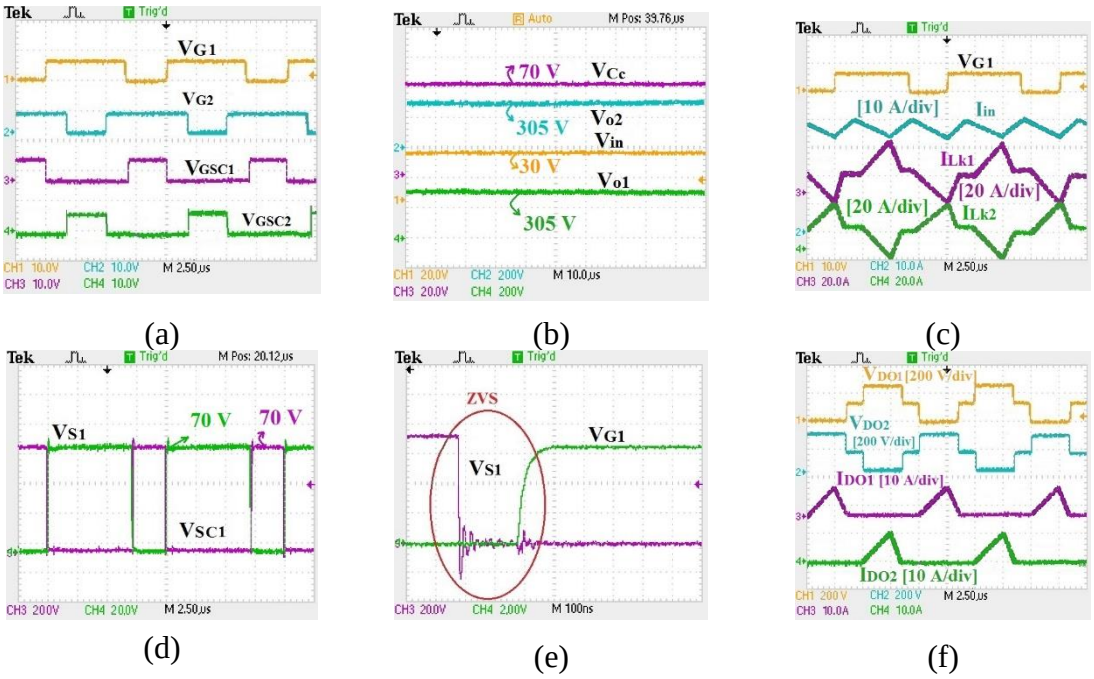


Figure 9.12: Experimental results at full-load condition and input voltage 30 V. (a) The gate pulse of switches. (b) The voltage across different capacitors. (c) The current of leakage inductors L_{k1} and L_{k2}. (d) The voltage stress across switches S_1 and S_{c1}. (e) The gate-source and drain-source voltage of switch S_1. (f) The voltage and current of diodes D_{o1} and D_{O2}.

Therefore, ZCS at turn-off instant is fulfilled that helps alleviate the reverse recovery issue. The theoretical and measured efficiency of the proposed converter for different output power and input voltage values are shown in Figure 9.14 (a). The theoretical and measured efficiency of the converter at the nominal output power (1000 W) and input voltage 40 V are 97.1 % and 97.0 %, respectively. From Figure 9.14, it is clear that the maximum efficiency occurs at the output power 600 W, where theoretical and measured efficiency values are 97.7 % and 97.5 %, respectively. Figure 9.14 (b) compares the efficiency curves of the proposed converter and other converters versus output power. In this comparison, it has been assumed that the all the converters are working under the same operating conditions (given in Table IV). Also, the same switches and diodes are being used in all the converters.

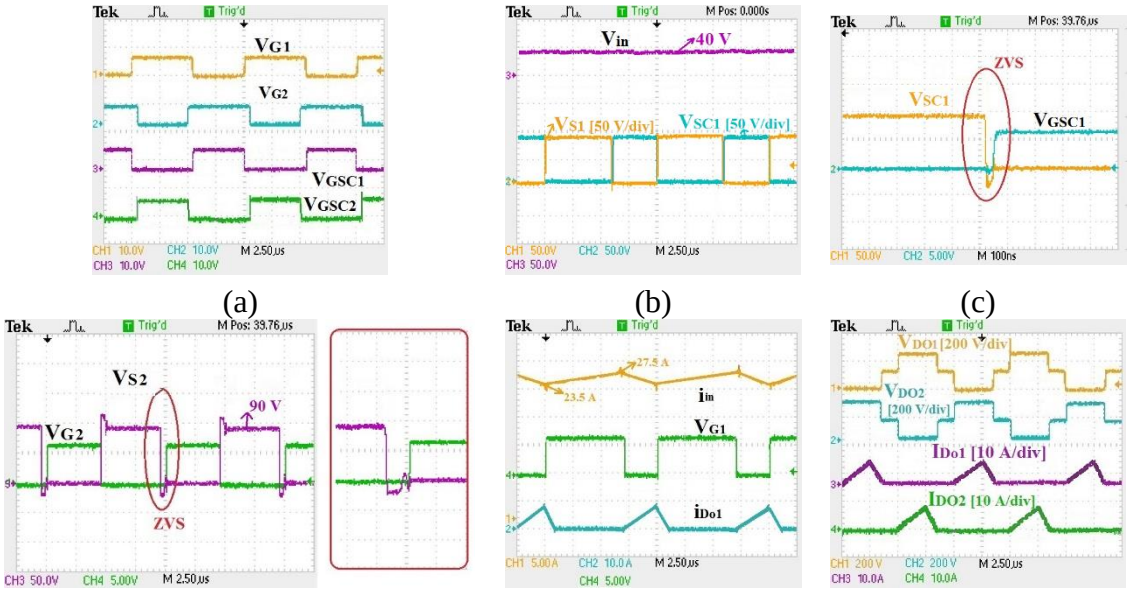
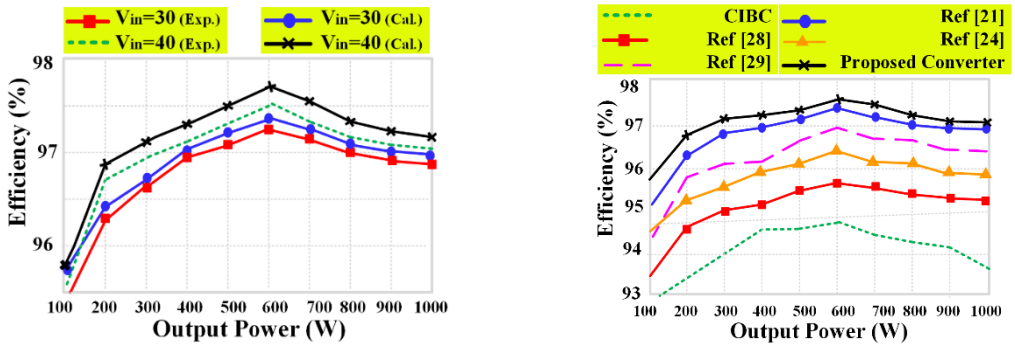


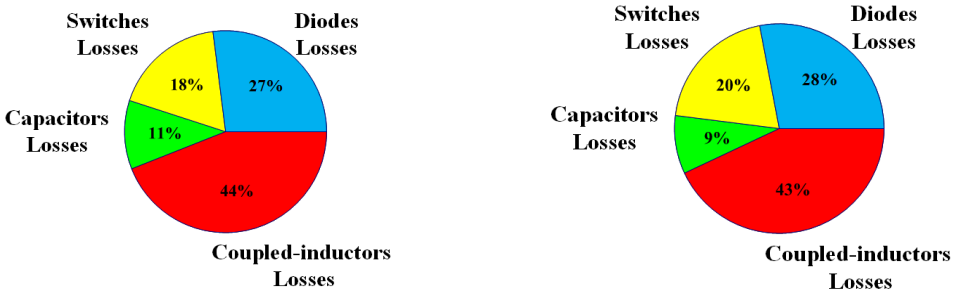
Figure 9.13: Experimental results at full-load condition and input voltage 40 V. (a) The gate pulse of switches. (b) The voltage stress across switches S_1 and S_{c1}. (c) The gate-source and drain-source voltage of switch S_{C1}. (d) The gate-source and drain-source voltage of switch S_2 (e) The gate voltage of switch S_1, current of diode D_{O1}, and input current. (f) The voltage and current of diodes D_{o1} and D_{O2}.



(a) (b)

Figure 9.14: Efficiency variation under different voltage level and comparison of efficiency. (a) measured and theoretical efficiency of the proposed converter. (b) The efficiency comparison (V_{out} = 600 V, V_{in}= 30 V, f_s = 100 kHz, P_{out} = 1 kW).

It can be seen that the efficiency of the proposed converter is higher than the other converters due to the reduced voltage stress of the semiconductors. The loss breakdown at the full-load condition for different input voltage V_{in} =30 V and V_{in} =40 V are presented in Figure 9.15(a) and (b), respectively. It can be seen that the coupled-inductor losses, especially conduction losses, is the dominant power losses in the proposed circuit. To further improve the efficiency of the proposed system, the better-graded wires for coupled-inductors can be adopted.



(a) (b)

Figure 9.15: The loss breakdown at full-load condition for different input voltage. (a) V_{in} = 30 V. (b) V_{in} = 40 V.

9.8 Conclusion

In this chapter, a soft-switched dc-dc interleaved converter with high voltage gain was proposed that integrates two coupled inductors and switched-capacitor circuit so as to improve the power density, which is suitable for applications demanding high voltage conversion ratio such as for FC-based HEV systems. To absorb the voltage spike across the switches and recycle the leakage energy to the load, a promising integrated regenerative snubber circuit is adopted. Compared to the other HSUC, the salient advantages of proposed topology are high voltage gain, small input current ripple, low voltage stress across the semiconductors, and built-in automatic current sharing. ZVS performance of switches, along with ZCS operation of diodes, paves the way for improving the efficiency of the proposed converter. As the asymmetrical pulse-width-modulation is used as a control technique, there is no complexity added to the control technique. As the diodes current is controlled by the leakage inductance, the reverse recovery problem is alleviated, and EMI noise is restrained as well. The experimental results of a 1kW prototype of the converter were presented to validate the proposed topology, which demonstrate the converter suits well for applications demanding with high voltage gain.

Chapter 10 A Soft-Switched DC/DC Converter using Integrated Dual Half-Bridge with High Voltage Gain and Low Voltage Stress for DC Microgrid Applications

10.1 Introduction

In this chapter, a soft-switched boost converter including an integrated dual half-bridge circuit with high voltage gain and continuous input current is introduced that can be suitable for the applications requiring a wide voltage gain range, such as for the front-end of the inverter in a DC microgrid to integrate renewable energy sources (RES). In the proposed converter, two half-bridge converters are connected in series at the output stage to enhance the voltage gain. Additionally, the balanced voltage multiplier stage is employed at the output to increase the voltage conversion ratio, as well as distribute the voltage stress across semiconductors; hence, switches with smaller on-resistance $R_{DS(on)}$ can be adopted resulting in an improvement in the efficiency. The converter takes advantage of the clamp circuit not only to confine the voltage stress of switches, but also to achieve the soft-switching characteristics, which leads to a reduction in the switching loss as well as the cost. The mentioned features make the proposed converter a proper choice for interfacing RES to the DC-link bus of the inverter. The operation modes, steady-state analysis, and design consideration of the proposed topology have been demonstrated in the chapter. A 1-kW laboratory prototype was built using gallium nitride (GaN) transistors and silicon carbide (SiC) diodes to confirm the effectiveness of the proposed topology.

10.2 Structure and Operating Principles of the Proposed Converter

The general layout of a hybrid microgrid including a high step-up DC/DC converter is demonstrated in Figure 10.1. Since PV modules can generate the low-level voltage, it needs a DC-DC converter with a high voltage gain to solve the issue resulting from the mismatch in the voltage level of PV and the DC-bus. In other words, this converter must boost the voltage of PV (15–30 V) to the essential level demanded by the DC-bus (around 400 V).

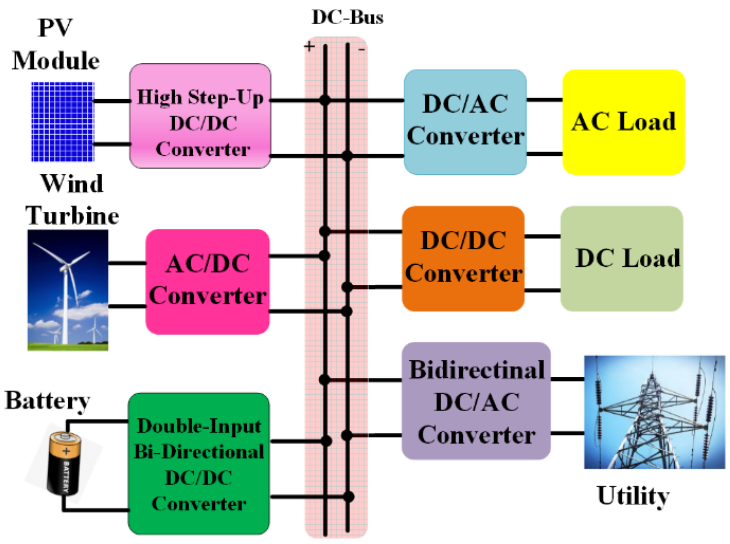


Figure 10.1: General layout of a hybrid microgrid system.

10.2.1 General Structure of the Proposed Converter

The proposed converter is shown in Figure 10. 2(a), which consists of conventional boost converter with active-clamp circuit to provide an input current with low ripple as well as soft-switching performance, and the balanced VMS to increase the voltage conversion ratio. The equivalent circuit of proposed converter is depicted in Figure 10.2(b), in which V_{in} denotes the PV source; V_o denotes the output voltage; L_B denotes the boost inductor; C_r denotes the DC-blocking capacitor; C_{o1}–C_{o4} denote the output capacitors; C_{m1} and C_{m2} denote the switched capacitor; S_M and S_C denote the main and clamp switch, respectively;

D_{o1}–D_{o4} denote the output diodes; and R_o denotes the load resistance. It is noteworthy to mention that a magnetizing inductor (L_m), a leakage inductor (L_k), and an ideal transformer with a turn-ratio of $n = N_2/N_1$ are used to model the transformers. In Figure 10.2(b), L_{k1} and L_{m1} denotes the leakage inductor and the magnetizing inductor of transformer T_1; L_{k2} and L_{m2} denotes the leakage inductor and the magnetizing inductor of transformer T_2.

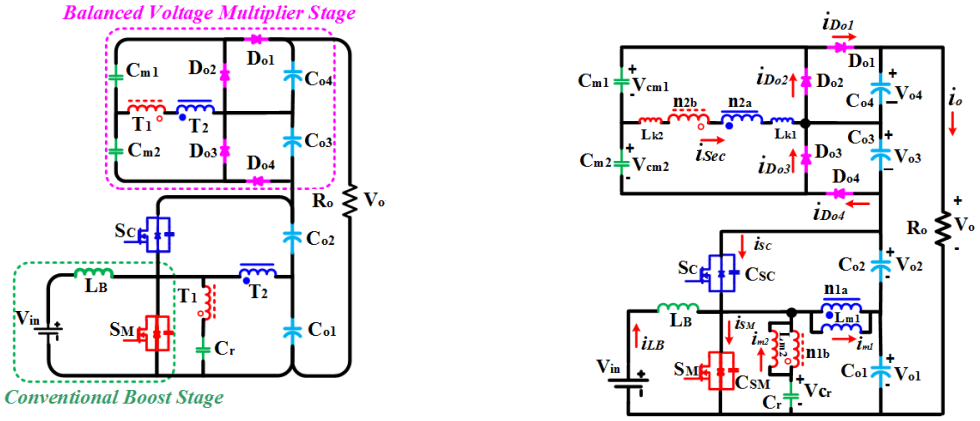


Figure 10.2: The schematic of the proposed converter: (a) proposed converter; and (b) the equivalent circuit.

10.2.2 Operation Modes

There are six operation modes in the proposed converter during one switching period, as illustrated in Figure 10.3. The key waveforms during one switching period are shown in Figure 10.4. To analysis the operation in the steady-state and derive the operational parameters of proposed converter, following assumptions are made:

1) The inductor L_k shows the total inductance of leakage inductors L_{k1} and L_{k2}.
2) all passive and active semiconductors are considered ideal.
3) the capacitors are large enough to assume that their voltage is constant during one switching period.

Mode 1 [t_0–t_1]: Before t_0, the clamp switch was conducting the current. At t_0, the gate pulse of S_C is removed, as shown in Figure 10.4. As depicted in Figure 10.3(a), during this state, the parasitic capacitors of switches S_M and S_C are being discharged and charged, respectively. Due to the parasitic capacitor, the voltage stress of clamp switch increases linearly, which is expressed by:

$$V_{SM} \cong \frac{i_{LB}(t_0) - 2ni_{Lk}(t_0) - i_{Lm1}(t_0) + i_{Lm2}(t_0)}{C_{SM} + C_{SC}}(t - t_0) \tag{10-1}$$

The duration of this mode can be determined by:

$$\Delta t_{01} = \frac{(C_{SM} + C_{SC})(V_{o1}(t_0) + V_{o2}(t_0))}{i_{LB}(t_0) - 2ni_{Lk}(t_0) - i_{Lm1}(t_0) + i_{Lm2}(t_0)} \tag{10-2}$$

Mode 2 [t_1–t_2]: This mode starts when the voltage of main switch V_{SM} becomes zero and, hence, its antiparallel diode starts conducting the current. Thus, the ZVS performance of main switch at turn-on instant is ensured. During this mode in Figure 10.3(b), the voltage stress of clamp switch is restricted to the total voltage of capacitors C_{o1} and C_{o2} without spikes problem. At the output stage, the output diodes D_{o2} and D_{o4} are cut off, and diodes D_{o1} and D_{o3} are conducting the current, expressed as:

$$i_{Do1}(t) = i_{Do3}(t) = 0.5i_{Lk}(t) = 0.5i_{Lk}(t_0)$$
$$+\frac{nV_{Cr}(t_0) + nV_{o1}(t_0) + V_{o4}(t_0) - V_{cm1}(t_0)}{2L_k}(t - t_0) \tag{10-3}$$

During this mode, the boost inductor stores the energy of the input source, i.e., PV source, and the input current increases which can be determined by:

$$i_{LB}(t) = i_{LB}(t_1) + \frac{V_{in}}{L_B}(t - t_1) \tag{10-4}$$

The current of magnetizing inductors can be defined by:

$$i_{Lm1}(t) = i_{Lm1}(t_1) - \frac{V_{o1}(t_1)}{L_{m1}}(t - t_1) \quad (10\text{-}5)$$

$$i_{Lm2}(t) = i_{Lm2}(t_1) + \frac{V_{Cr}(t_1)}{L_{m2}}(t - t_1) \quad (10\text{-}6)$$

Mode 3 [t_2–t_3]: This mode starts at t_2 when the leakage inductors current becomes zero; so, the diodes D_{o2} and D_{o4} turn on, as shown in Figure 10.3(c). Therefore, ZCS at turn-on instant is achieved for these diodes, alleviating their losses. In the meantime, the transformers transfer the energy of input source and output capacitor C_{o1} to the switched capacitor C_{m1} and output capacitor C_{o3}. The secondary windings of transformer are connected in a way that the total voltage of the output stage increases. The current of leakage inductance and output diodes, and main switch can be expressed by:

$$i_{Do2}(t) = i_{Do4}(t) = 0.5 i_{Lk}(t) \quad (10\text{-}7)$$

$$= 0.5 i_{Lk}(t_2) + \frac{nV_{Cr}(t_2) + nV_{o1}(t_2) - V_{cm1}(t_2)}{2L_k}(t - t_2)$$

$$i_{SM}(t) = i_{in}(t) + 2n i_{Lk}(t) + i_{Lm2}(t) - i_{Lm1}(t) \quad (10\text{-}8)$$

Mode 4 [t_3–t_4]: At t_3, the gate pulse of clamp switch is removed, and the output capacitors of switches S_M and S_C are being charged and discharged, respectively. Due to the parasitic capacitor, the voltage stress of main switch increases linearly. The circuit condition at the VMS is the same as in Mode 3. The following equations define the voltage stress of main switch and the duration of this mode as:

$$V_{SC} \cong \frac{i_{LB}(t_3) + 2n i_{Lk}(3) - i_{Lm1}(t_3) + i_{Lm2}(t_3)}{C_{SM} + C_{SC}}(t - t_3) \quad (10\text{-}9)$$

$$\Delta t_{34} = \frac{(C_{SM} + C_{SC})(V_{o1}(t_3) + V_{o2}(t_3))}{i_{LB}(t_3) + 2n i_{Lk}(t_3) - i_{Lm1}(t_3) + i_{Lm2}(t_3)} \quad (10\text{-}10)$$

Mode 5 [t_4–t_5]: As shown in Figure 4, at the beginning of this mode, the voltage across clamp switch V_{SC} becomes zero; thus, the current flows through the antiparallel diode of

clamp switch. Accordingly, the ZVS implementation of clamp switch at turn-on instant is guaranteed. During this mode, the voltage stress of main switch is effectively confined to the total voltage of capacitors C_{o1} and C_{o2} without ringing and spikes issue, shown in Figure 10.3(e). In the meantime, the boost inductor is transferring the PV-source energy to the output capacitor C_{o1} and C_{o2}. At the output stage, the output diodes D_{o2} and D_{o4} are conducting the current. The following equations can be written for this operation mode:

$$\begin{aligned} i_{Do2}(t) = i_{Do4}(t) &= 0.5 i_{Lk}(t) \\ &= 0.5 i_{Lk}(t_4) \\ &+ \frac{nV_{Cr}(t_4) - nV_{o1}(t_4) - 2nV_{o2}(t_4) - V_{cm1}(t_4)}{2L_k}(t - t_4) \end{aligned} \tag{10-11}$$

$$i_{LB}(t) = i_{LB}(t_4) + \frac{V_{in} - V_{o1} - V_{o2}}{L_B}(t - t_4) \tag{10-12}$$

$$i_{Lm1}(t) = i_{Lm1}(t_4) + \frac{V_{o2}(t_4)}{L_{m1}}(t - t_4) \tag{10-13}$$

$$i_{Lm2}(t) = i_{Lm2}(t_4) + \frac{V_{Cr}(t_4) - V_{o1}(t_4) - V_{o2}(t_4)}{L_{m2}}(t - t_4) \tag{10-14}$$

Mode 6 [t_5–t_6]: At the beginning of this mode, the direction of inductor current changes; thus, the diodes D_{o2} and D_{o4} are cut off and diodes D_{o1} and D_{o3} turn on, as shown in Figure 10.3(f). Therefore, ZCS at turn-on instant is enabled for diodes D_{o1} and D_{o3}, which helps alleviate turn-on losses. In the meantime, the energy stored in the switched-capacitor C_{m1} is being released to the output capacitor C_{o4}. On the other hand, the switched-capacitor C_{m2} is storing the energy transferred by transformers from the input stage. The current of leakage inductance and output diodes, and clamp switch can be expressed by

$$i_{Do1}(t) = i_{Do3}(t) = 0.5 i_{Lk}(t) = \tag{10-15}$$

$$0.5i_{Lk}(t_0) + \frac{nV_{Cr}(t_5) - nV_{o1}(t_5) - 2nV_{o2}(t_5) + V_{o4}(t_5) - V_{cm1}(t_5)}{2L_k}$$

$$(t - t_5)$$

$$i_{SC}(t) = i_{in}(t) + 2ni_{Lk}(t) + i_{Lm2}(t) - i_{Lm1}(t) \qquad (10\text{-}16)$$

At the end of this operation mode the gate pulse of clamp switch will be removed, and the converter begins a new switching period.

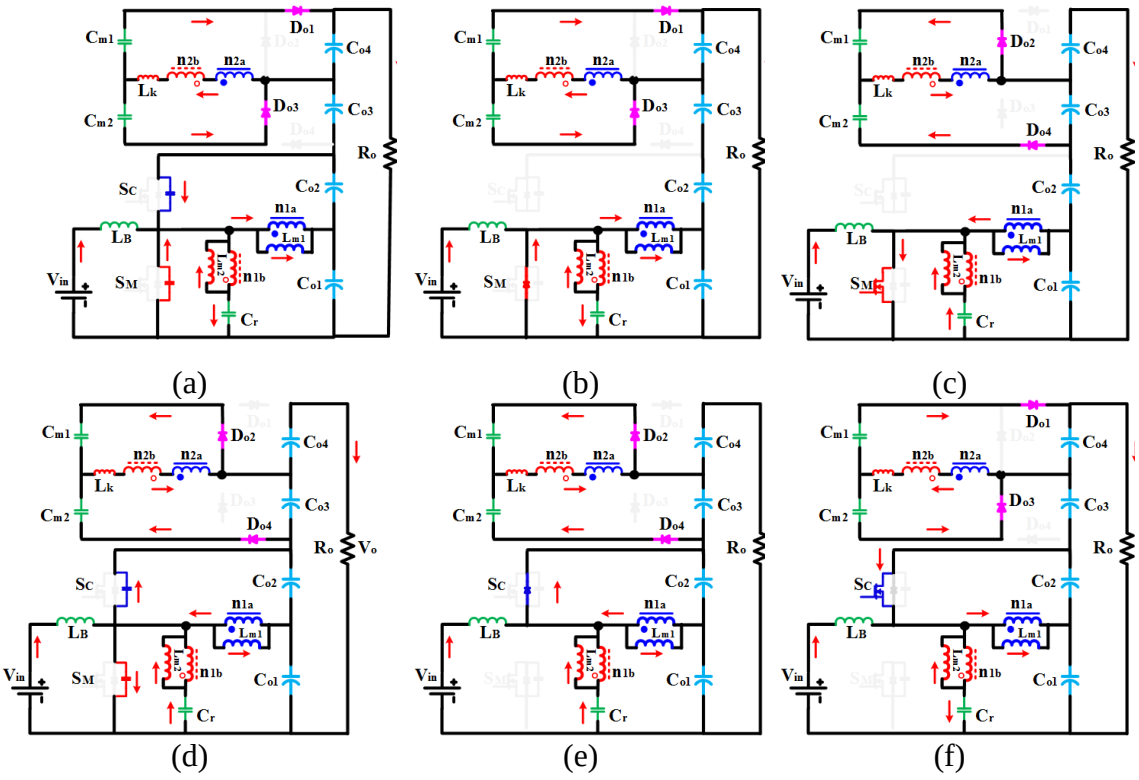


Figure 10.3: Operation modes: (a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4; (e) Mode5; and (f) Mode 6.

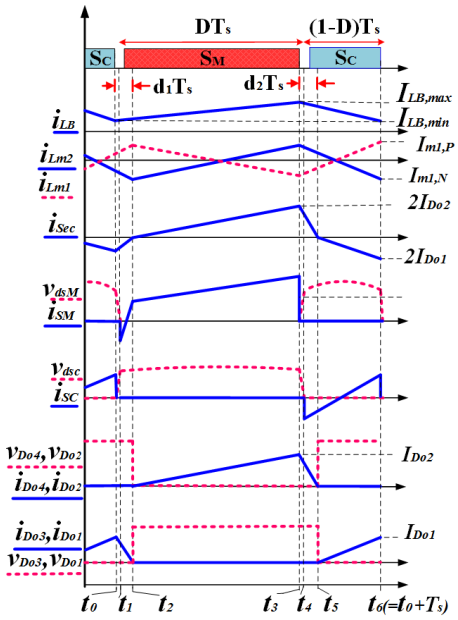


Figure 10.4: Key waveforms of the proposed converter.

10.2.3 Voltage Gain

To derive the operational parameters of proposed converter, it is assumed that as compared with the leakage inductors, the magnetizing inductors are so large that their effect can be neglected. By applying the voltage-second balance to the inductor L_B and the primary winding of transformers T_2, the output voltage V_{o1} and V_{o2} can be expressed as:

$$V_{o1} + V_{o2} = \frac{V_{in}}{1 - D} \tag{10-17}$$

$$V_{o1} = V_{in} \tag{10-18}$$

$$V_{o2} = \frac{DV_{in}}{1 - D} \tag{10-19}$$

The duty cycle of the main switch is denoted as $D = T_{on}/T_S$, where T_{on} represents the conduction time of main switch in each switching period and T_S represents the switching period. Considering Figure 10.3, the voltage of DC-blocking capacitor can be derived by applying the voltage-second balance to the primary windings of transformers T_1 as follows:

$$V_{Cr} = V_{in} \tag{10-20}$$

From Equation (3) and (15), the diode D_{o1} peak current, I_{Do1}, can be written as follows:

$$I_{Do1} = \frac{2nV_{in} + V_{o4} - V_{cm1}}{2L_k} d_1 T_s = \frac{\frac{2nDV_{in}}{1-D} - V_{o4} + V_{cm1}}{2L_k} (1 - D - d_2) T_s \tag{10-21}$$

From Equations (7) and (11), the diode D_{o2} peak current, I_{Do2}, can be achieved from:

$$I_{Do2} = \frac{2nV_{in} - V_{cm1}}{2L_k} (D - d_1) T_s = \frac{\frac{2nDV_{in}}{1-D} + V_{cm1}}{2L_k} d_2 T_s \tag{10-22}$$

From Equations (21) and (22), the output voltage V_{o4} and the voltage of switched capacitor C_{m1} can be obtained by:

$$V_{cm1} = 2nV_{in} \frac{(D - d_1)(1 - D) - Dd_2}{(1 - D)(D - d_1 + d_2)} \tag{10-23}$$

$$V_{o4} = 2nV_{in} [\frac{(D - d_1)(1 - D) - Dd_2}{(1 - D)(D - d_1 + d_2)} + \frac{D(1 - D - d_2) - (1 - D)d_1}{(1 - D)(1 - D + d_1 - d_2)}] \tag{10-24}$$

Since the average capacitor current must be zero at steady state, the output diode currents I_{Do1} and I_{Do2} can be expressed as:

$$I_o = \int_0^{T_s} i_{Do1}(t) dt = \int_0^{T_s} i_{Do2}(t) dt \tag{10-25}$$

From Equation (10-25) and Figure 10.4, the output current can be determined by:

$$I_o = \frac{(D - d_1 + d_2)}{2} I_{Do2} = \frac{(1 - D + d_1 - d_2)}{2} I_{Do1} \tag{10-26}$$

From Equations (10-23), (10-24), and (10-26), the parameters d_1 and d_2, which are shown in Figure 10.4 can be demonstrated in the form of:

$$d_1 = kD \tag{10-27}$$

$$d_2 = k(1 - D) \tag{10-28}$$

$$k = 0.5(1 - \sqrt{1 - \frac{8L_k I_o f_s}{nDV_{in}}}) \tag{10-29}$$

Since the VMS operates symmetrically, the voltage stress of capacitors C_{o3} and C_{o4} is identical; so, the voltage gain, $M = V_{out}/V_{in}$, can be defined as follows:

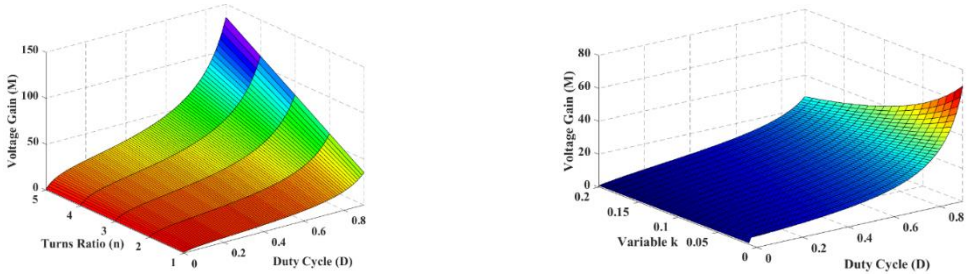
$$M = \frac{V_o}{V_{in}} = \frac{V_{o1} + V_{o2} + V_{o3} + V_{o4}}{V_{in}} \tag{10-30}$$

$$= \frac{1}{1 - D} + \frac{4n(1 - 2k)D}{(D - 2Dk + k)(1 - D + 2Dk - k)}$$

When ignoring the variable k in Equation (30) due to the small order of value of leakage inductance, the ideal voltage gain will be:

$$M = \frac{V_o}{V_{in}} = \frac{4n + 1}{1 - D} \tag{10-31}$$

Figure 10.5 shows the voltage gain characteristic of proposed converter versus different duty cycle (D) and turns-ratio (n) for different values of variable k. The converter ensures high voltage gain with a small turns ratio even with a low duty cycle and, thus, the voltage stress as well as the switching loss can be reduced.



(a) (b)

Figure 10.5: Voltage gain characteristics: (a) voltage gain versus different duty cycle and turns-ratio when k = 0.06; and (b) voltage gain versus different duty cycle and variable k when n = 1.5.

10.2.4 Voltage Stress Across Switches and Diodes

From the operation principle of proposed converter, the voltage stress of switches is effectively restricted to the voltage across output capacitors C_{o1} and C_{o2} without ringing and spikes issue due to adopting active-clamp configuration. Thus, the voltage stress of switches can be expressed by:

$$V_{SM,max} = V_{SC,max} = V_{o1} + V_{o2} = \frac{V_{in}}{1-D} = \frac{V_o}{4n+1} \tag{10-32}$$

Due to the balanced operation of VMS, the voltage stress of all diodes is identical and can be achieved by:

$$V_{Do1} = V_{Do2} = V_{Do3} = V_{Do4} = \frac{2nV_o}{4n+1} \tag{10-33}$$

From (10-33), it can be concluded that the switches and diodes withstand much lower voltage stress than the output voltage resulting in switches with smaller on-resistance $R_{DS(on)}$ can be used; hence, the efficiency can be improved. Moreover, when turns-ratio keeps increasing the voltage stress of switches and diodes reduces.

10.2.5 The Magnetizing Inductor Minimum and Maximum Currents i_{m1} and i_{m2}

From (10-5), (10-6), (10-13), and (10-14), the relation between maximum and minimum magnetizing current for transformers T_1 and T_2 can be written as follows:

$$I_{m1,P} - I_{m1,N} = I_{m2,P} - I_{m2,N} = \frac{V_{in}DT_s}{2L_{m1}} \tag{10-34}$$

From Figure 10.2, along with the ampere-second balance for capacitors, it can be concluded that the average value of the current of magnetizing inductors is zero. Thus, the magnetizing inductor maximum and minimum current can be achieved from:

$$I_{m1,P} = I_{m1,N} = I_{m2,P} = I_{m2,N} = \frac{V_{in} D T_s}{2 L_{m1}} \tag{10-35}$$

10.2.6 ZVS Soft-Switching Conditions for Switches S_M and S_C

As illustrated in "Operation Modes" section, the soft-switching performance can be achieved for both switches as an inherent advantage of proposed topology leading to less switching loss in the active semiconductors. The ZVS performance is guaranteed for switch S_C if its gate-pulse is applied when the anti-parallel diode is conducting the current during mode 5. In other words, the following condition should be satisfied:

$$0.5 L_B I_{SC,ZVS}^2 \geq 0.5 (C_{SM} + C_{SC}) (\frac{V_{in}}{1-D})^2 \tag{10-36}$$

where the ZVS current $I_{SC,ZVS}$ is defined by:

$$I_{SC,ZVS} = I_{LB,max} + 2 I_{m1,P} + \frac{8 n I_o}{D} = \frac{2 L_B P_o + D T_s V_{in}^2}{2 V_{in} L_B} + \frac{V_{in} D T_s}{L_{m1}} + \frac{8 n P_o}{D V_o} \tag{10-37}$$

To ensure the ZVS performance at turn-on instant for main switch S_M, the energy difference between the energy stored in the leakage inductor L_k and magnetizing inductor L_m should be larger than the energy stored in the parasitic capacitors of S_M and S_C. This condition can be written as follows:

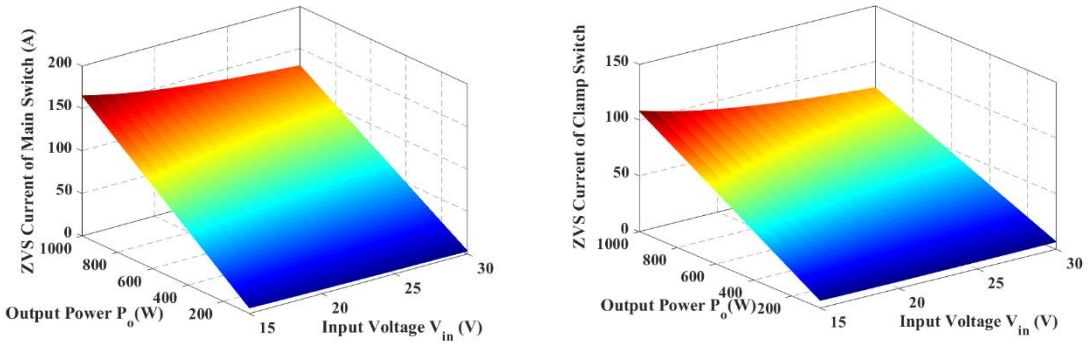
$$0.5 L_B I_{SMZVS}^2 \geq 0.5 (C_{SM} + C_{SC}) (\frac{V_{in}}{1-D})^2 \tag{10-38}$$

The ZVS current of main switch $I_{SM,ZVS}$ is defined by:

$$I_{SM,ZVS} = I_{LB,min} - 2 I_{m1,P} - \frac{8 n I_o}{1-D} = \frac{2 L_B P_o - D T_s V_{in}^2}{2 V_{in} L_B} - \frac{V_{in} D T_s}{L_{m1}} + \frac{8 n P_o}{(1-D) V_o} \tag{10-39}$$

The relationship between the ZVS current versus the input voltage and output power for both switches S_M and S_C are plotted in Figure 10.6(a) and (b), respectively. It can be seen

that the soft-switching performance can be achieved for both switches for a wide range of input voltage and output power, improving the efficiency of power conversion system.



(a) (b)

Figure 10.6: Soft-switching characteristics of the proposed converter. (a) ZVS current of the main switch; and (b) ZVS current of the clamp switch.

10.2.7 Current Stress of Power Switches and Diodes

From Figure 10.2 and Equation (8), the maximum current of main switch can be derived by:

$$I_{SM,max} = I_{LB,max} + 2I_{m1,P} + \frac{8nI_o}{D} = \frac{2L_BP_o + DT_sV_{in}^2}{2V_{in}L_B} + \frac{V_{in}DT_s}{L_{m1}} + \frac{8nP_o}{DV_o} \quad (10\text{-}40)$$

Similarly, the maximum current of clamp switch can be derived from Equation (16), determined by:

$$I_{SC,max} = I_{LB,min} - 2I_{m1,P} + \frac{8nI_o}{(1-D)} \quad (10\text{-}41)$$

$$= \frac{2L_BP_o - DT_sV_{in}^2}{2V_{in}L_B} - \frac{V_{in}DT_s}{L_{m1}} + \frac{8nP_o}{(1-D)V_o}$$

The maximum current and average current of output diodes can be estimated by ignoring the effect of leakage inductance, which is given as follows:

$$I_{Do1,max} = I_{Do3,max} = \frac{2I_o}{1-D} \quad (10\text{-}42)$$

$$I_{Do2,max} = I_{Do4,max} = \frac{2I_o}{D} \tag{10-43}$$

$$I_{Do1,avg} = I_{Do2,avg} = I_{Do3,avg} = I_{Do4,avg} = I_o \tag{10-44}$$

10.2.8 2.8. Comparison with Other High Step-Up Converters

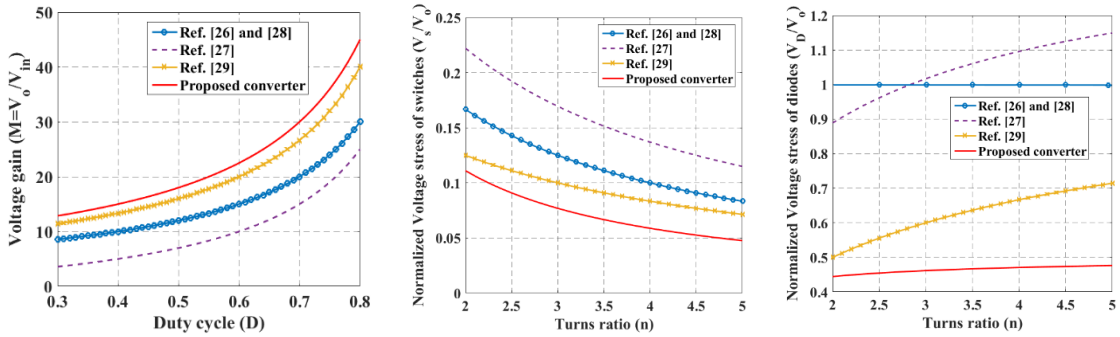
To have a better insight into the performance superiority of proposed topology, a comparison is carried out regarding the functional characteristics, including the voltage gain, voltage stress of switches and diodes, number of passive and active components, soft-switching performance, and complexity of control circuit. Table 1 compares the proposed converter with the state-of-the-art high step-up DC/DC converters. It can be seen that the proposed converter offers the much higher voltage gain, as well as lowest voltage stress of semiconductors. Thus, the losses and price for implementing a prototype will be lower. Regarding the soft-switching, even though the converters cited in [26] and [28] have the soft-switching characteristic, the proposed converter can provide ZVS conditions for both switches with minimum number of switches, resulting in efficiency improvement. Furthermore, compared to other converters, the control technique and gate-driver circuit are simple for proposed converter due to the asymmetrical PWM control scheme. Figure 7 shows the voltage gain and voltage stress of switches and diodes for proposed converter in comparison to that of other converters. The relation between the voltage gain and duty cycle (D), as shown in Figure 10.7a, indicates that the proposed converter boosts the input voltage with lower operating duty cycle. Therefore, the voltage stress of the switches and the losses will be lower. Figure 10.7 (b) and (c) demonstrates the voltage stress of switches and diodes for different values of turns ratio (n), respectively. To sum up, the proposed

topology outperforms its counterparts regarding the vital specifications of a high step-up converter.

Table 10.1: Performance comparison among proposed converter and other converters.

Item		Converter Cited in [26]	Converter Cited in [27]	Converter Cited in [28]	Converter Cited in [29]	Proposed Converter
Voltage gain		$\frac{2n+2}{1-D}$	$\frac{D(2n+1)+1}{1-D}$	$\frac{2n+2}{1-D}$	$\frac{2n+4}{1-D}$	$\frac{4n+1}{1-D}$
Switch voltage stress		$\frac{V_o}{2n+2}$	$\frac{V_o}{D(2n+1)+1}$	$\frac{V_o}{2n+2}$	$\frac{V_o}{2n+4}$	$\frac{V_o}{4n+1}$
Diode voltage stress		V_o	$\frac{2nV_o}{D(2n+1)+1}$	V_o	$\frac{nV_o}{n+2}$	$\frac{2nV_o}{4n+1}$
No. of Components	S [1]	4	2	4	2	2
	D [2]	2	3	4	6	4
	C [3]	4	3	5	6	7
	L [4]	0	0	2	0	1
No. of Transformer or coupled inductors		2	2	1	2	2
Soft-switching		Soft switching (ZVS)	Hard switching	Soft switching (ZVS)	Hard switching	Soft switching (ZVS)
Control circuit		Complex	Simple	Complex	Simple	Simple

[1] Switch; [2] Diode; [3] Capacitor; [4] Inductor.



(a) (b) (c)

Figure 10.7: Comparison between the proposed converter and other step-up converters. (a) Voltage gain versus duty cycle (D) when n = 2; (b) voltage stress of switches versus turns ratio (n); and (c) voltage stress of diodes versus turns ratio (n).

10.3 Loss Analysis of Proposed Converter

The losses in the proposed converter can be divided into five major contributors, namely: conduction and switching losses of the switches, losses of the diodes, losses of the transformers, and losses of the inductor.

10.3.1 Conduction Loss of Switches

The conduction loss of switches can be calculated by:

$$P_{Cond,S} = R_{DS(on)} I_{rms,s}^2 \tag{10-45}$$

where $I_{rms,s}$ denotes the root mean square (RMS) current of the switch, and $R_{DS(on)}$ denotes the on-resistance of the switch.

10.3.2 Switching Loss of Transistors

In the implemented converter, GaN E-HEMTs switches are employed. As an advantage of GaN switches, they do not have a body diode, as well as the reverse recover charge, the loss caused by the reverse recovery charge of the body diode can be neglected. Other contributors to the switching loss in a GaN switches can be listed as follows: (1) the overlap of current and voltage during turn-on and turn-off; (2) gate charge loss; and (3) the loss caused by the parasitic capacitance of switch. The total switching loss of the switches of the proposed converter can be achieved from:

$$P_{Sw,S} = \left[0.5 V_s I_s \left(t_r + t_f\right) + 0.5 C_{oss} V_s^2 + Q_T V_G\right] f_s \tag{10-46}$$

where f_s is the switching frequency, t_r, and t_f are the rise and fall times of the transistor, Q_T is the gate charge, V_s the voltage stress of switch, and V_G is the gate driver voltage.

10.3.3 Diode Losses

The switching and capacitive charge (Q_C) losses of the SiC diodes can be estimated by:

$$P_{Di} = Q_C V_D f_s + V_{fi} I_{D,rms} \tag{10-47}$$

where V_{fd}, and V_D are the forward voltage and the voltage stress of the diode, respectively. It is noteworthy to mention that the reverse recovery switching loss of the SiC diodes can be ignored.

10.3.4 Inductor Losses

The losses of inductors include two main factors, the copper loss and the core loss. The conduction loss, P_{L_cond}, is caused by the DC current component flowing in the inductors' windings, while the core loss, P_{L_core}, is caused by the inductors' ripple currents, which is given in datasheet. The losses of inductor can be expressed as:

$$P_{Cond,L} = R_{L,ESR} I_{rms,L}^2 \tag{10-48}$$

$$P_{Core,L} = \frac{f_s}{\frac{a}{B^3} + \frac{b}{B^{2.3}} + \frac{c}{B^{1.5}}} + d f_s^2 B^2 \tag{10-49}$$

where $R_{L,ESR}$ and $I_{L,rms}$ are the series parasitic resistances and the RMS current of inductor, respectively. Additionally, the coefficients *a*, *b*, *c*, and *d* are given by manufacturer.

10.3.5 Transformer Losses

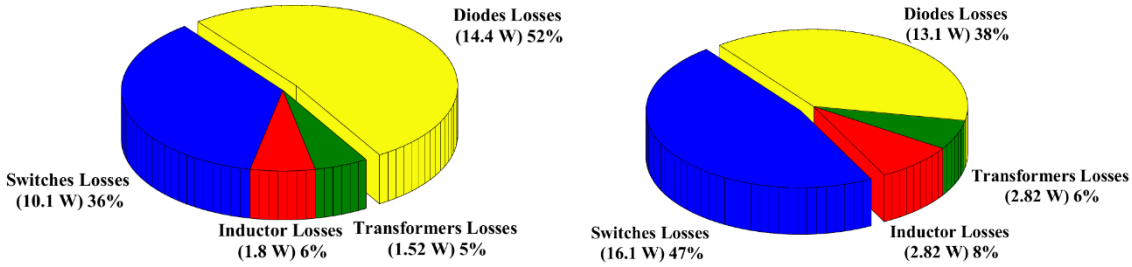
Similar to the inductor, the losses of transformer include two main contributors, the copper loss and the core loss, which are express as:

$$P_{Cond,T} = R_{T,ESR} I_{dc}^2 \{1 + \sum_{n=1}^{\infty} \frac{R_{wn}}{R_{T,ESR}} (\frac{I_n}{I_{dc}})^2\} \tag{10-50}$$

$$P_{Core,T} = \frac{f_s}{\frac{a}{B^3} + \frac{b}{B^{2.3}} + \frac{c}{B^{1.65}}} + d f_s^2 B^2 \tag{10-51}$$

where $R_{T,ESR}$, R_{wn}, I_{DC}, and I_n are the series parasitic resistances, the AC winding resistance, the RMS current of transformer, and the RMS current of the nth frequency component, respectively.

The theoretical breakdown of total loss at half-load and full-load conditions are shown in Figure 10.8 (a) and (b), respectively. It can be seen that the switches and diodes are the major contributors to power loss in the proposed converter.



(a) (b)

Figure 10.8: Loss breakdown (a) half-load condition (P_o = 500 W); and (b) full-load condition (P_o = 1000 W).

10.4 Design Considerations

10.4.1 Selection of Turns Ratio

The proper selection of the turns-ratio helps employ the switches with lower voltage rating. The turns ratio can be achieved from (31), and expressed as:

$$n = \frac{V_o(1-D) - V_{in}}{4V_{in}} \tag{10-52}$$

10.4.2 Choice of Leakage Inductance

The leakage inductance plays an important role in the operation of converter regarding ZVS performance and voltage gain. It can be calculated from (29) and is given by:

$$L_k = \frac{nDV_{in}(1-(1-2k)^2)}{8I_o f_s} \tag{10-53}$$

10.4.3 Choice of Magnetizing Inductance

A good criterion for selecting the magnetizing inductance is to help the switches to obtain ZVS. Thus, it can be derived from Equation (39) as follows:

$$L_{m1} = L_{m2} > \frac{T_s D V_{in}}{\frac{2L_B P_o - D T_s V_{in}^2}{2V_{in} L_B} - \frac{8nP_o}{(1-D)V_o}} \tag{10-54}$$

10.4.4 Choice of Boost Inductance

The boost inductance is adopted to reduce the input current ripple, so to have 20% current ripple ratio, the required boost inductance can be obtained from:

$$L_B = \frac{V_{in} D_{max} T_s}{20\% I_{in}} \tag{10-55}$$

10.4.5 Design of Capacitors

From the operating principle of proposed converter along with charge-second balance on the capacitors, the capacitance can be selected as:

$$C_{o1} = \frac{(1 - D + d_1 - d_2) I_o}{f_s \Delta V_{o1}} \tag{10-56}$$

$$C_{o2} = \frac{(1-D) + d_1 - d_2) I_o}{f_s \Delta V_{o2}} \left(\frac{4n+1}{1-D} I_o - \frac{d_2 I_{Do2} - (1 - D - d_2) I_{Do1}}{2}\right) \tag{10-57}$$

$$C_{o3} = \frac{(1 - D + d_1 - d_2) I_o}{f_s \Delta V_{o3}} \tag{10-58}$$

$$C_{o4} = \frac{(D - d_1 + d_2) I_o}{f_s \Delta V_{o4}} \tag{10-59}$$

$$C_{m1} = C_{m2} = \frac{(D - d_1 + d_2) I_{Do1}}{2 f_s \Delta V_{cm1}} \tag{10-60}$$

$$C_r = \frac{(d_2 I_{Do2} - (1 - D - d_2) I_{Do1})(1 - D)}{2 f_s \Delta V_{cr}} \tag{10-61}$$

Where ΔV_{o1}, ΔV_{o2}, ΔV_{o3}, ΔV_{o4}, ΔV_{cm1}, and ΔV_{cr} denote the maximum allowed voltage ripples allowed for C_{o1}, C_{o2}, C_{o3}, C_{o4}, C_{m1}, and C_r, respectively. Additionally, f_s is the switching frequency.

10.5 Simulation and Experimental Results

To demonstrate the operation modes of the proposed converter along with its effectiveness, a scaled-down laboratory prototype is simulated and implemented. The specifications and components of studied converter are given in Table 10.2.

Table 10.2: Parameters and components of implemented converter.

Parameter	Value
Input DC-voltage (V_{in})	15–30 V
Output voltage (V_o)	400 V
Output power (P_o)	1000 W
Switching frequency (f_s)	100 kHz
Magnetizing inductance (L_{m1} and L_{m2})	100 µH
Leakage inductance (L_{k1} and L_{k2})	10 µH
Turns ratio of coupled inductors (n)	1.5
Switches	EPC2047 (200 V, 160 A,10 mΩ)
Diodes	C3D10065E
Output capacitors (C_{o1}, C_{o2}, C_{o3}, and C_{o4})	47 µF
Switched capacitors (C_{m1} and C_{m2})	10 µF

10.5.1 Simulation Results

To investigate the performance of the proposed converter, two simulations in full load and light load condition are done. In these simulations, the GaN switch model introduced by the company is used. The specifications of the converter are given in Table 10.2.

A) Full Load Condition (V_{in} = 22 V, P_o = 1000 W, and D = 0.65)

Figure 9 demonstrates the functional current and voltage waveforms of simulated converter at the rated output power (P_o = 1000 W), including the ZVS performance of switches, the

boost current i_{LB}, the secondary current i_{Sec}, and the current of diodes. From Figure 10.9(a), it can be seen that the output voltage is adequately regulated by the control circuit. Figure 10.9(b) shows the current of boost inductor L_B and leakage inductor L_k, which confirms that the design of boost inductor is carried out correctly. Moreover, the leakage inductor current is varying linearly, following the theoretical analysis. The current of output diodes are demonstrated in Figure 10.9(c), implying that ZCS performance at turn-off instant is realized for output diodes leading to the efficiency improvement.

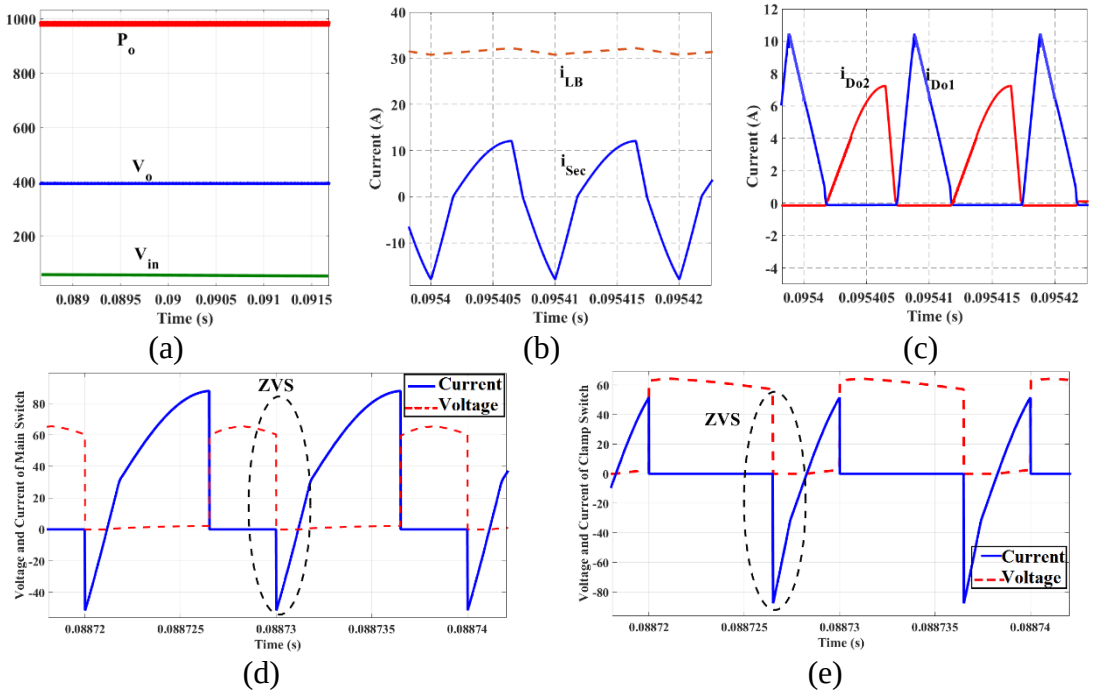


Figure 10.9: Simulation results. (a) Input voltage, output voltage, and output power; (b) the input current i_{LB} and the secondary side current i_{Sec}; (c) current of the output diodes I_{Do1} and I_{DO2}; (d) voltage and current of the main switch; and (e) voltage and current of the clamp switch.

The soft-switching operation for main and clamp switches is shown in Figure 10.9(b) and (c). It is clear that the voltage stress of switches becomes zero before the gate pulse of related switches is applied. Moreover, confirming the equations given in previous section, the voltage stress of switches is around 65 V, which is much lower than output voltage

(400 V). Therefore, switches with smaller on-resistance can be used, contributing to fewer conduction losses.

B) Light Load condition (V_{in} = 22 V, P_o = 100 W, and D = 0.48)

Figure 10.10 shows the functional current and voltage waveforms of simulated converter during light loading (P_o = 100 W), including the ZVS performance of switches and the voltage of output diodes V_{Do1} and V_{DO2}. The soft-switching operation for main and clamp switches is shown in Figure 10.10 (a) and (b). It is clear that the voltage stress of switches becomes zero before the gate pulse of related switches is applied.

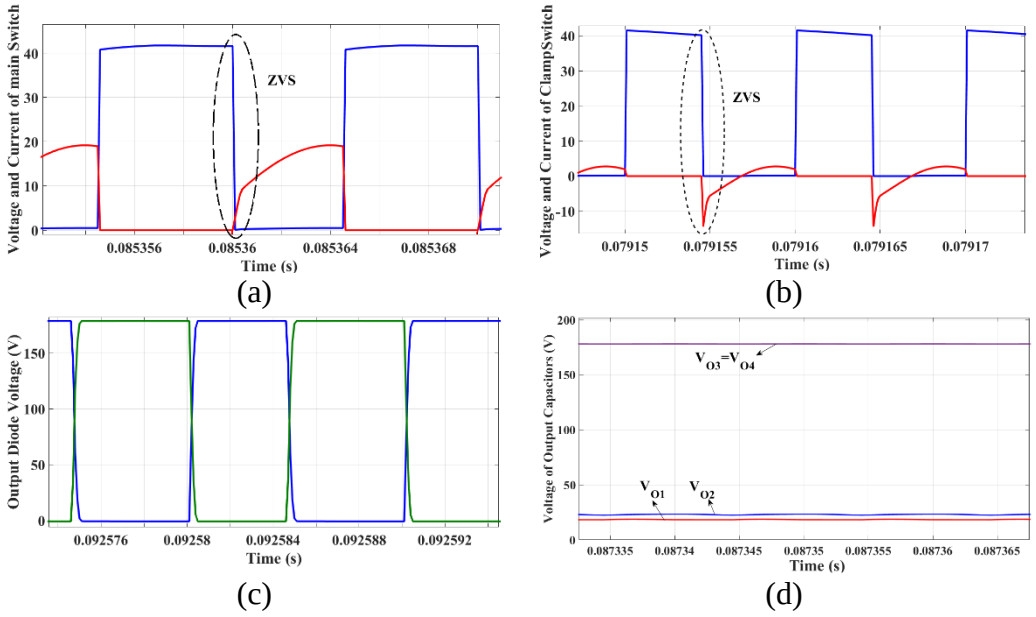


Figure 10.10: Simulation results during light loading when P = 100 W, D = 0.45, V_{in} = 22 V, and V_o = 400 V. (a) Voltage and current of the main switch; (b) voltage and current of the clamp switch. (c) voltage of the output diodes V_{Do1} and V_{DO2}; and (d) voltage of the output capacitors V_{o1}–V_{o4}.

Moreover, confirming the equations given in previous section, the voltage stress of switches is around 42 V, which is much lower than output voltage (400 V). Therefore, switches with smaller on-resistance can be used contributing to less conduction losses.

Figure 10.10(c) illustrates the voltage stress of the output diodes, which is 180 V that is much lower than the output voltage. From Figure 10.10(d), it can be seen that the voltage of capacitors is regulated enough with low ripple, implying the selection of the output capacitors are carried out correctly.

10.5.2 Experimental Results

In this section, the experimental results of implemented prototype with the specifications given in Table 10.2 are demonstrated. A photo of prototype converter is presented in Figure 10.11. The results demonstrating the performance of converter at full-load condition are shown in Figure 10.12. The gate pulse of switches is given in Figure 10.12(a), implying the driver circuit is effectively generating the signals for GaN switches. Moreover, it can be observed that there is no ringing in the gate-pulse; thus, a false turn-on or turn-off is avoided. Figure 10.12(b) demonstrates the current of boost inductor L_B and the current of leakage inductor L_k. The input current has a low ripple that proves the validity of equation given for designing the boost inductor.

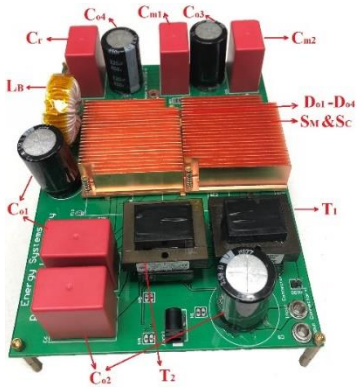


Figure 10.11: Photo of the implemented prototype.

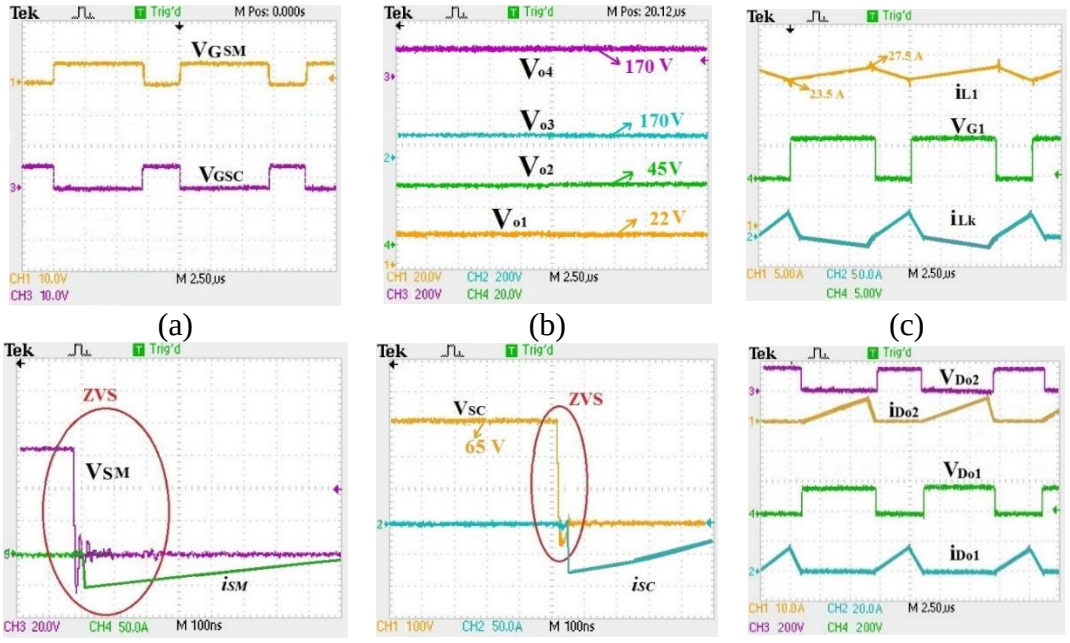


Figure 10.12: Experimental results for rated power when V_{in} = 20 V, D = 0.65, and P_{out} = 1000 W. (a) Gate-source voltage of switches S_M and S_C; (b) the voltage of output capacitors; (c) the current of boost inductor and leakage inductor, and gate pulse of main switch; (d) gate-source and drain-source voltage of switch S_M; (e) gate-source and drain-source voltage of switch S_C; and (f) the voltage and current of output diodes D_{o1} and D_{o2}.

Regarding the impact of current ripple on the efficiency and lifetime of PV source, the proposed topology can be a perfect candidate for power conversion in the PV-based DC microgrid. The voltage of output capacitors and input voltage are shown in Figure 10.12 (c). It is apparent from this figure that the voltage ripple of capacitors is in the acceptable range. Figure 10.12 (d) and (e) show the drain-source voltage and current of switches S_M and S_C, respectively. The turn-on instant clearly indicates that the voltage across switch becomes zero before the gate pulse of switch is applied, implying ZVS is achieved. This can lead to a considerable improvement in the efficiency of converter since the switching loss is the main contributor to the loss of the high step-up converters. Moreover, the voltage stress across the switches are confined properly by adopting an active-clamp configuration.

The voltage stress and the current of output diodes D_{o1} and D_{o2} are presented in Figure 10.12 (f).

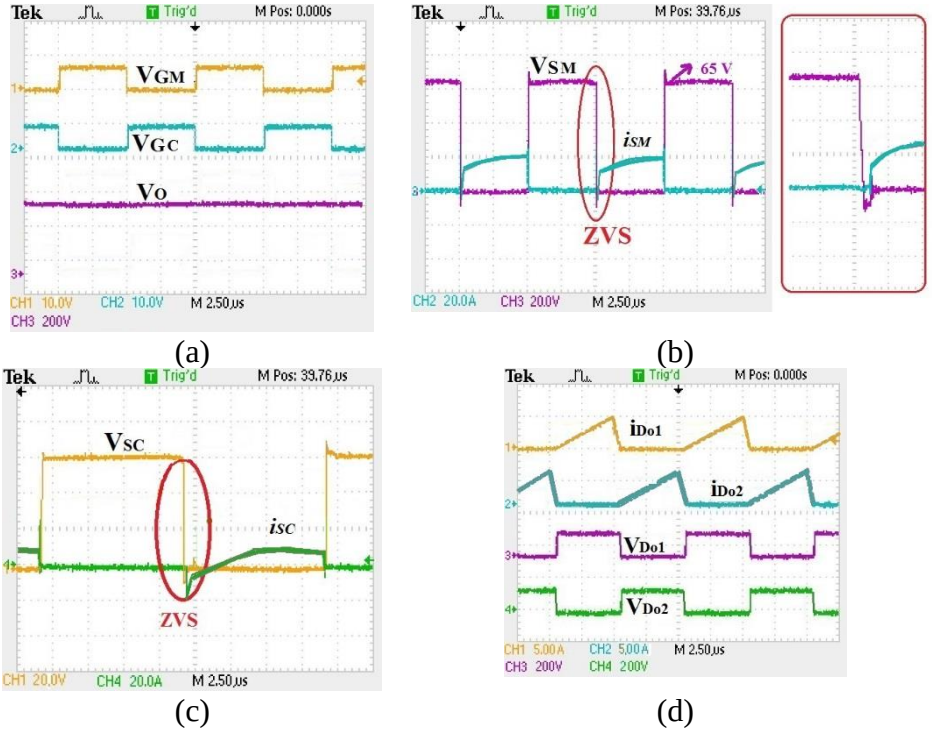


Figure 10.13: Experimental results for half load power when V_{in} = 30 V, D = 0. 5, and P_{out} = 500 W. (a) Gate-source voltage of switches S_M and S_C, and output voltage V_o; (b) gate-source and drain-source voltage of switch S_M; (c) gate-source and drain-source voltage of switch S_C; and (d) the voltage and current of output diodes D_{o1} and D_{o2}.

It is clear that the falling slope of diodes current is controlled by the leakage inductance; consequently, the turn-off loss of the diodes is reduced. Since the soft-switching realization at light load is critical for high step-up converters, the performance of converter at half of rated power is investigated. Figure 10.13 shows the results for a test done at half load (P_o = 500 W). Figure 10.13(a) demonstrates the gate pulse of switches S_M and S_C, and the output voltage V_o. It indicates that the duty cycle (D) of main switch is equal to 0.5, which

confirms the equation (31). The drain-source voltage and current of switches S_M and S_C are illustrated in Figure 10.13 (b) and (c), respectively.

The turn-on instant clearly indicates that the voltage across the switch becomes zero before the gate pulse of switch is applied. This means ZVS is obtained for this loading condition, which can greatly lead to improvement in the efficiency of converter since the switching loss is responsible for major losses of the high step-up converters, especially at light load. Figure 13d shows the voltage and currents flowing through the output diodes I_{Do1} and I_{Do2}. This figure reveals that the current of the diodes is controlled by the leakage inductance of the transformers; thus, the overlap between the voltage and current during turn-off process can be reduced. Figure 10.14 exhibits the measured and calculated efficiency using the equations given in Section 2.9. From Figure 10.14, the theoretical and measured efficiencies at full-load situation are 96.3% and 96.7%, respectively. It is noteworthy to mention that the maximum efficiencies achieved at an output power of 600 W are 97.3% and 97.1%, associated with the theoretical and measurement, respectively.

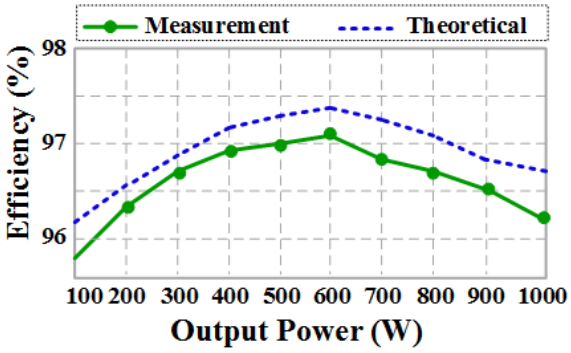


Figure 10.14: Calculated and measured efficiency versus output power.

10.6 Conclusions

A soft-switched high step-up DC/DC converter based on the dual half-bridge circuit is proposed in this chapter. Presenting a high voltage gain, as well as the soft-switching

performance for a wide range of input voltage and output power, the proposed converter is an excellent candidate for a DC/DC converter as the front-end of the inverter in DC microgrid applications. The voltage multiplier concept and dual half-bridge are combined at the output stage to increase the voltage gain and reduce the voltage stress across the switches and diodes. To suppress the voltage ringing resulting from the leakage inductance of transformers, the active-clamp circuit is adopted, thus, switches with lower rated voltage can be used. To minimize the voltage stress of output capacitors, the symmetrical voltage multiplier is implemented at the rectifier stage that can ensure the voltage distribution evenly among output diodes. Furthermore, this stage increases the voltage gain by recycling the leakage energy to the output capacitors as well. The voltage stress of switches. A comparison is carried out to show the effectiveness of the proposed topology compared to state-of-the-art converters for EV applications. A 1-kW laboratory prototype of the proposed converter is implemented using GaN E-HEMTs and SiC Schottky diodes to validate the theoretical analysis.

Chapter 11 Family of Modular Single-Stage Quasi-Resonant Inverters

11.1 Introduction

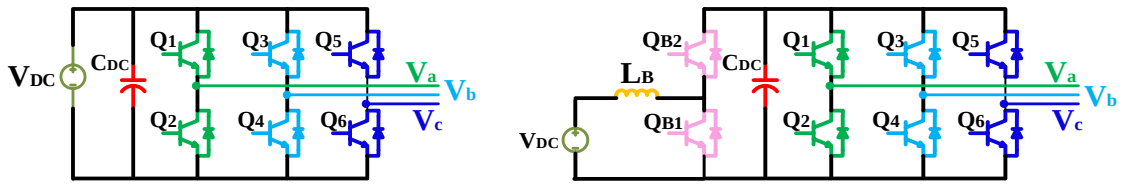
DC/AC inverters play an important role in the integration of the energy storage and renewable energy resources, hybrid DC/AC inverter for home applications, AC motor drives, electric vehicle, wherein the efficiency and power density are the vital design criteria. Up to now, voltage source inverter (VSI) and current source inverter (CSI) were the most common inverters for various applications; however, in the last few years, we have witnessed a progressively rapid pace of change, principally because of advent of Z-Source inverters. Generally, to supply the loads which need higher AC voltage, a DC/DC converter followed by a DC/AC inverter is employed, in which a bulky 60-Hz transformer is used that result in low power density. A high step-up DC/DC converter with high-frequency transformer is the second approach to reduce the size of the system. Using a high-frequency transformer in the DC/AC stage, known as high-frequency link (HFL) converters, is the third common architecture. However, the number of switches in such HFL converters is high leading to complex control circuitry. The advances in single-stage inverters, coupled with the new control technique, have the potential to give rise to a new generation of high-efficiency converters with high power density. The Modular Quasi-Resonant Inverters (MQRIs) provide high voltage gain for input source without utilizing any transformer, resulting in higher power density and higher efficiency. In the proposed family of MQRIs, a resonant circuit is employed not only to achieve soft switching for all switches but to limit the inrush current during start-up. Indeed, the resonant circuit operates like a series resonant tank but controlled by a simple pulse width modulation (PWM). So,

the proposed converters can handle the complexity of frequency modulation (FM). Moreover, because of using active-clamp configuration, the voltage stress of switches are confined; consequently, switches with small on-resistance $R_{DS(on)}$ can be used leading to increase in the efficiency.

11.2 Examples of the existing inverters

11.2.1 Three-phase Voltage Source Inverter (VSI)

As shown in Figure 11.1 (a), consisting of six switches (like MOSFETs or IGBTs) that form three legs, VSI is very simple and is used in uninterruptible power supply (UPS), electronic frequency, and adjustable speed drives, and so on. The voltage of three-phase VSI generally have the same magnitude and frequency but their phases are 120◦ apart. Any false turn-on in each leg caused either by purpose or by EMI can make the shoot-through problem that would destroy the device. Meanwhile, the magnitude of output AC voltage is limited by the voltage level of DC source. A boost converter should be added to VSI for applications with low and unregulated input voltage, therefore, to enhance the magnitude of DC voltage.



(a) (b)

Figure 11.1: schematic of Three-phase voltage source inverter. (a) buck VSI. (b) bi-directional boost VSI

11.2.2 Three-phase Z-Source Inverter (ZSI)

ZSI employs an impedance network to overcome the limitations of the conventional VSI converter which can either increase or decrease the input voltage. In other words, ZSI is a

buck-boost converter that can provide unique features in terms of having a wide range of output ac voltage. Furthermore, the shoot-through state is a fascinating characteristic of ZSI paving the way to realize the buck-boost performance. Figure 11.2(a) and Figure 11.2(b) show the unidirectional and bi-directional ZSI, respectively. Quasi-ZSI (qZSI) is a new version of ZSI which draws a continuous constant current from DC source, a vital feature to tackle with the problem of using large electrolytic capacitor in VSI. Moreover, it can handle a wide range of DC voltage as a result of buck-boost operation. Using components with lower ratings and reducing the stress of the source are the other advantage of qZSI. Figure 11.2(c) and Figure 11.2(d) demonstrates the schematic of unidirectional and bi-directional qZSI, respectively.

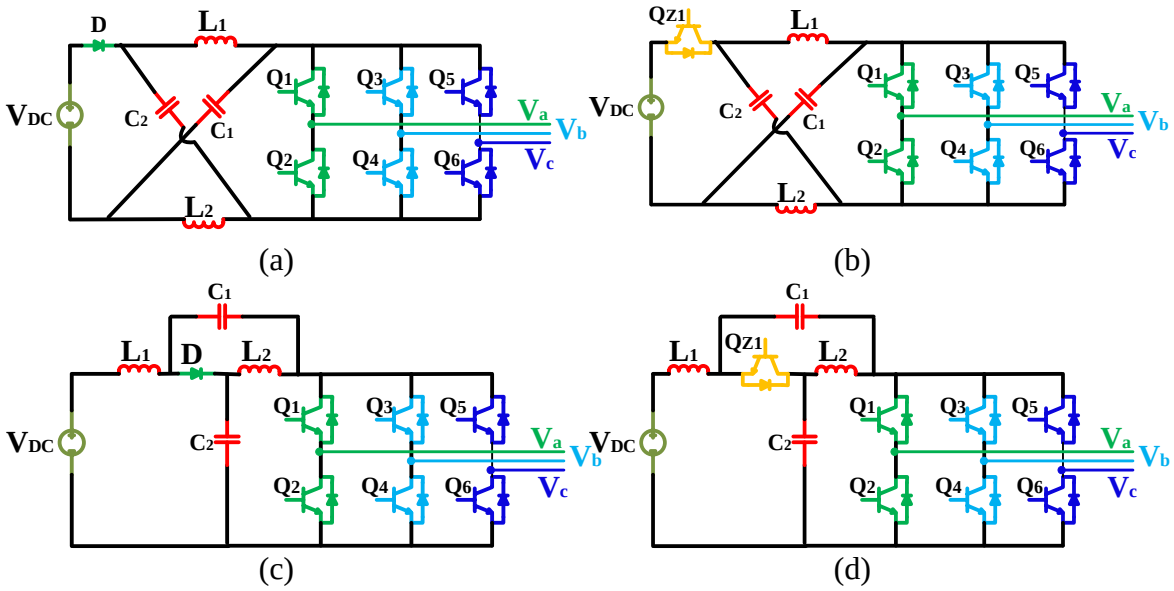
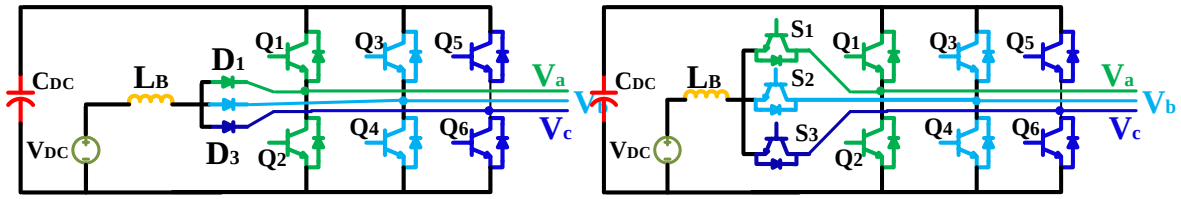


Figure 11.2: Schematic of three-phase Z-source inverter. (a) unidirectional ZSI. (b) bi-directional qZSI. (c) unidirectional qZSI. (d) bi-directional qZSI.

11.2.3 Three-phase Split-Source Inverter (SSI)

The Split-Source Inverter is derived based on the combination of three-phase SI and a conventional boost converter. It uses less number of passive components in comparison to

the ZSI. SSI utilizes the same modulation technique used in VSI, compared with ZSI that need an extra switching state. Having a filter inductor in the DC side, SSI also draws a continuous input current. Unidirectional and bi-directional SSI are shown in Figure 11.3(a) and Figure 11.3(b), respectively.



(a) (b)

Figure 11.3: Schematic of three-phase split source inverter. (a) unidirectional SSI. (b) bi-directional SSI.

11.3 The proposed Family of MQRIs

The proposed family of MQRIs is combined of half-bridge buck-boost modules to generate the high-voltage from the distributed energy resources such as PV and FC which are low, unregulated voltage sources. The modules are connected in parallel in the input side and differential-mode in the output side such that a one-phase and three-phase sinusoidal wave can be generated from two and three modules, respectively. To extend the voltage gain and reduce the voltage stress of switches, modules are placed in the cascaded configuration so that the output voltage is distributed equally across switches. Besides the cascaded configuration, the active-clamp structure limits the voltage stress across switches; thus, the switches with low rated-voltage and low on-resistance $R_{DS(ON)}$ can be employed. The switching loss is the major factor for losses in the inverters, which can be alleviated by realizing the soft-switching performance. A resonant tank is utilized to shape the current and voltage waveforms so that the soft-switching operation can be achieved. Meanwhile, the big difference with respect to the conventional resonant inverters is that the control

technique is the conventional PWM which is very simple compared to FM. In fact, the advantages of resonant circuits in terms of soft-switching realization for wide load range is attained without using FM technique.

11.4 The Proposed Family of Single-Stage Quasi-Resonant Inverters Design Directions

The concept of differential mode inverter stems from connecting dc/dc converters to generate an ac output. This method was introduced initially for synthesizing a single-phase inverter from differentially connected two bi-directional dc/dc converters [240].

Adding a dc offset is necessary in such a way that the output of each converter is either positive (non-inverting converters) or negative (inverting converters). An example of a single-phase buck-boost inverter is shown in Figure 11.5(a). The output of each converter is depicted by (1), and (2), and the differential output is depicted in (3).

Since this family of inverters are appropriate for high-density applications, such as renewable energy resources, their switching frequency is very high, more than 50 kHz; so, they should be implemented by GaN or Silicon Carbide (SiC) MOSFETs. However, regarding the small on-resistance $R_{DS(ON)}$ of GaN switches, they are superb candidates for the distributed energy resources applications.

11.5 Application Examples Using the Proposed MQRI

A family of single-stage quasi-resonant inverters is proposed which has a generalized structure- parallel connection of modules in the DC-side and the differential connection of modules in the AC-side. Based on the voltage and current level of DC-source, the members

of the proposed family of inverter can be categorized into a single-phase boost MQRI, a single-phase buck MQRI, and a three-phase boost MQRI.

11.5.1 Single-Phase Boost MQRI

A single-phase three-level boost MQRI can be synthesized with two units, wherein a source is connected as V_{DC} to the low-voltage side, and the load is connected as V_{AC} to the high-voltage side. Figure 11.4 shows a single-stage single-phase boost inverter.

The proposed inverter can be used for producing ac voltage from the renewable energy resources. As an example, a solar panel is connected to the input side of the inverter which includes two modules, as shown in Figure 11.5. In this application, a high voltage gain is the major requirement; so, a greater number of modules can be added to the proposed inverter to enhance the voltage gain ratio. For applications that input current is high and the input current ripple impact the performance of the system, such as Fuel-Cell (FC), the interleaved configuration can be utilized. Figure 11.6 shows an inverter used for FC applications. In some applications, isolation is a vital characteristic regarding the EMI issue. As shown in Figure 11.7, the proposed single-stage inverter can provide isolation to have different grounds in the input and output of the system. To provide more step-up ratio, the built-in transformer topology can be merged into the proposed MQRIs, shown in Figure 11. 8. Besides enhancing the voltage gain, the coupled inductor acts like a filter in the DC-side to reduce the current ripple. The leakage inductance of coupled-inductor can be used in combination with capacitor to form a resonant circuit resulting in soft-switching performance of switches.

11.5.2 Single-Phase Buck MQRI

Figure 11.9 shows a single-stage single-phase inverter for buck-mode operation, a source is connected as V_{DC} to the high-voltage side and the load is connected as V_{AC} to the low-voltage side, in which the output ac voltage is lower than the input dc voltage.

11.5.3 Three-Phase Boost MQRI

In Figure 11.10, a three-phase boost MQRI consisting of three single-stage quasi-resonant modules is shown, in which a source is connected as V_{DC} to the low-voltage side, and the load is connected as V_{AC} to the high-voltage side. Three single-stage quasi-resonant modules are connected in the differential mode

11.6 Advantages of The Proposed Single-Stage Quasi-Resonant Inverter

- Both modularity and the active clamp structure of proposed inverter reduce the voltage stress of switches; so, the switches with smaller on-resistance $R_{DS(ON)}$ can be used, resulting in the conduction loss decreases.
- The resonant circuit paves the way for realizing the soft-switching performance which considerably reduces the switching loss in terms of turn-on and turn-off losses.
- The flexibility of proposed inverter allows the designer to configure it for various application with different characteristics, such as high output voltage, low input current ripple, and so forth.
- The specific connection of modules removes the need for an output filter, improving the power density.
- The high voltage gain is achieved without using any transformer, contributing to increase in both power density and efficiency.

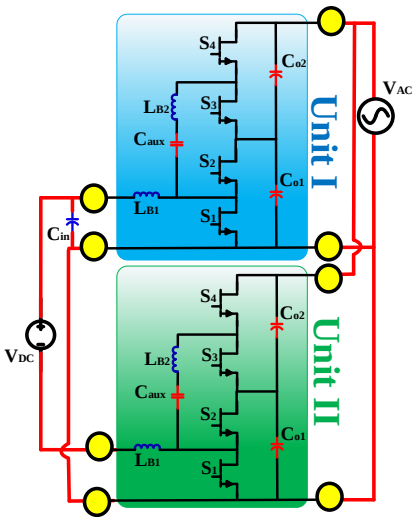


Figure 11.4: A single-phase boost version of MQRI.

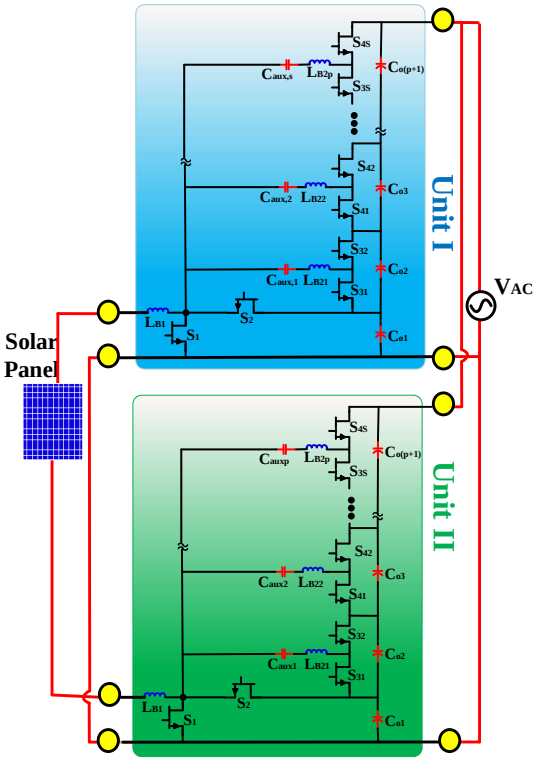


Figure 11.5: A single-phase boost MQRI with high voltage gain for low-voltage input source.

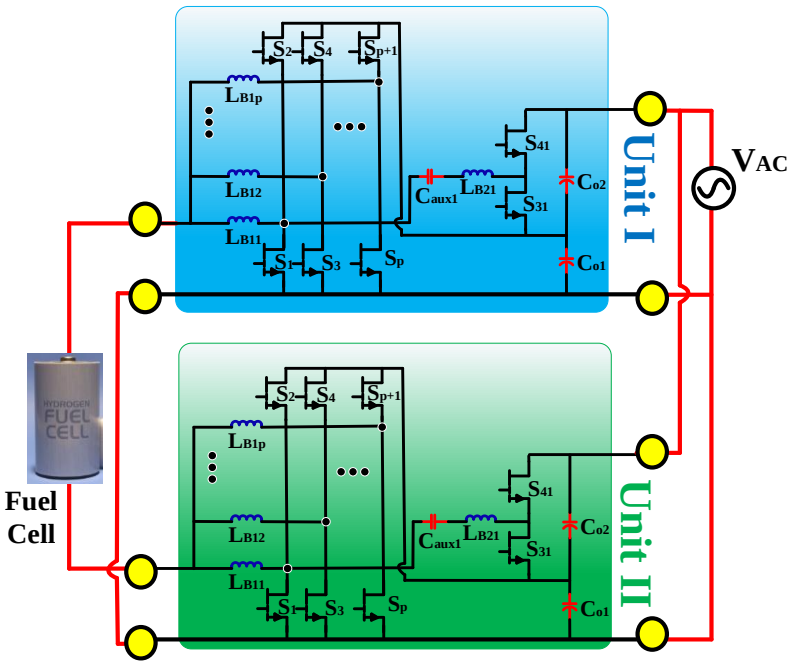


Figure 11.6: A single-phase interleaved MQRI for high-current application.

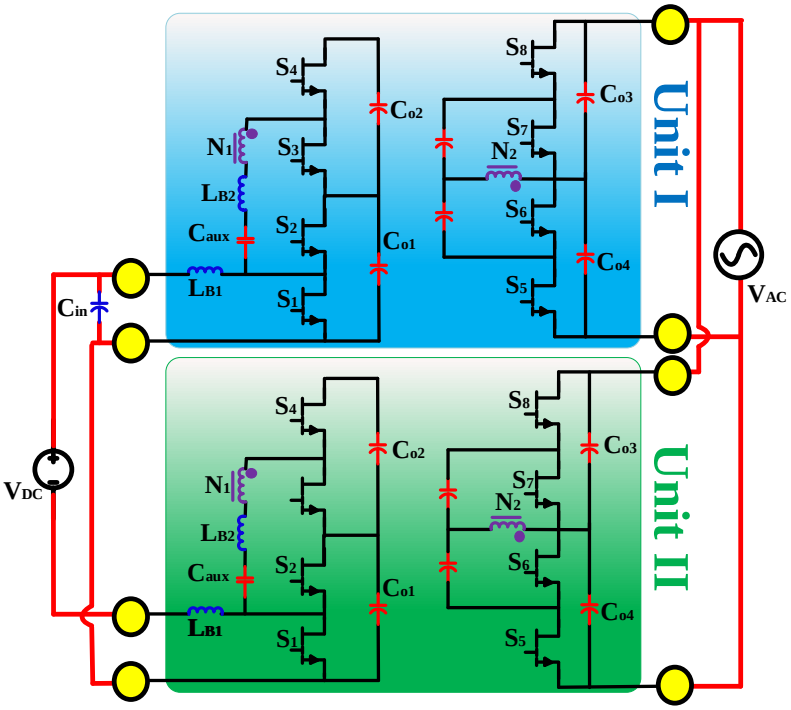


Figure 11.7: Single-phase isolated MQRI.

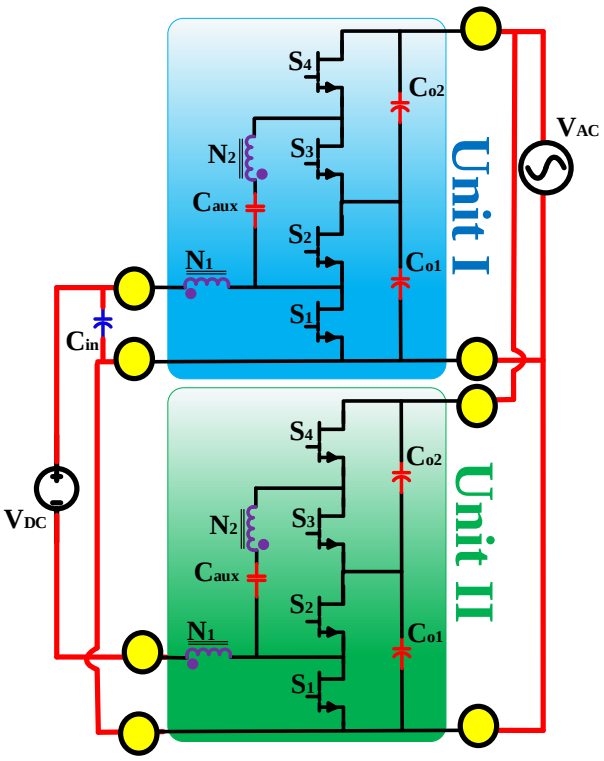


Figure 11.8: Single-phase non-isolated MQRI with built-in transformer.

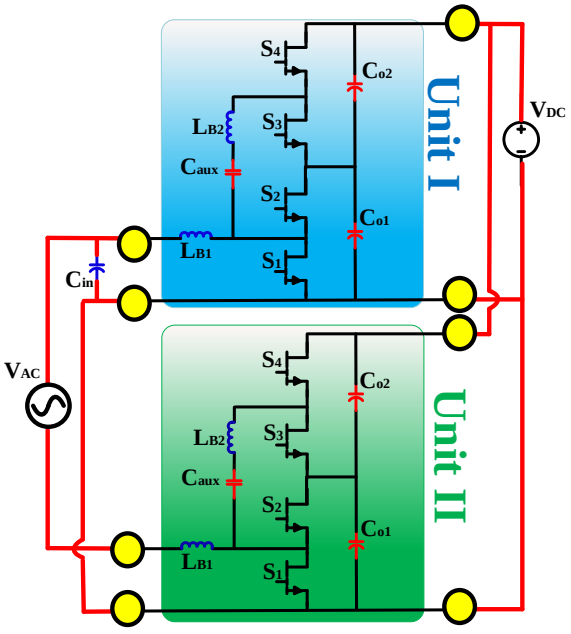


Figure 11.9: A single-phase buck version of MQRI.

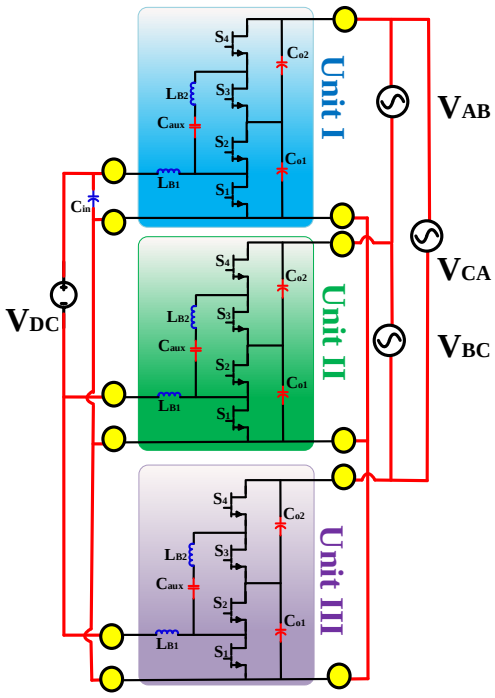


Figure 11.10: A three-phase boost version of MQRI.

11.7 Experimental Results

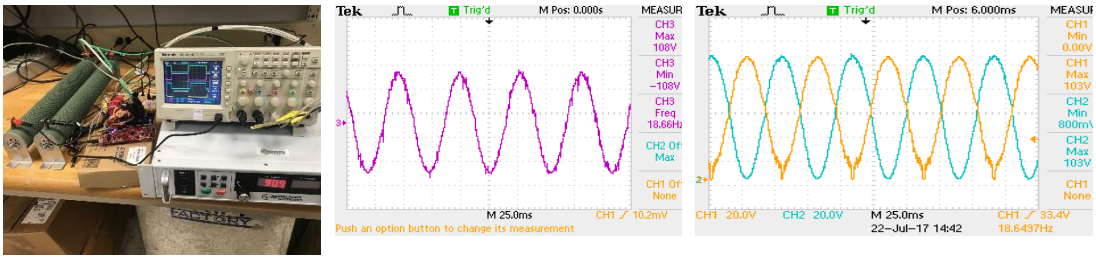
In this section, a single-phase buck version of MQRI inverter using two modular units is investigated experimentally. Figure 11.9 shows the circuit schematic, which is composed of 8 switches, two resonant inductors, two filter inductors and input and output filter capacitors. The specification of test setup is given in Table 11.1. The laboratory setup is shown in Figure 11.11(a), in which the GaN switches GS66508T from GaN Systems Inc. are employed, which has the nominal drain-source voltage of 650 V and current ratings of 30A. It is noteworthy to mention that the drain-source resistance of these switches ($R_{DS(on)}$) are 50 mΩ. In this setup, a TMS320F28377S digital signal controller is utilized to generate PWM pulses with desired switching frequency of 100 kHz.

The experimental results of the prototype are shown in Figure 11.8(b) and Figure 11.8(c). While the inverter is operating in the buck mode, as the input voltage (V_{in}) from the power

supply is equal to 90 V, the generated differential output is shown in Figure 11.11(b), with a positive peak voltage of 45 V, a negative peak voltage of -45 V, and a frequency of 190 Hz. The output voltage of each unit is shown in Figure 11.8(c).

Table 11.1: The laboratory Setup specification

Parameters	**Values**
V_{source}	190 Vpk
f_{sine_wave}	190 Hz
$Load$	10 Ω
f_s	100 kHz



(a) (b) (c)

Figure 11.11: The experimental results. (a) the setup. (b) Differential-mode output voltage of the inverter. (c) Output voltage of each converter.

11.8 Conclusion

In this chapter a family of modular quasi-resonant inverters combined of half-bridge buck-boost modules is presented. To extend the voltage gain and reduce the voltage stress of switches, modules are placed in the cascaded configuration so that the output voltage is distributed equally across switches. Moreover, the active-clamp structure limits the voltage stress across switches; thus, the switches with low rated-voltage and low on-resistance

$R_{DS(ON)}$ can be employed. The switching loss can be alleviated by realizing the soft-switching performance, which is implemented by a resonant tank. Also, the advantages of resonant circuits in terms of soft-switching realization for wide load range is attained without using frequency modulation.

Chapter 12 Conclusions and Future Work

12.1 Conclusions

In this dissertation, various techniques have been introduced to improve the efficiency and power density of the power electronics converters to employ them for different MVDC applications, such ship power system, electric vehicle powertrain, MVDC-based power grid and so on. WBG devices have been used that help to achieve these goals since they have small on-resistance, output capacitance, gate-charge, and footprint compared to their Si counterparts. Moreover, the capability to work in higher switching frequency paves the way for utilizing smaller passive components; therefore, it can improve the power density considerably.

Firstly, an extendable isolated bipolar dc-dc converter is proposed for MVDC distribution system in marine vessels, which is derived from the conventional half-bridge circuit. The active clamp circuit is adopted in the proposed converter not only to limit the voltage stress of switches but also to provide the soft-switching performance. The voltage conversion ratio is improved considerably due to employing the diode-capacitor cells. Since the short circuit fault is inevitable in the ship power system, the proposed converter can protect the system by isolating the battery side from DC-bus.

Furthermore, a family of TPTLC for hybridizing of renewable energy sources is introduced which features simple topology, low voltage stress across switches, and ZVS performance for wide load variation. It also inherits the salient advantages of the conventional ABHB converter in terms of the lower number of components, small size, and weight. The proposed stacked TPTLC is taken as an example to investigate the

correctness of the proposed concept, which has different operation scenarios based on the output power of FC and the state of the charge of battery. In the stacked TPTLC, a high voltage gain is achieved without using the transformer, which results in significantly reduced cost and size of the system. The RMS current of inductance and the boundary condition of the phase-shift controller in different operation scenarios are analyzed to find the low-conduction-loss operation mode. A control system comprised of PWM and phase-shift controlled algorithm is proposed, which provides a solution to simultaneously regulate the voltage of different ports and control the power flowing between ports.

Also, a modular, quasi-resonant bidirectional dc/dc converter has been presented as an interface between the battery and high-voltage bus in EV system. Analysis of the experimental results show the following: 1) the voltage stress of switches is reduced in proportion to the number of modules; so, switches with lower drain-source resistance can be used. 2) A resonant circuit is formed that enables the soft-switching performance even under light load condition. 3) Modularity of proposed topology helps the designer to employ the modules in such a way that different needs of various applications can be met. 4) Due to the small package, zero reverse-recovery, fast switching speed, and small gate charge, use of GaN switches brings about reduction in the losses and the size of the converter.

To improve the power density, a steep-gain interleaved bidirectional DC-DC converter with intrinsic voltage-quadrupler and reduced total switch stress has been proposed. Charging the capacitors in parallel and then delivering the energy through different paths during the discharging process is the operating principle of SGIBC in forward mode to achieve high voltage conversion ratio. On the other hand, in backward mode, the switched

capacitors are charged in series and discharged in parallel, which provides a high step-down gain. Due to the capacitive voltage divider, the voltage stress across the switches becomes smaller, which facilitates employing lower voltage rating switches. Consequently, a significant reduction in switching and conduction losses is realized. Moreover, the proposed converter possesses the built-in equal current sharing feature without adopting extra circuitry. Therefore, the proposed topology is appropriate for applications demanding bidirectional power flow with a wide voltage range, such as interfacing the UC with the dc bus in EV systems.

Additionally, magnetic integration is another solution to improve the power density, which offers a high voltage gain. The circuit integrates two coupled inductors and switched-capacitor circuit so as to improve the power density, which is suitable for applications demanding high voltage conversion ratio such as for FC-based HEV systems. To absorb the voltage spike across the switches and recycle the leakage energy to the load, a promising integrated regenerative snubber circuit is adopted. Compared to the other HSUC, the salient advantages of proposed topology are high voltage gain, small input current ripple, low voltage stress across the semiconductors, and built-in automatic current sharing. ZVS performance of switches, along with ZCS operation of diodes, paves the way for improving the efficiency of the proposed converter. As the asymmetrical pulse-width-modulation is used as a control technique, there is no complexity added to the control technique. As the diodes current is controlled by the leakage inductance, the reverse recovery problem is alleviated, and EMI noise is restrained as well.

For micro-grid application, a soft-switched high step-up DC/DC converter based on the dual half-bridge circuit is proposed. Presenting a high voltage gain, as well as the soft-

switching performance for a wide range of input voltage and output power, the proposed converter is an excellent candidate for a DC/DC converter as the front-end of the inverter in DC microgrid applications. The voltage multiplier concept and dual half-bridge are combined at the output stage to increase the voltage gain and reduce the voltage stress across the switches and diodes. To suppress the voltage ringing resulting from the leakage inductance of transformers, the active-clamp circuit is adopted, thus, switches with lower rated voltage can be used. To minimize the voltage stress of output capacitors, the symmetrical voltage multiplier is implemented at the rectifier stage that can ensure the voltage distribution evenly among output diodes. Furthermore, this stage increases the voltage gain by recycling the leakage energy to the output capacitors as well.

Finally, a family of modular quasi-resonant inverters combined of half-bridge buck-boost modules is presented. To extend the voltage gain and reduce the voltage stress of switches, modules are placed in the cascaded configuration so that the output voltage is distributed equally across switches. Moreover, the active-clamp structure limits the voltage stress across switches; thus, the switches with low rated-voltage and low on-resistance $R_{DS(ON)}$ can be employed. The switching loss can be alleviated by realizing the soft-switching performance, which is implemented by a resonant tank. Also, the advantages of resonant circuits in terms of soft-switching realization for wide load range is attained without using frequency modulation.

12.2 Recommendations for Future Work

The aim of this dissertation was to study the different techniques to improve the efficiency and power density of power converters and propose new modular topologies using WBG semiconductors, such as GaN and SiC MOSFETs. Despite the ideas and

solutions in this dissertation and the influx of research activities on the topic of using WBG devices in high voltage dc-dc systems in recent years, a number of interesting questions are yet to be addressed properly and comprehensively.

Even though GaN devices provide high efficiency power conversion, their reliability is the major concern for different applications, which is the main weakness of this study. Further works needs to be carried out to improve the reliability of the power electronics circuit using WBG devices. Additionally, further research should be undertaken to concentrate on the improving the thermal performance of these systems especially in harsh working environments. Understanding the thermal performance of integrated circuits has always been essential to avoid the overheating that can cause system malfunctions. The miniaturization of electronic systems that produces a lot of heat make the role of thermal analysis principal as a tool to provide the desired performance and reliability of circuit.

An important issue to resolve for future studies is the electromagnetic interference (EMI) performance of WBG-based circuits as their fast switching speed and the ability to operate at high frequencies brought new challenges. Future studies on the current topic are therefore required, including WBG devices influence on noise sources, noise propagation paths, EMI reduction techniques, and EMC reliability issues.

Developing an optimization-oriented design approach for extending the modular circuit is a vital issue for future research. The number of boost half-bridge modules and the input current ripple need to be selected based on a trade-off between the converter efficiency and cost. A high number of modules lead to further reduction in the input current ripple, as well as extended power level However, more inductors, switches, capacitors, and driving circuitry are required, which results in higher cost.

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VITA

HADI MORADISIZKOOHI

Born, Karaj, Iran

2006-2010	B.S., Electrical Engineering University of Guilan Guilan, Iran
2011-2013	M.S., Electrical Engineering Amirkabir University of Technology Tehran, Iran
2018-2019	Teaching Assistant of the Year Award Florida International University Miami, Florida
2018-2020	Doctoral Candidate Florida International University Miami, Florida

PUBLICATIONS AND PRESENTATIONS

- H. Moradisizkoohi, N. Elsayad, and O. Mohammed, "A Family of Three-Port Three-Level Converter Based on Asymmetrical Bidirectional Half-Bridge Topology for Fuel-Cell Electric Vehicle Applications", IEEE Transactions on Power Electronics.
- H. Moradisizkoohi, N. Elsayad, and O. Mohammed, "PWM Plus Phase-Shift Modulated Three-Port Three-Level Soft-Switching Converter Using GaN Switches for Photovoltaic Applications", IEEE Journal of Emerging and Selected Topics in Power Electronics.
- H. Moradisizkoohi, N. Elsayad, and O. Mohammed, "An Integrated Interleaved Ultra High Step-Up DC-DC Converter Using Dual Cross-Coupled Inductors with Built-in Input Current Balancing for Electric Vehicles", IEEE Journal of Emerging and Selected Topics in Power Electronics.
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- N. Elsayad, H. Moradisizkoohi, and O. Mohammed, "Design and Implementation of a New Transformerless Bidirectional DC-DC Converter with Wide Conversion Ratios", IEEE Transactions on Industrial Electronics.