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OPTIMAL TILE-BASED DNA SELF-ASSEMBLY DESIGNS FOR LATTICE GRAPHS AND PLATONIC SOLIDS

LEYDA ALMODÓVAR, JO ELLIS-MONAGHAN, AMANDA HARSY, CORY JOHNSON, AND JESSICA SORRELLS

1. INTRODUCTION

This paper is a repository to supplement the results presented in [1]. We exhibit a collection of tile-based DNA self-assembly proofs for specific graphs, namely Platonic solids, square lattice graphs, and triangular lattice graphs. We find the minimum number of tile types and bond-edge types needed in all scenarios for the octahedron and icosahedron and we find partial results, i.e. bounds, for the do-decahedron. Note that the tetrahedron is a complete graph so those results were presented in [3] and full results on the hexahedron are presented in our paper [1]. We also obtain partial results for lattice graphs in Scenarios 2 and 3. Note that the notation and terminology presented here are consistent with the notation presented in [1].

2. Square Lattices

We follow the convention given in [1] that an $m \times n$ square lattice graph is the graph Cartesian product $P_m \times P_n$ of path graphs on m and n vertices, where #V(G) = mn and there are (m-1)(n-1) total 4-cycles. Results for all dimensions of square lattice graphs in Scenario 1 are provided in [1]. In this section we provide Scenario 2 and 3 results for a square lattice graph of specific dimensions, 2×3 . Optimal values for Scenarios 2 and 3 for larger dimensions remain an open problem.

Proposition 1. Let G be the 2×3 square lattice graph. Then $B_2(G) = 2$ and $T_2(G) = 4$.

Proof. By Theorem 2 in [3], $T_2(G) \ge 3$. If $G \in \mathcal{O}(P)$ with #P = 3, then P either consists of two 3-armed tile types and one 2-armed tile type, or two 2-armed tile types and one 3-armed tile type.

Suppose there is only one 2-armed tile type in P. Since the degree 2 vertices are adjacent, the tile must be of the type $\{a, \hat{a}\}$. However, a pot with this tile type realizes a graph of order 1. Hence, there cannot be only one 2-armed tile type.

Suppose there is only one 3-armed tile type in P. The two degree 3 vertices are adjacent, so the tile must both have a hatted and an un-hatted cohesive-end of the same type. Then, without loss of generality, this tile is of type $\{a, \hat{a}, b\}$, where b may or may not be distinct from a. Any possible labeling of the graph using this tile for both degree 3 vertices results in either three 2-armed tile types (i.e. #P = 4) or a 2-armed tile type that realizes a graph of order 1. Therefore $T_2(G) \ge 4$.

Note that $B_2(G) \neq 1$, as this would either result in a tile type of the form $\{a, \hat{a}\}$, which can realize a graph of order 1, or in two tile types of the form $\{a, a\}$ and $\{\hat{a}, \hat{a}\}$, which can realize a graph of order 2. Therefore $B_2(G) \geq 2$.

The following pot realizes G:

(1)
$$P = \left\{ \{a, b\}, \{a, \hat{b}\}, \{\hat{a}^2, b\}, \{\hat{a}^2, \hat{b}\} \right\}$$

The spectrum of P follows:

$$\mathcal{S}(P) = \left\{ \frac{1}{6r} \langle r+t, 3r-t, 2r-t, t \rangle \ \middle| \ r \in \mathbb{Z}^+, t \in (\mathbb{Z} \cap [-r, 2r]) \right\}.$$

It can be verified by hand or by the program outlined in [1] that for all $H \in \mathcal{O}(P), \#V(H) \geq 6$. Specifically, V(H) = 6 occurs when r = 1 and $t \in \{0, 1, 2\}$. \Box

Proposition 2. Let G be the 2×3 square lattice graph. Then $B_3(G) = 3$ and $T_3(G) = 4$.

Proof. By Proposition 1, $B_2(G) = 2$ and $T_2(G) = 4$; thus $B_3(G) \ge 2$ and $T_3(G) \ge 4$. Note that the pot P given in Equation (1) will not satisfy Scenario 3, as there exists a graph $H \in \mathcal{O}(P)$ such that $H \not\cong G$. Such a graph H can be realized with tile distribution $R_1 = 1, R_2 = 3, R_3 = 2, R_4 = 0$, in which H contains both a multiple-edge and a 3-cycle.

We argue that $B_3(G) > 2$. Consider the vertex labeling of G provided in Figure 1. Suppose $\lambda(v_1, \{v_1, v_2\}) = a$. Then $\lambda(v_5, \{v_5, v_4\}) \neq a$, otherwise a non-isomorphic



FIGURE 1. Vertex labeling of 2×3 square lattice for Proposition 2

graph with multiple-edges can be realized.

Case 1: Suppose $\lambda(v_4, \{v_4, v_5\}) = a$. Then $\lambda(v_1, \{v_1, v_4\}) \neq a$, $\lambda(v_4, \{v_4, v_1\}) \neq a$, $\lambda(v_2, \{v_2, v_5\}) \neq a$, and $\lambda(v_5, \{v_5, v_2\}) \neq a$, otherwise a graph with loops can be realized. Without loss of generality, let $\lambda(v_1, \{v_1, v_4\}) = b$. Then $\lambda(v_2, \{v_2, v_5\}) \neq b$ and $\lambda(v_5, \{v_5, v_2\}) \neq b$, otherwise a graph with a 5-cycle can be realized. Thus, this assembly design would require at least 3 bond-edge types.

Case 2: Without loss of generality, suppose $\lambda(v_4, \{v_4, v_5\}) = b$. Then, to avoid realizing a graph with loops, $\lambda(v_1, \{v_1, v_4\}) = a$ or $\lambda(v_4, \{v_4, v_1\}) = b$. These cases are symmetric, so without loss of generality let $\lambda(v_1, \{v_1, v_4\}) = a$. As noted in Case 1, $\lambda(v_2, \{v_2, v_5\}) \neq a$, and $\lambda(v_5, \{v_5, v_2\}) \neq a$, as otherwise a graph with a loop or multiple-edge can be realized. For the same reason, $\lambda(v_5, \{v_5, v_2\}) \neq b$. Thus, the only choice without introducing a new bond-edge type is $\lambda(v_2, \{v_2, v_5\}) = b$. The edge $\{v_2, v_3\}$ cannot be labeled with either bond-edge type a or b, in either orientation, without the possible realization of a graph with a loop or multiple-edge. Thus, this labeling would require 3 bond-edge types.

In each case, 2 bond-edge types is insufficient to satisfy the restrictions in Scenario 3. Thus, $B_3(G) > 2$.

The pot $P=\left\{\{a,\hat{c}\},\{\hat{b},c\},\{\hat{a}^3\},\{a,b^2\}\right\}$ realizes G and has spectrum

$$\mathcal{S}(P) = \left\{ \frac{1}{6r} \left\langle 2r, 2r, r, r \right\rangle \middle| r \in \mathbb{Z}^+ \right\}.$$

Since a graph of order 6 must use tile distribution $R_1 = 2, R_2 = 2, R_3 = 1, R_4 = 1$, it is straightforward to verify that no non-isomorphic graphs of order 6 can be realized. Thus $B_3(G) = 3$ and $T_3(G) = 4$.

3. TRIANGLE LATTICE GRAPHS

We follow the convention given in [1] that the $m \times n$ triangular lattice graph is the graph Cartesian product $P_m \times P_n$ of path graphs on m and n vertices with diagonal edges from the bottom left to the top right of each square. That is, if the vertices of the square lattice are integer Cartesian coordinates, then the diagonal edges are in between coordinates (i, j) and (i + 1, j + 1). The number of 3-cycles is 2(m-1)(n-1) and #V(G) = mn. In Proposition 3 we provide results in Scenario 1 for such triangle lattice graphs of nearly all sizes $m \times n$. An example of the 2×3 triangular lattice graph in Scenario 3 is given in [1].

Proposition 3. Let G be a $m \times n$ triangle lattice graph such that m > 3, n > 3. Then $T_1(G) = 5$ for $\{m, n\} \notin \{\{5, 5\}, \{5, 7\}, \{5, 9\}, \{5, 11\}, \{5, 13\}, \{7, 7\}\}.$

Proof. Note that the valency sequence of G is (2, 3, 4, 6), so $4 \leq T_1(G) \leq 5$. Assume $G \in \mathcal{O}(P)$ with #P = 4. Let $t_1 \in P$ denote the 2-armed tile type, $t_2 \in P$ denote the 3-armed tile type, $t_3 \in P$ denote the 4-armed tile type, and $t_4 \in P$ denote the 6-armed tile type. Note that in G there are always two vertices of degrees two and three, 2(m + n - 4) vertices of degree four, and (m - 2)(n - 2) vertices of degree six.

The following equation must be satisfied:

(2) $2z_{1,1} + 2z_{1,2} + 2(m+n-4)z_{1,3} + (m-2)(n-2)z_{1,4} = 0$, where $m, n \in \mathbb{Z}^+$

Note that in G with m > 3, n > 3 degree four vertices are adjacent to one another and degree six vertices are adjacent to one another (i.e. each tile type contains at least one a and \hat{a}), so $z_{1,3} \in \{0, \pm 2\}$ and $z_{1,4} \in \{0, \pm 2, \pm 4\}$. In addition, $z_{1,2} \in \{0, \pm 2\}$ and $z_{1,3} \in \{\pm 1, \pm 3\}$. Given these limited options, the only integer pair solutions (m, n) to equation (2) are (5, 5), (7, 7), (5, 7), (7, 5), (5, 9), (9, 5), (5, 11), (11, 5), (5, 13), (13, 5). Therefore, if (m, n) is not one of these integer pairs, no possible pot P with #P = 4 will realize G. Hence, $T_1(G) = 5$. Algorithm 1 from [3] will produce such a pot.

Remark 4. For triangle lattice graphs G with dimensions m = 3, n = 3, or $\{m, n\} \in \{\{5, 5\}, \{5, 7\}, \{5, 9\}, \{5, 11\}, \{5, 13\}, \{7, 7\}\}$, it remains true that $4 \leq T_1(G) \leq 5$. Work on these particular dimensions of triangle lattice graphs is still in progress.

3.1. Alternative Types of Triangle Lattice Graphs. Another way to consider and construct triangle lattice graphs, as seen in [2], is to call the $m \times n$ lattice graph the lattice consisting of m - 1 rows of 3-cycles and n 3-cycles in each row. Some triangle lattice graphs of this form are isomorphic to graphs constructed with the definition of triangle lattice given in [1], but others are non-isomorphic. When constructing lattices with this strategy, more difficulties arise and the values for T_1 vary greatly depending on the values of m and n. In Propositions 5, 6, and



FIGURE 2. Assembly design of 3×6 triangle lattice graph in Scenario 1

7 we provide full results in Scenario 1 for triangle lattice graphs of this type for the case m = 3 and partial results for the case m = 4. Other results for triangular lattice graphs of this type in Scenario 1 are given in [2]. To distinguish the following triangle lattice graphs from those above and in [1], we will explicitly mention the number of triangles per row.

Proposition 5. Let G be a $3 \times n$ triangle lattice graph with n > 4 triangles per row. Then

$$T_1(G) = \begin{cases} 4 & \text{if } n \text{ is odd and } n \neq 7,11 \\ 5 & \text{if } n \text{ is even} \end{cases}$$

Proof. Suppose n is odd. Note that the valency sequence of G is (3, 4, 6), so $3 \leq T_1(G) \leq 4$. Assume $G \in \mathcal{O}(P)$ with #P = 3. Let $t_1 \in P$ denote the 3-armed tile type, $t_2 \in P$ denote the 4-armed tile type, and $t_3 \in P$ denote the 6-armed tile type. Note that in G there are always six vertices of degree 3 and (n-3) vertices of degree 4.

The following equation must be satisfied:

(3)
$$6z_{1,1} + (n-3)z_{1,2} + mz_{1,3} = 0$$
, where $m, n \in \mathbb{Z}^+$

Note that in G each tile type is adjacent to itself (i.e. each tile type contains at least one a and \hat{a}), so $z_{1,1} \in \{\pm 1\}$, $z_{1,2} \in \{0, \pm 2\}$ and $z_{1,3} \in \{0, \pm 2, \pm 4\}$. If n = 4k + 1, then m = 2k and if n = 4k + 3 then m = 2k + 1. Note that if m = 2k, then Equation (3) has no integer solutions given that (n - 3) is even and $z_{1,1} \in \{\pm 1\}$. If m = 2k + 1, then n > 11 by assumption, so n - 3 > 8 and k > 2. Then, the equation becomes

(4)
$$6z_{1,1} + (n-3)z_{1,2} + (2k+1)z_{1,3} = 0.$$

It is straightforward to verify from Equation (4) that no possible pot P with #P = 3 will realize G. Hence, $T_1(G) = 4$. Algorithm 1 from [3] will produce such a pot.

Now, suppose *n* is even. Note that the valency sequence of *G* is (2, 3, 4, 5, 6), so $5 \leq T_1(G) \leq 7$. The pot $P = \{\{a, \hat{a}\}, \{a^2, \hat{a}\}, \{a^2, \hat{a}^2\}, \{a, \hat{a}^4\}, \{a^3, \hat{a}^3\}\}$ will realize *G*. Hence, $T_1(G) = 5$. An example labeling for the case n = 6 is shown in Figure 2. Note that only one bond-edge type is necessary in Scenario 1 so arrows alone are used to indicate the labeling.



FIGURE 3. Assembly design of 3×7 triangle lattice graph in Scenario 1

Proposition 6. Let G be a $3 \times n$ triangle lattice graph with n triangles per row. Then

$$T_1(G) = \begin{cases} 2 & \text{if } n = 3\\ 3 & \text{if } n = 1, 2, 7, 11 \end{cases}$$

Proof. The case where n = 1 follows from [2]. The case where n = 3 follows from [5]. When n = 2, G has vertices of degrees 2, 3, and 5. From [3], $3 \le T_1(G) \le 4$ and the pot $P = \{\{a, \hat{a}\}, \{a^2, \hat{a}\}, \{a, \hat{a}^4\}\}$ realizes the graph.

When n = 7 or 11, G has valency sequence (3, 4, 6). By $[3], 3 \le T_1(G) \le 4$. The pots $P = \{\{a^2, \hat{a}\}, \{a^2, \hat{a}^2\}, \{a^2, \hat{a}^4\}\}$ and $P = \{\{a^2, \hat{a}\}, \{a, \hat{a}^3\}, \{a^4, \hat{a}^2\}\}$ realize G for n = 7 and n = 11, respectively. An example when n = 7 is shown in Figure 3. Note that all edges are labeled with only one bond-edge type so arrows alone are used to indicate labeling in this figure.

Proposition 7. Let G be a $4 \times n$ triangle lattice graph with n > 2 triangles per row and n even. Then $T_1(G) = 6$.

Proof. Note that the valency sequence of G is (2, 3, 4, 5, 6), so $5 \leq T_1(G) \leq 7$. Assume $G \in \mathcal{O}(P)$ with #P = 5. Let $t_1 \in P$ denote the 2-armed tile type, $t_2 \in P$ denote the 3-armed tile type, $t_3 \in P$ denote the 4-armed tile type, $t_4 \in P$ denote the 5-armed tile type, and $t_5 \in P$ denote the 6-armed tile type. In G, there are always two vertices of degree 2, four vertices of degree 3, and two vertices of degree 5. Therefore, in any assembly pot constructing G there are 2 tiles of type t_1 , 4 tiles of type t_2 , and 2 tiles of type t_4 . Since n is even, there are (n-2) tiles of type t_3 and (n-2) tiles of type t_5 . The following equation must be satisfied:

(5)
$$2z_{1,1} + 4z_{1,2} + (n-2)z_{1,3} + 2z_{1,4} + (n-2)z_{1,5} = 0.$$

Note that in *G* each tile type is adjacent to itself except t_1 and t_4 , so $z_{1,1} \in \{0, \pm 2\}, z_{1,2} \in \{\pm 1\}, z_{1,3} \in \{0, \pm 2\}, z_{1,4} \in \{\pm 1, \pm 3, \pm 5\}$, and $z_{1,5} \in \{0, \pm 2, \pm 4\}$. Hence, Equation (5) will have no integer solutions since every term is divisible by 4 except $2z_{1,4}$. The pot $P = \{\{a, \hat{a}\}, \{a^2, \hat{a}\}, \{a, \hat{a}^2\}, \{a^2, \hat{a}^2\}, \{a^2, \hat{a}^3\}, \{a^3, \hat{a}^3\}\}$ realizes *G*. Thus $T_1(G) = 6$.

4. Platonic Solids

Previously the only known results for platonic solid graphs in a flexible tilebased self-assembly model were for the tetrahedron, K_4 [3]. In [1] full results for the hexahedron (cube) graph are given in all three scenarios. In this section we provide full results for the octahedron and icosahedron graphs, as well as partial results for the dodecahedron graph.

4.1. Octahedron. Let G be the octahedron. Then $B_1(G) = 1$ for all graphs G [3]. The octahedron is a 4-regular graph, so $T_1(G) = 1$. Algorithm 1 of [3] yields a pot of tiles realizing G.

Proposition 8. Let G be the octahedron. Then $T_2(G) = 3$ and $B_2(G) = 2$.

Proof. Since G is 4-regular, $P = \{\{a^2, \hat{a}^2\}\}$ is the only pot such that #P = 1 and $G \in \mathcal{O}(P)$. However, P constructs a graph of order 1, so $T_2(G) > 1$. Suppose $T_2(G) = 2$. Since $B_2(G) + 1 \leq T_2(G)$, this implies $B_2(G) = 1$. Without loss of generality and to avoid a pot that realizes graphs of orders 1 or 2, $P = \{\{a^4\}, \{a, \hat{a}^3\}\}$. However, this pot realizes a graph of order 3. Hence, $B_2(G) > 1$ and $T_2(G) > 2$. The pot $P = \{\{a^3, b\}, \{\hat{a}^2, b, \hat{b}\}, \{b, \hat{b}^3\}\}$ realizes G and

$$\mathcal{S}(P) = \left\{ \frac{1}{6r} \left\langle 2r, 3r, r \right\rangle \middle| r \in \mathbb{Z}^+ \right\}.$$

The spectrum of P shows for all $H \in \mathcal{O}(P)$, $\#V(H) \ge 6$. Thus, $T_2(G) = 3$ and $B_2(G) = 2$.

Proposition 9. Let G be the octahedron. Then $T_3(G) = 5$.



FIGURE 4. Vertex labeling of octahedron graph for Propositions 9 and 10

Proof. Let λ be an assembly design for the octahedron graph and let $\lambda(v_1) = t_1$ using the vertex labeling shown in Figure 4. No vertices adjacent to v_1 can be labeled with t_1 [3]. Let $\lambda(v_6) = t_6$. To minimize the number of tile types, suppose $t_1 = t_6$, and without loss of generality assume $\lambda(v_1, \{v_1, v_2\}) = a$. Then $\lambda(v_6, \{v_6, v_3\}) \neq a$, $\lambda(v_6, \{v_6, v_4\}) \neq a$, and $\lambda(v_6, \{v_6, v_5\}) \neq a$, otherwise a graph with a multiple-edge can be realized. Thus $\lambda(v_6, \{v_6, v_2\}) = a$. Now, $\lambda(v_1, \{v_1, v_3\}) \neq a, \lambda(v_1, \{v_1, v_4\}) \neq a$, and $\lambda(v_1, \{v_1, v_5\}) \neq a$, otherwise a graph with a multiple-edge can be realized. By similar repeated reasoning, t_1 must contain four distinct bond-edge types. Let $t_1 = \{a, b, c, d\}$ such that $\lambda(v_1, \{v_1, v_3\}) = b, \lambda(v_1, \{v_1, v_4\}) = c$, and

 $\lambda(v_1, \{v_1, v_5\}) = d$. To avoid the possibility of P realizing graphs with multipleedges, this labeling forces $\lambda(v_6, \{v_6, v_3\}) = b, \lambda(v_6, \{v_6, v_4\}) = c$, and $\lambda(v_6, \{v_6, v_5\}) = d$. Now, if $\lambda(v_2) = \lambda(v_5)$ or if $\lambda(v_3) = \lambda(v_4)$ (the only other possibilities for repeated tiles [3]), then a graph can be realized with multiple-edges. Thus, all four remaining vertices must be labeled with distinct tile types (i.e. $T_3(G) \ge 5$). The following pot realizes G

(6)
$$P = \left\{ \{a, b, c, d\}, \{\hat{a}^4\}, \{\hat{d}^4\}, \{a, \hat{b}^2, d\}, \{a, \hat{c}^2, d\} \right\},$$

and the spectrum of P is

$$\mathcal{S}(P) = \left\{ \frac{1}{6r} \left\langle 2r, r, r, r, r \right\rangle \middle| r \in \mathbb{Z}^+ \right\}.$$

The spectrum of P shows for all $H \in \mathcal{O}(P)$, $\#V(H) \ge 6$. It is straightforward to verify that no non-isomorphic graphs are realized by this pot when $R_1 = 2, R_2 = 1, R_3 = 1, R_4 = 1, R_5 = 1$. Thus $T_3(G) = 5$.

Proposition 10. Let G be the octahedron. Then $B_3(G) = 4$.

Proof. As proven in Proposition 8, $B_2(G) = 2$, so $B_3(G) \ge 2$. Suppose $B_2(G) \le 3$. Let λ be an assembly design of G. Since #E(G) = 12, then one bond-edge type must be used at least four times in the assembly design of G. Consider the vertex labeling of G given in Figure 4. Let $\lambda(v_1) = t_1$ and $\lambda(v_2) = t_2$. Suppose $\lambda(v_1, \{v_1, v_2\}) = a$. In order to avoid realizing a graph with loops or multipleedges, there are six edges remaining that can be labeled with bond-edge type a: $\{v_1, v_4\}, \{v_1, v_5\}, \{v_1, v_3\}, \{v_2, v_4\}, \{v_2, v_6\}, \{v_2, v_3\}$. An additional cohesive-end a on t_1 or an additional cohesive-end \hat{a} on t_2 are equivalent cases. Suppose without loss of generality $\lambda(v_1, \{v_1, v_4\}) = a$ (choice of other half-edges results in analogous cases). In order to avoid realizing a graph with multiple-edges or loops, if $a^m \in t_1$ where m > 1, then $\hat{a}^n \notin t_2$ for any n > 1. Let $\lambda(v_1, \{v_1, v_3\}) = a$ and $\lambda(v_1, \{v_1, v_5\}) = a$. Now four edges of G are labeled with bond-edge type a and no edges remain that can be labeled with a. Suppose $\lambda(v_2, \{v_2, v_4\}) = b$. Edges $\{v_3, v_5\}, \{v_3, v_6\}, \text{ and } \{v_5, v_6\}$ cannot be labeled with bond-edge type b, otherwise a graph with a loop or multiple-edge can be realized. However, these three edges cannot simultaneously be labeled with a third bond-edge type c either, as a graph with a loop on vertex v_4, v_5 , or v_6 can be realized. Thus $B_3(G) \ge 4$. The pot given in Equation (6) realizes G, so $B_3(G) = 4$.

4.2. **Icosahedron.** The icosahedron is a 5-regular graph, so $T_1(G) = 2$ and $B_1(G) = 1$ [3]. Algorithm 1 of [3] yields a pot of tiles realizing G.

Proposition 11. Let G be the icosahedron. Then $T_2(G) = 3$ and $B_2(G) = 2$.

Proof. Suppose $T_2(G) = 2$. Since $B_2(G) + 1 \leq T_2(G)$, this implies $B_2(G) = 1$. Without loss of generality and to avoid a pot that realizes graphs of order 2, there are three possible pots of tiles: $P_1 = \{\{a^5\}, \{a, \hat{a}^4\}\}, P_2 = \{\{a^5\}, \{a^2, \hat{a}^3\}\}$, or $P_3 = \{\{a^4, \hat{a}\}, \{a^2, \hat{a}^3\}\}$. However, P_1 realizes a graph of order 8, P_2 realizes a graph of order 6, and P_3 realizes a graph of order 4. Hence, $B_2(G) > 1$ and $T_2(G) > 2$. The pot $P = \{\{a^3, b^2\}, \{a, \hat{a}^3, b\}, \{a, \hat{a}, b, \hat{b}^2\}\}$ realizes G (see Figure 6) and

$$\mathcal{S}(P) = \left\{ \frac{1}{12r} \left\langle 2r, 3r, 7r \right\rangle \middle| r \in \mathbb{Z}^+ \right\}.$$



FIGURE 5. Vertex labeling of icosahedron graph for Propositions 11, 12, 13

The spectrum of P shows for all $H \in \mathcal{O}(P)$, $\#V(H) \ge 12 = \#V(G)$. Thus, $T_2(G) = 3$ and $B_2(G) = 2$.



FIGURE 6. Assembly design of icosahedron graph for Proposition 11

Proposition 12. Let G be the icosahedron. Then $T_3(G) = 12$.

Proof. Let λ be an assembly design for the icosahedron graph and let $\lambda(v_1) = t_1$ using the vertex labeling shown in Figure 5. No vertices adjacent to v_1 can be labeled with t_1 [3].

Suppose $\lambda(v_6) = t_1$. By the symmetry of the icosahedron, this is analogous to $\lambda(v_i) = t_1$ for i = 7, 8, 10 or 12 since each of these vertices are distance 2 from v_1 . Suppose $\lambda(v_1, \{v_1, v_2\}) = a$. Then $\lambda(v_6, \{v_6, v_2\}) = a$, else a graph with a multipleedge can be realized. Now, $\lambda(v_1, \{v_1, v_3\}) \neq a, \lambda(v_1, \{v_1, v_4\}) \neq a, \lambda(v_1, \{v_1, v_5\}) \neq a$, and $\lambda(v_1, \{v_1, v_9\}) \neq a$, otherwise a graph with a multiple-edge can be realized. Suppose $\lambda(v_1, \{v_1, v_5\}) = b$. By previous reasoning, $\lambda(v_6, \{v_6, v_5\}) = b$ and no other edge incident to v_1 may be labeled with bond-edge type b. Suppose $\lambda(v_1, \{v_1, v_4\}) = c$. Then either $\lambda(v_6, \{v_6, v_7\}) = c, \lambda(v_6, \{v_6, v_{10}\}) = c$, or $\lambda(v_6, \{v_6, v_{11}\}) = c$. However, each of these possibilities can result in a non-planar, non-isomorphic graph (see Figure 7). Thus, $\lambda(v_6) \neq t_1$.



FIGURE 7. Example of non-isomorphic graph formed in proof of Proposition 12

Now suppose $\lambda(v_{11}) = t_1$ and suppose $\lambda(v_1, \{v_1, v_2\}) = a$. It can be verified through *Maple* that a non-planar, non-isomorphic graph can be realized if $\lambda(v_{11}, \{v_{11}, v_i\}) = a$ for any i = 6, 7, 8, 10, 12.

Therefore, no tile types can be repeated in the assembly design of G. Hence, $T_3(G) = 12$.

Proposition 13. Let G be the icosahedron graph. Then $B_3(G) = 9$.

Proof. Let λ be an assembly design for the icosahedron graph. We first show that no bond-edge type may be repeated on a non-incident edge in G. Suppose $\lambda(v_1, \{v_1, v_2\}) = a$ using the vertex labeling shown in Figure 5. Suppose bond-edge type a is repeated on an edge that is not incident to edge $\{v_1, v_2\}$. That is, suppose $\lambda(v_i, \{v_i, v_j\}) = a$ for $i \neq 1$ or for $j \neq 2$. In order to avoid realizing a graph with a multiple-edge, there are 18 half-edges which must be considered. By the reflective

symmetry of the icosahedron, this list may be further refined to the following 10 possibilities: $(i, j) \in \{(4, 10), (4, 12), (10, 6), (10, 12), (12, 10), (12, 11), (11, 12), (8, 11), (11, 8), (11, 7)\}.$

One can use software such as *Maple* to verify that in each of these cases, if the edges associated to bond-edge type a were to break and reattach, then a non-planar non-isomorphic graph can be realized (see Figure 8). Thus, a bond-edge type may not be repeated on a non-incident edge in Scenario 3. Since there are 30 edges in G and G is a 5-regular graph, then $B_3(G) \ge 6$.



FIGURE 8. Example of non-isomorphic graph formed in proof of Proposition 13

In order to find the minimum number of bond-edge types, we want to maximize the number of times each bond-edge type appears. By above, we may only repeat a bond-edge type on incident edges. The independence number of G is 3, which means we may select a maximal independent set of vertices in which each vertex has a bond-edge type repeated five times. Without loss of generality, we may use tile-types $\{a^5\}, \{b^5\}$ and $\{c^5\}$ at vertices v_1, v_7 , and v_{10} , respectively. Since we cannot repeat another bond-edge type five times, we then select a vertex with four unlabeled edges from the list: v_8, v_9 , or v_{12} . Note that we can only repeat a bondedge type four times at only one of these vertices since they are pairwise adjacent. The choice is arbitrary since a selection of any vertex leaves the same sequence of unlabeled edges. Suppose we select v_8 and use bond-edge type d on the unlabeled edges. Using our previous reasoning, we next want to select vertices with three unlabeled edges. The options are $\{v_2, v_4, v_5, v_6, v_9, v_{12}\}$. From within this set, we can select at most two non-adjacent vertices. Suppose we then select v_2 and v_4 . We next select vertices with two unlabeled edges, which leaves v_9 and v_{11} . There is one edge remaining that must be labeled with the last bond-edge type. This process of selecting vertices in independent sets allows us to repeat a bond-edge type the maximum number of times possible. Therefore $B_3(G) = 9$.

The pot

$$P = \left\{ t_1 = \{a^5\}, t_2 = \{b^5\}, t_3 = \{c^5\}, t_4 = \{\hat{b}, d^4\}, t_5 = \{\hat{a}, \hat{b}, e^3\}, t_6 = \{\hat{a}, \hat{c}, f^3\}, t_7 = \{\hat{a}, \hat{d}, \hat{f}, g^2\}, t_8 = \{\hat{b}, \hat{c}, \hat{d}, h^2\}, t_9 = \{\hat{a}, \hat{c}, \hat{e}, \hat{f}, i\}, t_{10} = \{\hat{a}, \hat{b}, \hat{d}, \hat{e}, \hat{g}\}, t_{11} = \{\hat{b}, \hat{c}, \hat{e}, \hat{h}, \hat{i}\}, t_{12} = \{\hat{c}, \hat{d}, \hat{f}, \hat{g}, \hat{h}\} \right\}$$

realizes the icosahedron graph (see Figure 9) and the spectrum of the pot is

$$\mathcal{S}(P) = \left\{ \frac{1}{12r} \langle r, r, r, \dots, r \rangle \middle| r \in \mathbb{Z}^+ \right\}.$$

The spectrum of P shows for all $H \in \mathcal{O}(P), \#V(H) \ge 12 = \#V(G)$.

Lastly, we show that the pot P does not realize any non-isomorphic graphs of order equal to G. We use the property that two graphs G_1 and G_2 with adjacency matrices A_1 and A_2 , respectively, are isomorphic if and only if there exists a permutation matrix P_{π} such that $P_{\pi}A_1P_{\pi}^{-1} = A_2$ [4]. The pot P contains 12 unique tile types and S(P) shows that a graph of minimal order must use exactly one of each tile type. Using the vertex labeling from Figure 5, the adjacency matrix for G is given in Equation (7).

Suppose $H \in \mathcal{O}(P)$, then using the labeling convention that $\lambda(u_i) = t_i$, the adjacency matrix of H must be Equation (8).

			u_1	u_2	u_3	u_4	u_5	u_6	u_7	u_8	u_9	u_{10}	u_{11}	u_{12}
(8)	$A_H =$	u_1	$\int 0$	0	0	0	1	1	1	0	1	1	0	0 \
		u_2	0	0	0	1	1	0	0	1	0	1	1	0
		u_3	0	0	0	0	0	1	0	1	1	0	1	1
		u_4	0	1	0	0	0	0	1	1	0	1	0	1
		u_5	1	1	0	0	0	0	0	0	1	1	1	0
		u_6	1	0	1	0	0	0	1	0	1	0	0	1
		u_7	1	0	0	1	0	1	0	0	0	1	0	1
		u_8	0	1	1	1	0	0	0	0	0	0	1	1
		u_9	1	0	1	0	1	1	0	0	0	0	1	0
		u_{10}	1	1	0	1	1	0	1	0	0	0	0	0
		u_{11}	0	1	1	0	1	0	0	1	1	0	0	0
		u_{12}	$\setminus 0$	0	1	1	0	1	1	1	0	0	0	0 /

Let P_{π} be the following permutation matrix

The permutation matrix in Equation (9) proves that H and G are isomorphic. \Box

Note that it would suffice to find an isomorphism from V(G) to V(H) for Proposition 13. However, the authors felt the technique of using a permutation matrix would be more interesting and would serve as an example of an additional technique that has not been used in the current literature on self-assembly.

4.3. **Dodecahedron.** Let G be the dodecahedron. Then G is a 3-regular graph, so $T_1(G) = 2$ and $B_1(G) = 1$ [3]. Algorithm 1 of [3] yields a pot of tiles realizing G.

Proposition 14. Let G be the dodecahedron. Then $T_2(G) \leq 6$ and $B_2(G) \leq 4$.

Proof. Both upper bounds are realized by the following pot (see Figure 10)

$$P = \left\{ \{a^2, b\}, \{\hat{a}, c^2\}, \{a, \hat{a}, \hat{c}\}, \{\hat{b}^2, \hat{d}\}, \{c, \hat{c}^2\}, \{a, c, d\} \right\}.$$

The spectrum of P is

$$\mathcal{S}(P) = \left\{ \frac{1}{20r} \left\langle 2r, 5r, 11r - t, r, t, r \right\rangle \middle| r \in \mathbb{Z}^+, t \in \mathbb{Z} \cap [0, 11r] \right\}.$$

Thus, if $H \in \mathcal{O}(P), \#V(H) \ge 20$.

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FIGURE 9. Assembly design of icosahedron graph for Propositions $12 \ {\rm and} \ 13$



FIGURE 10. Assembly design of dodecahedron in Scenario 2 for Proposition $14\,$

Proposition 15. Let G be the dodecahedron. Then $B_3(G) \ge 10$.

Proof. Note that G contains no cycles of lengths 3, 4, 6, or 7. Consider the vertex labeling of G as shown in Figure 11. Suppose $\lambda(v_1, \{v_1, v_2\}) = a$. Then, in order to avoid realizing a graph with a loop, multiple-edge, 3-cycle, 4-cycle, 6-cycle, or 7-cycle, the only possible options for $\lambda(v_i\{v_i, v_j\}) = a$ are $(i, j) \in \{(1, 5), (1, 16), (3, 2), (15, 2)\}$.

If $\lambda(v_1, \{v_1, v_5\}) = a$, in order to avoid realizing a graph with a 4-cycle, 6-cycle, or 7-cycle, the only remaining edge that can be labeled with bond-edge type a is $\{v_1, v_{16}\}$. Similarly, if $\lambda(v_1, \{v_1, v_{16}\}) = a$, the only remaining edge that can be labeled with bond-edge type a is $\{v_1, v_5\}$.

If $\lambda(v_3, \{v_3, v_2\}) = a$, in order to avoid realizing a graph with a multiple-edge or 3-cycle, the only remaining edge that can be labeled with bond-edge type a is $\{v_{15}, v_2\}$. Similarly, if $\lambda(v_{15}, \{v_{15}, v_2\}) = a$, the only remaining edge that can be labeled with bond-edge type a is $\{v_3, v_2\}$.

Therefore, a bond-edge type can be repeated at most three times in any assembly design of G satisfying Scenario 3. Since #E(G) = 30, then $\#\Sigma(P) \ge 10$ for any P realizing G in Scenario 3.

Proposition 16. Let G be the dodecahedron. Then $T_3(G) = 20$.

Proof. We follow the vertex labeling of G shown in Figure 11. Suppose $t = \{a, b, c\}$, with a, b, c not necessarily distinct, and $\lambda(v_1) = t$ such that $\lambda(v_1, \{v_1, v_2\}) = a, \lambda(v_1, \{v_1, v_5\} = b, \lambda(v_1, \{v_1, v_{16}\}) = c$. According to the proof of Proposition 15, bond-edge type a can only be used to label half-edges at v_3 or v_{15} . In particular, if $\lambda(v_3) = t$ then $\lambda(v_3, \{v_3, v_2\}) = a$ and if $\lambda(v_{15}) = t$ then $\lambda(v_{15}, \{v_{15}, v_2\}) = a$.

If $\lambda(v_3) = t$ such that $\lambda(v_3, \{v_3, v_2\}) = a, \lambda(v_3, \{v_3, v_4\}) = b, \lambda(v_3, \{v_3, v_{13}\}) = c$, then a graph with a 7-cycle can be realized. If $\lambda(v_3) = t$ such that $\lambda(v_3, \{v_3, v_2\}) = a, \lambda(v_3, \{v_3, v_4\}) = c, \lambda(v_3, \{v_3, v_{13}\}) = b$, then a graph with a 6-cycle can be realized. Thus, $\lambda(v_3) \neq t$.

If $\lambda(v_{15}) = t$ such that $\lambda(v_{15}, \{v_{15}, v_2\}) = a, \lambda(v_{15}, \{v_{15}, v_{14}\}) = b, \lambda(v_{15}, \{v_{15}, v_{17}\}) = c$, then a graph with a 7-cycle can be realized. If $\lambda(v_{15}) = t$ such that $\lambda(v_{15}, \{v_{15}, v_2\}) = a, \lambda(v_3, \{v_{15}, v_{14}\}) = c, \lambda(v_3, \{v_{15}, v_{17}\}) = b$, then a graph with a 3-cycle can be realized. Thus, $\lambda(v_{15}) \neq t$.

A unique tile type must be used for each vertex in any labeling of G satisfying Scenario 3. Therefore, $T_3(G) = \#V(G) = 20$.

5. Conclusion

This collection of proofs serves as a supplement to the work provided in [1]. We have shown results for particular square and triangular lattice graphs in certain scenarios as well as full results for the octahedron and icosahedron in all scenarios. For the dodecahedron we have given upper bounds for Scenario 2, a lower bound for bond-edge types in Scenario 3, and a proof that each vertex requires a distinct tile type in Scenario 3.

Additional work is still needed to determine optimal solutions for lattice graphs in Scenarios 2 and 3. Lower bounds for the dodecahedron in Scenario 2 and a pot realizing the graph in Scenario 3 are necessary next steps to achieve full results for the collection of platonic solids.



FIGURE 11. Vertex labeling of dodecahedron graph for Propositions 15 and 16

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