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Design and Simulation of Single Electron Transistor based SRAM and its Memory Controller at Room Temperature

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Abstract: Heterogeneous 3D integration of single electron transistor (SET) circuits with CMOS based circuits is achieved by stacking a SET layer above CMOS IC. Low power and delay efficient circuits can be designed using SET. In this paper, we have designed and simulated 6T SRAM array operating at room temperature and at CMOS comparable voltage. Peripheral circuit like sense amplifier, decoder, write circuit and pre-charge circuit using SET have been designed for optimum performance. The stability of 6T SRAM cell is verified using N-curve method. The designed SET based 8 x 8 bit SRAM is 99.54 % power efficient, 92.19 % faster in write access time and 78.58 % faster in read access time compared to 16 nm CMOS based SRAM. The SRAM is designed to work at CMOS comparable voltage of 800 mV, which can be scaled up to 20 mV with better efficiency. The designed SRAM is tested and verified for variation in process, voltage and temperature. The maximum frequency of operation for the designed SET based SRAM with memory controller is 4 GHz.

Keywords: Nanoelectronics, Semiconductor Devices, Single Electron

1. Introduction

Integrated circuits require high speed and low power for processing data. Scaling of technology plays an important role for improvement in the performance of an IC. By technology scaling, the performance of processor can be improved in terms of speed but the speed of a memory is lagging behind the processor speed [1]. Modern SRAM demands high density while maintaining low power consumption and high performance. Presently, the density of SRAM is increasing and it occupies 90 % of the chip area [2]. One of the solutions is to scale the transistor of the SRAM cell. Scaling of the transistor causes velocity saturation, mobility degradation, lower breakdown voltage, increased leakage currents and thus increases in leakage power [3, 4]. These challenges of CMOS has motivated numerous novel device like I-MOS, NEMS switch, Spin MOSFET, spin FET, Mott FET and single electron transistor (SET) [5] for either memory or logic applications. SET is a promising and elegant device in nanoelectronics because of its ultra-low power consumption, room temperature operation, scaling potential and CMOS comparable voltage that enables SET to be interfaced with CMOS circuits. SET with a wide operating temperature range up to 130 ˚C can be successfully fabricated with a CMOS compatible back-end-of-line (BEOL) process [6]. SET based low power applications like nonvolatile memory, PLA and logic circuits can be heterogeneously integrated with CMOS circuits [7].

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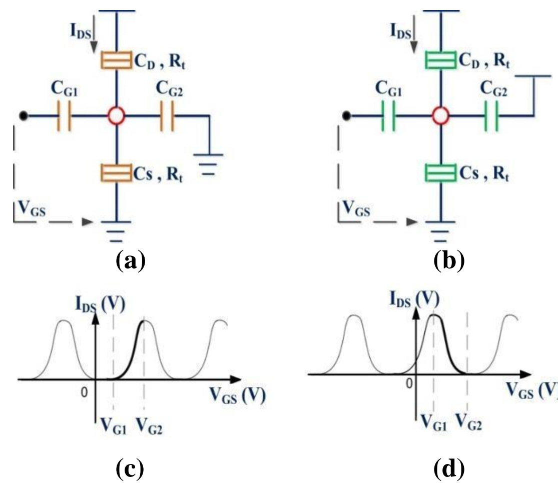


Fig.1 -(a) P – SET, (b) N – SET, (c) Unbiased back gate, (d) Biased back gate

Fig. 1(a) and 1(b) shows the symbol of double gate SET. It can be used in a complementary fashion by providing a proper bias voltage to back-gate. If back-gate voltage is equal to VDD then that acts as N-SET and if it is zero volts, then that acts as P-SET, similar to NMOS and PMOS. Fig. 1(c) and 1(d) shows the complimentary behaviour of the characteristics curve [8]. A Verilog-A model based on the Mahapatra–Ionescu–Banerjee Model [9] and 16 nm BSIM-CMG high performance predictive model for multi-gate transistors [10,11] is implemented in the spectra circuit simulator and Virtuoso Analog Design Environment of CADENCE [12] for simulation. The SET parameters in this work used for simulation are temperature (T) = 300 K, tunnel resistance (Rt) = 1 MΩ, drain or source capacitance (CD or CS) = 0.03 aF, gate capacitance (CG1) = 0.045 aF and back gate capacitance (CG2) = 0.05 aF [7]. This paper represents an 8 x 8 bit SRAM memory with a memory controller using SET and it can be expanded to n x n bits. To date, there have been few publications on the design of SRAM using SET / hybrid SET-CMOS circuits. The architecture of 1-bit SRAM memory showing write operation based on SET technology is discussed in [13] operating at 400 mV. SRAM designed in [14] using hybrid SET-CMOS technology face the challenge of fabrication of SET and CMOS on a single layer. In this paper, we have designed and simulated an 8 x 8 bit SRAM with controller for read and write operation at 800 mV and operating at room temperature. The peripheral circuit like sense amplifier, write circuit and pre-charge circuit are designed for optimum delay and power using pure SET circuits and compare the simulation results with 16 nm CMOS. The remainder of the paper is organized as follows, section II explains the architecture of 8 x 8 bit SRAM and the stability of SRAM is verified using N-Curve. Section III discusses the design of peripheral circuit like sense amplifier, pre-charge circuit, write circuit and memory controller. Section IV shows the simulation result and compare this work with 16 nm CMOS in terms of delay and power. PVT simulations are also carried out for designed SRAM. Section V concludes the result.

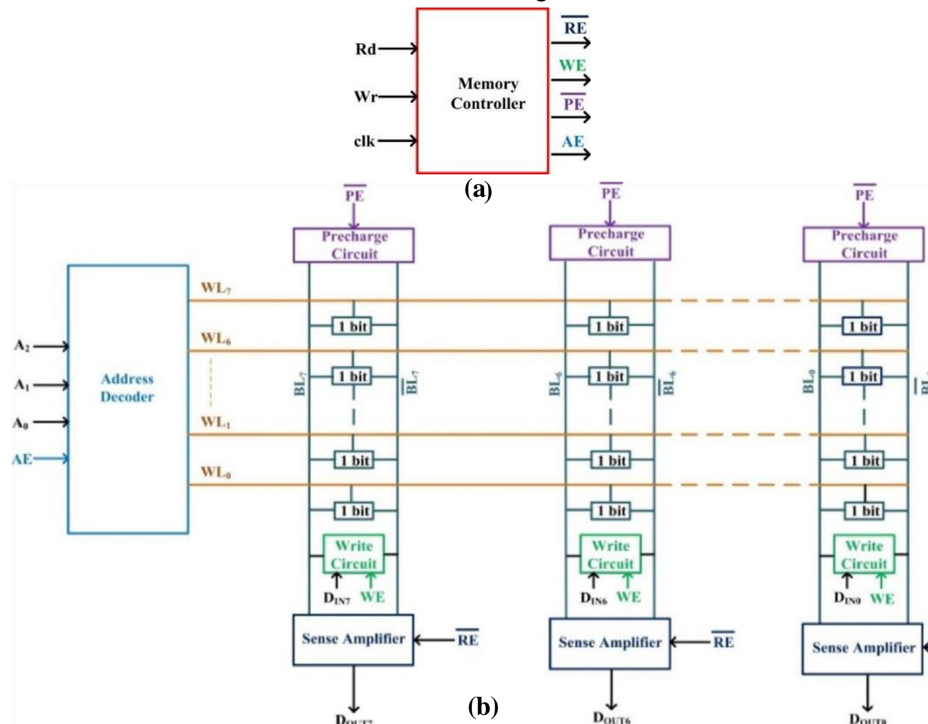


Fig.2- (a) Block diagram of memory controller, (b) Block diagram of 8x8 bit SRAM

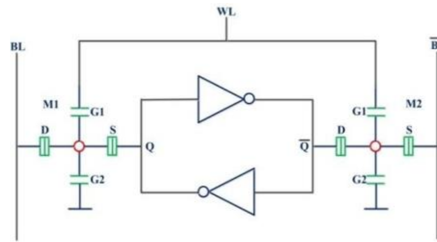


Fig.3 - 6 SET SRAM Cell

2. 8 x 8 bit SRAM Architecture

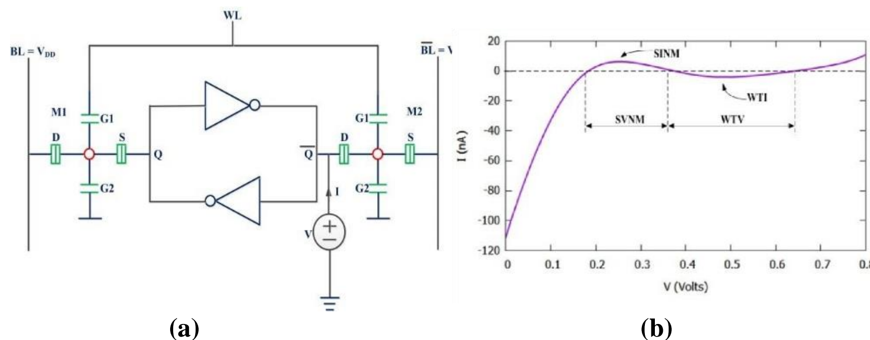
Fig. 2(a) shows the block diagram of memory controller which generates properly timed signals for read and write operation. The control signals generated by memory controller i.e. read enable ($\overline{RE}$) active low, write enable (WE) active high, pre-charge enable ($\overline{PE}$) active low and address enable (AE) active high are fed to the SRAM architecture shown in Fig. 2(b). The designed architecture for 8 x 8 bit SRAM is shown in Fig. 2(b). The Memory cell is an essential element that stores one bit of information in the form of 1 or 0. The architecture consists of pre-charge circuit which pre-charges the bit line before the read operation. The sense amplifier senses the difference in voltage between the bit lines during a read operation. Write circuit is used to write data in the corresponding memory cell selected by the address decoder.

2.1 Structure

The 6T SRAM cell shown in Fig. 3 consists of 6 SETs of which M1 and M2 act as pass transistors and the remaining 4 are used to make back to back inverter which latches data in between them. SRAM operates in two modes i.e. write and read. The data present at BL is written to node "Q" of SRAM cell, when WL is active high. To write 0, we would apply a 0 to the bit line, i.e. setting BL to 0 and ($\overline{BL}$) to 1. The read cycle is started by the pre-charging both bit lines BL and ($\overline{BL}$) to VDD by using pre-charge circuit. Then asserting the word line WL to 1, enables both the pass transistors M1 and M2. Depending on the value of data present in the SRAM cell, one of the bit lines will discharge through pass transistors. As a result, voltage difference is created between them. A sense amplifier will sense voltage difference between bit lines and thus determine whether there was 1 or 0 stored. The higher the sensitivity of sense amplifier, the faster the read operation.

2.2 Stability calculation for 1-bit SRAM

The stability of SRAM is defined as noise acceptance capability. Static Voltage Noise Margin (SVNM) governs the speed of SRAM. If SVNM is high that means the speed of SRAM is high [14]. Fig.4(a) shows the circuit to measure stability. A dc variable voltage which is varied from 0 V to 0.8 V is applied at node Q. The data fixed in 6T SRAM cell is zero i.e. node Q is 0 and $\bar{Q}$ is 1. Bit lines BL and ($\overline{BL}$) are to be at V_{DD}. Fig. 4(b) shows simulation results for the N curve of 6T based SRAM cell which shows the graph of current (I) v/s voltage (V), where V is varied from 0 V to 0.8 V. At the points A, B and C the value of the current is zero. The curve between A and B gives the read ability. The voltage difference between point A and B is SVNM, and can be defined as maximum dc noise voltage added at the cell before its data changes. Peak current located between point A and B is static current noise margin (SINM) defined as the maximum value of DC current that can be added to the SRAM cell before its data changes. The value of SVNM and SINM gives the read stability of the SRAM cell during read operation [15]. If SVNM or SINM are high then that will imply higher read ability [16]. The curve between C and B gives the write ability. The voltage difference between C and B gives the write trip voltage (WTV) and can be defined as the maximum voltage required for writing data in a cell. The negative current peak between C and B gives the write-trip current (WTI), which can be defined as the maximum current required to write data in a cell. If WTV or WTI are high, then that will imply smaller write ability [18].



(a) **(b)**

Fig.4 - (a) 6T SRAM for N-Curve measurement (b) N-Curve simulation result for 6T SET cell

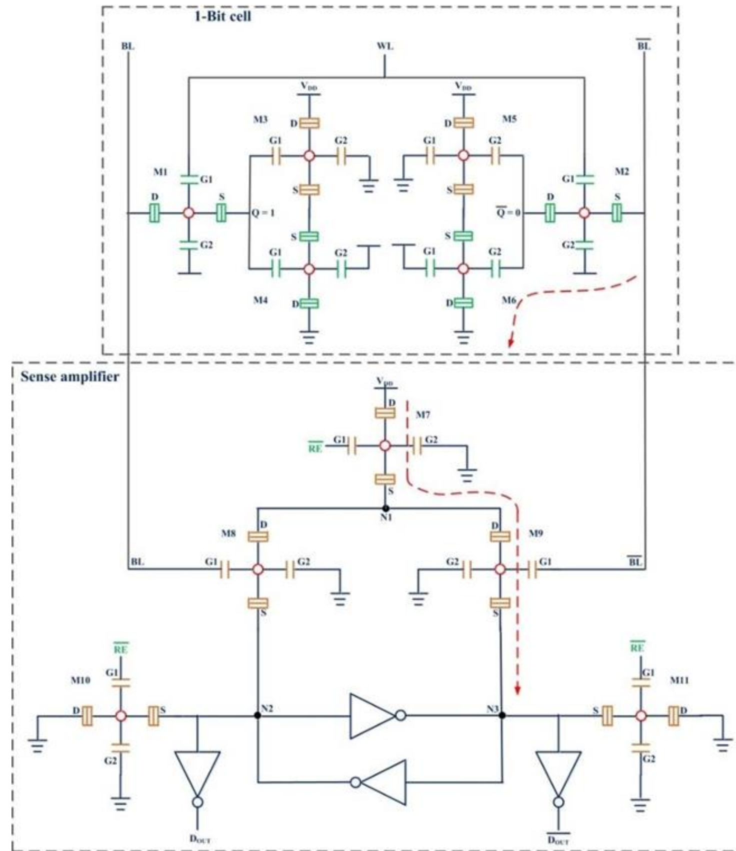


Fig. 5 - SET based latch type sense amplifier

Table 1 shows the comparison of various stability parameters for SET, CMOS and CNTFET based SRAM cell. Specially when comparing with higher technology node, the SVNM for SET based SRAM cell is much higher than16 nm CMOS based SRAM cell.

Table 1 Comparison of stability parameter of 6T SRAM

Stability Parameter	SET based SRAM cell	CMOS 16 nm SRAM cell	CMOS 22 nm SRAM cell [17]	CNTFET SRAM cell [18]
SVNM	142.89 mV	81 mV	251.44 mV	259.74 mV
SINM	3.82 nA	186.71 nA	9.78 µA	15.89 µA
WTI	2.52 nA	114.07 nA	800.24e-3 µA	14.36 µA
WTV	197.76 mV	105.43 mV	317.94 mV	397.69 mV

3. 8 x 8 bit SRAM Architecture

This section discusses the design of peripheral circuits used for designing 8 x 8 bit SRAM array, like sense amplifier, write circuit, pre-charge circuit and memory controller depicted in Fig. 2.

3.1 Sense Amplifier

The SET based circuit is composed of Ti interconnects which are in the range of nanometers scale, so it offers low parasitic as compared to CMOS. Hence, bit lines of SET based SRAM discharge faster as compared to CMOS. Therefore, during read operation voltage difference generated between bit lines is larger as compared to CMOS. Hence latch type sense amplifier is preferred since it is faster than the voltage differential sense amplifier [19]. Fig. 5 explains the operation of a latch type sense amplifier along with 1-bit SRAM cell where (BL) , $\overline{BL}$ and ($\overline{RE}$) are inputs and DOUT is the output. SETs M1 to M6 constitute 1-bit SRAM cell and M7 to M11 are part of the sense amplifier. The latch type sense amplifier has two inverters connected back to back that act as a latch. As shown in the Figure, suppose the data bit at Q = 1 and $\overline{Q}$ = 0. During read operation, both the bit lines are pre-charged to V_{DD}. During read operation, $\overline{RE}$ = 0 V and WL = V_{DD}. With $\overline{Q}$ = 0V, ($\overline{BL}$) will discharge through M2 → M6 → gnd. At the same time M7 is on and node N1 = V_{DD}. Suppose at an instance of time BL = 800 mV and ($\overline{BL}$) = 400 mV. As BL = 1, M8 will be off. Similarly, as ($\overline{BL}$) ≈ 0, M9 will be on. Therefore voltage at node N1 is passed to node N3 which is equal to V_{DD} and voltage at node N2 will be 0 V. So DOUT will be 800 mV. So the data which was stored inside the cell is retrieved successfully.

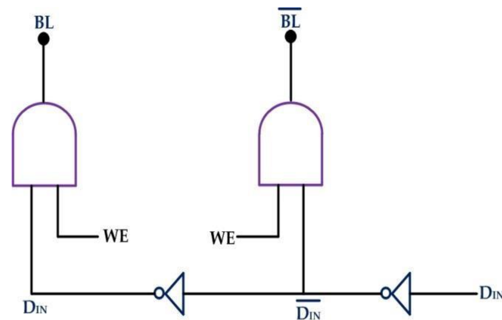


Fig.6 - SET based write circuit

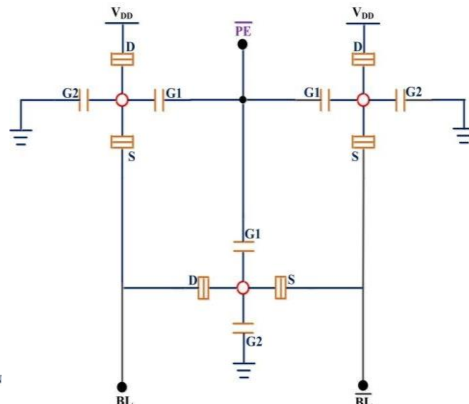


Fig.7 - SET based pre-charge circuit

3.2 Write Circuit

Fig. 6 shows the data write circuit which consists of two AND gate and two inverters. Write circuit passes the D_{IN} to BL and ($\overline{D_{IN}}$) to ($\overline{BL}$) whenever WE goes active high. The control signal for the write circuit is given by the memory controller when the SRAM is undergoing write cycle. After that, WL signal is enabled by the address decoder and the data present on the bit line is latched into the bit cell.

3.3 Pre-Charge Circuit

The pre-charge circuit sets bit lines BL and ($\overline{BL}$) to V_{DD} just before the read operation. The simplest version of the pre-charge circuit consists of three transistors that are P-SET as shown in Fig. 7. ($\overline{PE}$) is the control signal given to the pre-charge circuit by the memory controller during the start of read cycle and it should be active low enabled.

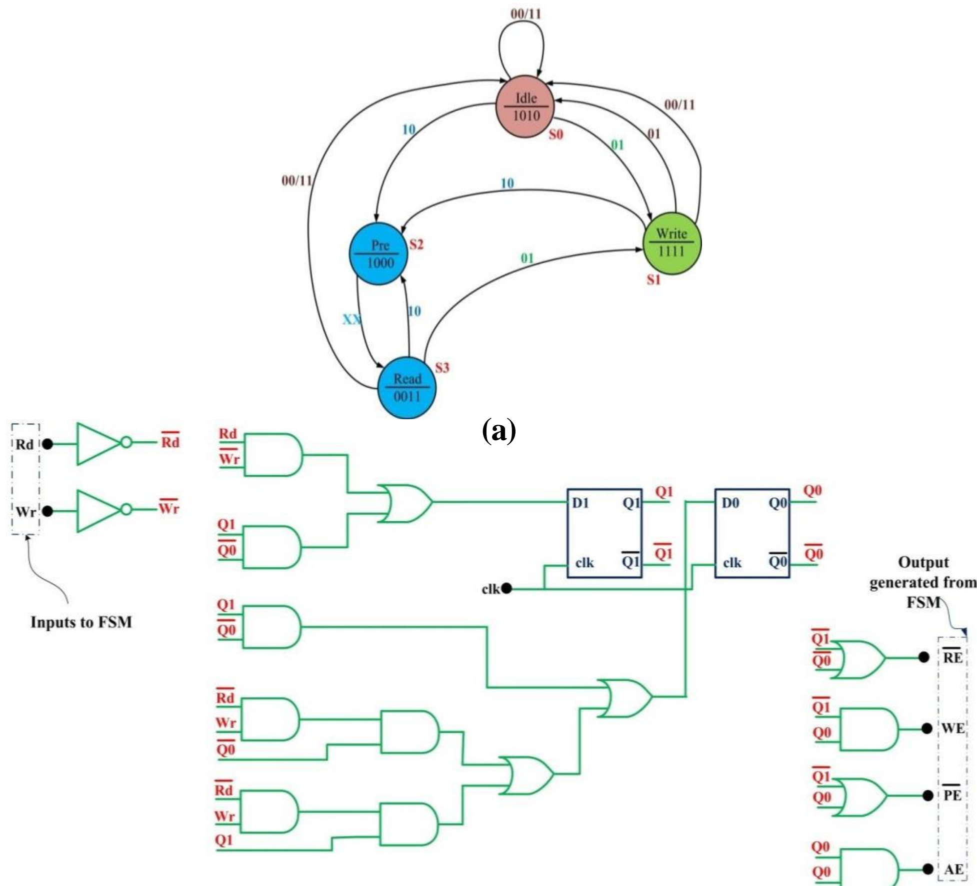


Fig.8 - (a) Finite state Machine (b) Circuit diagram of memory controller

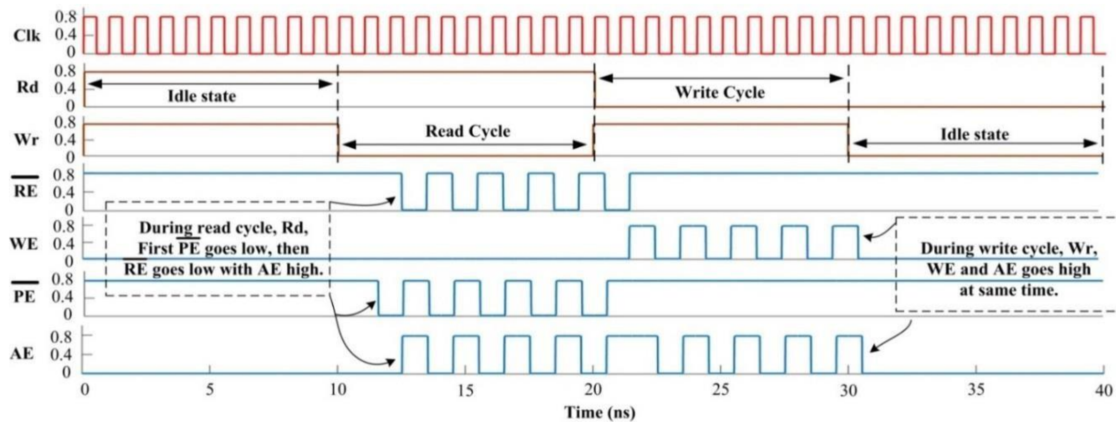


Fig.9 - Simulation result of memory controller

3.4 Memory Controller

In register or flip-flop data is sampled and stored on an active clock edge, but accessing data from asynchronous SRAM is more complicated. During read and write operation of SRAM, signals such as data, address, and control signals must be asserted in a specific order and must be held for a specific amount of time for the proper working of SRAM cell. As the SRAM cell is asynchronous, it is very difficult for a system which is synchronous to access SRAM directly [20]. The Memory controller acts as an interface between the synchronous system and asynchronous SRAM. The Memory controller takes inputs from the synchronous system and generates properly timed signals to access the SRAM. The performance matrix of memory can be measured by the number of memory accesses that can be completed in a given period of time. The memory controller is designed using finite state machine (FSM) with Rd (Read) and Wr (Write) as input signal and Read Enable ($\overline{\text{RE}}$), Write Enable (WE), Pre-charge Enable ($\overline{\text{PE}}$) And Address Enable (AE) as output signals from FSM. The block diagram for the memory controller is shown in Fig. 2 (a). The memory controller is basically implemented with the help of a FSM. The finite state machine is shown in Fig. 8(a). The circuit is basically implemented using basic gates and D-flip-flops. The controller has three states to function, i.e. idle state (no operation), read state (control signal for read operation) and write state (control signal for write operation). Depending on the inputs the controller generates properly timed signals for read, write, pre-charge and address enable in their respective states. The circuit diagram for the controller is shown in Fig. 8(b).

4. Simulation Results

The verification of design is done through read and write operations. The pulse duration and delay of each input signal depends on each peripheral circuits, taking all paths in consideration through which read, pre-charge and write signal are travelling.

4.1 Simulation result for memory controller

The simulation result for the memory controller is shown in Fig. 9. The inputs to the memory controller are clk, Rd (Read) and Write (Write) and the corresponding function defined is shown in Table 2.

Table 2 Functions defined on Input

Rd	Wr	Function
0	0	Idle State
0	1	Write operation
1	0	Read operation
1	1	Idle State

Depending on the inputs the controller generates properly timed signals for read, write, pre-charge and address enable in their respective states. During the read cycle, first ($\overline{\text{PE}}$) goes low, then ($\overline{RE}$) goes low and simultaneously AE goes high. Similarly during write cycle WE and AE goes high simultaneously.

4.2 Delay and power analysis for 1-bit SRAM cell

The delay and rms power calculated in this work for 1-bit SET based SRAM has been compared with the 22 nm CMOS [21] based SRAM as shown in Table 3 and Table 4. Further, the average read and write delay of standard 6T SRAM cell at 0.8V presented in this work are 34.4ps and 3.9ps as compared to 3000ps and 60ps respectively at 1V demonstrated by Sharma et al. [22].

Table 3 Comparison of delay for 1-bit SET and CMOS 22nm based SRAM [21]

Parameters	SET 1-bit SRAM (ps)	CMOS 22 nm 1-bit SRAM [18] (ps)
$Read_0$	34.3	97
$Read_1$	34.4	124
$Write_{0\to1}$	4	42
$Write_{1\to0}$	3.7	37

Table 4 Comparison of power for 1-bit SET and CMOS 22nm based SRAM [21]

Parameters	SET 1-bit SRAM (nW)	CMOS 22 nm 1-bit SRAM [18] (nW)
$Read_0$	9.71	372
$Read_1$	9.68	337
$Write_{0\to1}$	21.93	1485
$Write_{1\to0}$	21.91	1338

4.3 Delay and power analysis for 8 x 8 SRAM array

The simulation for 8 x 8 bit SET based SRAM array with memory controller is carried out in cadence virtuoso tool. The SRAM architecture is designed to operate at 800 mV and at room temperature operation. The simulation shown in Fig. 10 is for SET based SRAM, all the locations are selected from address decoder using a vector file format which is included during the simulation. Initially, the input to the FSM is Rd = 0 and Wr = 1. So during the write cycle, the corresponding data is written to the respective location. Then the read cycle is initiated by Rd = 1 and Wr = 0. So the data which are written before are retrieved properly from the respective location without the loss of data during read operation. The delay and power calculated for SET based SRAM is compared with 16 nm CMOS as shown in Table 5 and Table 6. The comparison is at a clock frequency of 1 GHz because, CMOS maximum frequency of operation is 1 GHz whereas SET is 4 GHz.

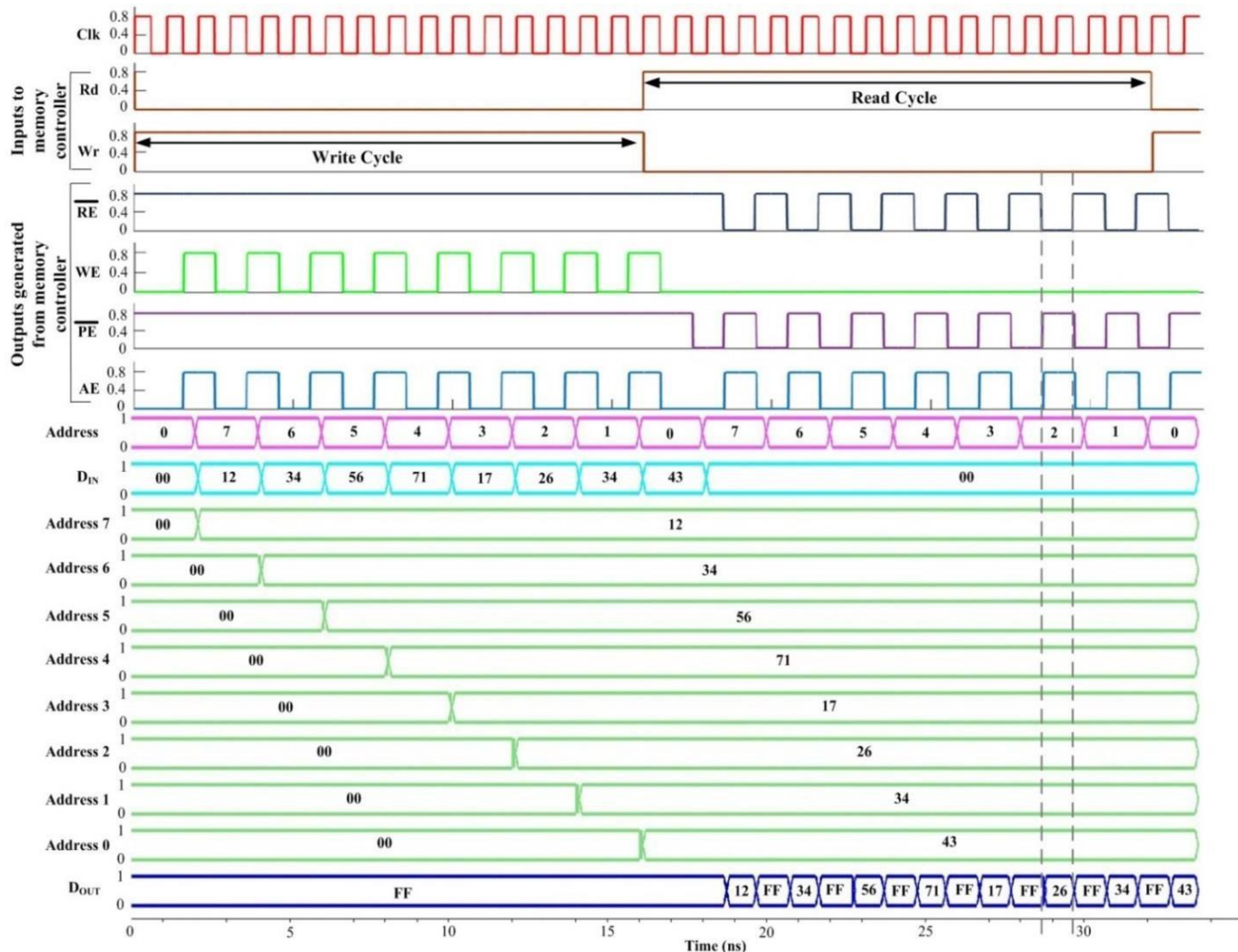


Fig. 10 - Simulation result for SET based SRAM

Table 5 Comparison of speeds for 8x8 bit SET and 16 nm CMOS based SRAM array

Parameters	SET based SRAM (ps)	CMOS 16 nm based SRAM (ps)
Write Access Time	10	128.12
Read Access Time	66	546.22

Table 6 Comparison of power for 8x8 bit SET and 16 nm CMOS based SRAM array

Parameters	SET based SRAM (nW)	CMOS 16 nm based SRAM (nW)
Total Power	0.828	181.2
Static Power	0.753	102.5
Dynamic Power	0.075	78.6

4.4 PVT variation and simulation results

The process-voltage-temperature (PVT) variations are carried out for the designed SET based SRAM. The data written in the memory can be affected due to PVT variation. PVT variations are important steps during simulation of memory. PVT simulations have been performed to assure that the design of memory meets the entire requirement during the simulation stage.

Table 7 PVT Variation for the 64-bit SRAM architecture with memory controller [20]

	Case no.	Variation	Parameter values	Memory read data output	
				Low (mV)	High (mV)
Reference values [5]	-		Cj = 0.03 aF, Cg = 0.045 aF, Cb = 0.05 aF, Rt = 1 MΩ, T = 300 K , V_S = 800 mV	21.05	788.92
Process: capacitance, resistance	1	Cj, Cg, Cb by +10 % Rt at 0.1 MΩ	Cj = 0.033 aF, Cg = 0.0495 aF, Cb = 0.055 aF, Rt = 0.1 MΩ, T = 300 K , V_S = 800 mV	75.29	769.95
	2	Cj, Cg, Cb by +10 % Rt at 2 MΩ	Cj = 0.033 aF, Cg = 0.0495 aF, Cb = 0.055 aF, Rt = 2 MΩ, T = 300 K , V_S = 800 mV	74.74	769.95
	3	Cg, Cb by -10 % Rt at 0.1 MΩ	Cj = 0.03 aF, Cg = 0.0405 aF, Cb = 0.045aF, Rt = 0.1 MΩ, T = 300 K , V_S = 800 mV	37.42	788.17
	4	Cg, Cb by -10 % Rt at 2 MΩ	Cj = 0.03 aF, Cg = 0.0405 aF, Cb = 0.045aF, Rt = 2 MΩ, T = 300 K , V_S = 800 mV	37.39	788.17
Supply Voltage	5	+10%	Cj = 0.03 aF, Cg = 0.045 aF, Cb = 0.05 aF, Rt = 1 MΩ, T = 300 K , V_S = 880 mV	52.69	853.33
	6	-10%	Cj = 0.03 aF, Cg = 0.045 aF, Cb = 0.05 aF, Rt = 1 MΩ, T = 300 K , V_S = 720 mV	18.25	711.50
Temperature	7	100 K	Cj = 0.03 aF, Cg = 0.045 aF, Cb = 0.05 aF, Rt = 1 MΩ, T = 100 K , V_S = 800 mV	0.008	799.99
	8	350K	Cj = 0.03 aF, Cg = 0.045 aF, Cb = 0.05 aF, Rt = 1 MΩ, T = 350 K , V_S = 800 mV	55.24	780.98

The SET capacitance and resistance values depend on its dimensions. But during fabrication of chip, the dimension can vary from their reference value. PVT has been performed varying process parameters like gate capacitance (CG1, CG2) by ± 10 %, tunnel junction capacitance (CD, CS) by + 10 % (cannot be decreased due to fabrication limitation) and tunnel junction resistance (Rt) varied from 0.1 MΩ to 2 MΩ, by keeping other parameters to their reference value. For temperature variation we simulate the same circuit by varying temperature from 100 K to 350 K. Similarly, we vary the supply voltage by ±10% and simulate the SRAM array from 720 mV to 880 mV [23]. The SET based SRAM memory gives proper output voltage for read and write operation during simulation of memory for PVT variations. Table 7 shows the high and low value of the read output from the SRAM memory. From the simulations carried out, it can be found that the lower and upper output voltages can be improved to approximately 20 mV and 788 mV respectively by inserting inverter/buffer before the output stage. The designed SRAM operating at CMOS comparable voltage (800 mV) can be used in integration with CMOS based processor. Further, it is possible to decrease the operating voltage upto 20 mV by redesigning the SET device parameters. The fabrication process for SET device parameters operating at low voltage is comparatively easy because the capacitance values of junction and gate capacitors are larger compared to the parameters used in this paper.

5. Conclusion

This paper presents the successful implementation and simulation of SET based SRAM and its memory controller. The design of peripheral circuits like sense amplifier, write circuit and pre-charge circuit is done for optimum performance. The stability of SRAM has been verified using the N- curve method. The delay taken by 1-bit SET based SRAM during writing data 0 to 1 is 4 ps and for CMOS 22 nm based SRAM it is 42 ps. The rms power taken by 1-bit SET based SRAM during $read_1$, $read_0$, $Write_{1\rightarrow 0}$, Write $_{0\rightarrow 1}$ is 9.68nW, 9.71nW, 21.91nW, 21.93 nW as compared to 22 nm CMOS, which is 337 nW, 372 nW, 1338nW, 1485 nW respectively. Thus the performance parameters, delay and rms power of 1-bit SET based SRAM presented in this work are better than 22 nm CMOS. The designed SET based 8x8 bit SRAM with memory controller can be characterized with read access time and write access time being 66 ps and 10 ps respectively with the total average power consumption being 830 nW during read and write operation. It is verified that SET based SRAM architecture with memory controller is 99.54 % more power efficient, 92.19 % faster in write access time and 78.58 % faster in read access time compared to 16 nm CMOS technology. Hence it can be concluded that SRAM designed using SET outperforms CMOS based SRAM in terms of power and speed. The maximum operating frequency of a SET based SRAM is 4 GHz compared to 1 GHz of CMOS based SRAM. The stability of SET based SRAM is much higher compared to CMOS based SRAM. Hence SET based SRAM can be stacked above CMOS carrier to achieve high density, high speed and ultra-low power operation using BEOL compatible process.

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