Design of FPGA- Based SPWM Single Phase Full-Bridge Inverter

Afarulrazi Abu Bakar[1,*] ,Md Zarafi Ahmad[1] and Farrah Salwani Abdullah[1]
[1]Faculty of Electrical and Electronic Engineering, UTHM

*Email:afarul@uthm.edu.my

Abstract

Nowadays power inverters serve as an important emergency power supply system in events of main power supply failure. The AC output voltage of a power electronic inverter is usually non-sinusoidal and hence has a high harmonic content. Sinusoidal Pulse Width Modulation (SPWM) scheme is normally used to convert the DC power supply into AC power supply by comparing the reference voltage waveform with the triangular waveform known as carrier. SPWM provides a way to reduce the total harmonic distortion of load current. The objective of this paper is to demonstrate a SPWM switching scheme by using Altera DE2-70 board. In this SPWM technique, a sinusoidal reference voltage waveform is compared with the triangular carrier voltage to generate the on and off switching states. This switching scheme will trigger the gate of the power switch. In this paper, the SPWM switching strategies implemented using Altera DE2-70 (Cyclone II EP2C35F672C6) with 16 bit serial configuration devices. The switching between reference and carrier waveforms of SPWM is obtained by using Matlab software. Simulation on the design waveform is conducted using Quartus II software tools provided by Altera. The output frequency of SPWM is 50 Hz and the design is limited to two values of modulation indices which are 0.5 and 0.75.

Keywords: SPWM-Sinusoidal Pulse Width Modulation, FPGA-Field Programmable Logic Array, VHDL- Very High Description Language.

1. INTRODUCTION

Pulse width modulation (PWM) is the most popular switching technique used in several types of converters with an appropriate switching scheme to produce a desired switching pattern. PWM is one of the switching techniques used for an AC-to-DC converter to produce an AC output signal fed from DC input [1]. The on and off scheme is based on the intersection of the triangular carrier signal and a constant DC reference signal. The PWM technique still contains a harmonics and another approach is to use Sinusoidal Pulse Width Modulation (SPWM) switching technique [2]. This paper presents the work carried out to produce the bipolar SPWM control signal. In SPWM a fixed triangular waveform is compared with a sinusoidal waveform and the amplitude of output waveform can be varied from range 0 to 1 [1]. The on and off switching states will be generated when the instantaneous value of the reference signal is larger than the triangular carrier. In order to implement SPWM switching using Altera DE2-70 board, the switching interval between each crossing is calculated using Matlab software. The crossover point of the signal is then transferred into a table.

For the hardware, Altera DE2-70 Cyclone II DE-2 70 is used. It provides a wide range of density, memory, embedded multiplier and packaging options in a customer-defined FPGA feature set optimized for low-cost applications. In addition, Cyclone II FPGA also supports a wide range of common external memory interfaces and I/O protocols common in low-cost applications. It is expected the use of FPGA easier to generate the control signal for single phase full bridge inverter. Furthermore, the design of the switching pulse can be altered without any changes in hardware. This is the main advantage of this approach that applied the FPGA technology where there is a flexibility of any change on the switching parameter and directly eliminates the complexity of the hardware.
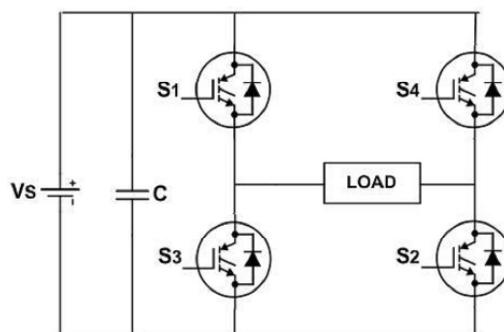

Fig. 1 Single phase Full-Bridge Inverter

2. MATLAB PROGRAMMING

A program is developed from the fundamental concept of the SPWM switching technique by using Matlab M-File. The program is capable to produce the SPWM waveform characteristic over several ranges of frequencies, modulation and number of pulses. The input data is processed through a mathematical programming and the intersection between reference signal and carrier signal generates PWM pulses for a period of αn to βn in each pulse as shown in Fig. 2. In Fig. 2, n is the number of pulse for half cycle of reference signal. The program is implemented using Matlab/M-file programming and is achieved through six steps as demonstrated in Fig. 3.
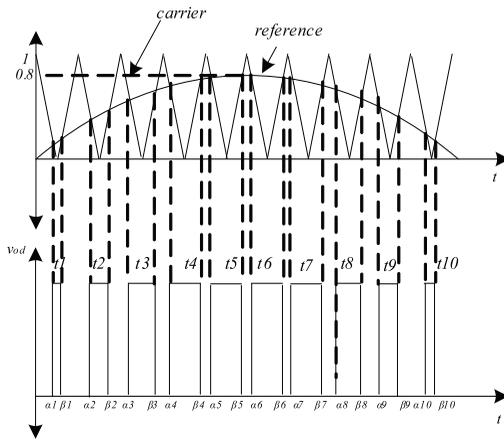
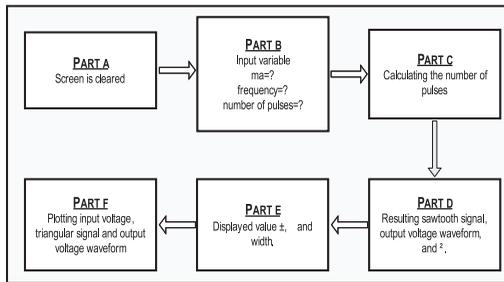Fig 2 Generation of SPWM switching scheme

Fig. 3 Block diagram of Matlab Programming

In this paper, the selected frequency of the output inverter is 50Hz with two modulation indices that is 0.75 and 0.5. The SPWM output signal is recorded based on time scale and degree scale. These data are used to produce the SPWM switching states whereas the time will be digitized.

3. SWITCHING STRATEGIES

The converter is used an Insulated Gate Bipolar Transistor (IGBT) as the switching device. The IGBTs have simpler driving circuits than other power switching devices which lead to high-power application. The inverter is single phase full-bridge topology

with IGBT used as switching devices. The 50Hz reference frequency data and the chosen modulation induces are obtain from Matlab software then depicted in Table 1 (a) and (b) respectively. The recorded data are taken over one complete cycle of reference signal. Initially, the data recorded are in degree scale; this are converted to time scale. In this form, the data is easier to use to generate digital SPWM signal. From the table, it can be observed that the width of each pulse at the beginning and at the end of every half cycle in the same scale. For instant, the positive half cycle of reference signal, the width of the pulse t_1 is equal to the pulse of t_{20}.

The period of the reference input frequency is

$$T = \frac{1}{f_{ref}}$$

$$(1)$$

For the half cycle, $\frac{T}{2}$

The values of αn, βn and the width of the pulses expressed in term of time can be determined from equations (3), (4), and (5) respectively.

$$\alpha_n(t) = \alpha_n(\degree) \times \frac{T/2}{180\degree}$$

$$(2)$$

$$\beta_n(t) = \beta_n(\degree) \times \frac{T/2}{180\degree}$$

$$(3)$$

$$Width = \beta_n - \alpha_n$$

$$(4)$$

All the calculated intersection values for α and β are shown in Table 1 (a) and (b). The last intersection point between the reference signal and carrier signal occurs at β40 which is equal to 19.76ms and this happens at the last pulse over one cycle of 20ms.

Table 1: (a) and (b): Data obtained from Matlab for modulation indices 0.5 and 0.75

Switching time	α(°)	ß(°)	Width(°)	α(t)	ß(t)	Width(t)
t1	4.32	4.68	0.36	0.000240	0.000260	0.000020
t2	12.96	14.04	1.08	0.000720	0.000780	0.000060
t3	21.69	23.40	1.71	0.001205	0.001300	0.000095
⋮	⋮	⋮	⋮	⋮	⋮	⋮
t10	83.25	87.75	4.50	0.004625	0.004875	0.000250
t11	92.25	96.75	4.50	0.005125	0.005375	0.000250
⋮	⋮	⋮	⋮	⋮	⋮	⋮
t18	156.60	158.31	1.71	0.008700	0.008795	0.000095
t19	165.96	167.04	1.08	0.009220	0.009280	0.000060
t20	175.32	175.68	0.36	0.009740	0.009760	0.000020
t21	184.32	184.68	0.36	0.010240	0.010260	0.000020
t22	192.96	194.04	1.08	0.010720	0.010780	0.000060
t23	201.69	203.40	1.71	0.011205	0.011300	0.000095
⋮	⋮	⋮	⋮	⋮	⋮	⋮
t30	263.25	267.75	4.50	0.014625	0.014875	0.000250
t31	272.25	276.75	4.50	0.015125	0.015375	0.000250
⋮	⋮	⋮	⋮	⋮	⋮	⋮
t39	345.96	347.04	1.08	0.019220	0.019280	0.000060
t40	355.32	355.68	0.36	0.019740	0.019760	0.000020

(a)

Switching time	α(°)	ß(°)	Width(°)	α(t)	ß(t)	Width(t)
t1	4.23	4.77	0.54	0.000235	0.000265	0.000030
t2	12.78	14.31	1.53	0.000710	0.000795	0.000085
t3	21.24	23.85	2.61	0.001180	0.001325	0.000145
⋮	⋮	⋮	⋮	⋮	⋮	⋮
t10	82.17	88.92	6.75	0.004565	0.004940	0.000375
t11	91.17	97.83	6.66	0.005065	0.005435	0.000370
⋮	⋮	⋮	⋮	⋮	⋮	⋮
t18	156.15	158.76	2.61	0.008675	0.008820	0.000145
t19	165.69	167.22	1.53	0.009205	0.009290	0.000085
t20	175.23	175.77	0.54	0.009735	0.009765	0.000030
t21	184.23	184.77	0.54	0.010235	0.010265	0.000030
t22	192.78	194.31	1.53	0.010710	0.010795	0.000085
t23	201.24	203.85	2.61	0.011180	0.011325	0.000145
⋮	⋮	⋮	⋮	⋮	⋮	⋮
t30	262.17	268.92	6.75	0.014565	0.014940	0.000375
t31	271.17	277.83	6.66	0.015065	0.015435	0.000370
⋮	⋮	⋮	⋮	⋮	⋮	⋮
t39	345.69	347.22	1.53	0.019205	0.019290	0.000085
t40	355.23	355.77	0.54	0.019735	0.019765	0.000030

(b)

4. VHDL PROGRAMMING USING QUARTUS II

By using Quartus II 8.0 sp1 software provided by Altera, the data obtained from Table 1 digitized for implementation in Quartus II software. Fig. 4 illustrates the block diagram of the complete SPWM generator for modulation indices 0.5 and 0.75. The block diagram consists of altpll which is able to generate a 25 MHz clock output from the 50 MHz internal clock of Altera DE2-70 board. The altpll megafunction can be used to generate other clock. It can be set to operate at multiples frequency. The clock divider is applied to divide internal clock of Altera DE2-70 board into several frequency ranges. For example, the internal clock frequency can be divided into 25 MHz, 1 MHz, 100 kHz, 1 kHz and etc. Then, the 1 MHz of the output frequency of clock divider is connected to the lpm_counter which count from 0 to 19999 over one complete cycle. This means, one cycle of this frequency represents the period of 1 μs. The lpm_counter megafunction is a binary counter that either can be set for counting up, down or simultaneously. The on and off signal is created by VHDL programming and generator converted into block diagram. The VHDL program for 0.75 and 0.5 modulation indices are created by employing four switches which are operated in pairs at a time (S1-S2 and S3-S4).
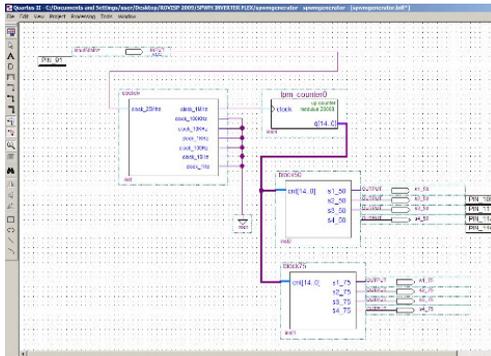
Fig. 4 Block diagram of SPWM generator

Modulation Indices (ma)	Switch	Expansion Header
0.5	S1	PIN N_24
	S2	PIN N_29
	S3	PIN M_22
	S4	PIN M_21
0.75	S1	PIN N_21
	S2	PIN N_22
	S3	PIN L_21
	S4	PIN L_22

Before uploading the program into DE2-70 board, the SPWM signal is first simulated by using Waveform Editor. Fig. 5 shows the output SPWM generated. At this point, the measured value is compared with the different between the observed. The shapes of the SPWM waveform at high speeds for short interval can be observed by using compress option to compress the waveform. The output of the SPWM generator is then assigned to the expansion header of the DE2 board through Pin Planner. The expansion headers connect directly to 36 pins of the Cyclone II FPGA chip. Table 2 show the output control signal available at expansion header pins.
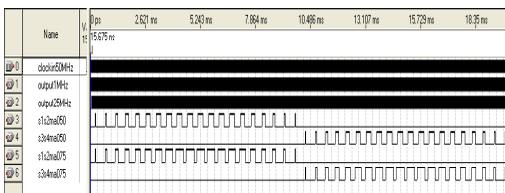
Fig. 5 Control signal for 0.5 and 0.75

Table 2: Output of SPWM connected to expansion header DE2 board

The Assembler which is the compiler module that completes project processing will generate a device programming image. For the FPGAs, this programming image is in the form of one or more Programmer Object Files (.pof) and SRAM Object Files (.sof). The configuration data for devices are downloadad to programm the hardware. The voltage level of the input and output on the expansion header can be adjusted to 3.3V, 2.5V or 1.8V.

5. RESULTS

Tektronix four channel digital oscilloscope TDS3054B is used to measure the output voltage from the DE2-70 board. The experiment was conducted for both modulations which are 0.5 and 0.75. Fig. 6 and Fig. 7 demonstrate the width difference implementation modulation 0.5 and 0.75 respectively. In actual situation, the upper traces signals of Fig. 6 and Fig. 7 are used to control the turning on/off of the power switches S1S2 while the lower traces is to control power switches S3S4 of the inverter. The width of both pulses from t_1 to t_{40} is analyzed and compared with the simulated signal using Quartus II software. The timing differences between the waveform at the screen are compared

for verification check for accuracy. Thus it can be said that the accuracy of the internal clock of the DE2 board is very precise.
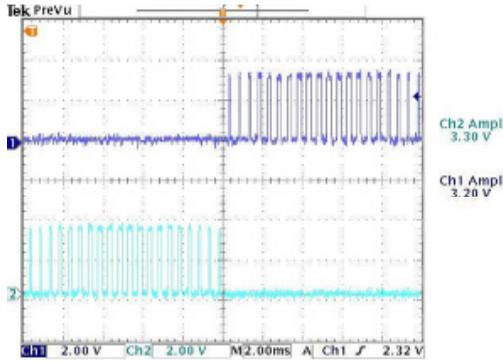

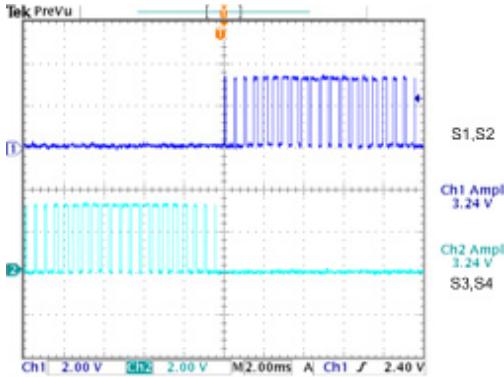Fig. 6 Output signal for modulation index 0.5

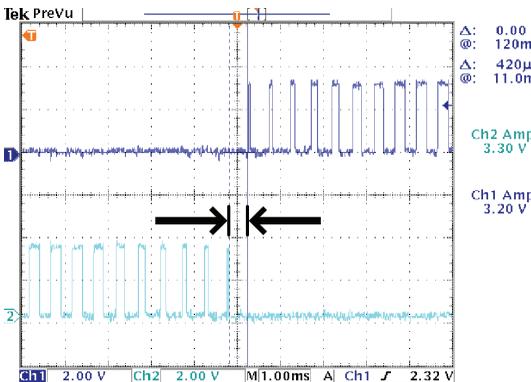Fig. 7 Output signal for modulation index 0.75
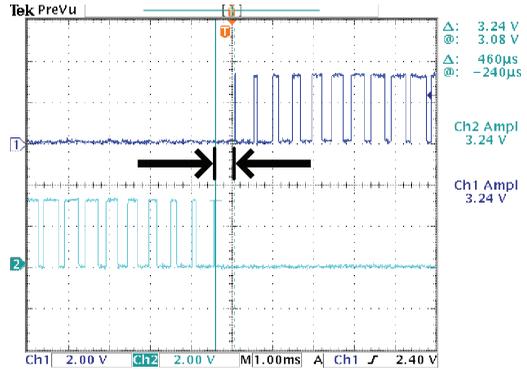

Fig. 8 Dead time for 0.5 modulation index

Fig. 9 Dead time for 0.75 modulation index

Fig. 8 and Fig. 9 show the dead time between switches S1S2 and S3S4 for the modulation indices of 0.5 and 0.75 respectively. From these figures, it can be observed that the dead time for modulation indices 0.5 and 0.75 are 420μs and 460μs respectively. The occurrence of dead time between the S1S2 and S3S4 shows that the signal is possible to be implemented. It is based on the characteristics of the turn on and turn off of the IGBT which up to nano second. The SPWM signals with the modulation indices of 0.5 and 0.75 have the amplitudes of 3.3 V and 3.24 V respectively and shown in Fig. 10 and Fig. 11.
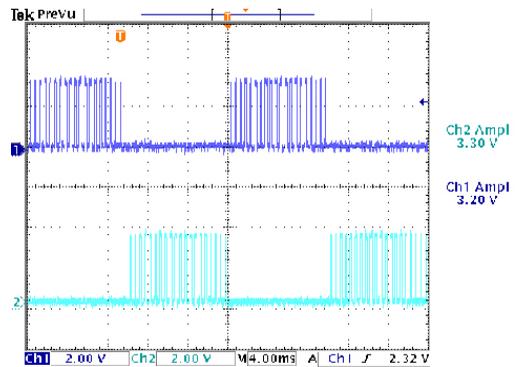

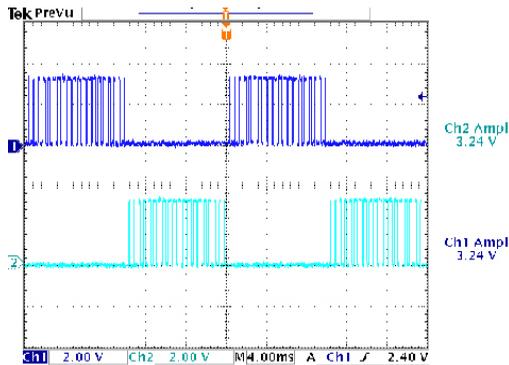Fig. 10 Output signal for S1S2 and S3S4 with modulation index= 0.5

Fig. 11 Output signal for S1S2 and S3S4 with modulation index= 0.75

6. CONCLUSIONS

This paper has outlined and illustrated a method to obtain the switching pulses in generating a SPWM signal for a single-phase inverter. The SPWM signal has been design and tested using Quartus II software and implemented on Altera DE2-70 Board. The modulation index, number of pulses over a period and the output frequency can be easily changed using the program. The SPWM signal is uploaded on a single chip of Altera Board and it capable to provide flexibility, reliability and ease to program in order to control a single-phase inverter.

REFERENCES

[1] Muhammad, H. Rashid. *Power Electronics Circuits, Devices and Application*. Upper Saddle River, NJ: Prentice Hall, 2004.

[2] M. N. Md Isa, M.I. Ahmad, Sohiful A.Z. Murad and M. K. Md Arshad, "FPGA Based SPWM Bridge Inverter", American Journal of Applied Sciences 4 (8), 2007, pp 584-586.