This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2021.3094631, IEEE Journal of Emerging and Selected Topics in Power Electronics

Comprehensive design procedure for Racetrack Microinductors

Jaime López López, *Member, IEEE,* Pablo Zumel, *Member, IEEE,* Seamus O'Driscoll, Zoran Pavlovic, Ruaidhri Murphy, Cian O'Mathuna, *Fellow, IEEE,* and Cristina Fernandez, *Member, IEEE*

***Abstract*—Present needs in efficiency and integration are driving research towards the miniaturization of power converters. Among the latest components to achieve the desired degree of integration are cored micro-inductors and they are still one of the hardest devices to optimize, due to the high number of freedom degrees in their fabrication. In this paper, a comprehensive design procedure for these micro-inductors is presented. The proposed method makes it possible to design the optimal device in a single iteration. It also allows the designer to easily ascertain the limits of the inductor in terms of handled current and losses and provides valuable physical insight on the output of the process.**

***Index Terms*—PwrSoC, inductor-on-silicon, microinductor, integrated power, thin-film, race-track, planar BEOL, magnetics-on-silicon**

I. Introduction

The optimization and miniaturization of power converters has been steadily ramping for many years. Although air-cored microinductors allow a reasonably high efficiency, a very large area is needed if the inductance exceeds a few nH, bringing down power density [1]. In the aim for the fully integrated Power-Supply-on-Chip (PwrSoC), micro-fabricated cored inductors have risen as one of the preferred choices [2]. Thanks to the new manufacturing technologies, that allow full control of every geometric parameter, micro-inductors make it possible to achieve inductance densities of up to more than a hundred nanohenries per square millimeter while maintaining a high efficiency [3], [4].

There are many structures available when designing a microinductor [5]. One of the most developed choices is the racetrack inductor, which consists of a copper conductor spiral, in two sections and surrounded by a magnetic core, as shown in Fig. 1. This geometry makes all the flux in the core travel along the hard anisotropy axis [6], reducing core losses [7], while easing the manufacture of the device [8].

Although the advantages of microinductors are clear, they come with the added difficulty of design complexity, derived from the high number of freedom degrees. In this regard, the design procedures are still not well developed [9], and so, new designs are mostly done by the comparison of thousands of possible parameter combinations, selected by multi-objective optimization methods, as in [8] and [10]. Whilst these methods allow the design of the optimum inductor, the amount of data needed makes it hard to integrate the process in the design of the whole power converter.

This paper presents the complete design procedure to find the optimum device in a single iteration, allowing an easy integration of inductor and converter optimization. It also gives the designer a broad insight on the limits of the technology, determined by the lowest achievable loss, the highest saturation current and the maximum allowed temperature increase.

The rest of the paper is organized as follows: Section II presents the equations needed to model the inductor; Section III states the problem and the need for the new design procedure; in Section IV, three new models for inductance calculation are proposed; Section V details the procedure to design the optimum device; Section VI validates the proposed procedure and, in Section VII, the main conclusions extracted from the process are presented.

II. Micro-inductor model

The physical model of the micro-inductor is depicted in Fig. 1. As shown in the picture, the racetrack inductor is a stretched circular spiral, where the magnetic core wraps the straight parts of the conductors. A detail of the cross-section of the inductor is also depicted in the picture, with a close-up view of the rectangular section of the conductor.

To determine the inductor dimensions, it is very helpful to consider the device form factor D_{FF}, a parameter that relates the length D_l and the width D_w of the inductor (2). If this parameter is close to one, the component is almost a round spiral inductor with no magnetic core. On the other hand, as the form factor increases, the inductor becomes more elongated, and therefore the contribution of the magnetic core and the straight section of the tracks becomes more significant.

$$D_{Area} = D_l \cdot D_w \tag{1}$$

$$D_{FF} = \frac{D_l}{D_w} \tag{2}$$

This work was supported in part by the Spanish Ministry of Economy and Competitiveness and FEDER funds through the research project EPIIoT DPI2017-88062-R, in part by CarrICool EU FP7-ICT-619488 and in part by the Madrid Government (Comunidad de Madrid-Spain) under the Multiannual Agreement with UC3M in the line of Excellence of University Professors (EPUC3M26), and in the context of the V PRICIT (Regional Programme of Research and Technological Innovation).

J. López López, P. Zumel and C. Fernandez are with the Electronic Technology Department, Carlos III University of Madrid, Legans 28911, Madrid, Spain (e-mail: jailopez@ing.uc3m.es; pzumel@ing.uc3m.es; cfernand@ing.uc3m.es).

S. O'Driscoll, Z. Pavlovic and R. Murphy are with the Microsystems Center, Tyndall National Institute, T12 R5CP Cork, Ireland (e-mail: seamus.odriscoll@tyndall.ie; zoran.pavlovic@tyndall.ie; ruaidhri.murphy@tyndall.ie).

C. O'Mathuna is with the Microsystems Center, Tyndall National Institute, T12 R5CP Cork, Ireland, and also with the Department of Electrical Engineering, University College Cork, T12 YN60 Cork, Ireland (e-mail: cian.omathuna@tyndall.ie).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2021.3094631, IEEE Journal of Emerging and Selected Topics in Power Electronics

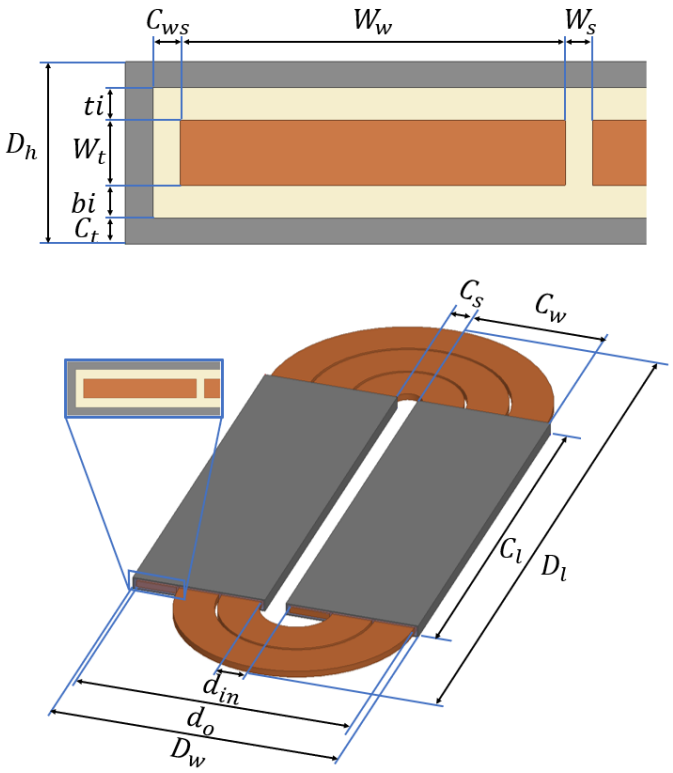

Fig. 1. Physical model of the racetrack inductor

In this section, the equations that model the inductance and losses of this racetrack are presented.

A. Inductance equations

Using the inductance models presented in [7], [10], [11], [12] and [13], the total inductance L of the device can be calculated as the sum of four terms (3): the inductance due to the presence of the core L_{core}, calculated as the squared number of turns N divided by the reluctance of the core (4); the inductance of the spirals outside the core L_{spiral} (5); the self inductance of the straight wires under the core $L_{w,self}$ (6); and the mutual inductances of the straight wires under the core $L_{w,mutual}$ (7).

$$L = L_{core} + L_{spiral} + L_{w,self} + L_{w,mutual} \tag{3}$$

$$L_{core} = 2\frac{\mu_0 \cdot \mu_r \cdot N^2 \cdot C_t \cdot C_l}{l_{mag}} \tag{4}$$

$$L_{spiral} = \frac{\mu_0}{4} N^2 \delta' \left[ln\left(\frac{2.46}{\delta/\delta'}\right) + 0.2\left(\frac{\delta}{\delta'}\right)^2 \right] \tag{5}$$

$$L_{w,self} = \frac{\mu_0 \cdot N \cdot C_l}{\pi} \left[\ln\left(\frac{2\,C_l}{W_t + W_w}\right) + \frac{1}{2} \right] \tag{6}$$

$$L_{w,mutual} = \frac{\mu_0 \cdot C_l}{\pi} \sum_{k=1}^{N-1} \sum_{j=k+1}^{N} \left[\begin{array}{c} \ln\left(\frac{2C_l}{(j-k)(W_w+W_s)}\right) - 1 \\ + \frac{(j-k)(W_w+W_s)}{C_l} - \left(\frac{(j-k)(W_w+W_s)}{2C_l}\right)^2 \end{array} \right] \tag{7}$$

where

$$l_{mag} = 2(C_w + W_t + ti + bi) \tag{8}$$

$$\delta = d_o - d_{in} \tag{9}$$

$$\delta' = d_o + d_{in} \tag{10}$$

Fig. 2 shows the accumulated contribution of each inductance term relative to the total inductance, versus the device form factor. Two scenarios are shown: a thin core ($C_t = 1\ \mu m$) with a low number of turns ($N = 2$); and a thick core ($C_t = 5\ \mu m$) with a relatively high number of turns ($N = 5$).

For a fixed D_{FF}, the thicker the core, the higher the impact of L_{core}, since the volume of magnetic material increases. The number of turns also has a major impact on L_{core}, since it is squared in equation (4).

As can be seen, the impact of L_{spiral} reduces as D_{FF} increases, since the contribution of the spirals lowers with respect to that of the core and the straight wires. At low D_{FF} values, L_{spiral} becomes important and can even be the main inductance driver when the length of the spiral is greater than that of the straight wire tracks.

For every form factor, the mutual inductance represents a very small amount of the inductance.

Once the device has an elongated shape, $D_{FF} > 3$, which is usually the case [7], the impact of every inductance term remains almost constant. The analysis of this term distribution is key for the new inductance models that are going to be proposed in Section IV.

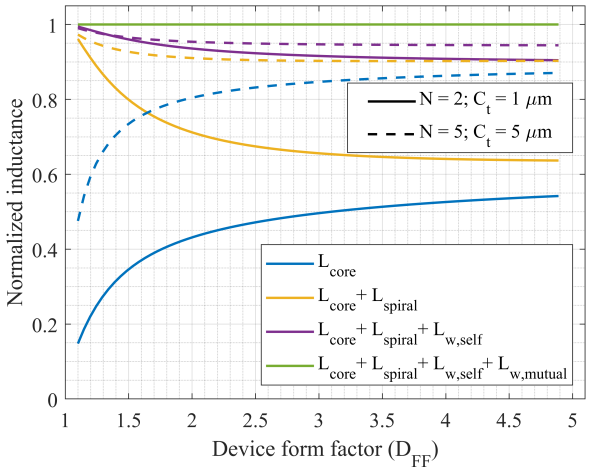

Fig. 2. Inductance terms distribution

B. Losses equations

Total loss, P, can also be divided in four terms (11), as described in [7]: DC loss in the wire, $P_{w,DC}$ (12); AC loss in the wire, $P_{w,AC}$ (13); hysteresis loss in the core, $P_{c,hyst}$ (14); and eddy current loss in the core, $P_{c,eddy}$ (15).

$$P = P_{w,DC} + P_{w,AC} + P_{c,hyst} + P_{c,eddy} \tag{11}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2021.3094631, IEEE Journal of Emerging and Selected Topics in Power Electronics

$$P_{w,DC} = R_{DC} \cdot I_{DC}^2 \tag{12}$$

$$P_{w,AC} = \sum_{k=1}^{k\ max} R_{AC,k} \cdot I_{k,rms}^2 \tag{13}$$

$$P_{c,hyst} = K_{hyst} \cdot f_{sw} \cdot \left(\frac{\Delta B_{pp}}{2}\right)^{\beta} \cdot C_{vol} \tag{14}$$

$$P_{c,eddy} = 2\frac{\rho_c\,(C_w + D_h)\,C_l}{C_t} \sum_{k=1}^{k\,max} v_k \frac{\sinh(v_k) - \sin(v_k)}{\cosh(v_k) + \cos(v_k)} H_k^2 \tag{15}$$

where

$$R_{DC} = \rho_{cu} \frac{l_{cu}}{W_w \cdot W_t} \tag{16}$$

$$l_{cu} = N\,(2\,C_l + \pi\,(C_s + C_w)) \tag{17}$$

$$\Delta B_{pp} = \frac{\mu_0 \cdot \mu_r \cdot N \cdot I_{k,peak}}{C_w + D_h} \tag{18}$$

$$C_{vol} = 2\ (C_t \cdot C_l \cdot l_{mag}) \tag{19}$$

$$\delta_c = \sqrt{\frac{\rho_c}{\mu_0 \cdot \mu_r \cdot \pi \cdot k \cdot f_{sw}}} \tag{20}$$

$$v_k = \frac{C_t}{\delta_c} \cdot \frac{\sqrt{\pi}}{2} \tag{21}$$

$$H_k = \frac{N \cdot I_{k,peak}}{2 \cdot\ (C_w + D_h)} \tag{22}$$

where subscript k represents the $k'th$ harmonic of the wave.

Wire AC loss, $P_{w,AC}$, usually has a small weight in the total loss calculation, and proximity effect is usually not significant at the frequencies of operation (10's of MHz) due to the spacing between conductors [14]. Thus, a good approximation for R_{AC} is the 1-D Dowell method, which provides a good trade off between accuracy and complexity [8]:

$$R_{AC,k} = F_k \cdot R_{DC} \tag{23}$$

where

$$F_k = \theta_k \left[\frac{\sinh(2\theta_k) + \sin(2\theta_k)}{\cosh(2\theta_k) - \cos(2\theta_k)} - \frac{1}{2}\frac{\sinh(\theta_k) - \sin(\theta_k)}{\cosh(\theta_k) + \cos(\theta_k)}\right] \tag{24}$$

$$\theta_k = \frac{W_t}{\delta_w} \tag{25}$$

$$\delta_w = \sqrt{\frac{\rho_{cu}}{\mu_0 \cdot \pi \cdot k \cdot f_{sw}}} \tag{26}$$

If this approximation does not suffice, the ones presented in [15] and [16], with increasing complexity, can be used.

Fig. 3 shows the contribution of each loss term relative to the total loss versus the device form factor, for the same design parameters that are going to be used later in the design example and a fixed N of 2. For this comparison among the loss terms, D_{Area} and N are fixed and C_t takes the value needed to maintain a constant specified inductance (L_s) of 14.4 nH for every D_{FF}.

As can be seen, the main loss drivers are $P_{w,DC}$ and $P_{c,eddy}$. $P_{c,eddy}$ dominates when D_{FF} is low, since the device has very short tracks and most of the inductance comes through having a thicker core and more material, which increases core loss. In contrast, $P_{w,DC}$ dominates for high D_{FF} values, where the tracks are much longer and provide much more inductance, reducing the need of core material but increasing wire loss.

Although $P_{w,AC}$ and $P_{c,hyst}$ usually represent a small amount of the total loss, there is no loss term that is the most or the least relevant for every D_{FF} value, so every loss contributor has to be taken into account.

The diamonds in Fig. 3 are the results from FEA simulations. As can be seen, simulations and calculations are in excellent agreement for form factors (D_{FF}) higher than 2.2. For lower D_{FF}, the power loss due to eddy currents increases due to the edge effect, which is not considered in the analytic model. The high accuracy of the model for aspect ratios of the magnetic core higher than 2 was already described in [7]. Nevertheless, it is important to highlight that for such low factor forms, the racetrack geometry is not so interesting, and a coreless inductor would be an acceptable option.

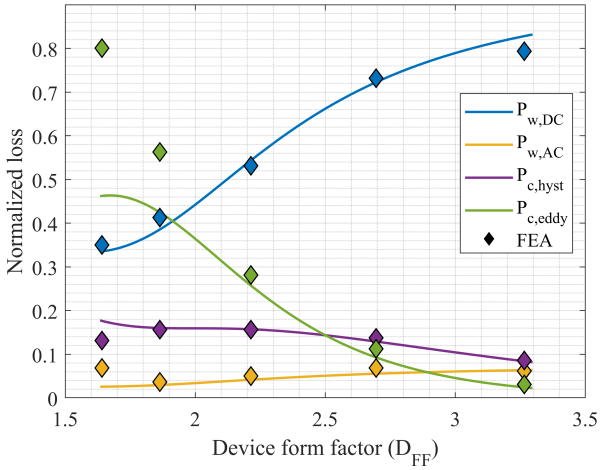

Fig. 3. Loss terms distribution

III. Problem Statement

In general, the inductor specifications from the designer's point of view are inductance, L, power loss, P, operating frequency, f_{sw}, rms and peak current through the device (I_{rms} and I_{peak} respectively) and maximum area that the device can occupy, $D_{Area,max}$. To build the optimum device with these specifications and using the previously presented model, the designer needs to obtain the best combination of number of turns N, core thickness C_t, wire thickness W_t, turn width W_w, and the remaining dimensions shown in Fig. 1.

As shown in equations (3) to (26), inductance L and power loss P depend on many physical parameters, making the number of possible designs, for a given specification, very high. The most common approach to solve the issue is to find the optimum device using numerical methods, iterating through every possible parameter combination [9], [17].

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2021.3094631, IEEE Journal of Emerging and Selected Topics in Power Electronics

This optimization process yields the best design from the formulation of cost functions. However, it has some disadvantages, with loss of physical insight being one of them. Consequently, it becomes difficult to compare the achieved optimum design with other designs that are similar but not considered optimum, and which may present other advantages, difficult to formulate in a cost function, such as a decrease in the manufacturing complexity [18]. An added drawback of the numerical approach comes from the complexity of the equations and the amount of data generated by solving them for every parameter combination. Both aspects are time and resource consuming, making it hard to include the design of the microinductor in the optimization procedure of the whole power converter.

To overcome the problems of the amount of data generated (related to the number of variables) and the lack of physical insight (due to the numerical method), a new procedure for the design of racetrack microinductors is proposed in this paper.

To increase power density, these inductors can be built on top of the rest of the power converter (semiconductors, capacitors and control circuit) [19], [20]. Thus, the maximum allowable area is fixed for a given design. Additionally, as already studied in [10], the largest area always yields the lowest losses, so the selected device area, D_{Area}, can be set to that maximum value, $D_{Area,max}$.

To increase power density even further, other geometrical parameters (namely W_s, C_{ws}, C_s, bi, and ti) can be set to the minimum values allowed by the manufacturing technology, while wire thickness W_t, can be set to its maximum value to minimize DC resistance. Doing so, the design variables can be reduced to only three: number of turns N, core thickness C_t and device form factor D_{FF}.

In (27-34), presented in Table I, the geometrical parameters required to compute the inductor model are expressed as a function of the three design variables N, C_t and D_{FF}, and the fixed geometrical parameters D_{Area}, W_t, W_s, C_{ws}, C_s, bi, and ti.

The minimum wire width ($W_{w,min}$) may be limited by the technology, but there is also a minimum width not to exceed the maximum specified temperature increase ΔT (35) [7]. And, for a given area, the shape of the device, defined by its form factor (D_{FF}), can take any value from 1 (same length as width) to the maximum $D_{FF,max}$ (37), (an elongated device with D_l as big as possible and the smallest D_w). This minimum device width ($D_{w,min}$), where only one turn of wire can be fitted while maintaining C_t set to its maximum ($C_{t,max}$), can be calculated using (36).

The definition of the design constants, along with the values used in the next examples, are presented in Table II.

In this paper the design problem is stated as follows: given the specifications in terms of inductance L_s, DC value and current ripple, I_{DC} and $I_{1st,peak}$ respectively (only the 1st harmonic is considered), frequency of the current ripple f_{sw}, and maximum device area D_{Area}, find the combination of number of turns N, core thickness C_t and form factor D_{FF} that yields the optimum design.

TABLE I
MAIN PHYSICAL RELATIONSHIPS

Design variables (unknowns)	N, C_t, D_{FF}
Design constants	D_{Area}, W_t, W_s, C_{ws}, C_s, bi, ti

$$D_l = \sqrt{D_{Area} \cdot D_{FF}} \tag{27}$$

$$D_w = \sqrt{\frac{D_{Area}}{D_{FF}}} \tag{28}$$

$$C_w = \frac{D_w - C_s}{2} \tag{29}$$

$$d_o = D_w - 2C_{ws} - 2C_t \tag{30}$$

$$d_{in} = C_s + 2C_{ws} + 2C_t \tag{31}$$

$$C_l = D_l - d_o = D_l - D_w + 2C_{ws} + 2C_t \tag{32}$$

$$D_h = 2C_t + W_t + ti + bi \tag{33}$$

$$W_w = \frac{C_w - (N-1)W_s - 2C_{ws} - 2C_t}{N} \tag{34}$$

$$W_{w,min} = \frac{\left(\frac{I_{RMS}}{k_W \cdot \Delta T^b W}\right)^{1/c_W}}{W_t} \cdot \left(25.4 \cdot 10^{-6}\right)^2 \tag{35}$$

$$D_{w,min} = C_s + 4C_{t,max} + 4C_{ws} + 2W_{w,min} \tag{36}$$

$$D_{FF,max} = \frac{D_{Area}}{D_{w,min}^2} \tag{37}$$

TABLE II
DESIGN EXAMPLE PARAMETERS

Parameter	Description	Value
W_s	Wire-to-wire spacing	15 μm
C_{ws}	Core-to-wire spacing	15 μm
C_s	Core-to-core spacing	250 μm
W_t	Wire thickness	15 μm
C_t	Core thickness	0.25 - 5 μm
bi	Bottom insulator thickness	10 μm
ti	Top insulator thickness	65 μm
	Core material	$Ni_{45}Fe_{55}$
B_{sat}	Saturation flux density	1.4 T
μ_0	Vacuum permeability	$4\pi \cdot 10^{-7}$
μ_r	Relative permeability of the core	280
K_{hyst}	Steinmetz K factor	300
β	Steinmetz β factor	1.73
ρ_{core}	Core resistivity	$0.45 \cdot 10^{-6}$ Ω·m
ϵ_0	Permittivity of free space	$8.85 \cdot 10^{-12}$ F/m
ϵ_r	Relative permittivity of the insulator	4.5
ρ_{cu}	Copper resistivity	$1.72 \cdot 10^{-8}$ Ω·m
μ_{cu}	Relative permeability of the copper	1
ΔT	Allowed inductor temperature rise	80 K
k_W	k factor for Minimum Wire Width	0.048
b_W	b factor for Minimum Wire Width	0.44
c_W	c factor for Minimum Wire Width	1
I_{DC}	DC current	0.29 A
f_{sw}	Frequency	150 MHz
$I_{1st,peak}$	Peak value of current's first harmonic	0.1 A
D_{Area}	Device Area	0.813 mm^2
L_s	Specified inductance	14.4 nH

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2021.3094631, IEEE Journal of Emerging and Selected Topics in Power Electronics

IV. Proposed models

The inductor model described in sections II and III contains nonlinear relationships between the design variables (N, C_t and D_{FF}) that are difficult to manage in terms of having a straightforward approach to analysing the influence of every design variable.

In this section, three simplified models, with linear relationships between the design variables, are proposed to establish the design procedure.

A. Model 1

In (3), both $L_{w,self}$ and $L_{w,mutual}$ contain a natural logarithm where N and C_t are present in both numerator and denominator, making them transcendental functions, which can not be easily solved. Since $L_{w,self}$ and $L_{w,mutual}$ are usually the less significant inductance terms [7], in this first approach they are omitted, so the inductance can be calculated by means of (38).

$$L_1 = L_{core} + L_{spiral} \tag{38}$$

Because of the simplicity of this model, it is possible to calculate the number of turns as a function of D_{FF} and C_t (39) to achieve a specified inductance L_s.

$$N_1(C_t,D_{FF}) = \sqrt{\frac{L_s}{\frac{\mu_0\delta'}{4}\left[\ln\left(\frac{2.46}{\delta/\delta'}\right)+0.2\left(\frac{\delta}{\delta'}\right)^2\right]+\frac{2\mu_0\mu_r C_t C_l}{l_{mag}}}} \tag{39}$$

L_1 equals $L_{core} + L_{spiral}$ so its accuracy is lower for low values of N and high values of D_{FF}. The lowest accuracy of L_1, for the example shown in Fig. 2 ($N = 2$, $C_t = 1\mu m$) is only of 64%.

This model can serve as a good initial approximation to calculate the number of turns, but may yield a considerable error depending on the relative impact of $L_{w,self}$ and $L_{w,mutual}$. Since their values are not taken into account to achieve a specified inductance L_s, they have to be compensated with additional L_{core} and L_{spiral}. This results in a predicted number of turns N_1, equal to or higher than the the required N, considering the complete model.

B. Model 2

The model can be improved in a second step by also including $L_{w,self}$. However, this expression includes a natural logarithm containing C_t and N. To overcome this inconvenience, $L_{w,self}$ can now be made dependent only on C_t by substituting N_1 (39) for N in (6). This way, a better approximation for inductance can be derived as:

$$L_2 = L_{core} + L_{spiral} + L_{w,self}|_{N=N_1} \tag{40}$$

L_2 is very close to $L_{core} + L_{spiral} + L_{w,self}$. As shown in Fig. 2, that sum of inductances make up for up to 95% of total inductance if N and C_t are at their highest, even for the highest D_{FF}. Also notice that since $N_1 \geq N$, $L_{w,self}|_{N=N_1}$ is always going to be equal to or higher than $L_{w,self}$, so the absence of $L_{w,mutual}$ in the model is partially compensated.

With this model, N can be more accurately calculated to achieve the specified inductance L_s, by means of (41).

$$N_2(C_t, D_{FF}) = \frac{-b_N + \sqrt{b_N^2 - 4\,a_N\,c_N}}{2\,a_N} \tag{41}$$

where:

$$a_N = \frac{\mu_0\delta'}{4}\left[\ln\left(\frac{2.46}{\delta/\delta'}\right) + 0.2\left(\frac{\delta}{\delta'}\right)^2\right] + \frac{2\mu_0\,\mu_r\,C_t C_l}{l_{mag}} \tag{42}$$

$$b_N = \frac{C_l\mu_0}{\pi}\left[\ln\left(\frac{2\,C_l}{W_t - \frac{2C_t - C_w + 2C_{ws} + W_s\,(N_1-1)}{N_1}}\right) + \frac{1}{2}\right] \tag{43}$$

$$c_N = -L_s \tag{44}$$

This model allows the calculation of the required number of turns N, for a particular core thickness C_t. However, it does not allow calculation of the core thickness C_t for a given number of turns N and form factor D_{FF}.

C. Model 3

In this approach, some physical approximations can be made to reduce the complexity of the equations by getting rid of some terms that may be neglected.

- To approximate L_{core}: if the core thickness is much lower than the core length ($C_t << C_l$), (32) can be approximated by (45) and the inductance due to the core can then be approximated as (46).

$$C_l(C_t, D_{FF}) \approx C_{l3}(D_{FF}) = D_l - D_w + 2C_{ws} \tag{45}$$

$$L_{core,3} = \frac{2N^2 \cdot \mu_0 \cdot \mu_r \cdot C_t \cdot (D_l - D_w + 2C_{ws})}{l_{mag}} \tag{46}$$

- To approximate L_{spiral}: If the core thickness is much lower than the outer diameter of the spiral ($C_t << d_o$) and also lower than the internal diameter of the spiral ($C_t << d_{in}$), (30), (31), (9) and (10) can be approximated by (47), (48), (49) and (50) respectively. Thus, the inductance of the spiral can be calculated by means of (51).

$$d_o \approx d_{o3} = D_w - 2C_{ws} \tag{47}$$

$$d_{in} \approx d_{in3} = C_s + 2C_{ws} \tag{48}$$

$$\delta \approx \delta_3 = D_w - 4C_{ws} - C_s \tag{49}$$

$$\delta' \approx \delta'_3 = D_w + C_s \tag{50}$$

$$L_{spiral,3} = \frac{\mu_0}{4}N^2\delta'_3\left[\ln\left(\frac{2.46}{\delta_3/\delta'_3}\right) + 0.2\left(\frac{\delta_3}{\delta'_3}\right)^2\right] \tag{51}$$

- To approximate $L_{w,self}$: if $C_t << 0.5 \cdot N \cdot W_w$ and $C_t << C_l$, (34) can be approximated by (52), and the self inductance of the straight wires can be calculated using (53).

$$W_w \approx W_{w3} = \frac{C_w - (N-1)W_s - 2C_{ws}}{N} \tag{52}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2021.3094631, IEEE Journal of Emerging and Selected Topics in Power Electronics

$$L_{w,self,3} = \frac{N\,\mu_0\,(2\,C_{ws} + D_l - D_w)}{\pi} \cdot \left[\ln\left(\frac{2\,(2\,C_{ws} + D_l - D_w)}{W_t + \frac{C_w-(N-1)W_s-2C_{ws}}{N}}\right) + \frac{1}{2}\right] \quad (53)$$

- To approximate $L_{w,mutual}$: taking the previous assumptions, W_w can be substituted by W_{w3} and C_l by C_{l3} in (7). By doing so, the mutual inductance of the straight wires can be calculated using (54).

$$L_{w,mutual,3} = \frac{\mu_0 \cdot C_{l3}}{\pi} \sum_{k=1}^{N-1} \sum_{j=k+1}^{N} \left[\begin{array}{c} \ln\left(\frac{2C_{l3}}{(j-k)(W_w+W_s)}\right) - 1 \\ + \frac{(j-k)(W_{w3}+W_s)}{C_{l3}} - \left(\frac{(j-k)(W_{w3}+W_s)}{2C_{l3}}\right)^2 \end{array}\right] \quad (54)$$

Taking into account all the previous approximations, a new model to calculate the inductance L_3 is introduced (55).

$$L_3 = L_{core,3} + L_{spiral,3} + L_{w,self,3} + L_{w,mutual,3} \quad (55)$$

Since C_t is not inside a natural logarithm anymore, it can be found, to achieve a specified inductance L_s, by means of (56).

$$C_{t,3}(N, D_{FF}) = \frac{C_w + W_t + bi + ti}{N^2\,\mu_0\,\mu_r\,(2\,C_{ws} + D_l - D_w)} \cdot \cdot (L_s - L_{spiral,3} - L_{w,self,3} - L_{w,mutual,3}) \quad (56)$$

L_3, is very close to L ($L_{core} + L_{spiral} + L_{w,self} + L_{w,mutual}$), but with some geometric approximations. Since C_t is omitted in some calculations, the predicted inductance is slightly smaller than L. This last model has the advantage of providing a way to calculate the needed core thickness C_t for any D_{FF} and N, with a very high degree of accuracy.

D. Discussion of the models

As a conclusion, the combination of the three proposed simplified models allows for easy expressions that can relate the three design variables: number of turns N, core thickness C_t and device form factor D_{FF}.

However, when using a simplified model, there is always a trade-off between accuracy and complexity. An example of the error in the inductance predicted by every model compared to the complete model, for $N = 2$ and $C_t = 2.62\,\mu m$, is shown in Fig. 4. The diamonds in this figure are the total inductance obtained from FEA simulations normalized with respect to L. These results are in good agreements with the calculations, with a difference always below $\pm 2\%$.

The error incurred by using Model 1 makes it unsuited to be used as an approximation for L, and so, it is only used as a needed step to estimate $L_{w,self}$ in Model 2. Model 2 shows an acceptable error, similar to the difference between $L_{core}+L_{spiral}+L_{w,self}$ and L (composed by $L_{core}+L_{spiral}+L_{w,self}+L_{w,mutual}$) in Fig. 2 and is used to calculate N. Model 3, which takes into account every inductance term, presents a very small error, and is used to calculate C_t with a high precision. These errors result always in the overestimation of D_{FF}, N or C_t to compensate the absence of $L_{w,mutual}$ in Model 2 and the geometric approximations in Model 3.

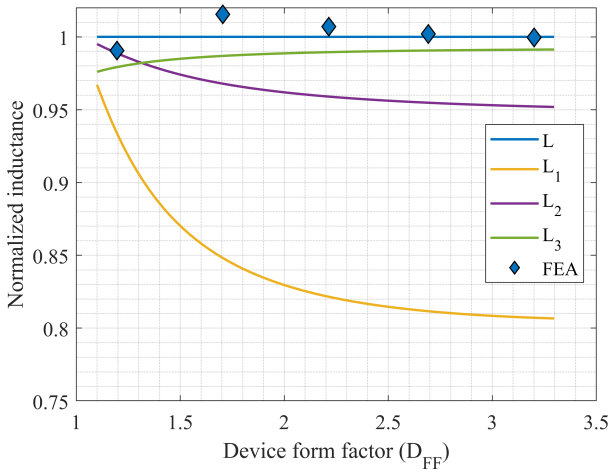

Fig. 4. Inductance predicted by every model

This error when calculating inductance implies the designed device is not the one that exactly meets specifications, but a close one (in terms of the selection of D_{FF}, N and C_t). As stated before, for every D_{FF}, there would be an overestimation of N and/or C_t when using any of the models. The overestimation of N means the wire will be longer and thinner than needed, increasing wire loses ($P_{w,DC}$ and $P_{w,AC}$) and the overestimation of C_t means there will be more core material than is really needed, increasing core losses ($P_{c,hyst}$ and $P_{c,eddy}$).

To analyse the impact of the models on the losses, a different test has been conducted. For instance, for Model 1 and a given D_{FF}, the number of turns N_1 was calculated by means of (39) and the core thickness was adjusted by an iterative approach to determine the core thickness $C_{t,1}$ required to obtained $L_1 = 14.4nH$. The resulting number of turns N_1 and core thickness $C_{t,1}$ have been used to calculate the total loss using the complete model $P(N_1, C_{t,1})$. A similar procedure was used to calculate the number of turns and core thickness for models 2 and 3 and compute their total loss.

The results are depicted in Fig. 5, which represents the comparison of the loss achieved with the different models compared to the complete model. As explained before, the FEA results (shown as diamonds in the figure) match with high accuracy the losses for D_{FF} higher than 2.2, with a difference within $\pm 2.5\%$. However, this accuracy depends on the design of the component itself due to the relative contribution of the eddy loss compared to other losses, as depicted in Fig. 3. In this particular example, the maximum deviation of the loss is 30% for the worst case. In that case the core is very short and the edge effect plays an important role. Moreover, the number of turns is low and eddy losses are dominant. In other designs with higher number of turns, the losses due to the wire could make the relative contribution of the eddy loss less important, and thus the accuracy of the model would increase.

As can be seen in Fig. 5, the overestimation of N and/or

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2021.3094631, IEEE Journal of Emerging and Selected Topics in Power Electronics

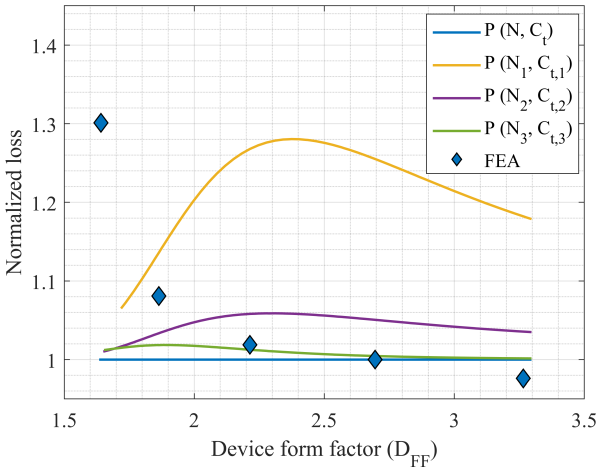

Fig. 5. Loss predicted by every model

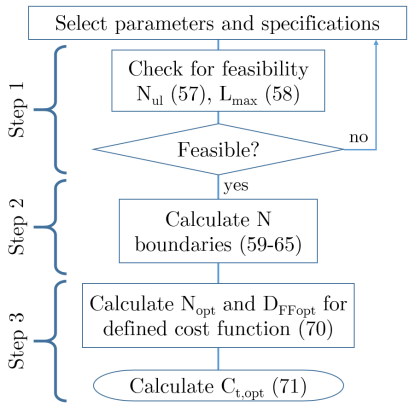

Fig. 6. Flowchart of the inductor optimization procedure

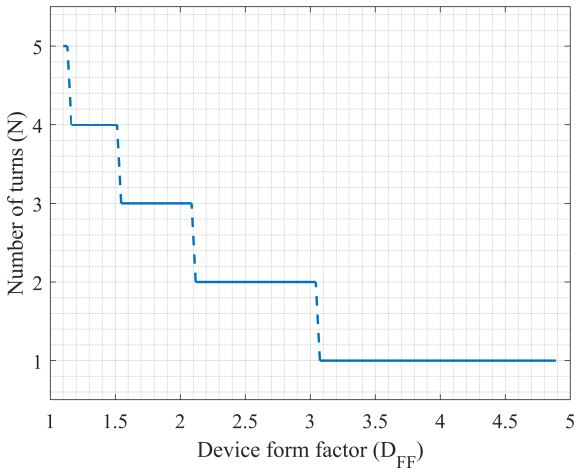

Fig. 7. Upper limit for the number of turns (N_{ul})

C_t when using Model 1 results in a device with losses $P(N_1, C_{t,1})$ much higher than $P(N, C_t)$ (up to 28% increase for this particular example) which, again, makes it unsuited for the design. $C_t(N_1)$ has been calculated iteratively using expression (38). On the other hand, the increase in losses due to the use of Model 2, needed to calculate N, is considered acceptable in exchange for the reduction in complexity (less than 6% increase for this particular example). Model 3, which is used to finely adjust the value of C_t to meet the specifications, presents a very small error, as it does when calculating inductance.

The small difference between the losses predicted by Model 3, and the ones calculated using the model without any approximation, ensures the designed device is very close to the optimum one.

V. Design Procedure

In this section, a new design procedure, using the models presented in the section IV, is detailed. The flowchart for the proposed procedure is shown in Fig. 6 and, to illustrate the process, an example of the output of every step, using the values provided in Table II, is shown in figures 7 to 10.

A. Step 1: Check feasibility of the solution

The maximum possible inductance is achieved by using the maximum amount of core material (C_t) while fitting the maximum number of turns (N).

The upper limit of the number of turns (N_{ul}) that can fit in the device, depends on the minimum wire width ($W_{w,min}$) and the maximum core thickness $C_{t,max}$ (57). Notice that, since the number of turns has to be discrete, N_{ul} is rounded down.

$$N_{ul}(D_{FF}) = floor\left(\frac{C_w - 2\,C_{ws} - 2\,C_{t,max} + W_s}{W_s + W_{w,min}}\right) \quad (57)$$

N_{ul} is different for every device form factor. For a given area, and the values provided in Table II, the upper limit for the number of turns for any possible form factor is shown in Fig. 7.

Once the limit for the number of turns is known, N can be substituted by N_{ul} in equations (3) to (7) and the maximum achievable inductance (L_{max}) can be calculated as:

$$L_{max} = L|_{N=N_{ul}, C_t=C_{t,max}} \quad (58)$$

For the values provided in Table II, the maximum achievable inductance for any possible form factor is shown in Fig. 8. The sawtooth shape of the curve derives from rounding down of the number of turns shown in Fig. 7. Since N has a major impact on inductance value (equations (3) - (10)), the D_{FF} values where there is a change on the maximum number of turns show a very pronounced difference in achievable inductance. This highlights the big impact that very small differences in geometry (D_{FF}) can have when designing a microinductor.

If the specified inductance value (purple line in Fig. 8) is lower than the maximum inductance (blue line), the value is achievable for the valid form factors (D_{FF}). Otherwise, the design should be stopped at this point and the specifications should be revised.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2021.3094631, IEEE Journal of Emerging and Selected Topics in Power Electronics

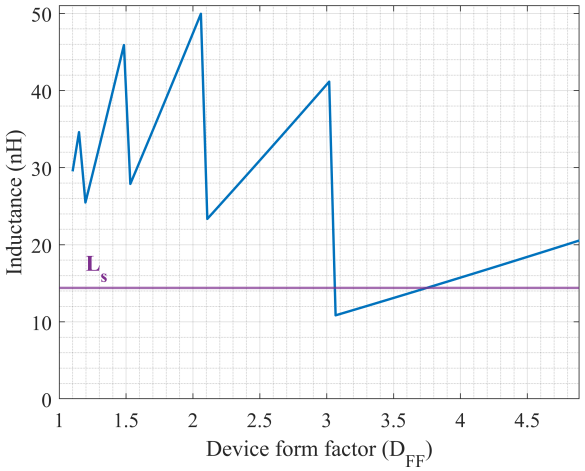

Fig. 8. Maximum achievable inductance (L_{max})

B. Step 2: Valid number of turns

Next, the values that the number of turns can take to provide the specified inductance are found. In this step, Models 2 and 3 are used.

To obtain the minimum needed number of turns to achieve a specified inductance (N_{min}), C_t can be substituted by its maximum value, $C_{t,max}$ in (41).

$$N_{min} = ceil(\,N_2|_{C_t=C_{t,max}}) \tag{59}$$

For the maximum number of turns (N_{max}), 3 conditions have to be met.

- The specified inductance is achieved.
  The maximum number of turns to achieve a given inductance can be obtained substituting C_t by $C_{t,min}$ in (41):
$$N_{max,L} = N_2|_{C_t=C_{t,min}} \tag{60}$$
- The maximum temperature increase is not reached.
  To ensure the temperature stays within its allowed range, W_w has to be higher than $W_{w,min}$, which translates into:
$$N_{max,T} = \frac{C_w + W_s - 2C_{ws}}{W_{w,min} + W_s} \tag{61}$$
- The device will not saturate at maximum current.
  The maximum current to avoid saturating the core can be calculated as:
$$I_{sat} = B_{sat}\frac{2(C_w + 2\,C_t + W_t + bi + ti)}{\mu_0\mu_r N} \tag{62}$$
  I_{sat} can be made dependent only on N by assuming $C_t << (C_w + W_t + bi + ti)$, as done in Model 3:
$$I_{sat,3} = B_{sat}\frac{2(C_w + W_t + bi + ti)}{\mu_0\mu_r N} \tag{63}$$
  The maximum N that avoids saturation is then calculated as:
$$N_{max,B} = B_{sat}\frac{2(C_w + W_t + bi + ti)}{\mu_0\mu_r\,(I_{DC}+I_{k,peak})} \tag{64}$$

The maximum number of turns that ensures the three conditions are met is calculated as the lowest of the three maximum limits:

$$N_{max} = floor(\min(N_{max,L}, N_{max,T}, N_{max,B})) \tag{65}$$

Once the maximum and minimum values are known, the selected N will always be between them:

$$N_{min} \leqslant N \leqslant N_{max} \tag{66}$$

For the values provided in Table II, the valid numbers of turns are shown in Fig. 9. Any value between or on the yellow and blue lines, is a valid number of turns for a given form factor.

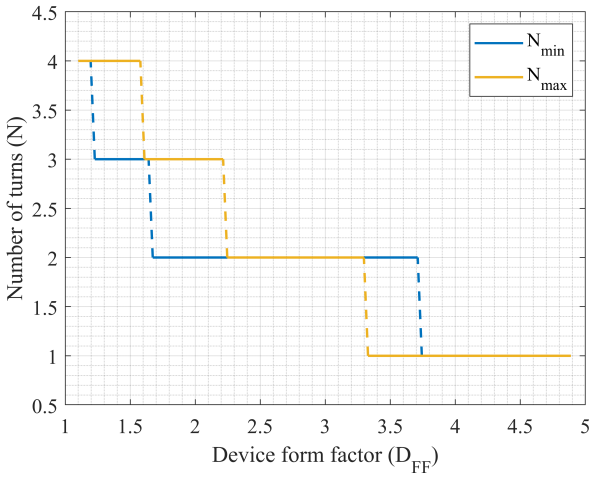

Fig. 9. Boundaries for the number of turns (N)

C. Step 3: Optimum device

Once the valid number of turns for every D_{FF} is known, the optimum device can be found. This procedure can be adapted to the use of any cost function, as long as it can be expressed as functions of D_{FF}, N and C_t. In the present example, the cost functions are total loss and device volume and the optimum device is defined as that with the minimum loss.

Total loss can be approximated using (67) by substituting C_t by $C_{t,3}$ in (11) and thus making it dependant only on N and D_{FF}.

$$P_3(N, D_{FF}) = P|_{C_t=C_{t,3}} \tag{67}$$

The local minimums for this cost function are defined by (68) and (69):

$$\frac{\partial P_3(N, D_{FF})}{\partial D_{FF}} = 0 \tag{68}$$

$$\frac{\partial^2 P_3(N, D_{FF})}{\partial D_{FF}^2} > 0 \tag{69}$$

Since the D_{FF} range for every number of turns is limited, being a local minimum does not suffice to be an absolute minimum and the value at the boundaries (minimum and

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2021.3094631, IEEE Journal of Emerging and Selected Topics in Power Electronics

maximum D_{FF} values for every number of turns) has also to be checked. Thus, the combination of N and D_{FF} that yields the optimum device is defined as that which provides the total minimum power loss:

$$\{N_{opt}, D_{FFopt}\} = \{N, D_{FF}\}\,|_{P_3=\min(P_3)} \tag{70}$$

For the values provided in Table II and the valid numbers of turns previously calculated (Fig. 9), the resulting total losses are shown in Fig. 10. The optimum device, resulting from the previous calculation, is highlighted with a yellow diamond.

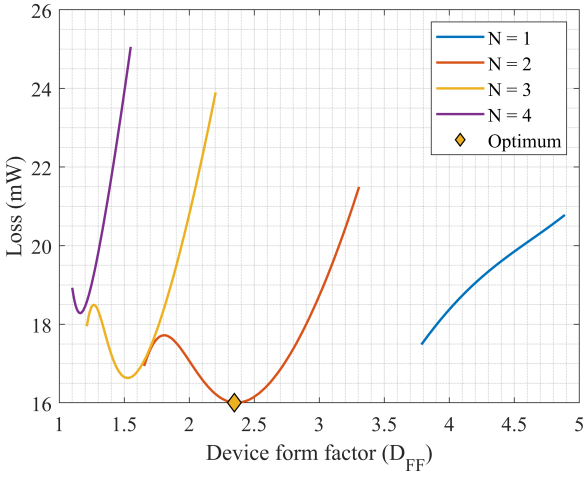

Fig. 10. Losses (P_3) for every number of turns (N)

Once the optimum N and D_{FF} are known, the only remaining design variable, C_t, can be calculated using (71).

$$C_{t,opt} = C_{t,3}(N_{opt}, D_{FFopt}) \tag{71}$$

After this last step, every physical parameter is known:

- W_s, C_{ws}, C_s, bi, and ti are set to their minimum values to increase power density.
- W_t and D_{Area} are set to their maximum to reduce losses.
- D_{FF}, N and C_t have their optimum values, given by the presented design procedure.

The calculation of the remaining parameters shown in Fig. 1 is straightforward using equations (27)-(34) and so, every physical dimension is known and the optimum device can be built.

Even though the design could stop at this point, the previous figures shown in this section highlight one of the advantages of the presented procedure over the traditional numerical approximation: the physical insight on the design. The two most important conclusions extracted from those figures are:

- As can be seen in figures 7 to 10, there are very big differences in the designed device when there is a change in the number of turns (shown as steps or discontinuities in the graphs). So, even if the area and shape of the inductor were in principle to be imposed by the rest of the circuit, slight modifications in that area could yield big improvements for the inductor by enabling a wider range of number of turns.
- As shown in Fig. 10, even though there is only one optimum device, there can be designs that, with only a slight decrease in performance, could be more interesting from the manufacturing point of view, for example by reducing the number of turns (and making them wider and more immune to process variability) or reducing core thickness (C_t) (reducing processing time and cost).

VI. Validation of the Design Procedure

The proposed procedure has been compared to a numerical approach based on the calculation of all possible inductor designs taking into account all the combinations of the physical parameters (summarized in Table II). The resulting 300,000 designs are shown in Fig. 11 as blue dots. Superimposed on them there are two diamonds: the optimum device given by the numerical approximation, in purple, and the one given by the proposed procedure, in yellow (corresponding to the one shown in Fig. 10). The proposed procedure achieves a near optimal design while dramatically reducing the amount of processed data.

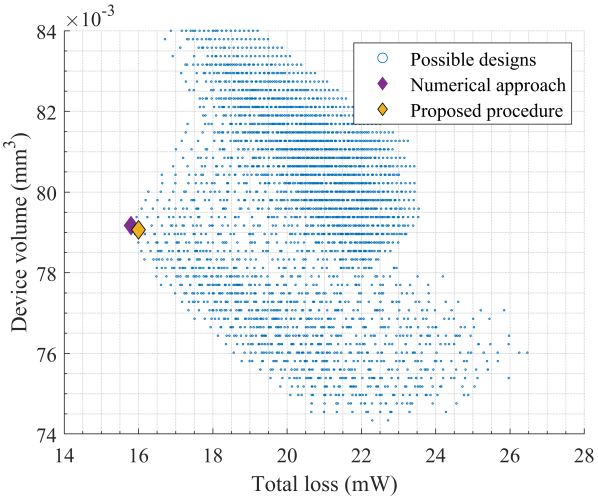

Fig. 11. Numerical results and optimum devices

The main parameters of the output designs obtained by the numerical approximation and the proposed procedure are shown in Table III. The detailed comparison of both designs is shown in Fig. 12 (inductance) and Fig. 13 (losses). As shown, the designs obtained by calculating thousand of possible parameter combinations using the complete inductance and loss models and the one resulting from a single iteration of the proposed design procedure are almost the same. Both have the same N, there is less than a 1% deviation in C_t and D_{FF} and in inductance and loss.

As stated before, the difference in the calculations is due to a small overestimation of D_{FF} or C_t, which results in an excess of core material. This excess yields an inductance slightly higher than specified (Fig. 12) as well as slightly higher losses

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2021.3094631, IEEE Journal of Emerging and Selected Topics in Power Electronics

(Fig. 13). Since this error is always an overestimation, it can be partially compensated by reducing the value of C_t or D_{FF} given by the proposed model.

TABLE III
OPTIMUM DEVICE PARAMETERS

	N	C_t (μm)	D_{FF}	L (nH)	P (mW)
Numerical approach	2	2.04	2.347	14.4	15.9
Proposed procedure	2	2.06	2.347	14.52	16
Difference	-	+0.98%	0%	+0.9%	+0.6%

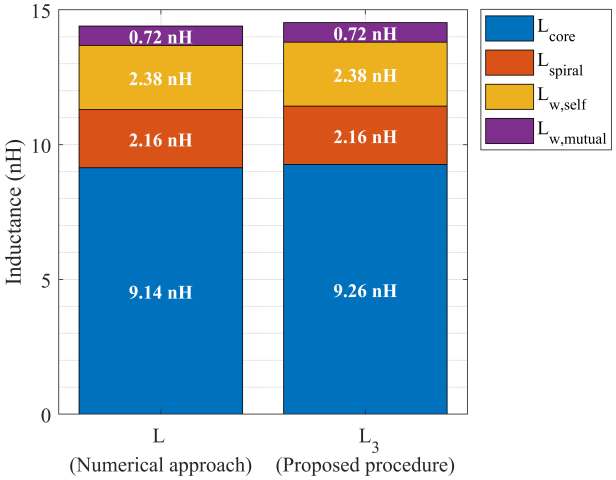

Fig. 12. Optimum devices inductance comparison

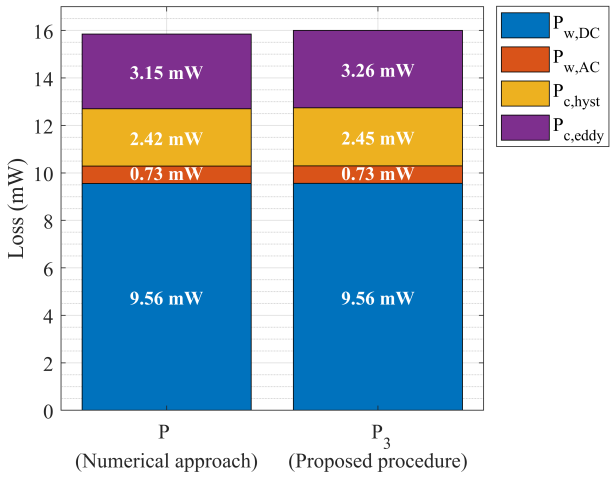

Fig. 13. Optimum devices losses comparison

Finally, to experimentally verify the accuracy of the analytical equations and the proposed models, a manufactured device has been modeled using Ansys Maxwell 3D as well as measured in the laboratory. Due to fabrication purposes, instead of manufacturing the optimized device in terms of losses (Table III), the choice was to use less core material with a reduced form factor. This device corresponds to the one with the lowest loss for $N = 3$ (Fig. 10), which has $C_t = 1.647\,\mu m$ and $D_{FF} = 1.53$. The fabricated microinductor is a coupled inductor with an additional winding, as shown in Fig. 14. This additional winding is not considered in our models. However, it has been used for the calculation of core losses in large-signal tests [21]. Voltage and current were measured using voltage probes and a sense capacitor, with the phase correction method described in [22], producing excitation signals in accordance to the specified DC and AC current through the device [23], shown in Table II. The used equipment are: three Tektronix TAP1500 voltage probes (1.5GHz), a Tektronix MD03104 mixed domain oscilloscope (5GS/s, 1GHz) and an Applied Research 25A250A power amplifier.

These measurements were used to calculate core losses. To separate between hysteresis and eddy current losses in the core, large signal measurements were done in a frequency range. Steinmetz parameters can be obtained from a low frequency measurement, where hysteresis losses are dominant.

The permeability value (μ_r) was initially measured on blanket magnetic material and was further adjusted to be consistent with inductance measurements of fabricated devices. The accuracy of the presented method is related to the material parameters in Table II, since they are essential to calculate the inductance and the losses.

The experimental measurements (with open secondary winding) and the finite element analysis (FEA) results are compared with our best design for $N = 3$ in Table IV. As can be seen, the values given by the analytical equations and the proposed model are in very good agreement with both measurements and FEA results, with the only discrepancy of eddy loss ($P_{c,eddy}$), which may be due to the unconsidered open winding. These results validate our proposal.

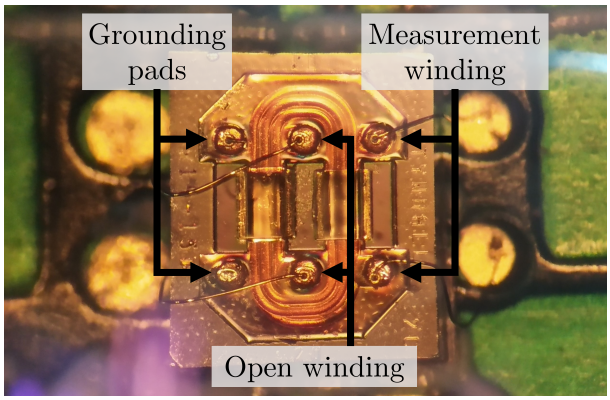

Fig. 14. Top view of the fabricated microinductor

VII. CONCLUSION

This paper presents a complete procedure for the design of a racetrack microinductor. In contrast to previously presented numerical approaches, it avoids the need to calculate for every parameter combination in order to design the optimum device. Additionally, the proposed process ensures critical design

TABLE IV
MEASUREMENTS AND FINITE ELEMENTS MODEL OF THE FABRICATED MICROINDUCTOR ($N = 3$, $C_t = 1.647\,\mu m$, $D_{FF} = 1.53$)

	L (nH)	P_w (DC+AC) (mW)	$P_{c,hyst}$ (mW)	$P_{c,eddy}$ (mW)
Proposed best design	14.3	13	1.8	1.6
Measurem.	14.4	13.7	1.8	4.2
FEA	14.5	12.6	1.2	1.2

requirements are met, the inductance value is achievable and the temperature rise will be kept below the specified value.

The new procedure is based on three proposed models for inductance calculation, which reduce the complexity of the equations and allows a simpler relationship between the design variables. This translates in a big reduction in the computation time of the design, and facilitates the integration of the inductor design in the design of a power converter.

A relevant contribution of the proposed procedure is the insight on the physical meaning of every step of the process, making it possible to identify potential strengths and weaknesses of the employed technology. This insight allows the designer to easily evaluate trade-offs when deciding which inductor to make, which is a hard task when using numerical methods. For example, slightly increasing the losses for a large reduction in magnetic material, or slightly changing the shape of the device for a large increase in performance.

An example of an inductor designed using the proposed method, has been compared to the optimum design calculated by a conventional approach, based on the analysis of all possible physical combinations. Discrepancies between the two designs are less than 1% in inductance and losses, confirming the accuracy of the proposed straightforward procedure.

Finally, to validate the analytical equations and the models, a manufactured device has been measured. The theoretical results match both measurements and finite element simulations, which ensures the suitability of the proposal.

REFERENCES

[1] S. Kulkarni, D. Li, D. Jordan, N. Wang, and C. O. Mathuna, "PCB Embedded Bondwire Inductors with Discrete Thin-Film Magnetic Core for Power Supply in Package," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 2, pp. 614–620, 2018.

[2] E. Haddad, C. Martin, C. Joubert, B. Allard, C. Buttay, T. A. Tannous, and P. Bevilacqua, "Planar, double-layer magnetic inductors for low power, high frequency DC-DC converters," *CIPS 2014 - 8th International Conference on Integrated Power Electronics Systems, Proceedings*, pp. 25–27, 2014.

[3] C. Feeney, M. Duffy, and C. O'Mathuna, "Design procedure for inductors-on-silicon in power supply on chip applications," *Proceedings of the Universities Power Engineering Conference*, 2013.

[4] R. Meere, T. O'Donnell, N. Wang, N. Achotte, S. Kulkarni, and S. C. O'Mathuna, "Size and performance tradeoffs in micro-inductors for high frequency DC-DC conversion," *IEEE Transactions on Magnetics*, vol. 45, no. 10, pp. 4234–4237, 2009.

[5] C. R. Sullivan, D. V. Harburg, J. Qiu, C. G. Levey, and D. Yao, "Integrating magnetics for on-chip power: A perspective," *IEEE Transactions on Power Electronics*, vol. 28, no. 9, pp. 4342–4353, 2013.

[6] D. V. Harburg, A. J. Hanson, J. Qiu, B. A. Reese, J. D. Ranson, D. M. Otten, C. G. Levey, and C. R. Sullivan, "Microfabricated Racetrack Inductors with Thin-Film Magnetic Cores for On-Chip Power Conversion," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 3, pp. 1280–1294, 2018.

[7] C. Feeney, N. Wang, S. Cian O'Mathuna, and M. Duffy, "Design Procedure for Racetrack Microinductors on Silicon in Multi-MHz DC-DC Converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6897–6905, 2015.

[8] T. M. Andersen, C. M. Zingerli, F. Krismer, J. W. Kolar, N. Wang, and C. Mathuna, "Modeling and pareto optimization of microfabricated inductors for power supply on chip," *IEEE Transactions on Power Electronics*, vol. 28, no. 9, pp. 4422–4430, 2013.

[9] C. Feeney, N. Wang, S. C. O Mathuna, and M. Duffy, "A 20-MHz 1.8-W DC-DC converter with parallel microinductors and improved light-load efficiency," *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 771–779, 2015.

[10] J. Lopez Lopez, C. Fernández, P. Zumel, S. O. Driscoll, and C. O. Mathuna, "Integrated inductor optimization for Power Supply on Chip," in *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, pp. 1–6, IEEE, 2018.

[11] T. M. Andersen, C. M. Zingerli, F. Krismer, J. W. Kolar, and C. O'Mathuna, "Inductor optimization procedure for power supply in package and power supply on chip," *IEEE Energy Conversion Congress and Exposition: Energy Conversion Innovation for a Clean Energy Future, ECCE 2011, Proceedings*, pp. 1320–1327, 2011.

[12] J. A. Ferreira, "Improved Analytical Modeling of Conductive Losses in Magnetic Components," *IEEE Transactions on Power Electronics*, vol. 9, no. 1, pp. 127–131, 1994.

[13] F. W. Grover, *Inductance calculations: working formulas and tables*. Courier Corporation, 2004.

[14] P. R. Morrow, C. M. Park, H. W. Koertzen, and J. T. DiBene, "Design and fabrication of on-chip coupled inductors integrated with magnetic material for voltage regulators," *IEEE Transactions on Magnetics*, vol. 47, no. 6 PART 2, pp. 1678–1686, 2011.

[15] D. V. Harburg, X. Yu, F. Herrault, C. G. Levey, M. G. Allen, and C. R. Sullivan, "Micro-fabricated thin-film inductors for on-chip power conversion," *Proc. IEEE Conf. Integrated Power Electron. Sys.*, vol. 8, pp. 1–6, 2012.

[16] N. Wang, T. O'Donnell, and C. O'Mathuna, "An improved calculation of copper losses in integrated power inductors on silicon," *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 3641–3647, 2013.

[17] P. A. Bezerra, F. Krismer, T. M. Andersen, J. W. Kolar, A. Sridhar, T. Brunschwiler, T. Toifl, M. Jatlaoui, F. Voiron, Z. Pavlovic, N. Wang, N. Cordero, C. Rabot, and C. O'Mathuna, "Modeling and multi-objective optimization of 2.5D inductor-based Fully Integrated Voltage Regulators for microprocessor applications," *2015 IEEE 13th Brazilian Power Electronics Conference and 1st Southern Power Electronics Conference, COBEP/SPEC 2016*, 2015.

[18] A. Kriga, D. Allassem, M. Soultan, J. P. Chatelon, A. Siblini, B. Allard, and J. J. Rousseau, "Frequency characterization of thin soft magnetic material layers used in spiral inductors," *Journal of Magnetism and Magnetic Materials*, vol. 324, no. 14, pp. 2227–2232, 2012.

[19] N. Wang, J. Hannon, R. Foley, K. McCarthy, T. O'Donnell, K. Rodgers, F. Waldron, and C. Ó Mathúna, "Integrated magnetics on silicon for power supply in package (PSiP) and power supply on chip (PwrSoC)," *Electronic System-Integration Technology Conference (ESTC)*, 2010.

[20] C. Mathúna, S. Kulkarni, Z. Pavlovic, D. Casey, J. Rohan, A. M. Kelleher, G. Maxwell, J. O'Brien, and P. McCloskey, "Power inside - Applications and technologies for integrated power in microelectronics," *Technical Digest - International Electron Devices Meeting, IEDM*, pp. 3.3.1–3.3.4, 2018.

[21] C. Fernandez, Z. Pavlovic, S. Kulkarni, P. McCloskey, and C. O'Mathuna, "Novel high-frequency electrical characterization technique for magnetic passive devices," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 2, pp. 621–628, 2018.

[22] M. Mu, Q. Li, D. J. Gilham, F. C. Lee, and K. D. Ngo, "New core loss measurement method for high-frequency magnetic materials," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4374–4381, 2014.

[23] J. Mühlethaler, *Modeling and multi-objective optimization of inductive power components*. PhD thesis, ETH Zürich, 2012.