physica status solidi a
www.pss-a.com

Fabrication of Single-Crystalline InSb-on-Insulator by Rapid Melt Growth

Heera Menon, Nicholas Paul Morgan, Crispin Hetherington, Robin Athle, Matthew Steer, Iain Thayne, Anna Fontcuberta i Morral, and Mattias Borg*

InSb has the smallest bandgap and highest electron mobility among III-V semiconductors and is widely used for photodetectors and high-frequency electronic applications. Integration of InSb directly on Si would drastically reduce the fabrication cost and enable new applications, however, it is very challenging due to its 19% lattice mismatch with Si. Herein, the integration of single-crystalline InSb microstructures on insulator-covered Si through rapid melt growth (RMG) is reported and specifically provides details on the fabrication process. The importance of achieving high-quality conformal capping layers at low thermal budget to contain the InSb melt is assessed when the sample is annealed. The importance of ensuring a pristine Si seed area to achieve single-crystalline InSb is illustrated and demonstrated here for the first time.

1. Introduction

InSb is an attractive material for applications such as high-frequency electronic circuits,[1] Si photonic integrated circuits,[2] and quantum computing.[3] The key features that distinguish InSb are a high electron mobility of up to 70 000 $cm^2 V^{-1} s^{-1}$, a narrow bandgap of 0.17 eV, a large g factor and strong spin–orbit coupling.[4] To make InSb a viable material for large-scale application, it should be integrated with mainstream Si electronics. For instance, for the InSb midwavelength infrared photodetector application, monolithic integration[6] of InSb on Si would achieve high density integration with the read-out integrated circuit in Si complementary metal oxide semiconductor (CMOS) with higher pixel count for a reduced unit price compared with conventional flip-chip bonding.[5] In addition, InSb high-speed electronic devices integrated on Si would be compatible with the large-scale manufacturing of RF/CMOS foundries. However, the monolithic integration of InSb on Si is strenuous due to the 19% lattice mismatch and the difference in crystallographic symmetry between Si and InSb.

A considerable amount of literature has been published on[6] techniques for integration of compound semiconductors on Si. Among them, direct epitaxial growth with buffer layers,[7] aspect ratio trapping (ART),[8] nanowire epitaxy, and template-assisted epitaxial growth (TASE)[9] are a few techniques that enable the integration of III-V semiconductors on Si. The techniques of ART and TASE are of particular interest in this regard, as they are complementary-metal-oxide-semiconductor (CMOS) compatible processes that achieve high-quality crystals. However, one major challenge of these techniques is that the size of III-V integrated structures is limited in the lateral dimensions; for ART, growth is confined along a linear trench, and with TASE, the lateral size of the template is restricted by diffusive precursor transport to the growth interface.[10]

In recent years, a novel technique to fabricate Ge-on-insulator on Si has been developed, known as rapid melt growth (RMG).[11] High-quality III-V-on-insulator on Si has also been realized.[12–15] RMG enables the growth of III-V semiconductor structures of several hundreds of micrometers in the lateral dimension, and thus allows for large area integrated III-V devices[16–18] to be realized.

Recently, we demonstrated integration of polycrystalline InSb-on-insulator on Si using RMG with grain size exceeding 1 μm and an average electron mobility of 3100 $cm^2 V^{-1} s^{-1}$.[19] Here, we provide new insights into the fabrication process steps

H. Menon, R. Athle, M. Borg
Electrical and Information Technology
Lund University
Lund 221 00, Sweden
E-mail: heera.menon@eit.lth.se

H. Menon, C. Hetherington, R. Athle, M. Borg
NanoLund
Lund University
Lund 221 00, Sweden

N. P. Morgan, A. Fontcuberta i Morral
Laboratory of Semiconductor Materials
Ecole Polytechnique Federale de Lausanne
Lausanne 1015, Switzerland

C. Hetherington
Centre for Analysis and Synthesis and NanoLund
Department of Chemistry
Lund University
Lund SE 221 00, Sweden

M. Steer, I. Thayne
School of Engineering
University of Glasgow
Glasgow, Scotland G12 8QQ, UK

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/pssa.202100467.

DOI: 10.1002/pssa.202100467

necessary to achieve single-crystalline InSb-on-insulator with well-defined shapes by RMG. Specifically, we evaluate the properties of the capping layer that encapsulates the InSb structure during the melting and recrystallization phase, while demonstrating single-crystalline InSb microstructures exceeding 5 μm in lateral size made possible by controlling the interface between the Si seed area and InSb.

2. Experimental Section

The fabrication steps of the process are shown in **Figure 1**a. The first step is to deposit 40 nm of Si_3N_4 onto a Si (100) 3 in. wafer using inductively coupled plasma chemical vapor deposition (ICPCVD) at 250 °C using SiH_4 and N_2 precursors. A 50 μm long and 70 nm wide opening in the Si_3N_4 layer is then patterned using electron beam lithography (EBL) and Si_3N_4 dry etch using CHF_3 and N_2 chemistry (15:85 sccm at 10 mTorr) in an ICP-reactive ion etcher (RIE). Following this step, a partial V-groove was formed in the Si seed area using TMAH (25%) etch at 60 °C. The formation of a V-groove was also used as a verification, by inspection in scanning electron microscopy (SEM), that the opening in the Si_3N_4 was indeed complete. Once the V-groove was formed, a conformal layer of near amorphous InSb is deposited. This deposition was done using low-temperature molecular beam epitaxy (MBE), with a substrate temperature of ≈240 °C as measured by IR thermal camera, an indium beam equivalent pressure (BEP) of 1.75×10^{-7} Torr and an Sb BEP of 3.5×10^{-7} Torr. InSb layers of both 30 and 120 nm thickness have been attempted in this study. The InSb structure with thickness of 30 nm has an average roughness of 1.86 nm, whereas the structures with thickness of 120 nm have an average roughness of 3 nm. The 120 nm-thick InSb films had visible In droplets on the surface which contribute additional roughness in some regions of the InSb. These droplets can be avoided by controlling the stoichiometry of In and Sb in the MBE process.

InSb is very sensitive to the standard hydroxide-based chemicals used as resist remover and buffered oxide etch (BOE), and thus needs to be protected during processing. Therefore, after InSb film deposition, 3 nm of Al_2O_3 was deposited using atomic layer deposition (ALD) at 250 °C to protect the InSb from the subsequent processing steps. For our experiments, InSb structures of width varying from 200 to 1000 nm were then defined in negative AR-N 7520.17 resist by EBL. The resist patterns were developed using a diluted MF319 (4:1) and InSb structures etched out using $CH_4/H_2/Ar$ chemistry in ICP-RIE with RF power of 150 W and ICP of 600 W at 110 °C. Following the dry etch, the resist was removed using acetone in an ultrasonic bath for 10 min and isopropanol rinse for 1 min. The samples were then treated with oxygen plasma in a Tepla Microwave Plasma system for 30 min at 800 W to ensure no organic residues remain on the surface. This step is essential, as any organic residues would be trapped underneath the subsequent capping layers and, upon annealing, could lead to voids or even rupture of the capping layer. During the oxygen plasma treatment, the protective Al_2O_3 film prevents the InSb layer from being severely oxidized. SEM inspection after this step is used to verify that the InSb structures are thoroughly cleaned.

Following this, the Al_2O_3 protective layer was partly etched in BOE to remove overhanging Al_2O_3 on the edges of the InSb structures, resulting from lateral InSb etching in the preceding steps (Figure 1b). The BOE etch is timed to etch away about half of the 3 nm Al_2O_3 layer, thus completely removing any overhanging Al_2O_3 (which is etched from both sides) while not exposing the top InSb surface to the BOE. If left in place, the overhangs would lead to void formation if the capping layer deposition is not sufficiently conformal.

The InSb structures were then capped by a thick dielectric layer consisting of either SiO_2, Si_3N_4, or a stack of Al_2O_3 and Si_3N_4. Al_2O_3 was deposited by ALD, while SiO_2 and Si_3N_4 were deposited using ICPCVD at 200 °C. To melt and recrystallize the InSb, flash lamp annealing (FLA) with a duration of 1.5 ms and energy of 19.5 J cm^{-2} was used. The peak temperature was varied by altering the chamber temperature prior to the flash and controlled via a calibrated finite element simulation model.[19] Once annealed, the Si_3N_4 capping layer was removed by dry etch using SF_6 and O_2 chemistry in reactive ion etcher (RIE). A SiO_2 capping layer was removed by BOE. The InSb structures were then characterized by SEM and electron backscatter diffraction (EBSD).

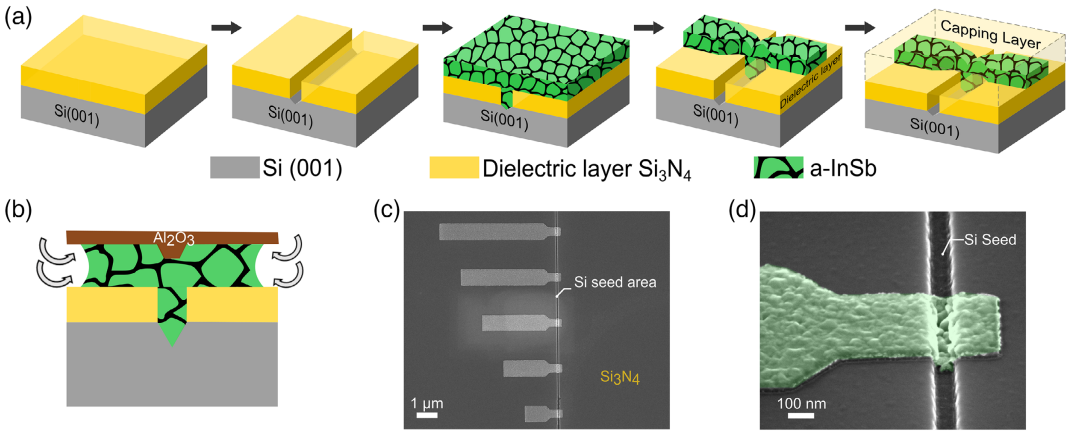

Figure 1. a) Schematic illustrating the sample fabrication process. b) 2D schematic showing the protective Al_2O_3 layer on top of InSb layer and Al_2O_3 overhang that could be produced due to any lateral etch. c) SEM image of sample with InSb structures of varying length before annealing. The opening to the Si substrate is also shown. The Si seed area is located at the interface between the InSb and this opening. d) Fifty two degrees tilted close-up SEM image of InSb structure before annealing.

To inspect the sample using transmission electron microscope (TEM), lamellae of the InSb were prepared by means of focused ion beam (FIB) milling. InSb is a very soft material and is easily damaged by the FIB process. Therefore, 20 nm of Au was evaporated on to the sample prior to the FIB process. This was followed by Pt deposition using electron beam and ion beam to fully protect the sample surface from the damages induced by the ion beam. Finally, the lamella was cut and extracted using a standard in situ lift-out process. Even with this careful process we still observe some signs of ion beam damage in our InSb lamellas.

3. Results and Discussion

To maintain the designed structure and material stochiometry, it is key to contain the III-V melt throughout the RMG annealing process. For this purpose, we use the underlying Si_3N_4 layer and a capping layer to hold the liquid, together these are denoted the crucible. Commonly used capping layer materials for Ge RMG are SiO_2 and Si_3N_4, high-quality films of which are deposited by low-pressure CVD at >650 °C.[20–22] Although these films are well-suited as crucible materials, the deposition temperature, which is higher than the InSb melting temperature (527 °C),

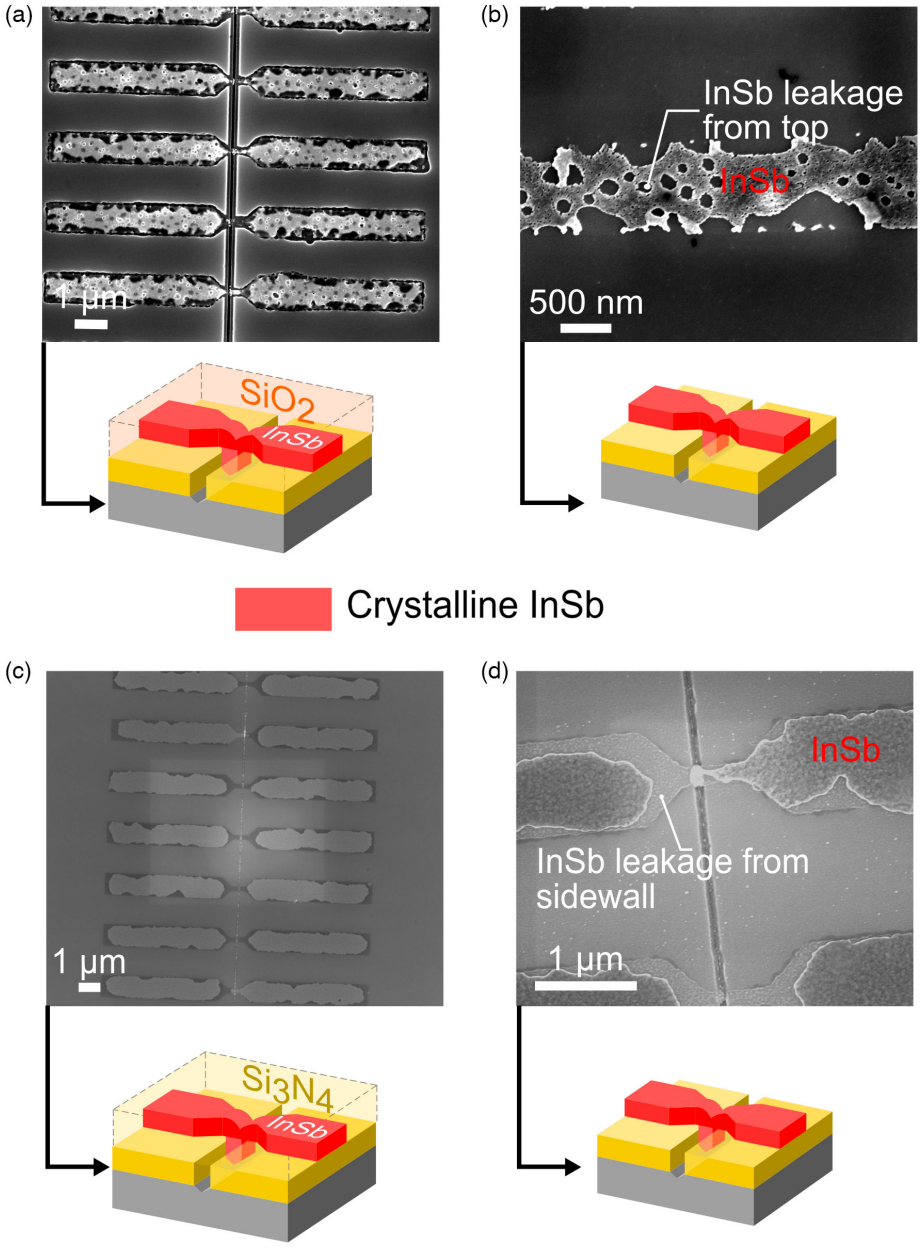

Figure 2. SEM images of InSb structures after annealing with a,b) SiO_2 or c,d) Si_3N_4 as the capping layer. a) SEM image with thinned down SiO_2 capping layer so that the underlying shape of the InSb is visible. b) Close-up SEM image of a InSb structure when the SiO_2 capping layer is completely removed, indicating voids in the InSb. c) SEM image of InSb structures with thinned down Si_3N_4 capping layer. d) Close-up SEM image with Si_3N_4 completely removed indicating loss of InSb material from the sidewalls.

precludes their use for InSb RMG. In this work, we instead used ICPCVD SiO_2 and Si_3N_4, which can be deposited at <300 °C. The most striking difference between samples annealed with SiO_2 and Si_3N_4 as the capping layer is shown in **Figure 2**. For the samples capped with 260 nm SiO_2, the InSb structures have strongly deteriorated, with the appearance of holes in the top surface and severe loss of material on the edges as well (Figure 2a,b). As this only happens for samples exposed to temperatures above the InSb melting temperature it seems clear that In and Sb has leaked out of the crucible during the period in the liquid phase.

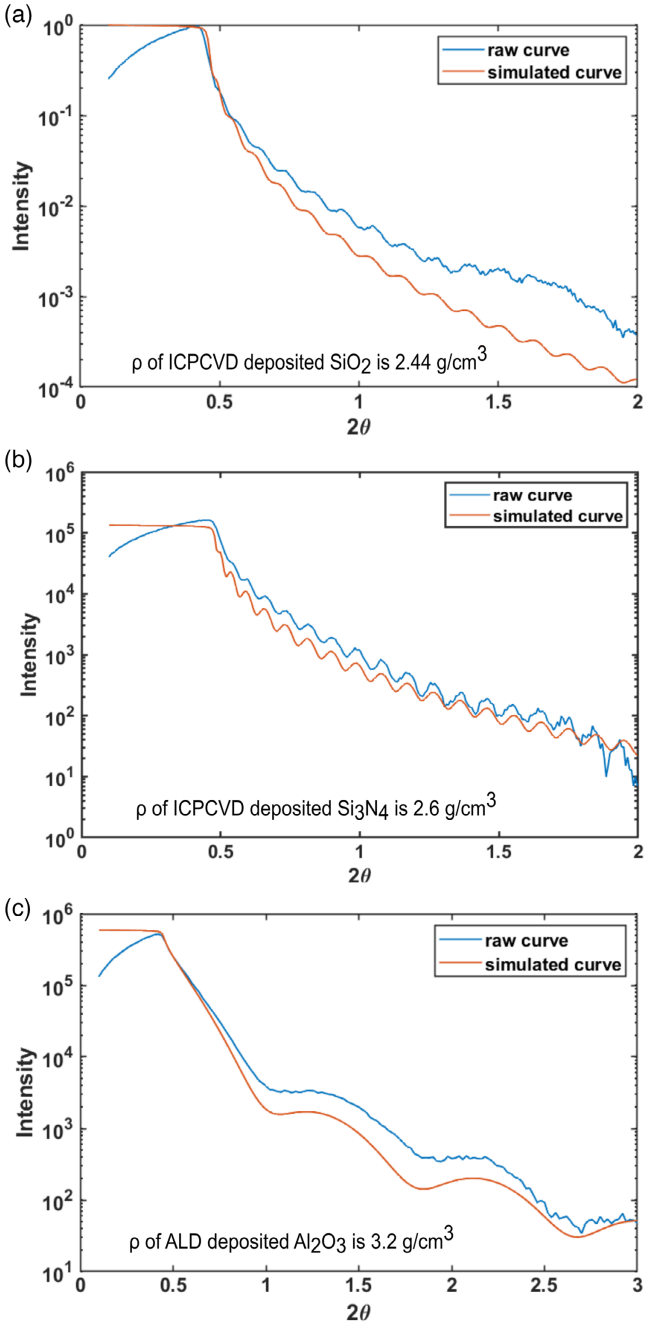

Figure 3. XRR measurement illustrating the raw and simulated data for a) ICPCVD deposited SiO_2 b) ICPCVD deposited Si_3N_4 c) ALD deposited Al_2O_3.

This is an indication that the SiO_2 film may not be sufficiently dense to prevent out-diffusion of In and Sb from the melt. Interestingly, the sample with a 580 nm Si_3N_4 capping layer had a much reduced prevalence of holes in the top surface but still considerable deterioration of the structure on the side-edges (Figure 2c,d). To investigate further, the material quality of SiO_2 and Si_3N_4 was studied using X-ray reflectometry (XRR) measurements and BOE etch.

XRR is a precise technique to analyze material properties such as thickness, density, or interface roughness of thin films without being sensitive to crystal structure.[23] The measured XRR data (blue) for the SiO_2 and Si_3N_4 films are shown in **Figure 3**a,b. A simulated XRR curve (red) is fitted to the measured data to obtain the density of the films. A notable difference between the density of inhouse deposited SiO_2 (2.44 g cm^{-3}) and the table value density (2.65 g cm^{-3}) was observed. This difference is also reflected in the measured BOE 1:10 etch rate of

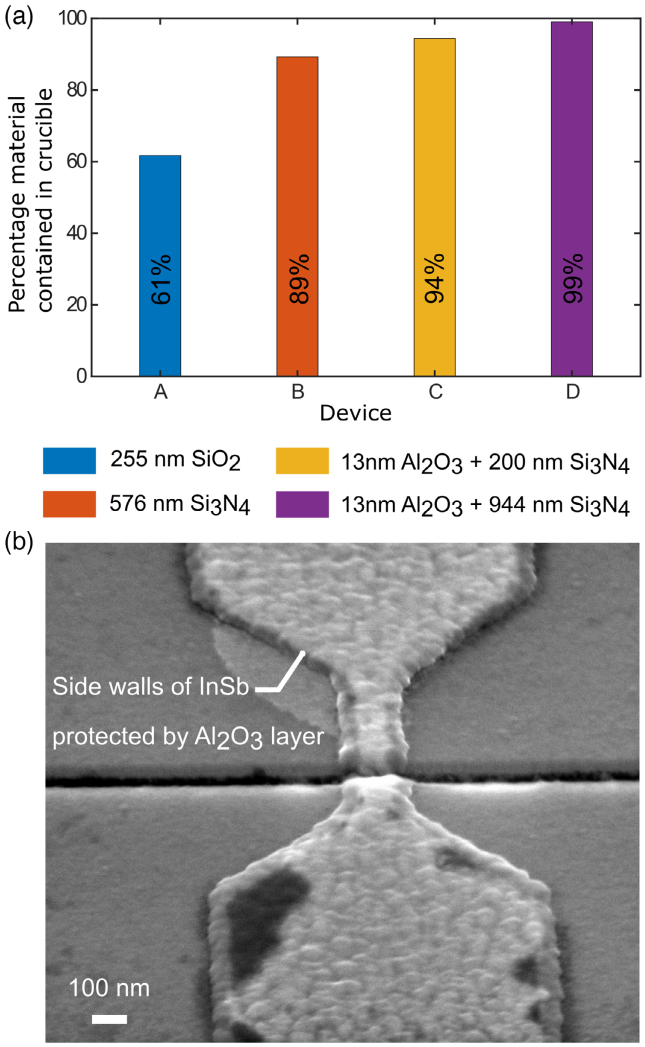

Figure 4. a) Bar plot representing the percentage of material contained in the InSb structure for different capping layer samples. b) Fifty two degree tilted SEM image indicating the sidewalls of InSb structure protected by Al_2O_3 when annealed.

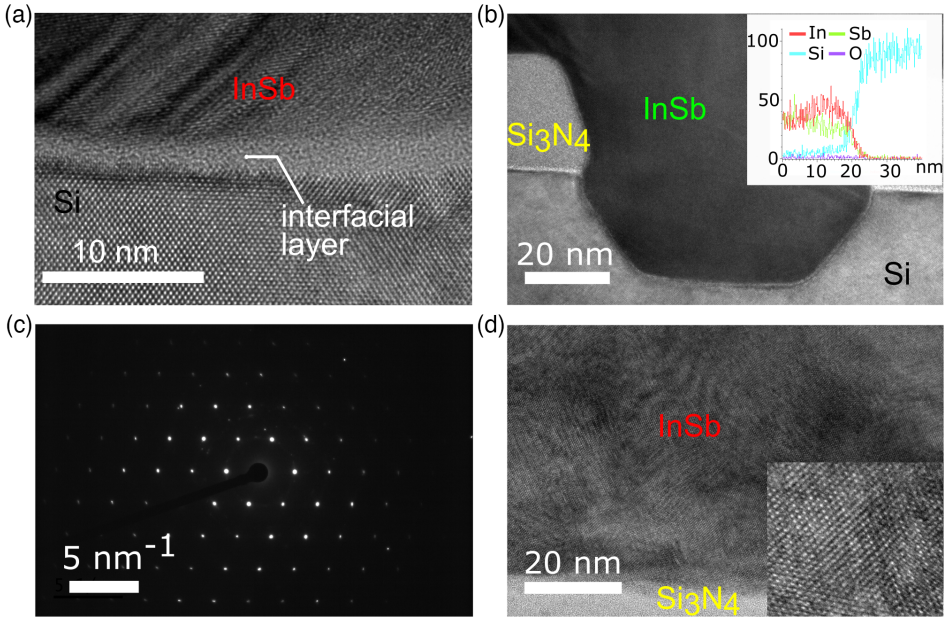

Figure 5. a) TEM image revealing the interfacial layer between Si and InSb when no HF dip is performed before MBE growth b) TEM image of the sample (before annealing) with HF dip performed before MBE growth. The inset shows the EDX line scan across the interface of InSb and Si indicating absence of oxygen at the interface. c) SAED pattern of annealed InSb d) HRTEM of the annealed InSb with the inset showing the lattice spacing.

2.7 nm s^{-1} compared with a typical value of 1.3–1.6 nm s^{-1} for thermal oxide.[24] Previous research[25] have concluded that the inclusion of OH groups during plasma-enhanced CVD lead to low density of SiO_2, which is particularly severe at low deposition temperatures as we use here. Another study reported the protection of III-V nanowires by PECVD-deposited SiO_2. However these nanowire structures were implanted and thus may have hardened the oxide layer preventing any leakage of material.[26] In thermal SiO_2, diffusion of both In and Sb is negligible below 700 °C,[27,28] it is thus likely that the higher porosity in the ICPCVD SiO_2 makes it susceptible to In and Sb leakage during the annealing process. Si_3N_4 has a greater degree of covalent bonds than SiO_2 and is thus generally a much better diffusion barrier than SiO_2. However,[29] finds that Si_3N_4 is an excellent H diffusion barrier only if its density is higher than 2.5 g cm^{-3}, especially for N-rich films. In our case, we find that the Si_3N_4 film has a density of 2.6 g cm^{-3} which should be sufficient for it to be an efficient diffusion barrier. This explains why the Si_3N_4 capping layer resulted in less material leakage from the crucible, at least on the top surface. The reasonably low BOE etch rate of 6 nm min^{-1} is still much higher than for LPCVD-grown stochiometric Si_3N_4, which could be explained by a significant H-content which can lead to a reduction of its barrier properties.[30] The high-density anisotropic plasma in ICPCVD is designed to give dense film deposition on planar surfaces, but the quality is not guaranteed on steps and vertical surfaces.[31] Indeed we find a much higher Si_3N_4 BOE etch rate close to any sample topography, which implies that the Si_3N_4 quality is lower here. Thus it can be expected that there would be increased out-diffusion on the side-edges of the InSb structures, as we also observe.

To mitigate the issue of material leakage from the sidewalls of the InSb structure, deposition of a conformal layer of Al_2O_3 was introduced after the dry etching of the InSb. This layer of Al_2O_3 acts as an intermediate capping layer, with high density of 3.2 g cm^{-3} as measured by XRR (Figure 3c), giving a uniform diffusion barrier around both the side and top surfaces of the structures. The thickness of the Al_2O_3 layer cannot be too thick or it will crystallize upon annealing and be very difficult to remove without damaging the InSb beneath. We find that a 10 nm thick layer provides a good compromise. A quantitative evaluation of the fidelity of the InSb structures after annealing is shown in **Figure 4**a. It can be observed that when a conformal Al_2O_3 layer is used together with 200 nm Si_3N_4, 94% of the material is contained during the annealing process (Figure 4b). The amount of contained material decreases to 89% for Si_3N_4 only, and down to 61% for SiO_2. Moreover, using a 944 nm Si_3N_4 layer together with Al_2O_3 provides a 99% containment suggesting that the combination of Al_2O_3 and Si_3N_4 is crucial for our InSb structures to survive the RMG process.

In the following, the crystallinity of the annealed InSb structures is discussed. When the InSb is briefly annealed above its melting point using flash annealing, the InSb is melted and resolidified. We expect solidification to originate at the point with the highest nucleation probability and if nucleation probability is low enough lead to an expansion of the crystallite throughout the full crucible. The interface between the crystalline Si and InSb should provide a preferential nucleation point allowing for single-crystalline epitaxial InSb to form. A thermodynamics-based growth model first introduced by Liu et al.[32] indicates that there exists a process window where epitaxial growth dominates over homogeneous and heterogeneous nucleation for InSb.[19] However, in our previous work,[19] single-crystalline InSb was not observed. Instead, there was a transition from amorphous to a polycrystalline structure with an average grain size of

1 μm after the annealing process. To understand the reason for the polycrystalline growth, the interface between InSb and Si was inspected using TEM. This inspection revealed the presence of an interfacial layer which hindered the nucleation of InSb on Si (**Figure 5**), essentially preventing the Si/InSb interface from providing a preferential nucleation site.

To obtain single-crystalline InSb, it is critical to have a pristine Si/InSb interface, to facilitate the preferential nucleation at the seed area. In the original work, we conducted a 1 h anneal at 850 °C in the MBE chamber prior to InSb film deposition, with the aim of removing the native SiO_2 on the Si surface. It thus was not clear whether the interfacial layer was due to a failure to remove the native oxide or whether it had appeared due to interfacial reactions at a later stage. Here, we introduce a 10 s etch in 1% HF right before transferring the sample into the MBE chamber. This etch should remove the native oxide and passivate the Si surface during transfer to the MBE chamber, allowing us to evaluate the origin of the interfacial layer by evaluating the crystallinity of the InSb using EBSD. After MBE growth, we confirm the absence of an interfacial layer by high-resolution transmission electron microscope (HRTEM) (Figure 5b), where we observe an abrupt contrast observed between the Si substrate and InSb film. An energy-dispersive X-ray spectroscopy (EDX) line scan across the Si/InSb interface (inset in Figure 5b) highlights the absence of oxygen at the interface or in its vicinity.

We find that introduction of the HF dip prior to MBE results in better InSb crystal quality after the RMG process. **Figure 6**a,b shows the EBSD *Z*-orientation inverse pole figure (IPF) map and SEM image of a sample processed after the introduction of the HF etch and Figure 6c,d shows the EBSD Z-orientation IPF map of sample without HF etch. The red area on the left hand side is the Si seed area which has (001) orientation. We observe a large single InSb crystal (Figure 6a), which extends from the seed area toward the end of the crucible more than 5 μm away. The InSb crystal was also investigated by HRTEM, shown in Figure 5d, which confirms the high crystal quality. Visible in the HRTEM image are also small moiré patterns in some areas. This is suspected to be due to surface damage caused by FIB milling of InSb which is well documented in literature.[33,34] Selected area electron diffraction (SAED) along the 110 zone axis in Figure 5c allows for extraction of the InSb lattice parameter from the 111 diffraction spot spacing. By calibration to the Si substrate, we obtain $d_{111} = 3.67$ Å, resulting in an InSb lattice parameter of 6.36 ± 0.13 Å, which coincides with the table value for InSb. Furthermore, the InSb chemical composition was investigated using EDX. The composition of the polycrystalline InSb film deposited by MBE was 51.5 at% In and 48.5 at% Sb, i.e., slightly In rich and also had In droplets on the surface. After annealing, the composition of the InSb crystals was obtained to be 50.34 at% In and 49.66% Sb. (The EDX spectrum of the annealed structure is provided in the Supporting Information.) This is considered stoichiometric within the estimated error of the quantification (±0.78%).[35]

Even though not all structures on the sample have InSb crystallites extending throughout the whole crucible (Figure 6e), they clearly in most cases originate from the Si seed. It is thus evident that the BOE dip has led to a preferential nucleation at the Si seed, possibly by removing the interfacial layer, and we can conclude that the interfacial layer does not arise later in the process. Here, we can also see occasional gaps in the InSb structures, which we believe are caused by the In droplet defects on top of the as-deposited InSb film. Upon annealing, pure In becomes liquid already (at 157 °C) in the preheating phase before the flash, and thus can locally decompose the InSb, leading to the observed

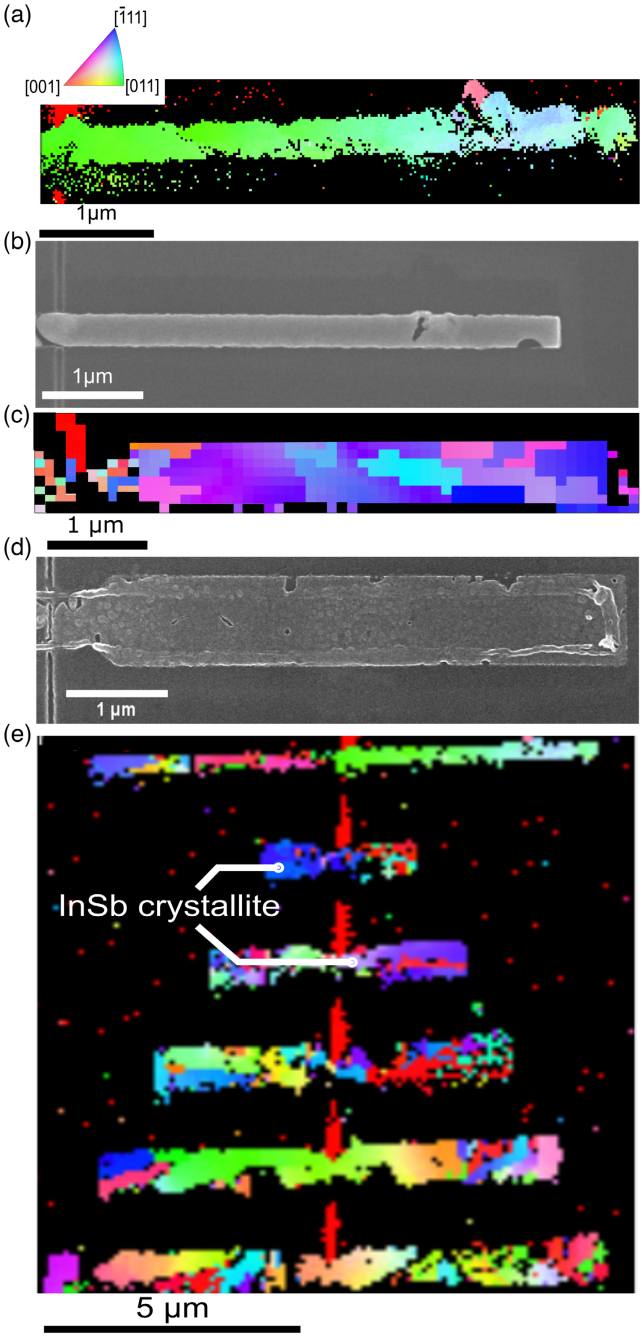

Figure 6. a) EBSD *Z*-orientation IPF map indicating the single-crystalline InSb. The inset provides the color code representation of orientation of crystal in EBSD map b) SEM image of EBSD scanned InSb structure c) EBSD *Z* orientation IPF map of InSb grown on sample which did not have an HF step introduced before MBE deposition. d) SEM image of EBSD scanned InSb structure grown without HF etch. e) EBSD *Z*-orientation map of an array of InSb structures on top of a vertically oriented Si seed line, indicating largest InSb crystallites when originating from the seed area.

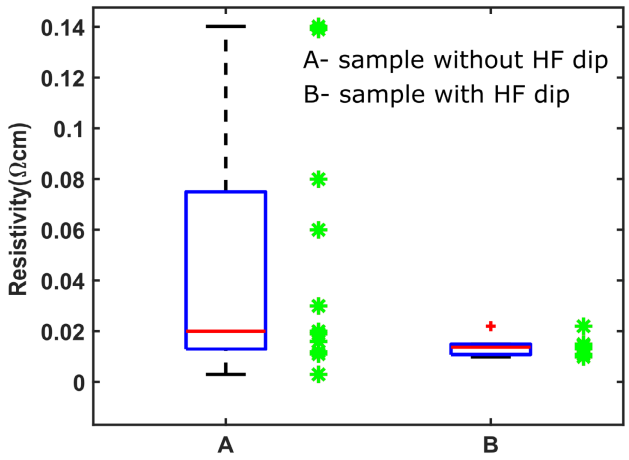

Figure 7. Box plot showing the resistivity of InSb devices from a sample in which HF was not used A) and was used B) prior to MBE growth The distance between top and bottom of the blue box represents the interquartile range of the sample, the red line represents the median of each dataset, and the red cross mark represents outliers in these datasets. The green * markers represent the resistivity data points measured for each sample.

gaps in the structure. A firm control of the InSb stoichiometry should avoid this issue, and lead to higher yield of single-crystalline InSb. The orientation of the InSb crystal in Figure 6a,b is not the same as the Si substrate, and we do not claim epitaxy at this point, but the complex crystallographic relationship between the InSb-on-insulator structures and the Si substrate is the topic of further study, in addition to detailed materials characterization.

Finally, the resistivity of the RMG InSb obtained with and without the HF dip before MBE growth are compared using TLM measurement (**Figure 7**). For electrical measurement, the Si_3N_4 capping layer was dry etched and Ni/Au leads contacts were patterned using electron-beam exposed PMMA, metal evaporation and lift off. Prior to metal evaporation, the Al_2O_3 capping layer and the native oxide on the InSb surface was removed using BOE (30:1) etch and the InSb contact area was passivated using an ammonium sulfide solution for 90 min. The sample which did not have an HF dip before the MBE step had an average resistivity of 40 mΩcm and a large resistivity spread between devices. Contrary, the average resistivity of the InSb for which a HF dip was made was 10 mΩcm, a reduction in resistivity by a factor of 4. In addition, the spread in resistivity between devices was much improved. These results directly reflect the improvement in crystal structure obtained from introducing the HF dip prior to MBE growth.

4. Conclusion

In conclusion, we have detailed the fabrication process considerations necessary for RMG of single-crystalline InSb on Si. Our work specifically focuses on the design of a low-temperature deposited capping layer and the necessary protection of the InSb throughout the process. The importance of a conformal capping layer that provides an efficient diffusion barrier for the InSb melt is highlighted and a solution to use a combined Al_2O_3/Si_3N_4 capping layer is demonstrated. The paper demonstrates the first realization of single-crystalline InSb-on-insulator structures by introduction of an HF etch prior to MBE. The insights gained from this study provide a first important step toward the realization of high-quality InSb-on-insulator devices on Si for optoelectronics and quantum applications.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was supported by Swedish Foundation for Strategic Research, Crafoord Foundation and Royal Physiographic Society of Lund, and NanoLund. A.F.M. and N.M. thank funding from SNSF though the NCCR QSIT and project nr CRSK-2_190289.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

Research data are not shared.

Keywords

electron backscatter diffraction (EBSD), InSb, rapid melt growth (RMG), single crystal, Si, TEM, XRR

Received: July 16, 2021
Revised: September 17, 2021
Published online: November 5, 2021

[1] K. Isono, D. Tsuji, T. Taketsuru, S. Fujikawa, I. Watanabe, Y. Yamashita, A. Endoh, S. Hara, A. Kasamatsu, H. I. Fujishiro, in *2016 Compound Semiconductor Week (CSW) [Includes 28th Int. Conf. on Indium Phosphide & Related Materials (IPRM) & 43rd Int. Symp. on Compound Semiconductors (ISCS)*, IEEE, Piscataway, NJ **2016**, p. 5090.
[2] B. W. Jia, K. H. Tan, W. K. Loke, S. Wicaksono, K. H. Lee, S. F. Yoon, *ACS Photonics* **2018**, *5*, 1512.
[3] J. W. G. Van Den Berg, S. Nadj-Perge, V. S. Pribiag, S. R. Plissard, E. P. A. M. Bakkers, S. M. Frolov, L. P. Kouwenhoven, *Phys. Rev. Lett.* **2013**, *110*, 066806.
[4] Y. Chen, S. Huang, D. Pan, J. Xue, L. Zhang, J. Zhao, H. Q. Xu, *npj 2D Mater Appl.* **2021**, *5*.
[5] G. Gershon, A. Albo, M. Eylon, O. Cohen, Z. Calahorra, M. Brumer, M. Nitzani, E. Avnon, Y. Aghion, I. Kogan, E. Ilan, L. Shkedy, *Infrared Technol. Appl. XXXIX* **2013**, *8704*, 870438.
[6] T. T. Wu, C. H. Shen, J. M. Shieh, W. H. Huang, H. H. Wang, F. K. Hsueh, H.-C. Chen, C.-C. Yang, T.-Y. Hsieh, B.-Y. Chen, Y.-S. Shiao, C.-S. Yang, G.-W. Huang, K.-S. Li, T.-J. Hsueh, C.-F. Chen, W.-H. Chen, F.-L. Yang, M.-F. Chang, W.-K. Yeh, in *Tech Dig – Int. Electron Devices Meet IEDM*, IEEE, Piscataway, NJ **2015**; 2016-February, pp. 25.4.1–25.4.4.

[7] S. Chen, M. Tang, Q. Jiang, J. Wu, V. G. Dorogan, M. Benamara, Y. I. Mazur, G. J. Salamo, P. Smowton, A. Seeds, H. Liu, *ACS Photonics* **2014**, *1*, 638.
[8] N. Waldron, C. Merckling, L. Teugels, P. Ong, F. Sebaai, K. Barla, N. Collaert, V.-Y. A. Thean, *Solid-State Electron*, Elsevier Ltd, **2016**, *115*, 81.
[9] H. Schmid, M. Borg, K. Moselund, L. Gignac, C. M. Breslin, J. Bruley, D. Cutaia, H. Riel, *Appl. Phys. Lett.* **2015**, *106*, 233101.
[10] M. Borg, H. Schmid, K. E. Moselund, D. Cutaia, H. Riel, *J. Appl. Phys.* **2015**, *117*, 144303.
[11] Y. Liu, M. D. Deal, J. D. Plummer, *Appl. Phys. Lett.* **2004**, *84*, 2563.
[12] Shu-Lu Chen, Peter B. Griffin, James D. Plummer, *IEEE Electron Device Lett.* IEEE, **2010**, *31*, 597.
[13] Y.-H. Chen, J.-W. Jheng, P. Mishra, C.-Y. Lin, M.-C. M. Lee, *IEEE Photonics Technol. Lett.* **2018**, *30*, 1013.
[14] X. Bai, C. Y. Chen, N. Mukherjee, P. B. Griffin, J. D. Plummer, *Adv. Mater. Sci. Eng.* **2016**, *2016*, 5 https://doi.org/10.1155/2016/7139085.
[15] C. G. Littlejohns, M. Nedeljkovic, C. F. Mallinson, J. F. Watts, G. Z. Mashanovich, G. T. Reed, F. Y. Gardes, *Sci. Rep.* **2015**, *5*, 8288.
[16] I. Mizushima, K. Toko, Y. Ohta, T. Sakane, T. Sadoh, M. Miyao, *Appl. Phys. Lett.* **2011**, *98*, 182107.
[17] R. L. M. Op het Veld, D. Xu, V. Schaller, M. A. Verheijen, S. M. E. Peters, J. Jung, C. Tong, Q. Wang, M. W. A. de Moor, B. Hesselmann, K. Vermeulen, J. D. S. Bommer, J. S. Lee, A. Sarikov, M. Pendharkar, A. Marzegalli, S. Koelling, L. P. Kouwenhoven, L. Miglio, C. J. Palmstrøm, H. Zhang, E. P. A. M. Bakkers, *Commun. Phys.* **2020**, *3*, 1.
[18] S. R. Plissard, I. Van Weperen, D. Car, M. A. Verheijen, G. W. G. Immink, J. Kammhuber, L. J. Cornelissen, D. B. Szombati, A. Geresdi, S. M. Frolov, L. P. Kouwenhoven, E. P. A. M. Bakkers, *Nat. Nanotechnol.* **2013**, *8*, 859.
[19] H. Menon, L. Södergren, R. Athle, J. Johansson, M. Steer, I. Thayne, M. Borg, *Nanotechnology*, IOP Publishing, **2021**, *32*, 165602.
[20] F. S. Becker, *J. Vac. Sci. Technol., B* **1987**, *5*, 1555.
[21] N. Sharma, M. Hooda, S. K. Sharma, *J. Mater.* **2014**, *2014*, 1.
[22] C. Yang, J. Pham, *Silicon,* **2018**, *10*, 2561.
[23] T. Tao, in *An Epsil Room, II.*, The Rigaku Journal, Summer, **2010**, Vol. *26*, p. 141–239.
[24] K. R. Williams, K. Gupta, M. Wasilik, *J. Microelectromech. Syst.* **2003**, *12*, 761.
[25] M. F. Ceiler, P. A. Kohl, S. A. Bidstrup, *J. Electrochem. Soc.* **1995**, *142*, 2067.
[26] M. Glaser, A. Kitzler, A. Johannes, S. Prucnal, H. Potts, S. Conesa-Boj, L. Filipovic, H. Kosina, W. Skorupa, E. Bertagnolli, C. Ronning, A. Fontcuberta I Morral, A. Lugstein, *Nano Lett.* **2016**, *16*, 3507.
[27] A.H. Van Ommen, *Appl. Surf. Sci.* **1987**, *30*, 244.
[28] H. G. Francois-Saint-Cyr, F. A. Stevie, J. M. Mckinley, K. Elshot, L. Chow, K. A. Richardson, *J. Appl. Phys.* **2003**, *94*, 7433.
[29] D. Benoit, J. Regolini, P. Morin, *Microelectron. Eng.* **2007**, *84*, 2169.
[30] G. N. Parsons, J. H. Souk, J. Batey, *J. Appl. Phys.* **1991**, *70*, 1553.
[31] J. Yota, J. Hander, A. A. Saleh, *J. Vac. Sci. Technol., A.* **2000**, *18*, 372.
[32] Y. Liu, M. D. Deal, J. D. Plummer, *J. Electrochem. Soc.* **2005**, *152*, G688.
[33] S. Rubanov, P. R. Munroe, *Microsc Microanal.* **2005**;*11*:446.
[34] S. Rubanov, *The Study of the Focused Ion Beam Induced Damage in Semiconductor Materials*, The University of New South Wales Faculty of Science and technology School of Materials Science and Engineering, **2014**.
[35] M. Ek, B. M. Borg, A. W. Dey, B. Ganjipour, C. Thelander, L.-E. Wernersson, K. A. Dick, *Cryst. Growth Des.* **2011**, *11*, 4588.