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Analysis of Steady-State Characteristics for a Newly Designed High Voltage Gain Switched Inductor Z-Source Inverter

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Abstract: This paper aims to develop a new switched inductor assisted strong boost Z-source inverter (SL-SBZSI) topology with high voltage gain and analyze the steady-state characteristics of the proposed topology. In the proposed topology, two switched inductors are used within the series impedance structure of the Z-source inverter (ZSI) in order to achieve the high voltage gain. The steady-state characteristics of the proposed topology are analyzed to disseminate its several advantages as compared to traditional ZSIs. The key advantages include the higher boost factor with lower shoot-through duty ratio and lower voltage stresses on capacitors as well as on switches of the inverter bridge. Furthermore, the proposed topology has the soft-start ability which significantly reduces the inrush start-up current while comparing with the traditional ZSI. In the proposed topology, a common ground is shared between the output AC voltage and the input DC voltage source which categorizes this topology to the doubly grounded inverter. The characteristics of the proposed SL-SBZSI are analyzed by considering two operating condition where the simple boost pulse width modulation (PWM) scheme is used to extract the shoot-through pulses. The characteristics of the proposed topology are also compared with different existing topologies along with the conventional modified capacitor assisted Z-source inverter (MCA-ZSI), whose boost factor is much closer to the proposed topology. Rigorous mathematical analyses are presented to clearly demonstrate the benefits of the proposed topology while simulation studies are carried out to demonstrate its distinct features as compared to the existing topology. Finally, experimental studies are conducted to further validate the theoretical and simulation results.

Keywords: boost factor; impedance network; switched inductor; shoot-through; Z-source inverter

1. Introduction

Modern power networks are dominated by power electronic converters as these converters convert power from one to another, e.g., DC to AC or vice-versa. Since many renewable energy sources in modern power grids directly produce DC power, the voltage source inverter (VSI) is widely used to convert DC power to AC power. Typically, the operation of the VSI is restricted to the buck mode in many applications where the output AC peak voltage always lags behind the input DC voltage. Thus, a high AC peak voltage is generated by an interim DC–DC converter which increases the size and operational cost of the system.

Furthermore, the dual-stage conversion (one through DC–DC and other through DC–AC converters) increases the overall loss in the system. To overcome such problems in VSIs, an impedance network can be incorporated as presented in [1] and the VSI with such an impedance network is commonly known as the Z-source inverter (ZSI). The ZSI exhibits step-up and down of its output voltage through a unique shoot-through control and hence, converts the dual-stage power conversion problem into a single stage. Additionally, the shoot-through control scheme within the ZSI eliminates the dead time of the conventional VSI which reduces distortions in the output AC voltage [2]. These features of the ZSI allow it to apply for so many applications which include electric motor drives [3], photovoltaic power generation [4], fuel cell [5], electric vehicle [6], electrical vehicle to grid application [7], uninterruptable power supply [8], power line AC to AC voltage booster [9], grid-connected wind power generation [10], and hybrid PV-wind based microgrid system [11] etc. The major drawbacks of the ZSI so far presented in this paper are the limited boost factor and high voltage stresses on capacitors of its impedance network as well as on switches. High input inrush current is also a disadvantage of conventional ZSIs which may destroy the inverter circuitry [12]. The lower modulation index is considered as another limitation of the existing ZSI as this affects voltage gain and produces distorted output voltage waveforms [13]. These problems are avoided in several works of literature where new topologies such as an improved ZSI [12], embedded ZSI [14], qZSI [15], and series ZSI [16] are developed by introducing distinct impedance configurations. Most of these topologies are used to minimize the voltage stress on capacitors and switches along with the input inrush current reduction of the traditional ZSI. Though these topologies reduce the voltage stress, the boost factor remains similar to that traditional ZSI. The boost factor is considered as a crucial factor of ZSI and all factors associated with the steady-state characteristics need to be improved simultaneously. A number of new topologies are presented in [17–24], which improves the boost factor. However, the stress of passive components capacitor remain high and hence, these do not meet the criteria for simultaneously improving all performance-related factors. The impedance network of ZSI topologies in [25–30] uses a transformer to increase the voltage gain, and the proper operation of these topologies heavily relies on the perfect magnetic coupling, i.e., the design of the transformer. In these transformed-based topologies of ZSIs, the switching of currents during the transient events generally produce high voltage spikes due to improper couplings of magnetic components and the inverter circuitry will be damaged.

Recently, the high boost factor is achieved by composing additional capacitors, inductors, and diodes to the impedance network of ZSIs while using a low shoot-through duty ratio. This low shoot-through duty ratio increases the modulation index which improves the quality of output voltage waveforms. Hence, a new trend is drifting towards the low shoot-through duty ratio driven ZSI having additional passive components in its impedance network. An enhanced boost ZSI (EB-ZSI) is presented in [31], where the boost factor is stepped up by using two combined Z-impedance networks. However, this topology suffers from the high voltage stress across capacitors which is even severe than traditional ZSIs. An embedded switched-inductor qZSI (ESL-qZSI) is presented in [32] where two input DC sources are embedded in the quasi Z-impedance structure which significantly reduces the voltage stress across the capacitor as compared to EB-ZSI while maintaining the same boost factor. Though the performance of the ESL-qZSI is better than the EB-ZSI, it requires an additional DC source. The modified capacitor assisted ZSI (MCA-ZSI) as presented in [33] exhibits the strong boost factor which is even better than EB-ZSI and ESL-qZSI. However, the voltage stresses across capacitors are still higher and similar to that of a traditional ZSI while having more passive components, i.e., capacitors on its impedance network. Therefore, the simultaneous improvement of the boost factor and reduction in the voltage stresses are not solved yet.

In this paper, a new switched inductor assisted strong boost ZSI (SL-SBZSI) topology is proposed based on a series impedance structure. The boosting capability of the inverter strongly increases the voltage gain by maintaining lower voltage stress on the capacitor. The proposed SL-SBZSI generates a higher boost factor than all four topologies as mentioned above for the same shoot-through duty ratio. With the proposed SL-SBZSI, there are lower voltage stresses on semiconductor switches and higher voltage conversion ratio while using a similar modulation index to that of existing ZSIs. The proposed SL-SBZSI also couples the ground of both DC and AC side which can be used to eliminate the common-mode leakage current in renewable energy applications, e.g., photovoltaic power generation systems as there exist such currents which can be evidenced from [34]. Furthermore, the benefits of a doubly grounded feature in terms of minimizing the leakage is covered in [35] and this feature is utilized in [36] using the proposed SL-SBZSI. Though a similar structure is used in [36], it only analyzes the simple feature associated with power conversion for the solar photovoltaic system. Some important features such as the modeling of the inductor ripple current, capacitor voltage ripple, inverter switching device power (SDP) calculation and efficiency are not covered in [36].

This work has the following contributions as compared to existing literature so far discussed in this section:

1. The detailed analytical model has been developed along with the analysis of the ripples in the inductor currents and capacitor voltages.
2. This work includes more analyses associated with the switching device power and efficiency calculation.
3. The analytical models reveal several advanced features of the proposed topologies such as the reduced capacitor voltage stress for the same boost factor; improved boosting capability for the same input voltage and shoot-through duty ratio, improved efficiency, reduced inrush current, and significantly improved dynamic voltage compensation capability as compared to all existing topologies.

The rest of the paper is organized as follows. The operating characteristic of the proposed topology is discussed in Section 2 and the detailed mathematical analysis associated with the proposed SL-SBZSI is presented in Section 3. The simple boost PWM scheme for the proposed topology is discussed in Section 4. The comparative results of the proposed scheme in comparison with different traditional topologies are provided in Section 5. The power loss calculation and efficiency analysis are demonstrated in Section 6. Simulation results with different case studies are presented in Section 7 by comprising with conventional MCA-ZSI. Finally, the experimental result is provided in Section 8 and the paper concluded in Section 9.

2. Operating Characteristics of the Proposed SL-SBZSI Topology

The circuit configuration of the proposed topology is shown in Figure 1. The impedance network of this topology is placed in series with the input DC-side and there is a common ground between this input and the output inverter. There are two switched inductor (SL) cells: one on the left and another right part of the impedance network which are used for improving the boost capability. The left cell includes inductors (L_1 and L_2) and diodes ($D_1, D_2,$ and D_3) whereas the right cell includes inductors (L_4 and L_5), diodes ($D_4, D_5,$ and D_6). The voltages V_{C1} and V_{C4} across capacitors C_1 and C_4, respectively are same, i.e., $V_{C1} = V_{C4}$ and similarly, $V_{C2} = V_{C3}$ which are voltages across C_2 and C_3, respectively. The operating characteristics of the proposed SL-SBZSI can be characterized in a similar manner to that of traditional ZSIs which have shoot and non-shoot through modes. These operating modes are discussed in the following subsections based on the corresponding equivalent circuits as shown in Figure 2a,b, respectively.

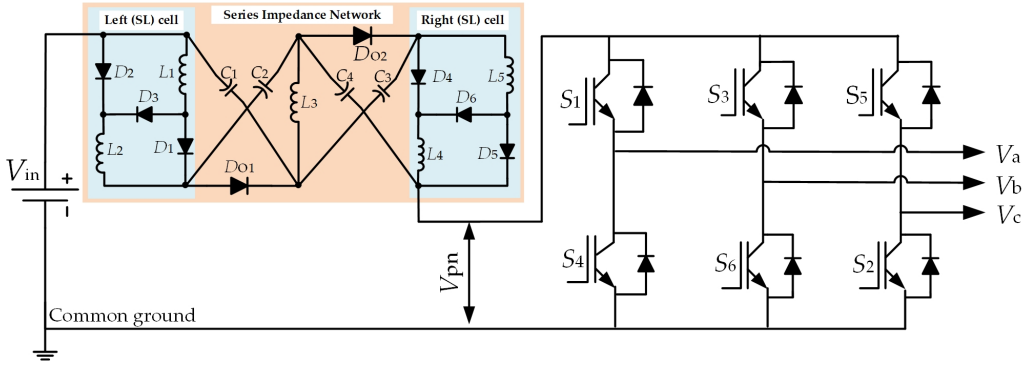
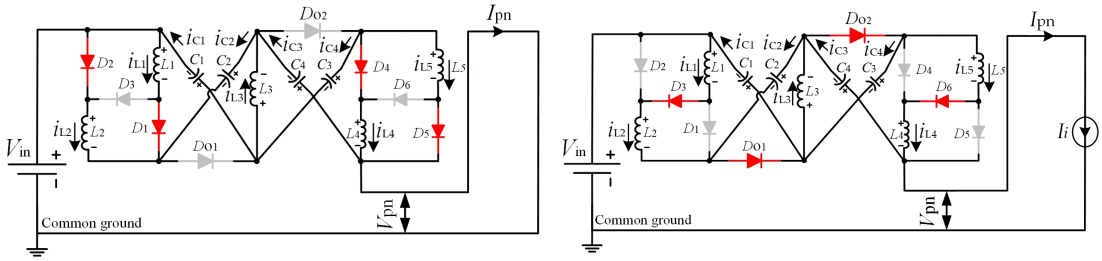


Figure 1. Proposed inverter (SL-SBZSI).



(**a**) (**b**)

Figure 2. Equivalent circuit: (**a**) shoot-through mode (**b**) non-shoot-through mode.

2.1. Shoot-Through Operating Mode

During the shoot-through (ST) operating mode, all semiconductor switches, i.e., S_1 to S_6 remain closed which can also be seen from Figure 2a. In this situation, the DC-link voltage becomes zero while diodes D_{01} and D_{02} remain open due to the reverse bias condition. The left and right SL cells are switched to a parallel configuration as diodes D_1, D_2, D_4 and D_5 are forward-biased. This operating mode allows to discharge capacitors C_1, C_2, C_3 and C_4 for which all currents through inductors L_1, L_2, L_3 and L_4 increase from their minimum to maximum values.

The relationships among voltages across different points and currents through different elements can be obtained by applying Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL), respectively. By applying KVL in Figure 2a, the inductor voltages across all inductors can be written as follows:

$$V_{L1} = V_{in} + V_{C2} + V_{C4}; V_{L1} = V_{L2} = V_{L4} = V_{L5} \tag{1}$$

$$V_{L3} = 3(\frac{V_{in}}{2} + V_{C2}), \tag{2}$$

where V_{L1} is the voltage across L_1, V_{L2} is the voltage across L_2, V_{L3} is the voltage across L_3, V_{L4} is the voltage across L_4, V_{L5} is the voltage across L_5, and V_{in} is the input voltage.

By applying KCL in Figure 2a, the currents flowing through capacitors can be written as follows:

$$I_{C1} = 2I_{L1} - I_{pn} \tag{3}$$

$$I_{C2} = -2I_{L1} \tag{4}$$

where I_{C1} is the current flowing through C_1, I_{C2} is the current flowing through C_2, I_{L1} is the current flowing through L_1, and I_{pn} is the shoot-through current.

The non-shoot-through operating mode, which is also known as the normal PWM mode or state, is discussed in the following subsection.

2.2. Non-Shoot-Through Operating Mode

During the non-shoot-through operating mode, the proposed SL-SBZSI acts like a traditional voltage source inverter as shown in Figure 2b. In this mode, the proposed topology generates the AC output voltage with the common complementary fashion of semiconductor switches. In this mode, diodes D_{01} and D_{02} become closed due to the forward bias condition. Furthermore, this operating mode enables D_3 and D_6 into the forward bias while the remaining diodes, i.e., D_1, D_2, D_4 and D_5 into the reverse bias for which inductors in both left and right SL cells are switched to series configurations. During this operating mode, all inductors and the input DC source supply power to the inverter. This means that the currents through inductor decrease and the voltages across the capacitor increase.

The relationships among voltages and currents in this operating mode can be obtained in a similar way to that of the shoot-through operating mode as discussed in the previous subsection, i.e., by applying KVL and KCL. By applying KVL in Figure 2b, the inductor voltages across all inductors can be written as follows:

$$V_{L1} = -\frac{V_{C4}}{2}; V_{L1} = V_{L2} = V_{L4} = V_{L5} \tag{5}$$

$$V_{L3} = -V_{C2} \tag{6}$$

By applying KCL in Figure 2b, the currents flowing through capacitors can be written as follows:

$$I_{C1} = I_{L1} - I_i \tag{7}$$

$$I_{C2} = \frac{I_{L3} - I_i}{2} \tag{8}$$

where I_{L3} is the current flowing through L_3 and I_i is the DC-link current during non-shoot-through state.

These operating characteristics are used to analyze the performance of the proposed SL-SBZSI. The performance characteristics of the proposed topology also require to have the mathematical model, analysis for the ripple in the inductor current, ripples in the voltages across capacitors, and inverter switching device power. All these are discussed in the following section.

3. Performance Characteristics of Proposed SL-SBZSI

This section provides the theoretical frameworks for analyzing the steady-state performance characteristics of the proposed topology. The theoretical frameworks are mainly based on the mathematical model, nature of the ripple current, ripples in the voltage across capacitors, and the inverter switching device power. The mathematical model of the proposed SL-SBZSI is presented in the following subsection.

3.1. Mathematical Modeling of Proposed SL-SBZSI

The mathematical model for the steady-state analysis is developed in this subsection and the key switching waveforms for the proposed SL-SBZSI is shown in Figure 3. During the steady-state condition, the average inductor voltage should be zero over a complete switching period as per the volt-sec balance principle. Thus, the inductor voltage, by using volt-sec balance principle for the proposed SL-SBZSI, can be expressed through the following equation:

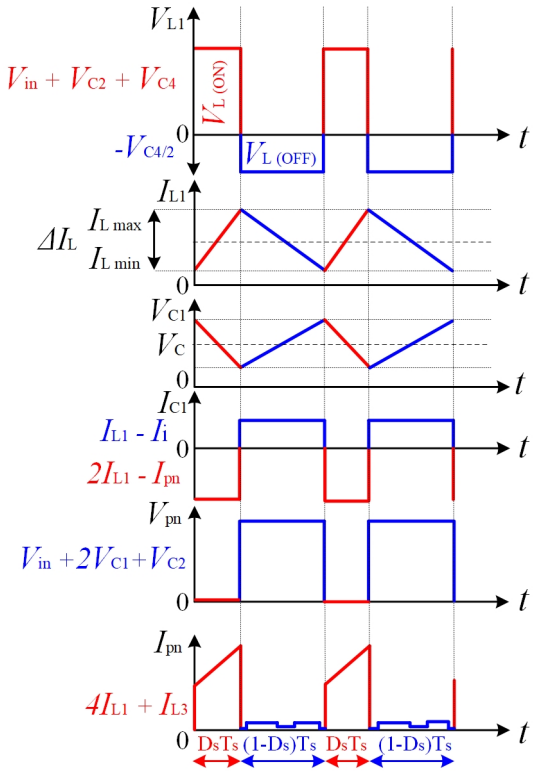


Figure 3. Key switching waveforms for the switched inductor assisted strong boost Z-source inverter (SL-SBZSI).

$$\frac{V_L(ON).D_S.T_S + V_L(OFF)(1-D_S).T_S}{T_S} = 0 \tag{9}$$

where D_S is the shoot-through duty ratio and T_S is the sampling time.

By using Equations (1) and (5) for V_{L1}, it can be written as:

$$\frac{(V_{in} + V_{C2} + V_{C4}).D_S.T_S + (-\frac{V_{C4}}{2})(1-D_S).T_S}{T_S} = 0. \tag{10}$$

By using Equations (2) and (6) for V_{L3}, it can be expressed as:

$$\frac{(\frac{3V_{in}}{2} + 3V_{C2}).D_S.T_S + (-V_{C2})(1-D_S).T_S}{T_S} = 0. \tag{11}$$

By solving Equation (10) for the voltage across capacitor V_{C4}, it can be written as follows:

$$V_{C1} = V_{C4} = \frac{2D_S(V_{in} + V_{C2})}{(1-3D_S)}. \tag{12}$$

Similarly, the solution of Equation (11) for the voltage across capacitor V_{C2} can be written as:

$$V_{C2} = V_{C3} = \frac{3D_S.V_{in}}{2(1-4D_S)}. \tag{13}$$

Substituting Equation (13) into Equation (12), the equation for V_{C4} can be simplified as:

$$V_{C1} = V_{C4} = \frac{D_S(2 - 5D_S).V_{in}}{(1 - 7D_S + 12{D_S}^2)}. \tag{14}$$

The peak DC-link voltage ($\hat{V}_{pn}$) during the non-shoot-through mode can be written as follows:

$$\hat{V}_{pn} = 2V_{C1} + V_{C2} + V_{in}. \tag{15}$$

Substituting Equations (13) and (14) into Equation (15), the peak DC-link voltage can be obtained as follows:

$$\hat{V}_{pn} = \frac{(2 - 3D_S - 5{D_S}^2).V_{in}}{2(1 - 7D_S + 12{D_S}^2)}. \tag{16}$$

The boost factor, B for the proposed SL-SBZSI can be written as the ratio of $\hat{V}_{pn}$ to V_{in} and this can be written as follows:

$$B = \frac{\hat{V}_{pn}}{V_{in}} = \frac{(2 - 3D_S - 5{D_S}^2)}{2(1 - 7D_S + 12{D_S}^2)}. \tag{17}$$

The boost factor and the capacitor voltage stress with variations in the shoot-through duty ratio are shown in Figure 4a–c, respectively. From these figures, it can be clearly seen that there is a fast increase in the boost factor and capacitor voltage stresses for a small duty ratio, especially when the shoot-through duty ratio is higher than 0.2. By considering the lossless condition, it can be written as:

$$P_{in} = V_{in}.I_{in} = P_{out} = V_{ph}.I_i \Rightarrow I_{in} = I_{L1} = \frac{V_{ph}.I_i}{V_{in}}, \tag{18}$$

where P_{in} is the input DC power, I_{in} is the input current, I_{L1} is the inductor current, I_i is the output current and V_{ph} is the output AC phase voltage. The input current can be expressed in terms of the load and AC voltage as $V_{ph} = I_i R_L$ where R_L is the load resistance. By substituting the relation in Equation (18), it can be rewritten as follows:

$$I_{L1} = \frac{(V_{ph})^2}{V_{in}.R_L}. \tag{19}$$

The input DC and output AC voltages can be expressed in terms of the modulation index and boost factor which can be written as follows:

$$V_{ph} = \frac{1}{\sqrt{2}}.(MB\frac{V_{in}}{2}), \tag{20}$$

where M is the modulation index. By using Equation (20), the inductor current in Equation (19) can be rewritten as follows:

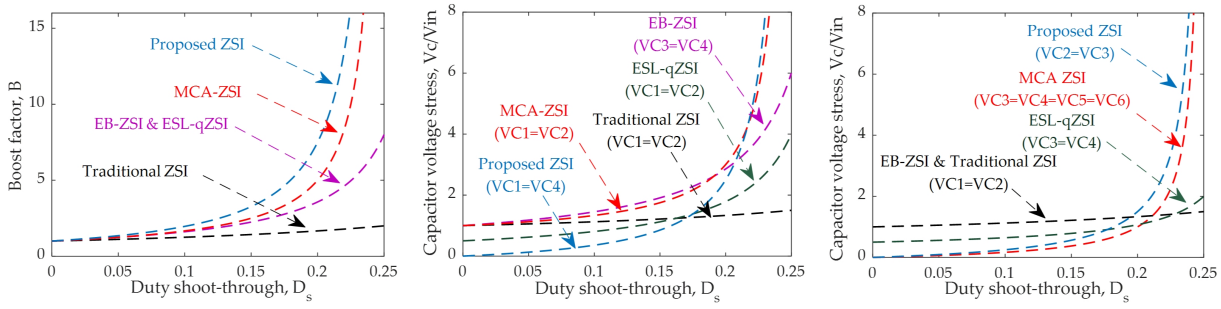
$$I_{L1} = \frac{[\frac{1}{\sqrt{2}}(MB.\frac{V_{in}}{2})]^2}{V_{in}.R_L}. \tag{21}$$

According to the simple boost PWM control method, the relationship between the duty cycle and modulation index can be expressed as $M = (1 - D_S)$. Using this relationship along with the substitution of Equation (17) into Equation (21) for three-phase proposed SL-SBZSI, it can be written as follows:

$$I_{L1} = \frac{3(1 - D_S)^2(2 - 3D_S - 5D_S^2)^2.V_{in}}{32R_L(1 - 7D_S + 12D_S^2)^2}. \tag{22}$$

During the shoot-through mode, the input current is zero for the proposed ZSI. At non-shoot-through mode, it can be expressed as the summation of the inductor and DC-link current as follows:

$$I_{in} = I_{L1} + I_i. \tag{23}$$



(**a**) (**b**) (**c**)

Figure 4. Characteristics curve: (**a**) boost factor, (**b**) capacitor voltage stress—high, (**c**) capacitor voltage stress—low.

The performance characteristics of the proposed SL-SBZSI is analyzed by considering this mathematical model.

3.2. Analysis of Ripples in the Inductor Current for the Proposed SL-SBZSI

It is well known that the voltage across the inductor (v_L) depends on the changes in the current flowing through the inductor which can be written as follows:

$$v_L = L\frac{di_L}{dt}, \tag{24}$$

where i_L is the current flowing through an inductor L. This voltage can be expressed in terms of the small changes in the current, i.e., the ripple current (Δi_L). For this purpose, the inductor voltage can be expressed as V_L which is actually the average value of v_L. If Δt is considered is a small period, the average value of the voltage in Equation (24) can be written as follows:

$$V_L = L\frac{\Delta i_L}{\Delta t}. \tag{25}$$

From Equation (25), the ripple in the current through L_1 can be written as follows:

$$\Delta i_{L1} = \frac{V_{L1}}{L}\Delta t. \tag{26}$$

From Equation (1), it can be seen that $V_{L1} = V_{in} + V_{C2} + V_{C4}$ during the shoot-through operating mode. Hence, the ripple in i_{L1} in Equation (26) during the shoot-through mode can be written as follows:

$$\Delta i_{L1}(ST) = \frac{V_{in} + V_{C2} + V_{C4}}{L}\Delta t(ST). \tag{27}$$

In the simple boost control, each switching cycle contains two shoot-through pulses and thus, the duration per shoot-through, $\Delta t(ST)$, is $\frac{D_S.T_S}{2}$. Using this, Equation (27) can be written as follows:

$$\Delta i_{L1}(ST) = \frac{V_{in} + V_{C2} + V_{C4}}{L}.\frac{D_S.T_S}{2}. \tag{28}$$

Substituting the values of V_{C2} and V_{C4} from Equations (13) and (14), respectively into Equation (28); it can be written as follows:

$$\Delta i_{L1}(ST) = \frac{D_S(D_S-1)(5D_S-2).V_{in}}{4f_S L_1(1-7D_S+12D_S^2)}, \tag{29}$$

where $f_S = 1/T_S$ is the sampling frequency.

From Equation (5), it can be seen that $V_{L1} = -\frac{V_{C4}}{2}$ during the non-shoot-through operating mode. Hence, the ripple in i_{L1} in Equation (26) during this non-shoot-through mode can be written as follows:

$$\Delta i_{L1}(nST) = -\frac{V_{C4}}{2L}\Delta t(nST). \tag{30}$$

In the simple boost control, the duration per non-shoot-through, $\Delta t(nST)$, is $\frac{(1-D_S).T_S}{2}$. Using this, Equation (30) can be written as follows:

$$\Delta i_{L1}(nST) = \frac{-V_{C4}}{2L}.\frac{(1-D_S).T_S}{2}. \tag{31}$$

Substituting the value of V_{C4} from Equation (14) into Equation (31), it can be written as follows:

$$\Delta i_{L1}(nST) = -\frac{D_S(D_S-1)(5D_S-2).V_{in}}{4f_S L_1(1-7D_S+12D_S^2)}. \tag{32}$$

From Equations (29) and (32), it can be seen that the ripple currents in i_{L1} during the shoot and non-shoot-through operating modes are the same. This statement is true for all currents flowing through different inductors though the amount of ripple can be different. To further justify this statement, the ripple currents in i_{L3}, i.e., the current flowing through L_3 during both shoot and non-shoot-through operating modes are calculated here.

During the shoot-through mode, the ripple in i_{L3} can be written as follows:

$$\Delta i_{L3}(ST) = \frac{V_{L3}(ST)}{L}.\frac{D_S.T_S}{2}. \tag{33}$$

From Equation (2), it can be seen that $V_{L3} = 3\left(\frac{V_{in}}{2} + V_{C2}\right)$ during the shoot-through operating mode. Hence, the ripple in i_{L3} in Equation (33) during the shoot-through mode can be written as follows:

$$\Delta i_{L3}(ST) = \frac{3V_{in}+6V_{C2}}{2L}.\frac{D_S.T_S}{2} \tag{34}$$

Substituting the value of V_{C2} from Equation (13) into Equation (34), it can be written as follows:

$$\Delta i_{L3}(ST) = \frac{3D_S(1-D_S).V_{in}}{4f_S L_3(1-4D_S)}. \tag{35}$$

During the non-shoot-through mode, the ripple in i_{L3} can be written as follows:

$$\Delta i_{L3}(ST) = \frac{V_{L3}(nST)}{L}\frac{(1-D_S).T_S}{2}. \tag{36}$$

From Equation (6), it can be seen that $V_{L3} = -V_{C2}$ during the non-shoot-through operating mode. Hence, the ripple in i_{L3} in Equation (36) during the non-shoot-through mode can be written as follows:

$$\Delta i_{L3}(nST) = \frac{-V_{C2}}{L}\frac{(1-D_S).T_S}{2}. \tag{37}$$

Substituting the value of V_{C2} from Equation (13) into Equation (37), it can be written as follows:

$$\Delta i_{L3}(nST) = -\frac{3D_S(1-D_S).V_{in}}{4f_S L_3(1-4D_S)}. \tag{38}$$

Equations (35) and (38) clearly indicate that the ripple currents in i_{L3} during the shoot and non-shoot-through operating modes are the same. The ripples in the current through the inductors in the ZSI affect the performance of input sources (e.g., fuel cell, PV units, etc.) which are connected to this inverter. The trade-off for minimizing the mismatch between the fuel cell and air utilization in fuel cells directly links with the generation of ripple currents [37] and the reduction in the average output power of the PV unit increases the generation of the ripple current [38]. Depending on the application of the power conditioning system, a certain value of the ripple can be allowed in the current flowing through the inductor for the satisfactory operation which needs to be selected in a precise way. In [39], the value of the ripple in the current flowing through an inductor is selected for prototyping a 50-kW fuel cell-based ZSI by following the standard design criteria. For the proposed SL-SBZSI, the ripple current value for the inductors is chosen as 30% of its average inductor current. Furthermore, as part of the fundamental mathematical modeling, the ripples in the voltages across capacitors are analyzed in the following subsection.

3.3. Analysis of Ripples in the Capacitor Voltage for the Proposed SL-SBZSI

The ripples in the capacitor voltage can be calculated in a similar way as presented in the previous subsection. The charging current flowing through the capacitor (i_C) can be written as follows:

$$i_C = C\frac{dv_C}{dt}, \tag{39}$$

where v_C is the voltage across the capacitor C. This current can be expressed in terms of the small changes in the voltage, i.e., the ripple voltage (Δv_C). For this reason, the capacitor current can be expressed as I_C which is actually the average value of i_C. When Δt is taken as a small period, the average capacitor current can be written as follows:

$$I_C = C\frac{\Delta v_C}{\Delta t}. \tag{40}$$

From Equation (40), the ripple voltage of capacitor C_1 can be written as follows:

$$\Delta v_{C1} = \frac{I_{C1}}{C}\Delta t. \tag{41}$$

From Equation (3), it can be seen that $I_{C1} = 2I_{L1} - I_{pn}$ during shoot-through operating mode. Hence, the ripple in v_{C1} in (41) during the shoot-through mode can be written as follows:

$$\Delta v_{C1}(ST) = \frac{2I_{L1} - I_{pn}}{C}\Delta t(ST). \tag{42}$$

Each switching cycle contains two shoot-through pulses and as stated in the in the previous subsection, the duration per shoot-through, $\Delta t(ST)$ is $\frac{D_S.T_S}{2}$. Using this, Equation (42) can be written as follows:

$$\Delta v_{C1}(ST) = \frac{2I_{L1} - I_{pn}}{C}.\frac{D_S.T_S}{2}. \tag{43}$$

By using Equations (3) and (7), the voltage ripples for capacitor C_1 and C_4 during the shoot-through and non-shoot-through modes can be derived as follows:

$$\Delta v_{C1}(ST) = \Delta v_{C4}(ST) = \frac{D_S(2I_{L1} - I_{pn})}{2Cf_S}. \tag{44}$$

$$\Delta v_{C1}(nST) = \Delta v_{C4}(nST) = \frac{(1 - D_S)(I_{L1} - I_i)}{2Cf_S}. \tag{45}$$

The numerical values of ripples for voltages across C_1 and C_4 during the shoot and non-shoot-through modes are same though their expressions in Equations (44) and (45) appeared differently.

By applying the same process and using Equations (4) and (8), the voltage ripples for capacitor C_2 and C_3 during the shoot-through and non-shoot-through modes can be expressed as follows:

$$\Delta v_{C2}(ST) = \Delta v_{C3}(ST) = \frac{-D_S.I_{L1}}{Cf_S}. \tag{46}$$

$$\Delta v_{C2}(nST) = \Delta v_{C3}(nST) = \frac{(1 - D_S)(I_{L3} - I_i)}{4Cf_S}. \tag{47}$$

The numerical values of ripples for voltages across C_2 and C_3 during the shoot and non-shoot-through modes will also be same though their expressions in Equations (46) and (47) look different. The purpose of these capacitors in the ZSI is to absorb the ripples in the current and maintain a constant voltage. In [39], the value of the ripple in the voltage across the capacitor is chosen 3% which is a standard allowable value for designing power converters. In this proposed ZSI, the value of capacitor voltage ripple is kept within the standard design value and which is 0.6%.

3.4. Inverter Switching Device Power

For any inverter, the semiconductor switches in the H-bridge circuit need to be selected in such a way that these switches can withstand the maximum impressed voltage while flowing the peak and average currents through these. The switching device power (SDP) is a measure which is used to determine the switching requirements according to generated voltage and current stress. The SDP is expressed in terms of the product of the voltage and current stress. Hence, the total SDP is measured as the cumulative SDP of all switching devices within the H-bridge circuit. As the total SDP indicates the size of the semiconductor device used in the circuit, it becomes an important cost index for the inverter. The average value of the total SDP (SDP_{av}) can be calculated as follows:

$$SDP_{av} = \sum_{i=1}^{N} V_i.I_{i_{av}}, \tag{48}$$

where N is the number of semiconductor devices within the H-bridge, V_i is the impressed voltage on i-th device, and $I_{i_{av}}$ is the average current flowing through i-th device. Similarly, the peak value of the total SDP (SDP_P) can be calculated as follows:

$$SDP_P = \sum_{i=1}^{N} V_i.I_{i_P} \tag{49}$$

where I_{i_P} is the peak current flowing though i-th device.

The currents flowing through the inverter bridges during different operating modes mainly comprise of two components:

- Current to load during the non-shoot-through mode and
- Current through switches during the shoot-through mode.

The SDP is usually calculated by considering the shoot-through operation and the current paths for switches during the shoot-through operation is shown in Figure 5. From this figure, it can be seen that the current during this shoot-through mode is distributed into three parallel paths due to the symmetric structure of the H-bridge.

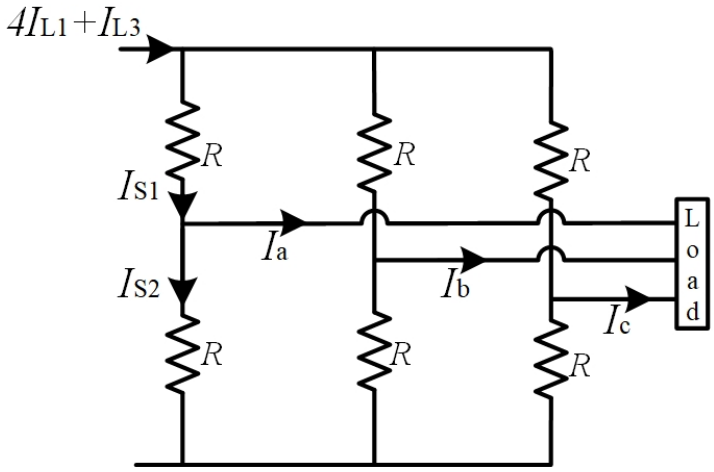


Figure 5. Inverter switching device power (SDP) model.

The current flowing through the inverter bridge is the sum of all currents flowing through the inductor. Hence the average current through each switch during the shoot-through mode can be written as follows:

$$I_{av}(ST) = \frac{4I_{L1} + I_{L3}}{3} \tag{50}$$

The proposed topology acts as a traditional inverter during the non-shoot-through operation and hence, the average current during this non-shoot-through mode can be written as follows:

$$I_{av}(nST) = \frac{\sqrt{2}P_o}{3V_{ph}\cos\phi\pi}.(1 - D_S), \tag{51}$$

where $\hat{V}_{ph}$ is the output phase voltage, $\cos\phi$ is the power factor of the load, and P_o is the output power of the inverter. The output phase voltage of the inverter can be written as follows:

$$\hat{V}_{ph} = \frac{M.\hat{V}_{pn}}{2\sqrt{2}} = \frac{M.BV_{in}}{2\sqrt{2}} \tag{52}$$

as $\hat{V}_{pn} = BV_{in}$. Using Equation (52), Equation (51) can be written as follows:

$$I_{av}(nST) = \frac{\sqrt{2}.2\sqrt{2}P_o}{3.B.V_{in}.M.\cos\phi\pi}.(1 - D_S). \tag{53}$$

The overall average value of the current can be written as follows:

$$I_{av} = I_{av}(ST) + I_{av}(nST) = \frac{4I_{L1} + I_{L3}}{3}.D_S + \frac{\sqrt{2}.2\sqrt{2}P_o}{3.B.V_{in}.M.\cos\phi\pi}.(1 - D_S). \tag{54}$$

The average value of the total SDP for the proposed inverter can be written as:

$$SDP_{av} = 6.I_{av}.\hat{V}_{pn}. \tag{55}$$

Substituting the value of I_{av} from Equation (54) and using $\hat{V}_{pn} = BV_{in}$, Equation (55) can be rewritten as follows:

$$SDP_{(Average)} = 2.B.V_{in}.(4I_{L1} + I_{L3}).D_S + \frac{8P_o.(1 - D_S)}{\cos\phi\pi M}. \tag{56}$$

The switches conduct peak inverter current during the shoot-through mode. This peak current was calculated by assuming all switches within the H-bridge were ON and presenting these switches through pure resistors with the same value as shown in Figure 5. By applying KCL in Figure 5, it can be written as:

$$I_{S1} + I_{S2} = \frac{2(4I_{L1} + I_{L3})}{3} \tag{57}$$

$$I_{S1} - I_{S2} = I_a, \tag{58}$$

where I_{S1} is the current flowing through the first switch, I_{S2} is the current flowing through the second switch, and I_a is the current flowing through line a. By solving Equations (57) and (58) for I_{S1}, it can be written as follows:

$$I_{S1} = \frac{4I_{L1} + I_{L3}}{3} + \frac{I_a}{2}. \tag{59}$$

The peak current flows through the first switch when the line current of the inverter is at its peak value, i.e., I_a is at its peak. The peak value of I_a can be written as:

$$I_{a_{(Peak)}} = \frac{\sqrt{2}P_o}{3\cos\phi\hat{V}_{ph}}. \tag{60}$$

Substituting the value of $\hat{V}_{ph}$ from Equation (52) into Equation (59), it can be written as:

$$I_{a_P} = \frac{4P_o}{3\cos\phi M.B.V_{in}} \tag{61}$$

The peak value of the total SDP for the proposed inverter can be calculated as follows:

$$SDP_P = 6.I_{a_P}.\hat{V}_{pn}. \tag{62}$$

Substituting the value of I_{a_P} from Equation (61) and using $\hat{V}_{pn} = BV_{in}$, Equation (62) can be rewritten as follows:

$$SDP_{(Peak)} = 2.B.V_{in}.(4I_{L1} + I_{L3}) + \frac{4P_o}{\cos\phi M}. \tag{63}$$

For selecting semiconductor devices in any power converter, the proper selection of the SDP is crucial as it is associated with the thermal requirement of the inverter. A detailed comparative study associated with the SDP for traditional and Z-source inverters is carried out in [40] where the average and peak SDP with the same specification are calculated. Equations (16) and (59) are the dominant parts of the final SDP model derived in (56) and (63) and can be used for the selection of semiconductor devices of proposed ZSI. Based on the application and peak power of the converter, the SDP requirement will vary as the peak current following through the semiconductor switches will vary and thus, the maximum voltages across these. Typically, the SDP is measured in KVA and the required KVA is generally chosen as a higher value than the calculated value.

All these performance characteristics are analyzed through rigorous simulation results in the later section. As the proposed topology uses a simple boost control method, it is discussed in the following section.

4. Inverter Switching Control Method

This section describes the PWM scheme to generate the shoot-through pulses. For the simplicity in control algorithm, the simple boost control (SBC) method as presented in [41] is used in this proposed topology. In the normal PWM scheme, the top and bottom switches of the inverter bridge legs are triggered in a complementary fashion when the triangular waveform $V_{Carrier}$ is greater or lower than upper or lower values of the modulation waveforms V_a, V_b, and V_c as shown in Figure 6.

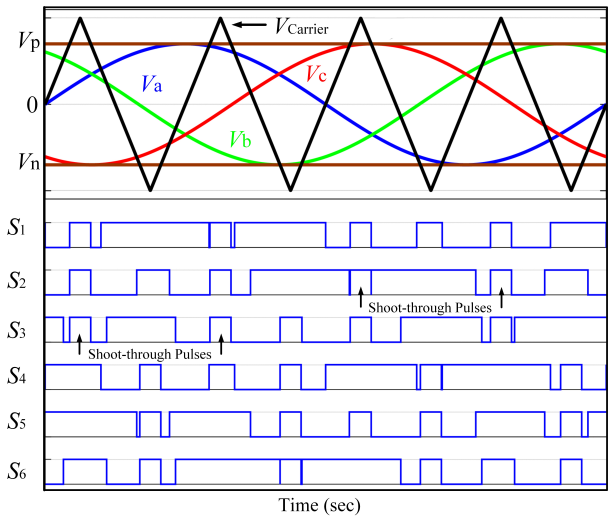


Figure 6. Switching signals of simple boost pulse width modulation (PWM) control.

In the SBC method, one positive DC waveform, V_p and another negative DC waveform, V_n are inserted to the traditional PWM scheme to control the shoot-through pulses. When the triangular carrier wave is greater than the positive DC waveform, first inverter bridge leg enters into the shoot-through

state whereas another inverter bridge leg will enter into the shoot-through state when triangular carrier wave is lower than the negative DC waveform. This shoot-through can be generated through only one phase leg or the combination of any two legs or all three-phase legs of the inverter bridge. During zero state switching period of the traditional PWM control, the shoot-through pulses are placed into zero states which turn ON the semiconductor switches by keeping the active PWM states unchanged. Hence, the output sinusoidal voltage is maintained normally and at the same time, the inverter obtains high boosting capability by shooting through the DC-link voltage of the inverter. The switching pulses of the SBC with the shoot-through pulses for the three-phase inverter bridge are also depicted in Figure 6.

The voltage gain of the inverter can be written as follows [36]:

$$G = M \times B. \tag{64}$$

Substituting Equation (17) to Equation (64), the voltage gain of the proposed inverter can be written as:

$$G = M \times \frac{(2 - 3D_S - 5{D_S}^2)}{2(1 - 7D_S + 12{D_S}^2)}. \tag{65}$$

Since $M = (1 - D_S)$ for the SBC method, Equation (65) can be written as follows:

$$G = \frac{(1 - D_S)(2 - 3D_S - 5{D_S}^2)}{2(1 - 7D_S + 12{D_S}^2)}, \tag{66}$$

which represents the relationship between the voltage gain and the modulation index.

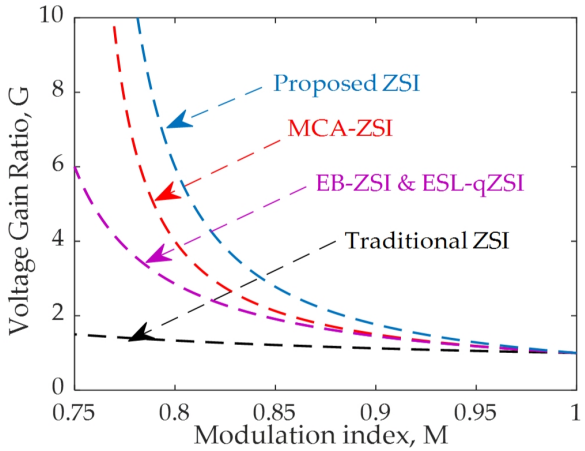


Figure 7. Characteristic curve: modulation index vs. voltage gain.

Figure 7 shows the voltage gain characteristics of the proposed SL-SBZSI along with different existing topologies with respect to the modulation index. From the characteristic curves in Figure 7, it can be clearly seen that the voltage gain significantly increased in the proposed SL-SBZSI as compared to other topologies while using the same value of the modulation index. The improved voltage gain characteristics of the proposed SL-SBZSI ensures the superiority over other existing ZSIs. A comparative study is presented to justify other steady-state characteristics, e.g., capacitor voltage stress with respect to the boost factor in the following section.

5. Comparative Analysis for the Capacitor Voltage Stress

This section presents a comparative analysis for the proposed SL-SBZSI against different existing topologies such as traditional ZSI, EB-ZSI, ESL-qZSI, and MCA-ZSI. As mentioned earlier, the proposed SL-SBZSI exhibits quite similar characteristics to that of an MCA-ZSI. Table 1 shows different factors associated with the performance of the proposed SL-SBZSI and MCA-ZSI. However, the comparative performance is analyzed against all above-mentioned topologies in terms of the capacitor voltage stress (both high and low stressed conditions) with variations in the boost factor. The capacitor voltage stresses for the high and low stressed capacitors are shown in Figure 8a,b, respectively. From these figures, it can be clearly seen that there are lower stresses on the capacitor voltages for the proposed topology as compared to all other topologies.

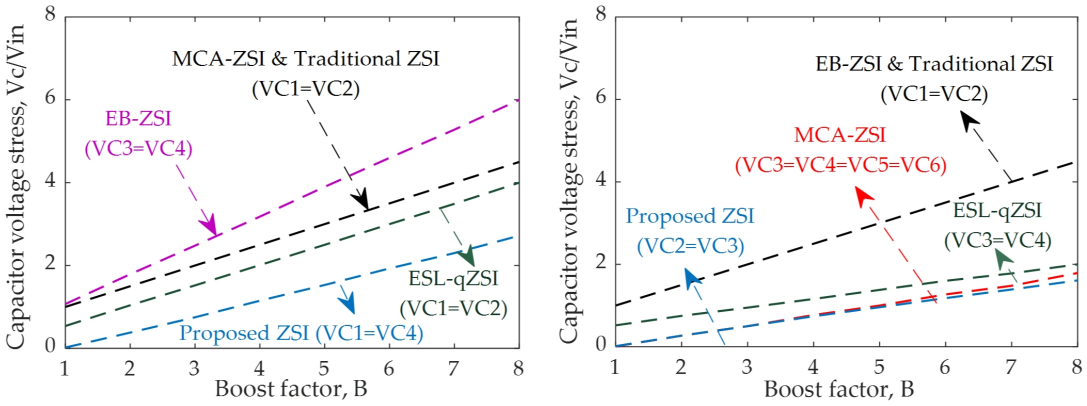


Figure 8. Characteristics curve: (**a**) high stressed capacitor and (**b**) low stressed capacitor.

Table 1. Parameters associated with the performance of the switched inductor assisted strong boost Z-source inverter (SL-SBZSI) and modified capacitor assisted Z-source inverter (MCA-ZSI) for the same D_S and V_{in}

No	Parameters	MCA-ZSI	Proposed SL-SBZSI
1	Boost factor, B	$\frac{(1-D_S)}{(1-5D_S+4{D_S}^2)}$	$\frac{(2-3D_S-5{D_S}^2)}{2(1-7D_S+12{D_S}^2)}$
2	Capacitor voltage, V_{C1}	$\frac{(1-2D_S)(1-D_S)}{(1-5D_S+4{D_S}^2)}V_{in}$	$\frac{D_S(2-5D_S)}{(1-7D_S+12{D_S}^2)}.V_{in}$
3	Capacitor voltage, V_{C3}	$\frac{D_S(1-D_S)}{(1-5D_S+4{D_S}^2)}V_{in}$	$\frac{3D_S}{2(1-4D_S)}.V_{in}$
4	Voltage gain, G	$\frac{(1-D_S)^2}{(1-5D_S+4{D_S}^2)}$	$\frac{(1-D_S)(2-3D_S-5{D_S}^2)}{2(1-7D_S+12{D_S}^2)}$
5	Inductor current, $\bar{I_L}$	$\frac{(1-D_S)(I_{in}-I_i)}{4D_S}$	$\frac{3(1-D_S)^2(2-3D_S-5D_S^2)^2}{32R_L(1-7D_S+12D_S^2)^2}.V_{in}$
6	Input current, I_{in}	$\frac{(1-D_S)I_i}{(1-5D_S+4{D_S}^2)}$	$\frac{3(1-D_S)^2(2-3D_S-5D_S^2)^2.V_{in}}{32R_L(1-7D_S+12D_S^2)^2}+I_i$
7	ST current, I_{pn}	$4I_{L1}$	$4I_{L1}+I_{L3}$
8	Load current, I_o	$\frac{(1-D_S)V_{pn}}{R_L}$	$\frac{(1-D_S)V_{pn}}{R_L}$

6. Calculation of Power Loss and Efficiency of the Proposed SL-SBZSI

The total power loss of the proposed SL-SBZSI is calculated based on the power loss in each component. In the proposed topology, there are some diodes which are ON during the shoot-through mode while remaining diodes are ON during the non-shoot-through operating mode. The input diodes (D_{01} and D_{02}) are on during the non-shoot-through mode and the power loss ($P_{D_{01},D_{02}}$) within these diodes can be calculated as follows:

$$P_{D_{01},D_{02}} = 2 * [v_D.I_{in} + (1 - D_S).I_{in}^2.r_D + \frac{2}{M}\hat{V}_{ph}.I_{in}\frac{T_{sw}}{6}], \tag{67}$$

where v_D is the forward voltage drop across the diode, r_D is the internal resistance of the diode, and T_{sw} is the switching time.

The diodes (D_3 and D_6) in the SL cells were also ON during the non-shoot-through mode and the power loss (P_{D_3,D_6}) within these two diodes can be calculated as follows:

$$P_{D_3,D_6} = 2 * [v_D.(1 - D_S).I_{L1} + (1 - D_S).I_{L1}^2.r_D + 2V_{C1}.I_{L1}.\frac{T_{sw}}{6}]. \tag{68}$$

During the shoot-through mode, diodes (D_1, D_2, D_4, and D_5) in the SL cells were ON and the power loss in these diodes can be written as:

$$P_{D_1,D_2,D_4,D_5} = 4 * [v_D.D_S.I_{L1} + D_S.I_{L1}^2.r_D + \frac{V_{C1}}{2}.I_{L1}.\frac{T_{sw}}{6}] \tag{69}$$

The power loss (P_{L_1,L_2,L_4,L_5,L_3}) in all inductors, i.e., L_1, L_2, L_4, L_5, and L_3 for the proposed topology can be counted as follows:

$$P_{L_1,L_2,L_4,L_5,L_3} = 4 * [I_{L1}^2.r_L] + [I_{L3}^2.r_L], \tag{70}$$

where r_L is the internal resistance of the inductor. Similarly, the power loss (P_{C_1,C_4,C_2,C_3}) in all capacitors can be written as follows:

$$P_{C_1,C_4,C_2,C_3} = 2 * [D_S.I_{C1}^2.r_C + (1 - D_S).I_{C1}^2.r_C] + 2 * [D_S.I_{C3}^2.r_C + (1 - D_S).I_{C3}^2.r_C], \tag{71}$$

where r_C is the internal resistance of the capacitor.

The switching (P_{sw}) and conduction (P_{cond}) losses for the MOSFET switches can be expressed as follows [31]:

$$P_{sw} = (t_{on} + t_{off}).f_S.V_{out}.(2 - D_S).I_{in} \tag{72}$$

$$P_{cond} = r_{ds} * [\frac{2}{3}.D_S.(2 - D_S)^2.I_{in}^2 + \frac{1.08.(1 - D_S)^3.P_{out}^2}{M^2.B^2.V_{in}^2}], \tag{73}$$

where t_{on} in the ON time of the switch, t_{off} in the OFF time of the switch, r_{ds} is the MOSFET drain to source resistance.

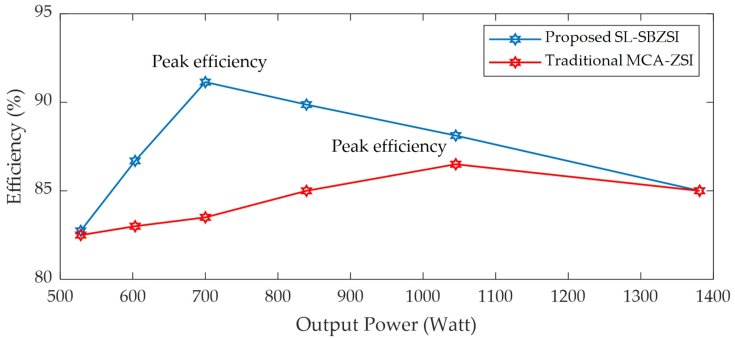


Figure 9. Efficiency curves.

All these losses are used to calculate the total loss for the proposed SL-SBZSI and the efficiency is calculated based on these losses. The values of equivalent series resistors for the inductor and capacitor are obtained from BOURNS toroid inductor and KEMET (ELG108M200AT2AA) datasheets, respectively [42]. The internal resistance of the inductor (r_L), which is also known as the equivalent series resistor (ESR) of the inductor, is chosen as 16 mΩ and the internal resistor of the capacitor, i.e., the ESR of the capacitor as 45 mΩ. The efficiency of the proposed topology is calculated by considering the diode model as MUR840G and the MOSFET model as STW45NM50.

The overall efficiency is shown in Figure 9, from where it can be noticed that the proposed inverter works in maximum efficiency of 91.14% at 700 W, whereas the traditional inverter has a maximum efficiency of 86.5% at 1045 W.

7. Simulation Results

The performance of the designed SL-SBZSI topology as shown in Figure 1 is verified through simulation results in Matlab/Simulink and compared with the existing MCA-ZSI topology. The SBC-based PWM scheme is adopted as a shoot-through control technique for both topologies. The parameters used for the simulation are listed in Table 2.

Table 2. Simulation parameters.

No	Parameters	Symbols	Value
1	Input voltage	V_{in}	50 V
2	Capacitance	$C_1 = C_2 = C_3 = C_4$	500 µF
3	Inductance	$L_1 = L_2 = L_3 = L_4 = L_5$	700 µH
4	Switching frequency	f_S	10 kHz
5	Output filter	L_f, C_f	1 mH, 110 µF
6	Load	R_L	60 Ω/phase

The simulation studies are carried out by considering the following four cases:

- Analysis of the voltage and current characteristics with the fixed input voltage and shoot-through duty ratio.
- Analysis of the voltage and current characteristics with the fixed input voltage and boost factor but different shoot-through duty ratios.
- Analysis of the voltage and current characteristics with the fixed input voltage but slower variations in the shoot-through duty ratio.
- Analysis of dynamic voltage compensation characteristics.

All these cases are discussed in the following with detailed analysis.

- Case 1: analysis of the voltage and current characteristics with the fixed input voltage and shoot-through duty ratio.

In this case, the input voltage, V_{in} is considered as 50 V and the shoot-through duty ratio as $D_S = 0.2$ for both the designed SL-SBZSI and existing MCA-ZSI. Under this condition, the voltage and current responses are observed for both SL-SBZSI and MCA-ZSI. The DC-link voltage V_{pn}, the capacitor voltage V_C, and the output load voltage (V_{ab}) between phase a and phase b are shown in Figure 10a,b for the existing MCA-ZSI and designed SL-SBZSI, respectively. The corresponding enlarged versions of these responses are shown in Figure 10c,d, respectively.

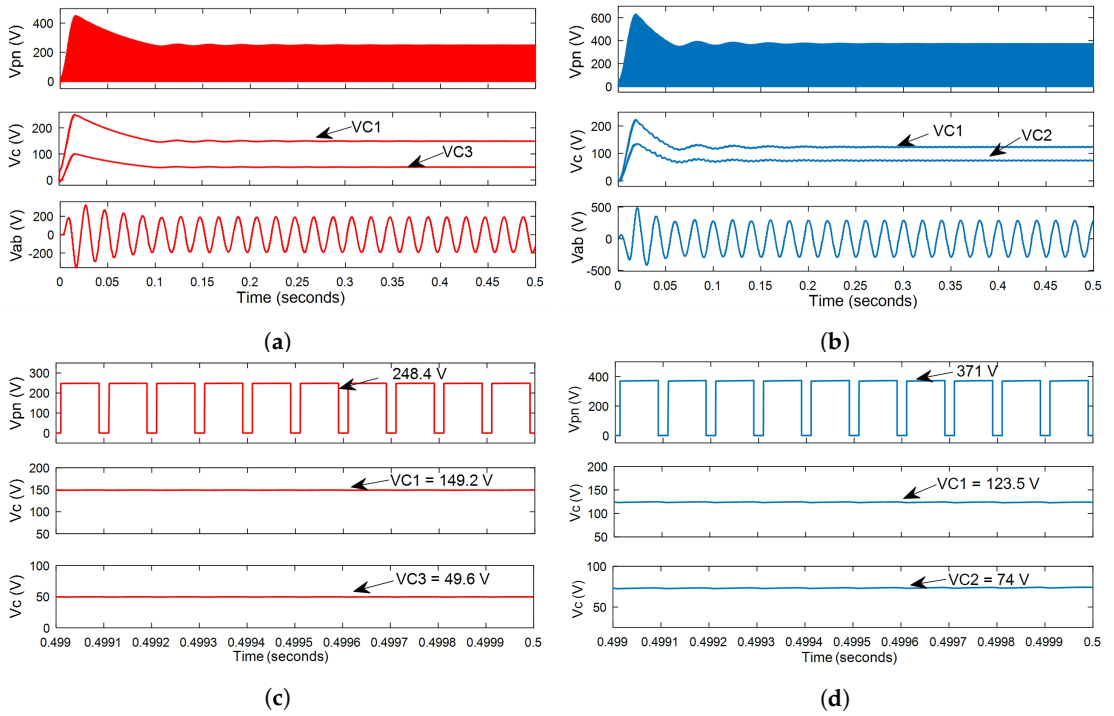


Figure 10. Simulation results (case 1): (**a**) traditional modified capacitor assisted Z-source inverter (MCA-ZSI). (**b**) Proposed SL-SBZSI. From top to bottom: DC-link voltage, V_{pn}; capacitor voltage, V_C and output line voltage, V_{ab}. Enlarge waveform: (**c**) traditional MCA-ZSI. (**d**) Proposed SL-SBZSI. From top to bottom: DC-link voltage, V_{pn}; capacitor voltage; V_{C1} and capacitor voltage; V_{C3}.

From Figure 10c, it can be seen that the DC-link voltage of the existing MCA-ZSI boosted from 50 V to 248.4 V. Figure 10c also shows that the capacitor voltages for the MCA-ZSI corresponding to this condition are $V_{C1} = 149.2$ V and $V_{C3} = 49.6$ V while the rms value of the phase to phase voltage is obtained as 136 V, i.e., $V_{ab}(rms) = 136$ V as presented in Figure 10a. By using all these values, the boost factor (B) and the voltage gain (G) for the existing MCA-ZSI can be calculated as 4.96 and 3.97, respectively. The similar voltage responses for the designed SL-SBZSI can be seen from Figure 10b,d.

From Figure 10d, it can be seen that DC-link voltage of the designed SL-SBZSI boosted from 50 V to 371 V. Figure 10d also shows that the capacitor voltages for the SL-SBZSI corresponding to this condition are $V_{C1} = 123.5$ V and $V_{C3} = 74$ V while the rms value of the phase to phase voltage is obtained as 204 V, i.e., $V_{ab}(rms) = 204$ V as presented in Figure 10b. By using all these values, the boost factor (B) and the voltage gain (G) for the designed SL-SBZSI can be calculated as 7.42 and 5.93, respectively. From these

analyses, it can be summarized that the designed topology improves the boost factor and voltage gain almost 1.5 times higher than an existing MCA-ZSI for the same input voltage and shoot-through duty ratio. Furthermore, the capacitor voltage reduces by around 17% for the high stressed capacitor in the designed SL-SBZSI as compared to the MCA-ZSI. However, the capacitor voltage increases by around 33% for the low stressed capacitor in the designed SL-SBZSI as compared to the MCA-ZSI.

Similarly, the input current I_{in}, the shoot-through current I_{pn}, and the inductor current (I_L) are shown in Figure 11a,b for the existing MCA-ZSI and designed SL-SBZSI, respectively. The corresponding enlarged version of these responses is shown in Figure 11c,d, respectively.

From Figure 11a,b, it can be seen that there exist input inrush current occurrence in both topologies. However, the inrush current in the designed SL-SBZSI is much lower than the existing MCA-ZSI. From Figure 11c, it can be seen that the average values of the input, shoot-through, and inductor currents for the existing MCA-ZSI are 6.3 A, 25.2 A, and 6.3 A, respectively. On the other hand, the average values of the input, shoot-through, and inductor currents for the designed SL-SBZSI are found 14.05 A, 60.77A, and 11.68 A, in Figure 11d respectively.

The ripples in the capacitor voltages and inductor are shown in Figure 12. From Figure 12, it can be seen that ripples of the capacitor voltages V_{C1} and V_{C2} are 0.75 V and 0.44 V, respectively while these values in the inductor currents I_{L1} and I_{L3} are 3.5 A and 4.2 A, respectively.

- Case 2: analysis of the voltage and current characteristics with the fixed input voltage and boost factor but different shoot-through duty ratios.

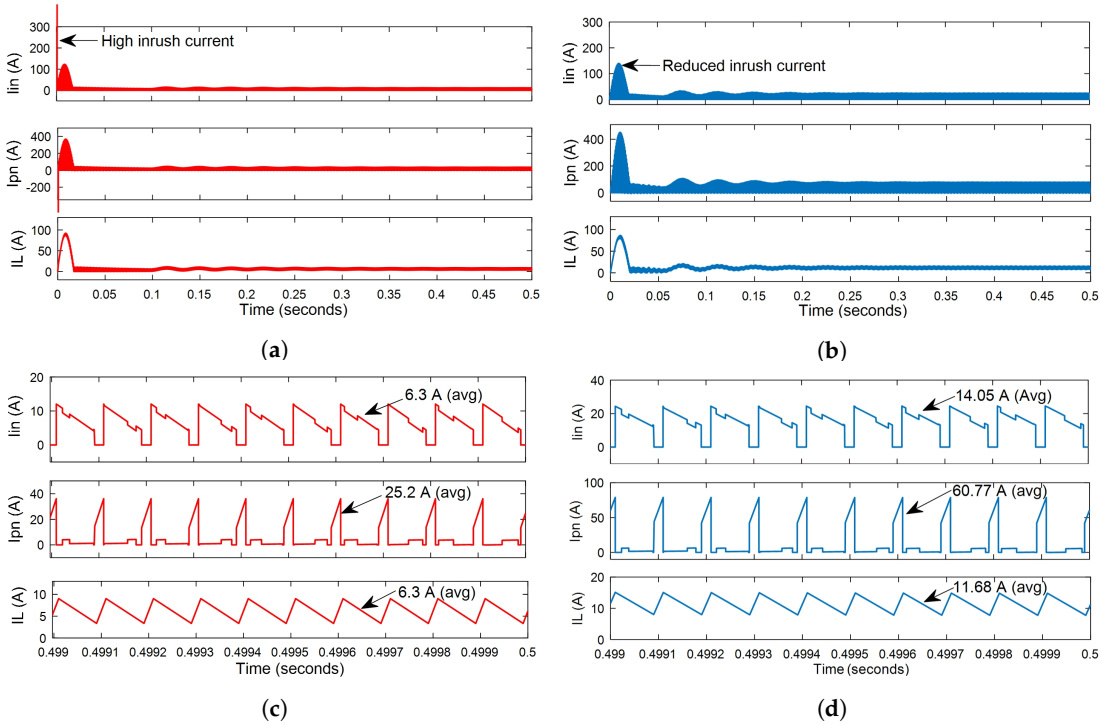


Figure 11. Simulation results (case 1): (**a**) traditional MCA-ZSI. (**b**) Proposed SL-SBZSI. From top to bottom: input current, I_{in}; shoot-through current; I_{pn} and inductor current, I_{L1}. Enlarge waveform: (**c**) Traditional MCA-ZSI. (**d**) Proposed SL-SBZSI. From top to bottom: input current, I_{in}; shoot-through current; I_{pn} and inductor current, I_{L1}.

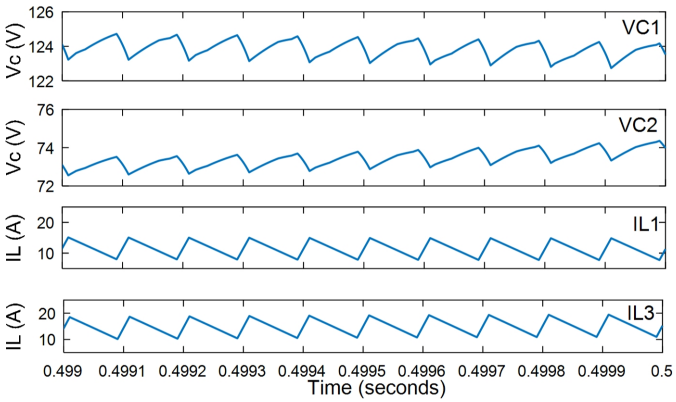


Figure 12. Capacitor and inductor voltage and current ripple.

In this case study, the input voltage and the boost factor are considered as same for both the existing MCA-ZSI and designed SL-SBZSI while using different shoot-through duty ratios. The value of the input voltage (V_{in}) and the boost factor (B) are considered as 50 V and 5, respectively. The values of the shoot-through duty ratio (D_S) are considered as 0.2 and 0.18 for the existing MCA-ZSI and designed SL-SBZSI, respectively. The DC-link voltage, the high stressed capacitor voltage, and the low stressed capacitor voltage for the existing MCA-ZSI and designed SL-SBZSI are shown in Figure 13a,b, respectively.

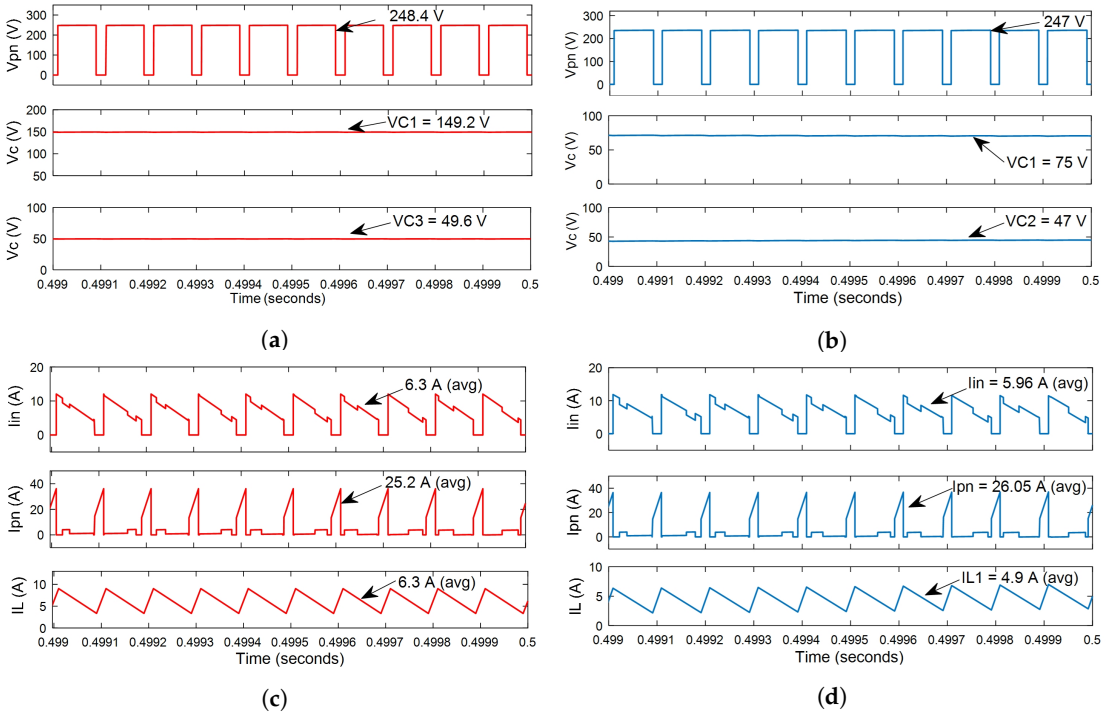


Figure 13. Simulation results (case 2): (**a**) traditional MCA-ZSI. (**b**) Proposed SL-SBZSI. From top to bottom: DC-link voltage, V_{pn}; capacitor voltage, V_{C1} and capacitor voltage, V_{C3}. Enlarge waveform: (**c**) Traditional MCA-ZSI. (**d**) Proposed SL-SBZSI. From top to bottom: input current, I_{in}; shoot-through current, I_{pn} and inductor current, I_{L1}.

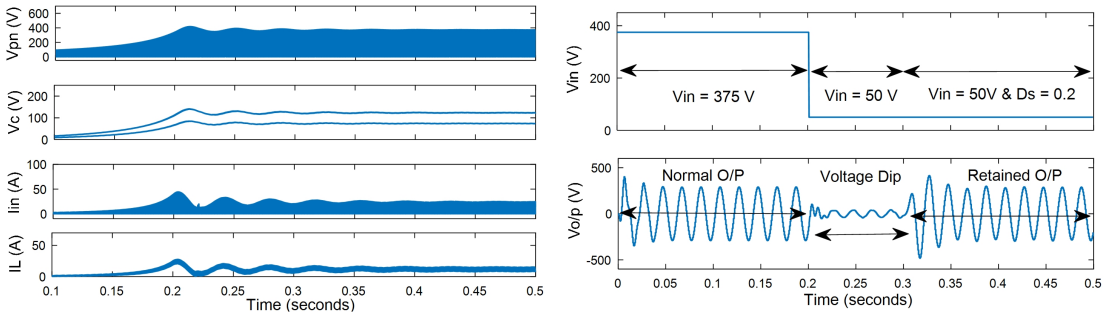
From these figures, it can be seen that the values of these voltages for the MCA-ZSI are 248.4 V, 149.2 V, and 49.6 V, respectively; while these for SL-SBZSI are 247 V, 75 V, and 47 V, respectively. This situation

clearly indicates that the input voltage is boosted to a similar value for both topologies. However, the capacitor voltage stresses are reduced for the designed SL-SBZSI as compared to the MCA-ZSI. Hence, it can be concluded that the designed topology exhibits lower capacitor voltage stresses as compared to the MCA-ZSI for the same boosting capability.

The corresponding input, shoot-through, and inductor currents for the existing MCA-ZSI and designed SL-SBZSI are shown in Figure 13c,d, respectively. From these figures, it can be seen that the average value of the shoot-through current for the designed SL-SBZSI is slightly higher than the MCA-ZSI. However, the input and inductor currents are lower in the designed SL-SBZSI as compared to the MCA-ZSI.

- Case 3: analysis of the voltage and current characteristics with the fixed input voltage but slower variations in the shoot-through duty ratio.

This case study was used to analyze the impact of the inrush current while applying a fixed input voltage. The input voltage (V_{in}) is still considered as 50 V but the duty shoot-through ratio (D_S) is slowly varied from 0 to 0.2 within 200 ms. In this way, the soft-start strategy is adopted which is an inherent characteristic of the designed SL-SBZSI. From Figure 14a, it can be seen that the slow increases in the shoot-through duty ratio from 0 to 0.2 within 200 ms, significantly reduces the inrush current and suppresses the resonance without any voltage and current surge. Therefore, it can be summarized that the designed SL-SBZSI does not exhibit high start-up inrush current.



(**a**) (**b**)

Figure 14. Simulation results: (**a**) soft-start waveform in case 3, and (**b**) dynamic voltage compensation in case 4.

- Case 4: analysis of dynamic voltage compensation characteristics

In this case, the dynamic voltage compensation characteristic is examined by applying different input voltages within a period of 0.5 s. The designed SLSBZSI operates in the normal state from 0 to 0.2 s with a normal input voltage (V_{in}) of 375 V and generates a line to line rms voltage $V_{ab}(rms)$ of 204 V.

At time, t = 0.2 s, the input inverter voltage drops down to 50 V and continues until t = 0.3 s. To further justify the boosting effect of the designed SL-SBZSI in terms of the dynamic voltage compensation capability, a shoot-through duty ratio (D_S) of 0.2 is applied at t = 0.3 s. From Figure 14b, it can be observed that the output line voltage is successfully returned to 204 V. Hence, it can be summarized that the designed SL-SBZSI maintains the desired voltage level even for a lower input voltage while using a shoot-through duty ratio.

8. Experimental Validation

The proposed topology was also validated through experimental studies and the experimental setup is shown in Figure 15. The experimental setup looks quite similar to that as presented in [36] and the

similar parameters are used for the experiment. For this reason, the parameters of the SL-SBZSI were not listed here in order to avoid repetition. However, Figure 15 shows the experimental setup for a three-phase inverter while it is for a single-phase in [36].

Another difference is the use of a PV emulator in [36] while the same component was used here as a fixed DC supply. In this experiment, the input DC voltage was used as 50 V while the shoot-through duty ratio is considered as 0.2 in order to make the scenario consistent with the simulation result as presented in Case 1. The experiment was conducted to observe the capacitor voltage stresses, i.e., the voltages across C_1 and C_2. Figure 16 shows V_{C1} and V_{C2} which are actually the voltages across C_1 and C_2, respectively for the proposed SL-SBZSI from where it can be seen that V_{C1} = 122 V and V_{C2} = 73 V with some ripples in these voltage responses. These results matched with the simulation results and hence, it can be said that the proposed topology reduces the capacitor voltage stresses significantly. Similarly, other responses, e.g., the output voltage of the inverter is also observed but it has not been presented here as it has already been discussed in [36].

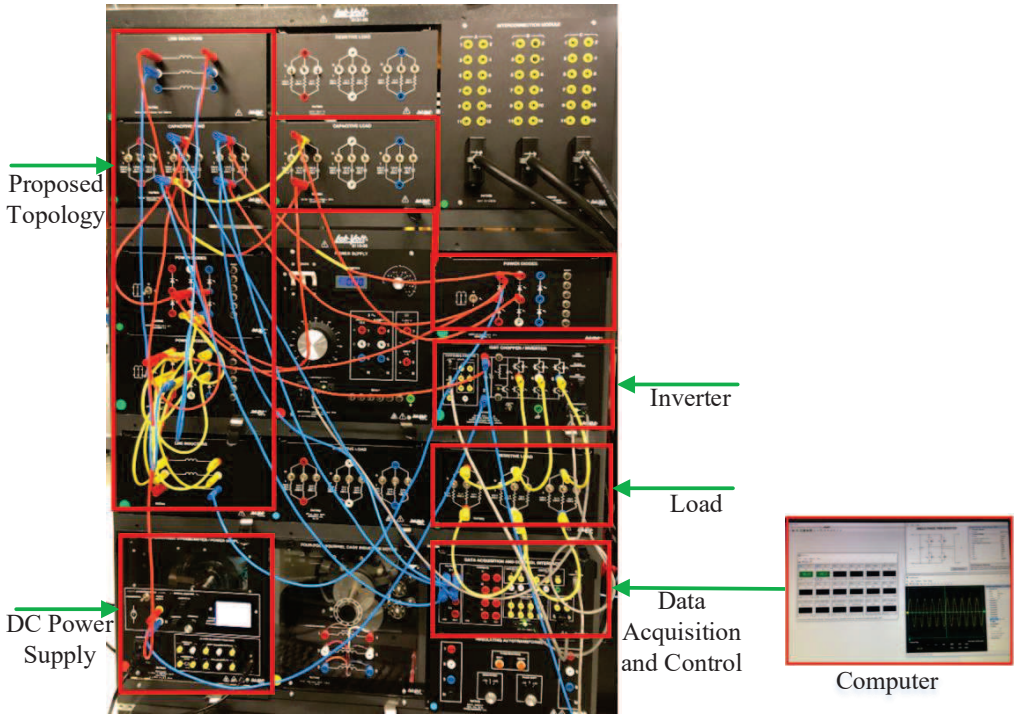


Figure 15. Experimental setup.

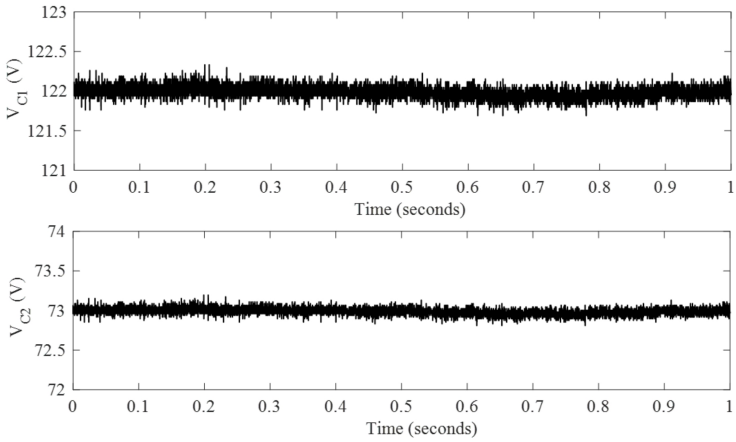


Figure 16. Proposed SL-SBZSI: capacitor voltage, V_{C1} and V_{C2}.

9. Conclusions

A switched inductor-based simple boost ZSI (SL-SBZSI) is designed, which is driven by the low shoot-through duty ratio. From both analytical and simulation results, it can be concluded that the designed SL-SBZSI guarantees reduced capacitor voltage stresses for the same boost factor and input voltage; improved efficiency; very high boosting capability for the same input voltage and shoot-through duty ratio; reduced inrush current; and significantly improved dynamic voltage compensation capabilities during the sudden changes in the input voltage. The analytical results to validate the theories and simulation results under different cases clearly demonstrate the superiority of the designed SL-SBZSI as compared to all existing topologies within the same category. Experimental results support the theoretical and simulation results which clearly indicate the practical applicability of the newly developed topology. The dynamic voltage compensation characteristics of the designed SL-SBZSI also reduces the size and cost of the system as this will help to eliminate the use of transformers. Furthermore, the dynamic compensation capability of the designed SL-SBZSI makes it suitable for the renewable energy applications where the DC voltage input to the inverter changes frequently.

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