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A New Step-Up Switched-Capacitor Voltage Balancing Converter for NPC Multilevel Inverter-Based Solar PV System

AMIR TAGHVAIE, (Student Member, IEEE), MD. ENAMUL HAQUE, (Senior Member, IEEE), SAJEEB SAHA, (Member, IEEE), AND MD. APEL MAHMUD, (Senior Member, IEEE)
School of Engineering, Deakin University, Geelong, VIC 3216, Australia
Corresponding author: Amir Taghvaie (ataghvaiegelehk@deakin.edu.au)

ABSTRACT This paper proposed a grid connected solar Photovoltaic (PV) Systems with a new voltage balancing converter suitable for Neutral-Point-Clamped (NPC) Multilevel Inverter (MLI). The switched-capacitors used in the proposed converter is able to balance the DC link capacitor voltage effectively by using proper switching states. The proposed balancing converter can be extended to any higher levels and it can boost the DC input voltage to a higher voltage levels without using any magnetic components. This feature allows the converter to operate with the boosting capability of the input voltage to the desired output voltage while ensuring the self-balancing. In this paper the proposed converter is used for a grid connected solar PV system with NPC multilevel inverter, which is controlled using vector control scheme. The proposed grid connected solar PV system with associated controllers and maximum power point tracking (MPPT) is implemented in *Matlab/SimPowerSystem* and experimentally validated using dSPACE system and designed converters. The simulation and experimental results show that the proposed topology can effectively balance the DC link voltage, extract maximum power from PV module and inject power to the grid under varying solar irradiances with very good steady state and dynamic performances.

INDEX TERMS Solar photovoltaics, NPC multilevel inverter, balancing circuit, dc-link voltage balancing, grid connected PV system.

I. INTRODUCTION

Multilevel inverters (MLIs) are broadly used for the grid integration of solar photovoltaic (PV) systems due to several advantages such as lower harmonic distortions, less electro-magnetic interference (EMI), less standing voltage on semi-conductors, high output waveform quality and smaller filter size [1], [2]. Three principal types for MLIs are Cascaded H-Bridge (CHB), Neutral-Point-Clamped (NPC), and Flying Capacitors (FC) [3]. These MLIs have several drawbacks and limitations such as: 1) CHB converters require large number of separate input DC-link sources [4], 2) FC MLIs have both balancing and large number of capacitors problems in high output voltage levels [5], and 3) NPC MLIs also require separate DC source and have balancing problems due to the use of capacitors which necessitate an additional balancing circuit [6].

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The Neutral-Point-Clamped Multilevel Inverter (NPC-MLI) is initially suggested by Nabae in 1981 [7] which has numerous applications such as electric motor drives [8], grid integration of renewable energy sources (PV, fuel cell, and wind turbine) [9], [10] and utility applications [11], [12]. The main drawback of this type of converter is capacitor voltage balancing at the input of MLI in solar PV system which causes problems with the grid connected solar PV system [13]. In the existing literature, several methods have been suggested to solve the problem of capacitor voltage balancing of NPC-MLIs [14]. The adjacent switching technique is used in [15] to balance the capacitors' voltage where redundant states are used for voltage balancing and maintaining the output voltage at the acceptable range. However, the external circuit used to balance the capacitors' voltage increases the inductor size at higher voltage levels which introduces challenges in implementation. A voltage balancing technique for DC-link capacitors in parallel three-phase and single-phase NPC MLIs is presented in [16]. In this method, the voltage

balancing capability is achieved where NPC-MLIs are connected in parallel. In this system, at least one of the inverters generates opposite voltage which limits the output voltage levels and increases the number of power semiconductors in higher voltage levels. A carrier-based pulsed-width modulation (CB-PWM) using zero-sequence voltage injection proposed in [17]. The switching frequency under this method is low and can balance the capacitors' voltage without using any extra control. However, this method above mentioned methods are computationally intensive. Another DC-link voltage balancing method is proposed in [18]. This method uses a passive RLC circuit which requires magnetic elements. Some topologies are suggested in [19]–[22] for the balancing capacitors' voltage at higher voltage levels, which are derived from 3L NPC. Although these topologies can be used for more than two level; however, they have difficulties for balancing capacitors in more than five voltage levels. It is worth mentioning that in NPC-MLIs, the series connection of the DC-link capacitors is used to charge the capacitors through the PV unit in order to produce high voltage levels at the output. However, these converters with series capacitors are more vulnerable to capacitors unbalancing and voltage dynamics instability as compared to the converters using capacitors in parallel.

Another concern in NPC-MLIs is voltage boosting incapability which causes the use of massive magnetic components. This condition is dealt using DC-DC boost converter. A multi-output boost (MOB) DC-DC converter is suggested in [19] as an additional circuit to balance the DC-link capacitors while boosting the voltage. A new power conversion system for wind turbine application is proposed and validated in [20], [21]. In this system a four-level boost converter has been proposed as an alternative to the traditional DC-DC boost converters. Another boost-type grid-connected inverters are proposed in [22], [23] where magnetic elements are used to boost the input voltage to its chosen value at the output. However, in these topologies, the drawback is using magnetic elements at the input, which increase size, volume and complexity, and reduces the efficiency of the system. In this paper:

- A new step-up switched capacitor voltage balancing converter for NPC multilevel converter based solar PV system is proposed. The proposed converter is able to balance the DC link capacitor voltage effectively by using proper switching states.
- The proposed topology can boost the input DC voltage at the desired output voltage level without using any magnetic elements. It also requires only one DC source or PV array output to produce multi-level output, which reduces the number of input voltage sources required in such system. The proposed topology is cost effective than the traditional dc-dc converter and produce better output.
- The proposed grid connected solar PV system with associated controllers is implemented in Matlab/SimPowerSystem and experimentally validated using dSPACE DSP (digital signal processor) system and designed converters. Results confirms that the proposed topology can effectively balance the DC link voltage, extract maximum power from PV module and inject power to the grid effectively.

The proposed system structure with balancing converter is presented in Section II along with its building block. The operating principle of the proposed converter is discussed in Section III while section IV includes the switching and control strategies. The calculation of power losses along with the values of capacitors and the circuit extension are presented in section VII. Section VI presents a comparative analysis of the proposed scheme with traditional DC-DC boost converter. Simulation and experimental results are presented in Sections VII and VIII. Finally, the paper is concluded in Section IX.

II. SYSTEM STRUCTURE

The proposed grid connected solar PV System with a new voltage balancing converter is presented in Fig1, which include (i) PV array, (ii) proposed step-up converter for balancing the capacitors' voltage, (iii) a three-phase seven-level NPC MLI along with its controllers (iv) LC filter to improve total harmonic distortion (THD) and converting the staircase voltage to a near sinusoidal waveform by reducing the THD, (iv) grid interface transformer and (v) power grid.

The PV array output is fed to the proposed step-up voltage balancing converter. The output voltage of proposed converter is 3 times the input PV voltage, which is the input to the 7 level NPC MLI. The inverter is controlled using vector control scheme. The incremental conductance based maximum power point tracking algorithm is used for the system. The output of the MPPT controller provides the DC link voltage reference. The output of the DC link voltage controller provides the d-axis current reference. The q-axis current reference is calculated from the reactive power requirement and d-axis grid voltage. The active/reactive power flow into the grid is controlled by controlling d-axis and q-axis currents, respectively.

III. PROPOSED STEP-UP BALANCING CONVERTER

Fig. 2 shows the proposed step-up balancing converter [24]. The proposed converter comprises of five power switches and two diodes which are designed in such a way that input DC source can be connected in parallel with each capacitor during charging states. Simultaneously, the higher efficiency is achieved by discharging the capacitors at the load. It is essential to select appropriate switching states for charging all capacitors equal to the input DC voltage while the boosted output voltage can be achieved by series connections of all capacitors. Table 1 shows the switching states for the proposed converter.

Fig. 3 shows the proposed step-up balancing converter connected to a four-level (three positive and one zero) NPC-MLI. By adding three-phase NPC-MLI (as shown in Fig. 4), seven-level can be achieved (three positive, three negative and one zero). From a four-level NPC-MLI as shown in Fig. 3 (a),

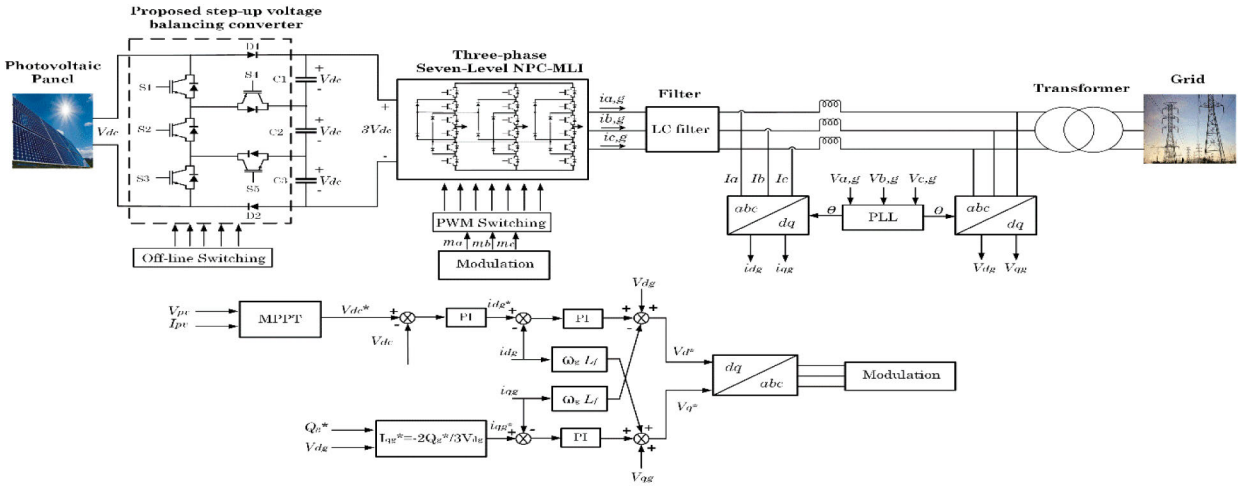


FIGURE 1. The Grid-connected PV system of the proposed step-up voltage balancing converter and seven-level NPC-ML.

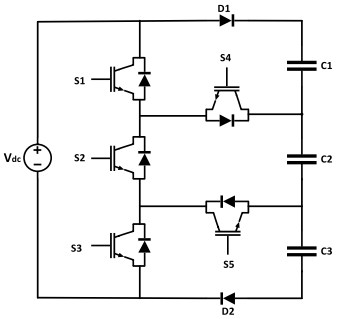
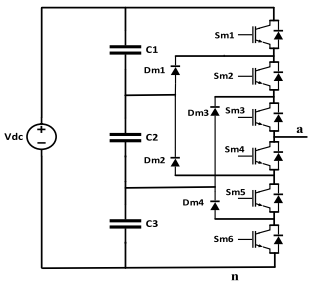


FIGURE 2. Proposed voltage balancing converter.

TABLE 1. Switching states for the proposed balancing converter.

Charging capacitor	On state switches	Conducting diodes
C_1	S_2, S_3, S_4	D_1
C_2	S_1, S_3	-
C_3	S_1, S_2	D_2

it can be seen that capacitors need to be charged their maximum values, which is equal to the input DC voltage, ($1V_{dc}$). Moreover, during the charging states, the sum of the capacitors (series connection) are connected in parallel with input DC source which affects the dynamic performance of the capacitors and causes voltage difference across each capacitor. Therefore, an appropriate converter needs to be proposed to not only boost the input DC voltage to a desired output voltage but also to charge each capacitor in parallel with input DC voltage. The voltage balancing and boosting can be achieved by connecting the proposed balancing network with the NPC converter as shown in Fig. 3 (b). Figures 4 (a-d) show the potential switching states for the proposed converter which is connected to a seven-level NPC-MLI. It is clear that a three-phase NPC-MLI has been considered to investigate the potential switching states (three levels for the positive states and one level for zero state) [24].



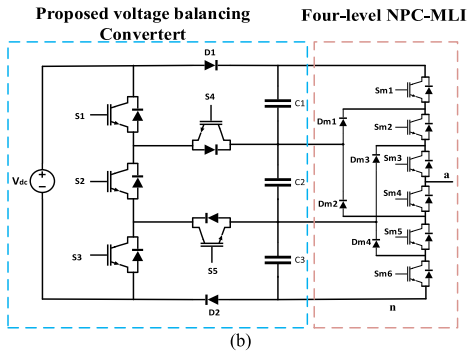


FIGURE 3. (a) Conventional 4-level NPC converter (b) Proposed voltage balancing converter connected to the four-level NPC-MLI.

From Fig.4, it is clear that the green color demonstrates the charging route, blue color displays discharging route and red color displays the capacitors which are charging and discharging at the same time. Moreover, Fig. 4 (a) displays $V_{ab} = 0$ state. It is worth mentioning that each capacitor is able to be charged one time more than other capacitors. Selecting which capacitor needs to be charged one more time depends on the balancing conditions of the capacitors (at this point C_3 is chosen). In Fig. 4 (b), the terminal voltage between a and b is $+1V_{dc}$ whereas capacitor C_3 is charging, simultaneously. The terminal voltage across points ab equals

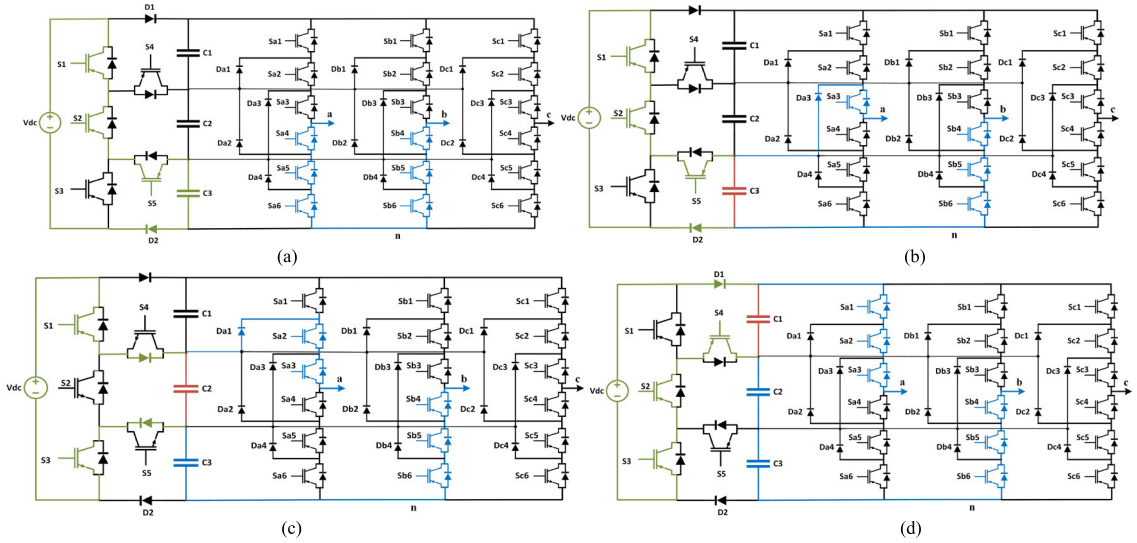


FIGURE 4. (a) Charging state of C_3 and $V_{ab} = 0$ (b) charging state of C_3 and $V_{ab} = 1V_{dc}$ (c) charging state of C_2 and $V_{ab} = 2V_{dc}$ (d) charging state of C_1 and $V_{ab} = +3V_{dc}$.

to $V_{ab} = +2V_{dc}$ which representing capacitor C_2 is charging (Fig. 4 (c)). Capacitor C_1 charging state as well as output voltage terminal value of $+3V_{dc}$ is also shown in Fig. 4 (d). It is worth mentioning that for saving space, only positive states and zero state of phase a and b are explained.

From Fig. 4, it is clear that all of the capacitors are located between the voltage balancing converter and the three-phase NPC MLI which can produce multilevel at the output by using only a simple control strategy. The control strategy for the grid side inverter and modulation strategy are presented in the following sub-sections.

IV. DESIGN AND CONTROL OF GRID SIDE INVETER

A. CONTROL STRATEGY

The control structure of grid side multilevel inverter is shown in Fig.1, The vector control technique is used for the grid connected converter which consists of a dc link voltage controller which provides the reference d-axis current. The d- and q-axis currents are controlled to control active and reactive power flow to the grid.

The active and reactive power supplied to the grid can be obtained as follow:

$$P_g = 3V_g \cdot I_g \cos\phi_g \tag{1}$$

$$Q_g = 3V_g \cdot I_g \sin\phi_g \tag{2}$$

where V_g, I_g, and φ_g are the rms phase voltage, rms current, and power factor angle of the grid, respectively. For the inverter in the grid-connected PV system, the carrier-based PWM strategy is used as described in the next part.

The voltages of d-axis and q-axis are as follow [25]:

$$V_{dg} = V_{d1} - R_f i_{dg} - L_f \frac{di_{dg}}{dt} + \omega L_f i_{qg} \tag{3}$$

$$V_{qg} = V_{q1} - R_f i_{qg} - L_f \frac{di_{qg}}{dt} - \omega L_f i_{dg} \tag{4}$$

The inverter output voltage amplitude is given by

$$|V_g| = \sqrt{(V_{dg})^2 + (V_{qg})^2} \tag{5}$$

In dq reference frame, the active and reactive powers are given by

$$P_g = \frac{3}{2}\left(V_{dg} i_{dg} + V_{qg} i_{qg}\right) \tag{6}$$

$$Q_g = \frac{3}{2}\left(V_{dg} i_{qg} + V_{qg} i_{dg}\right) \tag{7}$$

If the voltage vector is aligned with d-axis, $v_{qg} = 0$ and $v_{dg} = |V_g|$, the active and reactive power can be given as,

$$P_g = \frac{3}{2}\left(V_{dg} i_{dg}\right) = \frac{3}{2}|V_g| i_{dg} \tag{8}$$

$$Q_g = \frac{3}{2}\left(V_{dg} i_{qg}\right) = \frac{3}{2}|V_g| i_{qg} \tag{9}$$

Equations (10 and (11) show that by controlling the d-axis and q-axis currents, we can simply regulate the active and reactive powers. The q-axis current reference i_{qg}^* can be achieved from

$$i_{qg}^* = -\frac{2}{3}\frac{Q_g^*}{V_{dg}} \tag{10}$$

where, Q_g^* is the required reactive power

B. MODULATION TECHNIQUE

A carrier-based (CB) PWM scheme is chosen to achieve an output voltage with seven-levels using the proper switching frequency. The CB-PWM method is simple and easy to expand with less computation efforts as compared to other schemes such as Space Vector PWM (SVPWM) [26]. Six carrier waveforms (triangular) and a reference voltage is shown in Fig.5 and these are compared together for generating switching pulses to obtain a seven-level output voltage.

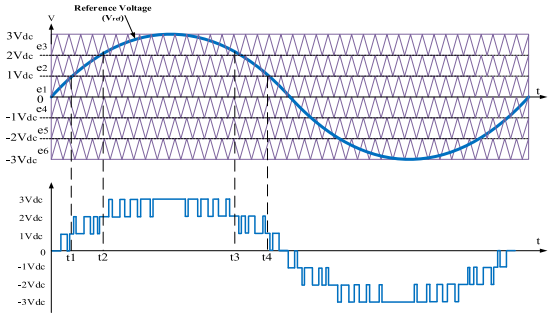


FIGURE 5. Carrier-based modulation technique and the output voltage.

As shown in Fig.5, three carrier waveforms (e_1, e_2 and e_3) are for the positive half-cycle and another three (e_4, e_5 and e_6) are for the negative half-cycle. The offline switching strategy as shown in Table 1 is used for the proposed step-up voltage balancing converter where switches S_1 and S_2 are ON for $0<t<t_1$; S1 and S_3 for the period $t_1 <t<t_2$; and S_2, S_3 and S_4 are for $t_2 <t<t_3$.

The waveform of staircase output voltage is composed of seven voltage levels with a peak value of $3V_{DC}$ [27]. The n^{th}-order harmonic rms voltage is normalized with respect to the total DC voltage:

$$E = \frac{m-1}{2} V_{DC} \tag{11}$$

At $ma = 1$, the rms fundamental line-to-line voltage is:

$$V_{(AB,LL)} = 0.612\,(m-1)\,E \tag{12}$$

It is worth mentioning that the staircase output voltage is composed of three, five, and seven voltage levels:

$$\left\{\begin{array}{ll} 0 < m_a < 0.33 & \text{outputlevels} = 3 \\ 0.33 < m_a < 0.74 & \text{outputlevels} = 5 \\ 0.74 < m_a < 1 & \text{outputlevels} = 7 \end{array}\right\} \tag{13}$$

V. CALCULATION OF POWER LOSS AND CAPACITANCE

The power loss within the converter along with the calculation of the capacitors and the extension of the proposed topology are discussed in the following sub-sections.

A. CALCULATION OF POWER LOSSES

The power losses within the proposed configurations are mainly due to the switching and conduction losses. The calculations of switching loss (P_{sw}) and conduction loss (P_{cond}) are shown in the following.

1) SWITCHING LOSSES

There are switching losses due to the turn ON and OFF actions of switching devices. The voltage and current are not completely zero during the changes in switching states. Therefore, there are losses due to these switching dynamics which can be calculated by following equation [24]:

$$\begin{aligned} P_{sw,i(ON)} &= f_s \int_0^{t_{on}} V_{off-state,i}\,(t)\,.i\,(t)\,dt \\ &= \frac{1}{6} f_s V_{off-state,i} I_{on-state1,i} t_{on} \end{aligned} \tag{14}$$

$$\begin{aligned} P_{sw,i(OFF)} &= f_s \int_0^{t_{off}} V_{off-state,i}\,(t)\,.i\,(t)\,dt \\ &= \frac{1}{6} f_s V_{off-state,i} I_{on-state2,i} t_{off} \end{aligned} \tag{15}$$

where $V_{off-state,i}$ is the voltage in off-state of i^{th} switch, $I_{on-state1,i}$ is the current when the switch becomes completely turned on for i^{th} switch, and $I_{on-state2,i}$ is the current switch before the turn-off of the i^{th} switch. Hence, the overall switching losses can be calculated using the equation below:

$$P_{sw,total} = \sum_{i=1}^{N_{switch}} \left(\sum_{j=1}^{N_{on(i)}} P_{sw,on(ij)} + \sum_{i=1}^{N_{off(i)}} P_{sw,off(ij)} \right) \tag{16}$$

where $N_{on(i)}$ and $N_{off(j)}$ are the number of turning ON and OFF during a period while N switch is the number of switches.

2) CONDUCTION LOSSES

There are on-state resistors and forward voltages during the conduction of the switches or diodes. In this condition, there will be conduction losses in power semiconductors which can be calculated by using the following equation:

$$\begin{aligned} P_{cond,level,i} &= P_{cond,sw,level,i} + P_{cond,D,level,i} \\ &= K_1 \left(V_{on,sw} i_{avg,level,i} + R_{on,sw} i^2_{rms,level,i} \right) \\ &\quad + K_2 \left(V_{on,D} i_{avg,level,i} + R_{on,D} i^2_{rms,level,i} \right) \end{aligned} \tag{17}$$

where $P_{con,sw,leveli}$ and $P_{con,D,leveli}$ are the conduction losses of power switches and diodes at i^{th} level, respectively, $i_{rms,level,i}$, $i_{avg,level,i}$ are the rms and average current of i^{th} voltage level and $V_{on,sw}$ and $V_{on,D}$ are the on-state voltages of power switches and diodes. Respectively. The coefficients K_1 is the number of power switches and K_2 is the number of diodes in different voltage levels.

B. CALCULATION OF CAPACITANCE

It is essential to calculate the values of capacitors used in the proposed configuration. For this purpose, the discharging time (t_1, t_2, t_3 and t_4) needs to be calculated and for the proposed, seven-level MLI; t_1, t_2, t_3, and t_4 can be calculated as follows [4]:

$$\begin{aligned} t_1 &= \frac{\sin^{-1}\left(\frac{1}{3}\right)}{2\pi f_{ref}}; \quad t_2 = \frac{\sin^{-1}\left(\frac{2}{3}\right)}{2\pi f_{ref}}; \\ t_3 &= \frac{\pi - \sin^{-1}\left(\frac{1}{3}\right)}{2\pi f_{ref}}; \quad t_4 = \frac{\pi - \sin^{-1}\left(\frac{2}{3}\right)}{2\pi f_{ref}} \end{aligned} \tag{18}$$

The capacitance can be calculated by considering the worst (longest) time when a capacitor is discharging within the proposed MLI as shown in Fig. 6.

If $(t_{a,j}, t_{b,j})$ is considered as the longest discharging time of capacitor j^{th}, the maximum discharge amount can be found as:

$$Q_{C_j} = \int_{t_{b,j}}^{t_{a,j}} I_{load}.\,\sin\left(2\pi f_{ref} t\right) dt \tag{19}$$

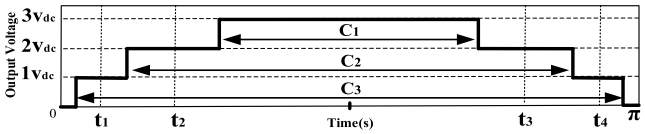


FIGURE 6. The longest discharging time for capacitors.

where I_{load} is the output current. Therefore, the capacitor value can be computed from the following equation:

$$C_j > \frac{Q_{C_j}}{\Delta V_{Cj}} \tag{20}$$

where ΔV_{Cj} is the j^{th} capacitor's voltage ripple. In the proposed switched-capacitors converter, where the capacitors are connected in parallel with PV cell, the performance of the system is significantly dependent on the voltage ripple magnitude of the capacitors and utilization of the capacitances to provide the boosted voltage. Hence, it is required to reduce the effects of the voltage ripple to the output voltage of the NPC-MLI. In this case, the capacitances are sized such that the capacitors' ripple is restricted in a certain percentage of the output voltage. If we consider the maximum ripple factor α_{rip} as follow [28]:

$$\alpha_{rip} = \frac{1}{V_p} \sum_{j=1}^{m} \Delta V_{Cj} \tag{21}$$

Thus the minimum required capacitor value is as follow:

$$C_{\min} = \frac{I_o}{2\pi f \alpha_{rip} V_p} \sum_{j=1}^{m} \theta_j \tag{22}$$

where V_p is the maximum voltage and θ_j is the firing angel of j^{th} capacitors related to times t_1, t_2, etc. By replacing the output power and capacitive energy into equation (22), the capacitive energy storage (E_c) per unit output power P_{out} can be achieved from the following equation:

$$\frac{E_c}{P_{out}} = \frac{\sum_{j=1}^{m} \left(\frac{V_{Cj}}{V_p}\right)^2}{2\pi f \alpha_{rip}} \sum_{j=1}^{m} \theta_j \tag{23}$$

From the equation, it is quite clear that both capacitive energy and the operating frequency are a function of capacitors' firing angels as well as the charging voltage of the capacitors. Meanwhile, the conversion ratio of the proposed converter is affected by the capacitors, the efficacy of storage utilization can be proved by the required capacitive energy per unit output power at the fundamental frequency and specific voltage ratio.

C. EXTENSION OF THE PROPOSED BALANCING CONVERTER

As stated earlier, the proposed voltage balancing converter is scalable and easily can be extended to use in high voltage levels as shown in Fig. 7. In this paper, a generalized topology has been proposed for high voltage levels in order to improve the quality of the output voltage waveform. For an example, Fig.7 shows the proposed converter with 11 voltage levels.

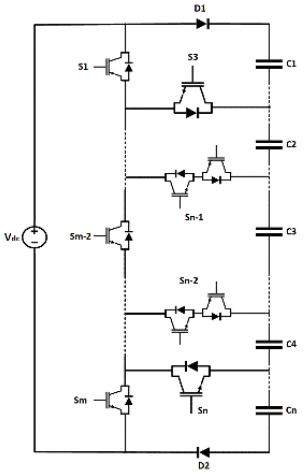


FIGURE 7. Extension of the proposed step-up voltage balancing converter.

It is worth noting that increasing the number of levels can improve the quality of the output voltage. The required capacitance to restrict the voltage ripple across the capacitors for a given carrier frequency can be achieved as the following equation:

$$C_j = \frac{I_{peak}}{\Delta V_{Cj}} \frac{1}{f_c} \tag{24}$$

where I_{peak}, ΔV_{Cj} and f_c are the peak phase current, the j^{th} capacitor's voltage ripple and the carrier frequency, respectively. The energy stored in the DC-link capacitors for one phase of n-level converter can be obtained from the following equation [29]:

$$E_c = \frac{1}{2} C_j \sum_{i=1}^{\frac{n-3}{2}} \left(\frac{i}{\frac{1}{2}(n-1)} V_{dc} \right)^2 \tag{25}$$

where n is the number of output voltage level. In order to achieve the required energy storage versus increasing the number of levels, the energy storage equation must be normalized which can be calculated as follow:

$$E_{c-normalized} = \frac{E_c}{\frac{1}{2} C_j V_{dc}^2} = \sum_{i=1}^{\frac{n-3}{2}} \left(\frac{i}{\frac{1}{2}(n-1)} \right)^2 \tag{26}$$

From Fig. 8, it is clear that the stored energy is linearly increasing when the number of levels increases. Moreover, the voltage stress on the power switches will be almost constant by increasing the number of levels which especially enables the switches to work under higher frequency and making the proposed converter useful at higher voltage levels.

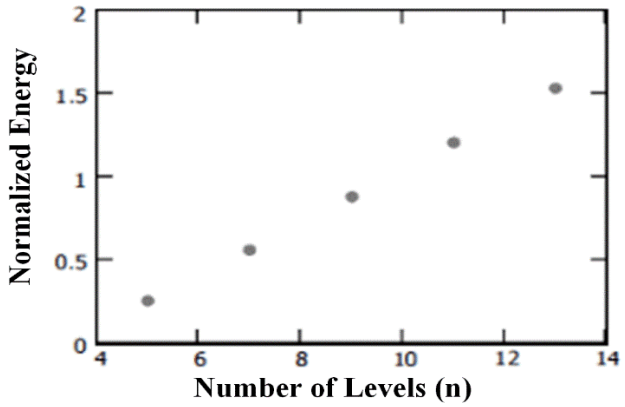


FIGURE 8. Normalized capacitors energy stored versus number of levels.

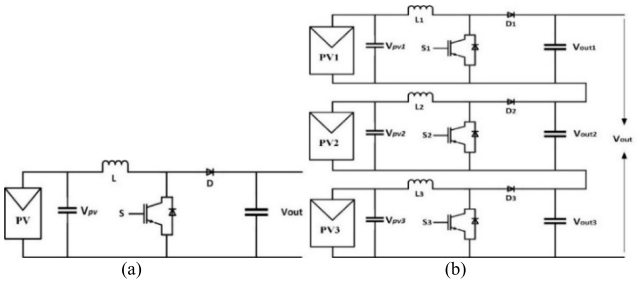


FIGURE 9. (a) Traditional DC-DC boost converter (b) seven-level DC-DC boost converter.

VI. COMPARISON WITH CONVENTIONAL DC-DC CONVERTERS

This section presents a comparative study of the proposed step-up voltage balancing converter with traditional DC-DC converters and other topologies. Fig 9 shows two DC-DC converters which are considered for comparison. Fig 9(a) shows a traditional boost DC-DC converter which include a DC source, an inductor, a power switch, and a power diode. Fig. 9(b) shows a seven-level DC-DC converter which produces three times of input voltage at the output. This converter requires higher number of components compared to a sing boost DC-DC converter. The cost factor is another important factor while comparing the proposed step-up converter with other DC-DC converters. For this purpose, the specifications for the output resistive load = 50 Ω, the switching frequency = 5 KHZ, losses = 5%, and efficiency of 90% are used in order to achieve a precise cost comparison. Three different scenarios are defined as presented in Table 2 are considered for the cost comparison. According to this table, the rating of switches changes with the increases in the input voltage. For example, a 100 volts switch is required (IRF530) for a 50 volts input voltage and 50% margin for the switch selection.

Another point needs to be noted that all converters (i.e., the proposed and conventional) use only one DC input sources which is an indication of the cost-effectiveness. However, the proposed step-up converter is more cost-effective as it generates seven-level at the output with the improved power

TABLE 2. Different scenarios used for comparison.

Scenarios	Input DC voltage (volts)	Type of switches (MOSFETs)	Type of diodes
1	20	ZXMC4A16DN8 (40 volts, 5A)	RBR5LAM40ATF (40 volts, 5A)
2	50	IRF530 (100 volts, 14A)	MBR30H100PT (100 volts, 15A)
3	100	IRFP250MPBF (200 volts, 30A)	RURP3020 (200 volts, 30A)

quality while the usual DC-DC converter generates only one level with the low quality output waveform. Hence, the conventional converters require larger filters which further increases the cost. For the seven-level DC-DC converter, three input DC sources need to used and three solar PV units are required during the practical implementation of such converters. For instance, a 24 V and 160 W PV is required for the first scenario (V_{dc} =20 V) and the price of such a panel is approximately $160. Whilst for the seven-level DC-DC converter needs three of this PV and it should multiplied by 3, but the proposed step-up is a single DC source converter and only require one of such DC source. The other priority of the proposed structure is that it is an inductor less converter whereas the usual DC-DC uses an inductor at the input which increases the cost. Traditionally, for a boost converter, the inductor value can be selected through the inductor current ripple. The average input current of the inductor can be calculated as follow:

$$I_{L(DC-MAX)} = \frac{V_{out} \times I_{out(MAX)}}{V_{dc} \times \eta} \tag{27}$$

where V_{out} is the output voltage of the boost converter, $I_{out(MAX)}$ is the maximum output current, V_{dc} is the input DC voltage value and η is the efficiency. Therefore, the inductance can be calculated as:

$$L = D \times \frac{V_{dc}}{\Delta I_{L(p-p)} \times f_{sw}} \tag{28}$$

where D is the duty cycle, $\Delta I_{L(p-p)}$ is the inductor current ripple and f_{sw} is the switching frequency. It is suggested that $\Delta I_{L(p-p)}$ should be 30% of $I_{L(DC-MAX)}$. According to the calculation, the inductance for the usual DC-DC boost converter for all scenarios become 2.398 mH. According to the commercial values (1 mH, 1.5 mH, 2.2 mH, 3.3 mH, 4.7 mH, and so on), the nearest value to the calculated inductor is chosen which is 3.3 mH. The average input current of the inductor, the type, and price of the selected inductor are shown in Table 3.

From Table 3, it can be seen that the proposed step-up converter can be designed with lower costs than other conventional DC-DC boost converters due to the reduced number of input sources and elimination of magnetic components (inductor).

Table 4 shows the comparisons of the proposed converter with other topologies proposed in [15], [20] as well as the

TABLE 3. Inductance specification of usual DC-DC boost converter.

Scenarios	Calculated inductance (mH)	$I_{L(DC-MAX)}$ (ampere)	Selected nductance (mH)	Type of inductance (choke)	Price ($)
1	2.398	3.61	3.3	B82724J24 02N001	5.02
2	2.398	9.025	3.3	B82725S21 03N004	16.01
3	2.398	18.05	3.3	B82727E62 23A040	20.46

TABLE 4. Comparison of the proposed step-up balancing converter with other conventional DC-DC converters.

	Traditional DC-DC	seven-level DC-DC	[15]	[20]	Proposed
Number of levels	1	4	4	4	4
Number of PV sources	1	3	1	1	1
Number of DC-link capacitors	1	3	3	3	3
Number of switches	1	3	3	3	5
Number of diodes	1	3	3	4	2
Number of inductors	1	3	1	1	NA
Balancing capability	NO	NO	YES	YES	YES

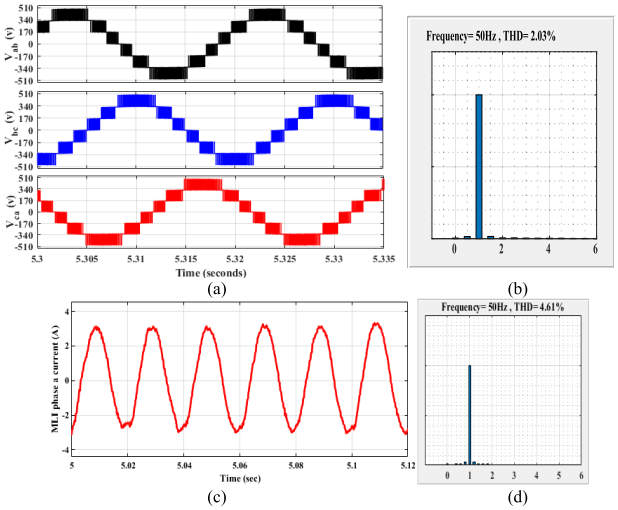


FIGURE 10. Simulation results for (a) output voltage of NPC-MLI (b) voltage THD (c) output current of NPC-MLI and (d) current THD.

conventional and seven-level DC-DC converter (shown in Fig. 9) in terms of the number of devices and voltage balancing capability. According to this table, all of the converters produce four-level (three positive and one zero) except the traditional DC-DC which only produce one level (V_{dc}). It is clear from the table that the proposed converter has two more switches than others; however, in the proposed converters in [15], [20] and the seven-level DC-DC converter, inductors has been used to step-up the input voltage to $3V_{dc}$. Because the capacitors of the proposed converters in [15], [20] charge by the input DC voltage has the value of $V_{dc}/3$, an inductor needs to be used to boost the voltage up to $3V_{dc}$. In the seven-level DC-DC converter, the capacitors require a separate inductor to boost the input DC voltage. However, in the proposed converter, the capacitors are charging in parallel with the input DC voltage source and are charging up to $1V_{dc}$ for each, and total $3V_{dc}$, without using any magnetic elements.

VII. SIMULATION RESULTS

This section presents a thorough validation of the proposed converter in interfacing solar PV system with the utility grid through a comprehensive simulation study using *MATLAB/SimpowerSystem* toolbox. This simulation studies a grid connected 1.14 kw solar PV system using the proposed converter topology. This simulation study thoroughly investigates the effectiveness of the proposed converter topology in harvesting maximum possible solar power under varying irradiation condition. The incremental conductance MPPT algorithm along with vector control approach have been considered in this simulation study to facilitate harvest of maximum solar power transfer to the grid. The other relevant parameters of the simulation study are as follows: PV module: BIPV BIPV054-T86, 28.8V voltage at maximum power point (V_{MPP}), 6.6A MPP current (I_{MPP}), string comprising 6 modules and the whole PV array includes 1 string with MPP power of 1.14kW at 172.8 V, switching frequency: 5 kHz, the sampling time is 50μs, output frequency: 50 Hz, capacitor value: of 4700 μf, output filter with L= 12 mH and C = 2.5 μf. In the simulation study, the irradiations are varied (at room temperature) as follows (refer to Fig. 16. (a)): 200 W/m^2 (0<t<1.2s), 400 W/m^2 (1.2s<t<2.4s), 600 W/m^2 (2.4s<t<3.6s), 800 W/m^2 (3.6s< t<4.8), 1000 W/m^2 (4.8s<t<6s), 800 W/m^2 (6s<t<7.2s), 600 W/m^2 (7.2s<t< 8.4s), 400 W/m^2 (8.4s<t<9.6s), 200 W/m^2 (9.6s<t<10s).

The responses of the simulation study are presented in Fig. 10-16. The voltage balancing capability of the proposed converter is demonstrated through the balanced output voltage (equal in magnitude and 120° phase shifts) of three-phase NPC-MLI in Fig. 10 (a) (for time 6s<t<7.2s). It can be seen from the figure that each phase voltages has three-levels in both positive and negative half-cycles, as well as one zero level that is seven levels in total. It is worth mentioning that each level of the inverter output voltage is following the required MPPT voltage corresponding to the irradiance. The phase *a* current of the MLI has been presented in Fig. 10 (c). In terms of reduction in harmonics in the proposed converter it can be seen from Fig. 10 (b) and Fig. 10 (d) that THD is quite low (2.03% and 4.61% for voltage and current, respectively). The PV array voltage and current as well as DC link capacitor voltages are shown in Fig. 11 (a), (b) and (c), respectively. It can be seen from Fig. 11 (a) that at different irradiance, the PV voltage for maximum power point is different and the reference and measured PV voltage is changing. In other words, the PV array voltage tracks the required MPPT voltage with the varying irradiance, and hence ensure harvesting of maximum possible solar power which validate the system thoroughly. The voltage and current responses of the switches S_1, S_2, and S_3 in the proposed voltage balancing

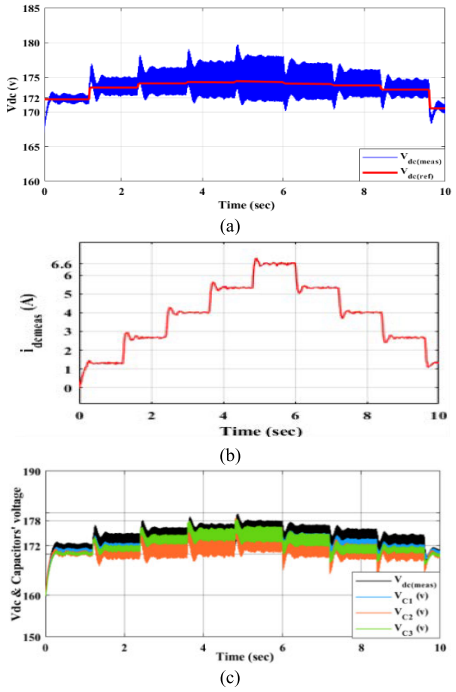


FIGURE 11. Simulation results for (a) PV reference and measured voltage (b) PV's measured current and (c) measured voltage of PV and capacitors' voltages.

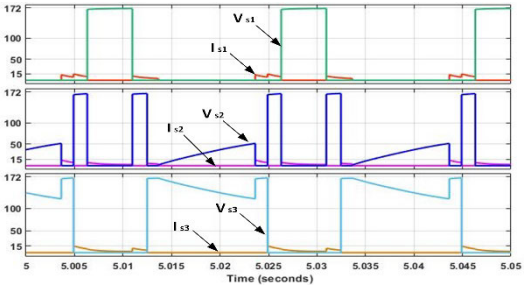


FIGURE 12. Voltage (volt) and current (ampere) of S_1, S_2 and S_3.

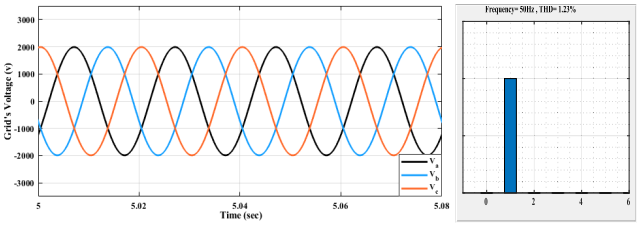


FIGURE 13. Simulation results for (a) grid voltage in 1000 w/m^2 irradiances and (b) its FFT analysis.

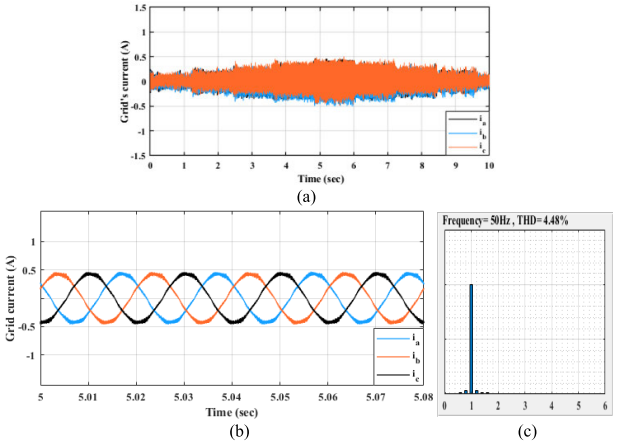


FIGURE 14. Simulation results (a) Grid current in different irradiances (b) Grid current in 1000 w/m^2 irradiance and (c) its THD performance.

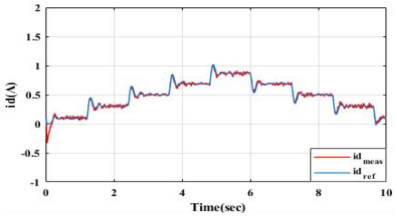


FIGURE 15. Simulation results for d-axis current under varying irradiations.

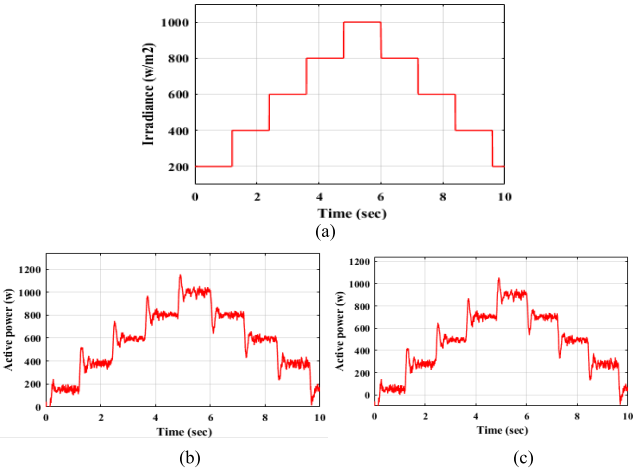


FIGURE 16. Simulation results (a) Irradiance changes (b) power transfer to grid at temperature 25°c under varying irradiation and (c) power transfer to grid at temperature 45°c under varying irradiation.

converter are shown in Fig. 12. It can be seen from the figure that voltage stresses on all the semiconductors are equal to voltage of the PV module at any instant. It is worth noting that in all switched-capacitors converters, the PV array and the DC link capacitors are required to be connected in parallel to ensure charging of the capacitors, which may cause high current spike that can potentially damage the switches. The proposed converter includes a small series resistance of appropriate size (as small as 300 mΩ) with the PV array to overcome this issue and minimized the current spike which is validated by showing the current waveforms of switches S_1, S_2 and S_3 in Fig. 12.

Three-phase grid voltage and current are shown in Fig. 13 and Fig. 14, respectively, which clearly validates the efficacy of the proposed converter, i.e., the voltage balancing and

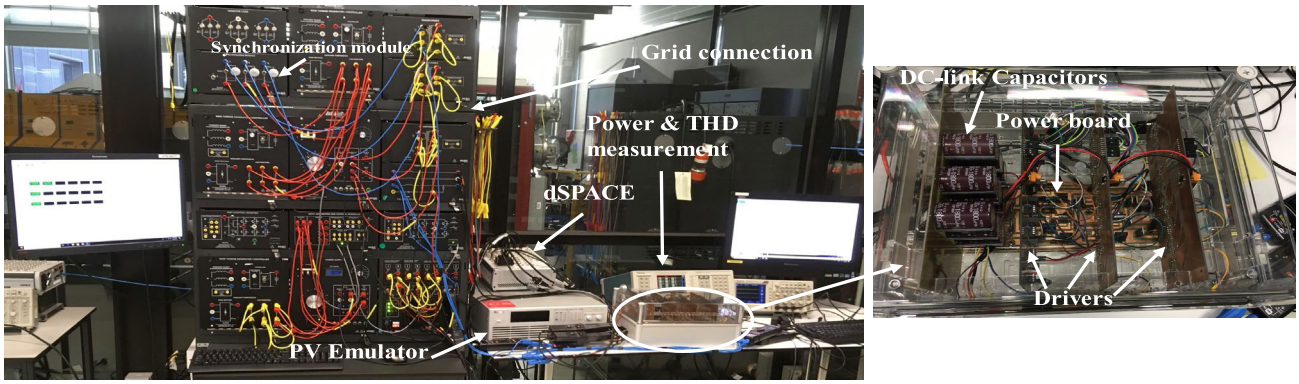


FIGURE 17. Laboratory experiments set-up (a) the whole System and (b) proposed converter with three-phase NPC-MLI.

boosting with the improved power quality in grid connected operation. It can be seen from the current response that the ac current flowing to the grid is varying in correspondence to different irradiation level and ensure export of maximum possible solar power (as shown in Fig. 16 (a)) under varying weather condition.

Fig. 15 shows the tracking of d-axis current, which illustrates that the current is accurately following its required reference value to ensure transfer of maximum solar power to the grid under varying weather condition. Furthermore, Fig. 16 shows the transfer of power to the grid (Fig. 16(b) at 25° and Fig. 16(c) at 45°) following the variation in irradiation (Fig. 16 (a)) and temperature.

VIII. EXPERIMENTAL RESULTS

In order to further evaluate effectiveness of the proposed converter in interfacing a solar PV system to the utility grid, this section demonstrates experimental validation of the proposed converter. Fig. 17 shows the experimental setup of a grid integrated solar PV system using proposed converter. The associated control operations of the PV system have been carried out using dSPACE-SY1202TP. In the experimental study, incremental conductance MPPT algorithm is used to ensure maximum solar power extraction, while vector control approach has been adopted to ensure seamless maximum possible power transfer to the grid. The solar PV array in the experimental study has been emulated using PV emulator: Chroma 62050H-600s with MPP power of 31.72W with voltage and current at the MPP are 48.8V and 0.65A, respectively. Other relevant parameters of the experimental study are switching frequency: 5 kHz, the sampling frequency is 10KHZ (the sampling time is 100μs), grid frequency: 50 Hz, capacitor value: of 4700 μf, output filter with L= 8 mH and C=1.5 μf, IGBT type G4PH40KD, Diode type RHR15120, Switches driver & optocoupler HCPL-3120 and Buffer SN74HC244N.

For the protection of the system, a circuit breaker has been used in the AC side when connecting to the grid using synchronizing module. The Synchronizing module has

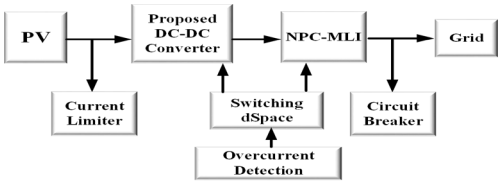


FIGURE 18. Protection diagram of the proposed system.

a three-phase switch mounted on the module front panel. This three-phase switch is a triple-pole, single-throw switch. Each phase leg of the three-phase switch is protected against overcurrent and short-circuits by a thermal-magnetic circuit breaker. At the DC-side, a current limiter at the PV emulator is used to protect the DC-side switches. Moreover, in the dSPACE software (controldesk), an overcurrent detection as well as fault detection have been used so that when a power switch of the proposed system is exceeding the current limit and/or going to fault, all of the power switches are switched-off to prevent any damages (the protection diagram is shown in Fig. 18). Since the proposed system is connected to the grid, the synchronization with the grid is required, which is provided by using voltage measurement, Phase-locked-loop (PLL) control that constantly adjust to match the frequency of the input signal, and a synchronization module as shown in Fig. 17.

The responses of the experimental study are presented in Fig. 19-24. The voltage balancing capability of the proposed converter is verified by the balanced output voltage (equal in magnitude and 120° phase shifts) of three-phase NPC-MLI in Fig. 19 (a), which is same as that of simulation results in Fig. 10 (a). It is quite evident that each level of the inverter output voltage (three-levels in both positive and negative half-cycles, as well as one zero level which is seven levels in total) are following the required MPPT voltage for the respected irradiance. The switching frequency order is also brought in Fig. 19 (a) which indicates that the switching frequency is 5 KHZ and the harmonic orders are in good conditions. The phase a current of the MLI has is shown

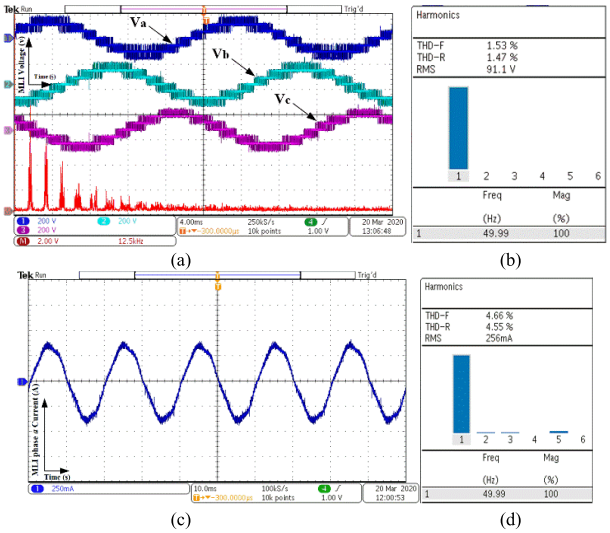


FIGURE 19. Experimental results for (a) the output voltage of MLI (b) THD voltage performance of MLI (c) phase *a* current of MLI (d) THD performance of phase *a* current.

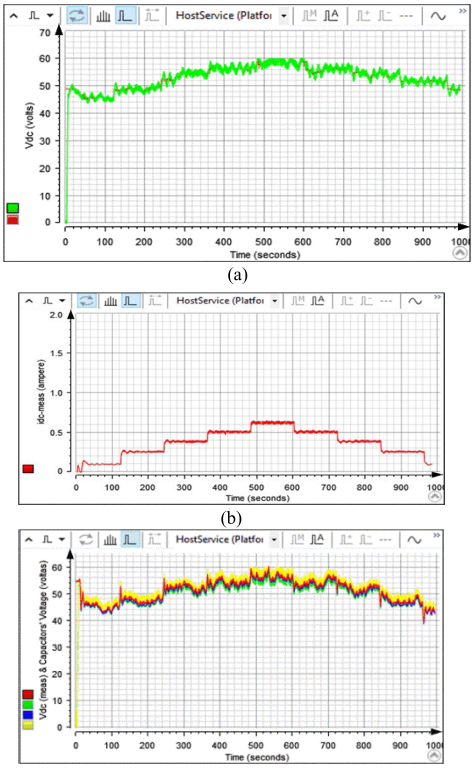


FIGURE 20. Experimental results for (a) reference and measured PV voltage (b) PV's measured current and (c) Capacitors' voltages comparing PV measured voltage.

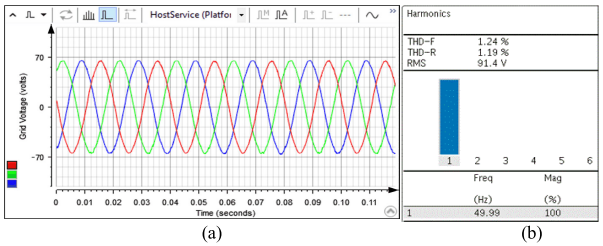


FIGURE 21. Experimental results for (a) Grid voltage zoomed in 1000 w/m^2 and (b) its FFT analysis.

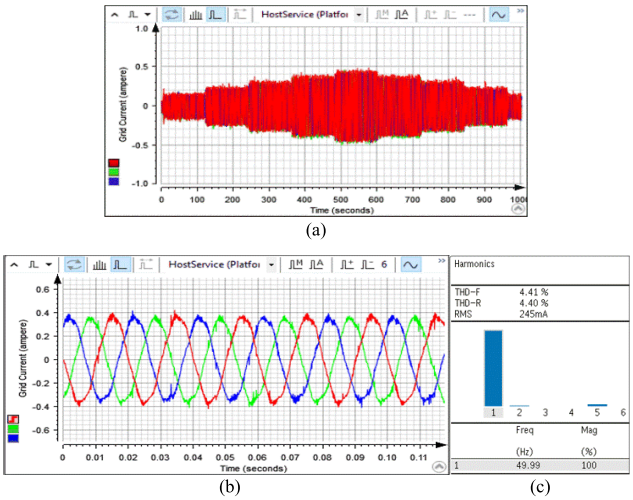


FIGURE 22. Experimental results for (a) Grid current in different irradiances (b) grid current in 1000 w/m^2 and (c) THD performance of MLI phase *a* current in 1000 w/m^2.

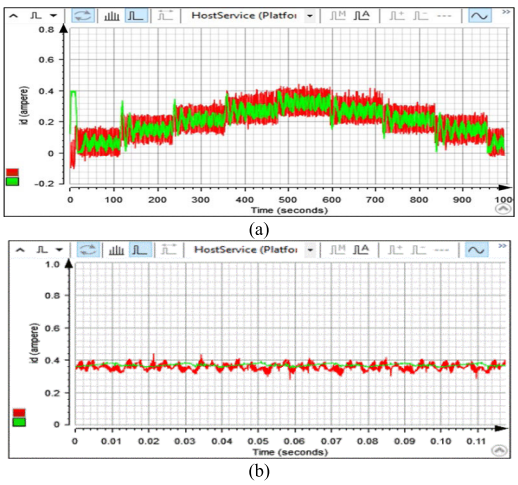


FIGURE 23. Experimental results for d-axis current (a) in different irradiances and (b) in 1000 w/m^2.

in Fig. 19 (c). The THD levels for inverter output voltage and currents are shown in Fig. 19 (b) and (d). The PV array voltage and current, as well as the DC link capacitor voltages are shown in Fig. 20 (a), (b) and (c), respectively. It is clear from the figure that the PV array voltage tracks the required MPPT voltage under different irradiance, and hence ensure harvesting of maximum possible solar power. Three-phase grid voltage and current are shown in Fig. 21 and Fig. 22, respectively, which confirms the ability of the proposed converter in voltage balancing and boosting with the improved power quality in grid connected operation. It can be seen from the current response that the AC current flowing to the grid

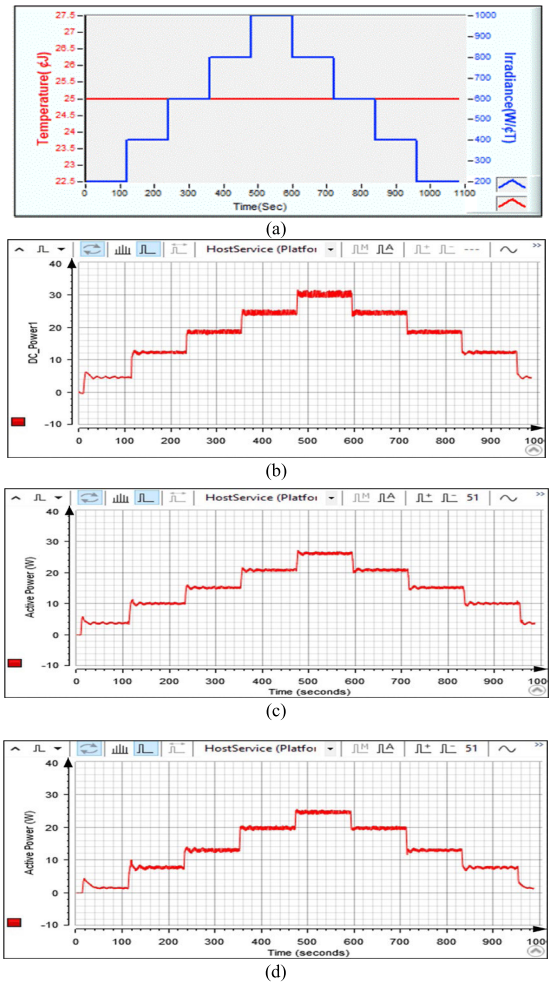


FIGURE 24. Experimental results (a) irradiance changes (b) input DC power in temperature of 25°c (c) active power in temperature of 25°c and (d) active power in temperature of 45°c.

is varying in correspondence to different irradiation level and ensure export of maximum possible solar power (as shown in Fig. 24 (a)) under varying weather conditions.

Fig. 23 shows the d-axis current under different irradiance (Fig. 23 (a)) and the zoomed in 1000 w/m^2 (Fig. 23 (b)) with its reference indicating its accurate tracking and transfer of maximum power to the grid. In addition, extracted solar DC power and the AC power transfer to the grid under varying irradiation and temperature conditions are shown in Fig. 24 (a)-(d), which depicts the capability of the proposed converter to extract and transfer maximum possible solar power to the grid under varying irradiation and temperature levels. It is worth noting that the experimental efficiency is 93.3% and it will be more in higher power.

IX. CONCLUSION

A new step-up voltage balancing converter for solar photovoltaic system which is suitable for NPC-MLI has been proposed in this paper. The proposed converter not only can boost the input PV voltage at the desired output level, but also can remove the magnetic elements which reduces the weight and cost of the system. It also requires only one DC source or PV array output to produce multi-level output, which reduces the number of input voltage sources required in such systems. Capacitance calculation, voltage ripple of the capacitors, output power and normalized energy according to the number of output levels are also analyzed. A deep comparison with other DC-DC topologies has been done and showed the cost effectiveness of the proposed converter. The proposed converter is implemented for a grid connected solar PV system with a NPC multilevel inverter, which is controlled using vector control scheme. The proposed system with associated controllers is implemented in *Matlab/SimPowerSystem* and experimentally validated using dSPACE DSP (digital signal processor) system and designed converters. The simulation and experimental results confirms that the proposed topology can effectively balance the DC link voltage, extract maximum power from PV module and inject power to the grid under varying solar irradiances with very good steady state and dynamic performances.

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AMIR TAGHVAIE (Student Member, IEEE) was born in Sari, Iran, in 1990. He received the B.Eng. degree in electrical engineering from the Islamic Azad University of Aliabad, Aliabad, Iran, in 2012, and the M.Eng. degree in electrical engineering from the Babol Noshirvani University of Technology, Babol, Iran, in 2016. He is currently pursuing the Ph.D. degree in electrical engineering with Deakin University, Geelong, VIC, Australia. His research interests include switched-capacitors converters, high-voltage high-power multilevel inverters, and power converters and its applications in renewable energy and power grid.

MD. ENAMUL HAQUE (Senior Member, IEEE) graduated in electrical and electronic engineering from the Bangladesh Institute of Technology (BIT), Rajshahi, Bangladesh. He received the M.Eng. degree in electrical engineering from the University of Technology Malaysia (UTM), Malaysia, and the Ph.D. degree in electrical engineering from the University of New South Wales (UNSW) Sydney, Sydney, Australia. He has worked for King Saud University, Saudi Arabia; United Arab Emirates University as an Assistant Professor; and the University of Tasmania, Australia. He is currently working as a Senior Lecturer with the School of Engineering, Deakin University, Australia. His research interests include control and power electronic applications in renewable energy (wind, solar PV), energy storage, electric vehicle, motor drives, microgrid, and smart grid. He is the current IEEE Industry Applications Society (IAS) Technical Chapters Area Chair, R10 Southeast Asia, Australia and Pacific, and the Vice Chair of the IEEE Power and Energy Society Victorian Chapter, Australia.

SAJEEB SAHA (Member, IEEE) received the Ph.D. degree in electrical and electronic engineering from The University of Melbourne, Melbourne, VIC, Australia, in 2012. Since 2016, he has been a Lecturer in electrical and electronic engineering with the School of Engineering, Deakin University, Geelong, VIC, Australia, where he is currently an Active Member of the Renewable Energy and Energy Storage Laboratory. His research interests include integration of renewable energy sources, smart grids, battery energy storage, and cyber security of power grid.

MD. APEL MAHMUD (Senior Member, IEEE) received the bachelor's degree in electrical engineering from the Rajshahi University of Engineering and Technology (RUET), in 2008, and the Ph.D. degree in electrical engineering from the University of New South Wales (UNSW) Sydney, Australia, in December 2012. He is currently working as a Senior Lecturer in electrical and renewable energy engineering with Deakin University, Australia. His research interests include power system stability, control of power systems, including renewable energy sources as well as microgrid, energy management for microgrid, energy storage systems, transactive energy (data analytics), and nonlinear control theory. He received the University Gold Medal for his bachelor's degree and the Best Thesis Award for his Ph.D. degree.