A Support Vector Regression based Machine Learning method for on-chip Aging Estimation

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Abstract*—Semiconductor supply chain industry is spread worldwide to reduce cost and to meet the electronic systems high demand for ICs, and with the era of internet of things (IoT), the estimated numbers of electronic devices will rise over trillions. This drift in the semiconductor supply chain produces high volume of e-waste, which affects integrated circuits (ICs) security and reliability through counterfeiting, i.e., recycled and remarked ICs. Utilising recycled IC as a new one or a remarked IC to upgrade its level into critical infrastructure such as defence or medical electronics may cause systems failure, compromising human lives and financial loss. This paper harvests aging degradation induced by BTI and HCI, observing frequency and discharge time affected by changes in drain current and sub-threshold leakage current over time, respectively. Such task is undertaken by Cadence simulations, implementing a 51-stage ring oscillator (51-RO) using 22nm CMOS technology library and aging model provided by GlobalFoundries (GF). Machine learning (ML) algorithm of support vector regression (SVR) is adapted for this application, using a training process that involves operating temperature, discharge time, frequency, and aging time. The data sampling is performed over an emulated 12 years period with four representative temperatures of 20°C, 40°C, 60°C, and 80°C with additional testing data from temperatures of 25°C and 50°C. The results demonstrate a high accuracy on aging estimation by SVR, reported as a normal distribution with the mean (μ) equal to 0.01 years (3.6 days) and a standard deviation (σ) of ±0.1 years (±36 days).

***Index Terms*—IC Age estimation, ML for IC age prediction, counterfeit ICs, subthreshold leakage and drain current, bias temperature instability (NBTI/PBTI), hot carrier injection (HCI), green ICT.**

I. Introduction

The distribution of semiconductor industry across the globe jeopardises the security and reliability of electronic systems due to counterfeiting, which is a growing threat for modern ICs. The high demand on semiconductor supply chain to produce billions of ICs, also generates high volume of e-waste. If the e-waste is not recycled professionally and under trusted recycling centre, it motivates recyclers to enter the IC market with components violating electronic systems lifetime and performance. This includes electronics such as smartphones, medical devices (pacemakers and devices used in ICU) to space and defence sectors [1]. In particular, IC counterfeiting incidents due to recycled and remarked components represent 80-90% of all counterfeits [1]. Among other types, it is worth mentioning ICs being overproduced, cloned, out-of spec/defective, tampered, and ICs with forged documentation [1]. Utilising recycled IC as a new or a remarked to upgrade its level in critical infrastructure such as defence or medical electronics may cause systems failure leading to a disaster, involving human lives and financial loss. As a result, detecting and estimating ICs age is critical for security applications to detect recycled and remarked ICs and age estimation for reliability applications to assure circuit performance and lifetime.

Detecting counterfeit ICs including recycled and remarked ICs has been extensively studied in the literature based on different techniques. These techniques vary in terms of implementation method as can be analysed as follow: physical and electrical inspections using external tools to image IC package and interior design architecture by a microscope scan [2], track and trace methods by providing a unique fingerprint for each IC such as physical unclonable function (PUF) to extract a signature through the IC physical characteristics with process variation [3].

Aging sensors can be used in recycled IC detection as proposed in [4]–[6] using transistor sub-threshold leakage current to measure discharge time (τ_{dv}) when a gate (transistor) is turned-OFF due to aging effects: bias temperature instability (BTI: positive and negative PBTI/NBTI) and hot carrier injection (HCI). Discharge time is defined as the time for output voltage to reach 10% of the supply voltage when the switching gate is turned-OFF [4]. Aging senors based on frequency (f) measurement were presented in [7] and [8] to distinguish between a fresh and aged ring oscillators for recycled ICs detection.

A different approach was proposed in [9] by introducing a real-time prediction ML model to predict IC age using path-delay. The proposed ML in [9] was validated with three scenarios of configurations and with age time of 8 years and at 10°C, 25°C, 50°C, and 75°C, and at different time intervals from 0 to 8 years. Each scenario was tested under a specific time-variant operating condition and five different ISCAS'89 benchmarks were utilised to extract only critical

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paths delay (paths degraded by 20%) during 8 year of aging on a 45-nm CMOS technology [9]. The root mean square error (RMSE) was used to evaluate the proposed model prediction accuracy based on path delays and the average value for the RMSE is less than a 2% for all critical paths for each benchmark utilised in the three implemented scenarios [9].In [10], a statistical method to detect recycled IC using a one-class support vector machine (SVM) is proposed to measure the electrical parameters during fabrication based on process variations (PVs) distribution of brand new devices without gathering actual aging degradation information over usage time.

Techniques used in [7] and [8] have a lower detection rate as the frequency is the only transistor parameter utilised to detect IC age compared to a more sensitive age detector that is utilised in [4] and [6] by measuring the sub-threshold leakage current changes over short usage time to detect the IC age. Moreover, the ML models to estimate ICs age in [9] suffer from a lower detection rate as the path-delay is deployed to estimate IC age, and the method in [10] does not represent a real-time aging degradation over usage time as the data is extracted during fabrication process only based on Early Failure Rate (EFR) from an industrial design.

The focus of this paper is to provide a cost-effective and accurate real-time age estimation on-chip based on a comprehensive supervised machine learning (ML) model that considers two transistors' parameters: sub-threshold leakage current and drain current, and operating conditions such as temperature to overcome limitation of the above techniques [7]–[10] to increase estimation rate. The advantage of combining the two parameters is explained in section III. This proposal can be used in a variety of security and reliability applications. Possible applications to deploy and adopt the proposed model include: 1) detect counterfeit recycled and remarked ICs, 2) boost the process of legalising recycled ICs market to reduce e-waste, and 3) use the proposed model for ICs age estimation to create quality assurance profiles of individual IC [11].

This comprehensive ML model is investigated based on the main transistors aging effects: BTI and HCI. The ML model deploys two critical transistors' parameters, namely- sub-threshold leakage current and drain current changes induced by BTI and HCI, to detect discharge time (τ_{dv}) increase and frequency (f) degradation over usage time depending on time-variant (age time) and operating conditions (e.g., temperature variations).

The rest of this paper is organised as follows. Section 2 presents transistor aging background. Section 3 focuses on related work that utilises the sub-threshold leakage and drain currents and explains the reason for combining the discharge time (τ_{dv}) and frequency (f) parameters in the proposed ML model. Section 4 proposes the research methodology and the proposal for a ML model for ICs age estimation for detecting a short period of usage in the field. Next, simulations and the proposed ML model results are discussed in Section 5. Finally, conclusions are drawn with the future work for the research.

II. Background

The aging phenomenon in ICs has existed for almost five decades; it has developed over time due to the materials used in ICs and the supply voltages scaling. This paper study the most affected aging mechanism to ICs, PBTI/NBTI and HCI but NBTI is the critical aging mechanism in the recent nanometre CMOS technologies [6] for PMOS transistors, whereas PBTI and HCI can be negligible and only impact NMOS transistors. Leveraging aging effects of BTI and HCI has been studied in [11], [13], [14]. NBTI occurs at elevated temperature and under negative gate bias, positive oxide charge and interface states traps are generated in the structure of metal-oxide-silicon (MOS) [12], [15]. This operation caused by the NBTI results shift in V_{th} and it becomes harder for the transistor to turn-ON with aging [12], [15]. NBTI not only shifts the device V_{th} but also decreases the drain current gradient over aging time due to positive charge creation and at the same time more interface states are created [15], [16]. The creation of interface states cause the carrier mobility (μ) to become smaller with aging [15].

The NBTI exhibits two phases during the ICs lifetime, stress and recovery and that impact the threshold voltage (V_{th}) shift [10], [15]. The stress phase happens when the transistor is ON when the NBTI at the gate expose to a negative voltage, whereas the recovery phase occurs when the voltage stress is removed and the transistor is OFF [10]. The degradation effect induced by the NBTI during the stress time may recover partially [10], [15].Thus, considering these two phases during simulations is important and it has a better age detection rate.

Hot carriers are composed of holes and electrons that have been exposed to a high energy by local electrical fields. If a carrier gains a kinetic energy, it could overcome the silicon-insulator barrier height and gate oxide and it may collide with atoms due to the ionization process effect in the pinch-off region and the electron-hole pairs are produced [17]. After the carrier surmount the barrier and reside in the insulator, the electron and hole are trapped into the gate oxide. Due to high energy carriers, the interface states are generated in the gate oxide. Two changes occur, 1) the device threshold voltage shift due to the accumulated trapped charges, and 2) a reduction in device drain current, a degradation in the sub-threshold slope and an increase in the device leakage due to the accumulated interface states. The HCI in recent CMOS technology is negligible. Although, in this work BTI and HCI are investigated to mimic the impact of aging degradation.

III. Related Work

A. Transistor Parameters

A reduction in the sub-threshold leakage current (I_{subth}) occurs by the NBTI aging effects. This reduction in the I_{subth} is beneficial for static power consumption [13], [14]. The I_{subth} reduction takes place due to the exponential increase induced by the NBTI between the I_{subth} and threshold voltage (V_{th}). This correlation with aging is an advantage for a sensor that underpins that change over time, referred as discharge

time (τ_{dv}) in literature and it increases over time as derived by (1) [6]:

$$I_{leak} \simeq I_{subth} \simeq \mu C_{ox} \frac{W}{L} (\frac{kT}{q})^2 e^{\frac{-qV_{th}}{nkT}}, \quad (1)$$

Where *W* is the channel width, *L* is the channel length, C_{ox} is the gate oxide capacitance, μ is the carrier mobility, *T* is the temperature, *K* is the Boltzmann constant, *q* is the electron charge and *n* is a parameter for the device fabrication. The *n* parameter contributes to the drain current gradient reduction along with the interface states creation with aging.

Based on the facts explained above, an exponential correlation between the decrease in the I_{subth} and the increase in the threshold voltage (V_{th}), as derived by (1). Therefore, the dischagre time (τ_{dv}) increases over the IC age time as the I_{subth} decreases. In contrast, drain current (I_D) has an approximate linear correlation between the decrease in the I_D and the increase in the V_{th} due to BTI-induced degradation, which is represented by (2 and 3); thus, the drain current in CMOS technologies [6] is shown as:

$$I_D(t) \simeq K_{act}[V_{gs} - (V_{th0} + \Delta V_{th}(t))], \quad (2)$$

$$I_D(t) = I_{D0} - K_{act} \Delta V_{th}(t), \quad (3)$$

Where K_{act} is a constant that depends on the technology parameters and the design, $V_{th}(t)$ is the threshold voltage drift over a period of time that is caused by the aging effects and V_{th0} is the fresh device threshold voltage.

Due to aging effect caused by BTI, the drain current is greater in a new IC than in an aged IC; this is due to the aforementioned linear correlation. Thus, the frequency of a ring oscillator (RO) is expected to be lower in the aged IC because it depends on drain current. Based on the correlations explained about sub-threshold leakage current and drain current, we can confirm that the discharge time (τ_{dv}) is more sensitive than the frequency degradation. Moreover, the I_{subth} is unstable with temperature, whereas the drain current is stable with temperature. This has an impact on the proposed ML model measurements when both parameters are combined. Towards that end, deploying the I_{subth} and f of a ring oscillator for the proposed ML model will help to explore these two transistor parameters with temperature variations based on the physical characteristics of each parameter. Thus, the investigation will lead to the development of the proposed ML IC age estimation model to accurately estimate the age of an IC and mitigate the risk of IC counterfeiting and provide lifetime quality assurance.

IV. Proposed ML Model for IC Age Estimation

A. Measuring Transistor Parameters

The discharge time (τ_{dv}) and output frequency (f) is measured from a 51 stage ring oscillator (51-RO) by an emulated period of 12 years in Cadence. This time is based on the lifetime expectancy of ICs for industrial, automotive and aerospace applications [23], [24]. During the aging time (12 years), transient analysis is performed for the 51-RO, generating a total of forty samples of τ_{dv} and f. The f is probed directly from the output of the RO, whereas the τ_{dv} is captured using a cycle-counter sensor described in [25]. Fig. 1 shows the adapted version of the sensor diagram that operates as time to digital converter, which is low cost and typically present in the infrastructure of electronic chips [25]. The sensor is formed by a logic AND gate, buffer and counter. The calculation is undertaken by counting the rising edges of the clock until the output of 51-RO drops to logic-0, considered when the voltage reaches 10% of V_{dd}. The counter value is then multiplied by the clock period to obtain the discharge time in units of time (ns).

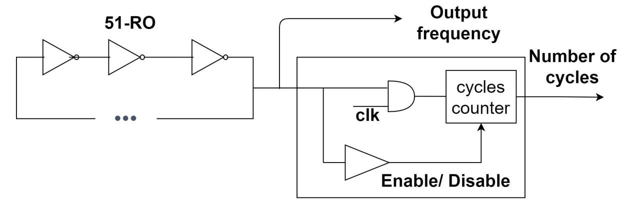

Fig. 1. Frequency and discharge time sensor.

Algorithm 1 Proposed age estimation model steps

1: **Offline**
2: Data pre-processing: Data collection from selected ICs on Cadence and labelling (discharge time and frequency, temperature and age time)
3: ML: Data processing: Selection of estimator and target data for SVR training
4: ML: Training and optimisation of SVR estimator
5: **Online**
6: ML: Testing of SVR estimator with random input data

B. Support Vector Machine Regression Model (SVR)

The machine learning algorithm of support vector regression (SVR) is known to have a reliable performance in predicting time-series data [21], [26]. An important characteristic of a supervised SVR is the capability to classify data which is not linearly separable. This algorithm introduces the kernel transformation which is a data manipulation that maps the input to a higher dimension space to solve the regression problem and reduces computational complexity [22]. The proposed algorithm for the generation of an aging estimator model has mainly two sections, offline and online (Algorithm 1). In general, the first section includes data collection from the integrated circuit (IC) using the Cadence tools such as the Virtuoso Analog Design Environment. In this case the collection of τ_{dv}, output f, working temperature and aging time of a 51 stage RO (51-RO). Then, data pre-processing and sorting is carried out. The next step is data processing, where labelling is undertaken to define the set of estimators and response values, in this case the target is aging. In addition, a suitable arrangement is chosen for the data, for instance an

array of four columns is built, including all data collected. The last step performed offline is the generation of a machine learning model for aging estimation. The result is a full, trained support vector machine regression model (SVR) that is able to estimate aging trend of individual ICs with its own working conditions. Finally, the SVR is tested online, where trained model receives random data of τ_{dv}, f and temperature, delivering the aging estimation. From this stage, the SVR can be portable and placed on-chip for real-time monitoring and aging estimation.

V. Results and Discussion

A. Simulation Results

The RelXpert tool provided by Cadence is used to simulate the 51-stage RO aging simulations, which is configured as follows: the supply voltage is $(V_{dd}) = 0.9$V, age time 12 years, the working temperature variation includes four temperatures, i.e. 20°C, 40°C, 60°C, and 80°C, with a RO output load capacitance of 250fF. The utilised CMOS technology and aging model is a 22nm provided by GlobalFoundries (22nm GF). The aging effects: NBTI, PBTI and HCI are selected for all simulation runs to measure aging for the circuit under test (51 RO) with each one of the four simulated temperatures to accurately build the proposed ML for ICs age estimation.

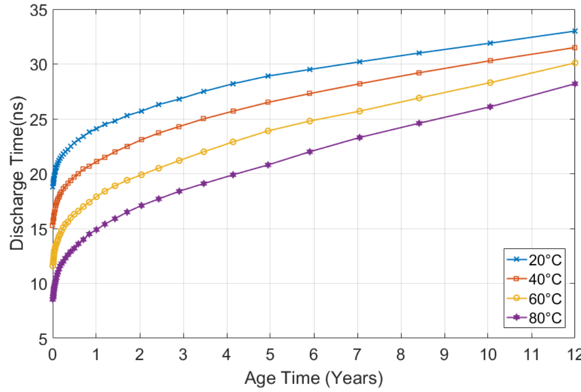

Fig. 2. 51-stage RO discharge time over 12 years.

Another critical aspect is included in the simulations to reduce the NBTI recovery effect when measuring the discharge time and frequency, and avoid misreading these two parameters. As can be seen from Fig. 2 and Fig. 3 that most of the aging occurs at early time of the RO and after that period a gradual increase is observed over the years for the 51 RO, τ_{dv} and f as the NBTI is saturated for longer stress time. These two trends are well-known and confirmed by the scientific research as discussed in [18]. Fig. 2 shows the 51 RO discharge time (τ_{dv}) results over 12 years lifetime, at 20°C the $\Delta\tau_{dv}$ after 2 years is 36.51%, 4 years is 49.74%, 6 years is 56.76%, 8 years is 64.62%, 10 years is 69.58%, and 12 years is 75.12%, whereas at 80°C the $\Delta\tau_{dv}$ after 2 years is 100.04%, 4 years is 133.20%, 6 years is 157.13%, 8 years is 188.14%, 10 years is 205.30%, and 12 years is 229.98% based on (4).

$$\%\tau_{dv} = \frac{Aged\tau_{dv} - Fresh\tau_{dv}}{Fresh\tau_{dv}} \times 100 \quad (4)$$

This range of simulated temperature values between 20°C and 80°C prove that the τ_{dv} can be detected even with temperature variation and as expected, it is more sensitive to higher temperature. From Fig. 2, we can observe the following: 1) the fresh τ_{dv} period is smaller and even more smaller with higher temperature due to the high I_{subth} current in new ICs (leaks faster), 2) the aged τ_{dv} period is bigger for all temperatures because the I_{subth} in aged ICs is low (less leaky), 3) the $\Delta\tau_{dv}$ is bigger at higher temperatures and age time. The τ_{dv} trends with temperature variation for fresh and age times are also captured by [4] and [6] using different temperature configurations. Fig. 3 shows frequency degradation data for the 51 RO with the same simulated temperatures as in Fig. 2, at 20°C the f after 2 years is 17.33%, 4 years is 21.35%, 6 years is 23.62%, 8 years is 26.02%, 10 years is 27.33%, and 12 years is 28.65%, whereas at 80°C the f after 2 years is 28.04%, 4 years is 33.91%, 6 years is 37.24%, 8 years is 41%, 10 years is 43.17%, and 12 years is 45.48% based on (5).

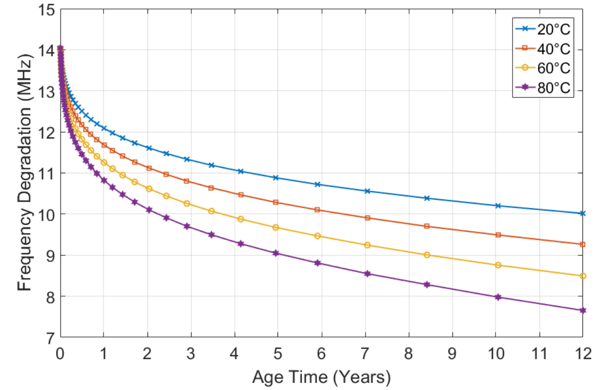

Fig. 3. 51-stage RO frequency degradation over 12 years.

$$\%f = \frac{Fresh_f - Aged_f}{Fresh_f} \times 100 \quad (5)$$

It can be seen clearly that the τ_{dv} is more sensitive to temperature and provides higher $\Delta\tau_{dv}$ compared with the f, and therefore, a better aging detector. For example, after 12 years at 20°C, Δf is 28.65% and $\Delta\tau_{dv}$ is 75.12% almost 2.62 times increase, whereas at 80°C, Δf is 45.48% and $\Delta\tau_{dv}$ is 229.98% almost 5.06 times increase. Before proceeding with the ML aging estimation model, Monte Carlo (MC) simulations were also performed to account for process variation (PV) when measuring the discharge time within RO (intra-die PV) and between ROs (inter-die) to avoid age misprediction when the ML model is deployed at the advance stages as detailed in Algorithm 1 steps. The PV simulations were configured for intra-die and inter-die PVs using 800 MC permutations for each individual temperature of the three representative temperature 20°C, 40°C, and 60°C with a total

of 4800 MC permutations. Results are reported in the scatter samples as can be seen from Fig. 4 and Fig. 5 for the 51-stage RO Gaussian distribution with standard deviations (σ), ±3 process variations.

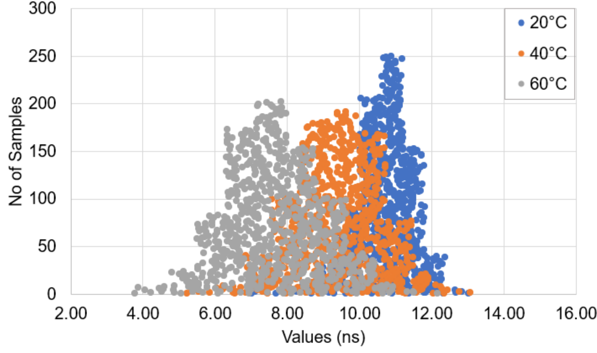

Fig. 4. 51-stage RO τ_{dv} inter-die process variation results at 20°C to 60°C.

In Fig. 4, at 20°C, the mean (μ) is 10.67ns, the standard deviations (σ) is 810.6ps and with a deviation of 7.60%, 40°C μ is 9.40ns, σ is 1.19ns and with a deviation of 12.66%, and at 60°C μ is 7.67ns, σ is 1.31ns and with a deviation of 17.08%. In contrast, in Fig. 5, at 20°C, the μ is 10.81ns, σ is 385ps and with a deviation of 3.56%, 40°C μ is 9.42ns, σ is 539.1ps and with a deviation of 5.72%, and at 60°C μ is 7.72ns, σ is 596.8ps and with a deviation of 7.73%. Computing PVs impact on device parameters along with operating conditions (i.e. temperature) before using the data set to train the ML model should improve the model age estimation accuracy because different versions of IC will behave differently.

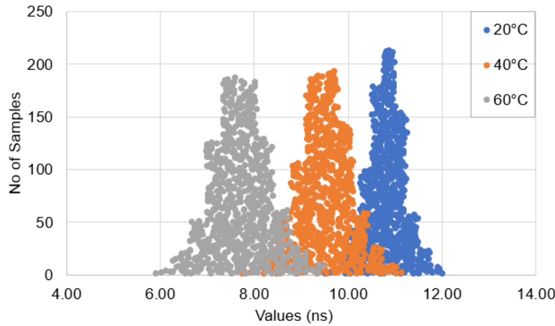

Fig. 5. 51-stage RO τ_{dv} intra-die process variation results at 20°C to 60°C.

B. Machine Learning Aging Estimation Results

The machine learning model used in this work is trained with a specific 22-nm CMOS technology provided by GlobalFoundries. However, this can be ported to any technology node and circuitry design by following the steps depicted in Algorithm 1. The data is collected from 51-RO based on GF 22-nm, working continuously over the simulation time of 12 years with a total of 252 data points. The RO size was chosen as proposed in [4], [5] and it can be selected from the manufacturing process monitors in modern circuits [8]. The simulation provides the aging numbers under six temperatures, where four are used as the training data: 20°C, 40°C, 60°C, and 80°C, whereas 25°C and 50°C are used as the testing data for the proposed machine learning. The generation of an estimator model is carried out by support vector regression (SVR), known to have a good performance in local minima [19], [20]. The Gaussian Kernel is used for the training of SVR, which has demonstrated to perform well for similar data set, employing the standard optimisation method of hyper-parameters described in [26], the values used are: Box Constraint = 294.27, Kernel Scale = 1.87 and Epsilon = 0.003. The training data for the SVR is an array constructed with temperature, RO output discharge time, RO output frequency and aging, where the aging is considered as the target to estimate.

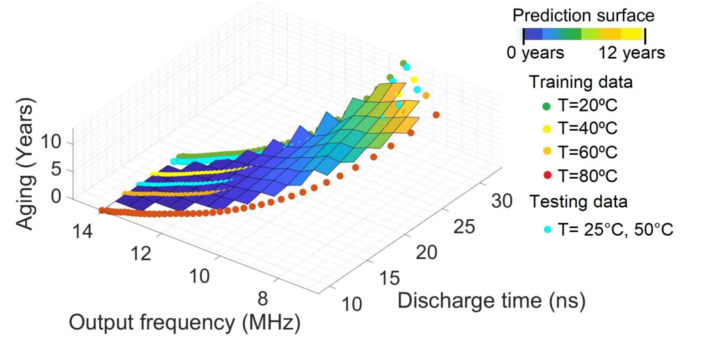

Fig. 6. Estimation surface and training Data.

The results can be observed in Fig. 6, where the estimation surface is constructed with response values generated by the trained SVR, which practically encloses all training and testing data points. This means that estimator model is capable to cover any neighbour data around the provided input. The figure reports the aging numbers for each combination of discharge time and output frequency from the 51-stage ring oscillator. The training data is presented as a reference for four representative temperatures, starting with 20°C in green colour, and varying these colours towards the red until 80°C. The testing data is shown in light blue colour for two temperatures, 25°C and 50°C. These data points demonstrate the decreasing trend of the frequency in Fig. 3 and the increment of the discharge time reported in Fig. 2. In addition the estimated data of aging is presented in a surface, which is the estimation provided by SVR, when using all training data. This surface has colours from blue to yellow, with the former representing the fresh time and the yellow part being the aging time of 12 years.

Furthermore, Fig. 7 presents the accuracy of aging estimations with given testing data (25°C and 50°C), demonstrating a high accuracy with the mean (μ) equal to 0.01 years (3.6 days) and a standard deviation (σ) of ±0.10 years (±36 days). Therefore, based on the 3 sigma rule for a normal distribution, when any randomly selected set of testing data point (temperature, discharge time, and frequency) is used as input of the aging estimator model, there is a probability of 68% (1-σ) that the deviation will be as small as ±36 days,

with the rest of cases falling into ±108 days (3-σ) of deviation. Our future work will use additional data to further validate our proposed SVR model to increase aging estimation accuracy and cover the impact of process variation as shown in Fig. 4 and Fig. 5.

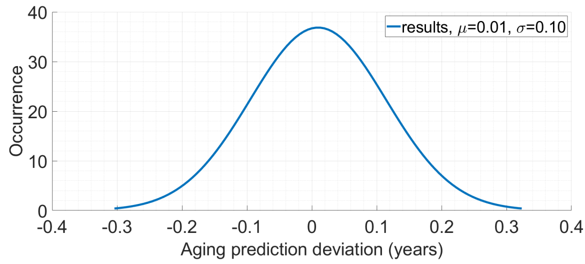

Fig. 7. Normal distribution results of aging estimation deviation.

VI. Conclusion

The semiconductor industry faces the challenge of recycled and remarked ICs, which threatens the security and reliability of electronic devices. Legalising and re-utilising recycled ICs with lifetime assurance under operating conditions should reduce recent global chips shortage. This paper proposes a technique to estimate aging of CMOS ICs, using a machine learning (ML) algorithm. The training data of the ML is the working temperature, τ_{dv} and f induced by BTI and HCI. This data is obtained from Cadence tools implementing 51 stage ring oscillator, using 22-nm CMOS technology library and aging model provided by GlobalFoundries. The selected ML algorithm is the support vector regression (SVR), known to have a reliable performance in estimating time-series data. The training process of SVR is undertaken over a 12 years period with four representative temperatures of 20°C, 40°C, 60°C, and 80°C. The testing of the trained model is conducted with two temperatures, i.e. 25°C and 50°C. The results show the aging estimation as a normal distribution with the mean (μ) equal to 0.01 years (3.6 days) and a standard deviation (σ) of ±0.1 years (±36 days). This proposal paves the way for a cost-effective on-chip solution to estimate IC age for security and reliability applications.

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