applied sciences

MDPI

Article

A 0.3 V, Rail-to-Rail, Ultralow-Power, Non-Tailed, Body-Driven, Sub-Threshold Amplifier

Francesco Centurelli, Riccardo Della Sala, Giuseppe Scotti * and Alessandro Trifiletti

Dipartimento di Ingegneria dell'Informazione, Elettronica e Telecomunicazioni (DIET), Università di Roma La Sapienza, 00184 Roma, Italy; francesco.centurelli@uniroma1.it (F.C.); riccardo.dellasala@uniroma1.it (R.D.S.); alessandro.trifiletti@uniroma1.it (A.T.)

* Correspondence: giuseppe.scotti@uniroma1.it

Abstract: A novel, inverter-based, fully differential, body-driven, rail-to-rail, input stage topology is proposed in this paper. The input stage exploits a replica bias control loop to set the common mode current and a common mode feed-forward strategy to set its output common mode voltage. This novel cell is used to build an ultralow voltage (ULV), ultralow-power (ULP), two-stage, unbuffered operational amplifier. A dual path compensation strategy is exploited to improve the frequency response of the circuit. The amplifier has been designed in a commercial 130 nm CMOS technology from STMicroelectronics and is able to operate with a nominal supply voltage of 0.3 V and a power consumption as low as 11.4 nW, while showing about 65 dB gain, a gain bandwidth product around 3.6 kHz with a 50 pF load capacitance and a common mode rejection ratio (CMRR) in excess of 60 dB. Transistor-level simulations show that the proposed circuit outperforms most of the state of the art amplifiers in terms of the main figures of merit. The results of extensive parametric and Monte Carlo simulations have demonstrated the robustness of the proposed circuit to PVT and mismatch variations.

Keywords: body-driven; ultralow voltage; ultralow-power; operational transconductance amplifier; non-tailed differential pair; inverter-based

Citation: Centurelli, F.; Della Sala, R.; Scotti, G.; Trifiletti, A. A 0.3 V, Rail-to-Rail, Ultralow-Power, Non-Tailed, Body-Driven, Sub-Threshold Amplifier. *Appl. Sci.* **2021**, *11*, 2528. https://doi.org/10.3390/app11062528

Academic Editor: Gilsoo Jang

Received: 1 February 2021
Accepted: 6 March 2021
Published: 11 March 2021

1. Introduction

The scaling of CMOS technology, and the diffusion of applications requiring very low power consumption, such as IoT (Internet of Things) nodes [1,2] or biomedical and wearable devices [3,4], have paved the way to the development of compact and ultralow voltage (ULV) circuits. The operation of MOS devices in the deep subthreshold region is mandatory [5,6], to achieve ultralow-power (ULP) consumption and to allow the usage of very low supply voltages.

However, to allow such ultralow supply voltages, specific design approaches are required: floating-gate [7] techniques have been proposed in the past, but the most common solutions are the body-driven (BD) technique and the inverter-based design approach.

Several amplifier designs operating at supply voltages in the order of 0.6 V or lower and exploiting multi-stage, folded cascode or symmetrical OTA topologies have been presented in the last years. The use of a very low supply voltage often requires to eliminate the bias current generator of the differential pair: the resulting pseudo-differential amplifier shows class-AB behavior, but no common mode rejection if the common mode output is exploited. Moreover, there is no control on the bias current, resulting in large variations of small signal performances under process, supply voltage and temperature (PVT) variations.

In BD amplifiers [8–13], the body is used as input terminal instead of the gate, thus allowing the input dc level not to be constrained by the threshold voltage of the devices, at the cost of reduced transconductance gain, higher noise, and an input impedance that is not purely capacitive. In this context, Ferreira et al. proposed a Miller amplifier designed in 350 nm CMOS process and operating at a supply voltage of 0.6 V in 2007 [8]. Magnelli et

al. published an amplifier with a supply voltage of 0.5 V and 75 nW power consumption in 2014 [10]. In the same year, Ferreira et al. designed an amplifier with a supply voltage as low as 0.25 V [9]. Abdelfattah et al. presented an ULV self-biased amplifier, insensitive to CMOS process variations in 2016 [14]. In 2018 Kulej et al. presented bulk-driven 0.5 V amplifiers, exploiting different gain-boosting techniques in 0.18 µm CMOS process [12]. In 2020 the same authors presented an ULV-ULP class AB amplifier, biased in deep sub-threshold region, that exploits the body-driven non-tailed differential pair [13], attaining state of the art performance in terms of the most important figures of merit.

Inverter-based solutions [15–18] exploit the CMOS inverter, or inverter-like structures, such as the Arbel cell [19], as building blocks that allow rail-to-rail signal swing with reduced supply voltages. Moreover, in these structures, the elimination of the bias current generator of the differential pair worsens the common mode rejection (CMRR) and results in large variations of small signal parameters under PVT variations.

In this paper, we propose an inverter-based, differential, body-driven input stage, with a replica bias loop that accurately sets the common mode current of the input stage by controlling the gate terminals of the MOS devices. The novel input stage is used to build an ULV, ULP, two-stage amplifier, in which a dual path compensation strategy is exploited to improve the frequency response of the amplifier.

The paper is structured as follows: Section 2 presents the proposed amplifier topology and describes the replica bias loop that sets the common mode current of the inverter based input stage as well as the CMFF technique adopted to improve the CMRR. Section 3 focuses on small signal analysis of dc-gain, CMRR, and frequency response explaining the adopted compensation strategy. Section 4 discusses the design of the amplifier and presents the simulation results and comparisons with ULV, ULP state of the art amplifiers. Finally some conclusions are reported in Section 5.

2. Proposed Topology

Due to its capability to allow almost rail-to-rail input and output swing, the Arbel cell (or differential inverter) is often used as a building block for low-voltage analog CMOS circuits. To further reduce the minimum supply voltage of the Arbel cell, the bias current generators can be removed and the common mode current can be set by controlling the body terminals of MOS transistors following the approach proposed in [20]. However, for supply voltages lower than 0.5 V, the limited swing of the control voltage at the body terminals reduces the effectiveness of the current setting loop. To overcome this limitation, we propose a body-driven fully differential inverter (Figure 1a) as input stage of the amplifier. We then exploit the gate terminals of the four MOS devices to set both the common mode current by means of a replica bias control loop, and the output common mode voltage through a common mode feed-forward (CMFF) approach. By using the gates as control terminals we are able to enhance the loop gain, thus requiring a smaller swing of the control voltages to guarantee proper operation of the bias control loop even at a very low supply voltage.

A simple push-pull second stage (Figure 1b) is exploited to convert the differential output of the first stage to a single-ended one, providing further gain to compensate for the reduced gain of the first stage due to the use of the body transconductance. One output of the first stage is directly applied to the gate of the PMOS common-source device, whereas the other one is applied to a NMOS common-source followed by a current mirror, to provide the required dc reversal needed both for the dual path compensation strategy and to improve the CMRR. The bias current of the output stage is given by:

$$I_{oQ} = M(I_6 - I_5), \tag{1}$$

where M is the ratio between the form factor (W_8/L_8) of transistor M_8 and the form factor (W_7/L_7) of transistorM_7. I_{oQ} is therefore determined by the current source M_6, by the sizing of M_5, and by the current mirror ratio M. This is also the maximum current that

can be sinked by the stage, that thus presents a class-A behavior, whereas the maximum sourced current is limited only by the available excursion of the gate voltage of M_9.

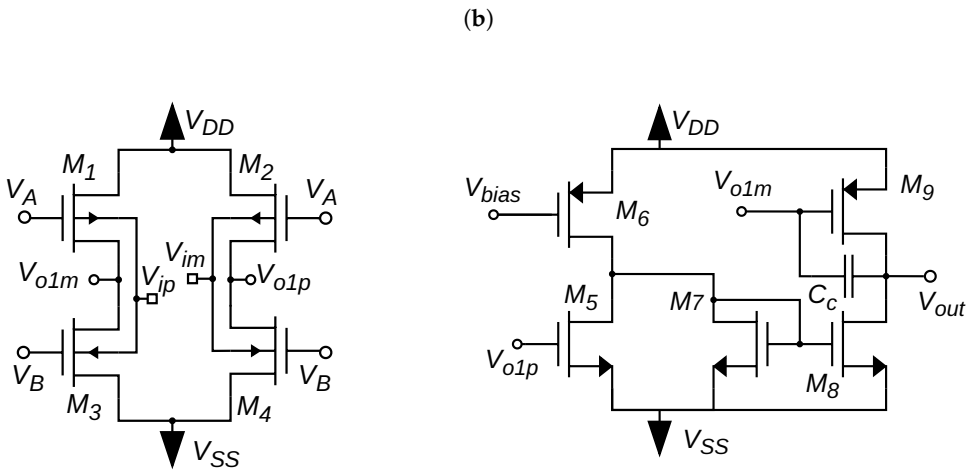


Figure 1. Schematic of the proposed amplifier: (**a**) first stage fully differential amplifier; (**b**) second stage differential to single ended amplifier.

The replica bias loop to set the common mode current of the first stage is shown in Figure 2. The reference current, set by transistor M_{b1}, is applied to devicesM_{b2}-M_{b3}, that are a replica of the N-part of the input stage and are diode connected: The loop acts varying the gate voltage V_B to contrast variations of the input common mode and of device parameters. This bias voltage is applied to the gates of the NMOS transistors of the input stage, thus setting its bias current to a scaled replica of the reference current (scaling factor is given by the ratio of the form factors of the devices).

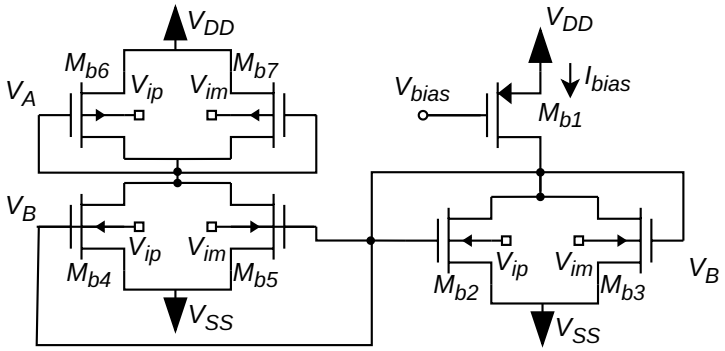


Figure 2. Schematic of the proposed replica bias circuit to set the common mode current of the input stage.

The gate control voltage V_A is exploited to set the output common voltage of the first stage using a common mode feed-forward (CMFF) technique: In the left part of Figure 2, the reference current is mirrored through devices M_{b4}-M_{b5} and applied to M_{b6}-M_{b7} that are a replica of the P-part of the input stage and are diode connected. The gate voltage V_A is applied to the PMOS transistor of the input stage, thus forming a current mirror, and it can be shown (detailed analysis in the Appendix A) that the output common mode voltage of the first stage is set to V_A. The proposed CMFF does not exploit any reference to set the value of the output common mode voltage of the input stage that is determined by the sizing of the devices. In fact, by looking at Figure 2, it is evident that V_A is equal to (V_{DD}-$|V_{GSb6}|$), and therefore, the output common mode is set close to the analog ground for an appropriate sizing of $|V_{GSb6}|$. For example, assuming a dual supply voltage with

V_{DD} = 0.15 V and V_{SS} = −0.15 V, $|V_{GSb6}|$ can be set to about 0.15 V in order to have V_A about equal to 0 V which in this example is the analog ground.

3. Small Signal Analysis

In this section, we report the small signal analysis of the proposed amplifier focusing both on the dc performance (in terms of differential gain and CMRR) and ac performance by computing the frequency response and presenting considerations about the compensation strategy.

3.1. DC-Gain and Common Mode Rejection

The replica bias stage contributes to enhance the common mode rejection ratio (CMRR) of the input stage that would otherwise be one (same gain for differential and common mode signals). Denoting with V_{id} and V_{o1d} the input and the output differential voltage of the input stage ,respectively, the differential gain can be easily derived referring to the circuit in Figure 1a:

$$A_{d1} = \frac{V_{o1d}}{V_{id}} = \frac{V_{o1p} - V_{o1m}}{V_{ip} - V_{im}} = \frac{G_1}{G_{o1}} = \frac{g_{mb_1} + g_{mb_3}}{g_{ds_1} + g_{ds_3}} \tag{2}$$

where G_1 and G_{o1} are the transconductance and the output conductance of the input stage respectively, g_{mb}, g_m and g_{ds} denote the body transconductance, the gate transconductance and the output conductance of the different MOS transistors, as usual, and the subscripts 1 and 3 refer to PMOS and NMOS devices in Figure 1a, respectively.

Denoting with V_{ic} = (V_{ip}+V_{im})/2 and V_{oc} = (V_{o1p}+V_{o1m})/2 the input and output common mode voltage of the input stage, respectively, the common mode gain, with the effect of the replica bias control loop, can be derived referring to the common mode equivalent circuit of the input stage shown in Figure 3:

$$A_{c1} = \frac{V_{o1c}}{V_{ic}} = -\frac{g_{m_1}g_{mb_3} + (g_{mb_1} + g_{mb_3})g_{ds_3}}{(g_{m_3} + g_{ds_3})(g_{m_1} + g_{ds_3} + g_{ds_1})} \approx -\frac{g_{mb_1}}{g_{m_1}} \tag{3}$$

where the approximation holds with the usual assumtpions $g_m >> g_{mb}$ and $g_m >> g_{ds}$. The resulting CMRR can then be calculated as

$$CMRR_1 = \frac{A_{d1}}{A_{c1}} = \frac{g_{mb_1} + g_{mb_3}}{g_{mb_1}} \frac{g_{m_1}}{g_{ds_1} + g_{ds_3}} \tag{4}$$

and is proportional to the intrinsic gain g_m/g_{ds} of the devices.

The CMRR is further improved by the second stage, since, with the dual path approach, the common mode components at the output of the first stage arrive to the output with opposite phases. The analysis of the circuit in Figure 1b provides:

$$V_o = \left(g_{m_8} \frac{g_{m_5}}{g_{m_7}} V_{o1_p} - g_{m_9} V_{o1_n} \right) \frac{1}{G_o} \tag{5}$$

where V_{o1p} and V_{o1m} can be expressed as follows:

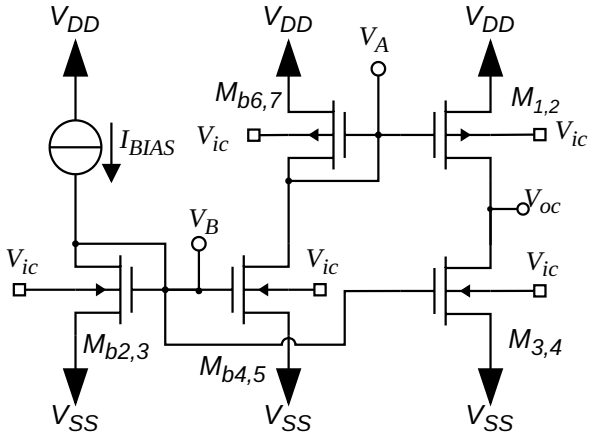
$$V_{o_{1p,m}} = \pm A_{d_1} \frac{V_{id}}{2} + A_{c_1} V_{ic} \tag{6}$$

and

$$G_o = g_{ds_8} + g_{ds_9} \tag{7}$$

is the output conductance of the second stage.

(**a**)



(**b**)

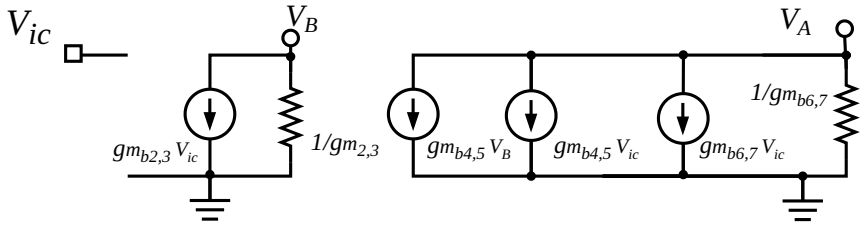


Figure 3. Common mode equivalent circuit of the input stage with replica bias (**a**) and corresponding small signal model (**b**).

The overall CMRR is therefore given by

$$CMRR = CMRR_1 \cdot CMRR_2 \tag{8}$$

with,

$$CMRR_2 = \frac{1}{2}\,\frac{g_{m_5}g_{m_8} + g_{m_7}g_{m_9}}{g_{m_5}g_{m_8} - g_{m_7}g_{m_9}} \tag{9}$$

It is clear from (9) that the CMRR can become infinite by choosing:

$$g_{m_5}g_{m_8} = g_{m_7}g_{m_9} \tag{10}$$

3.2. Frequency Response and Compensation

The use of a dual signal path in the second stage allows some flexibility in optimizing the frequency response: in particular, the zero provided by the dual path can be exploited to cancel one pole of the overall transfer function thus improving the phase margin.

An approximate analysis of the amplifier can be carried out by exploiting the Miller approximation and referring to the small signal equivalent circuit reported in Figure 4, where G_1 and G_{o1} are defined in (2), G_o is given by (7), C_L is the load capacitance and the other capacitances can be expressed as

$$C_1 = C_{gd_1} + C_{gd_3} + C_{db_1} + C_{db_3} + C_{gs_9} + C_{gd_9}\left(1 + g_{m_9}/G_o\right) \tag{11}$$

$$C_2 = C_{gd_1} + C_{gd_3} + C_{db_1} + C_{db_3} + C_{gs_5} + C_{gd_5}\left(1 + g_{m_5}/g_{m_7}\right) \tag{12}$$

$$C_x = C_{gd_5}\left(1 + \frac{g_{m_7}}{g_{m_5}}\right) + C_{gd_6} + C_{gs_7} + C_{gs_8} + C_{gd_8}\left(1 + \frac{g_{m_8}}{G_o}\right) \tag{13}$$

Since C_1 results much larger than C_2, the transfer function V_o/V_{id} has to be calculated by separately considering the paths from V_{ip}=$V_{id}/2$ and V_{im}= $-V_{id}/2$ to V_o:

$$A_d(s) = \frac{V_o}{V_{ip}}|_{V_{im}=0} + \frac{V_o}{V_{im}}|_{V_{ip}=0} \tag{14}$$

The analysis of the circuit in Figure 4 yields a transfer function in the form:

$$A_d(s) = \frac{A_0 N(s)}{(1+s\tau_1)(1+s\tau_2)(1+s\tau_3)(1+s\tau_4)} \tag{15}$$

where

$$A_0 = \frac{G_1}{2G_{o1}}\left(g_{m9} + g_{m8}\frac{g_{m5}}{g_{m7}}\right)\frac{1}{G_o} \tag{16}$$

is the dc gain, the time constants of the poles are

$$\tau_1 = C_L/G_o \tag{17}$$

$$\tau_2 = C_1/G_{o1} \tag{18}$$

$$\tau_3 = C_2/G_{o1} \tag{19}$$

$$\tau_4 = C_x/g_{m7} \tag{20}$$

and

$$N(s) = 1 + s\frac{C_1 g_{m8} g_{m5} + C_2 g_{m9} g_{m7} + C_x G_{o1} g_{m9}}{G_{o1}(g_{m8} g_{m5} + g_{m9} g_{m7})} + s^2\frac{C_x C_2 g_{m9}}{G_{o1}(g_{m8} g_{m5} + g_{m9} g_{m7})} \tag{21}$$

which can be solved by means of well known approximations to obtain the expression of the two zeros as follows:

$$\tau_{z1} \approx \frac{C_1 g_{m8} g_{m5} + C_2 g_{m7} g_{m9} + C_x G_{o1} g_{m9}}{G_{o1}(g_{m8} g_{m5} + g_{m7} g_{m9})} \tag{22}$$

$$\tau_{z2} \approx \frac{g_{m9} C_x C_2}{C_1 g_{m8} g_{m5} + C_2 g_{m7} g_{m9} + C_x G_{o1} g_{m9}} \tag{23}$$

For large load capacitances C_L, $1/\tau_1$ is the dominant pole, and the circuit can be sized to cancel the second pole with one of the zeros, thus improving the phase margin and providing stability without sacrificing the bandwidth. To add a further degree of freedom and achieve an adequate phase margin even for smaller load capacitances, a compensation capacitor C_c can be added between V_{o1n} and V_o (i.e., between gate and drain of M_9 in Figure 1b): Its pole-splitting effect leads to some reduction of the bandwidth that is however negligible if $C_c << C_L$ and moves the pole $1/\tau_2$, placing it nearer to the zero $1/\tau_{z1}$. To evaluate the effect of C_c, we can still exploit the Miller approximation and use the previous results; the capacitance C_L now becomes

$$C'_L = C_L + C_c \tag{24}$$

and the capacitance C_1 has to be substituted by

$$C'_1 = C_1 + C_c\left(1 + \frac{g_{m9}}{G_o}\right) \approx C_c\frac{g_{m9}}{G_o} \tag{25}$$

The expression of the Gain Bandwidth product for the proposed amplifier can be easily derived by combining Equations (16) and (17) as follows:

$$GBW = A_0 \cdot \frac{G_0}{C_L} = \frac{1}{2}\frac{g_{mb_1} + g_{mb_3}}{g_{ds_1} + g_{ds_3}}\left(g_{m9} + g_{m8}\frac{g_{m5}}{g_{m7}}\right)\frac{1}{C_L} \tag{26}$$

A simple expression of the negative slew rate SR_- can be obtained by noting that, during the discharge of the load capacitor C_L, the amplifier exhibits a class A behaviour with a bias current given by $M \cdot I_{bias}$:

$$SR_- = \frac{M \cdot I_6}{C_L} \tag{27}$$

During the charge of the load capacitor C_L, the amplifier exhibits a class B behaviour (maximum current is only limited by the voltage swing at the gate of M_9), and a formula expressing the positive slew rate SR_+ can be obtained by using the equation for the subthreshold conduction of the MOS transistor [21] as follows:

$$SR_+ = \frac{I_{D_{0_9}} \cdot \exp\left(\frac{V_{DD}+|V_{SS}|-|V_{th}|}{n \cdot U_T}\right)}{C_L} \tag{28}$$

A theoretical analysis of offset and noise performance of the proposed amplifier is reported in the Appendix A.

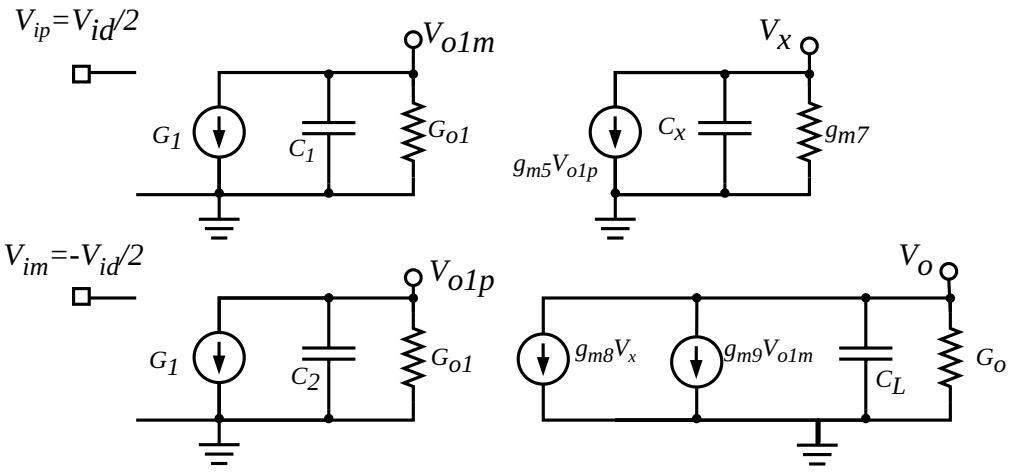


Figure 4. Simplified small-signal equivalent circuit of the amplifier after applying Miller approximation for frequency response computation.

4. Amplifier Design and Simulation Results

The proposed amplifier has been designed in a 130 nm CMOS technology from STMicroelectronics featuring a $|V_{th}| \approx 0.35\ V$.

4.1. Sizing

All the devices have been biased in the subthreshold region at $|V_{gs}| = |V_{ds}| = 150$ mV, and a dual supply of ± 0.15 V with $V_{DD} - V_{SS} = 2|V_{gs}|$ has been adopted. All the devices in the circuit have been sized with extremely long gates: this choice allows to minimize noise and increase the output resistance and the intrinsic gain of MOS devices as shown in [13]. The bias current of transistors in the input stage has been set to 5 nA as a tradeoff between power consumption and noise performance. For what concerns the second stage, simulations have shown that a design maximizing the CMRR according to (10) is very sensitive not only to mismatches but also to PVT variations; the stage has thus been

optimized to provide good CMRR performance in the different PVT conditions by means of a design centering approach.

To minimize power consumption, a 4 nA bias current has been adopted for the second stage. Even if this current is lower than the bias current of the first stage, the amplifier can still be efficiently compensated because the body driven input stage has a much lower transconductance than the second stage. A load capacitance C_L of 50 pF has been assumed and a compensation capacitor C_c of 1.2 pF has been added to provide an adequate phase margin. Table 1 reports sizing, bias current, and small signal parameters for all the devices.

Table 1. Nominal transconductance, sizing and output resistance of transistors.

	W [µm]	**L [µm]**	**I_D [nA]**	**g_m [nS]**	**g_{mb} [nS]**	**r_{ds} [GΩ]**
M_1,M_2,M_{b6}, M_{b7}	6.63	10	5	152.1	25.44	1.864
M_3,M_4,M_{b2},M_{b3},M_{b4},M_{b5}	0.9	10	5	131.8	23.68	0.667
M_{b1}	6.63	10	10	304.3	50.89	0.932
M_6	20	7.53	4	121.8	20.78	2.229
M_9	10	7.53	4	121.8	20.78	0.037
M_5,M_7	0.73	10	2	55.65	50.89	0.93
M_8	1.47	10	4	111.3	23.5	0.85

4.2. Simulation Results

The circuit has been simulated in the Cadence Virtuoso environment to test both open-loop and closed-loop performance. Figure 5 reports the magnitude and phase of the open-loop differential gain: a 64.6 dB dc gain with a 3.58 kHz unity gain frequency and a phase margin of about 54° are achieved in typical conditions. The amplifier has been simulated in a unity-gain buffer configuration to test closed-loop performance. Figure 6a shows the dc input-output characteristic of the buffer, highlighting a rail-to-rail output swing. The bias control loop is able to keep the common mode current of the input stage constant under input common mode variations, as shown in Figure 6b, thus improving common mode rejection and linearity. The CMRR is approximately 61 dB as shown in Figure 7. Supply rejection is around 27 dB, and the amplifier power dissipation is only 11.4 nW.

The slew rate has been evaluated simulating the response to a full swing (300 mV_{pp}) input step, shown in Figure 8: The positive slew rate is 1.7 V/ms, whereas a much lower negative slew rate of 0.14 V/ms is achieved, limited by the current source M_6. Total harmonic distortion (THD) for a 300 mV_{pp} input signal at 10 Hz is 0.84%. To give more detailed informations about linearity performance, the THD versus the peak-to-peak input voltage is shown In Figure 9a, whereas the differential voltage gain (in dB) as a function of the input common mode voltage is reported in Figure 9b to demonstrate the almost rail to rail input voltage range of the proposed amplifier. Finally the equivalent input referred noise is depicted in Figure 10 showing a spot noise at 100 Hz of about 2.69 $\mu V/\sqrt{Hz}$.

An area footprint of the amplifier of about 0.0064 mm^2 has been estimanted by using the Cadence Layout XL tool.

To assess the robustness of the proposed design, PVT and Monte-Carlo simulations have been carried out. Table 2 reports the simulated performance under different process corners, highlighting a very good stability of the amplifier performance. The amplifier's robustness has been tested also under supply voltage and temperature variations. Main amplifier parameters under supply voltage variations from 0.24 to 0.36 V are reported in Table 3, whereas simulation results under temperature variations in the range from −10 °C to 110 °C are shown in Table 4.

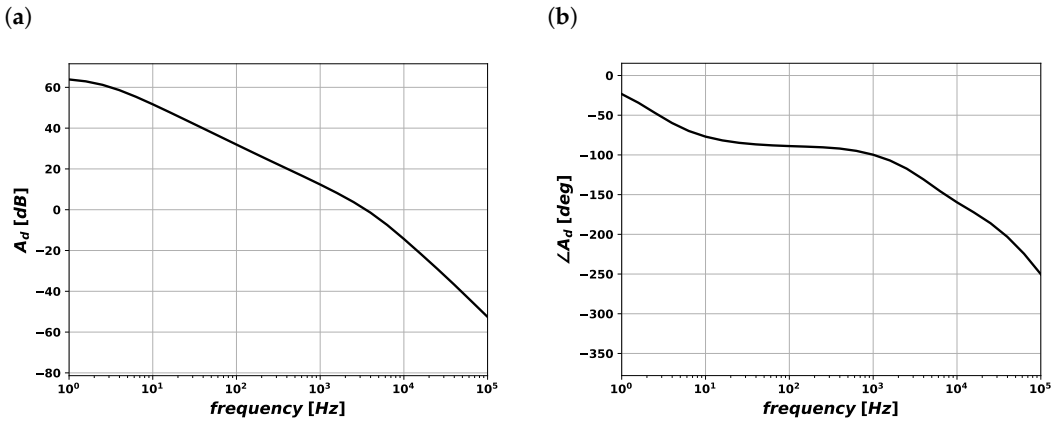


Figure 5. Open-loop differential gain frequency response: magnitude (**a**) and phase (**b**).

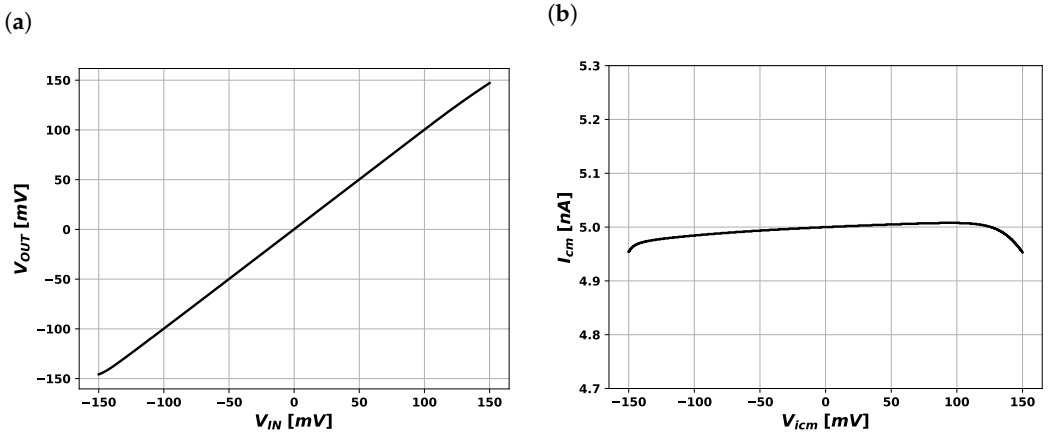


Figure 6. DC transfer charachterisitc (**a**) and DC bias current of the input stage vs. input common mode voltage (**b**).

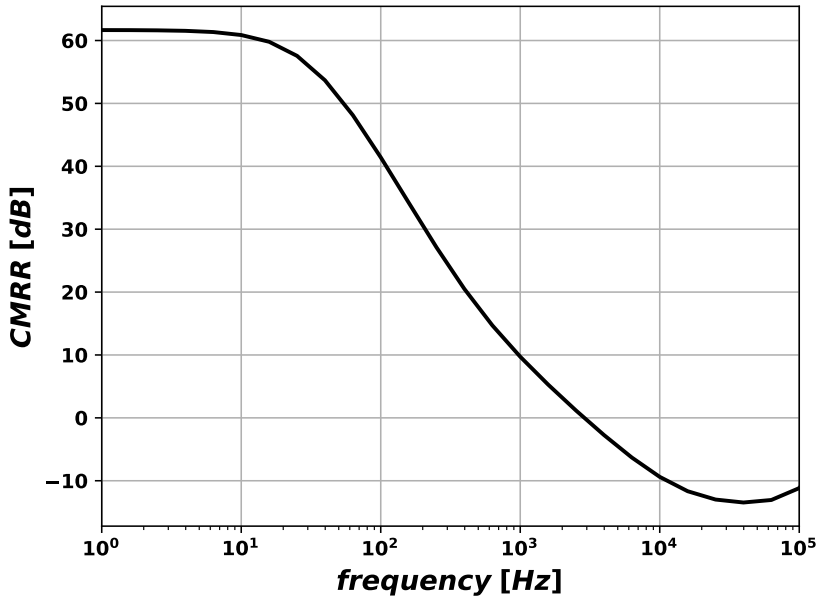


Figure 7. Magnitude of common mode rejection ratio (CMRR).

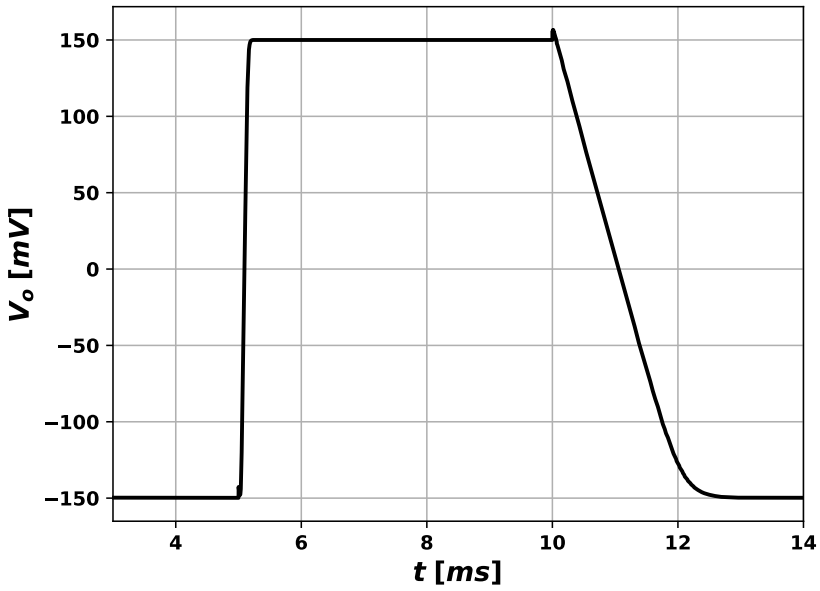


Figure 8. Response to a full swing input step.

(**a**) (**b**)

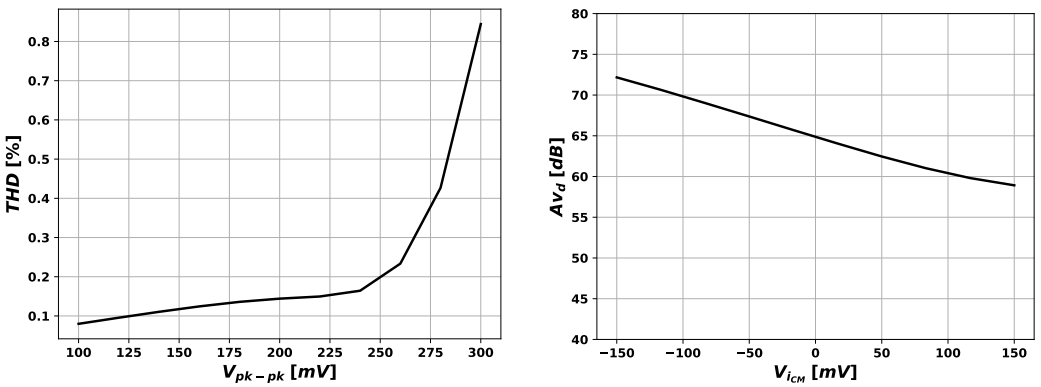


Figure 9. Total harmonic distortion (THD) vs. input signal amplitude (**a**) and differential gain vs. input common mode voltage (**b**).

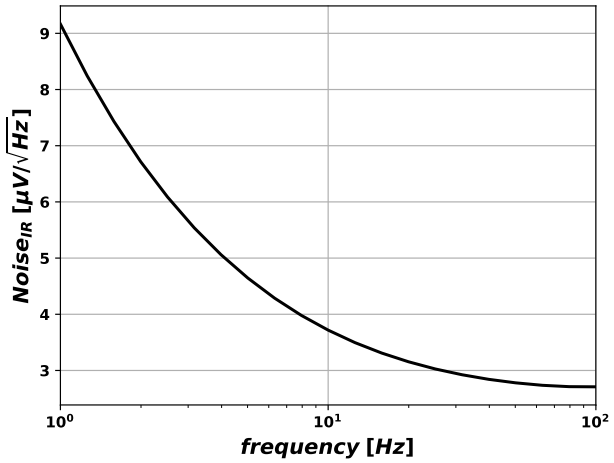


Figure 10. Equivalent input noise.

Table 2. Amplifier performance for different process corners.

	TT	**SS**	**FF**	**SF**	**FS**
$Gain\ [dB]$	64.60	59.85	68.83	64.96	62.90
$GBW\ [kHz]$	3.58	2.56	4.15	3.59	3.18
$m\varphi\ [deg]$	53.76	59.04	45.77	52.22	60.98
$CMRR\ [dB]$	61	59.83	67.51	65.02	62.85
$PSRR_+/PSRR_-\ [dB]$	26/28	23/26	28/29	27/28	24/26
$SR_+/SR_-\ [V/ms]$	1.7/0.15	1.19/0.15	2.31/0.15	2.46/0.15	1.09/0.15
$SR_{AVG};[V/ms]$	≈0.93	≈0.67	≈1.23	≈1.31	≈0.62
$noise\ [\mu V/\sqrt{Hz}]$	0.76	0.71	0.78	0.77	0.74
$P_{DISS}\ [nW]$	10.9	11.8	10.95	9.9	11.36

Table 3. Amplifier performance vs. supply voltage $V_{DD} - V_{SS}$.

$V_{DD} - V_{SS}[V]$	0.24	0.26	0.28	0.3	0.32	0.34	0.36
$Gain[dB]$	41.8	50.06	57.71	64.6	70.71	75.96	80.05
$GBW[kHz]$	1.05	1.78	2.5	3.58	4.42	4.86	4.92
$m\varphi\ [deg]$	71.47	66.75	64.27	53.76	40.97	31.91	29.02
$SR_+[V/ms]$	0.54	0.86	1.27	1.7	2.03	2.18	2.18
$SR_-[V/ms]$	0.14	0.14	0.15	0.15	0.15	0.15	0.15

Table 4. Amplifier performance vs. temperature.

$T[C]$	-10	0	27	50	80	110
$Gain[dB]$	55.05	57.76	64.6	67.51	61.36	50.07
$GBW[kHz]$	1.87	2.228	3.58	3.89	2.49	1.159
$m\varphi\ [deg]$	59.74	61.06	53.76	48.45	67.84	83.52
$SR_+[V/ms]$	1.11	1.28	1.7	1.96	2.16	2.29
$SR_-[V/ms]$	0.14	0.15	0.15	0.15	0.14	0.13
$Pdiss[nW]$	12.0	11.9	9.9	10.9	11.1	11.96

Monte-Carlo simulations have been performed to evaluate the effect of mismatches; Table 5 reports mean values and standard deviations of the main performance parameters for a 200-run Monte-Carlo mismatch simulation, highlighting a good stability.

Table 5. Monte Carlo simulations.

	Mean	**Std_dev**
$Gain[dB]$	65.48	7.43
$GBW[kHz]$	2.33	1.21
$m\varphi[deg]$	50.14	13.7
$CMRR[dB]$	46.5	10.7
$SR_+[V/ms]$	2.51	0.062
$SR_-[V/ms]$	0.183	0.006
$Pdiss[nW]$	11.35	0.831
V_{offset} [mV]	2.91	5.01

4.3. Results and Comparision

Table 6 compares the simulated performance of the proposed amplifier with other ULV, ULP implementations from the literature. In order to compare the performance of several different designs, we have considered the usually adopted four figures of merit (FOMs) defined as follows:

$$FOM_1 = \frac{GBW \cdot C_L}{I_{TOT}} \tag{29}$$

$$FOM_2 = \frac{SR_{AVG} \cdot C_L}{I_{TOT}} \tag{30}$$

$$FOM_3 = \frac{GBW \cdot C_L}{P_{DISS}} \tag{31}$$

$$FOM_4 = \frac{SR_{AVG} \cdot C_L}{P_{DISS}} \tag{32}$$

$$FOM_{4_{WC}} = \frac{SR_{WC} \cdot C_L}{P_{DISS}} \tag{33}$$

where the large signal FOM_4 has been computed both referring to the average slew rate and to the worst case one ($FOM_{4_{WC}}$). The comparison in Table 6 shows the effectiveness of the proposed approach: Extremely high values of the small signal FOMs (FOM_1 and FOM_3) are achieved. FOM_3 is particularly high thanks to the adoption of an extremely low supply voltage. This result is due to the combination of an Arbel-type approach, that doubles the gain of the first stage and thus the GBW product, and a dual-path second stage that allows achieving stability without sacrificing the bandwidth. Similar values of the small signal FOMs are obtained only by [22], that however uses a higher supply voltage, resulting in a lower FOM_3, and [18]. This latter however is a single-stage amplifier with limited input common mode range and which provides a much lower gain, and is biased at an extremely low current; no additional circuit is used to stabilize the dc current, that therefore presents large variations in PVT conditions. The proposed amplifier has not been optimized for large signal performance, and the negative slew rate is limited by the bias current set by M_6 resulting in a limited value for the worst case large signal $FOM_{4_{WC}}$. If we consider the average slew rate for the computation of the large signal FOM_4, the obtained values are comparable with state-of-the-art class-A amplifiers. Much better FOM_4 is achieved only by [12,13] that present a class-AB behavior.

Table 6. Comparison with ultralow voltage (ULV) state of the art amplifiers.

	This Work	[13]	[18]	[22]	[12]	[23]	[14]	[10]	[9]	[8]
Year	2021	2020	2020	2020	2018	2018	2015	2014	2014	2007
Technology $[\mu m]$	0.13	0.18	0.18	0.18	0.18	0.04	0.065	0.18	0.13	0.35
V_{DD} $[V]$	0.3	0.3	0.3	0.5	0.3	0.6	0.35	0.5	0.25	0.6
V_{DD}/V_{TH} $[V]$	0.86	0.6	0.6	1.19	0.6	1.27	1.16	1.29	1.16	1.02
DC_{gain} $[dB]$	64.6	64.7	39	69.5	65.8	41.35	43	70	60	69.4
C_L $[pF]$	50	30	10	15	20	5	3	30	15	15
GBW $[kHz]$	3.58	2.96	0.9	36	2.78	8260	3600	18	1.88	11.3
$m\varphi$ $[deg]$	53.76	52	90	65	61	86.6	56	55	52.5	65
SR_+ $[V/ms]$	1.7	1.9	-	9.7	6.44	844	5600	3	0.64	14.6
SR_- $[V/ms]$	0.15	6.4	-	9.7	7.8	844	5600	3	0.77	14.6
SR_{avg} $[V/ms]$	0.93	4.15	-	9.7	7.12	844	5600	3	0.71	14.6
$CMRR$ $[dB]$	61	110	30	90	72	52	46	-	-	75
$spot-noise$ $[\mu V/\sqrt{Hz}]$	2.69	1.6	0.81	0.91	1.85	-	0.93	0.31	3.3	0.29
@freq	100	-	1000	1000	36	-	-	1000	100	1000
$Power$ $[nW]$	11.4	12.6	0.6	60	15.4	15,735	17,000	75	18	548
$Mode$	BD	BD	GD	BD	BD	GD	BD	GD	BD	BD
FOM_1 $[MHz \cdot pF/mA]$	4711	2114	4500	4500	1083	1575	223	3600	392	186
FOM_2 $[V \cdot pF/(\mu s \cdot mA)]$	1224	2964	-	1213	2790	161	346	680	146	240
FOM_3 $[MHz \cdot pF/mW]$	15,702	7047	15,000	9000	3610	2625	635	7200	1568	311
FOM_4 $[V \cdot pF/(\mu s \cdot mW)]$	4079	9880	-	2425	9247	268	988	1200	587	400
$FOM_{4_{WC}}$ $[V \cdot pF/(\mu s \cdot mW)]$	658	4524	-	2425	8364	268	988	1200	583	400
$Area$ $[mm^2]$	0.0064	0.0085	0.00047	0.0034	0.0082	-	0.0050	0.057	0.083	0.06

5. Conclusions

In this paper, we have proposed an ultralow voltage Amplifier operating at 0.3 V supply voltage. The Arbel (differential inverter) approach and a dual-path differential-to-single-ended second stage are exploited to achieve 64.6 dB gain with high CMRR and an extremely high efficiency, resulting in an unity-gain frequency of about 3.6 kHz for a 50 pF load with a power consumption of only 11.4 nW. A replica-based bias control loop and a common-mode feed-forward approach are exploited to set the bias current and the output common mode voltage of the input stage, thus allowing a high robustness against PVT and mismatch variations. Comparison against the state of the art has shown that the proposed amplifier outperforms all the previously published Amplifiers in terms of the small signal figures of merit, while guaranteeing a very good tradeoff between noise, power consumption, area footprint, gain and CMRR.

Author Contributions: Conceptualization, R.D.S.; methodology, F.C., R.D.S. and G.S.; software, R.D.S. validation, F.C., R.D.S. and G.S., A.T.; formal analysis, F.C.; investigation, F.C., R.D.S. and G.S.; resources, A.T.; writing—original draft preparation, R.D.S.; writing—review and editing, F.C., G.S. and A.T.; supervision G.S.; funding acquisition, A.T. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Conflicts of Interest: The authors declare no conflicts of interest.

Appendix A

Appendix A.1. CMFF Analysis

The *CMFF* circuit can be analyzed with reference to Figure 3 and exploiting the equation for the subthreshold conduction of the MOS transistor [21]:

$$I_d = I_{D_0} \exp\left(\frac{V_{gs} - V_{th}}{nU_T}\right)\left[1 - \exp\left(\frac{-V_{ds}}{U_T}\right)\right] \tag{A1}$$

where

$$U_T = \frac{kT}{q} \tag{A2}$$

is the thermal voltage. We assume balanced supply voltage $\pm V_{DD}$, and no input common mode signal, so that $V_{ic} = 0$.

The analysis of the leftmost branch of the circuit provides

$$I_{ref} = I_{D_{0_n}} \frac{W_{b_2}}{L_{b_2}} \exp\left(\frac{V_B + V_{DD} - V_{Th_n}}{nU_T}\right)\left[1 - \exp\left(-\frac{V_B + V_{DD}}{U_T}\right)\right] \tag{A3}$$

Let I_1 the current flowing in M_{b_4}: an expression for I_1 similar to (A3) can be written, but now $V_{ds} = V_A + V_{DD}$. By exploiting Taylor expansion, the ratio between I_1 and I_{bias} can now be expressed as

$$\frac{I_1}{I_{bias}} = \frac{1 + \exp\left(\frac{V_A + V_{DD}}{U_T}\right)}{1 + \exp\left(\frac{V_B + V_{DD}}{U_T}\right)} \approx 1 + \frac{V_A - V_B}{U_T} \tag{A4}$$

The voltage V_A is set by M_{b_6}, since it results

$$I_1 = I_{D_{0_p}} \frac{W_{b_6}}{L_{b_6}} \exp\left(\frac{V_{DD} - V_A - V_{Th_p}}{nU_T}\right)\left[1 - \exp\left(-\frac{V_{DD} - V_A}{U_T}\right)\right] \tag{A5}$$

V_A and V_B are applied to the gates of M_1 and M_3, respectively; the currents of M_1 and M_3 can be derived by exploiting the same approximation in (**??**) as

$$I_{M1} = I_1\left(1 + \frac{V_A - V_o}{U_T}\right) \approx I_{ref}\left(1 + \frac{V_A - V_B}{U_T}\right)\left(1 + \frac{V_A - V_o}{U_T}\right) \tag{A6}$$

$$I_{M_3} = I_{bias}\left(1 + \frac{V_o - V_B}{U_T}\right) \tag{A7}$$

By imposing $I_{M_1} = I_{M_3}$ we obtain $V_o = V_A$.

Appendix A.2. Offset Analysis

The random offset of the proposed amplifier is mostly due to the mismatches of the devices in the input stage. The sub-threshold current equation can be rewritten as

$$I_a = I_{0_a} \exp\left(\frac{V_{ov_a}}{n_x U_T}\right) \tag{A8}$$

where

$$V_{ov_a} = \begin{cases} V_N + V_{DD} - V_{th_N}\left(V_{B_N} + V_{DD}\right) & a = N_1, N_2 \qquad x = n \\ V_{DD} - V_P - V_{th_P}\left(V_{DD} - V_{B_P}\right) & a = P_1, P_2 \qquad x = p \end{cases} \tag{A9}$$

and the effect of the drain-source voltage is neglected. We can assume the difference in the threshold voltages (hence in the overdrive voltages) as the main source of mismatch [13]. Considering the pair of NMOS (PMOS) devices, their overdrive voltages can be written as

$$V_{ov_a} = V_{ov_{0_x}} + \Delta_x/2 \tag{A10}$$

where x = n,p. Under the hypothesys of infinite CMRR (given by (10)), The input offset voltage can be calculated as the differential output voltage due to the overdrive mismatch divided by Ad1; since mismatches for NMOS and PMOS devices are uncorrelated, we get

$$\begin{aligned} V_{os} &= \frac{\sqrt{\left(\Delta_n/n_n\right)^2 + \left(\Delta_p/n_p\right)^2}}{\frac{n_n-1}{n_n} + \frac{n_p-1}{n_p}} = \\ &= \frac{\sqrt{n_p^2\Delta_n^2 + n_p^2\Delta_p^2}}{2n_n n_p - n_n - n_p} \end{aligned} \tag{A11}$$

Appendix A.3. Noise Analysis

We can assume that the main noise contributors are the channel noise currents of the devices in the input pair; noise in the second stage can be neglected, thanks to the gain of the first stage, and noise in the biasing circuit does not affect the output under the hypothesys of infinite CMRR. Noise sources in the MOS devices M1–M4 are uncorrelated, thus the equivalent input noise spectrum can be written as

$$S_{V_{eq}} = \frac{\overline{i_{d_1}^2} + \overline{i_{d_2}^2} + \overline{i_{d_3}^2} + \overline{i_{d_3}^2}}{2\left(g_{mb_n} + g_{mb_p}\right)^2} \tag{A12}$$

(we have exploited (10) to simplify the expression). The noise spectral density for each transistor can be written as

$$\overline{i_{nd}^2} = \overline{i_{nT}^2} + \overline{i_{n\frac{1}{f}}^2} \tag{A13}$$

where

$$\overline{i_{nT}^2} = 4kTn\gamma g_m \approx 2qI_D \tag{A14}$$

is the thermal noise contribution and

$$\overline{i_{n\frac{1}{f}}^2} = \frac{k}{fC_{ox}}\frac{g_m^2}{WL} \tag{A15}$$

is the flicker noise. Substituting (A14) and (A15) into (A13) we get

$$\frac{2qI_{bias} + \frac{1}{fC_{ox}}\left(\frac{k_n g_{m_n}^2}{W_n L_n} + \frac{k_p g_{m_p}^2}{W_p L_p}\right)}{\left(g_{mb_n} + g_{mb_p}\right)^2} \tag{A16}$$

References

1. Harpe, P.; Gao, H.; Van Dommele R.; Cantatore, E.; Van Roermund A.H.M. A 0.20 mm^2 3 nW signal acquisition IC for miniature sensor nodes in 65 nm CMOS. *IEEE J. Solid State Circuits* **2016**, *51*, 240–248.
2. Toledo, P.; Crovetti, P.; Klimach, H.; Bampi, S. A 300-mV supply, 2 nW-power, 80 pF-load CMOS digital-based OTA for IoT interfaces. In Proceedings of the 2019 International Conference on Electronics, Circuits and Systems (ICECS), Genova, Italy, 27–29 November 2019; pp. 170–173.
3. Della Sala, R.; Monsurrò, P.; Scotti, G.; Trifiletti, A. Area-efficient low-power bandpass Gm-C filter for epileptic seizure detection in 130 nm CMOS. In Proceedings of the 2019 International Conference on Electronics, Circuits and Systems (ICECS), Genova, Italy, 27–29 November 2019; pp. 298–301.
4. Liu, Z.; Tan, Y.; Li, H.; Jiang, H.; Liu, J.; Liao, H. A 0.5-V 3.69-nW complementary source-follower-C based low-pass filter for wearable biomedical applications. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2020**, *67*, 4370–4381.
5. Grasso, A.D.; Marano, D.; Palumbo, G.; Pennisi, S. Design methodology of subthreshold three-stage CMOS OTAs suitable for ultra-low-power low-area and high driving capability. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2015**, *62*, 1453–1462.
6. Centurelli, F.; Fava, A.; Olivieri, M.; Tommasino, P.; Trifiletti, A. A low-voltage class-AB OTA exploiting adaptive biasing. *Int. J. Electron. Commun. (AEU)* **2020**, *122*, 153282.
7. Algueta Miguel, J.M.; Lopez-Martin, A.J.; Acosta, L.; Ramirez-Angulo, J.; Gonzalez Carvajal, R. Using floating gate and quasi floating-gate techniques for rail-to-rail tunable CMOS transconductor design. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2011**, *58*, 1604–1614.
8. Ferreira, L.H.C.; Pimenta, T.C.; Moreno, L.R. An ultra-low-voltage ultra-low-power CMOS Miller OTA with rail-to-rail input/output swing. *IEEE Trans. Circuits Syst. II Express Briefs* **2007**, *54*, 843–847.
9. Ferreira, L.H.C.; Sonkusale, S.R. A 60-dB gain OTA operating at 0.25-V power supply in 130-nm digital CMOS process. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2014**, *61*, 1609–1617.
10. Magnelli, L.; Amoroso, F.A.; Crupi, F.; Cappuccino, G.; Iannaccone, G. Design of a 75-nW, 0.5-V subthreshold complementary metal-oxide-semiconductor operational amplifier. *Int. J. Circuit Theory Appl.* **2014**, *42*, 967–977.
11. Cabrera-Bernal, E.; Pennisi, S.; Grasso, A.D.; Torralba, A.; Gonzalez Carvajal, R. 0.7-V three-stage class-AB CMOS operational transconductance amplifier. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2016**, *63*, 1807–1815.
12. Kulej, T.; Khateb, F. Design and implementation of sub 0.5-V OTAs in 0.18-µm CMOS. *Int. J. Circuit Theory Appl.* **2018**, *46*, 1129–1143.
13. Kulej, T.; Khateb, F. A compact 0.3-V class AB bulk-driven OTA. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2020**, *28*, 224–232.
14. Abdelfattah, O.; Roberts, G.W.; Shih, I.; Shih, Y.-C. An ultra-low-voltage CMOS process-insensitive self-biased OTA with rail-to-rail input range. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2015**, *62*, 2380–2390.
15. Ruscio, D.; Centurelli, F.; Monsurrò, P.; Trifiletti, A. Reconfigurable low voltage inverter-based sample-and-hold amplifier. In Proceedings of the 2017 Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), Giardini Naxos, Taormina, Italy, 12–15 June 2017; pp. 133–136.
16. Braga, R.A.S.; Ferreira, L.H.C.; Coletta, G.D.; Dutra, O.O. A 0.25-V calibration-less inverter-based OTA for low-frequency Gm-C applications. *Microelectron. J.* **2019**, *83*, 62–72.
17. Baghtash, H.F. A 0.4 V, tail-less, fully differential trans-conductance amplifier: An all-inverter-based stracture. *Analog Integr. Circuits Signal Process.* **2020**, *104*, 1–15.

18. Rodavalho, L.H.; Aiello, O.; Ramos Rodriguez, A. Ultra-low-voltage inverter-based operational transconductance amplifiers with voltage gain enhancement by improved composite transistors. *MDPI Electron.* **2020**, *9*, 1410.
19. Arbel, A.F.; Goldminz, L. Output stage for current-mode feedback amplifiers, theory and applications. *Analog Integr. Circuits Signal Process.* **1992**, *2*, 234–255.
20. Grasso, A.D.; Pennisi, S.; Scotti, G.; Trifiletti, A. 0.9-V Class-AB Miller OTA in 0.35- μm CMOS with Threshold-Lowered Non-Tailed Differential Pair. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2017**, *64*, 1740–1747.
21. Fjeldly, T.A.; Shur, M. Threshold voltage modeling and subthreshold regime of operation of short-channel MOSFET's. *IEEE Trans. Electron Devices* **1993**, *40*, 137–145.
22. Deo, N.; Sharan, T. ; Dubey, T. Subthreshold biased enhanced bulk-driven double recycling current mirror OTA. Analog Integrated Circuits and Signal Processing. *Analog Integr. Circuits Signal Process.* **2020**, *105*, 229–242.
23. Centurelli, F.; Monsurrò, P.; Parisi, G.; Tommasino, P.; Trifiletti, A. A 0.6 V class-AB rail-to-rail CMOS OTA exploiting threshold lowering. *IET Electron. Lett.* **2018**, *54*, 930–931.