Image stitching algorithm for description of integrated circuit layouts

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Abstract: *The problem of optimum matching of partially overlapped frames of an image is formulated with use of common criteria of matching quality. The image stitching algorithm based on key points matching is proposed for quasi-optimal solution of the problem with the following restrictions: the frames are rectangular and have an identical scale. It was implemented as a software module in the system of integrated circuit layout analyses.*

***Keywords*:** Integrated circuit, layout, matching, stitching algorithm.

1. INTRODUCTION

Control and rapid analysis of the very large-scale integrated circuits (VLSI) layout is an important process in the integrated circuits (ICs) industry. Optical inspection can give important data about the layout state. Therefore, VLSI production is impossible without computer vision systems equipped with special software for automatic analysis. A large amount of data (up to 30 or more layouts, each layout is represented as a set of frames), the resolution on the verge of an optical wavelength, the complex nature of the interference (violation of the geometry, brightness distortion, violation positioning) significantly define the specificity of the data processed in the computer vision system.

The main initial data for ICs analyses are layout images, which may be prepared by standard or special equipment and devices for digital imaging and VLSI topological layers provided in the form of one or more image fragments. The fragments (frames) of the image layout are rectangular and they overlap on each other (dimensions of overlapping are known).

The images have taken by a single camera but at different time instants or different light. There are some misplacement due to effect of perspective distortion or blurring occurs when object is out of focus on boundaries or object is vary in height.

The main principle of the picture areas matching is based on correlation of the areas in the overlapping region. There are two approaches to extending correlation to include wider ranges of distortions. One method is to successively distort and correlate a reference template across a full range of distortions. Classical technique of correlation and relaxation is used to find an initial set of matches, and then a robust technique of the Least Median of Squares is used to discard false matches in this set. It is computationally very expensive. The algorithm calculates the squared difference per pixel of all possible overlaps between two adjacent images and selects the minimum. Using special transformations of initial images it is possible to speed up correlation [1, 2].

Another approach is that of composite filtering, where a single filter responds to a full range of distortions. Good technique for matching involves Fourier autocorrelation. This technique replaces convolution-based template matching by Fourier transforming the source and template images, multiplying one by the complex conjugate of the other, then inverse Fourier transforming the result. The result should ideally provide a single peak at the single point of correlation.

Widely a method is used when for matching some overlap regions those are smaller, than the real matching region should be, are used.

For each of this approaches it is possible to use parallel matching algorithm to performance of calculation process. First some adjacent images select. Then, it iterates over all possible overlaps of these images and calculates (in parallel) the sum of the differences between each pixel in the overlapping regions.

The main attention is paid to strategies for finding near-optimal matching algorithms. They are very important to reduce a computational complexity of matching

We discuss the problem in following two applications: wafer production and printed circuit boards inspection. The images are calibrated i.e. with known intrinsic parameters (have the same value of pixels). They are only rectangle images (Fig. 1), there are no rotations, that's way any overlapping areas are rectangles too.

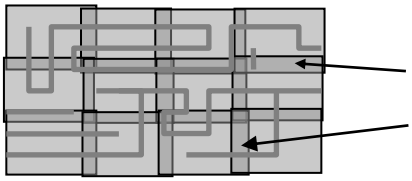


Fig.1 – Example of VLSI metallization layer.

Here we describe algorithm that allows to reduce a time complexity of stitching. The optimization stitching problem is formulated by the use common criteria of matching. An algorithm is proposed, that give us near optimal solutions for frames matching.

We can state the matching problem as follows. There is an image in the form of matrix $[P_{i,j}]$ of the bitmap picture frames of dimension n x n.

Lets $G = (N,R)$ be undirected adjacency graph of the picture areas were two areas are only vertical or horizontal adjacent. $N = \{ n_{i,j},\ i = \overline{1...n},\ j = \overline{1...n} \}$ is the set of the graph nodes. $R = \{ r_i,\ i = 1,2,...,2(n-1)n \}$ is the set of edges.

Define S_h and S_v as the size of adjacent frames overlap horizontally and vertically, respectively, as well as the tolerance of overlap horizontally and vertically Δh and Δv. Let $\Delta h < S_h$, $\Delta v < S_v$.

The similarity function of two picture areas P_1 and P_2 is the discrete distance function $d(P_1,P_2,h,v)$ where h and

v are the picture areas horizontal and vertical shifts of P_2 relative to P_1, $-\Delta h \le h \le \Delta h$, $-\Delta v \le v \le \Delta v$. Lets $d(r_i, h, v) = d(P_1, P_2, h, v)$ be the function of distance in some metric: Euclidean or angular (correlation function similarity), where r_i is the edge of graph G that defines vicinity of P_1 and P_2.

The best position of two neighbor pictures relative to each other is the position where d has minimal value.

So the goal function is defined as following

$$g = \sum_{i=1}^{2mn-m-n} d(r_i,h,v) \to \min. \qquad (1)$$

The task is to find the optimal pictures coordinates that value of the function g is minimal.

The trivial solution is the full search of all possible combinations of the overlapping. This is not acceptable because of big amount of the combinations $(2\Delta)^{2(n^2-1)}$. From this pint of view the algorithms that realize the restricted search are the best solution.

However, when the design rules smaller than 45 nm and we use modern scanning electron microscopes, difficulties arise in formation of complete or common image of VLSI layout, because the degree of circuit integration increases and the complexity of the topology also. Therefore, the development of new, more efficient algorithms for solving the problem of linking or stitching the frame layer circuit topology is relevant.

2. STITCHING ALGORITHM BY KEY POINTS

The stitching algorithm by key points consists of two phases:

1. Calculation offsets of the frames for the set of edges R of the graph G.
2. Correction of the location of the frames.

The first phase includes the following steps for each edge $r_i = (P_1, P_2)$ in the region of overlapping of two frames P_1 and P_2:

1. Search for key points and calculate their descriptors.
2. Mark the key points corresponding to each other
3. Remove false key points.
4. Calculate the offset of the frame P_2 in relation to the position *of* frame P_1.
5. Calculate the distance $d(P_1, P_2)$.
6. Calculate the weights of the edges as a weighted sum of the normalized number N_{ri} of the found points and normalized difference of the initial distance d_1 and the distance d_2 after displacement:

$$w_{r_i} = w_{kp}\frac{N_{r_i}}{N_{kp}} + w_d\frac{\left|d_{r_{i_1}} - d_{r_{i_2}}\right|}{d_{max}},$$

where, w_{kp} and w_d - the weights of the summands, N_{ri} – the number of the found key points for the edge r_i, N_{pi} - maximum allowable number of the key points (it is selected during setting up the algorithm, $d_{r_{i\,1}}$ and $d_{r_{i\,2}}$ - the initial value d_1 of the distance and the value d_2 after displacement for the edges r_i respectively, $d_{\max}$ - maximum possible difference of distance for the overlap region of the two frames P_1 and P_2.

The following algorithms for search of key points and description tags were tested: SIFT [3], SURF [4], ORB [5] and windowing method. The testing was conducted on data iW1696_Si_, with frame size 640×480 pixels, the size of overlapping area is 6×28, the total data size is 455,426 KB. The results are summarized in Table 1. You can see that SIFT algorithm show the lowest number of points for troubleshooting and high performance.

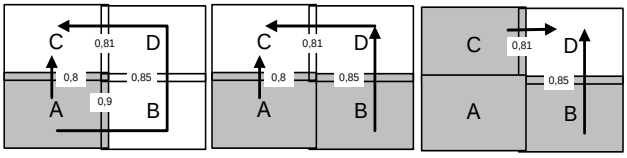
Table 1. Comparison of the performance and accuracy

Algorithm	Runtime,s	Accuracy,%
SIFT	47	96
SURF	52	79
ORB	45	76
Windowing	22	72

The weight of edger performs the role of quality control of the offset found for two frames. The more points, the more accurate and reliable calculation of offset for SIFT algorithms, the SURF and ORB. The more the second term, the best position for the second frame was found in relation to the original. The weights are adjusted terms on the basis of the analysis of the current image of IC, or are set to 0.5.

The complete image of VLSI layout is constructed on the basis of the set of edges R with respective offsets and weights: a route is searched along the edges from R that connect all the vertices N of the graph G with the maximum weights on one route. Further, the frames are shifted on the appropriate edges offsets. The search is performed for the four adjacent frames sequentially by rows.

There are three cases in the formation of the routs for four different frames (see Fig. 2.).



a) b) c)

Fig.2 – Possible roots with weight s of edges, the fixed frames are grey: a) one; b) - two; c) – three

1. One frame is fixed and it is searched for a route with a maximum weight of three adjacent frames. This case takes place one time for the first frame of matrix $[P_{i,j}]$ and its neighbors.
2. Two frame are fixed, either horizontally or vertically. It is searched a route with a maximum weight of two adjacent frames. Those cases take place for the frames of first row and first column of the matrix $[P_{i,j}]$.
3. Three frames are fixed and one of the two edges with a maximum weight is selected for the fourth of the frame. This case takes place for the remaining frames.

Further, any frame is fixed, if a route to it was found.

The work of the algorithm are illustrated on the example of the matrix of 30 frames. The initial weights of

the edges are shown between the neighboring frames on fig. 3.

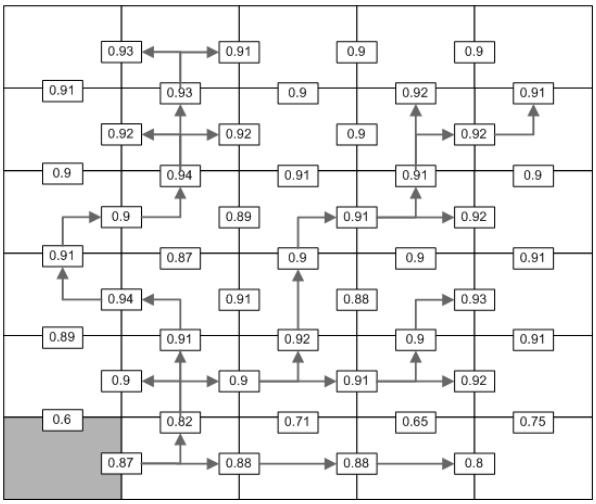


Fig.3 –Overlapping quality map with full route

The algorithm consists of the following steps:

1. The frame with index (0,0) is fixed in its current coordinates (frame A in Fig. 2).

2 The route from A is constructed beginning with the edge of the highest weight.

3. Fix the frames along the route and modify their coordinates.

4. The next frame in the line is processed (it is occupies the position of frame A in Fig. 2).

5. If the end of the line is reached, then move to the next line.

6. If there are no fixed frames, go to step 2.

7. End.

Thus formed the full route for construction complete or common image of VLSI layout by combining separated frames (Fig.4).

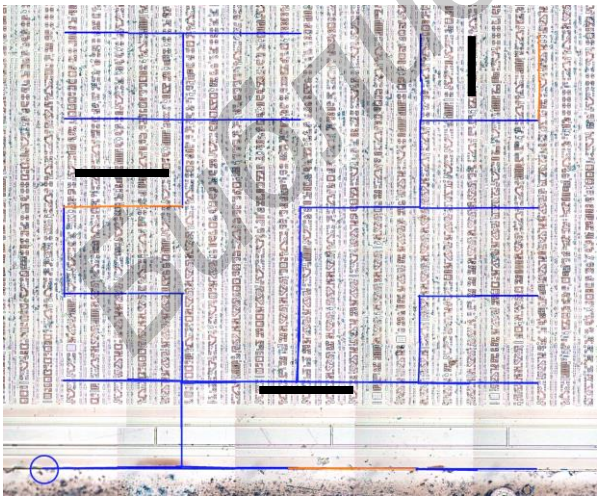


Fig.4 – Result layout and the full route of stitching

3. OPTIMIZATION ALGORITHM

Many frames require a lot of computation time for key point search and positioning each frame inside the common image.

Optimization is performed according to the following restrictions:

1. Search for frame offsets only in the overlapping of frames and small neighborhood of the overlapping (neighborhood size is smaller than the size of the overlapping).

2. There is no distortion of geometric characteristics for pattern matching on the frames.

According to these constraints stitching algorithm can be expanded by method of moving viewer (windowing). The idea of this method is based on searching the maximum correlation for template found on available for search area (Fig. 5). This serial comparison of the sample is carried out with the image at each point.

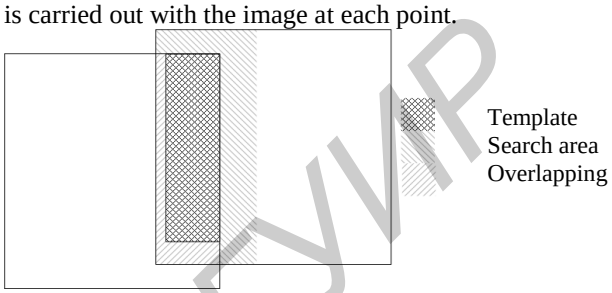


Fig.5 – Example of location of search area

In this way, the first stage of the algorithm is the following for all the neighboring frames in the overlapping:

1. Compute maximum correlation in the overlapping region of two frames.

2. If a single maximum is found, then go to step 6.

3. Search for key points and compute their descriptors.

4. Mark the key points corresponding to each other.

5. Mark a subset of the points with the maximum size and with the same offset parameters, the other points are discarded as false.

6. Compute the offset and the quality rank for the pairs of frames.

Testing proposed stitching algorithm showed that the maximum correlation was calculated double-quick than the calculation of descriptors and key points. At the same time, the correlation is correctly defined for 70-97 % frames depending on the input data.

4. CONCLUSION

The algorithm was implemented based on the OpenCV library, and on the basis of cross-platform Qt tools, this module is part of the software package for image data processing and analysis for VLSI manufacture. It performs the following tasks: construct complete image or common image of VLSI layout without distortion and provide viewer and specialized editor of VLSI layout with the possibility of scaling; pre-processing of images, brightness adjustment; identification of topology objects on VLSI layer image; automated library preparation of topology objects for identification; export result of layout object identification to the VLSI CAD Cadence.

By using of software implementation of stitching algorithm for layout frame of VLSI by key points to form a complete or common image of VLSI layout without distortion improve the quality of identification for control of technological processes of manufacturing of VLSI and improved the quality of designers work.

For large amounts of data, described algorithms are implemented using parallelization on the CPU and GPU by OpenMP, CUDA and / or OpenCL technologies.

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