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Development of fabrication processes toward integrated photonics in III-V semiconductors - GaP and GaN.

By

Geraint Paul Gough

April 2021

A dissertation submitted to the University of Bristol in accordance with the requirements for award of the degree of Doctor of Philosophy in the Faculty of Science.

Word count: 20103

Abstract

Quantum technologies are taking the next step in their evolution, from not just using quantum mechanical effects, but manipulating them to gain a quantum supremacy over their classical counterparts. Areas that will benefit from this quantum advantage are communications and security, simulations and sensing. The area this quantum supremacy is greatly anticipated is computing, with the dawn of the quantum computer promising quicker algorithms.

Superconducting and trapped ion qubits have shown significant promise for a quantum computer. However, with the vast industrial infrastructure available for Si integrated circuits, along with Si photonics' extensive history, a photonic quantum computer also shows promise. However, while Si does offer several useful properties for integrated photonics, it also has detrimental properties such as an indirect bandgap, centrosymmetric lattice structure and limited options for switching. Compound semiconductors offer beneficial properties like Si along with extra properties not available to Si (Pockels effect).

Simulations to find single mode waveguides in GaN and GaP, found waveguides with dimensions 1000 x 500 nm and 600 x 200 nm respectively. Single mode waveguides were found to avoid multimodal effects. With these waveguide dimensions, different switch designs were carried out where a MZI switch in a push-pull configuration was identified as the best design. Arm lengths of 8.4 mm and 11.4 mm for GaP and GaN respectively have a switching voltage of 4 V. The development of the fabrication process necessary to create these designs was done with the start of an etch matrix and lithographic tuning of designs. A novel angled cage etch was developed to create suspended GaN structures with singly and double clamped cantilevers created as well as experimenting with a conical cage. The goal is to create suspended photonic structures, the beginnings of which, a photonic nanobeam, are demonstrated.

Dedication and Acknowledgements

I would like to dedicate this thesis to everyone who has helped me get to this stage in my life and complete this thesis.

The main person I would like to thank is my fiancée Adelle who, without her, I would not be in this position. Without her support and encouragement throughout this PhD I would not be where I am today. I would also like to thank my son Hunter who has been a ray of light during this time and has been the inspiration I have needed to help me complete my thesis.

I would like to thank Daryl Beggs for all his time and support he has given me throughout my PhD. His expertise in photonics and fabrication have been invaluable in solving any issues I have faced with my thesis and helped me develop my knowledge and understanding to drive this thesis forward. I would like to thank Jorge Barreto for his support during this PhD. He has been my Bristol representative and helped with the organisation of things there in my absence.

I would also like to thank everyone at Cardiff University, especially all the cleanroom staff, for all the time and resources that have been made available to me and for also helping me develop the fabrication skills I have needed to develop my fabrication process. I would also like to thank everyone in Ser Cymru group for all the good times had during my time at Cardiff that helped me to settle into Cardiff University and make me feel a part of the group. Special thanks to Marie and Helen, who were there during the entirety of my time at Cardiff and made each day a fun day. Special acknowledgement to Anthony Bennett for his inclusion in the ACES project.

I would like to thank everyone at Bristol University for all the support that has been given. Special mentions to Martin Cryan and Krishna Balram who have gone above and beyond the APM supervisor role to help me with my thesis. Without whom, I may not have worked with GaN, which could have caused me to miss opportunities that would be beneficial to this thesis and their expertise with the material.

Author’s declaration

I declare that the work in this dissertation was carried out in accordance with the requirements of the University's *Regulations and Code of Practice for Research Degree Programmes* and that it has not been submitted for any other academic award. Except where indicated by specific reference in the text, the work is the candidate's own work. Work done in collaboration with, or with the assistance of, others, is indicated as such. Any views expressed in the dissertation are those of the author.

SIGNED: .... DATE:..........................

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Chapter 1

1 Introduction

We are now entering a new age of quantum devices that rely on quantum effects such as superposition and entanglement. These devices will supersede their classical counterparts due to their inherent quantum nature. There have already been demonstrations of this quantum supremacy in sensing [1]; security and communications [2]; and specialised quantum systems for quantum simulations [3], [4]. However, the pinnacle would be a quantum computer [5] capable of carrying out any quantum algorithm such as Shor's algorithm [6]. There are many obstacles that need to be surpassed, but there are many promising solutions and platforms available to achieve a universal quantum computer.

1.1 Quantum Computing

A quantum computer uses quantum bits, or qubits, that is a superposition state of both 1 and 0 with different probabilities:

$$|\Psi\rangle = \alpha\,|0\rangle + \beta\,|1\rangle \quad (1)$$

where α and β are the probability coefficients such that:

$$|\alpha|^2 + |\beta|^2 = 1 \qquad (2)$$

unlike a classical bit which is either in the 1 or 0 state.

In general, the generation, manipulation and measurement of these qubits are the three main operations any quantum computer will need to be able to do to carry out quantum algorithms. In its simplest form, like the Reck scheme [7] in Figure 1, a quantum computer consists of a source, a switching array and a readout; the Reck scheme is essentially a reconfigurable switching network. See Section 1.3 for a description of the Reck scheme.

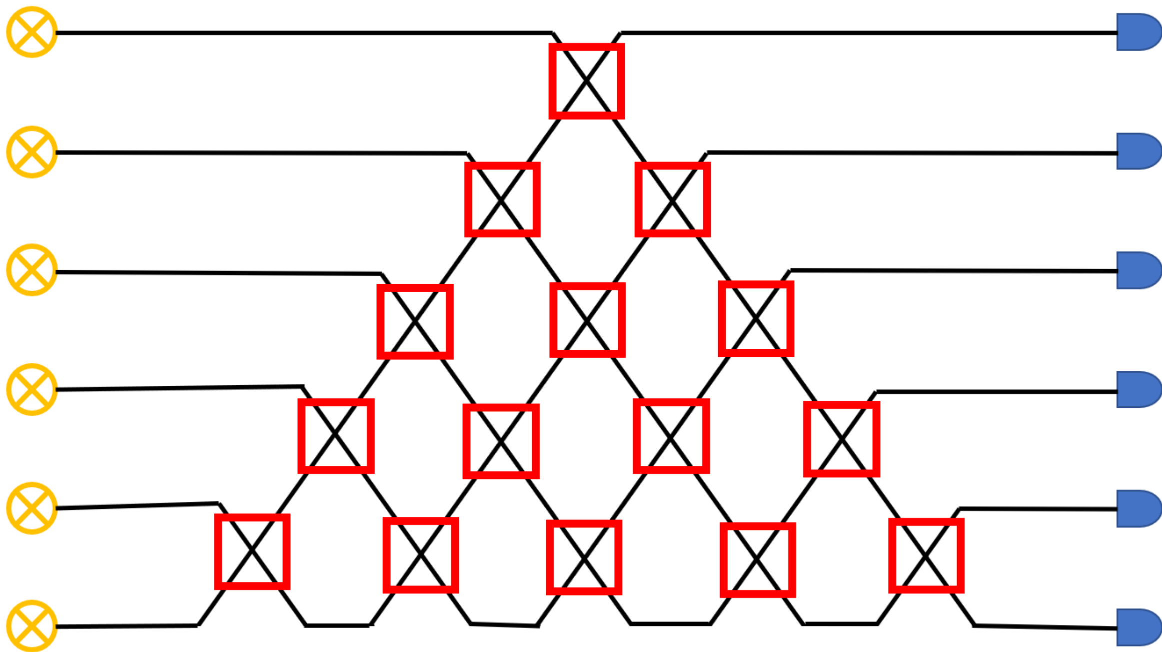


Figure 1: An example of a photonic universal quantum computer, the Reck scheme [7], *comprising of sources (yellow), switches (red) and detectors (blue) for readout.*

The sources generate qubits in a state ready to carry out an algorithm or to be initialised. For a source of entangled qubits, in a circuit this would be done by acting a CNOT gate on a superposition state created by performing a Hadamard gate (See Section 1.3 for gate descriptions). Physically this can be done by using spontaneous parametric down conversion sources [8] and entangling emitted photons of atoms [9] as well as other methods for different platforms [10], [11], [12].The qubits enter the quantum circuit made up of an array of switches or gates that can change the path or state of the qubit as required by the quantum algorithm. Once the quantum algorithm has been carried out the qubits need to be readout to give the final solution. Depending on the platform, each of these steps can either be easily achieved or have a range of challenges associated with it.

1.2 Quantum Computing Platforms

There have been many comparisons between the platforms available for quantum computing ([13], [14], [15]). Two such platforms are superconducting and trapped ion qubits.

Superconducting qubits come in many different forms: One of three fundamental qubits (a charge qubit [16], a flux qubit [17] or a phase qubit [18]) or different combinations of the three (transmons [19] being most notable). They have fast gate times (130 ns for single gate, between 250-450 ns for 2-qubit gate [20]) compared to trapped ion qubits and already have a mature technological fabrication base available to mass produce circuits. However, their short decoherence time (the time before external influences affect the quantum state, T_1 and T_2 ~ 60 μs [20]) and limited range of interaction (typically nearest neighbour between qubits) means intense error correction and extra operations will be required to carry out a

quantum algorithm. The main drawback for superconducting qubits is the extremely low temperature (around 100 mK) required for superconductivity to occur and these qubits to work. These require complicated and expensive cooling systems to reach this temperature.

On the other hand, trapped ion qubits can operate at room temperature, have excellent decoherence times ($T_1 = \infty, T_2 = 0.5$ s [20]), in comparison to superconducting qubits, and can interact with any other qubit in a circuit. While the optimal operation temperature is 4 K, which is still easier to achieve than their superconducting counterpart, they are required to be isolated in a vacuum, which requires an equally complicated system itself. They also have slower gate times in comparison (20 µs for single gate, 250 µs for two-qubit gate [20]) and the fabrication technology required to create these circuits still requires further development to be mass producible.

Another platform that can be used for quantum computing are photonic qubits. Photonic qubits have been referred to as the “ugly duckling” [21] of all the platforms proposed due to the probabilistic nature of some gates; to account for the probabilistic gates over 100 physical photons would be required to get one computational photonic qubit. However, it is possible to herald when a gate has been successful and determine when an algorithm has been carried out correctly. Heralding is where two photons are created such that one is detected (the signal photon) indicating the presence of the other (the idler photon) that continues in the circuit (See Section 2.2.2 a and b for more detail).

The reason the gates are probabilistic is the same reason why photons are also a great candidate for quantum computing. Photons interact weakly with their surroundings. However, because they interact weakly with their surroundings, they also interact weakly with other photons. This means getting interactions between photons relies on

intermediary processes which are probabilistic. This is important for 2 qubit gates where the state of the one qubit effects the state of another [22],[23]. Although the number of photons required to increase the likelihood of a gate working to near certainty is high, the number or auxiliary qubits required to carry out error correction codes is significantly higher, on the order of 10^8 [24]. Error correction codes come in many forms (find refs) but all enable fault tolerant quantum computing; if an external influence changes the state of a qubit (bit flip, phase flip) an auxiliary qubit entangled to the qubit can be measured to detect this and a correction made to the state. However, to account for any error, over all qubits, at any step in the algorithm requires a huge number of auxiliary qubits that are unable to be used again due to the measurement (See below).

Each of these platforms offers a quantum supremacy over a classical computer which is often compared when looking at factorising numbers. For a classical computer the general number field sieve (GNFS) [25] is the most efficient algorithm available for factorising large numbers, while its quantum counterpart is Shor's algorithm [6]. When an integer number of 375 bits is factorised, for the GNFS it would take approximately 2 hrs, for Shor's algorithm it would take < 1 s [26]. While this is a significant difference in time, for this to be a fault tolerant calculation (accounting for bit flips, phase flips, errors in the state generation and gate operations), the number of physical qubits required is high; [24] estimates to factorise a 2000 bit number, 4000 computational qubits are required, which equates to 220×10^6 physical qubits to generate the initial states and run the algorithm assuming an error rate of 1%.

1.3 Gate Model v Cluster Model

Quantum circuits discussed so far have been described via the gate model [5], where the algorithm a qubit follows is already predetermined without any alteration made during the qubits journey. These gates can be described in matrix form such as the X, Y and Z Pauli gates:

$$X = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} \quad Y = \begin{pmatrix} 0 & i \\ -i & 0 \end{pmatrix} \quad Z = \begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix}$$

The X and Z gate are commonly used in quantum algorithms as they are associated with a bit flip ($|0\rangle \rightarrow |1\rangle, |1\rangle \rightarrow |0\rangle$) or phase flip ($|1\rangle \rightarrow -|1\rangle$) respectively. For the Hadamard and the CNOT gate, discussed in Section 1.1, these are represented in matrix form:

$$H = \frac{1}{\sqrt{2}}\begin{pmatrix} 1 & 1 \\ 1 & -1 \end{pmatrix} \qquad CNOT = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{pmatrix}$$

The Reck scheme breaks down any N x N operation into multiple 2 x 2 operations described by a variable beamsplitter or switch and a phase shifter. For the Reck scheme [7] in Figure 1, the gates are already set corresponding to the operations to be acted on the state of the qubit. However, this relies on the gate operations being successful on the qubit. If the gate fails to be carried out the algorithm is carried out incorrectly and will give the wrong result.

A more robust method to probabilistic gates is measurement based quantum computing (MBQC) [27]. MBQC uses cluster states [28], a mass of qubits all entangled to each other, to perform a quantum algorithm by mapping the quantum circuit onto the cluster state via

measurements of qubits like Figure 2. The results of the measurements feed forward to determine the next set of measurements to be carried out depending if a corrective action is required to ensure the algorithm proceeds correctly; if the correct result is measured the algorithm carries on as normal, if the incorrect result is measured a correction can be made by measuring the next qubit in the appropriate basis.

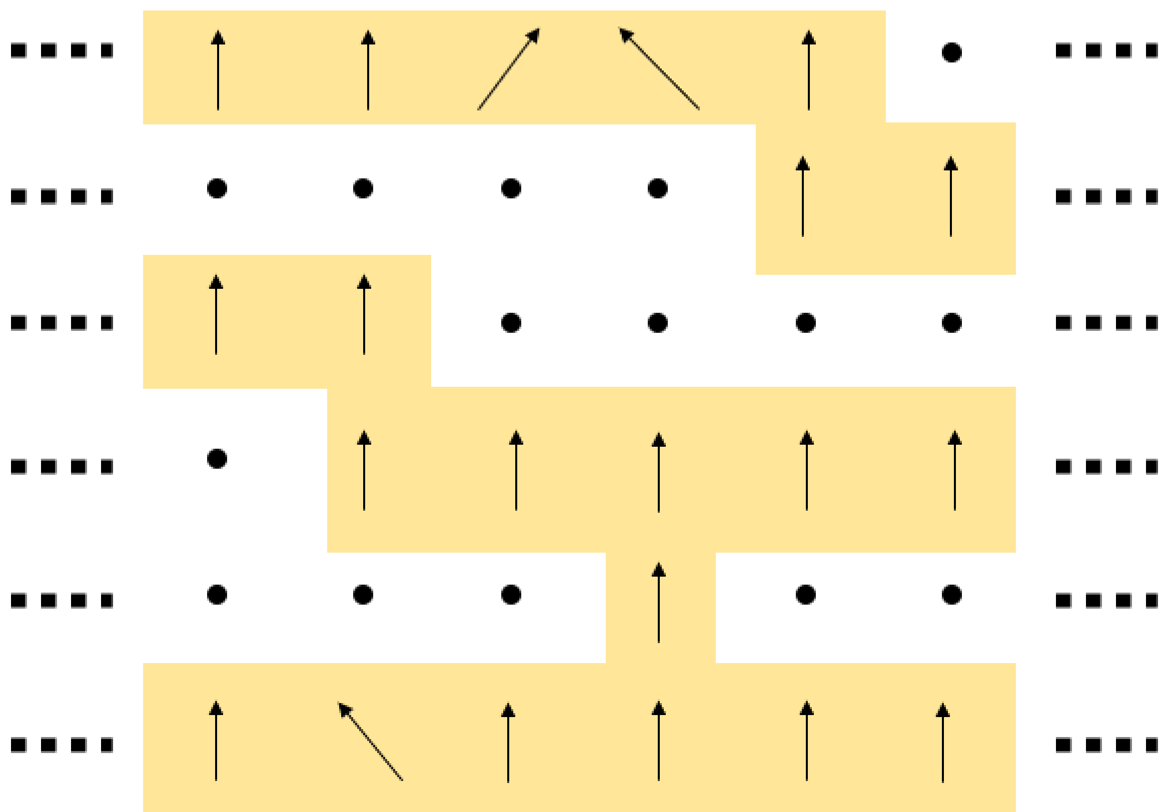


Figure 2 : Quantum algorithm carried out by MBQC. Cluster state changes based on localised 1 qubit measurements causing state to either move horizontally, vertically or tilt.

This method relies on one qubit measurements to affect the cluster state and carry out the algorithm. While tabletop optics could be used to create small scale cluster states ([29] [30]), to generate much larger cluster states would occupy an infeasibly huge area which will

increase the chance of accidental misalignment of optics, effecting the stability of the system.

To this end, the manufacturing industry, more specifically the integrated photonic industry, has turned its attention to photonic integrated circuits (PICs) towards the creation of a photonic based quantum computer. Companies such as PsiQuantum [31] aim to bring a quantum computer with over a million qubits to reality soon [32]. The realisation of this requires the development of techniques and technologies that are used in this thesis but on a much larger scale; where 10 x 10 mm chips were used for this thesis, full 12-inch wafers covered in chips of a similar size or smaller need to be processed repeatably.

1.4 Silicon Photonics vs Compound Semiconductor Photonics

1.4.1 Silicon

Silicon (Si) is a popular choice for PICs due to the well-established techniques and technologies the silicon industry has developed for the creation of electronic integrated circuits. With this advanced fabrication infrastructure, creation of multi-component PICs in bulk can produce large circuits capable of carrying out any quantum algorithm imaginable.

Si has excellent passive optical properties that are beneficial to PICs. At 1550 nm, a common communications wavelength, the refractive index of Si is 3.48 [33] which allows tight confinement of light in silicon waveguides; small, tight bends can be created reducing the size of a PIC and concentrating it in a small area. It also has a high χ^3 Kerr coefficient [34] that can be used to generate entangled photons through spontaneous four wave mixing (SFWM) ([35],[36]) and other non-linear effects; the probability of a Kerr effect occurring

increases in likelihood proportionally to the intensity I^2 [37] which is why the silicon is pumped intense coherent signals.

While these properties make it an attractive candidate for a photonic quantum computer, Si is centrosymmetric; it does not benefit from additional χ^2 Pockels effects that can be used for active components such as switches. The Pockels effect allows a materials refractive index to be changed by applying an electric field [38]. This can be used as a lossless switching mechanism by changing the resonance of a cavity or the phase picked up by light travelling a waveguide for example. Most integrated switches in Si use either the thermo-optic (TO) [39]effect or free carrier dispersion (FCD) [40] to induce a refractive index change used for switching although other methods exist [41], [42].

TO based switches are low loss (0.1 dB [43]) but operate on the order of μs [44]. Light in a circuit with TO switch with a 15 μs switching time [45] will cover a distance of 0.45 m. For feed-forward MBQC, delay lines will be required to allow the switch to change increasing the likelihood of losing photons during propagation, slowing processing times and increasing the footprint of chips. On the other hand, FCD based switches are faster, on the order of ns, but are lossy (0.8 dB) [46]. The introduction of free carriers into the Si to induce FCD allows the free carrier an opportunity to absorb the photons by free carrier absorption (FCA) losing the very photons intended to be switched. Given that photonic MBQC relies on single photons, losing a photon in a lossy FCD switch would alter an algorithm resulting in an incorrect result and an unreliable quantum computer. The limitation in switching mechanisms bottlenecks Si based photonic quantum computers to either slower, lossless switches or faster, lossy switches. Considering more complicated PICs may require a photon

to encounter many switches to carry out an algorithm ([47], [48]), another choice of material system may be a more attractive option.

1.4.2 Compound Semiconductors

Another group of materials that could be considered for PICs are compound semiconductors (CS). Many CS have a lattice structure like Si but because a CS is made up of different elements this breaks any centrosymmetric properties, giving CS access to an additional χ^2 Pockels effect that Si does not. They can not only overcome Si's limitation for switching but also possess similarly attractive properties like Si for passive components.

Gallium arsenide (GaAs) and indium phosphide (InP) are two such CS that have an extensive history in photonics with many difference devices being made over this time ([49], [50], [51], [52], [53], [54]). For instance, InP integrated photonics ranges back to the 1970s. The creation of CW lasers [55], leading to integrated laser diodes [56], distributed Bragg reflector (DBR) lasers and electro-absorption modulators [57] in the 1980s. Further developments produced to tuneable lasers [58] and multichannel wavelength dependent multiplexers [59] culminating to tuneable optical routers [60] and multichannel Gb/s transmitters [61]. However, PICs in either of these share a common disadvantage familiar with Si, two photon absorption (TPA) at 1550 nm [62] whose photons have an energy of 0.8 eV.

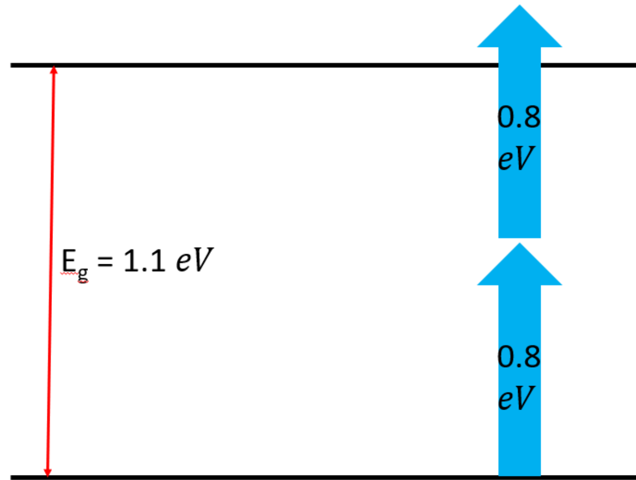


Figure 3 : Diagram showing the TPA process specifically in Si with photons at wavelength 1550 nm (0.8 eV)

TPA is the effect where two photons have a combined energy enough to excite an electron to a higher energy state, absorbing both photons in the process Figure 3. This is an issue when trying to use linear and/or nonlinear effects that are dependent on the intensity of light. This is especially an issue for heralded photon pair sources [63]; two photons at different wavelength are generated that can be separate such that one is detected indicating the presence of the other. If either of the photons are not separated from the pump field soon after creation the likelihood of TPA increases. Either the heralding photon is absorbed and an unaccounted photon is present in the circuit, or the heralded photon is absorbed so an assumed present photon is missing or both are absorbed.

Lithium niobate, $LiNbO_3$, is a material that has been used for a long time in tabletop active components as a phase modulator due to its incredibly high χ^2 coefficient [64], [65], [66]. However, with a refractive index of 2.1 [67] at 1550 nm, a $LiNbO_3$ waveguide would require larger dimensions to keep a mode confined and larger bends. This means larger circuits which incur higher losses due to additional propagation loss.

CS such as Gallium Phosphide, GaP, and Gallium Nitride, GaN, solve both issues as demonstrated in Table 1.

Material	Refractive Index at 1550 nm	Bandgap (eV)	Pockels coefficient (pm/V)
Si	3.48 [68]	1.1 [69]	X
$LiNbO_3$	2.1 [67]	4.9 [70]	30 [71]
GaP	3.05 [72]	2.26 [73]	-0.97 [74]
GaN	2.3 [75]	3.2 [76]	1.91 [77]

Table 1: Comparison of properties of Si, $LiNbO_3$, GaP and GaN at 1550 nm. Pockels coefficients dependent of crystal orientation being affected by electric field. Largest number presented.

Both have large bandgaps that avoid TPA at 1550 nm and possess a Pockels coefficient that can be manipulated for switching. Although neither has a refractive index as large as Si, both can create high contrast waveguides with suitable substrates. GaP can be used to create smaller waveguides and tighter bends compared to GaN but lacks as strong a Pockels coefficient requiring a higher voltage to switch paths.

GaN wafers have an issue with high defectivity densities because of the lattice mismatch of the GaN to the growth substrate. Commercially available wafers grown by HVPE [78] have a

dislocation density > 10^6 cm^{-2} [79] however different methods to reduce this defect density have been created [80] with ammonothermal growth producing low defect densities of $10^2 – 10^4$ cm^{-2} [81]. GaP grown on Si has a very low lattice mismatch (0.37% [82]) but defects can still arise through other mechanisms such as surface energy mismatch, chemical interactions between layers and symmetry difference between the film and the substrate [83]. However, it is possible to buy commercial available defect free GaP on Si wafers [84], [85].

These are promising materials to compete with Si in the PIC arena, but the development of fabrication processes as demonstrated in this thesis is vital.

1.5 Thesis Outline

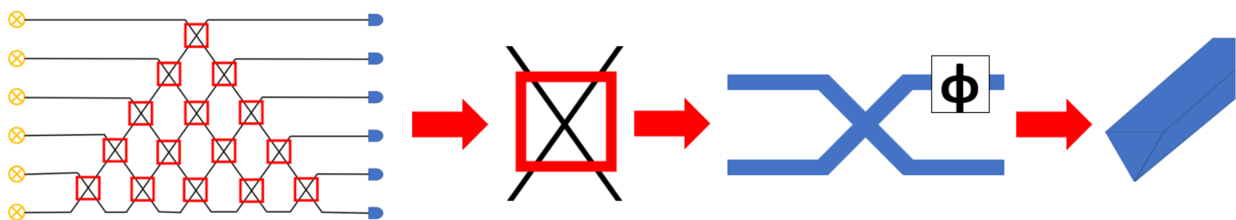


Figure 4 : Quantum computing structure zoomed in on switch breaking down each part to the lowest level, demonstrating importance of switch in the circuit.

To understand how devices in PICs work, an understanding of the physics behind waveguides and their ability to guide light is essential. It also allows waveguide dimensions to be determined that can be used for device designs. These dimensions also give us some idea of the demand on the fabrication process with regards to very small feature sizes. A

comparison between a Si foundry and a CS foundry will give a clear indication of the differences and similarities between the processes required to create PICS in either material as well as the development required to make CS a viable option in the market. These will be discussed in the remainder of this chapter.

With the basic grounding in waveguide physics provided in this chapter, the creation of simulations to determine feature sizes and device performance will be shown in the following simulations chapter. Determination of the single mode regime for CS waveguides and subsequent switch designs based on these dimensions is presented. The performance of the three different switch designs (ring resonator (RR), directional coupler (DC) and Mach-Zehnder interferometer (MZI)) are then simulated to generate dimensions for the switch designs with a similar switching voltage; and performance ultimately being chosen on the overall footprint of the design.

With designs finalised, the development of the fabrication processes required to create them are discussed in the Fabrication chapter. A basic explanation of each step of the process is given to understand the purpose of each step and the challenges that can occur. Solutions to some of these challenges are detailed. However, some challenges are still ongoing and require further investigation to be overcome.

Standard Si fabrication processes can be used to create PICs in CSs with some adjustments required to compensate for the different chemical composition of the materials. However, the growth of some CSs means a detriment in the quality of the material for it to be usable for photonics. Achieving high quality materials ideal for photonics, however, can mean growth on substrates that would not allow integrated photonics structures to function. GaN is one such material. The development of a novel new technique is outlined in the Angled

Cage Etch of GaN chapter allowing suspended photonic structures to be created in high quality GaN without the impedance from an inappropriate substrate leading to the journal paper [86].

The Conclusion and Outlook Chapter summarises the work that has been carried out in this thesis and the conclusions drawn from it. Plans for future work that build upon what has been done in this thesis will show the great potential that PICs in CS has to offer and the wealth of opportunities available in this field.

The breadth of opportunities in this area are many and varied but understanding how a PIC works allows insight into the areas that need to be developed. Understanding the operation of a photonic device requires knowledge of waveguides and modes which inevitably leads to the basis of all electromagnetic theory, the Maxwell Equations [87].

1.6 Maxwell's Equations, Modes and Waveguides

1.6.1 Maxwell's equations

In dielectric media, the Maxwell Equations are [87], [88]:

$$\boldsymbol{\nabla}.\boldsymbol{D} = 0 \tag{3}$$

$$\boldsymbol{\nabla}.\boldsymbol{B} = 0 \tag{4}$$

$$\boldsymbol{\nabla} \times \boldsymbol{E} = -\frac{\partial \boldsymbol{B}}{\partial t} \tag{5}$$

$$\boldsymbol{\nabla} \times \boldsymbol{H} = \frac{\partial \boldsymbol{D}}{\partial t} \tag{6}$$

here $\boldsymbol{E}$ is the electric field, $\boldsymbol{B}$ the magnetic induction**,** $\boldsymbol{D}$ the electric displacement, and $\boldsymbol{H}$ the magnetic field. For waveguides we assume, for simplicity, that the material is a dielectric with no free charges (the current density J and the charge density ρ are both zero already assumed in the equations above) and is linear and isotropic allowing $\boldsymbol{E}$ and $\boldsymbol{H}$ to be related to $\boldsymbol{D}$ and $\boldsymbol{B}$ using the equations:

$$\boldsymbol{D} = \varepsilon_r \varepsilon_0 \boldsymbol{E} \qquad 7$$

$$\boldsymbol{B} = \mu_r \mu_0 \boldsymbol{H} \qquad 8$$

Where ε_0 and μ_0 are the permittivity and permeability of free space and ε_r and μ_r are the relative permittivity and permeability of the material.

If we take the curl of Eq 5 and use the material equations Eq 7 & 8, substituting into Eq 6, it is possible to find the wave equation:

$$\mu_0 \varepsilon_0 \mu_r \varepsilon_r \frac{\partial^2 \boldsymbol{E}}{\partial t^2} - \nabla^2 \boldsymbol{E} = 0 \qquad 9$$

From the solutions to the wave equation, we can see that the unbound/unconfined eigenmodes of free space/continuous dielectric are a continuum of planewaves:

$$\boldsymbol{E} = E_0 e^{i(\boldsymbol{k}.\boldsymbol{r} - \omega t)} \qquad 10$$

travelling at speed c/n, where:

$$c = \frac{1}{\sqrt{\mu_0 \varepsilon_0}} \tag{11}$$

and

$$n = \sqrt{\mu_r \varepsilon_r} \tag{12}$$

An important relationship is the dispersion relation which describes the relationship between a wave's wavelength and frequency (or equivalently $\omega(k)$). When Eq 10 is substituted into Eq 9:

$$(\mu_r \varepsilon_r \mu_0 \varepsilon_0 \omega^2 - k^2) E_0 = 0 \tag{13}$$

As the $\boldsymbol{E}$ field exists, the bracket must be equal to 0 so:

$$k^2 = \mu_r \varepsilon_r \mu_0 \varepsilon_0 \omega^2 \quad 14$$

And so, the dispersion relation is

$$\omega = \frac{ck}{n} \quad 15$$

Where c, the speed of light, and n, the refractive index of the material, are Eq 11 & 12.

1.6.2 Waveguide Solution

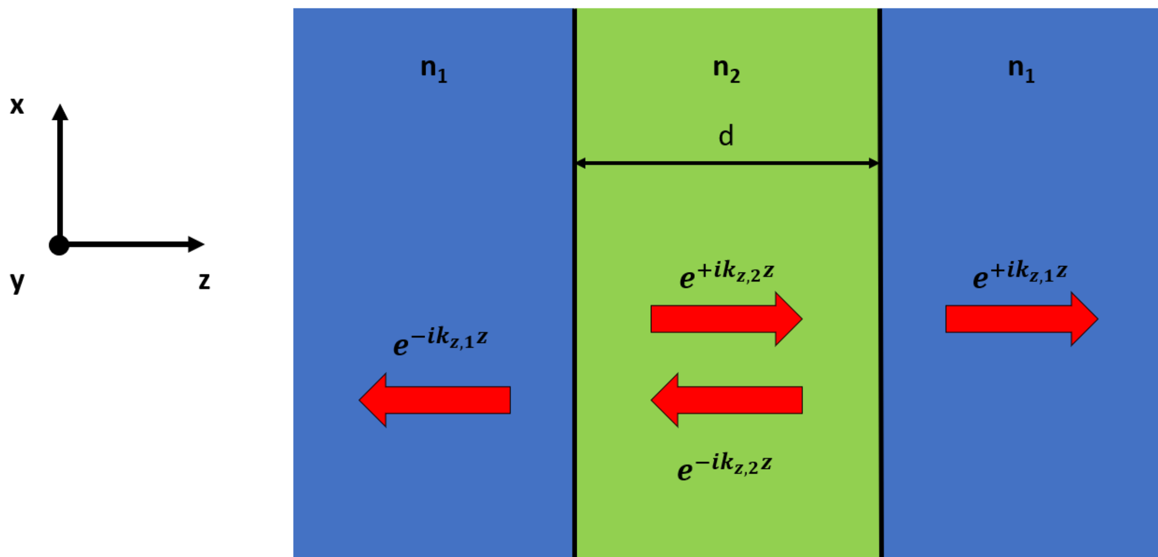


Figure 5: 1D waveguide of width d in the x-z plane divided into different sections associated with the refractive index between the surrounding and the waveguide where $n_2 > n_2$.

To find waveguide modes, we consider a transverse electric (TE) field, $\boldsymbol{E} = \left(0, E_y, 0\right)$, travelling in the x direction of a 1D waveguide with width d and refractive index n_2 surrounded by a cladding either side with refractive index n_1 (Figure 5); the $\boldsymbol{H}$ field can be found by substituting $\boldsymbol{E}$ into Eq 5, finding $\boldsymbol{H} = (H_x, 0, H_z)$. As in the free-space example, we would expect the waveguide mode to be a plane wave in the direction of travel, but modified to be confined to the waveguide region:

$$E_y = E_{0,y}(z)e^{ik_x x - i\omega t} \quad (16)$$

k_x is the wavevector in the x-direction and must be the same in all regions otherwise the wave would break up as it travels along the waveguide. $E_{0,y}$ is the waveguide mode profile, which describes how the waveguide mode is confined in the z-direction. For the wave in the z direction, we require the $\boldsymbol{E}$ field to oscillate in the waveguide region and decay exponentially in the cladding. Given these conditions we require $k_{z,1}$ to be imaginary and $k_{z,2}$ to be real.

While k_x is the same for all regions, k and k_z are different:

$$k_1^2 = \left(\frac{n_1\omega}{c}\right)^2 = k_x^2 + k_{1,z}^2$$

$$k_2^2 = \left(\frac{n_2\omega}{c}\right)^2 = k_x^2 + k_{2,z}^2$$

Rearranging for k_x:

$$k_x^2 = \left(\frac{n_{eff}\omega}{c}\right)^2 = k_1^2 - k_{1,z}^2 = k_2^2 - k_{2,z}^2 \qquad 17$$

Shows that n_{eff}, the effective refractive index of the waveguide mode, needs to be:

$$n_1 \le n_{eff} \le n_2 \qquad 18$$

To satisfy the conditions $k_{z,1}$ to be imaginary and $k_{z,2}$ to be real.

At the boundary of the waveguide, we require the tangential fields, E_y and H_x, to be continuous. The z component of E_y has already been calculated and the z component of H_x can be found using Eq 5. These lead to the eigenvalue equation:

$$\tan 2u = \frac{2uv}{v^2 - u^2} \qquad 19$$

Where:

$$u = \frac{k_{2,z}d}{2} \tag{20}$$

$$v = -\frac{ik_{1,z}d}{2} \tag{21}$$

And breaks down to:

$$v = u \tan u \tag{22}$$

$$v = -u \cot u \tag{23}$$

Substituting Eq 20 and 21, Eq 17 becomes:

$$u^2 + v^2 = \frac{\omega^2 d^2}{4c^2}(n_2^2 - n_1^2) \tag{24}$$

Showing how the frequency, width of the waveguide and the refractive index contrast determines the waveguide modes confined. Eq 19 can only be solved numerically and why a TE mode in a 1D waveguide was used to determine this instead of a full 3D calculation.

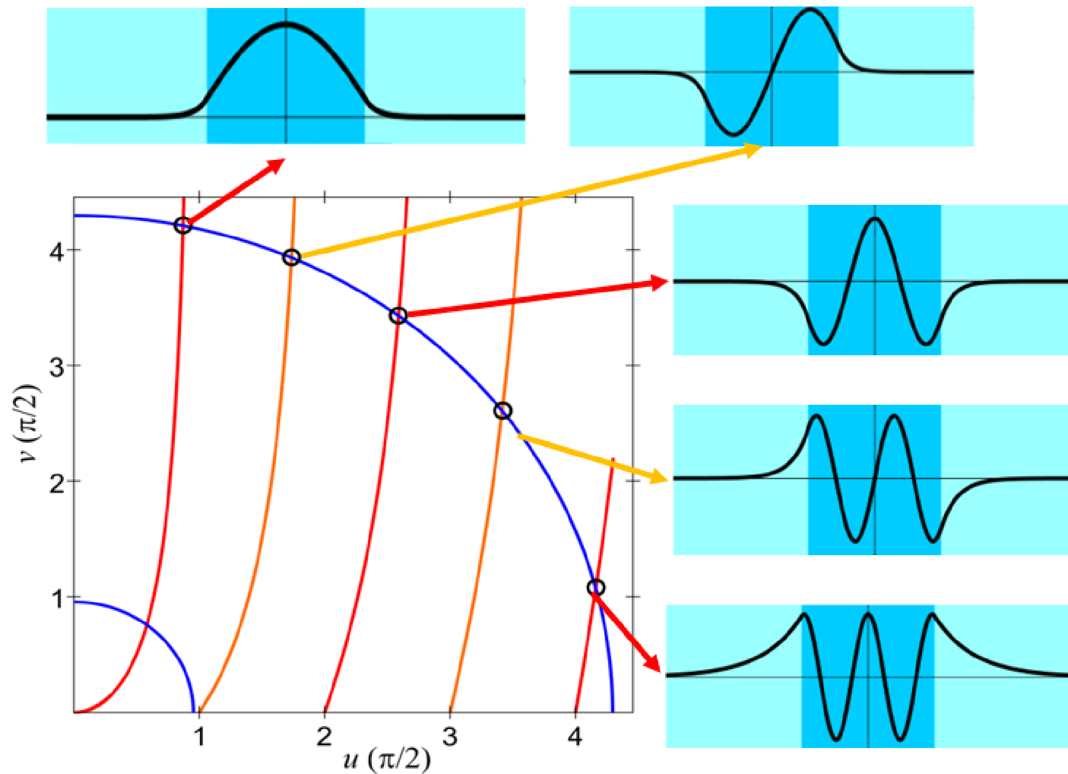


Figure 6 : Graph solutions of equations Eq 22 (red) and 23 (orange) intersecting with circle from Eq 24. Each intersection is supported mode in the waveguide shown around the outside of the graph.

With the waveguide modes demonstrated Figure 6, let us investigate the structures themselves.

1.6.3 Waveguides

As seen in the 1D solutions above, a waveguide is a structure that guides light in one direction of propagation while remaining confined in the others. The waveguide region, also known as the core, is grown on a substrate and has a cladding surrounding it, air or some

other material such as SiO_2. They can be categorised into different types but geometrically the main types are strip and rib waveguides, Figure 7.

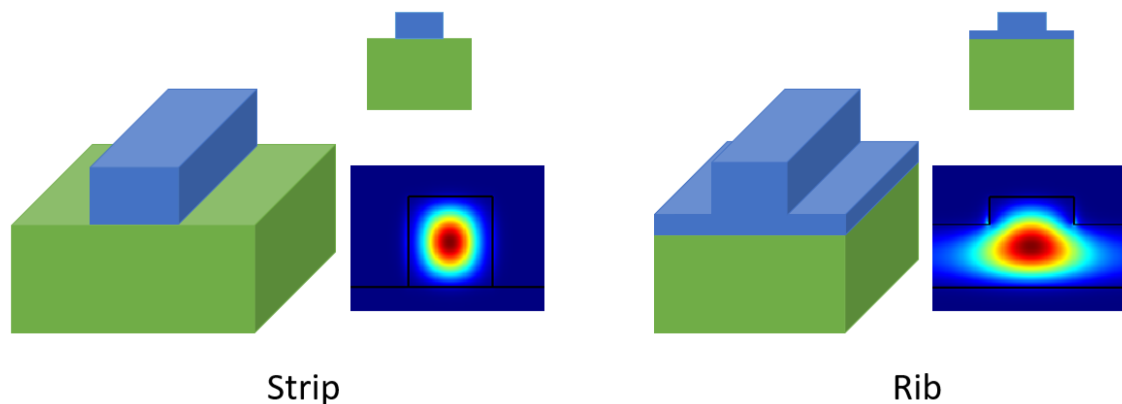


Figure 7: Different geometries of waveguides used for controlled propagation of light. Strip waveguides are etched down to substrate, mode is confined to etched area but susceptible to roughness of sidewall. Rib waveguides are partially etched reducing susceptibility to sidewall roughness. However, mode is centralised to partially etched section but spread out below.

Strip waveguides are fabricated by etching straight down to the substrate and can easily be made to operate in the single mode regime. However, their losses are more susceptible to sidewall roughness as light diffracts off the rough sidewalls and the light is lost to its surroundings. Rib waveguides are fabricated by etching down into the waveguide material to create the rib structure. The fabrication uses a partial etch which requires a more controlled etch process to achieve the specific rib depth and can struggle to be single mode depending on the rib height. However, the losses due to sidewall roughness are reduced as less material is etched away, reducing the area of roughness of the sidewall [89]. These waveguides can be categorised further by mode operation (single [90] or multimode [91]), refractive index profile (graded [92] or step [93]) and material [94], [95].

To quantify the overlap of the mode with the sidewall, the confinement factor, Γ, can be calculated [96]. The confinement factor is the percentage of the mode confined to the core waveguiding layer. For the TE mode, the polarisation of interest (See Section 2.1.1), the confinement factor is [97]:

$$\Gamma = \frac{h \times w \times \left(\frac{2\pi}{\lambda}\right)^2 \sqrt{(n_{core}^2 - n_{sub}^2)} \sqrt{(n_{eff}^2 - n_{clad}^2)}}{2 + h \times w \times \left(\frac{2\pi}{\lambda}\right)^2 \sqrt{(n_{core}^2 - n_{sub}^2)} \sqrt{(n_{eff}^2 - n_{clad}^2)}} \qquad 25$$

where h and w are the height and width of the waveguide, and n_{core}, n_{sub} and n_{clad} are the refractive index of the waveguide core, substrate and cladding respectively. n_{eff} is the effective refractive index for the specific mode. Each waveguide solution has a different wavevector and so propagates along the waveguide at different speeds. This is analogous to the mode propagating through a medium with a refractive index associated with its rate of propagation. This confinement factor can be used to determine the loss associated to the mode overlap with the sidewall as done in [98].

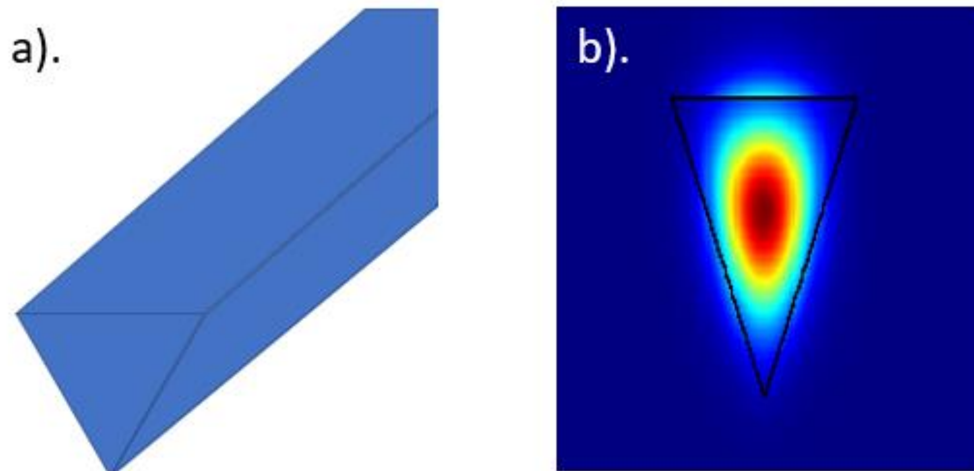


Figure 8 : Triangular waveguide , a), capable of supporting waveguide modes, b), created by novel etch process for suspended structure.

The geometries of standard waveguides are due to the limitations of traditional etch methods. In this thesis, a novel method of angled cage etch is used to create suspended structures in GaN. This method of etching creates triangular shaped waveguides capable of supporting waveguide modes for photonic processes Figure 8. This is detailed in the Angled Cage Etch of GaN Chapter of this thesis.

Waveguides are a vital component in a PIC, as they are the photonic equivalent of wires for electrical circuits. Poorly fabricated waveguides will loss light so quickly it will not reach the next photonic component let alone the end of the PIC. This impacts the performance of the photonic component itself; numerical analysis of a Si waveguides at 1550 nm with dimensions 500 x 500 nm and 260 x 260 nm show that, for a variation in the sidewall from 2 nm to 10 nm the propagation loss goes from 1.58 to 39.55 and 5.68 to 140 dB/cm respectively [99]. Creating low loss waveguides are important for PICs so light entering a circuit can make it through the entire circuit and still be detected, but there are certain devices that are essential for an algorithm to be processed.

1.7 Building blocks of quantum photonics

As mentioned in the Introduction, a simple photonic quantum computer is essentially a source, a switching array and a detector but each of these has component parts that are essentials for quantum optics.

1.7.1 Sources

Photons should ideally be created on chip to avoid any losses due to coupling light from an external source [100]. However, most sources are external and most on chip sources require pumping to generate photons. Coupling light can be done by edge coupling [101] in from the side but relies on optical quality facets and limits the positioning of a circuit. However, high efficiency can be achieved this way and has little polarisation or wavelength dependence, although positioning is crucial. Grating couplers [101], on the other hand, allow freedom of placement anywhere on the chip as the light is coupled top down. However, the efficiency is less than edge coupling and are very sensitive to polarisation and wavelength; any variation in the fabrication can shift the coupling wavelength or the efficiency of the coupling.

While sources are not the focus of this thesis the fabrication processes developed can be used to create on chip sources. Initial development of suspended cavities in a photonic crystal nanobeam are created with the angled cage etch which can be used as an integrated photon source.

1.7.2 Switches/Splitters

Once the light is coupled into a circuit, division of the light through the circuit can be done using beamsplitters and switches. A beamsplitter is a passive component and can be a Y-splitter [102], directional coupler (DC) [103] or multimode interference (MMI) splitter [104]. Each splits the light in different ways; be it by physically splitting a waveguide, bringing 2 waveguides into proximity or self-imaging principle. A switch is an active component relying on an external signal to initiate the change of path, be it an electric field or heater. Different switch designs include a ring resonator (RR) [105], DC [106] or Mach-Zehnder Interferometer (MZI) switch [107]; an MZI can also be used as an active phase modulator.

The three switches mentioned are simulated later in this thesis to determine their performance in the CSs GaP and GaN. The aim is to find the switch with the smallest switching voltage for a given area. This allows more switches to be fabricated on a single wafer enabling complicated circuits to be created that can carry out more complex algorithms in a cost-effective way in terms of manufacturing. If a circuit can be fabricated on a single wafer with all the processing done all at once, costs of creating a circuit are reduced with less variability between parts.

1.7.3 Detectors

Once the light has passed through the PIC, the light needs to be detected. These, like sources, ideally would be on chip, such as superconducting nanowire single photon detectors (SNSPDs) [108]. Usually, however, the light is coupled off chip and measured using detectors such as avalanche photo diodes (APDs) [109] or similar detectors [110], [111].

These too rely on couplers to remove the light from the chip and experience the same issues as mentioned before. I envisage using SNSPDs as the detectors.

These devices are required to carry out any form of quantum optical operation, not just for quantum computing, such as Hong-Ou-Mandel experiments [112] and squeezed light [113] or NOON states [114] for sensing. Many of these components can already be created in mass production in foundries and are integral parts of pre-existing circuits. State of the art equipment allows vast quantities of devices to be created in foundries already with some cross over in both Si and CS foundries.

1.8 Modern Day Foundries: Si v CS

Many modern-day foundries are set up for the creation of integrated electronic circuits dealing with 8 and 12-inch Si wafers to maximise the output of chips per wafer [115], [116]. This process usually involves the repetition of defining and etching structures on many layers, as well as the growth or deposition of layers for different components of a chip. For the creation of mass-produced PICs most of these processes would be used with some adaptation required for the sensitivity of the devices and the materials being used; photonic devices are sensitive to fabrication variation, shifting operation wavelengths and reducing device efficiency as well as different materials being more fragile than Si. Photolithography is used for circuit definition on the order of microns due to the speed of definition and area covered. However, to achieve dimensions on the order of nanometres deep UV (DUV) photolithography [117] is required [118] rather than conventional photolithography due to the diffraction limit.

For a CS foundry [116], [118], [119], a lot of the same equipment can be used once again for large scale production of circuits. The problem is that for many CSs the creation of 12-inch wafers is not possible due to the lack of maturity of the CS wafer technology. However, readily available Si manufacturing tools can be adapted for CSs simply by changing the chemistry used dependant on the material. While ideally this is the only change required more extensive changes are required often to keep wafer integrity during transit either between tools or while running.

This is the focus of this thesis: to endeavour to create or further optimise fabrication processes already available to make mass producible CS PICs a reality. Realising the challenge required to do this involves understanding the dimensions that need to be achieved to create competitive CS alternatives to already available Si devices. For this, simulations are a vital tool to efficiently design devices and gauge their operation compared to Si.

Chapter 2

2 Simulations

Simulations are a valuable theoretical tool that allows efficient design. In this chapter, devices were simulated using Lumerical FDTD Solutions and modes were calculated using Lumerical MODE. These use a finite difference time domain (FDTD) solver [120] and finite difference eigenmode (FDE) solver [121] respectively to solve the Maxwell equations to simulate light propagation and mode confinement.

The FDTD method ([122], [123], [124]) propagates an EM field using the relationships in Eq 5 and 6, where the spatial change of the $\boldsymbol{E}$ field relates to a change in the $\boldsymbol{B}$ field in time and vice versa. This is done incrementally on a grid, divided into cells called a Yee cell [125], across the device to be simulated. The Yee cell is such that the $\boldsymbol{E}$ field components lie on the vertices of the cell and the $\boldsymbol{B}$ fields lie at the centre of the face of the cell. Alternating between these relationships it is possible to simulate the evolution of an EM wave across a structure in time and so, via the Fourier transform, multiple frequencies simultaneously. However, it requires a large amount of computational memory to carry out the simulation and, especially with large structures, can take a long time to run depending on the density of Yee cells in the mesh.

The FDE solver, like FDTD, creates a 2D grid across a structure and solves the Maxwell equations across the grid. However, the FDE solver solves these equations by formulating the Maxwell equations into matrix form to solve the eigenmode problem using the procedure in [126]. Using this method, it is possible to find the effective refractive index and

mode profiles. This solver uses sparse matrix techniques to find the modes so is not as computationally demanding as FDTD, depending on the mesh.

The aim of the mode calculations carried out in this thesis is to determine at what waveguide widths single mode waveguides exist. The desire for single mode waveguides is to avoid multimodal effects [127]. Strip waveguides are also simulated as it is easier to fabricate these compared to rib waveguides, because the etch depth is less critical as we are etching to the substrate and, with the correct etch chemistry, only the waveguide material will be etched away. The modes of waveguides have been calculated as a function of waveguide width to determine the range over which a single mode waveguide exists.

With these waveguide designs, different types of switches are described with emphasis on their switching mechanisms to best simulate their operation. To determine the best switch design, the figure of merit used was the switching voltage compared to footprint size, $V_{\pi}A$. While the usual figure of merit for a switch is $V_{\pi}L$ ([128], [129], [130], [131]), $V_{\pi}A$ is used instead to maximise the coverage of a wafer with switches so more complex circuits can be created on a single wafer; V_{π} is the voltage required to change from one path to the other completely i.e. induce a π phase change, A is the total area covered by a switch and L is the switching length. A RR switch was simulated first to obtain an area the DC and MZI switch should similarly cover. The switching voltage, V_S, was calculated and from this $V_{\pi}A$ to determine the best design.

2.1 Mode Calculations

2.1.1 GaN

GaN is generally grown as thin epitaxial layers on silicon or sapphire [132]. Here we only consider sapphire, as the high refractive index of silicon makes it unsuitable as a waveguide cladding. To grow high quality layers, a buffer of aluminium nitride (AlN) is generally required [133]. When dealing with silicon waveguides, this wafer thickness is restricted by the demand of big silicon-on-insulator manufacturers. A minimum buffer thickness and layer thickness is required for high quality growth, but in general with GaN wafers we have a little more choice. We can ask for different layer thicknesses to be grown but the trade-off is an increased cost and decreased repeatability.

The setup of the simulation is key to achieve accurate and realistic simulations for real world fabrication. Below is an image of the simulation area used to determine the waveguide dimensions for single mode operation Figure 9.

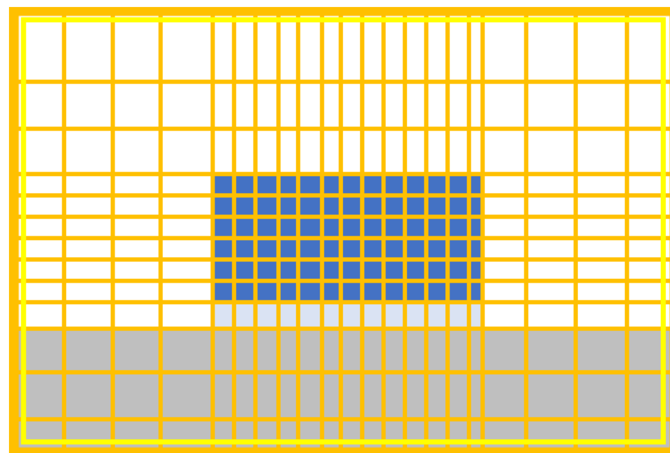


Figure 9: Diagram of simulation setup for mode calculations. Dark blue is GaN, light blue is AlN, and grey is sapphire. The yellow box is a mode monitor to measure the mode. The orange box is the FDTD simulation area.

The Lumerical database has a wide variety of materials already available to use for simulations, such as sapphire. However, GaN and AlN are not part of this but these materials can be created in the database given data. For AlN and GaN the data from [134] was used to create the materials for the simulation. Lumerical also allows you to select the level of accuracy for the FDTD simulation area; there is a trade-off between high accuracy and long computation time. This mesh accuracy setting is available with the auto non-uniform mesh type setting [135]. The auto non-uniform mesh type creates a mesh across the simulation automatically to best fit the object being simulated in the simulation areas. With increasing mesh accuracy, the number of cells per wavelength increases making the mesh across the simulation area finer.

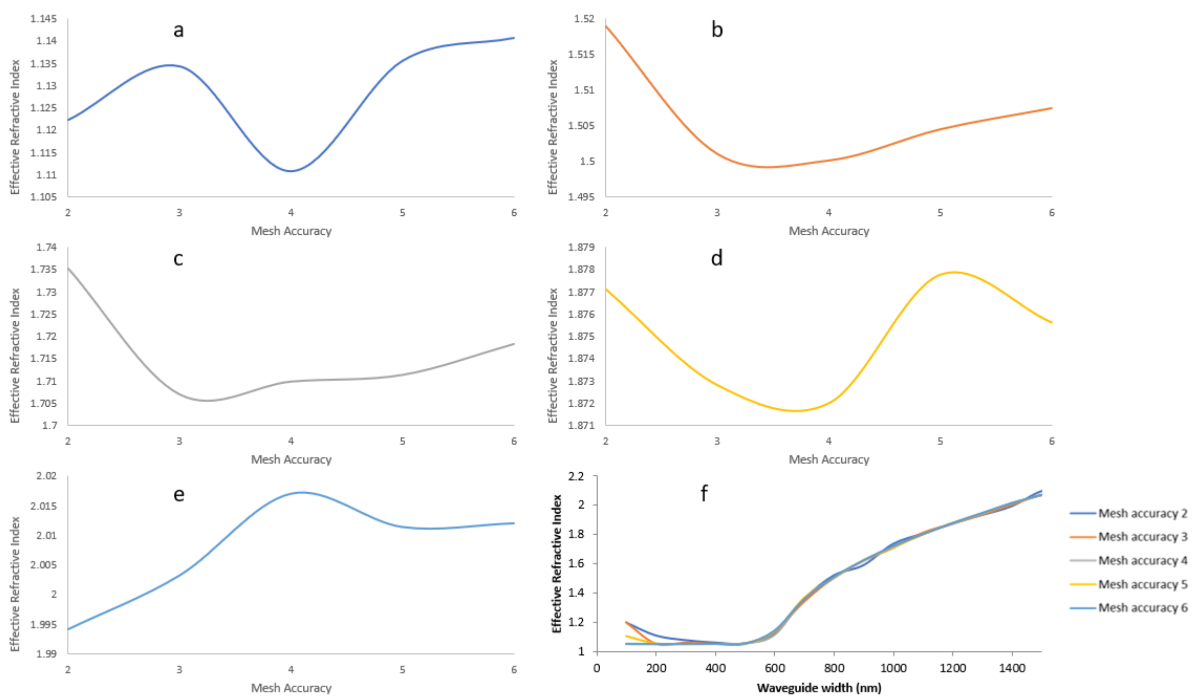


Figure 10: Simulation results of the variation in effective refractive index with mesh accuracy in the FDTD simulation area for waveguide width a). 600 nm, b). 800 nm, c). 1000 nm, d). 1200 nm, e). 1400 nm. f). Effective refractive index against waveguide width with each mesh accuracy overlapped.

To see the variation between mesh accuracies, a simulation to calculate the effective refractive index, n_{eff}, was run with varying waveguide width. From Figure 10, there is clearly differences between the mesh accuracies when simulating the n_{eff} of a Si waveguide; the biggest variation in effective refractive index between the mesh accuracies is 0.03 for a waveguide width of 600 nm. A mesh accuracy of 4 was set to compromise between the accuracy and the computation time as it closely follows mesh accuracy 6 in Figure 10, the highest mesh accuracy.

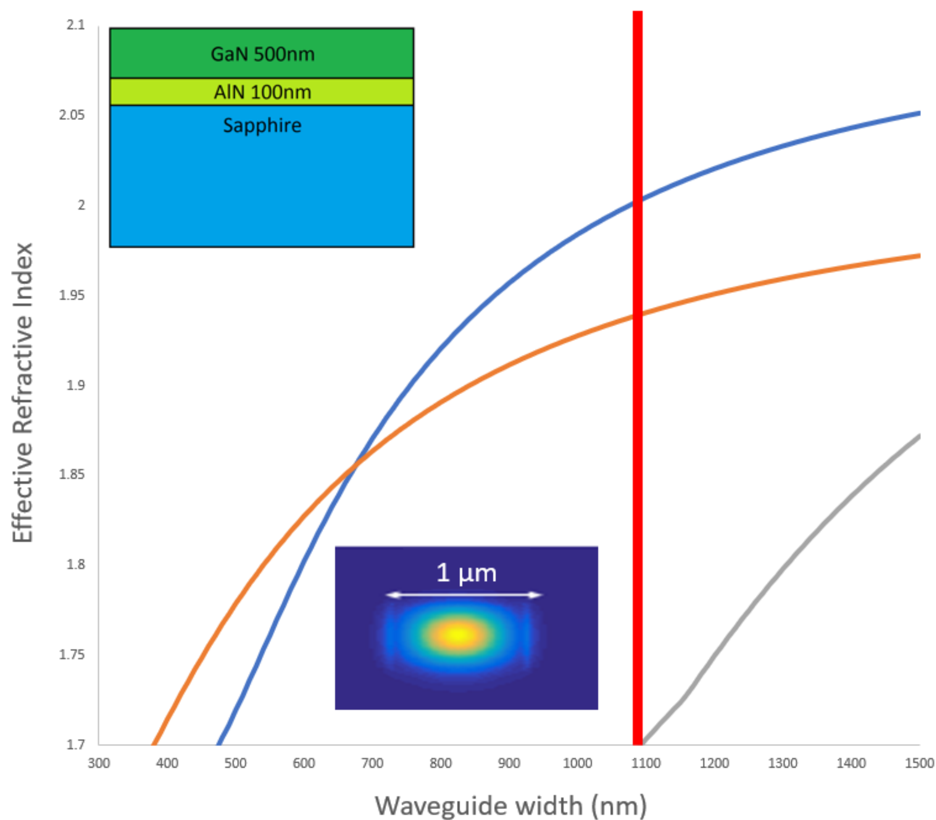


Figure 11 : Graph of effective refractive index against waveguide width for single mode waveguides in GaN. Blue line is the fundamental TE mode, orange line is the fundamental TM mode and grey line is the 2nd TE mode. Any width below the red line is in the single mode region for the TE mode. Insets: Wafer structure used for simulations. Simulated mode profile in a 1 µm wide by 500 nm high waveguide using Lumerical MODE Solutions.

For the actual mode simulation, the width of the strip waveguide was optimised to achieve single mode operation. Plotting this variation in width against n_{eff}, Figure 11 shows at which width each mode begins to be confined. We know all values of n_{eff} should lie between 1.7 and 2.4 as these are the refractive indices of sapphire and GaN at 1550 nm respectively [136],[137]. Values calculated by the simulation that are smaller 1.7 are discarded as these are unconfined modes. The width associated to the fundamental TE mode being confined is the width to be determined.

Technically this width is not a single mode waveguide as both the fundamental TE and TM mode are confined Figure 11. However, I am only interested in the TE mode as it will experience the greatest effect by the electro-optic effect as can be seen by the rate of change of the effective refractive index to width in Figure 11; while varying the width of the waveguide effect the effective refractive index so will the change in refractive index caused by the Pockels effect. From the simulations a waveguide width of 1 µm is near the maximum width that remains single mode. The wider the waveguide, the less the sidewall roughness will affect the dispersion of the mode as the field strength at the wall Figure 12.

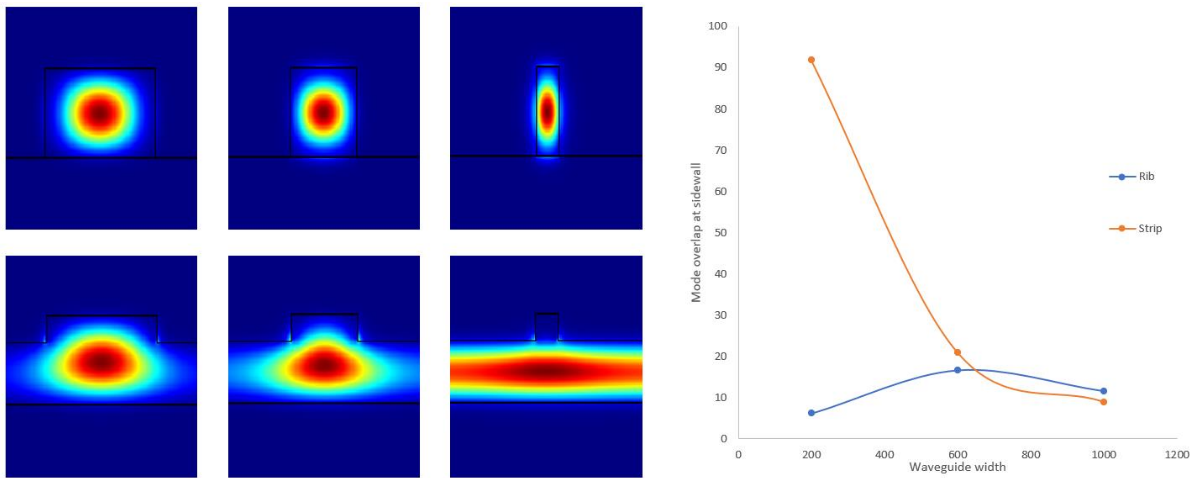


Figure 12 : Mode overlap with sidewall reducing as waveguide width increases for strip waveguide, reducing the susceptibility to loss due to any sidewall roughness for wider waveguides. In comparison, for a rib waveguide, as the rib width increases, the waveguide mode becomes more centralised and less confined in the unetched region.

Etching a device to the substrate is easier to fabricate than a rib waveguide because the lower cladding can be used as an etch stop rather than partially etching the substrate. However, creating rib waveguides means less of the substrate is etched, reducing the losses associated to the sidewall roughness due to the reduced overlap of the waveguide mode with the etched sidewall. From Figure 12, while most of the mode is confined in the etched area it is also confined in the area below which has not been etched. The etched part forces the mode to be more central rather than spread across the entire substrate width. This also reduces the confinement of the mode and means wider waveguides are required to confine the mode in the GaN waveguide. It also reduces the parameter space in which single mode waveguides can be achieved, as slab waveguides become created. However, as the rib width gets larger, more of the mode begins to be confined in the etched region. Light scatters off the corners where the etched and unetched regions meet but as the rib width increase this will reduce, like the strip waveguide.

2.1.2 GaP

The wafer structure for the switch to be designed in GaP can be seen in the inset of Figure 14. GaP has a refractive index of 3.05 [72] at 1550 nm which is less than Si which has a refractive index of 3.45 [138] so the mode would favour being confined to the Si. Ideally the GaP would be grown on a substrate with a lower refractive index compared to it but to grow high quality, low defect GaP the Si layer is required [139], [140]. Simulations of the mode confinement in the GaP layer with varying Si layer thickness were done Figure 13.

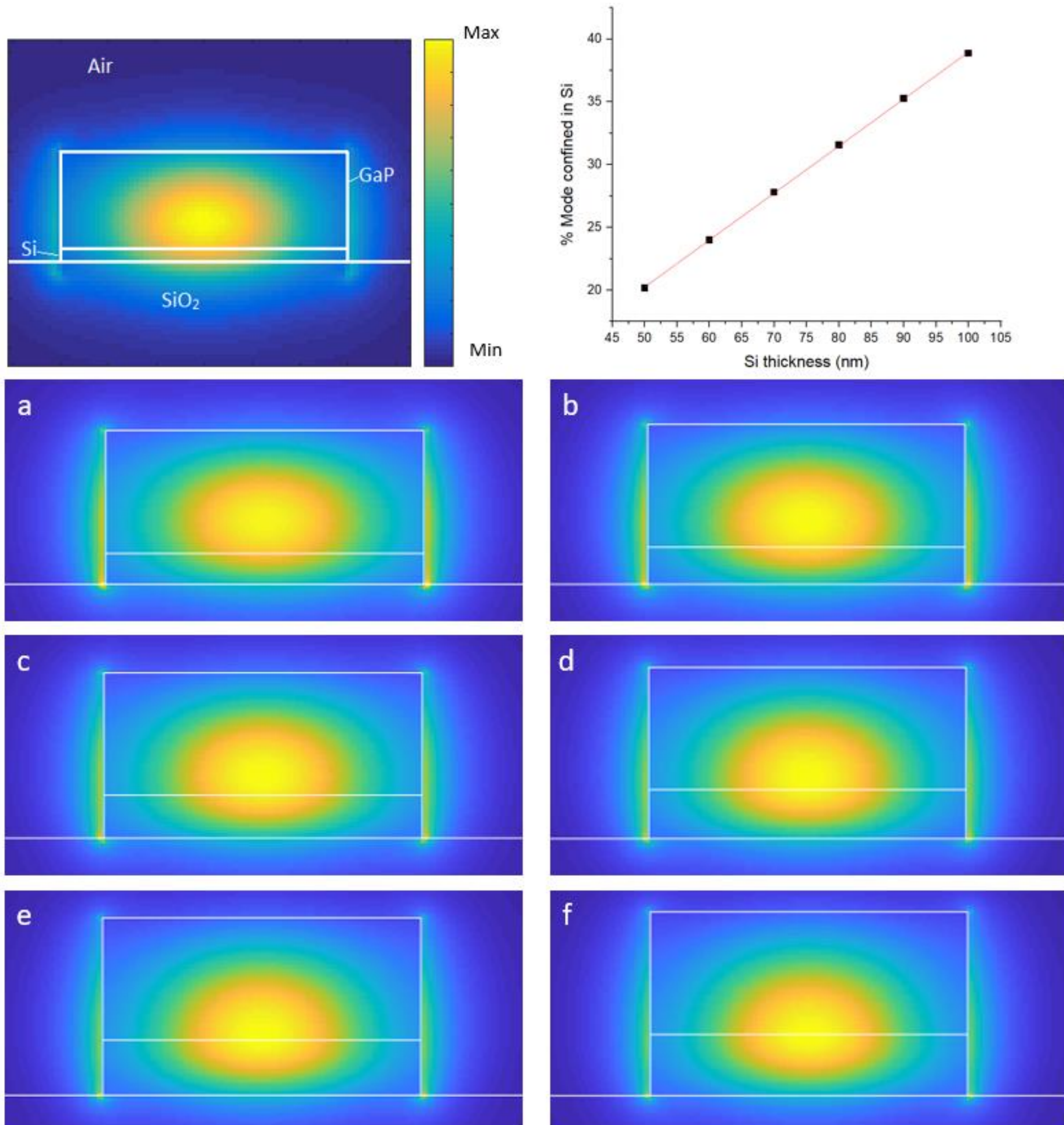


Figure 13 : Simulation of mode confinement in GaP layer with varying Si thickness. Si = a). 50 nm, b). 60 nm, c). 70 nm, d). 80 nm, e). 90 nm, f). 100 nm. Image at the top left is annotated version of 50 nm thick Si layer. As the Si thickness increases so the mode moves from the GaP layer towards the Si layer due to the higher refractive index. Graph (top right) showing percentage of mode confined in the Si layer against Si layer thickness. Line of fit indicates, for every extra 10 nm of Si the mode confinement in the Si layer increases by approximately 3.7%.

These simulations allow us to determine the proportion of the mode in the GaP layer that will experience the electro-optic effect. This was done by finding $|E|^2$ in the combined GaP/Si region and comparing it in the Si region alone based on the simulation. From the simulations, a Si thickness of 50 nm allows for approximately 83% of the mode to be confined to the GaP layer as shown in Figure 13. It is also thick enough to be able to grow low defect GaP due to the low lattice mismatch between GaP and Si [141], [142] With the given dimensions for the wafer structure, a width of 600 nm for the waveguide allows single mode operation as outlined in Figure 14.

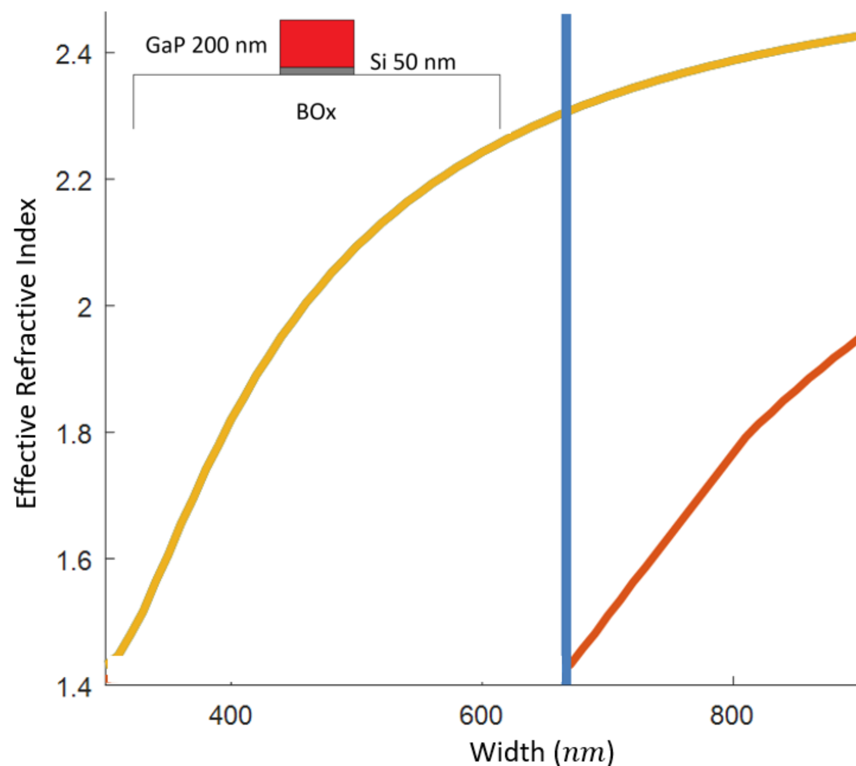


Figure 14 : Graph of effective refractive index against waveguide width for single mode waveguides in GaP. TE modes shown only. Yellow line is the fundamental TE mode, red line is the 2nd order TE mode. Any width below the blue line is in the single mode region. Inset: Wafer structure used for simulations.

With the waveguide dimensions determined for both GaN and GaP, simulations can be carried out to determine the dimensions and performance of various devices using these waveguides. In the Introduction several devices were mentioned briefly that were required to carry out quantum computation. Below is a more in-depth look at some of these devices, looking at the mechanisms that make them work and their important metrics to be simulated, as necessary.

2.2 Devices

With the capability to create integrated photonic circuits on the nanoscale various devices can be fabricated. For many of these circuits there are key devices required for both efficiently coupling light in and out of the device and manipulating the light in the circuit. These rely on various quantum effects, such as the Kerr effect, that are amplified when integrated due to the concentration of the light to a smaller area. Below is a discussion of some of these devices.

2.2.1 Grating couplers

Edge coupling [143] is a popular way of coupling light because of the wide bandwidth and insensitivity to polarisation with low coupling losses [144], but fabricating an optical quality facet is difficult and restricts the location of circuits. Grating couplers, on the other hand, allow the freedom to place a grating coupler anywhere on a chip but is sensitive to the wavelength [145] and the polarisation of the light [146]. Grating couplers can be

comparable to edge couplers ([147],[148]) but require tight fabrication tolerances to create them. [149] gives an in-depth review of both methods of coupling light into a circuit.

2.2.2 Integrated Sources

An on-chip source of photons would remove the issue of efficiently coupling light into a system to be used in a circuit [100]. While most integrated sources require optical pumping from an external source these sources have the advantage of increased photon number control [150]. With an external laser source ensuring a single photon source is difficult and usually relies on extreme attenuation of a beam which does not guarantee a single photon entering a circuit [151]. This can have adverse effects to systems where photon number control is important, such as optical quantum computing and metrology. However, there are two common processes used for on-chip photon generation that allow better photon number control.

(a) Spontaneous Parametric Down Conversion

Spontaneous Parametric Down Conversion (SPDC) is a probabilistic, nonlinear χ^2 process; the likelihood of an SPDC event occurring is proportional to the intensity of the light, I [152]. A photon enters a nonlinear material where it is absorbed to a virtual level and re-emits two photons with wavelengths different to the original photon Figure 15.

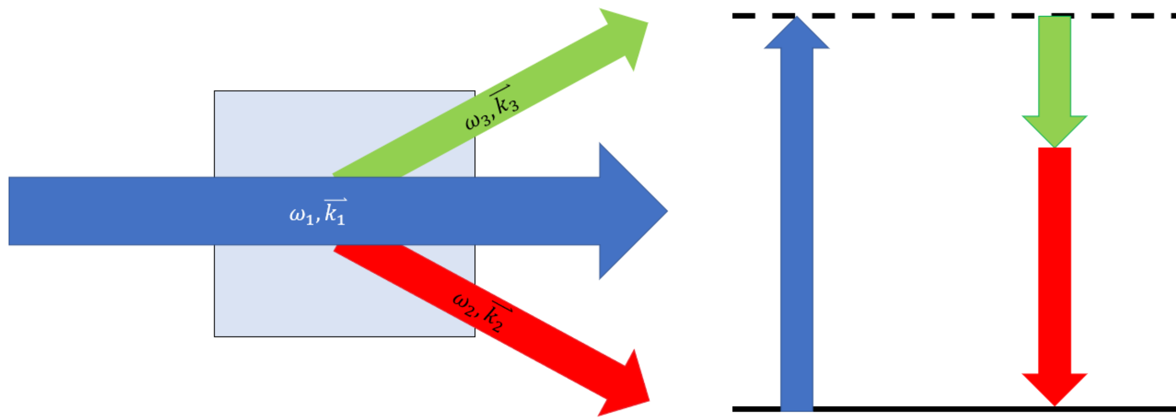


Figure 15 : SPDC occurs inside a birefringent crystal where a single photon is absorbed in a virtual level and re-emits 2 photons of different frequency. Not only does the energy need to be conserved but so does the momentum. The resulting photons travel at an angle away from each other, physically separating the photons as well by frequency.

As each photon is a different wavelength it will have a different refractive index travelling through the crystal. This limits the photon combinations as the phase matching condition of the photons must also conserve energy and momentum [152]:

$$\hbar\omega_3 = \hbar\omega_1 + \hbar\omega_2 \tag{26}$$

$$\overrightarrow{k_3} = \overrightarrow{k_1} + \overrightarrow{k_2} \text{ and } \Delta\vec{k} = \overrightarrow{k_3} - \overrightarrow{k_1} - \overrightarrow{k_2} = 0 \tag{27}$$

A birefringent crystal is normally used as the refractive index changes the polarisation of the photons which can be used to differentiate and separate the photons [153]. There are three types of SPDC:

Type 0: The photon entering the crystal has the same polarisation as the pair of photons created.

Type 1: The photons created have the same polarisation but are orthogonal to the photon entering the crystal.

Type 2: The pair of photons created have orthogonal polarisations to each other.

Type 2 SPDC is useful as a heralded photon source as the two photons created can be separated using a polarising beamsplitter; one can be redirected to a detector to indicate the presence of the other while the other can be rerouted into a circuit to be used for a desired operation. With photon counting detectors it is possible to resolve the number of photons created in an event. By controlling the intensity of the light, it is possible to influence the probability of an event occurring and the number of photons that are produced [154].

(b) Spontaneous Four Wave Mixing

Spontaneous Four Wave Mixing (SFWM) is a probabilistic, nonlinear χ^3 Kerr process analogous to SPDC. In contrast to SPDC, the likelihood of an SFWM event occurring is proportional to I^2 [155]. SFWM also has two photons absorbed on a virtual level instead of a single photon but re-emits 2 photons with wavelengths different from the original photons Figure 16.

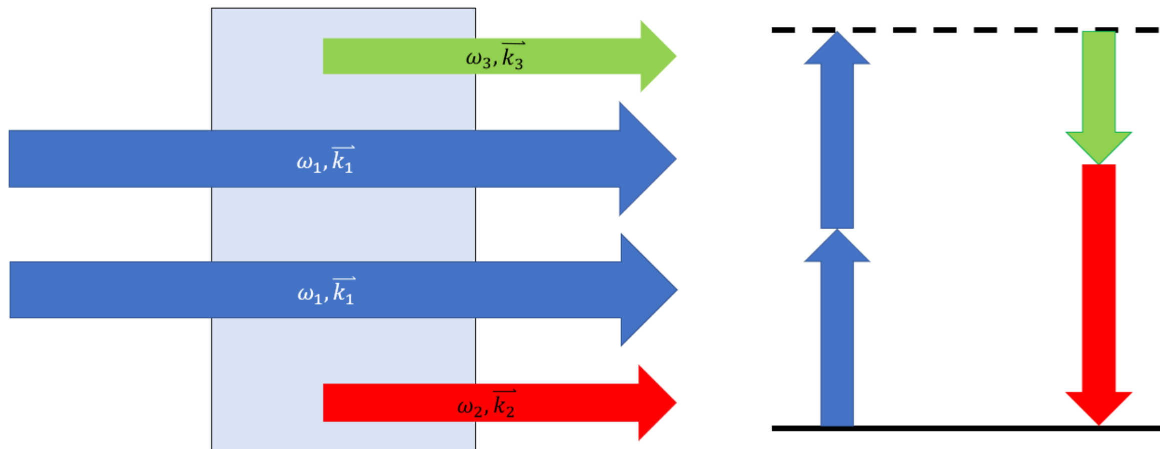


Figure 16 : Mechanism behind SFWM, where 2 photons with the same frequency, absorb on a virtual level and are re-emitted as 2 photons with different wavelengths. This can be used for a heralded single photon source where the signal photon is detected and the idler photon enters the circuit.

The fact that two photons are used instead of one means, through dispersion engineering, it is possible to vary the momentum of the photons to allow more possible wavelength combinations to be created [155].

2.2.3 Beamsplitters

A tabletop beamsplitter can take different forms; be it a half-mirrored mirror, polka dot mirror, periodically poled birefringent cube etc; but each perform the same task of dividing or recombining light. For integrated photonics, a beamsplitter can be a Y junction, directional coupler or multimode interference (MMI) coupler to name a few. Each does the same job of splitting and recombining the light but in different ways:

- The Y junction splits the waveguide into two separate paths with an adiabatic s-bend separating the paths to reduce any losses due to the change in direction [156].

- A directional coupler (DC) utilises the coupling of two waveguides in proximity such that light begins to transfer from one waveguide to the other and back over a distance known as the switching distance [157]. These too usually have s-bends to physically separate the coupled waveguides to halt the oscillation of the light between the two waveguides.

- An MMI coupler uses a wide section of waveguide that allows multimode operation to occur. The mode interferes with itself and using the self-imaging principle [158] splits itself into two identical images at half the amplitude that can then be separated back into single mode waveguides.

2.2.4 Phase Modulators

The phase difference between two beams of light travelling along different paths determines how they will interfere when they recombine. The optical path difference (OPD) between the two is calculated by:

$$\mathrm{OPD} = n_1 l_1 - n_2 l_2 \tag{28}$$

where n_x is the refractive index of the material the light is travelling through and l_x is the length of the path the light has taken $(x = 1,2)$. By varying either the refractive index or the path length you can vary the phase of the light. Changing the path length would require some sort of piezoelectric induced stretching or contracting of the waveguide [159] or using MEMs [160]. Most phase modulators choose to induce a change in refractive index of the material. This can be done in several ways namely the TO effect, FCD or the Pockels effect. TO and FCD effect were discussed in the Si section of the Introduction but the Pockels effect was only briefly discussed.

It is possible to induce a refractive index change using the χ^2 Pockels effect by applying an electric field across a material that has χ^2 properties [161]. The induced refractive index change is:

$$\Delta n = -\frac{1}{2} n^3 r_{xy} E \qquad 29$$

where n is the refractive index of the material without an electric field applied, r_{xy} is the Pockels coefficient of the plane experiencing the electric field and E, the electric field. The E field is generated by placing electrodes either side of the waveguide with electricity flowing through them. The E field can be calculated, assuming a constant electric field, by:

$$E = \frac{V}{d} \qquad 30$$

where V is the applied voltage and d is the distance between the electrodes. This effect does not introduce free carriers into the material, so FCA is eliminated, and the effect is only limited to the speed the electric field can be applied [162].

Each method of phase modulation has its pros and cons but due to the speed and lack of free carrier absorption, a χ^2 electro-optic Pockels modulator is the best option. While these can only be applied to materials that possess a χ^2 effect, for materials that do not a trade-off between speed and loss must be found to determine the best modulator.

2.2.5 Switches

The same principle of changing the refractive index of a material behind the phase modulators can be applied to create a switch. For this, a specific voltage known as the switching voltage, V_S, is applied to induce the refractive index change that will cause the light to change path completely. Three types of switches are presented below that use this as the switching mechanism: ring resonator [163], directional coupler (DC) [164] and Mach-Zehnder interferometer (MZI) [39] switch.

(a) Ring Resonator

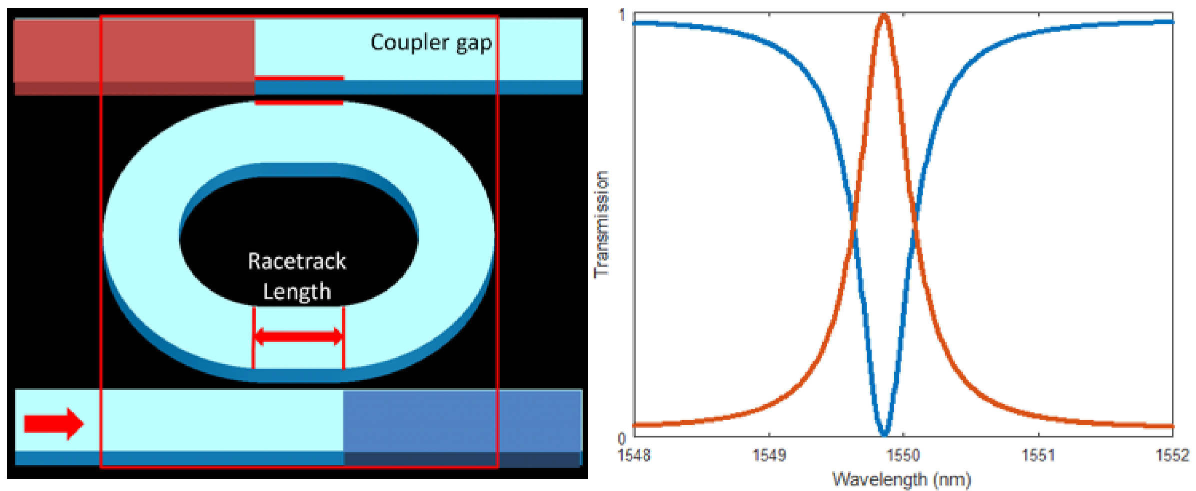


Figure 17 : Ring resonator switch. Light enters at input port (red arrow) and exits through port (blue) if off resonance or drop port (orange) if on resonance. Graph showing variation in transmission at through port (blue) and drop port (orange) with varying wavelength for GaP ring resonator with ring radius 29 µm, racetrack length 4 µm and 200 nm coupler gap.

A RR allows certain wavelengths, dependent on its dimensions, to interfere constructively dependent on the central resonator structure [165]. The refractive index change induced by the electrodes, in a similar configuration as [40], causes the resonant wavelengths to shift. The light can then be switched between coupling into the RR and out the drop port (orange in Figure 17) or continuing to the through port (blue in Figure 17). The full width at half maximum (FWHM) of the resonance peaks will determine the switching voltage to move on and off resonance. The smaller the FWHM, the smaller the switching voltage. The FWHM is dependent on the quality (Q) factor of the RR which determines the lifetime of the photon in the resonator. The Q factor is the measure of a cavity's ability to confine light given losses. The higher the Q factor, the better the cavity, the longer the light lasts in the cavity. Variations in the fabrication of the ring can affect the Q factor. If the sidewalls of the

waveguides are not smooth then light can scatter out of the resonator, reducing the Q factor and increasing V_s.

(b) Directional Coupler

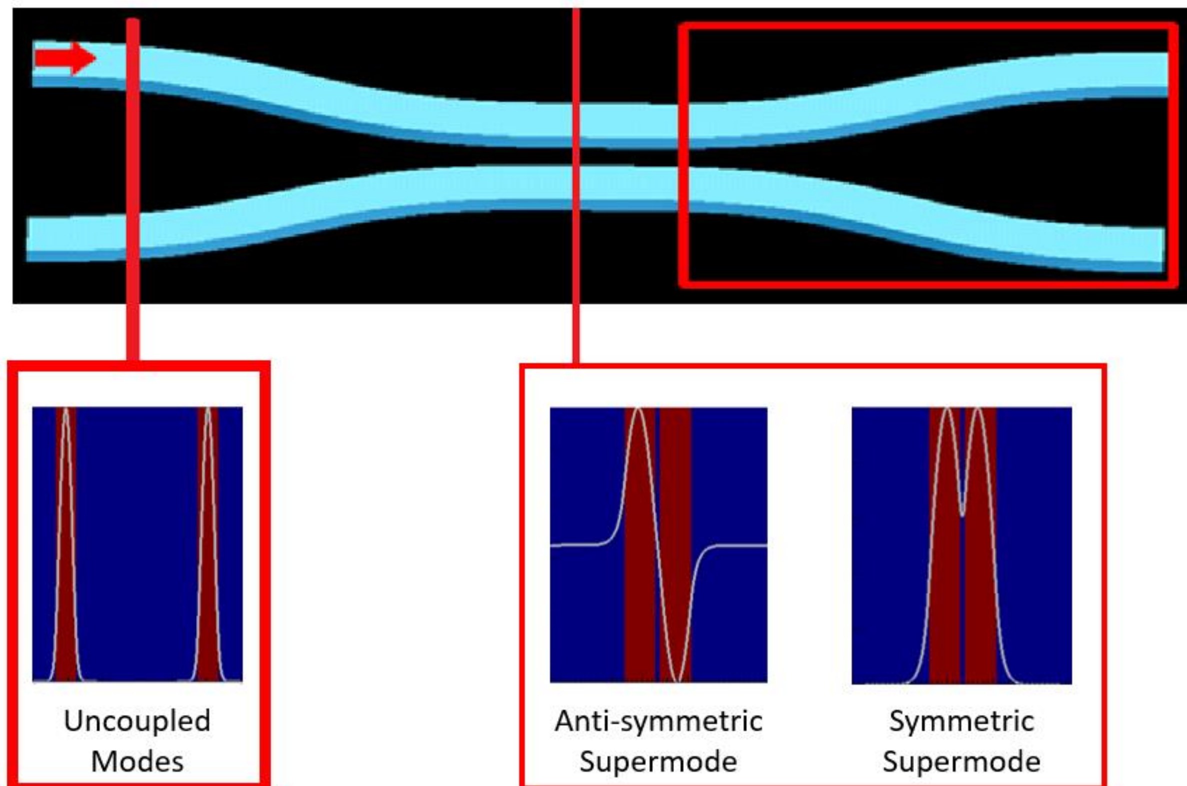


Figure 18 : Directional coupler switch. Light enters at input port (red arrow) and couples with the other waveguide creating supermodes in the coupled region. Both have different effective refractive indices, making the evanescent light oscillate between the two waveguides. Light exits either port depending on length and/or refractive index of waveguide. Images are uncoupled modes, symmetric supermode and anti-symmetric supermode for each region indicated by the red line.

When two waveguides are brought into proximity the mode of each waveguide is coupled creating a supermode that travels along the two waveguides [166]. When light enters this coupled region, the intensity of the light oscillates between the two waveguides. Depending

on the length of this coupled region the light can leave in either the waveguide it originally entered or the other. The minimum switching length, L_c, for the light to completely transfer from one waveguide to the other is calculated by:

$$L_c = \frac{\lambda}{2\,(\beta_s - \beta_{as})} \qquad 31$$

where λ is the wavelength and $\beta_{a,as}$ are the propagation constants of the symmetric and anti-symmetric supermodes respectively. The switching length is dependent on the difference between the propagation constants of the two supermodes, $\Delta\beta$. $\Delta\beta$ is equal to:

$$\Delta\beta = \Delta n\left(\frac{2\pi}{\lambda_0}\right) \qquad 32$$

Combining this with Eq 29 shows by applying an electric field, $\Delta\beta$ can be changed, changing the switching length. However, creating a switch at length, L_c, will mean a larger change will need to be induced in the refractive index to change waveguide. There is a trade-off between the switching voltage and the length of the device. By extending the length of the coupling region the switching voltage is reduced, but the footprint increases.

(c) Mach-Zehnder Interferometer

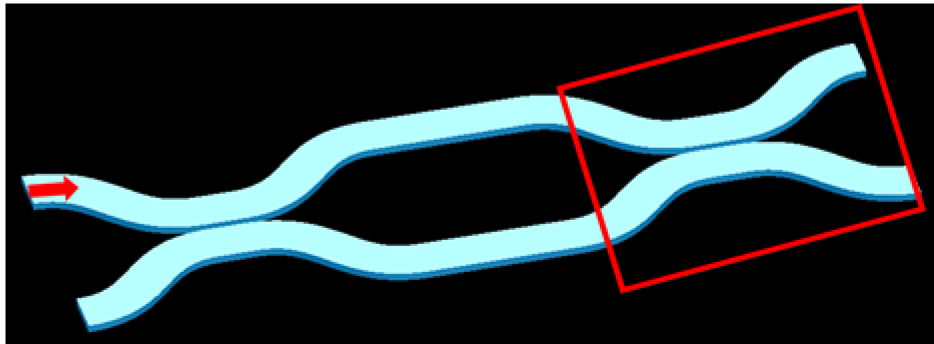


Figure 19 : Mach-Zehnder interferometer switch. Light enters input port (red arrow) and is split equally by the DC. As light travels along arms it picks up phase and recombines at 2nd DC. Depending on the phase change in each arm, light interferes and leaves in one of the ports.

Light entering a MZI [167] is split between two arms where the phase of the light may vary as it travels across the arms. As described in Phase Modulators section, the phase can be changed by varying the length of an arm or the refractive index, Eq 28. A π phase change needs to be induced to the light between the two arms for the light to change path completely:

$$\Delta n L = \frac{\lambda}{2} \quad (33)$$

Where Δn is the change in refractive index, L is the length of the MZI arms and λ is the wavelength.

Like the DC, the switching voltage of the MZI switch can also be reduced by making the arms longer. The fabrication of the beam splitters is crucial to ensure a good extinction ratio. In

the ideal case, the ratios of the beamsplitters at the start and end of the MZI matched such that when the light interferes the light exits through one port or the other. Realistically, it is likely that this will not be the case due to fabrication variation but to compensate for this a constant E field can be applied. This will induce the necessary refractive index change for the light to exit one port completely with a further voltage change required to switch ports.

2.3 Device Simulations

In this thesis, the focus is to simulate designs and develop the fabrication methods towards creating a switch. The aim is to find the smallest footprint, both to reduce losses associated with propagation losses and to maximise the number of devices on a chip. The switching voltage also needs to be small enough that the material is not going to breakdown or require complicated electronics to create a large voltage shift. A low switching voltage also means quick switching times as the change in voltage is small.

The effective refractive index approximation [168] was used to simplify the simulations to a 2D simulation rather than a 3D simulation as the Maxwell equations need to be solved numerically as shown towards the end of S1.6.2; finding the numerical solutions for 2D area compared to a 3D volume is less computationally demanding reducing the simulation time. The effective refractive index approximation works by calculating the mode profile of the multi-layer stack (see Figure 11 and Figure 14 for wafer stack) and approximates the effective refractive index of a waveguide that supports the same mode. A 1-D mode solver [169] was used to calculate the effective refractive index for the simulations; the effective refractive indices used were 2.571 and 2.18 for the GaP and GaN simulations respectively. The initial switch simulations were done in GaP to determine the best switch design

followed by a GaN version. All structures were terminated outside of the FDTD simulation area as a perfectly matched layer (PML) is simulated for the boundary which acts as a perfect absorber of the light to stop any back reflections. All simulations use waveguides that are fully etched ridge waveguides.

2.3.1 Ring Resonator

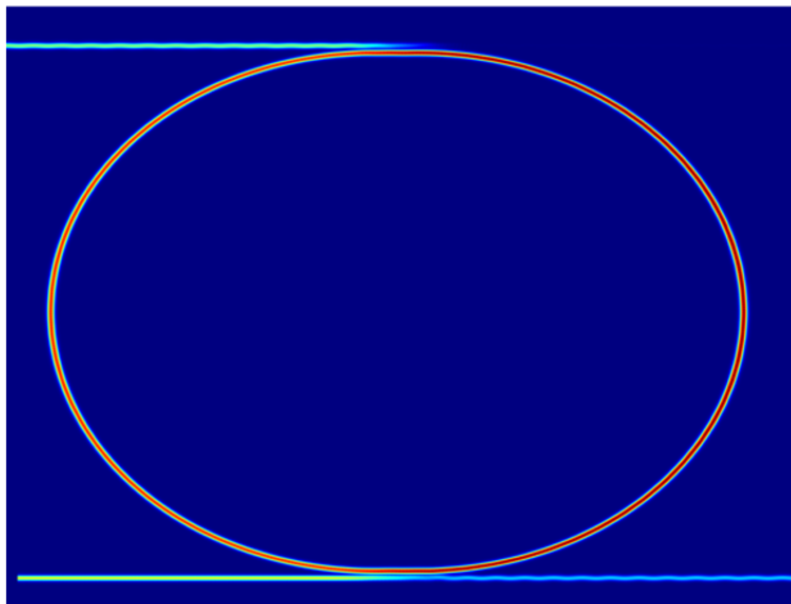


Figure 20 : Ring resonator simulation of area in red box in Figure 17. Radius 29 μm, racetrack edge length 4 μm and coupler gap 200 nm in bar state. Effective refractive index for bar state=2.571 and 2.57164 for the cross state. Footprint area = 3768.5 μm^2

Simulations of the ring resonator switch found that with a ring radius of 29 µm, a racetrack length of 4 µm and a coupler gap of 200 nm the switching voltage $V_s = 56$ V. V_s is calculated by combining Eq 29 and 30 and rearranging for V given the Δn in Eq 33. This switching voltage over the 600 nm wide waveguide is close to the breakdown field of GaP

[170]. The switching voltage is likely to be higher than this in a real device due to fabrication variations reducing the RR performance causing the GaP to breakdown. However, this switch may not be the best design to use. The footprint of the device was calculated to be the minimum area that contained all parts of the switch (red square in Figure 17). The dimensions for the directional coupler and MZI switch were calculated so they also had a similar footprint. This includes the S-bends to couple the light in and out of the coupling region and arms for each switch.

2.3.2 Directional Coupler

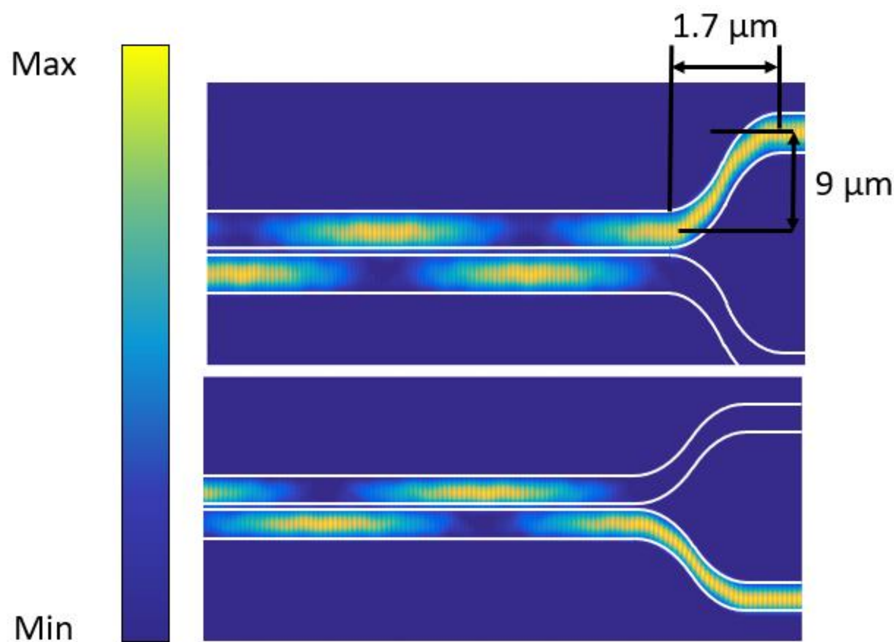


Figure 21 : Directional coupler simulation results of area in red box in Figure 18. Coupling region length = 769.7 μm and a coupler gap = 100 nm. Effective refractive index 2.561 for bar state (top image) and 2.571 for cross state (bottom image) Footprint area = 3702.19 μm^2. Scale bar showing E^2 intensity.

The DC uses S-bends to alter the path of the light to bring the 2 waveguides into proximity of each other. S-bends are a compact way to do this with minimal loss of light as partial arcs of circles are connected to create a continuous curve instead of 90° turns with straight waveguides in between [171]. In this case 2 arcs of a circle were connected to create a smooth continuous transition from one to the other. For the simulation, the height of the S-bend is defined as the change in the y-direction from the centre of the waveguides and width is the length from end to end travelled in the x-direction. Simulations were done and determined low loss S-bends with length and width 9 µm and 1.7 µm respectively as in as Figure 21.

The coupling region of the DC was calculated to be 769.7 µm long based on a similar footprint as the ring resonator where the coupler gap between the DC waveguides is 100 nm. This is much larger than the switching length which is why in Figure 21 multiple switches between waveguides can be seen. A 100 nm coupler gap was chosen as it should be possible to fabricate a gap this size with e-beam lithography and it reduces the switching voltage [166].

2.3.3 Mach-Zehnder Interferometer

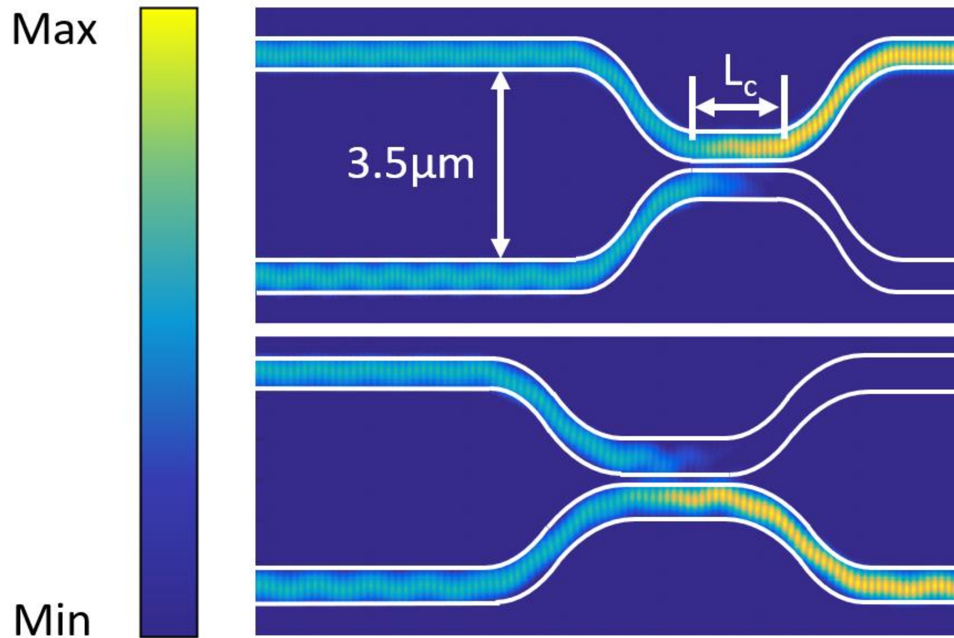


Figure 22 : MZI simulation. Results above show area in red box in Figure 19, close up of DC at end of MZI arms. MZI arm length = 760.8 µm and distance between the top and bottom arm = 3.5 µm. Effective refractive index 2.57 for bar state (top image) and 2.571 for cross state (bottom image). Footprint area = 3768.5 µm^2. Scale bar showing E^2 intensity.

The DC was adapted into a beamsplitter with coupling length 2.5 µm, L_c, to split and recombine the light in and out of the MZI switch. Considering the beamsplitter dimensions the length of the arms were 760.8 µm, with a distance between the arms of 3.5 µm which requires a switching voltage $V_s = 87$ V to change the phase across one of the arms.

2.4 Discussion

Table 2 shows the results of the design simulations in GaP for the three switch designs.

Switch Design	Δn	V_s (V)	$V_\pi A$ (Vm^2)
Ring Resonator	0.00064	56	2.11 x 10^{-7}
Directional Coupler	0.01	872	32.28 x 10^{-7}
MZI (one arm varied)	0.001	87	3.27 x 10^{-7}

Table 2 : Summary of switch design simulations in GaP for designs with a similar footprint

The RR appears to be the best design as it has the smallest V_s, thereby the smallest $V_\pi A$, however, it is possible to reduce the V_s of the MZI further. Using a push-pull configuration [66], the refractive index in both arms can be varied simultaneously in opposite directions using the same V_s, halving the V_s required to induce the same refractive index change. This would make $V_s = 48.5$ V, $V_\pi A = 1.64 \times 10^{-7}$ Vm^2. It is also simpler to reduce V_s for the MZI by making the arm lengths longer. For the RR, improvement of the V_s relies on improving the fabrication process to have smooth sidewalls, increasing the Q factor. Given these factors, the best switch design is the MZI switch.

This switch was then simulated for the GaN wafer in Figure 11 and compared with GaP,

Table 3.

V_s (V)	GaP arm length (mm)	GaN arm length (mm)
4	8.4	11.7
8	4.2	6.1
12	2.8	3.7

Table 3: Comparison of MZI switching voltages between GaP and GaN. These figures were found using Eq 29 and 30 based on simulation results.

The V_S calculated for the initial simulations would require complex electronics to be able to switch rapidly, so the arm lengths have been calculated that would reduce V_S to a level where simple electronic systems can be used and make switching times much shorter.

The performance and footprint of the switches could be further improved by making the coupler gap of the RR, DC and DC splitter in the MZI smaller than 100 nm. However, trying to fabricate gaps smaller than this would be difficult. It is important to make the dimensions in the simulations a realistic representation of what is obtainable using the tools available.

Another consideration is that the simulations use fully etched ridge waveguides for the switches. To induce the electro-optic effect the electrodes would need to be in contact with the GaP and GaN. This would mean the switches themselves would use rib waveguides instead of ridge waveguides, impacting the confinement of the light especially in bent waveguides. This is significant for the RR switch as seen in Figure 23 where the confinement of the light to the circular resonator reduces with increasing GaN layer thickness.

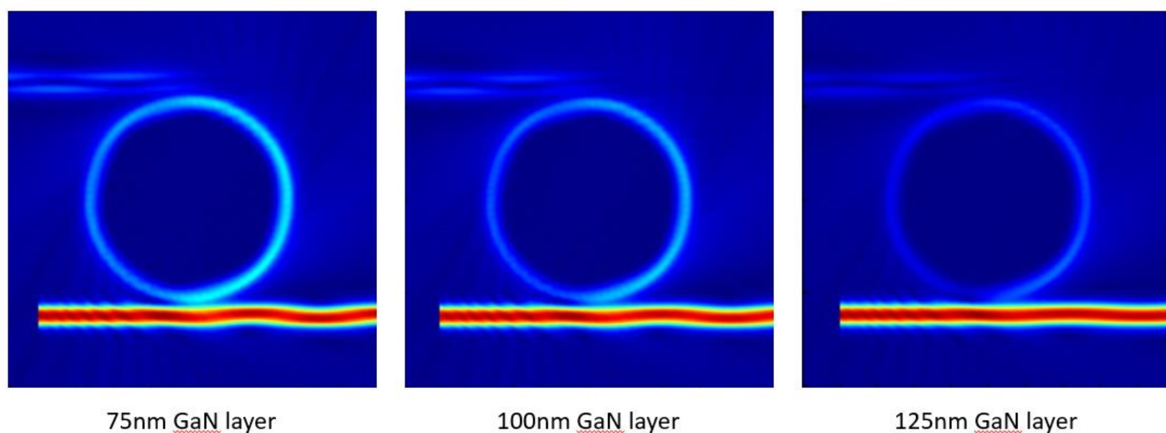


Figure 23: Simulation of GaN ring resonator with vary GaN layer thickness simulating the rib waveguide. Confinement of light to ring resonator reduces with increasing GaN layer thickness.

For the MZI the rib waveguides would not impact its performance and its overall footprint would only increase due to the change in the S bends. Even though the simulations have been carried out using ridge waveguides for the devices, the result for the best design is still the same although dimensions would need to be found.

2.5 Conclusion

From the simulations above the MZI switch in the push-pull configuration has the best $V_\pi A$ out of the three switch designs considered. It is also one of the easier designs to modify to reduce V_s for a more efficient switch. However, this comes with an increase in the arm length reducing the maximum number of switches possible to fabricate on a wafer. These simulations give the optimal performance of these switches also, as they do not consider the variation in the fabrication process. Nor do they consider the requirement for the electrodes to be in contact with the GaP or GaN, creating rib waveguides, to induce the electro-optic effect. It is the aim to improve the fabrication processes to achieve values as close to the optimal performance. This is discussed in the next chapter.

Chapter 3

3 Fabrication

The current infrastructure for integrated circuits is based around complimentary metal-oxide-semiconductor (CMOS) processes [172], for the creation of transistors for microchips in Si. However, as Moore's law [173] appears to be slowing due to both physical limitations and improvements becoming less significant [174], the opportunity for other platforms to compete with Si in the information arena has opened up. PICs are a complimentary technology to CMOS electronics in that they are used as a means of communication between electronic devices. However, PICs are vital in the realisation a photonic quantum computer. Fortunately, most of the CMOS processes can be used in the fabrication of PICs [175] and can be applied to compound semiconductors (CSs). Further adaptation of these techniques and technologies will help cement CSs as the next viable alternative to Si for the PIC platform.

The various techniques used to fabricate PICs in this thesis are discussed below followed by the progress made towards creating a process to fabricate PIC in GaP and GaN. This chapter is organised by explaining the process of a typical CS wafer to make generic waveguides. Specific examples are given in later chapters.

3.1 Fabrication techniques and technologies

3.1.1 Lithography

In semiconductor manufacturing, there are two types of lithographic processes used, photolithography [176] and e-beam lithography [177]. Each of these processes transfers a design into a resist to be used as a mask or used to create hard masks via lift off. The development of these processes is vital to ensure the correction dimensions for the waveguides and subsequent devices. Variations in these dimensions could affect, for instance, the number of modes confined by a waveguide or the operational wavelength of a device. Below is a description of each process and some of the challenges associated with them.

(a) Photolithography

Photolithography uses light to transfer patterns into resists to be used as masks. It is a quick process compared to e-beam lithography (seconds compared to minutes or hours) and can be used to expose an entire wafer all at once. There are two types of resist, positive and negative [178].

When a positive resist is exposed, it increases the solubility of the resist by breaking the polymer bonds, allowing the resist to be removed when placed in developer. Positive resists allow size control of areas to be exposed; the longer the sample is left in the developer, the larger the features become. Conversely, when a negative resist is exposed the polymer bonds are strengthened, decreasing the solubility of the resist, removing the unexposed

when placed in developer. Negative resists allow size control of areas to be protected; the longer left in the developer, the smaller the features become.

It is also possible to use a bilayer resist mask consisting of two different resists that develop at different rates [179]. This allows thicker masks to be created and create a substantial undercut that can be used for lift off processes, such as metal masks.

There are a number of variables that can affect the development of a mask in photoresist [180], but one significant one is the wavelength used for the exposure. This variable can determine the minimal size of the features possible to create. For devices with features sizes less than a micron the diffraction limit can be a problem. The diffraction limit is [181]:

$$d = \frac{\lambda}{2\, n \sin\theta} \qquad 34$$

Where d is the resolution of the feature, λ is the wavelength of the light, n is the refractive index of the medium the light is travelling through (air =1) and θ is the half angle from the aperture to the focal spot.

Shorter, more energetic wavelengths (deep UV (DUV)) [182] need to be used or more complicated methods [183] are required to create these masks. Steppers are another photolithographic tool that expose individual circuits one at a time onto a wafer stepping to the location next to the previous exposure eventually covering the wafer rather than a mask with an array of circuits that can expose the entirety of a wafer. The advantage of this is that a larger more detailed circuit can be created on a mask making it more robust to errors in the mask production. However, it is a longer method of pattern definition as an array of

circuits are exposed one at a time requiring the wafer to be moved and exposed multiple times. Alignment of the mask is also time-consuming to ensure the pattern is aligned correctly to avoid either overlapping or gapping of circuits. Either way more elaborate and complex methods and equipment are required to achieve features on the order of tens of nm using photolithography. However, there is another method of achieving nm sized features.

(b) E-beam Lithography

E-beam lithography [184] uses electrons to generate patterns in resists instead of photons as in photolithography. The advantage of using electrons is their wavelength is much smaller compared to the photons used in photolithography (less than 0.01 nm [185]) which is calculated de Broglie relation:

$$\lambda = \frac{h}{p} \qquad 35$$

Where h is Plancks constant and p is the momentum of the electron. The electrons are generated and accelerated towards the sample using magnetic and electric fields to direct them. These electrons require a relativistic correction due to the velocity the electrons reach after acceleration changing Eq 35 to [186], [187]:

$$\lambda = \frac{h}{\sqrt{2\, m_0 e\, E^*}} \qquad 36$$

Where m_0 is the rest mass of the electron, e is the charge of the electron and E^* is the acceleration voltage with relativistic corrections; for an acceleration voltage of 10kV, the wavelength of the electron would be 12.2 pm. Features on the size of tens of nm can be written using this method, allowing higher precision designs to be created. The mask writing process can be slower compared to photolithography (in the order of hours or days compared to seconds or minutes) with larger designs because of the smaller area that can be exposed.

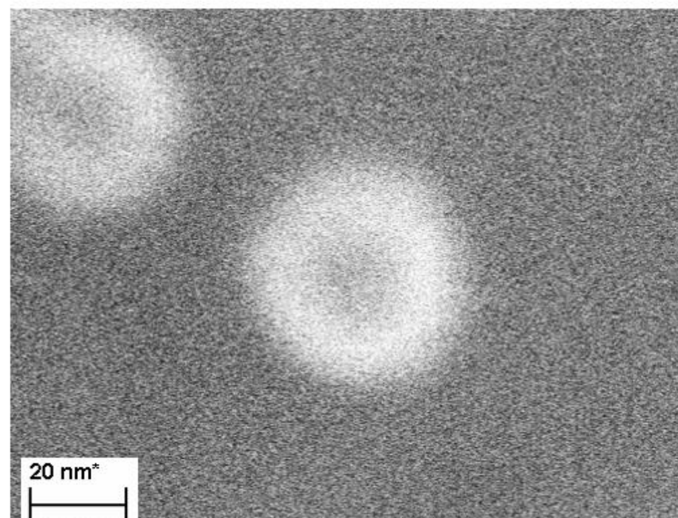


Figure 24 : Burn spot used for focusing electron beam

A well-focused, circular electron beam is necessary for writing accurate and precise designs. This is done by exposing an area, not to be written on, to the electron beam for some time (30 s – 1 min depending on the beam energy and how well focused it is), allowing a build-up

of burnt resist to pile up higher than the resist layer. This creates a ring that can be focused on Figure 24. Repeating this procedure allows the beam to be focused and determine the spot shape that can be altered to be more circular by changing the astigmatism of the beam. With the increased focusing the amount of time required to burn a spot reduces as the beam becomes more focused.

Once the spot has been focused and adjusted, the off-stage deflection of the beam needs to be calibrated. The write field is the area in which the electron beam is scanned across, writing the pattern. Once the pattern in the write field is written, the sample is moved to the next write field. To ensure the next write field is next to the previous a write field, alignment is required. A misaligned write field will cause stitching errors to occur, which can create gaps in waveguides or patterns written in the wrong area, Figure 25.

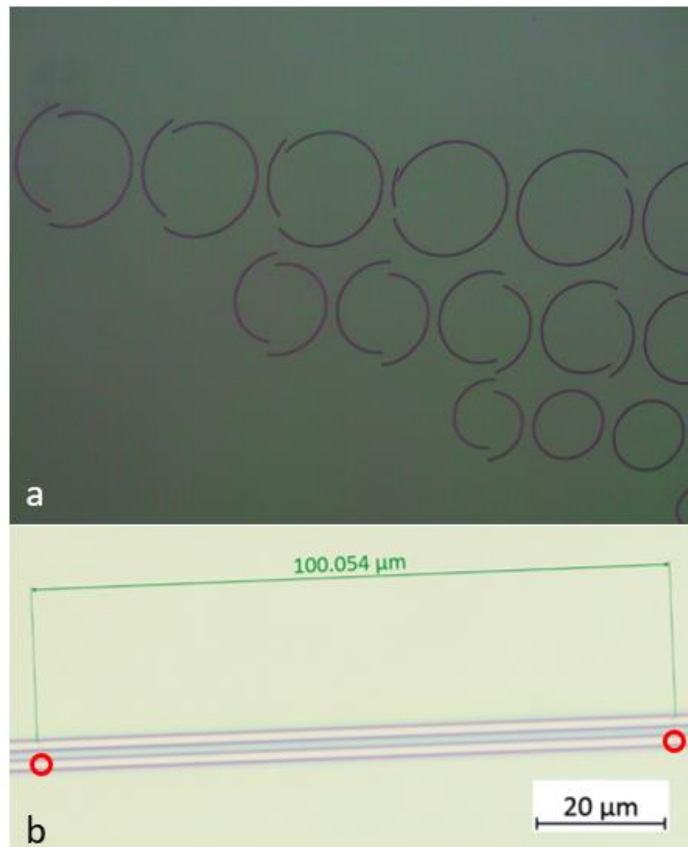


Figure 25 : Stitching errors a). Write field incorrectly aligned, b). Stitching errors 100 µm apart, same size as write field

Once the write field alignment is done the stitching errors should no longer be noticeable however, with large designs each time the stage moves from one write field to the next, the stage can drift slightly, causing a misalignment of the write fields. This misalignment will vary from tool to tool depending on the stage. Misalignment can be avoided using alignment markers placed periodically along the design that an automated alignment procedure can use to account for this drift [188]. The effectiveness of the automated alignment is determined by the quality of the alignment markers. Clear, well-defined markers are required to ensure an accurate alignment. Any imperfections in the alignment markers will cause an incorrect alignment of the write field and will cause errors in the

write. Alignment markers are usually done using photolithography due to the size of the markers and avoids any reliance on the e-beam being aligned if written using the e-beam.

b) i) Proximity Effect

There are a few factors that can affect the e-beam write [189], [190]. One that has a significant impact is the proximity of features to each other. When features are in proximity to each other, the initial electron beam can be spread due to forward scattering, from interactions with other electrons; or back scattering, due to interaction with the nuclei in the substrate. The forward scattering only deflects the electrons at a small angle while the back scattering can cause the electrons to be deflected at much greater angles as can be seen in from the Monte Carlo simulation in Figure 26.

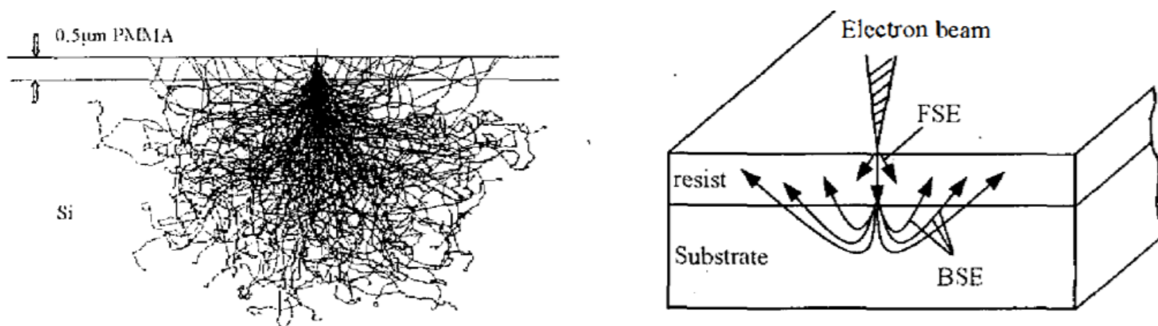


Figure 26: Monte Carlo simulation from [191] *demonstrating the different scattering occurring during an e-beam write. The main to the proximity effect is the back scattered electrons.*

This backscattering is the main cause for unintended areas of resist to be exposed, causing designs to merge in the case of negative resists as seen in Figure 27.

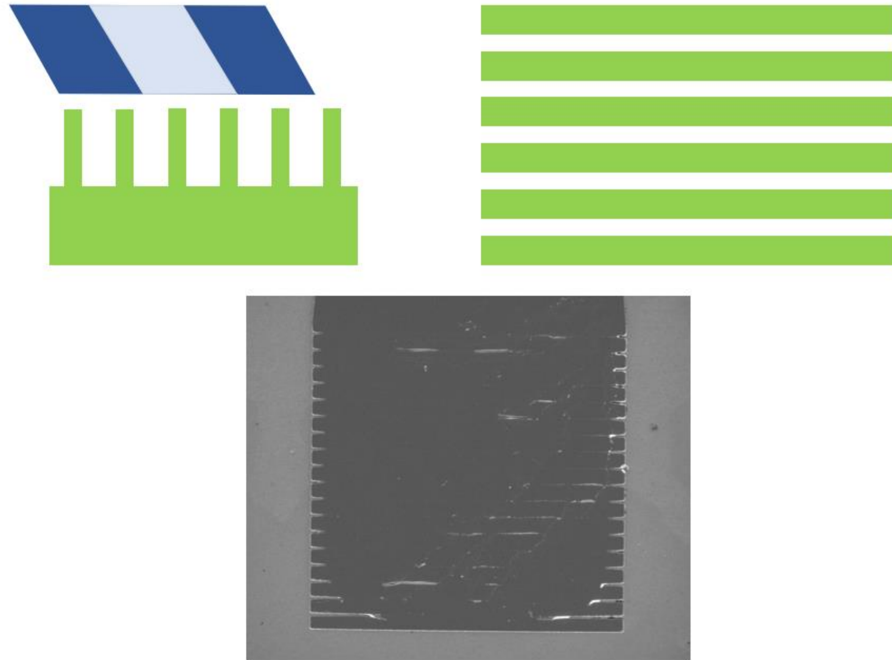


Figure 27 : Top left: Side profile of grating coupler with fibre above. Top right: Top view of grating coupler. Expected pattern to be achieved after e-beam lithography. Bottom: Grating coupler where the spacing between gratings (238.5 nm air gap, 715.5 nm GaN strip) has been overdosed due to the proximity of the grating to each other.

The exposure intensity distribution of this can be approximated by a double Gaussian profile [192],[193]:

$$f(r) = \frac{1}{1+\eta}\left(\frac{1}{\pi\alpha^2} exp\left(-\frac{r^2}{\alpha^2}\right) + \frac{\eta}{\pi\beta^2}\exp\left(-\frac{r^2}{\beta^2}\right)\right) \qquad 37$$

where the first term with range α is the forward scattering term, the second term with range β is the backscattering term, the parameter η is the deposited energy ratio of the backscattering component to the forward scattering component, and r is the distance from

the point of electron incidence. Proximity Effect Correction (PEC) techniques have been developed [194], [195], to account for this by adjusting the size of the designs or the dose received Figure 28. However, these variables are dependent on the resist, its thickness, and the substrate.

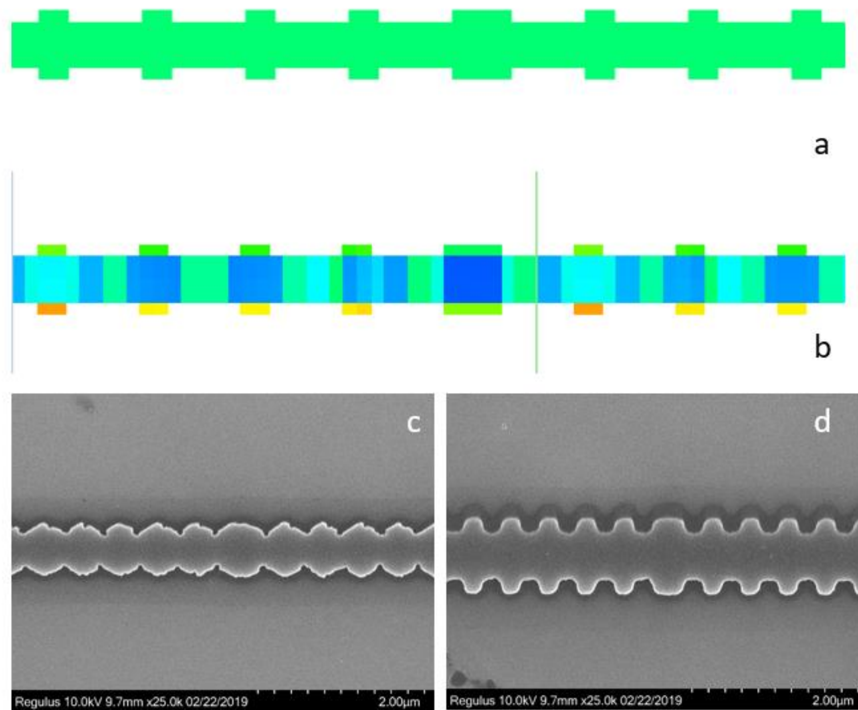


Figure 28 : a). Original design, b). Single design taken from array of designs after PEC hence asymmetry, c). Ni mask without PEC, d). Ni mask with PEC. Much closer to intended dimensions.

Lithographic tuning can also be used to determine the correct feature size and dose required to obtain the desired dimensions. This involves creating a dosing matrix consisting of multiple copies of the design with different doses and feature sizes that, once written and developed, the designs can be measured to find the correct dimensions. Thereby obtaining the appropriate design and dose parameters Figure 29.

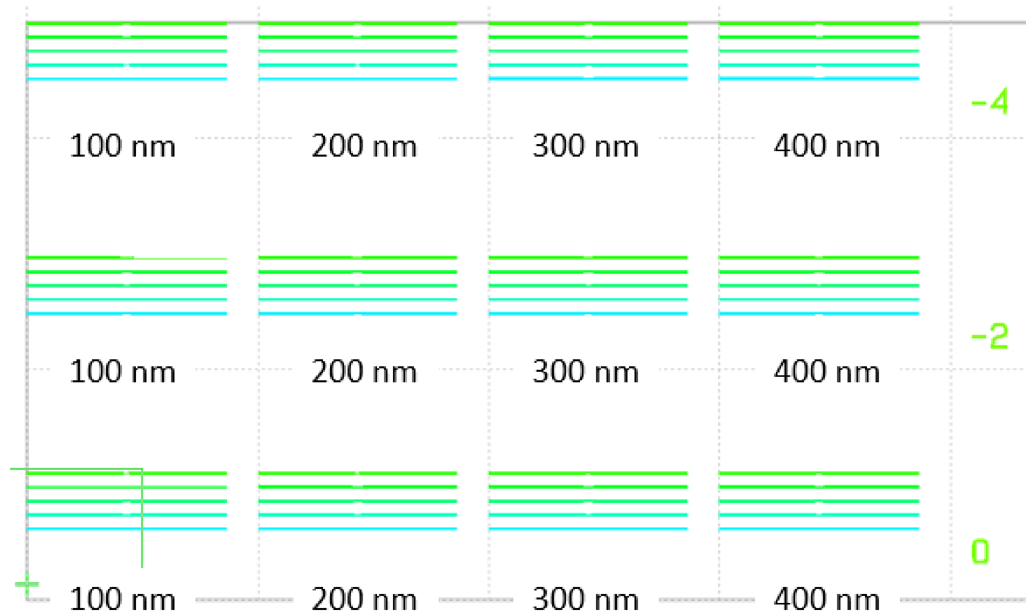


Figure 29 : DC dosing matrix varying the dose factor (indicated by varying colours), the design gap between waveguides (in each column) and varying waveguide dimensions by 2% increments (in each row). For instance, the bottom left grouping of DCs have a varying dose factor from 0.4 to and 0.8, have a designed gap of 100 nm and have no (0%) change of waveguide dimensions. The group to the left has all the same parameters except for a designed gap of 200 nm and above have the same parameter but with waveguide dimensions reduced by 2%.

b) ii) Charging

Another issue associated with e-beam lithography is the charging of a sample. Wafers on an insulating substrate or are insulator themselves have an issue where the charge from the electron beam cannot be discharged and causes the charge to build-up on the wafer. This build-up of charge can deflect the electron beam and affect the quality of the write [196], [197]. It also makes the focusing and shaping of the beam nearly impossible. The longer the beam is left exposed to the sample, the more the sample charges and causes the beam to

drift, Figure 30. The result is that a line is drawn rather than a spot, so the shape of the spot cannot be determined and during focusing any feature used becomes washed out by the charge. The inability to focus and shape the beam results in an overall reduction in resolution.

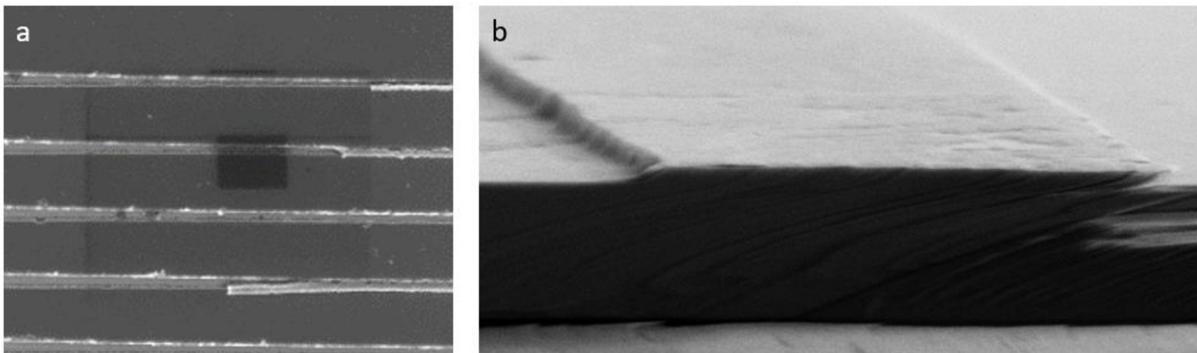


Figure 30 Examples of charging effects during e-beam lithography. a). Dark rectangles visible where e-beam has been in area causing specific areas to charge. b). Image distorted due to sample charging during e-beam raster scan of sample.

This issue can be overcome by depositing a thin layer of metal (around 10 nm) on top of the e-beam resist, creating a conductive layer that can remove the charge without detriment to the write [198].

This process allows designs on the order of tens of nm to be written however, it can be significantly slower to do in comparison to photolithography. A combination of photolithography and e-beam lithography can be used as a compromise, where a combination of large features and small features are included in the same design. However, alignment between the different features is crucial to reduce the losses due to mismatching of structures.

3.1.2 Etching

One of the most important steps in the fabrication process is the etch step. This can rely on a combination of physical and chemical etching.

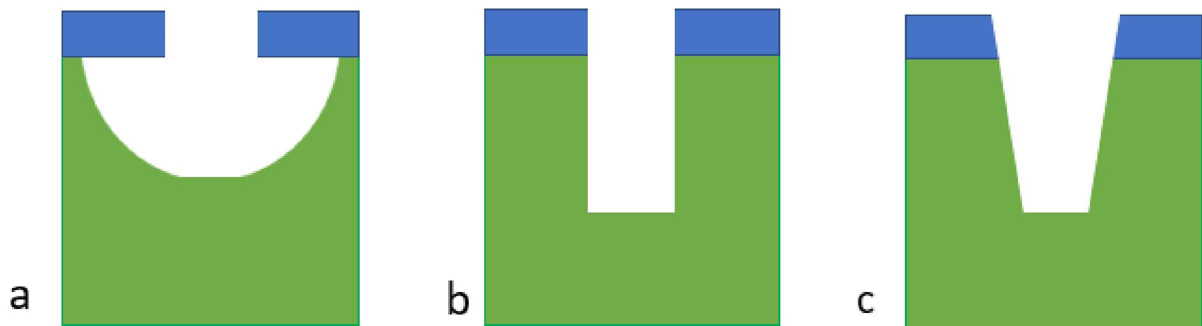


Figure 31 : a). Isotropic etch, b). Isotropic/anisotropic combined etch, c). Anisotropic etch

Chemical etching is an isotropic process, removing all surfaces exposed to the chemical at a similar rate producing rounded, under etched features like Figure 31a while physical etching is an anisotropic process and creates sidewalls like Figure 31c. A combination of the two processes creates a sidewall profile like Figure 31b. For integrated photonics and this thesis, the etch process is very important to reduce losses associated with sidewall roughness as well as waveguide structure (verticality, shape, under etch, etc). Each have their merits and issues as discussed below.

(a) Wet Etch

Wet etch involves the submersion of a sample into a solution, such as hydrofluoric acid (HF), so the exposed surface is removed chemically. This is usually an isotropic etch [199] but through careful manipulation of chemicals, concentrations, temperature, etc. an anisotropic etch can be achieved [200]. The crystallographic orientation of the material can be an issue, as different orientations can etch at different rates but can also be used for anisotropic etching [201]. When the directionality of etching is not important wet etching is appropriate but for more precision directionality, dry etching is used.

(b) Dry Etch

Dry etching works by accelerating ions generated in a plasma towards a sample and through a combination of physical and chemical processes remove the exposed sample. As mentioned previously, chemical etching is an isotropic process, however, physical etching is anisotropic. This anisotropic nature of the physical etch is what creates vertical sidewalls because of the directionality of the ions.

The ion bombardment breaks away the substrate however, this can also cause damage to the sample [202]. To reduce the damage a combination of heavy ions, such as argon, and reactive species, such as chlorine, are used so both physical and chemical etching takes place [203]. The reactive species also react with the removed substrate to avoid redepositing onto the sample. Through careful selection of conditions (pressure, temperature, bias, flow rate) [204], the profile of the substrate can be tailored to achieve smooth vertical sidewalls. Although the correct conditions will help with the smoothness of

the sidewalls, ultimately it is the quality of the mask that will determine the sidewall roughness.

For a more precise and direct etch, dry etch is the best option. While for a less precise, cheaper etch, wet etch would be better.

All the processes described above give an understanding of some of the processes used in this thesis. The experimental development of the flow process to create PICs is given below.

3.2 Fabrication Process Development

During the creation of this flow process various challenges were encountered. The process towards the solutions is detailed below, with impacts on the result.

3.2.1 Sample Preparation

All new samples were given a solvent bath and checked under a microscope to ensure the surface was clean, so a good adhesion of the resist was achieved. The resist was spun onto the sample and baked in ready for the lithographic mask design transfer. For photolithography, a SF11/S1813 bilayer was used and for e-beam lithography, a 950 PMMA A4 resist was used.

When a sample needed to be reworked, for photoresist samples, a more extensive solvent wash with additional solvents washes was required. This was followed by an oxygen plasma etch in an asher [205] to remove any residual photoresist that was not removed during the solvent bath.

For e-beam resist samples, overdosed PMMA appears to harden [206] which can cause ghost images of previous writes to appear when developed Figure 32. This can be overcome by following the previous procedure but using a more intense oxygen plasma etch. This will remove all residues from the surface regardless.

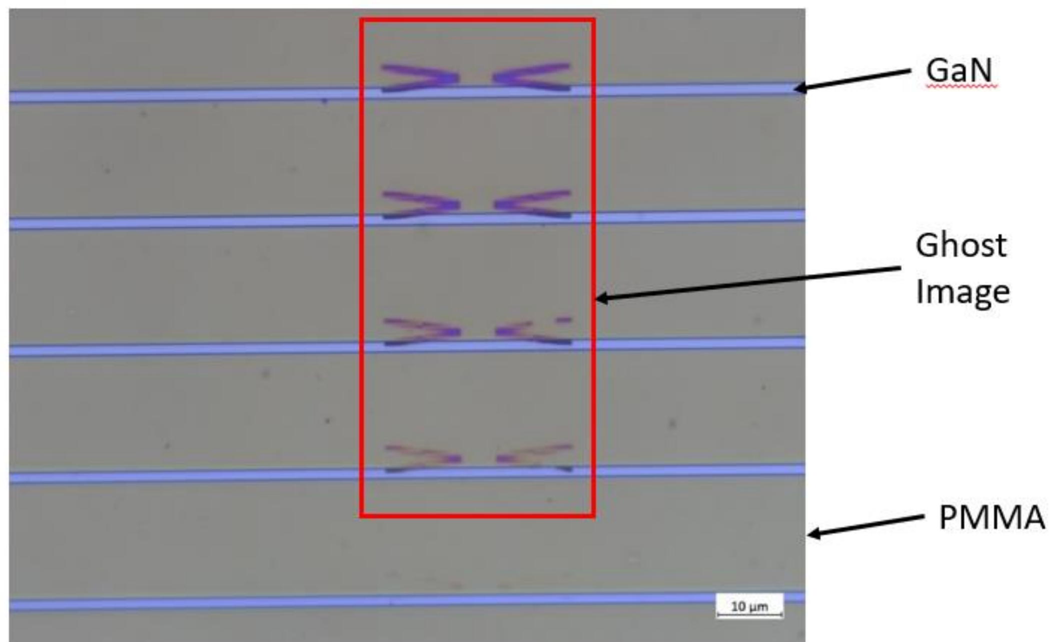


Figure 32 : Optical microscope image of ghost image from previous e-beam write appearing on sample after new write despite standard cleaning procedure. White – GaN substrate, Yellow – PMMA post development, Purple – Ghost image of pervious write

More detail about any of the preparation steps can be found in the Appendix.

3.2.2 Lithography Development

(a) Photolithography

The SF11/S1813 bilayer is exposed for 5 s and developed for 30 s in MF319 photoresist developer. The 2 µm lines produced have a line width of 3.9 µm Figure 33, 1.9 µm wider

than expected. There are mechanical aspects of the tool, such as the time delay for the shutter to open and close as well as power fluctuations in the lamp, that can affect the exposure of the pattern. It is more difficult to control the exposure compared to the development given the short time for the exposure. Shortening the development time to account for the 1.9 µm discrepancy is easier and allows more control over the final feature size. These structures were used as a test pattern to determine the performance of the tool.

Figure 33 : Optical microscope image of 3.9 µm lines created using photolithography on Si intended to be 2 µm using SF11/S1813 bilayer exposed for 5 s and developed for 30 s. Reduction in development time required as more control of the development rate than exposure. Black line edge of photoresist.

(b) E-beam

The write was done at 10 kV with a dose of 165 µAs/cm^2, 10 µm aperture and 500 µm writefield. The initial development was done in Cardiff using a Raith system but due to issues with the e-beam tool the final successful write was done in Bristol.

A single layer 950 PMMA A4 resist is used for the write of the directional couplers and gratings to be fabricated. The directional coupler gap was the focus of the e-beam development predominantly as this was the smallest feature (100 nm) to be fabricated in the design. However, due to the sensitivity of the grating couplers to fabrication variation this was optimised simultaneously as part of a cutback measurement design, Figure 34.

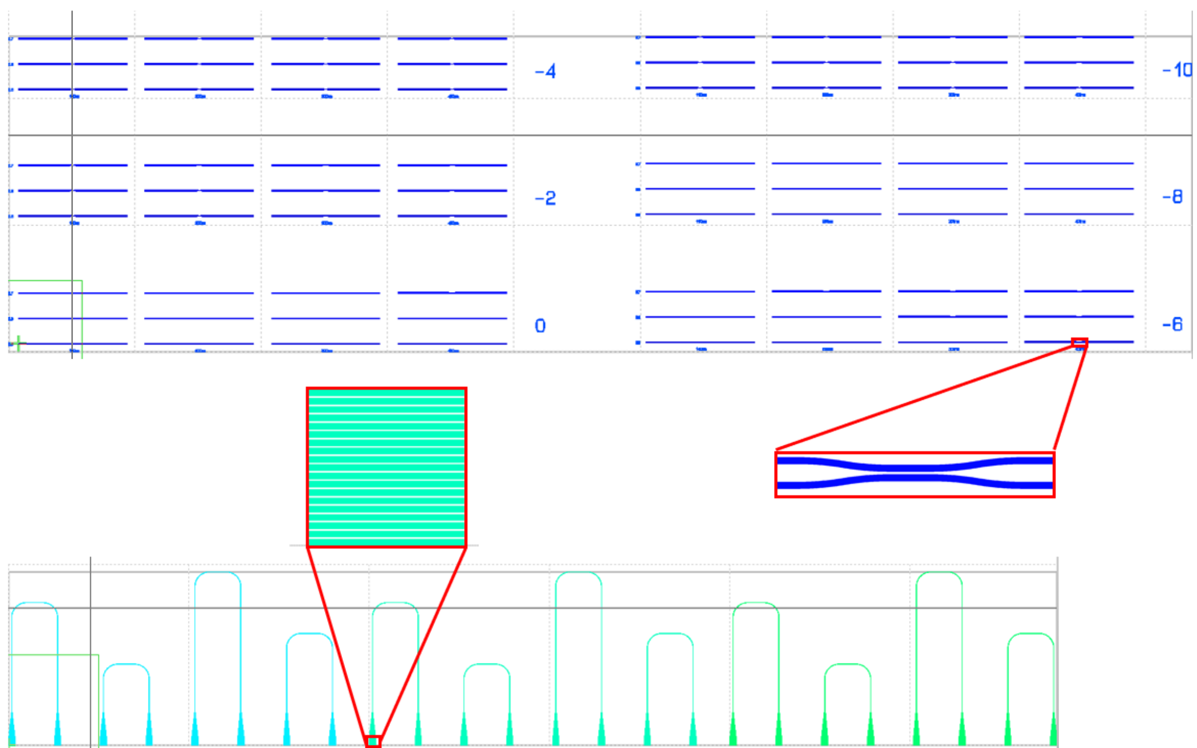


Figure 34 : E-beam designs to be optimised for DC and grating couplers. 18 x 18 µm grating coupler with grating period = 954 nm and fill factor = 0.75 designed to be etched to substrate by Simeng Jia [207] *for this thesis and her own. Directional coupler with 100 nm coupler gap in coupler region.*

GaN on sapphire suffers from charging effects due to the sapphire base being an insulator [208], not allowing the charge to discharge from the sample. A metal clip is used to secure the sample in place and allows some conductance for the charge however, this is not

substantial enough to discharge it completely. To avoid this a 10 nm layer of Al is deposited on top of the resist to conduct the charge away without effecting the write, Figure 35, as mentioned in Section 3.1.1b)ii). This is removed after the write using MF319 before the PMMA is developed.

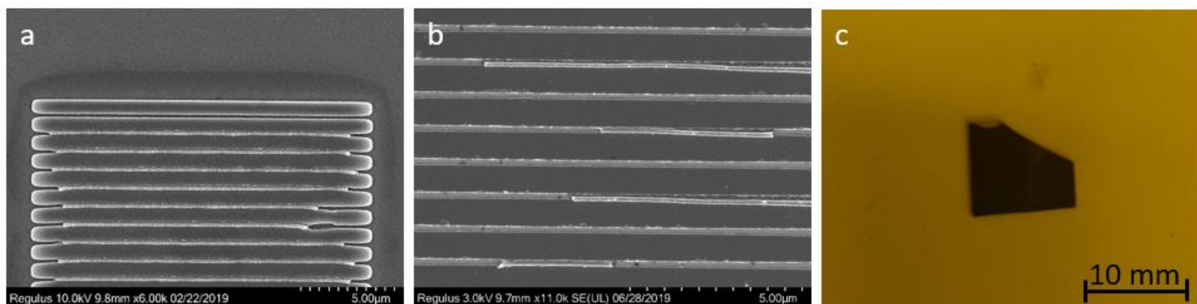


Figure 35 : Comparison between writes without a). and with b). Al layer deposited. Mask edges smoother in b). and more lines have lifted off between gratings. c). GaN sample with thin Al layer.

Figure 36 shows the difficulty to achieve a 100 nm gap using e-beam lithography due to the proximity effect and the problem of GaN on sapphire charging.

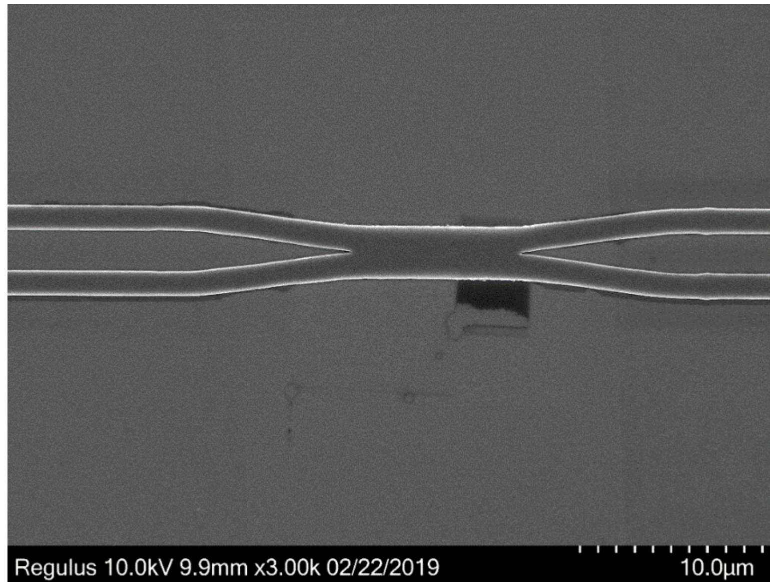


Figure 36 : SEM image of a directional coupler device fabricated on GaN. Without proximity effect compensation, the image shows an over-exposed gap – originally intended to be 100 nm wide. Black square result of sample charging when magnified.

Although lithographically 100 nm has not been achieved it is more important that after etching, the gap between the waveguides is 100 nm. A larger gap of 300 nm with a dose factor of 0.7 in the mask is required to achieve this as seen in Figure 37; this is prebiasing the pattern.

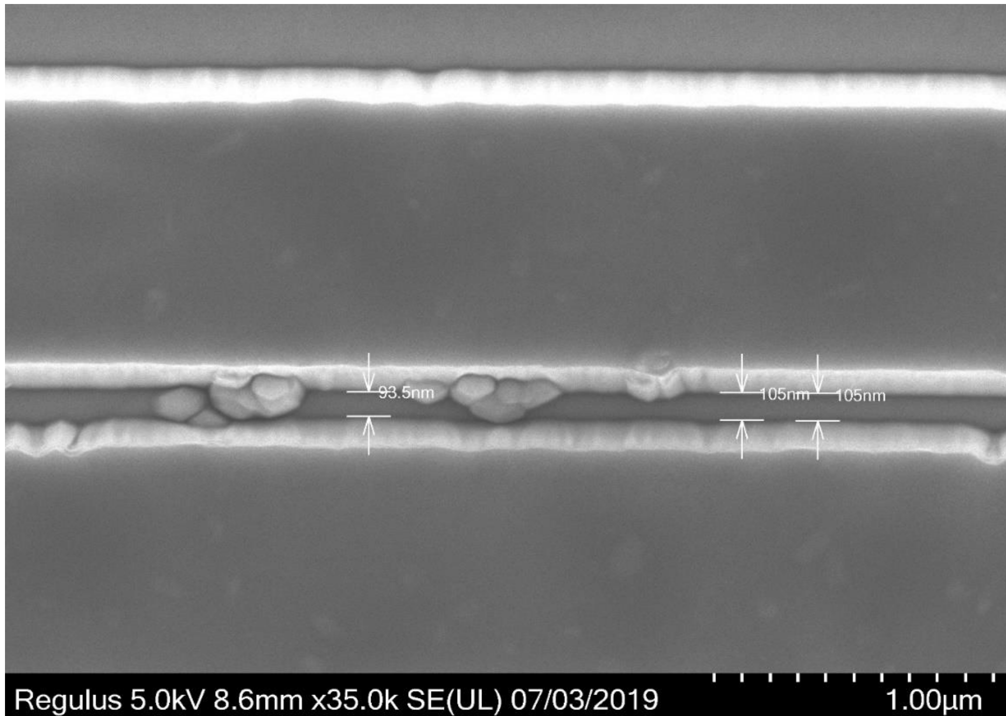


Figure 37 : SEM image of coupler region in DC. Approximately 100 nm gap achieved using a 300 nm lithographic design gap with a dose factor of 0.7 on GaN.

3.2.3 Etch Development

(a) ICP-RIE Dry Etch

A common chemistry used for the etching of III-V materials is chlorine-argon [209], [210], as used for the initial development of the GaP recipe. By varying the pressure, bias and flow of the gases, an etch matrix can be developed to determine the optimal combination of conditions to achieve vertical smooth sidewalls. The initial etch recipe to be optimised is summarised in

Table 4 provided by Cardiff University.

Cl	4 sccm
Ar	36 sccm
Pressure	10 mTorr
RIE	200 W
ICP	500 W
Temperature	25°C
Etch Time	3 mins

Table 4 : Initial etch recipe for GaP and GaN to be optimised for vertical, smooth sidewalls

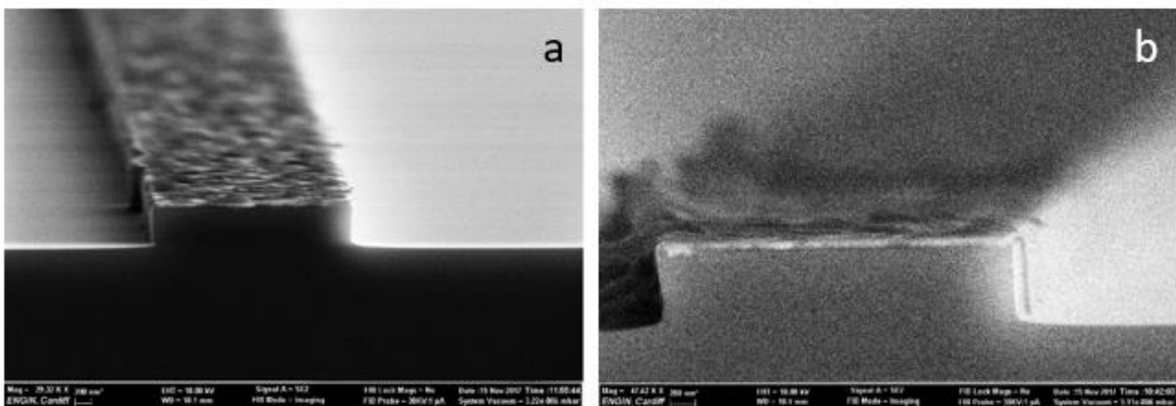


Figure 38 : Etched GaP waveguides using Cl/Ar chemistry with pressures at a). 10 mTorr and b). 14 mTorr

Increasing the pressure increases the etch rate of the GaP as seen in Figure 38 but does not seem to have a significant effect on the sidewall angle. The results of varying the etch pressure can be seen in Figure 39:

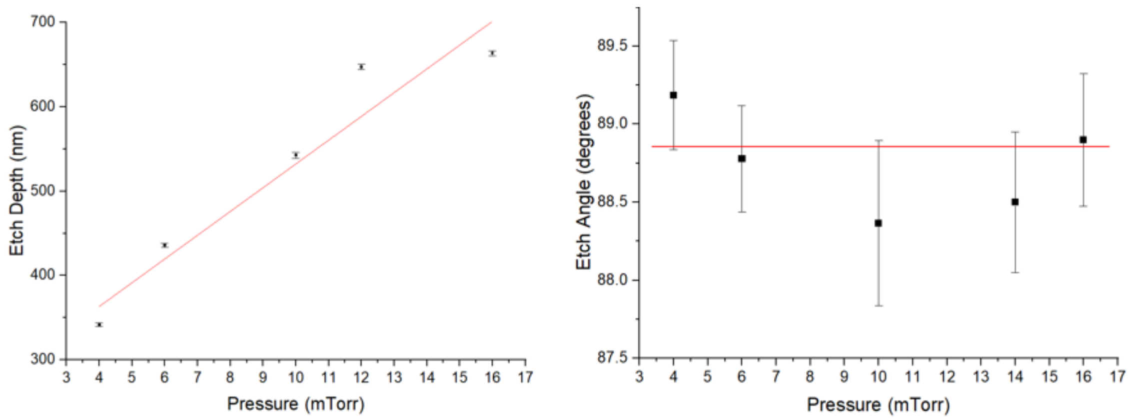


Figure 39 : Graph showing comparison of etch depth and angle against pressure for GaP. The etch length for each pressure variation was 1 min. While the etch rate increases with increasing pressure (red line indicates a rate of 28 mm/mTorr), it appears to have no significant effect on the etch angle averaging at around 88.7 ^{o}.

For the initial GaN etching a similar trend is observed with the variation in pressure as shown in Figure 40.

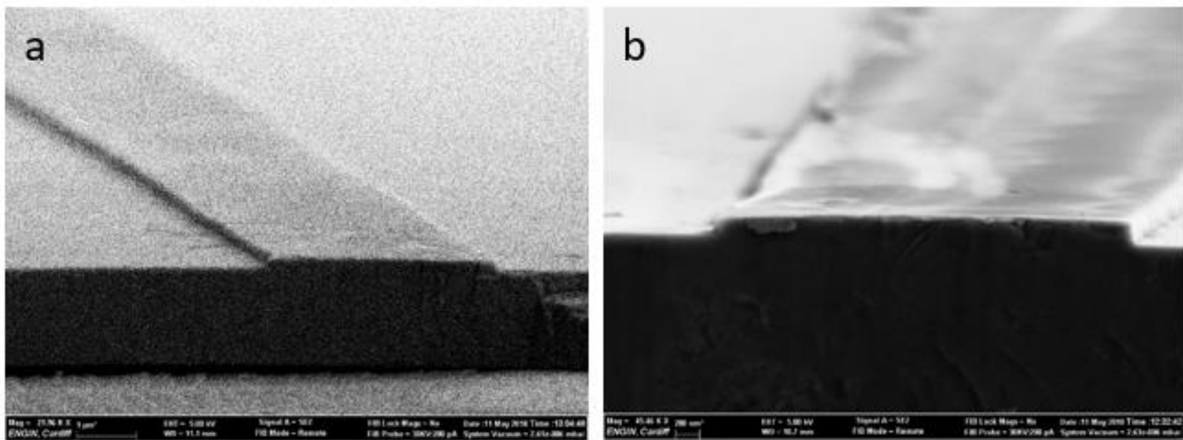


Figure 40 : Etched GaN waveguides using Cl/Ar chemistry with pressures at a). 6 mTorr and b). 10 mTorr

An alternative etch recipe using chlorine and argon, which will be referred to as Cl/Ar-2, was also used for comparison to monitor the optimisation progress of the partially optimised etch recipe. The intention is to achieve a smoother more vertical sidewall compared to Cl/Ar-2; this was provided by a colleague at Cardiff University. Cl/Ar-2 gives similar results to the partially optimised etch recipe but with a visibly smoother finish to the sidewalls Figure 41. Details for the Cl/Ar-2 recipe are summarised in

Table 5.

Cl	50 sccm
Ar	10 sccm
Pressure	10 mTorr
RIE	120 W
ICP	800 W
Temperature	150°C
Time	3 mins

Table 5: Alternative Cl/Ar recipe, Cl/Ar-2, to etch GaN

Cl/Ar-2 has a higher Cl/Ar ratio, is at a higher temperature and has a higher ICP power compared to Table 4 making it a more chemical etch.

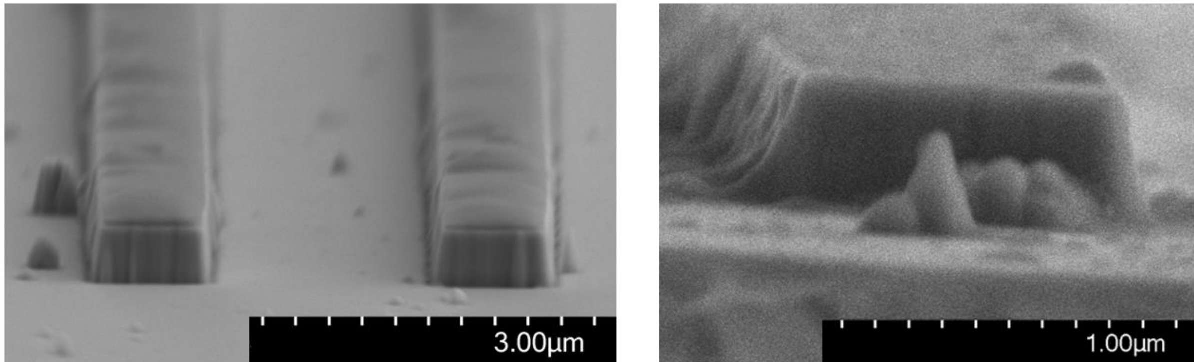


Figure 41 : GaN waveguide using (left) Cl/Ar-2 etch recipe and (right) Cl/BCl_3 recipe.

An additional recipe using chlorine and boron trichloride (BCl_3) Figure 41, propriety to Cardiff University, produces similar results, with the intention of causing low etch damage to the GaN surface.

A visual comparison of the sidewall smoothness between the BCl_3 etch and Cl/Ar-2 etch show the Cl/Ar-2 etch gives a smoother finish to the sidewalls compared to the BCl_3 recipe. While currently the Cl/Ar-2 recipe gives the better sidewall smoothness, with further optimisation of the initial etch recipe, improvement of the sidewall smoothness and verticality is still possible.

3.3 Conclusion

An initial flow process to create GaP and GaN waveguides to be used in the design of the MZI switch in the Simulations Chapter has been created. While there were challenges surrounding the e-beam lithography, an etched 100 nm gap was achieved from a 300 nm mask designed gap. Further development of the write will be required to ensure that the

3.7 mm long arms, predicted by the simulation, are achieved without stitching errors due to drift of the stage are considered. The development of the grating coupler will also be key to be able to couple light in and out of the circuit to perform cutback measurements for further recipe optimisation when visual improvements become less obvious.

Optimisation towards an etch recipe for GaP and GaN waveguides has begun with pressure and RIE bias variations so far. Other variables such as the gas ratio and temperature variations need to be done to obtain a fully flexed etch matrix. With this etch matrix obtaining the right conditions for vertical, smooth sidewalls for the waveguides can be achieved.

Low defect, high quality GaP should be possible due to the low lattice mismatch of GaP to Si ([140],[211]). For GaN, while the wafer structure in Figure 11 is readily available, it is not the best optical quality GaN available. For photonic structures to be created in low defect, high quality GaN development of alternative fabrication techniques are required. Such a fabrication development is detailed in the next chapter.

Chapter 4

4 Angled Cage Etch of GaN

GaN has many properties (high refractive index, Pockels coefficient, etc.) that make it attractive for integrated photonics as mentioned in the Introduction chapter. In the past, high contrast waveguides have been created in GaN on Sapphire wafers [212] with GaN having a refractive index of 2.3 [213] and sapphire 1.7 [214] at 1550 nm. However, silicon on insulator (SOI) has a greater refractive index difference, silicon 3.48 [215], SiO_2 = 1.4 [216] at 1550 nm, allowing smaller dimension waveguides with a similar confinement to GaN on Sapphire.

Another issue is, the defectivity of the GaN layer grown on sapphire is high, due to the lattice mismatch between GaN and sapphire (16% [217], [218]). While optical devices are still possible with this level of defectivity [219], with low defect GaN, optical losses would be reduced (optical losses come from the light scattering from defects and imperfections) improving the optical performance of photonic structures in GaN. GaN grown homoepitaxially produces the best optical quality GaN due to the lack of a lattice mismatch. However, it is impossible to create strip waveguides as there is no refractive index contrast between the layers of GaN; this makes device dimensions bigger and single mode operation more difficult.

A solution to both these issues is to create suspended photonic structures in air. It would be possible to create structure with dimensions capable of single mode operation, with a similar geometry to a strip waveguide, while simultaneously increasing the refractive index

contrast. Suspended structures in GaN [220] are already possible but uses a complicated, multi-step process to fabricate them. Suspended membranes in silicon are possible due to the ability to grow low defect silicon on a sacrificial substrate that can be removed easily post growth [221], [222].This is not the case for GaN as the substrates used to grow low defect GaN are hard substances and are not easily removed [223] while the use of a sacrificial layer results in optically poor quality GaN [224], [225].

In this chapter, we have created a novel solution to under etch GaN using an angled etch method. The angled etching uses an angled Faraday cage placed in the etching plasma. A brief outline of the theory behind the angled cage etch is presented followed by the development of the angled cage etch process with initial suspended structures demonstrated. The start of suspended photonic structures created using this angled cage etch are presented at the end.

4.1 Angled cage etch

A solution to creating suspended structures would be to use an angled cage acting as a Faraday cage, which shields the sample inside from the external field used to accelerate the ions. When the ions reach the cage, they are deflected at an angle perpendicular to the cages surface and travels unaffected by the electric field to the sample[1]; there is no electric field inside the cage. After constant angled bombardment from the ions, suspended structures in the GaN will be formed, Figure 42.

[1] [226] - Supplementary Material

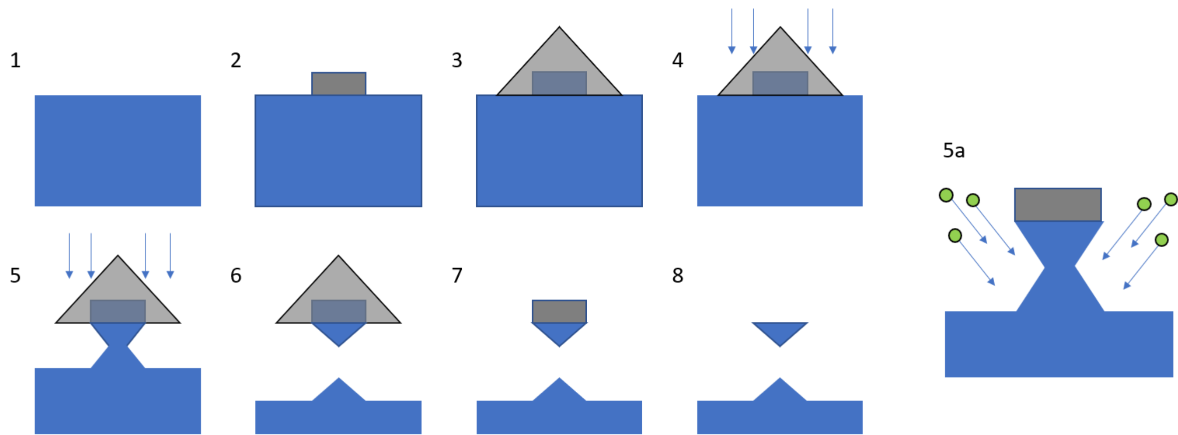


Figure 42 : Process to under etch GaN using an angle cage assisted etch. 1). Initial GaN wafer. 2). Metal mask design deposited. 3). Area to be angled etched placed under cage. 4). Ions accelerated towards sample. 5). Initial angled etch of GaN where ions are deflected towards the sample (5a) due to the lack of electric field inside cage. 6). GaN under etched until separated from GaN substrate. 7). Cage removed from sample. 8). Metal mask removed leaving suspended GaN structure.

A similar method is used in the creation of suspended structures in diamond [226] but an initial vertical etch is done to expose the sides. In comparison, for our method [86] the GaN is patterned and placed in the angled cage allowing an angled etch to occur from the beginning Figure 43. This method saves time and potentially money as only a single etch step is required.

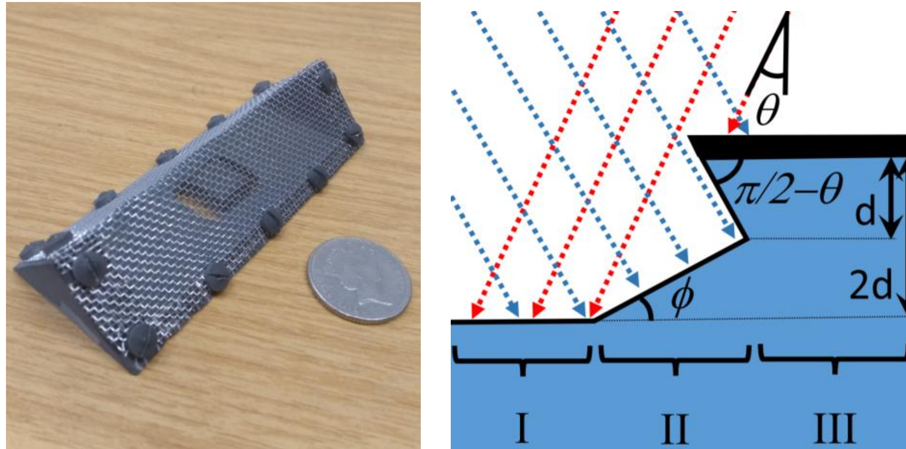


Figure 43 : Triangular Faraday cage used for angled etch. Equilaterial trianlge cross section with 45° angle, 70 mm length and mesh with spacing 1 mm using 0.25 mm diameter wire. Diagram showing the trajectory of the ion after deflection inside cage.

Creating suspended GaN structures this way would simplify the fabrication process to a single step method. Low defect GaN can then be grown on suitable substrates without the necessity for complicated multi-stage processes to create suspended structures.

4.1.1 Angled cage etch theory

The ion deflection diagram in Figure 43 shows there are 3 different areas of etching occurring inside the angled cage; the ions are deflected at an angle θ perpendicular to the cage surface. Area I will experience ion bombardment from both directions of the cage so experience twice the etch rate of Area II hence the total depth of the etch is $2d$, d being the etch depth. Area II only has ion bombardment from one direction due to the protective Ni mask defining the pattern creating the desired under etch profile. Area III is completely protected from any etching from the Ni mask. Angle φ (See Appendices) is equal to:

$$\varphi = tan^{-1}((3\,tan\,\theta)^{-1}) \qquad 38$$

For a structure to be under etched and suspended using this method it must have a minimum width, w, that satisfies:

$$2d\,tan\,\theta > w \qquad 39$$

4.2 Fabrication Process Development

With the information above the development of suspended structures in GaN is detailed below. Initial development of the mask to create the suspended structures is introduced followed by the development of the etch process and suspended structures created using this method.

4.2.1 Mask Development

Different designs were created using the angled etch method to create suspended structures. Both photolithography and e-beam lithography were used to create these structures due to the varying feature sizes.

For the photolithography, a bilayer mask consisting of LOR 3A and S1805 was used to create the pattern for a thick Ni mask (150 nm) to be deposited after. The thickness of the metal

mask means a bilayer resist is required as lift off after deposition using a single layer of S1805 would result in a poor lift off with winged edges to the mask Figure 44.

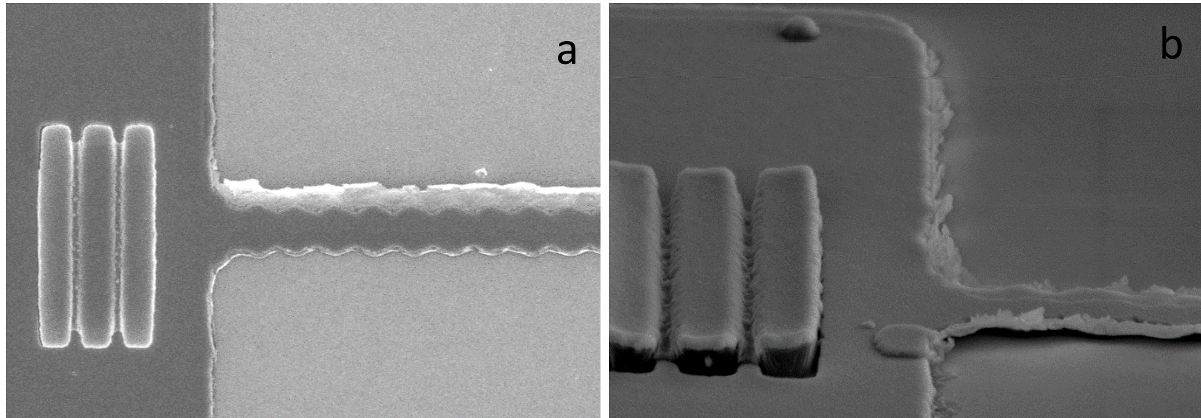


Figure 44 : Failed lift offs due to lithographic issues. a). Tearing and winged edge top view, b). Tearing and winged edge at 65° angle

LOR 3A and S1805 are positive resists so feature sizes can be increased with longer exposure or development time. Similarly, a bilayer mask consisting of MMA EL11 and 950 PMMA A4 was used for the e-beam lithography (EBL). The use of the thick Ni mask is necessary because of the aggressive nature of the etch and can strip the Ni off, before the structures are suspended Figure 45.

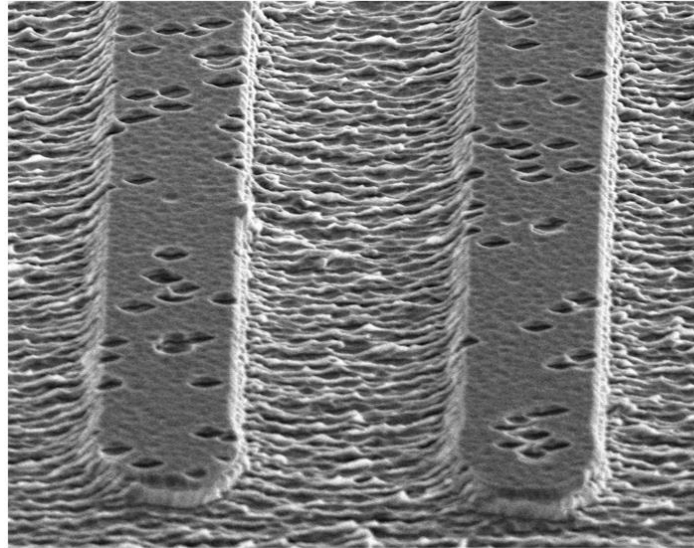


Figure 45: Ni mask has been etched away before structure has begun to be under etched

Warm acetone is used for lift off to leave the Ni design on the sample but unfortunately Ni flakes during the lift off process. Unless the sample is carefully manoeuvred through the warm acetone it is possible for the Ni to redeposit onto the sample, obscuring parts of the design, Figure 46.

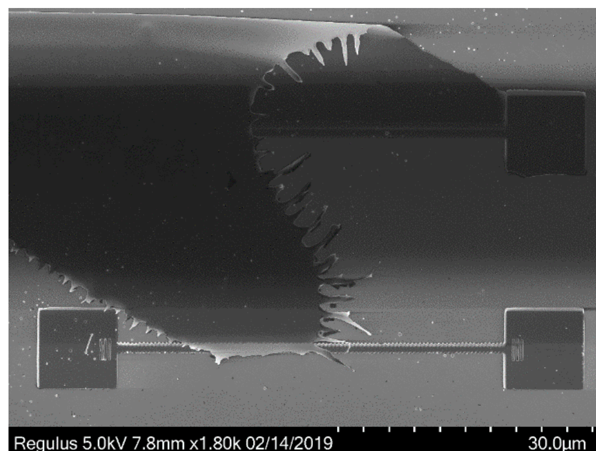


Figure 46 : SEM image of redeposited Ni after lift-off on GaN due to mask splintering causing metal mask of device to be covered.

The removal of the Ni mask after etch requires a 95:5 DI water: Nitric acid solution that can take a few minutes to remove depending on the length of time the Ni mask is left on the sample.

4.2.2 Cage/No Cage Comparison

A 45° angled cage with a triangular cross-section was used for the initial angled etch Figure 43. The cage and mesh are made of the same aluminium alloy that is used for the interior of the ICP tool to avoid any contamination of the tool. The length of the cage is 70 mm and the mesh has a spacing of 1 mm using wire of diameter 0.25 mm.

A comparison between an etch using the Cl/Ar-2 recipe from the Fabrication chapter can be seen in Figure 47 with and without the cage.

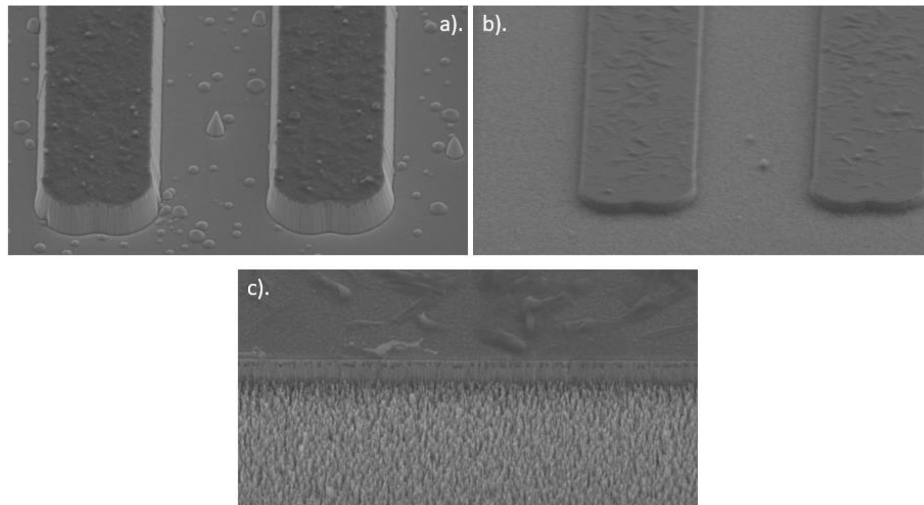


Figure 47 : SEM images of initial GaN etches using Cl/Ar-2 recipe a). with cage, b). without cage, c). Needle like structures (grassing) appearing around waveguides etched with cage.

The sample etched without the cage has a steeper outward angled ($\theta = -19^o$) sidewall profile compared to the samples etched in the cage ($\theta = -10^o$). A difference in etch depth is also visible with a shallow etch on the caged sample (~880 nm without cage, ~340 nm with cage). Although there is no under etching it is apparent that the cage is causing the ions to be deflected creating a slightly straighter sidewall; there is also an issue with grassing of the GaN surface. To overcome the grassing and to increase the under etch angle the ICP and RIE power was increased to 200 W and 1200 W respectively to accelerate the ions to a faster speed as seen in Figure 48 (TOP).

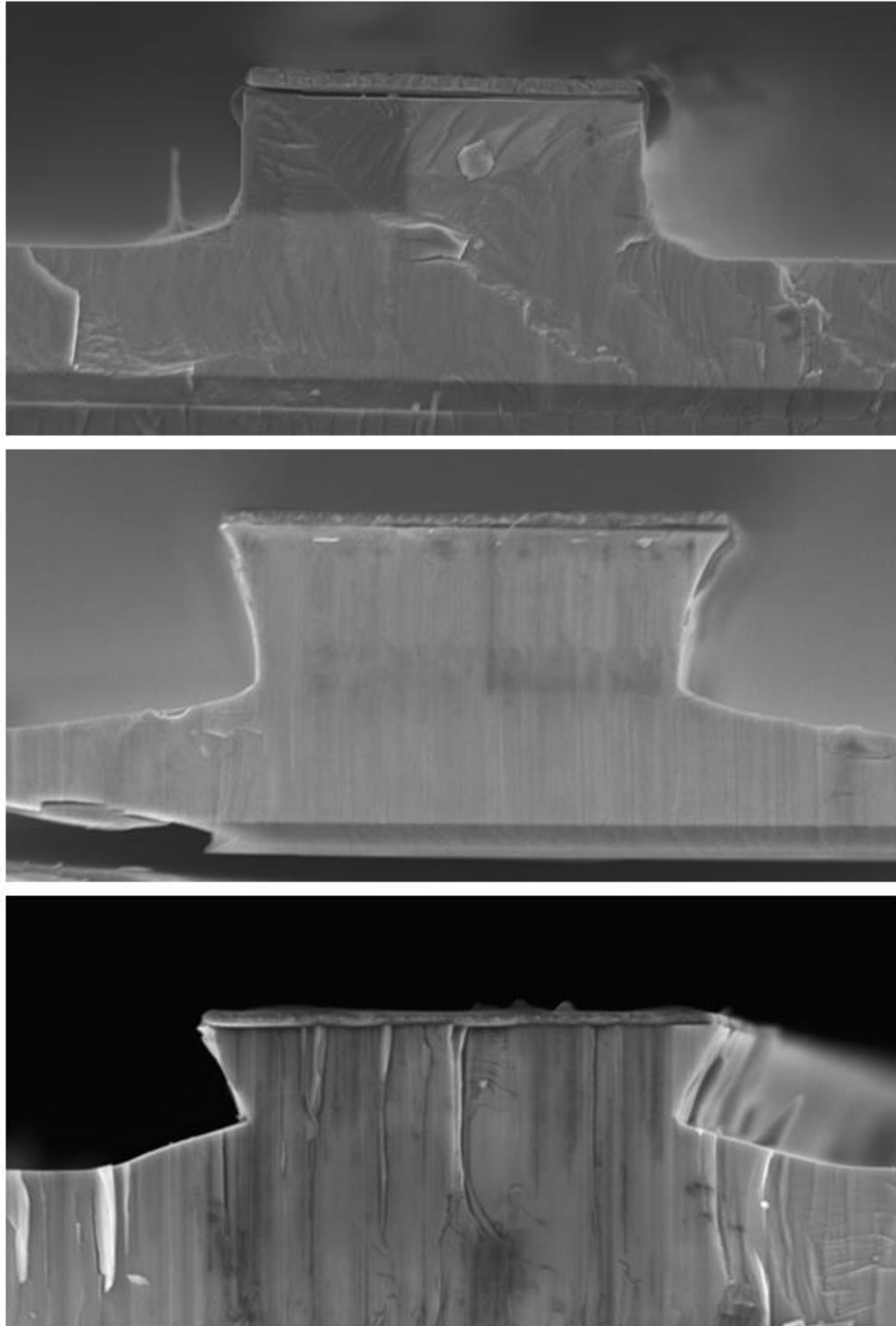


Figure 48 : SEM cross-section of 2 μm lines with increased ICP and RIE bias (Top), an equal Cl:Ar ratio (Middle) and finer cage mesh (Bottom). In Top image sidewalls are vertical (ϑ=0°) due to the increase in ion acceleration. A more balanced gas ratio produces the start of an under etched structure due to a more physical etch in the Middle image (ϑ=22°). The finer mesh used for the Bottom image further increases the undercut (ϑ=30°)

A more vertical etch is now achieved with no positive angle to the sidewall ($\theta = 0^o$) and grassing has been removed. The gas ratio of Cl:Ar was adjusted to be 1:1, 30 sccm each, to make the etch a more physical process and less reliant on the chemical, isotropic etch Figure 48 (Bottom). The start of an under etched profile ($\theta = 22^o$) is beginning to emerge from the more physical etch. To further increase the etch angle, a finer mesh is used to cover the cage as this blocks the external, vertical, accelerating electric field more [227]. With the coarser mesh there is still some vertical influence on the particles that are deflected and this reduces the deflection of the ions. With a finer mesh the undercut angle increases further ($\theta = 30^o$), but the expected angle of 45° is never achieved. There are a few reasons why this may be.

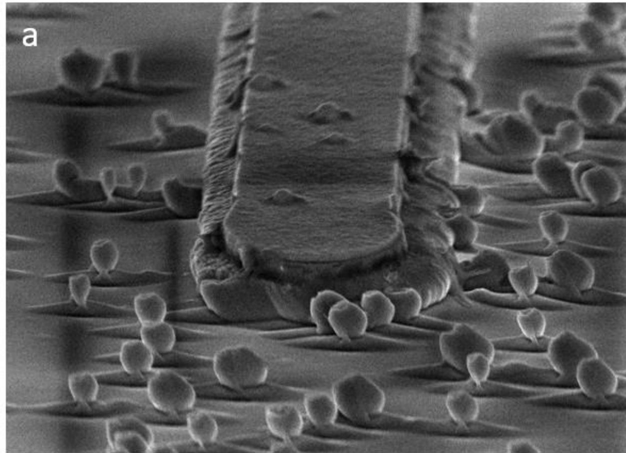
The mesh for the cage is held in place using screws that protrude from the surface that can distort the electric field causing the ions to deflect at angles undesirable for the under etch of the GaN. It is also possible for ions with a vertical trajectory to enter the cage, unaffected by the mesh. These can collide with the deflect ions adjusting their trajectory or reducing the etch. Ensuring a flat mesh across the angled cage is vital to ensure the ions deflect at a right angle to the mesh towards the sample and can also account for a smaller etch angle.

Other than the cage, during the etch itself the Ni mask will slowly be etched away. This will expose more GaN that can be etched and reduce the under etch of the GaN. Any inhomogeneities in the mask will also affect the angle of the etch and edge effects of the Ni can deflect the path of the ions. This expected angle only considers a physical etch and any chemical etch processes are not included.

Etch influences requires a much more thorough model beyond the scope of this thesis. However, considerations for the cage effects are easier to manage with a better designed cage. These are carried out for the angled etch for the suspended cantilevers.

4.2.3 Cantilevers

A mask consisting of singly clamped and doubly clamped cantilevers of varying lengths and widths was used to develop the under etch of the GaN with the higher bias and more physical etch to create suspended structures. A 60° angled cage, with a finer mesh, central beam and flatter screws, was used to create suspended structures with a more equilateral triangle cross section. Initial etches were not long enough to create suspended structures but was a promising start Figure 49a.



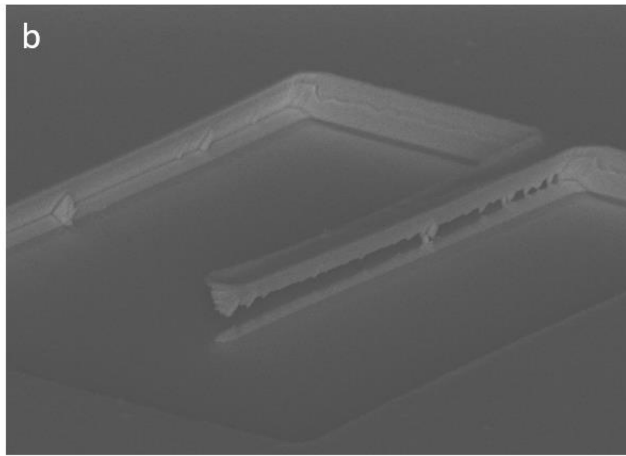


Figure 49 a). Initial cantilever etch using modified 60° angled cage for 7 mins using high bias, physical etch. Structures around cantilever caused by residual solvent drying on surface leaving marks. b). 45° angled cage etch for 12 mins using same recipe. Clear separation from the substrate. Still with Ni mask on.

However, given the etch angle of the 45° cage, $\theta = 30^o$, the cage was used again with successful results Figure 49b.

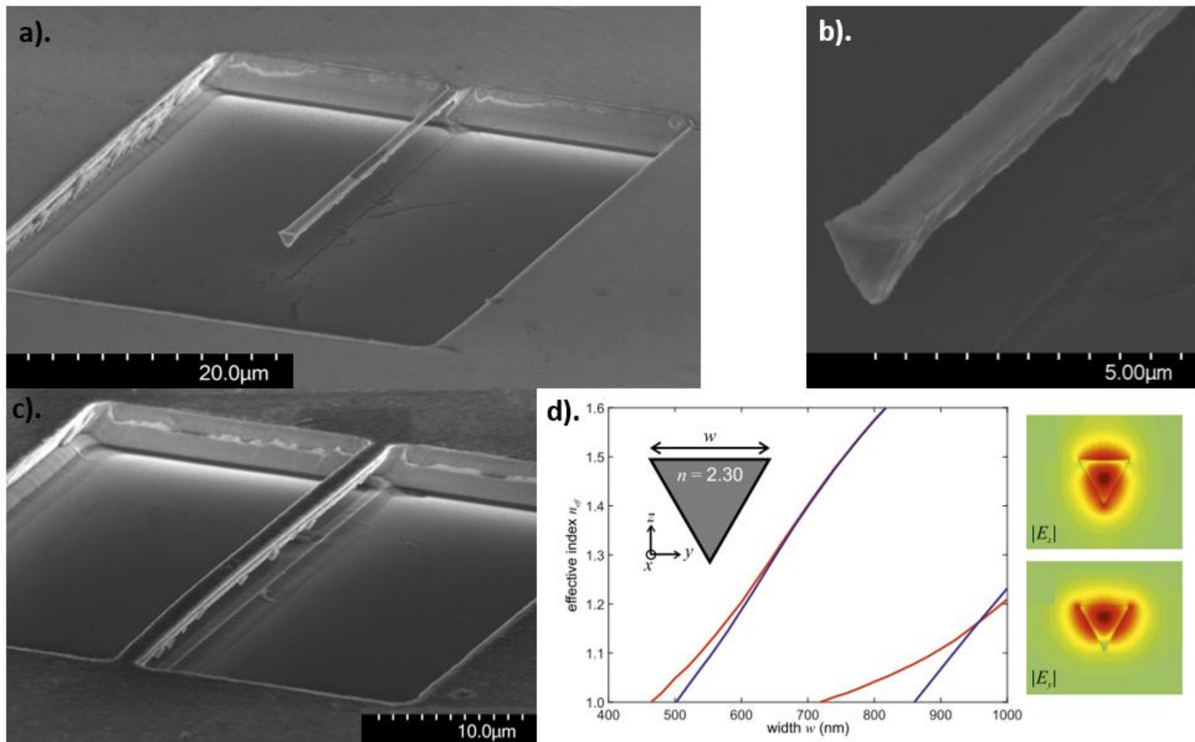


Figure 50 : Suspended cantilevers created using angled cage etch. a). Singly clamped cantilever, 18 µm long, 0.9 µm wide and 1 µm height b). Close up of a). c). Doubly clamped cantilever, 24 µm long and 1.4 µm width (Not possible to measure height due to angle of SEM but presume similar ratio as singly clamped cantilever), d). Simulation of supported waveguide modes in triangular waveguides.

It can be seen in Figure 50b that a triangular shaped cantilever has been under etched in the GaN. Figure 50 also demonstrates the strength of GaN given that a singly clamped cantilever of length 18 µm long, width 0.9 µm and height 1 µm Figure 50a and doubly clamped cantilever of length 24 µm and 1.4 µm width Figure 50b have stayed suspended after the removal of the Ni mask in nitric acid. It can withstand the surface tension exerted by the nitric acid. This triangular shape can be used as a waveguide with increased confinement of the light in the GaN waveguides, due to the suspension in air, as simulated in Figure 50d.

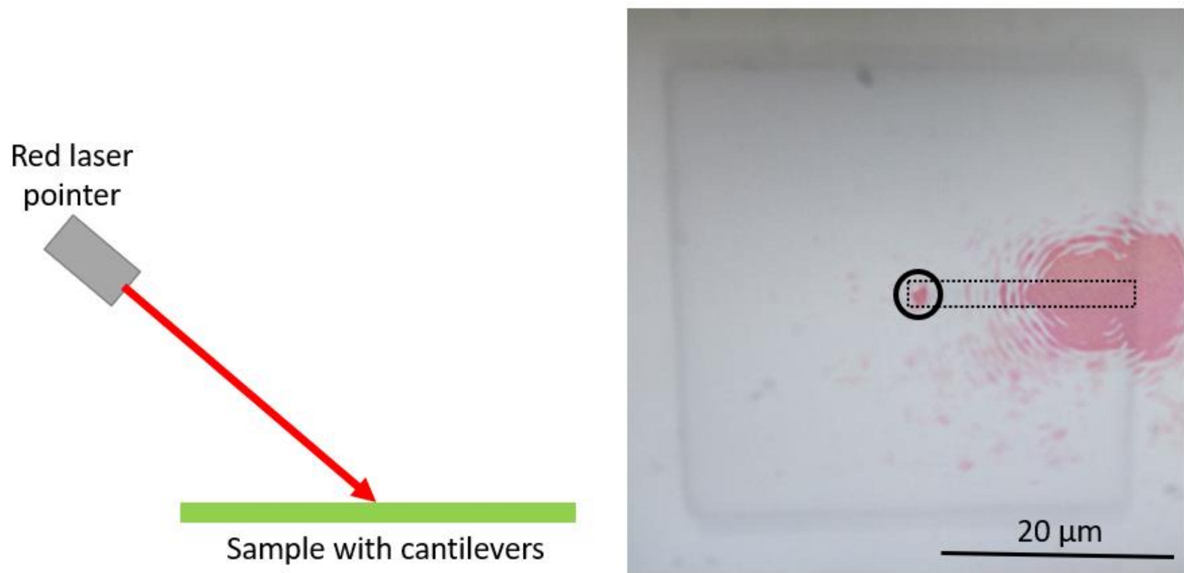


Figure 51 : Light emitting from the end of the cantilever in Figure 50a from above. Schematic of red laser pointer shone directly at end of cantilever. No grating structures used hence why so much reflection from surface of sample.

To demonstrate the triangular suspended structures ability to guide light, a red laser pointer was shone at the base of the cantilever where light can be seen emitting at the tip of the cantilever Figure 51. This indicates that the light has been confined in this triangle cantilever and travelled to the end. The optical transmission loss of the cantilever was not determined as this was used as a demonstration.

4.2.4 Rings and Discs

The angled caged etch is a versatile method of undercutting GaN provided you have the correct shaped cage. A conical cage Figure 52a was used to undercut circles and discs to create microrings and discs Figure 52b&c.

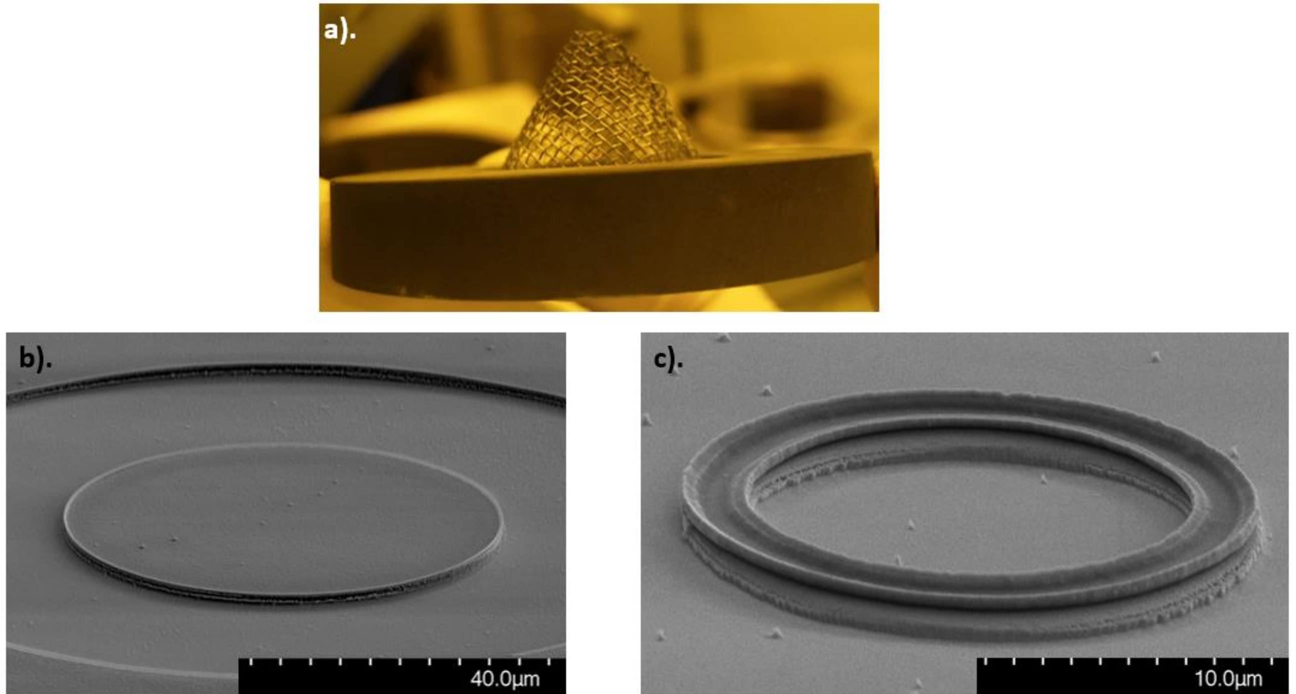


Figure 52 : a). Conical cage made from same material as triangular cage using initial mesh used to etch b) microdisk c). ring resonators

Ring resonators and microdiscs are key components in photonics; be it for switching [228], cavities [229] or optomechanical measurements [230]. The devices shown here are intentionally not undercut fully as additional supports would need to be added to suspend the rings and discs. Microdisks are usually fabricated on pedestals [230]. However, by varying the width in sections on the microring mask it is possible to undercut most of the ring while certain points are still in contact with the GaN [231]. An issue using the conical cage is that the angled etch occurs the entirety of the 360° cage causing the ions to focus their trajectories on a certain part of the chip Figure 53.

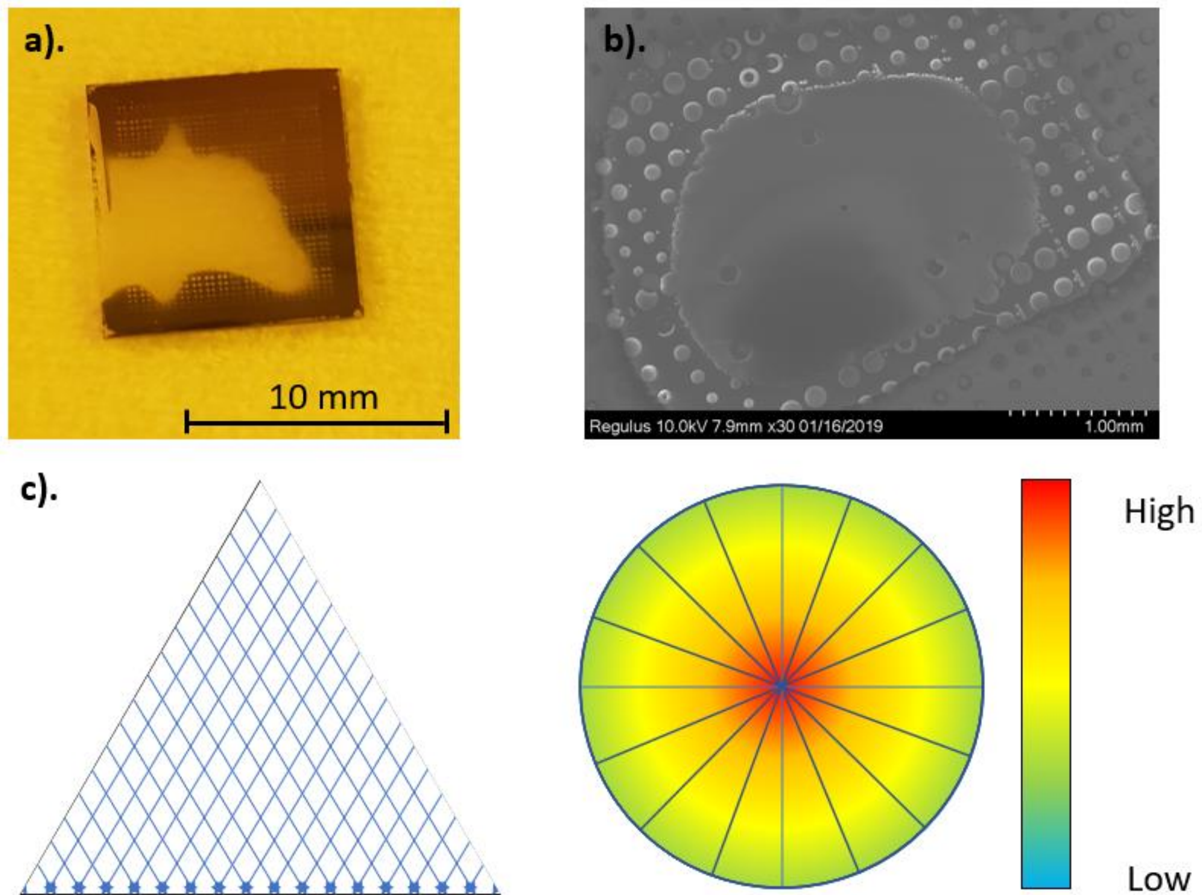
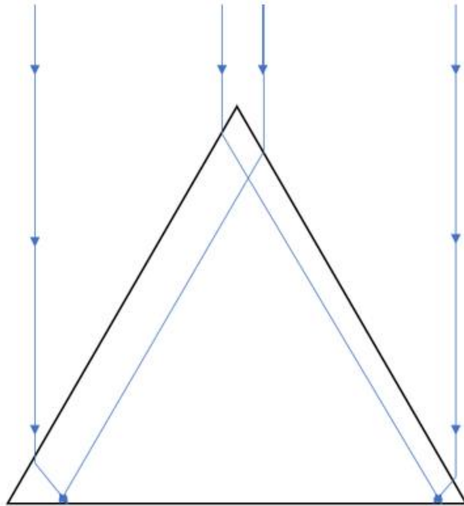


Figure 53 : Over etched region of conical cage where ion trajectories are focused. a). Visible to see by eye on GaN sample where Ni mask has been etched b). SEM image of focal spot, c). Representation of side and top down profile of ion flux in perfect conical cage.

This means the etch rate across the sample is not uniform; edges would experience a lower etch rate compared to the focal point of the cage. The mesh was added to the conical structure by hand making it difficult to create a conical cage that is symmetrical and round. As such, the focused spot caused by the ions is not a circular spot or necessarily at the centre Figure 53 a). and b). While this does allow the sample to experience a range of etch rates, effectively creating an etch matrix, the etch away from the centre is anisotropic Figure 54.



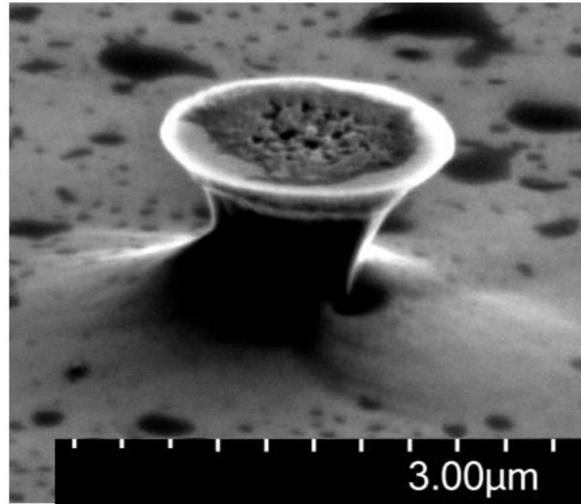


Figure 54 : Uneven etch of structure in conical cage. Left hand side has under etched more than right. Ions being deflected by the cage sooner, so closer to the top, will experience less acceleration due to a short time in the electric field. Ions deflected later, towards the bottom of the cage experience more acceleration due to the longer time in the electric field. This explains the asymmetry of the etch for devices closer to the edge of the cage.

The side of the sample being etched closest to the cage wall will experience a higher etch rate than the other side. This is because the ions will have spent more time being accelerated in the electric field compared to the ones from the other side. The ions on the other side will have reached the cage sooner and will not have experienced as much of an acceleration from the electric field. Therefore, they will have less kinetic energy and etch at a slower rate Figure 54. The difference in kinetic energy between the 2 ions is:

$$\Delta K.E = q\ E\ \Delta h \tag{40}$$

Where $\Delta K.E$ is the difference in kinetic energy, q is the charge of the ion, E is the electric field strength and Δh is the difference in the path length the 2 ions have travelled before reaching the cage.

This effect on a small chip will not have as much of an impact on devices due to the difference in path length from the edges of the cage to the sample being similar. However, development is required for this method if it is to be expanded for larger samples, e.g. 8' or 12' wafers, where a larger cage is required so a bigger difference in path length will be experienced.

4.2.5 Photonic Crystal Nanobeam

EBL was used to create a mask consisting of Bragg reflectors [232], [233] with a cavity at the centre of it to create a photonic crystal (PhC) like structure to be undercut Figure 55.

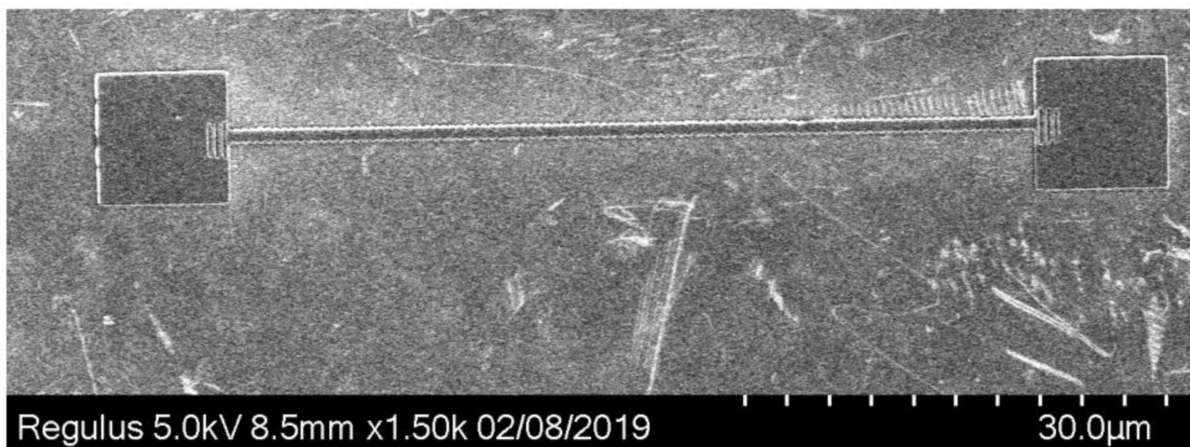


Figure 55 : SEM of the Ni mask of the photonic nanobeam structure comprising of Bragg reflectors either side of a cavity on GaN.

Bragg reflectors with dimensions for λ = 850 nm ((W1, L1) = (170, 300) nm, (W2, L2) = (126, 400) nm) and λ = 1550 nm ((W1, L1) = (246, 800) nm, (W2, L2) = (326, 600) nm) were used for fabrication (designs simulated by Daryl Beggs as seen in Figure 56). Only work on the 1550 nm device has been carried out due to the larger dimensions of both the Bragg reflectors and gratings.

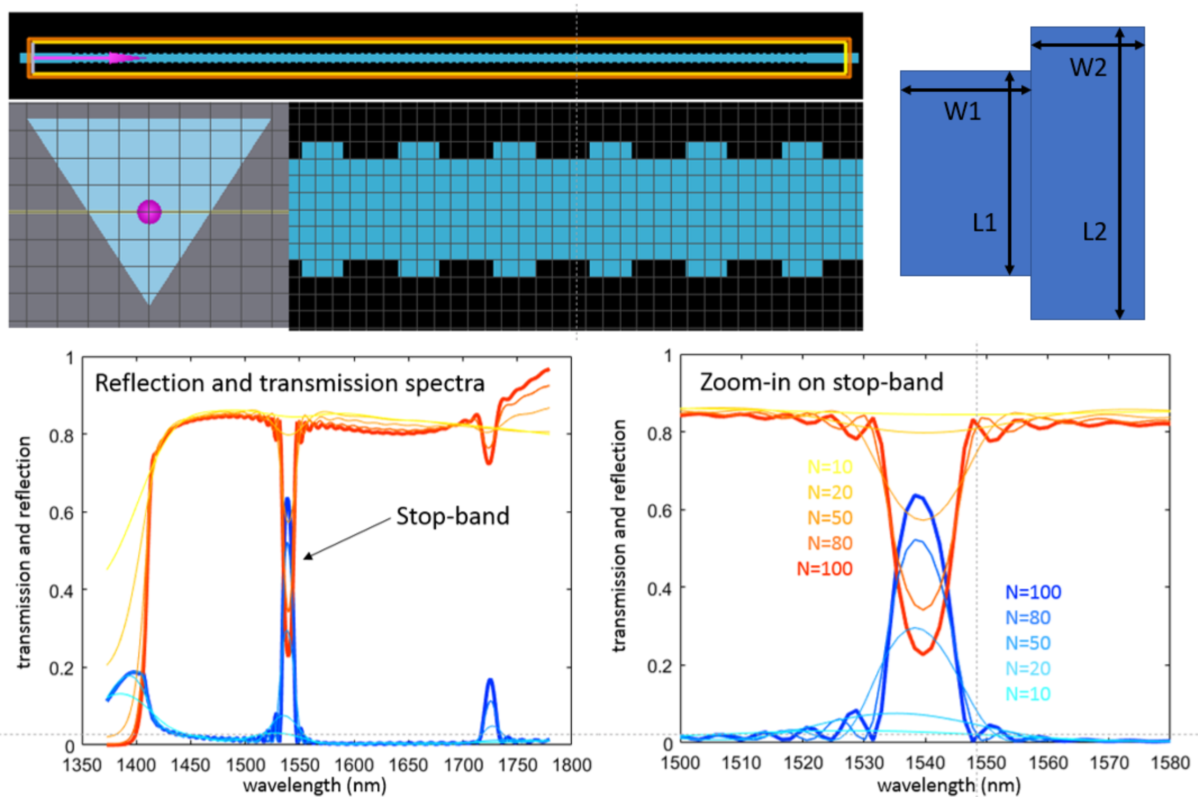


Figure 56 : Simulation of suspended triangular Bragg reflector by Daryl Beggs. Top right: Simulation area of Bragg reflector, Top left: Dimensions of repeated Bragg corrugated pattern (dimensions in text above), Bottom: Graph of reflection and transmission of light at different wavelengths.

Due to the small dimensions of the nanobeam structure, proximity effect correction (PEC) software was used to attempt to dose the mask to avoid any overdosing. A sinusoidal variation in shape would be expected to form if a PEC is not carried out Figure 57 because of the radial dispersion of the electrons, hence why a circular spot is produced during the focus of the e-beam.

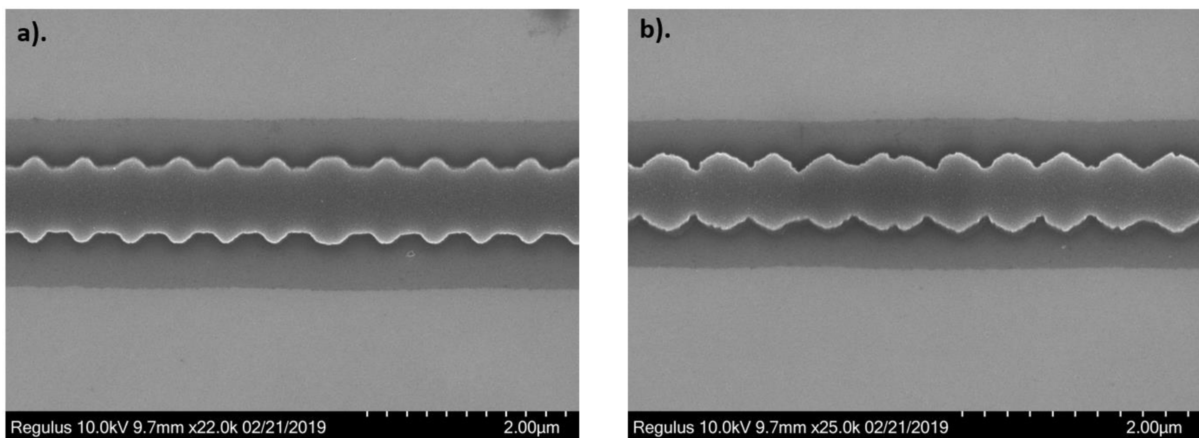


Figure 57 : Bragg reflectors and cavity a). with PEC b). without PEC

The gratings are calculated using:

$$g = \frac{m\lambda}{4n} \qquad 41$$

Where g is the size of gap based on the material used, in this case GaN and air, m is any odd, positive number, λ is the target wavelength and n is the refractive index of the

material at the target wavelength. No in-depth analysis has been carried out to optimise the coupling of light into and out of the nanobeams.

A 10 x 10 µm area either end of the PhC nanobeam was used initially for the gratings to be located and support the beam. There was however an issue with the gratings. It appears that for the $3\lambda/4n$ gratings, $n = 1$, the PEC was not sufficient to prevent the overexposure of the gaps for the gratings and were removed during development. These are 2nd order gratings that scatter light of a certain wavelength dependent on grating period and angle of light into or out of a waveguide such that they are in phase and interfere constructively [234]. To further improve the writing of the gratings, the 10 x 10 µm area was reduced to 2 µm, see Figure 58, either side of the grating coupler area, to reduce proximity effects and reduce the write time.

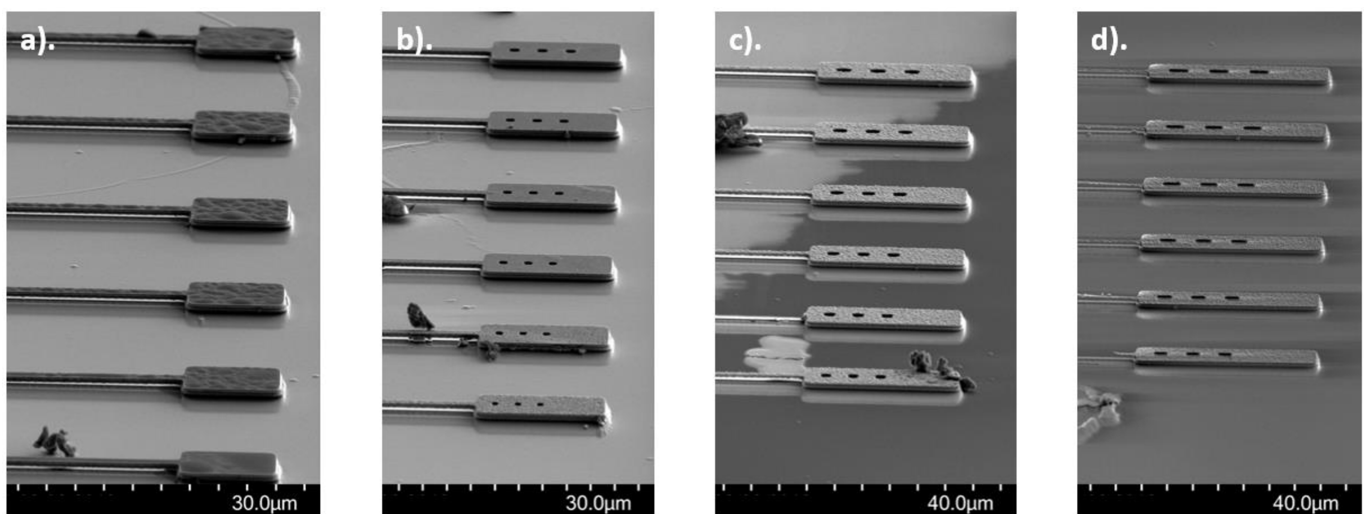


Figure 58 : SEM images of gratings a). $3\lambda/4$ *b).* $5\lambda/4$ *c).* $7\lambda/4$ *d).* $9\lambda/4$. $3\lambda/4$ *gratings have failed to be written due to overexposure causing features to be removed in development.*

The issue of the gratings was resolved with larger values of m however, when placed either side of the PhC beam the original corrugated pattern stopped appearing. Instead, a sinusoidal pattern expected when no PEC has been applied appears. It is unknown why this is, but it could be either the PEC algorithm used needs to be more specific to the current wafer and resist (a 500 nm PMMA on GaAs PEC is used) or some change has occurred with the equipment that is affecting the write.

Initial PhC nanobeams were designed to be 50 µm long to accommodate the range the optical setup can couple light in and out of the gratings. However, it appears that a 50 µm nanobeam cannot be supported on its own as is visible from the cracks at the edges and centre Figure 59.

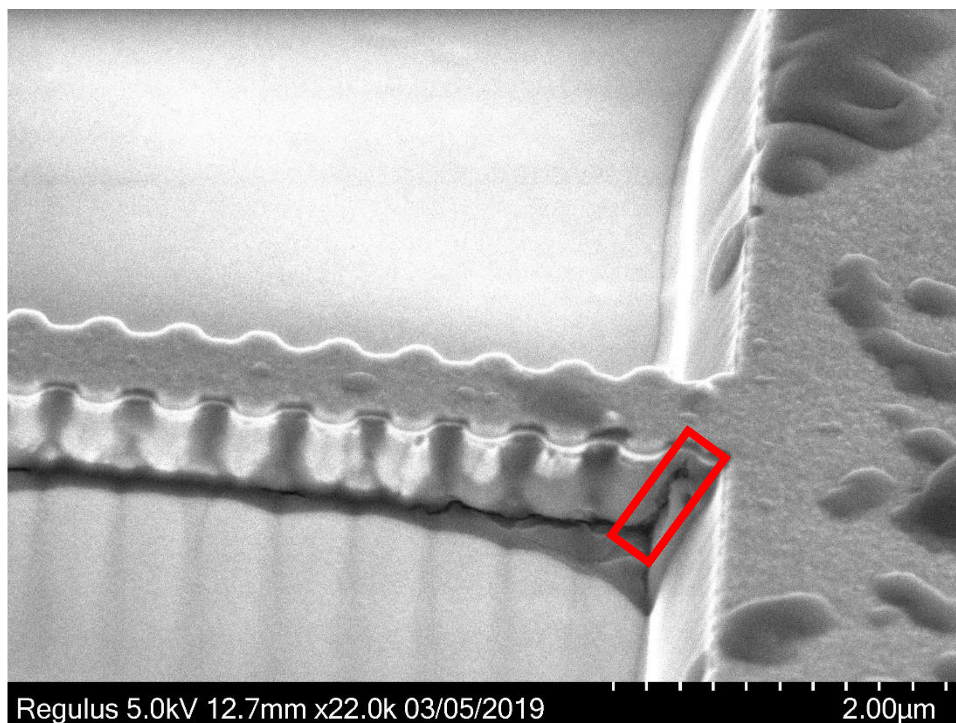


Figure 59 : SEM image of nanobeam cracking (red box) at grating area. Nanobeam length 50 µm.

A smaller length nanobeam of 40 µm was fabricated instead and appears to be able to sustain the weight of the nanobeam. For higher Q factors more repetitions of the Bragg reflector pattern is required, up to propagation loss limits [235]. To increase this, after optimisation of the etch recipe has been performed, supports will have to be included in the design of the nanobeam. It is unclear whether a similar solution that is used for the ring resonators [231] is possible without detriment to the Q factor, but would seem a logical approach to use instead of supports from arms.

4.3 Conclusion

A single step angled cage etch method has been demonstrated for integrated photonics. Doubly and singly clamped cantilevers and PhC nanobeams have been shown to support light transmission with light emitting at the other end. The versatility of this method for etching various shapes has been demonstrated with microrings and disks. Further development of e-beam masks and etch recipe are required to increase Q factors of cavities and reduce propagation losses of the waveguides.

Chapter 5

5 Conclusion and Outlook

With the Quantum 2.0 era beginning, quantum devices are taking a huge leap forward in all areas of modern-day life. The pinnacle of this would be a quantum computer [236]. While there are many different platforms available for a quantum computer [237], [238], photonics shows a promising realisation [239],[240] with fabrication technologies already in place for Si PICs [241]. However, this workhorse of the integrated era has its limitations with a bottleneck in switching, vital for a quantum computer, being one such issue. A fast and low loss switch is not possible with Si as the base material due to a slow thermo-optic effect and free carrier induced losses that are required for the switching mechanism.

Compound semiconductors have shown many properties comparable or greater than those available in Si [95]. They also possess additional properties Si is unable to access, due to its centro-symmetric nature [242]. These materials look to usurp Si as the material of choice for PICs but lack the extensive and well-established infrastructure available to its competitor. This thesis demonstrates the potential for developing an equally expansive fabrication base like Si, with the same technologies used for Si.

Single mode operation waveguides were simulated and used to show the potential a MZI switch made from either GaP or GaN could have, using their inherent Pockels effect that Si lacks. These design specifications became the basis that the fabrication process needed to achieve to create them. While the difficulties of producing these designs are self-evident, there has been good progress made towards achieving this goal with a clear scope for the

future. A novel way of under etching GaN was developed to show the possible adaptations and improvements of current technologies to create PICs in compound semiconductors.

There is a bright future for PICs in compound semiconductors that I hope the work in this thesis will make some contribution towards. While it may have only scratched the surface with some of the fabrication processes, there is a clear direction of where to take this research and how to develop it further.

5.1 Future Work

5.1.1 Simulations

For designs of devices, a DC splitter was used to split the light along two separate paths. This was due to the simulations already carried out for potential switch designs and believed to be a time saving strategy. The fabrication of these DCs however, was the one of main challenges which required a considerable amount of time to develop of the correct e-beam mask dosage and etch. As further adage to this, a different more, powerful machine was used to achieve the actual gap in the e-beam write instead.

MMIs [243] are a much simpler design compared to a DC, with significant simplification in the fabrication of them. Simulations would need to be carried out to determine the dimensions of these MMIs based on a compound semiconductor material system. While a simple MMI design would suffice as a proof of principle demonstration, further optimisation of the MMI can be done to improve the performance of it as a splitter.

Optimisation of the transferal of the waveguide mode from the waveguide to multimode area and back for the MMI would involve simulations of a tapered waveguide to allow a

near adiabatic transfer [244]. Optimisation of the multimode area can also be done to shorten the transfer area as well as reduce losses and improve robustness to defects in the area. Once developed, integrating the MMIs into previous simulations with the DC splitters replaced, would need to be carried out to judge the performance of the device and the footprint size.

Given these considerations a completely different design maybe chosen to be fabricated based on the overall footprint and performance of the simulation, as well as its ease to fabricate. A comparison of the footprint size was used as the defining factor between the designs with similar performances. Striving to improve the performance of these devices or reductions in size through simulation will be an ongoing endeavour. This will ensure that fabrication techniques or technologies are improved to enable these designs to be realised.

Many different components are needed to create an integrated photonic quantum computer, each of which will have to be simulated to gain insight into the dimensions for operation [245], [246]. There will also be a mix of passive and active components that will require different simulations to calculate their performance. While these components will take time to simulate, a more important part of this entire process needs to be built on and perfected to achieve these devices in real life - the fabrication process.

5.1.2 Fabrication

There are still many parts of the fabrication process that need to be expanded upon to create PICs in compound semiconductors. Further development of the etch matrix required to fully detail the different effects of different conditions on the etch is the easiest to achieve in the short term. Variations in bias, ICP, chemical ratios and chemistries to name a

few, will allow a detailed investigation leading to ideal conditions for creating straight smooth sidewalls for waveguides.

Although development of the etch recipe will improve the smoothness of sidewalls for the waveguide, the quality of the mask used to transfer designs can also be investigated. As has been demonstrated, Figure 44, tearing of a Ni mask can cause an issue with the finish of a mask leaving a rough edge that will be transferred into the material during the etch process. Further refinement of the lift off process to achieve a clean finish can be done but other materials for masks may produce more fruitful rewards.

The use of different metals that lift off easier, without splintering or redeposition onto the design would be an easily attainable, short term option [247], [248]. Different materials other than metal, such as spin on glass [249] could be viable options as well as harder or thicker photoresists that would survive the etch process. Development of a photoresist mask leaves a much smoother straight edge due to the development process compared to a lift off process.

While this current work would allow a passive component to be achieved, the creation of an active switching component would need the fabrication of electrodes and contact pads. These would supply the electric field needed to use the Pockels effect available in GaN and GaP for the switching mechanism. The push-pull configuration simulated for the MZI would require electrodes either side of the arms and a central electrode. Connecting the outer electrodes is straightforward but to connect the central electrode is a challenging feat. Either the central electrode is made large enough to wire bond directly to the electrode or a connection will need to run over the top of the waveguide to allow the voltage to flow to the central electrode. There are methods of creating suspended metal wires over

waveguides [250], but consideration of the field generated and its interaction with the waveguide mode will have to be considered.

Further development of the fabrication process is vital to achieve both low loss waveguides and high-performance devices. This is however, limited to the quality of the GaN as standard epitaxial GaN on substrate suitable for PICs still have defectivities that are high in comparison to Si. Less defectivities will limit the performance of devices in GaN, which is why the further improvement and advancement of the angled cage etch is essential.

5.1.3 Angled cage etch

The angled cage etch method of undercutting GaN to create suspended structures is still in its infancy even though a great leap in the structures fabricated has been achieved. Currently the etch is predominantly physical and effectively mills the GaN away like a FIB [251]. This leaves a rough sidewall that will impact the loss of light to the surroundings due to scattering. Refinement of the etch to include a more chemical contribution could help smooth the sidewalls and reduce losses associated with it. Although it has been shown with a red laser that light can travel along these triangular structures already.

Continuation of the e-beam mask to recreate the rectangular corrugated features that were achieved initially, while still fabricating the grating either side is required. This may involve investigations into the various values of variables required in the PEC software to get a better PEC [193]. It would be worth returning to the original design with the 10 x 10 µm grating area, where the PEC software was correctly dosing the PhC nanobeam, to investigate the condition of the tool. If the corrugated pattern returns, then a possible solution to the disappearing corrugation could be to start with the original design, run the

PEC software, remove the larger grating area and replace it with the smaller area with the PEC software run again just on that area. If, however, the PhC nanobeam structure returns and the grating survives at least the area of optimisation is significantly reduced.

Further alterations to the cage itself may result in an improved etch such as; varying the gauge of the spacing between the wire mesh that covers the cage, making the fixings flusher to the cage or making the cage from a different material to name a few [227]. Certainly, experimenting with different shape cages and the degree to which designs can be created, would make for interesting and unique devices to be created. As discussed in the main Angled Cage Etch chapter, developing the ring resonator designs to enable some suspension of the ring would allow a ring resonator cavity to be created and characterised for implications in switching or source generation.

5.1.4 Optical characterisation

The devices created so far are yet to have any optical characterisation. Losses associated to sidewall roughness would be a crucial value to find for monitoring the development of the flow process and improvement in the loss. With regards to the PICs, it is essential to have an optical setup available to test device structures and their performance. In the case of the switch, the fabrication tolerance of the splitter can be determined to ensure a 50:50 split of light occurs in passive operation or very close to that division. While an electric field can be applied to ensure the light exits through one path or another, ideally the system would be in either the bar or cross state completely without requirement of the electric field and only requiring it to switch paths. Realistically this is unlikely to happen, and some corrective field

would be required, but to ensure this is at as low a voltage as possible to make the switch more efficient is important.

The angled cage etch has many potentials with the suspended structures being used for PICs and sources. Similarly, for PICs, determining losses and improvement in losses would be vital to justify the usefulness of this method to create suspended structures. For the PhC nanobeam, measuring the Q factor of the cavity at the centre can be used to calculate the photon pair production via SFWM which can be used a heralded single photon source [252], but can also be used to gain a value for the nonlinear coefficient of the GaN. The efficiency of the gratings would also be of interest given the angular nature of the gaps. Whether this would hinder, which is more likely, or improve the coupling efficiency of the grating would be found.

The optical characterisation of any of the components or devices created, be it using angled cage etch or standard processes, is of utmost importance for any furtherment of the fabrication process. Without this crucial data, only by visual inspection can processes be seen to be improving and as they improve differences in appearance will be difficult to determine. Only through optical measurements is it likely a difference will be noticeable.

5.2 End statement

The future of photonics in quantum technologies is a certainty in one form or another. Whether crucial devices such as quantum computers will be based off this platform is unknown. If they are, while Si will be satisfactory initially, its short comings will inevitably become more prominent over time. It is important, in that case, to begin the fabrication of

compound semiconductor PICs to overcome issues with Si or surpass it completely. The beginning of this process is evident in this thesis and while it may be at the early stages of development, the direction for further improvement is clear with plenty of opportunities in the future. I hope my contribution will have some bearing on future technologies or techniques for fabrication in compound semiconductors or at least inspire others to do so.

Appendix

Fabrication Details

Solvent Wash/Recleans

solvent wash consisting of acetone, methanol and IPA heated to 80°C is used. The samples soak in the solvents respectively for 5 mins with an IPA rinse to finish the clean. After inspection under a microscope, a cotton bud soaked in IPA can be used to wipe away any marks left on the sample.

For samples with photoresist, a similar procedure is done but an initial acetone soak, followed by NMP (Remover 1165) soak at 80°C for 5 mins is done. Additionally, an asher can be used to clean the sample using an oxygen plasma. For most marks, including photoresists, a 5 mins Ash at 50 W is sufficient.

PMMA, an e-beam resist, overdosed appears to harden, making the previous cleaning process insufficient to remove it. A more vigorous Ash of 30 mins at 100 W will remove most residues and leave the sample clean. The samples are then ready for processing.

Resists

(a) *Photoresist*

For the initial development of the etch recipe 2 µm lines with a 50 µm pitch were used. A bilayer photoresist of SF11, spun for 20 s at 4000 rpm, baked at 97°C for 10 mins, followed by S1813, spun for 45 s at 6000 rpm, baked at 80°C for 5 mins.

(b) E-beam resist

950 PMMA A4 is spun at 6000 rpm for 45 s and baked at 180°C for 3 mins. A bilayer layer resist can be used to improve the lift off of the Ni mask consisting of an MMA EL11 layer spun at 4000 rpm for 45 s and then baked at 180°C for 3 mins followed by the 950 PMMA A4 layer spun at 4000 rpm for 45 s baked at 180°C for 3 mins. These are positive resists like the photoresists previously.

Angled Cage Etch of GaN

Calculation of ϕ

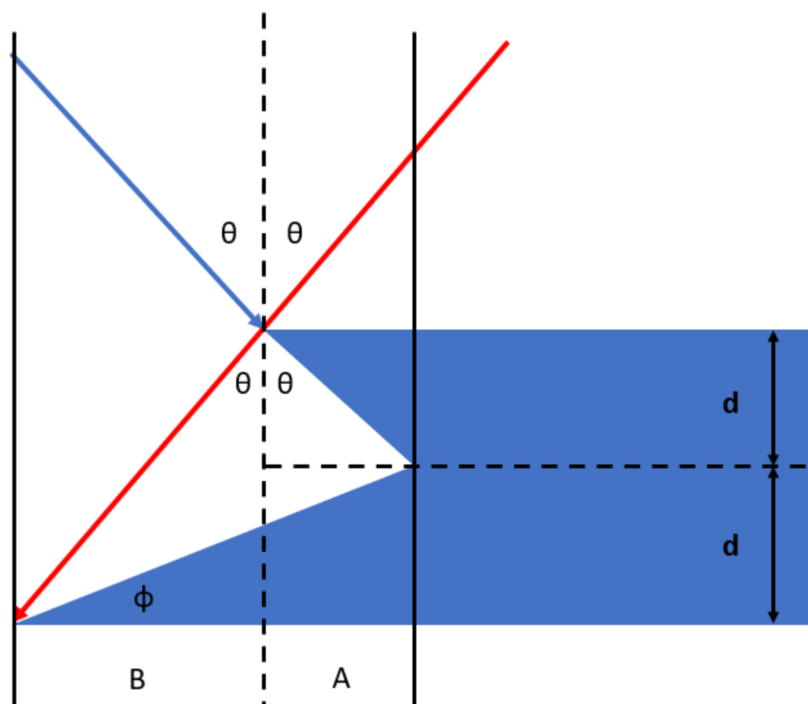


Figure 60 : Diagram of ion etching and trajectories.

Total etch depth = 2d

Etch depth from left (blue) ion = d

Etch depth from right (red) ion = d

From trigonometry we get:

$$\frac{A}{d} = \tan\theta$$

$$\frac{B}{2d} = \tan\theta$$

So:

$$A + B = 3d\tan\theta$$

From Figure 60 : Diagram of ion etching and trajectories. :

$$\tan\varphi = \frac{d}{(a+b)}$$

Therefore:

$$\varphi = tan^{-1}((3\tan\theta)^{-1})$$

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