Full Analytical Topology-Device Selection and Multi-objective Optimization of a 27 kVA Aircraft Inverter

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***Abstract*—This paper demonstrates a topology-device selection and multi-objective optimization tool for a 350 V dc, 27 kVA aircraft inverter system. The design space is generated with the topology-device combination as the primary variable and the switching frequency as the secondary variable, which considers two-level vs. three-level topologies and Silicon (Si) vs. Silicon Carbide (SiC) devices. The proposed optimization tool conducts automated design of each component and estimation of their performances regarding power loss and volume/weight through a holistic approach, which bases on full analytical models that have been derived in literature and those with latest development. The proposed tool can rapidly and accurately show the multi-objective design trade-offs and inform the optimal design choices.**

Keywords—optimization, analytical, Silicon Carbide devices, three-level converter, aircraft

I. INTRODUCTION

High efficiency and high power density are the two core targets for the design of next-generation power electronics converters, driven by the demand from advanced electrified transportation applications, e.g. electric vehicles and more electric aircraft. To achieve a high power density of the power electronics systems, the key aspect is to effectively reduce the passive components, such as heatsinks and filter components, which account for a major portion of the volume, weight and cost [1]–[5]. For example, the filter components occupy 40% of the total volume and weight of the converter system in [6]. [7] reported that the passive components contribute over 80 % weight of a converter. As for the efficiency, moving from 96% to 99% efficiency would significantly reduce the heatsink size and would allow a transformative change from liquid cooling to air cooling. However, to achieve the system-level optimal, several conflicting design constraints need to be considered together. For example, a lower switching frequency may lead to improved efficiency as a result of lower switching loss, but it comes with the cost of larger filter components. Increasing the switching frequency results in the reduced size of the filters, but the associated additional switching losses will require bigger heatsinks to extract the heat.

Therefore, the system-level optimization of a power converter calls for an automated design tool to evaluate the options of a wide design space and visualize the multi-objective design trade-offs. For example [8] presented such a tool to maximize the power density of two-level ac/dc converters, which evaluates several design variables and pools of available components. Apart from varying the design variables (e.g. switching frequency), there are two fundamental areas that drive improvement of the power density of power converters and reduction of passive components size: advanced converter topologies, such as three-level converters, and emerging power semiconductor devices, such as Silicon Carbide (SiC) devices, as pointed out in [9]. For a specific application context, it is important to quantitatively evaluate how much performance gain can be achieved through these two aspects.

The contribution of this paper is to demonstrate a topology-device selection and multi-objective optimization tool for a 350 V dc, 27 kVA aircraft inverter that considers a design space evaluating four device-topology combinations, i.e. Si vs. SiC devices and two-level (2L) vs. three-level (3L) topologies. The tool is fully based on analytical models to avoid real-time simulations and minimize the computation load. Compared with existing studies, this work uniquely incorporates the latest analytical models that recently became available, such as the device loss model under the special modulation scheme in three-level converters [10] and the accurate core loss modelling of the filter inductors [11] that are neglected in [8], [12], which factors in more unneglectable elements to improve the accuracy and meaningfulness of the estimation. These latest research advances enable such a full analytical tool to rapidly and accurately evaluate the design space to inform the optimal design choices.

II. SYSTEM SPECIFICATIONS AND DESIGN SPACE

A. Top-level considerations of the design space

This work targets a 27 kVA aircraft Pulse Width Modulated (PWM) inverter that operates with a nominal 350 volts dc-link. The design of the power converter primarily starts from the selection of the topology and the power devices, which are the two fundamental directions to improve the power converter performance. The considered power devices are the last-generation Silicon IGBTs and the emerging SiC MOSFETs. The candidates of topology are the conventional two-level converter (shown in Fig. 1(a)) and the advanced three-level T-type (3LT) neutral-point-clamped (NPC) converter (shown in Fig. 1(b)).

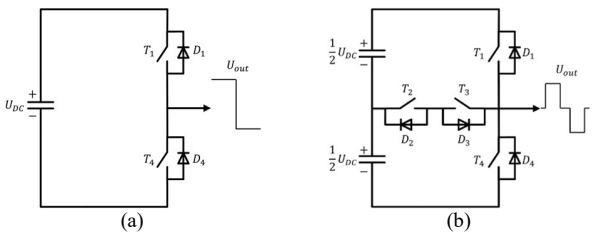

Fig. 1. Considered inverter topologies (a) two-level (b) three-level T-type

As shown in Fig. 2, this scope leads to four topology-device combinations to be evaluated, which are considered as the primary design variables.

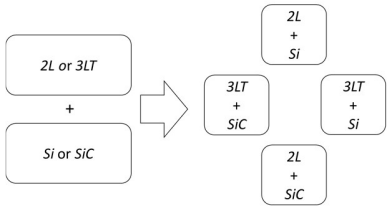

Fig. 2. Considered topology-device combinations

The secondary design variable is the switching frequency f_{sw}. Considering the 400 Hz fundamental frequency and the typical switching frequency of the power devices, the range of f_{sw} is defined in between 10 kHz to 100 kHz.

B. Multi-objective optimization

The optimization tool is developed based on analytical models to perform two tasks on each possible design in the design space: (1) automated design process of the passive components (2) estimation of the converter performance metrics. In the performance domain, there are two branches of models: the volume/weight models and the loss models, which correspond to the two objectives: power density and efficiency. From a top-level, the considered components and the structure of this work are shown in Fig. 3.

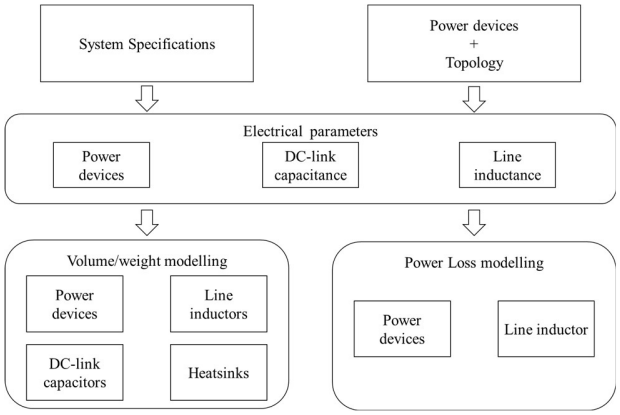

Fig. 3. The top-level structure of the optimisation tool

III. Analytical Power Loss Models

A. Analytical power loss models of power devices

The power losses of power devices consist of two mechanisms: conduction loss and switching loss. The conduction loss is modelled by the *U-I* characteristic of a power device. For simplicity, the *U-I* characteristic of an IGBT/MOSFET/diode can be approximated by a uniformed expression as

$$u_{FW}(t) = U_{FW0} + R_{on} \cdot i(t) \tag{1}$$

Where u_{FW} is the instantaneous device forward voltage drop; U_{FW0} is the initial device forward voltage drop; R_{on} is the device on-state resistance; *i(t)* is the instantaneous device current. Over one fundamental cycle, one power device does not constantly conduct the current. The conduction loss of a power device can be expressed and averaged as

$$P_{cond} = \frac{1}{2\pi} \cdot \int_0^{2\pi} g_{cond}(\omega t) \cdot u_{FW}(\omega t) \cdot |i(\omega t)| d\omega t \tag{2}$$

Where $g_{cond}(\omega t)$ is the conduction function, which is a piecewise function indicating the conduction intervals of a power device in one fundamental cycle.

The switching loss is a function of switching voltage U_{sw} and switching current I_{sw}. The switching energies with reference to various switching current I_{sw} can be found from the manufacturer datasheet, which can be curve-fitted with a cubic function as in (3) with coefficients *A*, *B* and *C*. The effect of U_{sw} is considered linear regarding the base voltage U_{base} [13], which is the testing voltage of the switching energy.

$$E_{sw} = \frac{U_{sw}}{U_{base}} (A + B \cdot I_{sw} + C \cdot I_{sw}^2) \tag{3}$$

From the fundamental cycle point of view, the averaged energy of each switching transition can be expressed as

$$E_{sw\_avg} = \frac{1}{2\pi} \cdot \int_0^{2\pi} g_{sw}(\omega t) \cdot E_{sw}\big(i(\omega t)\big) d\omega t \tag{4}$$

Considering one power device does not constantly switch in each switching window, a piecewise function $g_{sw}(\omega t)$ is introduced to indicate the switch intervals of a power device over a fundamental cycle. The total converter loss equals the sum of conduction losses and switching losses on all power devices.

$$P_{loss\_tot} = \sum (P_{cond} + f_{sw} \cdot E_{sw\_avg}) \tag{5}$$

Following the above uniformed expressions, the coefficients of the selected power devices are extracted from manufacturer datasheets and listed in Table I.

As required in formulas (2) and (4), the piecewise function indicating the conduction/switching intervals of each power device over one fundamental cycle need to be found. The functions g_{cond} and g_{sw} depend on the topology, the converter operating point, the conduction pattern of power devices, and the modulation scheme. When the synchronous conduction is enabled in MOSFETs, the device conduction/switching intervals are different to the case with IGBTs. Note when a special modulation scheme is applied (e.g. for voltage balancing purposes), the devices' conduction/switching intervals can also change as demonstrated in [10] for three-level converters applying the Virtual Zero-level Modulation (VZM), which can increase the switching loss by ≈ 40% in the worst case.

B. Copper loss of filter inductors

Apart from the power devices, the magnetic components can also contribute significant high-frequency PWM losses in a typical power converter [14], which consists of copper loss and

TABLE I. SELECTED POWER MODULES AND EXTRACTED PARAMETERS FROM THE DATASHEET

		U_{FW0}	R_{on}	E_{tot} [J] vs. I [A] $E_{tot} = E_{on} + E_{off}$ for IGBT/MOSFET, $E_{tot} = E_{rr}$ for diode			
		V	mΩ	A	B	C	U_{base} [V]
CAS300M12BM2 U_{GS} = -5/+20 V $R_{Gon} = R_{Goff}$ = 2.5Ω	T1/T4	0	7.5	1.54e-3	2.11e-5	4.431e-8	600
	D1/D4	0.72	4.9	0	0	0	600
SKiM301TMLI12E4B U_{GE} = -15/+15 V $R_{Gon} = R_{Goff}$ = 2.7Ω	T1/T4	0.78	4.6	6.27e-3	5.91e-5	2.13e-8	300
	D1/D4	0.86	5.8	2.21e-3	-1.72e-6	-2.99e-10	300
	T2/T3	0.75	3.7	8.46e-3	2.04e-5	6.12e-8	300
	D2/D3	0.7	3.4	2.27e-3	-2.14e-6	2.70e-10	300

core loss. The copper loss is relatively straightforward to estimate analytically relying on the Fourier superposition method, which is to add up the losses of each harmonic that is individually calculated [14] as

$$P_w = R_{wdc} I_0^2 + R_{wdc} \sum_{n=1}^{\infty} F_{Rn} I_n^2 \tag{6}$$

The dc resistance of the winding R_{wdc} can be found as ([14])

$$R_{DC} = \frac{\rho_{cu} l_w}{A_{cu}} \tag{7}$$

Considering both the skin effect and proximity effect [14], the ac-to-dc resistance ratio F_{R} of the winding selected at a particular frequency can be calculated analytically. For example, the F_{R} of rectangular windings can be expressed as ([14], [15])

$$F_R = \frac{R_{AC}}{R_{DC}} = \frac{h}{\delta}\eta \left[\frac{\sinh\left(2\frac{h}{\delta}\right) + \sin\left(2\frac{h}{\delta}\right)}{\cosh\left(2\frac{h}{\delta}\right) - \cos\left(2\frac{h}{\delta}\right)} + \frac{2}{3}(N_l^2 - 1) \cdot \frac{\sinh\left(\frac{h}{\delta}\right) - \sin\left(\frac{h}{\delta}\right)}{\cosh\left(\frac{h}{\delta}\right) + \cos\left(\frac{h}{\delta}\right)} \right] \tag{8}$$

Where h is the thickness of the conductor; δ is the skin depth; η is the porosity factor; N_l is the layer numbers.

In order to calculate the copper loss through (6), the current harmonic contents need to be analytically predicted. In PWM converters, the current harmonic content can be predicted from the converter output voltage harmonics [16], [17] and the line inductance. For a two-level converter with naturally sampled PWM, the amplitude of the voltage harmonic at a frequency f_{h}= $m \cdot f_{\text{sw}} + n \cdot f_0$ is expressed as (see [16])

$$\widehat{U}_{an(f_h)} = \frac{2U_{DC}}{m\pi} J_n\left(m\frac{\pi}{2}M\right) \sin\left((m+n)\frac{\pi}{2}\right) \tag{9}$$

Where U_{DC} is the total DC-link voltage; n is the multiplication index of fundamental frequency f_0; m is the multiplication index of the switching frequency f_{sw}; J_{n} is the Bessel function of order n. The combination of m and n represents the high-frequency harmonics content at multiples of the switching frequency and the sidebands. Similar expressions can be found for three-level converters as well in [16].

C. Core loss of filter inductors

The estimation of core loss is more challenging in PWM converters due to its nonlinear nature, which means the FFT superposition principle does not apply. The latest research suggests that the most practical way to accurately estimate core loss is to rely on empirical loss data measured from rectangular voltages [18], which emulates the waveform seen by an inductor in a converter. The basic segment of the core loss data in this manner is shown in Fig. 4.

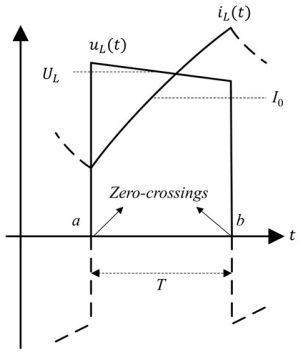

Fig. 4. A pulse segment for core loss calculation

The core loss can be then worked out based on the Composite Waveform Hypothesis to decompose a given PWM waveform into segments in the manner of Fig. 4 and look up the core loss from the empirical database for each segment. The total core loss of a fundamental cycle can then be found by adding up the loss of each segment. [11] presents analytical models to rapidly generate the "operating space" of the inductor, which is equivalently a series of virtual segments over a fundamental cycle derived iteratively by analytical expressions for a given converter operating point. Although this analytical approach is easy to use, the relied empirical core loss database (a user-friendly loss map [18]) measured from rectangular voltage is not commonly available from the manufacturers. But the authors believe that with the advances of standardized inductors, such datasheets would become common in the future.

IV. Analytical Parameter Design of Passive Components

A. Line inductance

The design of the line inductance is determined by the requirement of the current ripple defined as the maximum allowed peak-to-peak current ripple $\Delta I_{\text{pp-max}}$ in one switching cycle. The constraint regarding $\Delta I_{\text{pp-max}}$ is specified by a percentage k_{cr} of peak load current I_{m} as

$$\Delta I_{pp-max} = k_{cr} \cdot I_m \tag{10}$$

The worst-case amplitude of the current ripple in a three-phase voltage source converter can be approximated by the following formulas for two-level [19], [20] and three-level converters [21].

$$\Delta I_{pp-\max-2level} \approx \frac{U_{DC} T_{sw}}{6L} \; (2-level\ converter) \tag{11}$$

$$\Delta I_{pp-\max-3level} \approx \frac{U_{DC} T_{sw}}{12L} \; (3-level\ converter) \tag{12}$$

It can be seen that the required inductance in a three-level converter is approximately half of the value in a two-level converter.

B. DC-link capacitance

The DC-link capacitance is designed against the allowable maximum amplitude of high-frequency voltage ripple as (13), in which k_{vr} is the DC-link voltage ripple tolerance factor.

$$\Delta U_{DC} \leq k_{vr} \cdot U_{DC} \tag{13}$$

Modelling of the ripple components ΔU_{DC} determines the design of the DC-link capacitors. As the foundation of this topic, [22], [23] presents an analytical model to predict the amplitude of ΔU_{DC} in a three-phase VSC over various operating points. To quantify the high-frequency voltage ripple, the peak-to-peak amplitude of ΔU_{DC} is normalized over a base value as

$$\Delta U_{DCN} = k_{DC\_norm} \cdot \Delta U_{DCN} = k_{DC\_norm} \cdot I_{rms}/(C_{DC} f_{sw}) \tag{14}$$

Where C_{DC} is the total DC-link capacitance; I_{rms} is the load RMS phase current; $k_{\text{DC\_norm}}$ is the normalized high-frequency voltage ripple. According to [22], ΔU_{DC} is a function of modulation index M and power factor $cos\ \varphi$. The mathematical expression of $k_{\text{DC\_norm}}$ is expressed as.

$$k_{DC_{norm}} = \frac{M}{16}\left[\left(6 - \frac{96\sqrt{3}}{5\pi}M + \frac{9}{2}M^2\right)cos^2\varphi + \frac{8\sqrt{3}}{5\pi}M\right]^{0.5} \tag{15}$$

It can be seen that the amplitude of the ripple component reaches the worst-case when $M = 1.15$ and $cos\ \varphi = 0$, where $k_{\text{DC\_norm\_max}} \approx 0.0724$. Therefore, the required DC-link capacitance considering the worst case is found by

$$C_{DC} = k_{DC\_norm\_max} \cdot \frac{I_{rms}}{k_{vr} \cdot U_{DC} \cdot f_{sw}} \tag{16}$$

C. Heatsinks

The design of the heatsink is determined by the required heatsink-to-ambient thermal resistance R_{th_sa} in the worst case, which can be found by satisfying the junction temperature T_j constraint for each power device in a thermal resistance network as detailed in [8]. Fig. 5 shows the required R_{th_sa} for the evaluated case, in which the switching loss reduction of SiC devices is reflected as larger values of R_{th_sa} (smaller heatsink), especially at a higher f_{sw}.

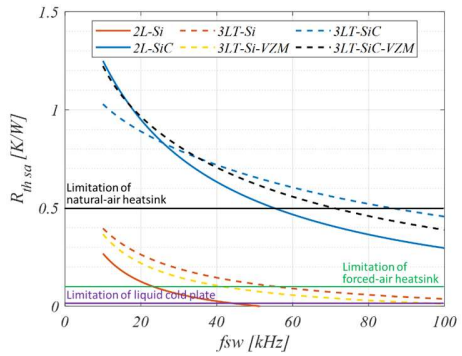

Fig. 5. Required thermal resistance with T_a = 40 °C, T_{j_max} = 125 °C

V. Analytical Volume/Weight Scaling of Passive Components

Once the parameter design is completed, the next step is to conduct the design or scaling of the components to find the volume/weight estimations of physical components. Depending on the purpose, the components can either be designed through an analytical procedure, or picked out from a pool of off-the-shelf products, or modelled with simplified scaling laws.

A. Filter inductor

The design of an inductor is commonly based on the Area Product (A_p) Method [14], [24], which is expressed as

$$A_p = W_a A_c = \frac{LI_{max} I_{rms}}{K_u J_m B_{pk}} \tag{17}$$

Where A_c is the cross-sectional area of the core; W_a is the core window area; K_u is the window utilization factor (copper filling factor); J_{max} is the maximum current density; B_{max} is the maximum flux density. The design/selection of the magnetic cores (material, shape etc.) must satisfy the required A_p, which can lead to selecting a commercial core or customizing a core. Then the design procedure is followed by designing the winding and airgap as in [24]. The specifications of the designed inductor can be fed into the loss modelling presented in the last section.

For a top-level estimation, the volume/weight of the inductor can also be scaled steplessly as a function of the stored energy [14] or the Area Product [2], [25].

B. Capacitor

The design of dc-link capacitors is relatively simple, which can be directly selected from commercial products. For a stepless scaling, this work extracts the scaling models from the commercial film capacitors *B3267X and B3277X series* with 450 V rated voltage from *EPCOS* as

$$V_{cap}\ (m\ell) = 8.054 + 0.8864 \cdot C(\mu F) \tag{18}$$

If two identical capacitors are placed in series to form the dc-link capacitance, e.g. in the 3L configuration shown in Fig. 1, the capacitance of each capacitor needs to be doubled to achieve the same DC-link capacitance as

$$C_1 = C_2 = 2C_{DC} \tag{19}$$

To distinguish these two configurations, they are labelled as 1cap (single dc-link capacitor) and 2caps (two capacitors in series) in this work.

C. Heatsink

Considering off-the-shelf products, the heatsink can be picked out from the manufacturer datasheet (e.g. [26]) based on the required R_{th_sa} value as presented in [8]. For simplified theoretical scaling, the size of air-cooled heatsinks can be estimated through the Cooling System Performance Index (CSPI) [30]. For example, the CSPI of an optimized air-cooled aluminum heatsink with fans can reach 17.7 W/K·L.

VI. System-Level Optimization

The structure and data flow of the full analytical optimization tool is illustrated in Fig. 11. A design space is generated from the four topology-device combinations and a range of switching frequency, through the *ndgrid()* function in Matlab. The performances of each component are estimated, gathered and visualized to show the quantified trade-offs and performance comparisons at the end. For simplicity, the ripple requirement k_{vr} and k_{cr} are defined as 1% and 20%, respectively.

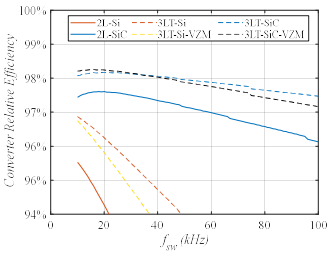

Fig. 6. Converter overall efficiency considering power device and line inductor losses

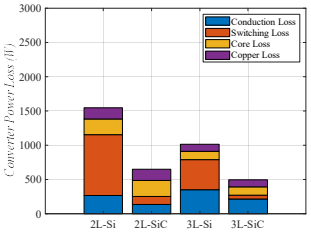

Fig. 7. Power loss breakdown of four power device-topology combinations f_{sw} = 20 kHz

Fig. 6 and Fig. 7 plot the efficiency curve and power loss breakdown of various design options. For Si options, device losses are the main contributor (>70 %) to the total loss. For SiC options, the switching loss is significantly lower so that a >96% efficiency can be maintained up to 100 kHz, and subsequently, the magnetic component loss becomes equally significant as the switching devices in this case.

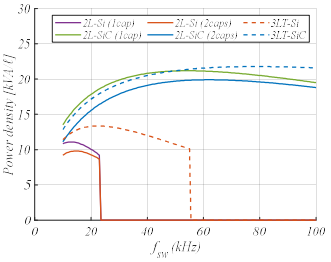

Fig. 8. Volumetric power density with forced-air cooling

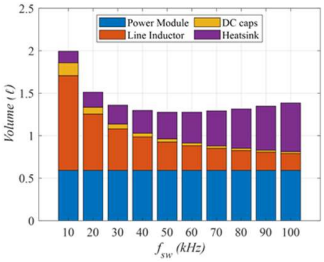

Fig. 9. Volume breakdown of the 2L-SiC case

Fig. 8 and Fig. 9 show the power density prediction and the volume breakdown of the evaluated options. The 2L-Si based configurations show a steep drop of power density after 20 kHz due to the substantial switching loss that leads to no heatsink that can satisfy the predefined temperature rise. In this case, the size of the heatsink is considered infinite, and the power density drops to nearly zero. As the last-generation option, the maximum achievable power density of *2L-Si* is at 15 kHz at around 10

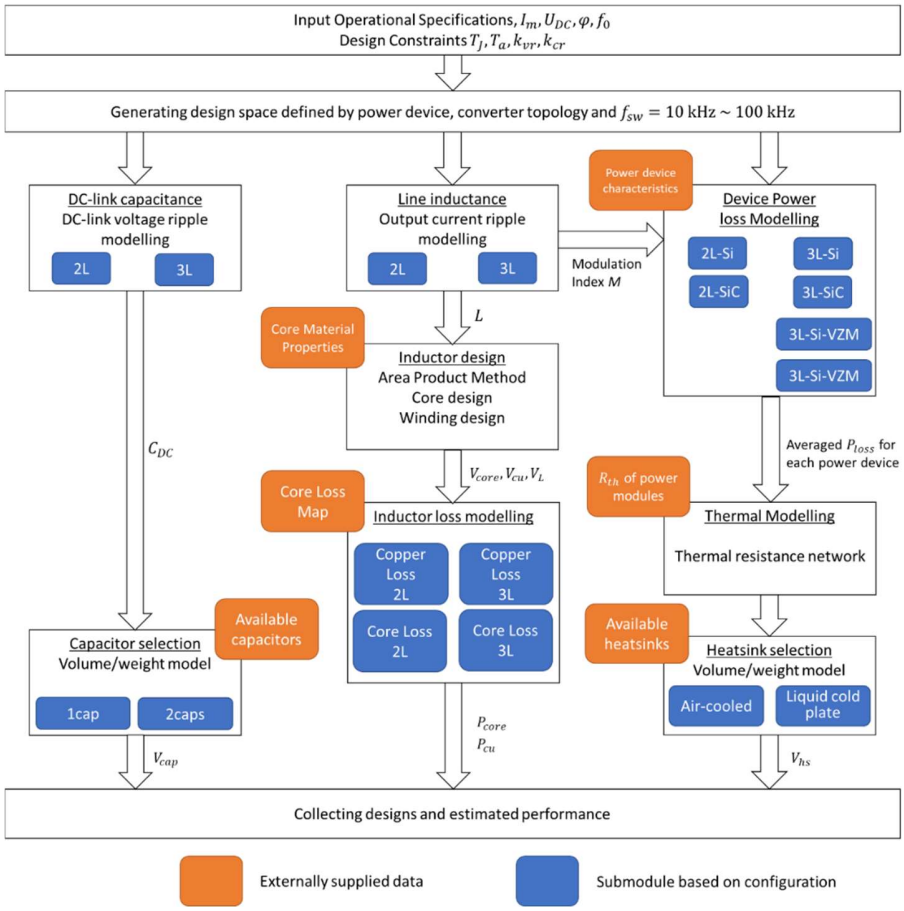

Fig. 11. Visualized data flow and structure of the optimization tool

Table II. Summary of applied analytical models

	Note	*Ref.*
Power loss modelling		
Power Device	2L-Si	[13]
	2L-SiC	[8]
	3L-Si	[29]
	3L-SiC	[10]
	3L-Si-VZM	[10]
	3L-SiC-VZM	[10]
Inductor Copper Loss	R_{wdc}, F_R	[3]
	PWM harmonics	[16]
Inductor core loss	2L	[11]
	3L	[11]
Parameter design		
Line inductance	2L	[21] [22]
	3L	[21]
DC-link capacitance	2L	[22]
	3L	[30]
Heatsink	R_{th} network	[31]
Volume/weight of physical components		
Line Inductor	Customized design	[14]
	Simplified scaling	[14] [2] [25]
DC-link Capacitor	Datasheet based design	[8]
	Simplified scaling	[28]
Heatsink	Datasheet based design	[8]
	Simplified scaling	[28]

kVA/L. The new-generation solutions, 2L-SiC and 3LT-SiC, can both reach around 20 kVA/L. To evaluate two objectives at the same time, Pareto Front analysis [27] is performed to visualize the performance limits considering both the efficiency and power density as shown in Fig. 11.

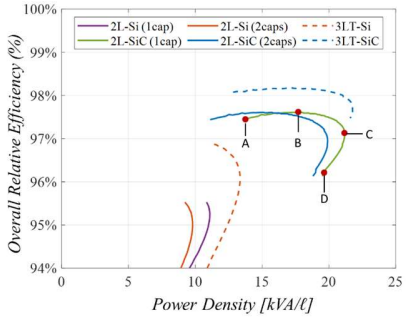

Fig. 10. Pareto Front analysis with forced air cooling

In Fig. 10, the 2L-SiC (1cap) configuration is set as an example. From point A to C, the power density increases as the switching frequency rises. This is because the volumes of the filter components are the major contributors in this region, while a higher switching frequency leads to smaller filter components. It is noticeable that from point A to B, both the power density and the efficiency are improving. In this part, the switching loss rises while the inductor loss drops. From point B, the increase in switching loss becomes dominant, and subsequently the efficiency shows a constant downward trend thereafter. The point C is where the theoretical maximum power density can be achieved. From point C to D, the power density starts to descend, because the heatsink volume starts to be the major contributor, since the heatsink size increases as a result of the increase of switching loss. In this region, the efficiency and the power density both degenerate as the switching frequency rises. Therefore, an optimal design should be selected between point A to C, which benefits both the efficiency and the power density.

In the evaluated case, upgrading the power device from Si to SiC alone can already significantly boost the power density to the theoretical limit of around 20 kVA/*l*. The 3L-SiC solution brings more benefit in the efficiency domain when the f_{sw} is higher, but it cannot significantly extend the power density limit of the 2L-SiC case. Additionally, there are no commercial power module available for the three-level configuration with full SiC devices up to the date of this work. Therefore, this study indicates that the optimal design is the 2L-SiC solution with a switching frequency of around 40 kHz.

The sources of the applied analytical models in this work are listed in Table II. More details can be found in [28].

VII. Features and Limitations

The features and limitations of the presented optimization tool can be summarized as follows. Firstly, the required computation load of the presented tool is relatively light, thanks to the full analytical models for both the automated design of the passive components and the performance estimation models. In contrast to existing approaches heavily relying on iterative algorithms or real-time simulations or finite-element models, the

computation effort of the presented approach is minimized, since the main effort is made externally in deriving the expressions.

Secondly, the presented tool is versatile and has strong expandability. The inputs of the tool are system specifications and constraints in the form of values, which can be easily adapted for various applications. Although the presented tool only evaluated two power devices and two topologies, it is relatively straightforward to plug in more device candidates by inputting the parameters of new devices in the format of Table I. If the operation models are pre-derived, such as the current ripple and switching/conduction intervals, any new topology can also be added into the model for evaluation.

Thirdly, if more practical estimation/design is required, the presented tool can be flexibly configured to select specific components out from a pool of commercial products, rather than applying the approximated and stepless scaling models. For example, the capacitor volume model (18) can be replaced by a automated selection module associated with a pool of available off-the-shelf products.

The limitation of the presented tool is due to its dependency on analytical models. One limitation is that part of the models and manufacturer datasheets can be unavailable for certain topologies or components, while each submodule (blue) and each database block (orange) in Fig. 11 need to be individually derived/collected and programmed beforehand. For example, the analytical model of the inductor operating space has only become available in 2021 [11], while the core loss modelling needed to rely on simulation/experiment waveforms. The empirical core loss data measured from rectangular voltage is also not commonly available. The mature analytical models used in this work were developed in the literature over a time span of 20 years. For new converter topologies, it requires significant research efforts to derive all the models accordingly.

The other limitation is the inherent constraint of analytical models due to simplification. For example, most of the models are valid for steady-state operation only, which typically ignores the dynamic temperature effects and the unordinary operations (e.g. unbalanced load, deadtime effect).

VIII. Conclusion

This work demonstrates a system-level optimization tool fully based on analytical models which conducts automated design and predicts the performance for a 350 Vdc, 27 kVA aircraft inverter considering various topology-device combinations. This analytical tool incorporates the up-to-date models that factor in more aspects of the passive components, e.g. the inductor core loss, than existing approaches and therefore can more accurately identify the trade-offs to inform the optimal design choice. The applied analytical models are well-established and verified in the literature. The presented framework of the tool can be straightforwardly adapted to various application contexts and expanded to include more candidates of power devices, topologies and passive components. Informed by the optimization tool, a real prototype is being built, with experimental verifications to be carried out in the future.

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