Chapter

Practical Approach to Induce Analog Switching Behavior in Memristive Devices: Digital-to-Analog Transformation

Firman Mangasa Simanjuntak, Sridhar Chandrasekaran, Debashis Panda, Aftab Saleem and Themis Prodromakis

Abstract

The capability of memristor devices to perform weight changes upon electrical pulses mimics the analogous firing mechanism in biological synapses. This capability delivers the potential for neuromorphic computing and pushes renewed interests in fabricating memristor with analog characteristics. Nevertheless, memristors could often exhibit digital switching, either during the set, reset, or both processes that degenerate their synaptic capability, and nanodevice engineers struggle to redesign the device to achieved analog switching. This chapter overviews some important techniques to transform the switching characteristics from digital to analog in valence change and electrochemical metallization types memristors. We cover physical dynamics involving interfacial diffusion, interfacial layer, barrier layer, deposition, and electrode engineering that can induce digital-to-analog switching transformation in memristor devices.

Keywords: digital, analog, switching transformation, switching mode, resistive memory, synaptic plasticity

1. Introduction

Memristive devices offer a great promise not only for ultra-high density data storage [1] but also for in-memory computing applications [2]. In-memory computing utilizes the synaptic plasticity of the memristors, where they can mimic the biological synapse or neuron (neuromorphic) [3]. A lot of parameter should be considered to achieve high-performance memristor-based artificial synapses (dynamic range, linearity, asymmetry, level of states, etc.) [4]. Much effort has been conducted to improve these parameter, such bi-layering [5], irradiation [6], doping [7], and deposition engineering [8]. Most of synaptic parameters can also be enhanced by tuning the potentiation and depression pulse schemes [5]. Nevertheless, none of these parameters can be performed by memristors that exhibit digital characteristics. On the other hand, several challenges exist in fabricating analog memristors, and, most often, the fabricated memristors exhibit semi- or pure digital characteristics. In this chapter, we review some important methods to induce analog characteristics by nanofabrication and electrical engineering that

could provide useful insight for the device development engineers to transform their digital memristors into analog.

Resistance switching in memristor devices, set (HRS-to-LRS) and reset (LRS-to-HRS) processes, can occur either in abrupt or gradual resistance change. **Figure 1** depicts the schematic of current–voltage and conductance-pulses curves of the abrupt and gradual resistance changes [2]. The abrupt resistance change is a phenomenon where the current or conductance of the resistance states is suddenly changed at a threshold voltage, as depicted in **Figure 1(a)** and **(b)**. Any memristor devices with this digital characteristic tend to have limited capability to exhibit multiple resistance states (multibit performance). Henceforth, this abrupt behavior is also called digital switching. The only possible way to induce multibit performance is by varying the current compliance level to limit the size of the conduction filaments, and thus it controls the amount of the current that can pass through the cell (**Figure 1(b)**). On the other hand, gradual resistance change is a phenomenon where the device does not require any threshold voltage to change the current or conduction of the states, as depicted in **Figure 1(c)** and **(d)**. In this case, any given voltage or electrical pulse stimulus is able to modulate the current or conduction of the states [9]; thus, the number of the states that the memristor can exhibit is equivalent to the number of voltage or pulse stimulus it can response to (**Figure 1(d)**). Henceforth, this gradual behavior is also called analog switching.

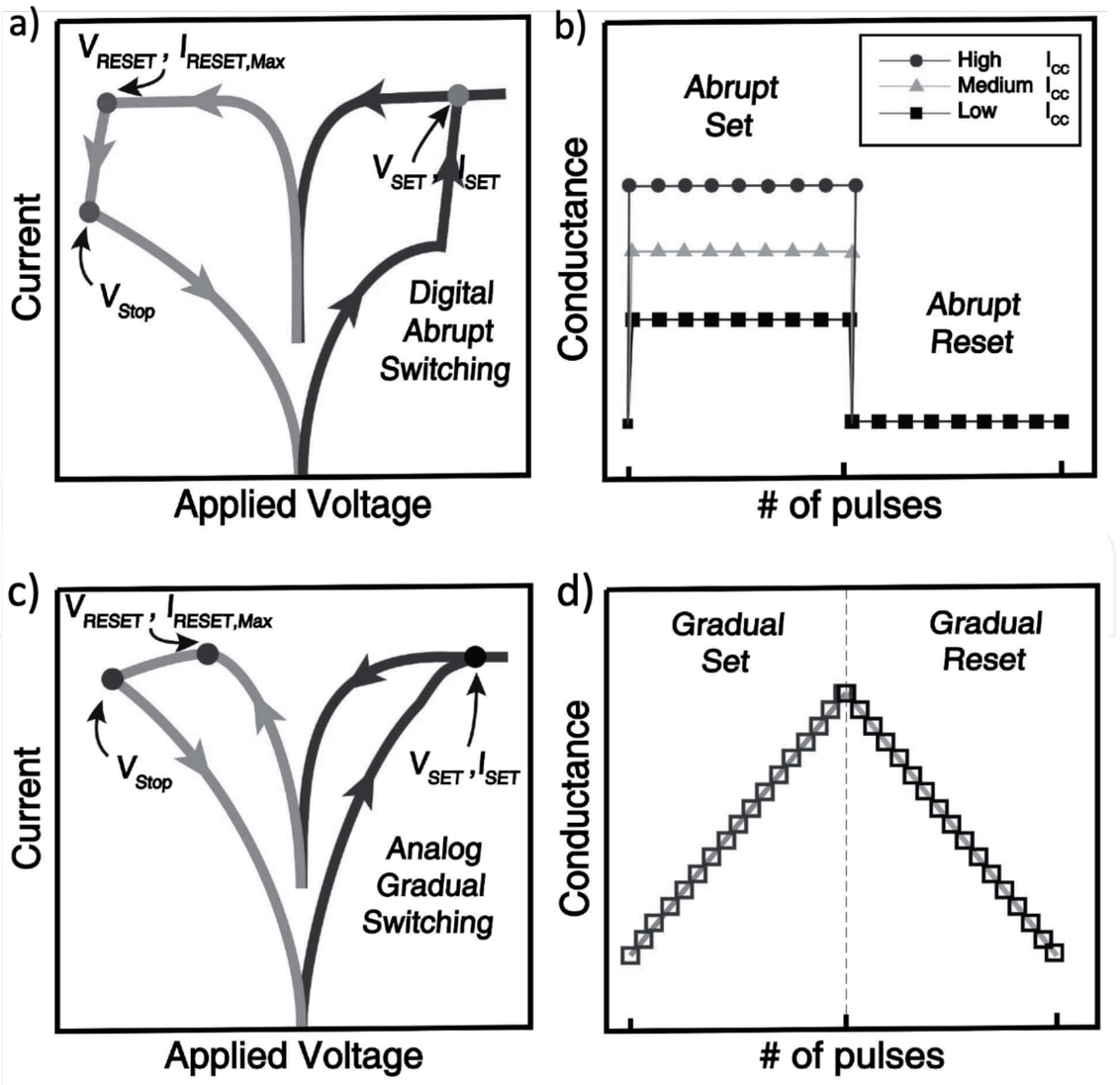

Figure 1.
Schematic of (a, b) digital and (c, d) analog switching behaviors. Reprinted from [2].

It is important to note that, based on our knowledge, the memristor, which works under unipolar mode (employing the same voltage polarity to set and reset the device), cannot show analog switching due to the rapid Joule heating process. Hence, the memristor should be designed in such a way where the Joule heating should not play a major role in its switching mechanism. Bipolar mode, however, has several variants of mode, such as conventional, complementary, and diode-like bipolar modes. **Figure 2** shows the conventional and complementary bipolar resistive switching in Pt/ZnO/TiN memristor that was observed by Khan SA et al. [10]. They suggested that the two modes can be exhibited by varying the bias condition; counter-clockwise and clockwise voltage sweeps exhibit conventional (BRS) and complementary (CRS) bipolar modes, respectively, as depicted in **Figure 1(a)** and **(b)**. The efficacy of the modes on

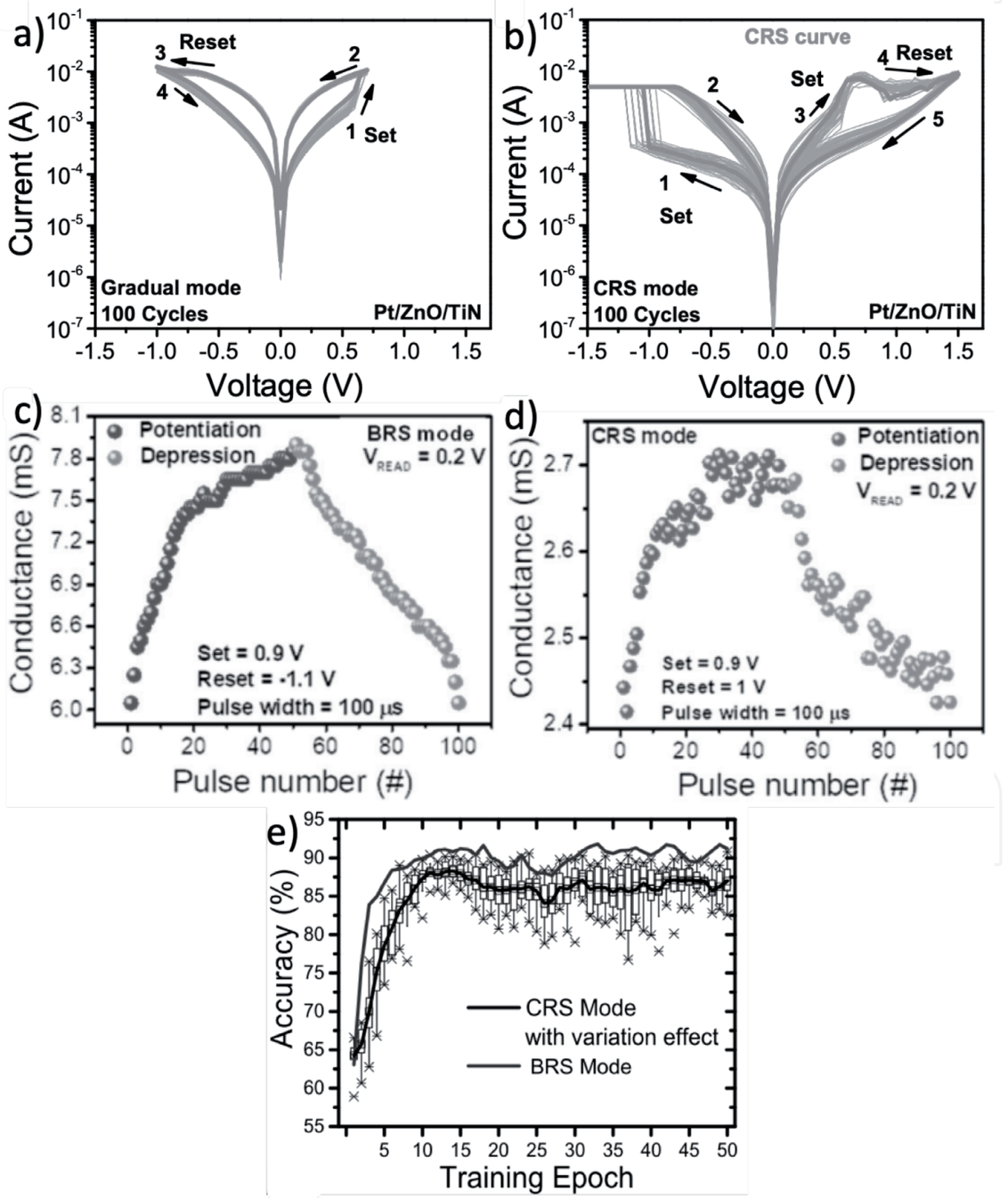

Figure 2.
I-V curves of (a) conventional analog bipolar (BRS) and (b) complementary (CRS) resistance switching modes in Pt/ZnO/TiN memristive device. Synaptic potentiation and depression of (c) BRS and (d) CRS. Epoch training accuracy of BRS and CRS devices. (e) Training accuracy of CRS and BRS modes. Reprinted from [10].

the synaptic performance was studied **Figure 1(c)** and **(d)**. Although both modes can exhibit synaptic plasticity (potentiation and depression characteristics), BRS performs superior linearity than that of CRS and, thus, better training accuracy (**Figure 2(e)**).

Memristors having a complementary or a diode-like mode offer benefit to the circuit integrations, which they do not need to be stacked with an additional select device in the array configuration [11, 12]. However, the exact switching mechanism of the complementary and diode-like bipolar modes is still not fully understood. Likewise, the synaptic properties of the complementary and diode-like memristor devices are still less investigated. Henceforth, based on these reasons, the present chapter only focuses on the device development on the conventional bipolar memristive devices.

2. Digital-to-analog switching transformation

In some cases, a memristor device can show both abrupt and digital behaviors in the same switching cycle, such as digital set and analog reset or vice-versa. This behavior may induce better multibit performance, but it may not be sufficient to induce satisfactory synaptic performance. For example, if the set or reset process exhibits digital behavior then we can assume that the device will not exhibit good potentiation or depression, respectively. Henceforth, it is important to have analog switching for both set and reset processes. We discuss several important techniques to induce analog behavior in memristor devices. These techniques include transforming the switching conduction from filamentary to homogeneous, adding an interfacial layer below the top electrode, and electrode engineering.

2.1 Filamentary to homogeneous switching transformation

Despite the filamentary switching is more scalable friendly, as the localized filaments (approximately 20 nm) [13] take part in the switching process than the homogeneous switching, which relies on the conduction changes of the entire bulk structure. However, the homogeneous switching tends to be easier to exhibit analog behavior. The co-existence of both filamentary and homogeneous resistive switching in a single device can be observed by adjusting the electrical operation (biasing condition).

Huang C-H et al. [14] reported that a digital unipolar in Pt/ZnO/Pt device could be controlled to show analog bipolar switching mode after reversing the bias condition at higher current compliance (CC), as depicted in **Figure 3(a)**. The reversed bias made the switching layer consists of two regions, the oxygen-rich region (below the top electrode) and the oxygen-deficient region (above the electrode), which transformed the filamentary into homogeneous switching. The reversed-biased technique can also be useful to transform filamentary bipolar to homogeneous bipolar, as reported by Ryu H. and Kim S. shown in **Figure 3(b)** [15]. They observed that applying appropriate stop voltage sweep prior to the LRS, at the negative differential region (NDR) voltage regime, can induce homogeneous switching in the Pt/Al_2O_3/TiN devices. Even though the *I-V* hysteresis of homogeneous switching is less obvious than the filamentary, it was reported that the synaptic behavior of the homogeneous switching is significantly improved, confirming the analog nature of the device [15]. A similar result was also observed in Pt/WO_x/W device [16].

The homogeneous switching tends to dominate when the device operates at a lower current regime. Li Y. et al. [17] reported that the homogeneous switching in Ag/NiO/Pt device can be observed prior to the electroformed process, as depicted

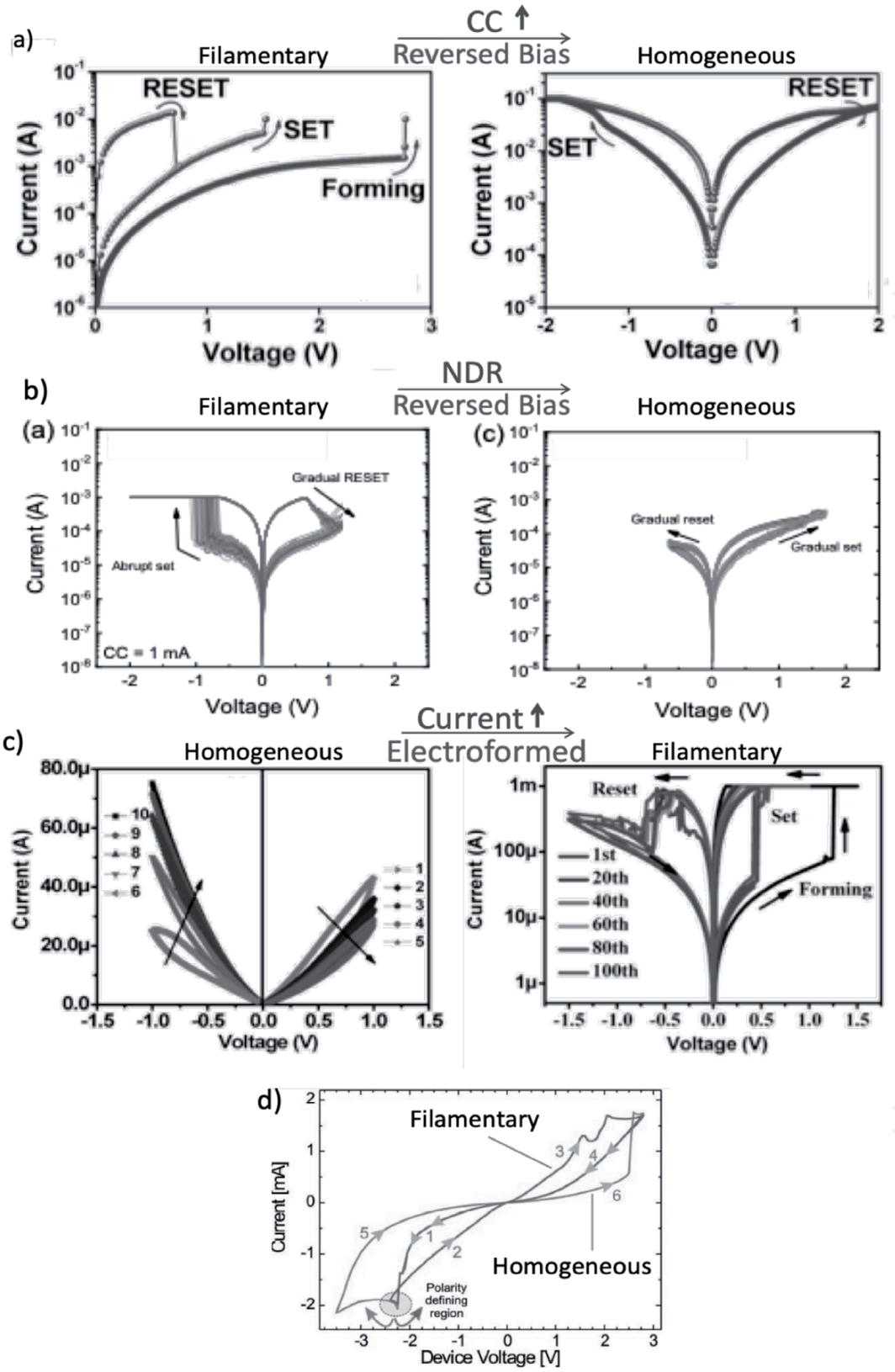

Figure 3.
Several strategies to induce homogeneous switching by controlling the biasing condition. The employment of (a) reversed bias and higher CC in Pt/ZnO/Pt device [14], (b) reversed bias at the NDR region in Pt/Al_2O_3/TiN device, [15] (c) successive voltage sweeps prior to the electroformed in the Ag/NiO/Pt device [17], and (d) opposite polarity in Fe-doped $SrTiO_3$ device [19]. Reprinted and adapted from [14, 15, 17, 19].

in **Figure 3(c)**. The successive voltage sweeps during positive and negative voltage incessantly decrease and increases the memristor conductance, respectively. Operating the device at a lower current regime unable to form the filament, but it

is sufficient to control the movement of the intrinsic defects within the bulk and, thus, modulate the Schottky barrier height (SBH). A variation of SBH was observed in this device at different scans, due to the widened of the Ag/p-NiO interface depletion width. A possible conduction mechanism of filament formation was also conferred there. Interestingly, as discussed there, the low temperature treated NiO device is not showing analog switching. A similar analog switching result was shown in PT/BiFeO3/Pt device [14]. The Ag/$CuAlO_2$/TiO2/p^{++}-Si structure was also shows similar analog switching due to the Ag ions and oxygen migration under the electric field [18]. In some cases, homogeneous and filamentary switching can also co-exist at the same current regime as well. Muenstermann R. et al. reported that the Pt/$SrTiO_3$(Fe)/Nb:$SrTiO_3$ device exhibited non-polar behavior, as shown in **Figure 3(d)** [19]. Intriguingly, the counter eightwise and eightwise switching are controlled by different switching mechanism which is filamentary and homogeneous switching, respectively.

Kim S. et al. [20] reported that the analog switching can also be achieved by a partial reset scheme. They observed that the reset process of the Cu/HfAlOx/Si device consist of two stages where the first stage (partial reset) is controlled by an electric field and the second stage (full reset) is dominated by Joule heating mechanism, as depicted in **Figure 4(a)**. **Figure 4(b)** and **(c)** show the device exhibits digital or analog switching when it operates with a full reset or a partial reset, respectively. As expected, device that was operated with a partial reset performs better potentiation and depression than that of the full reset one, as shown in **Figure 4(d)** and **(e)**. It is still not clear the physics behind this phenomenon; however, we hypothesis that this may due to the filamentary to homogenous switching transformation as well. Nevertheless, the relationship between the conduction mechanism, analog switching, and synaptic behavior should be investigated further.

2.2 Insertion layer engineering

Analog switching can be induced by inserting a metal film between the electrode and the storage layer. Here, we discuss insertion layer techniques that can transform

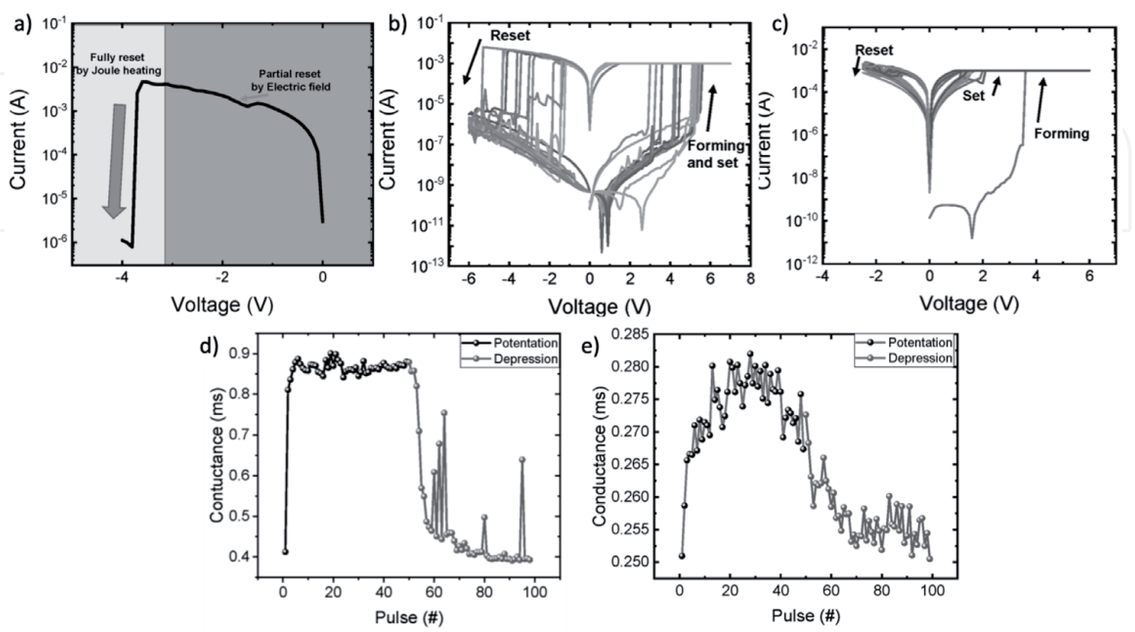

Figure 4.
(a) Two stages of reset process in Cu/AlHfOx/Si device. Switching characteristics of devices having (b) full and (c) partial resets. Synaptic behavior of the devices that operate with (d) full and (e) partial resets. Reprinted and adapted from [20].

valence change and conductive-bridge type memristors from digital into analog switching. In these techniques, a metal layer is inserted between the top electrode and storage layer to control the drift of the anions and cations defects during the switching process.

2.2.1 Oxygen scavenging layer

The formation and rupture of the oxygen conducting filament in the valence change memristor are controlled by redox of oxygen, where it is mainly taken place at the electrode/oxide interfaces [6]. Hence, in order to achieve analog behavior, we need to ensure that the oxygen ions that injected to- (set process) or from (reset process) the electrode should be continuously drifted during the entire switching process.

Chang L-Y et al. suggest that the continuous drift can be done by inserting a metal layer that has similar Gibbs free energy of oxide formation (ΔG_f) value to the storage layer [21]. **Figure 5(a)** and **(b)** show the *I-V* curves of TiN/TiO_2/Ti and TiN/Ti/TiO_2/TiN devices, respectively; the thickness of the Ti insertion layer was 4 nm. It is observed that the device without Ti insertion layer (0Ti) exhibits digital switching; conversely, analog switching can be observed after the insertion layer was employed (4Ti). This digital-to-analog switching transformation is further confirmed by the behavior of the synaptic plasticity of the devices, as shown in **Figure 5(c)** and **(d)**. Under a given pulse scheme, the conductance change of the 0Ti device rises (potentiation) and falls (depression) abruptly; meanwhile, the synaptic plasticity in the 4Ti device is more gradual.

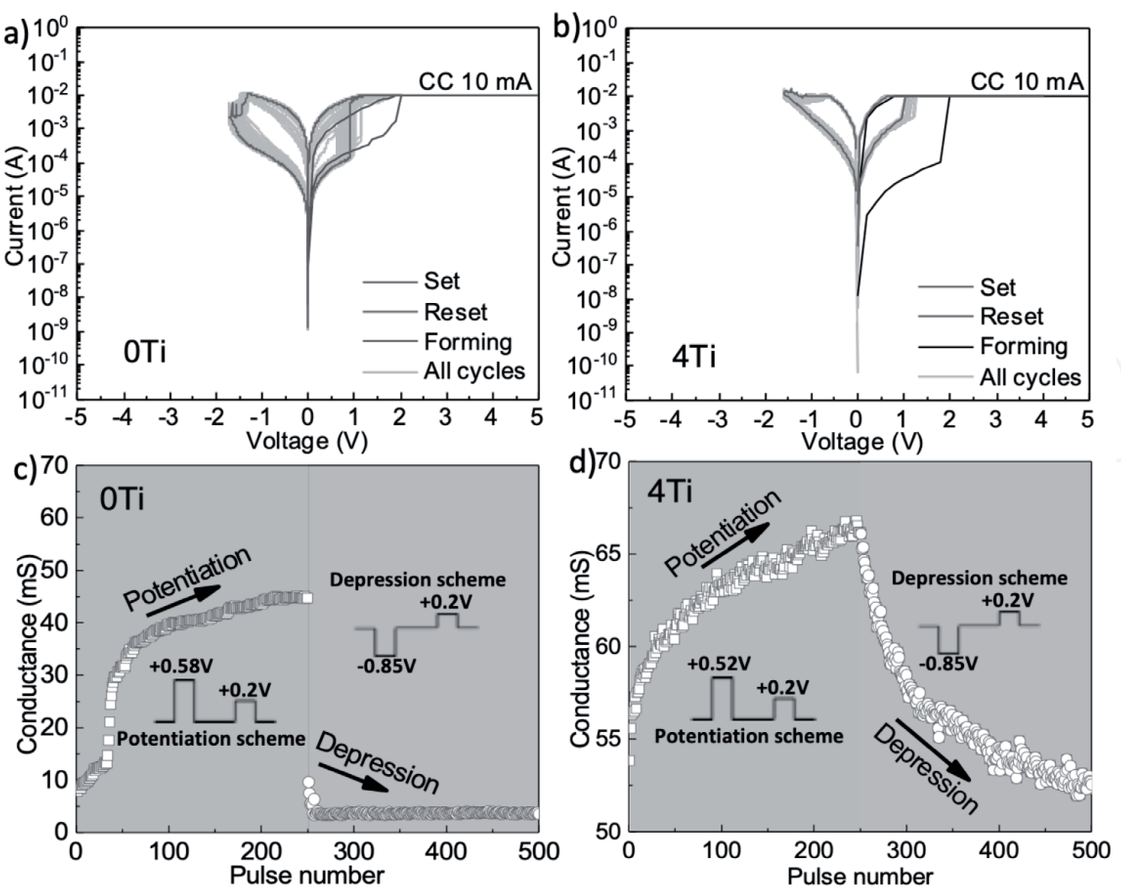

Figure 5.
Typical I-V curves of devices made (a) without (0Ti) and (b) with Ti (4Ti) insertion layer. Potentiation and depression synaptic plasticity of (c) 0Ti and (d) 4Ti devices. Reprinted from [21].

Chang L-Y et al. compared the interfacial properties between the stacks made without and with Ti layer, as depicted in **Figure 6**; for this purpose, they inserted 20 nm thick of Ti (20Ti) to obtain a more obvious reaction at the interface. Based on the depth-XPS analysis (**Figure 6(c–e)**), the Ti layer absorbed oxygen from the TiO_2 layer and forming TiOx interfacial layer at the TiN/TiO_2 interface. Note that the formation of the interfacial layer was occurred during the deposition process (pristine stack). Based on the material analysis, they proposed that TiOx interfacial layer can gradually ionize the oxygen ions during set/potentiation and reset/depression process that promotes the occurrence of gradual switching in the device (**Figure 6(f)**).

2.2.2 Cation drift barrier layer

The conductive-bridge type memristor utilizes the electrochemical metallization process where the atoms from the active electrode (Cu, Ag, or Ni) drift to the switching layer and form the conduction bridge (filament) [22, 23]. A diffusion barrier is usually employed in this type of memristor device to control the atomic drift [24, 25]. Aftab S. et al. used an oxidizable metal TiW as a diffusion barrier layer inserted between the switching layer and active metal top electrode to transform TaOx-based memritor from digital set into analog [26]. **Figure 7** shows the I-V curves and synaptic behavior of Cu/TaOx/TiN (device A) and Cu/TiW/TaOx/TiN (device B) memristors. It was observed that the device made without the TiW barrier layer exhibits digital set with a poor synaptic behavior.

In **Figure 7(a)** and **(b)** I-V curves for both devices is shown. The forming compliance current for both devices is 500 μA and set/reset cycle compliance current is 1 mA. The device with 20 nm TiW barrier layer (Device B) insertion clearly shows gradual switching for both set and reset cycles as compared to without barrier layer (Device A) device. The gradual behavior superiority is further confirmed by synaptic plasticity as shown in **Figure 7(c)** and **(d)**. By using an optimized pulse scheme with pulse width of 10 μs they observed abrupt conductance change when positive pulses are applied for potentiation process in Device A. However, Device B shows gradual change in conductance states when positive pulses are applied for

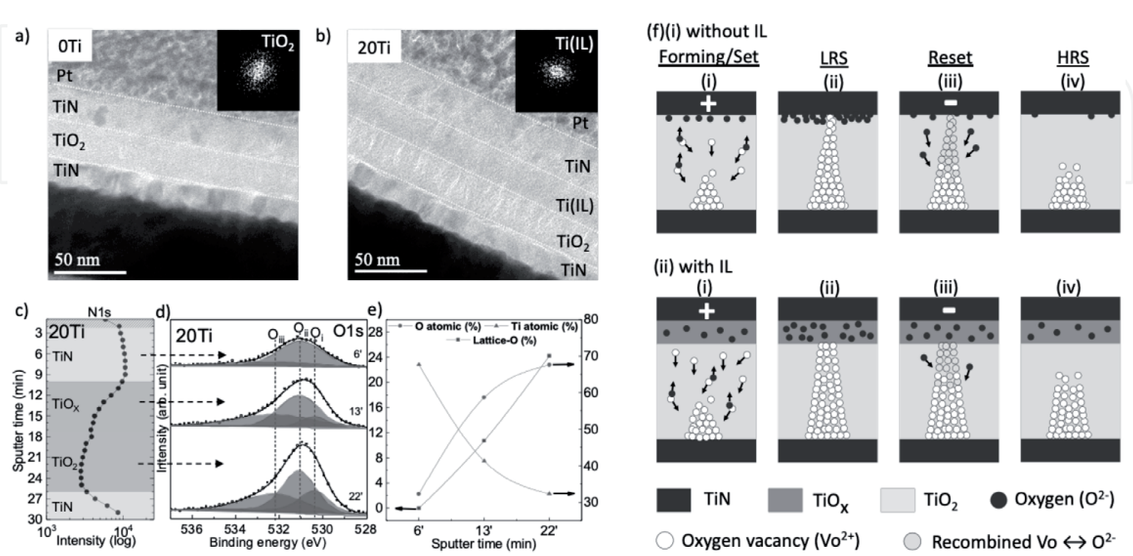

Figure 6.
Cross-sectional TEM image of (a) 0Ti and (b) 20Ti device stacks. (c) Intensity of N1s core level and (d) deconvolution of O1s core level spectra at various depth within the 20Ti stack. (e) Concentration of oxygen and titanium elements, and lattice-oxygen in the respective depth. (f) Conduction mechanism of the devices. Reprinted from [21].

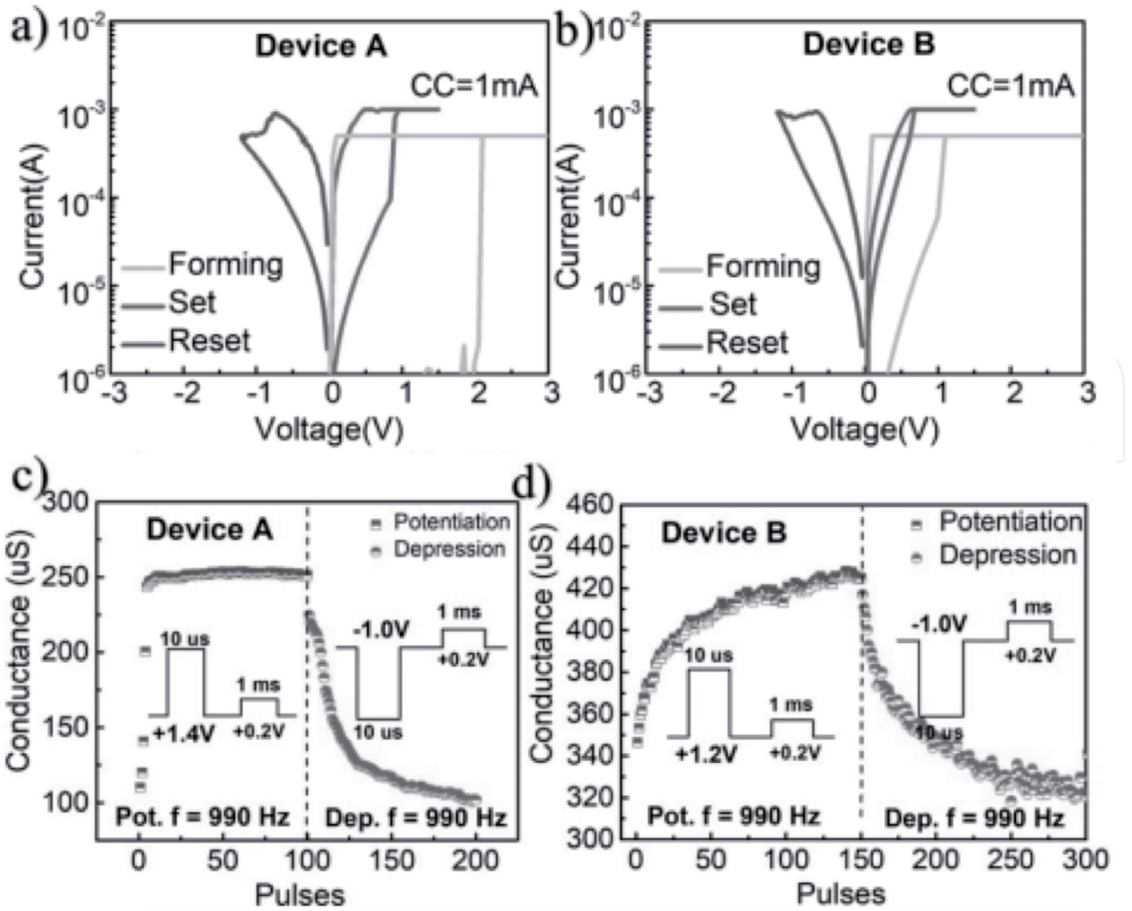

Figure 7.
Typical I-V curves and synaptic behavior of devices made without (device A) and with (device B) TiW barrier layer. Reprinted from [26].

potentiation. Note that they also observed a significant improvement in data retention of the device made with a barrier layer.

The inserted barrier layer restricts excessive metal ions diffusion into the TaOx layer and forms an oxygen vacancy-rich TiWOx layer at the interface, as depicted in **Figure 8(a–d)**. After the insertion of barrier layer, Cu diffusion into

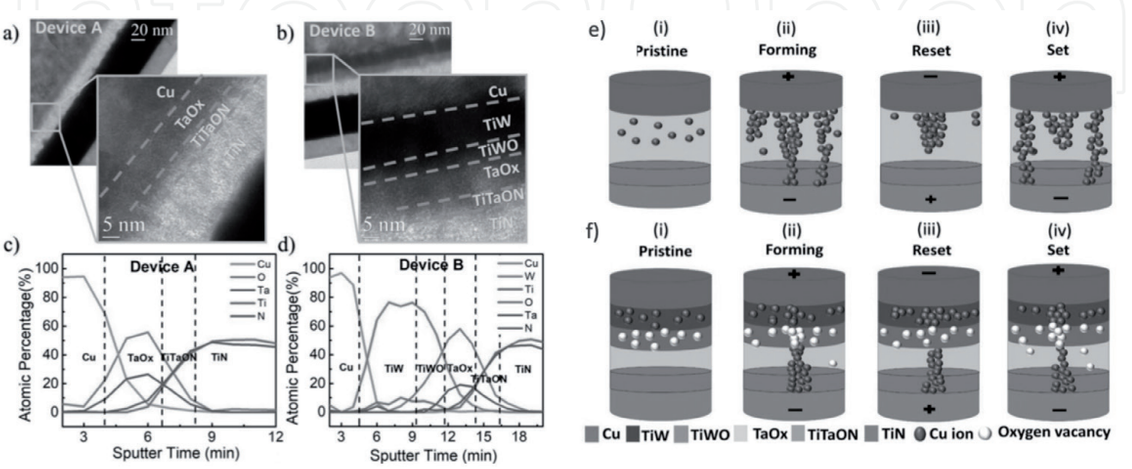

Figure 8.
Cross-sectional TEM image of (a) 0Ti and (b) 20Ti device stacks. (c) Intensity of N1s core level and (d) deconvolution of O1s core level spectra at various depth within the 20Ti stack. (e) Concentration of oxygen and titanium elements, and lattice-oxygen in the respective depth. (f) Conduction mechanism of the devices. Reprinted from [21].

the switching layer is limited to a great extent as can be seen by XPS depth spectra in **Figure 8(c)** and **(d)**. These results indicate towards the role of barrier layer TiW and interfacial layer TiWOx. The TiW insertion layer also promote confined filament which was not the case with device A having abundant Cu diffusion (**Figure 8e**). They suggest that the TiWOx interfacial layer promotes the formation of hybrid filament. Thus, device B shows superior device stability and performance compared to device A (pure metallic filament), as depicted in **Figure 8(e–f)**.

Nevertheless, Wan T. et al. [27] suggest that the digital to analog switching in Ag/$SrTiO_3$/FTO device can also be achieved with a pure metallic filament by controlling the size of the filament during the switching operation. They inserted a reduced graphene oxide (RGO) layer on top of the FTO bottom electrode. The RGO has high interfacial resistance and help to dissipate the Joule heat through the RGO. Hence, the size of the metallic filament can be easily tuned to perform good analog behavior.

2.3 Electrode engineering

Jang J.T. et al. [28] observed that a careful choice of top electrode material is crucial in achieving analog behavior. They compared Mo/IGZO/Pd (sample 1) and Pd/IGZO/Pd (sample 2) stacks. The devices made with the Pd top electrode exhibits digital switching, an abrupt transition in the resistance state during the set and reset operations are depicted in **Figure 9(a)**. On the other hand, the Mo/IGZO/Pd stack exhibits gradual transformation of resistance state for the set and reset operation, as shown in **Figure 9(b)**.

Energy band diagram analysis for sample 1 and sample 2 is depicted in **Figure 10(a)–(d)**. The abrupt switching in the Pd/IGZO/Pd stack is predominately due to a more significant barrier height of about 1 eV. A larger barrier height between the metal and semiconductor interface induces the formation of Schottky junction near the top and bottom electrode. However, the Mo/IGZO/Pd stack is observed to have a minimal barrier height of 0.3 eV, which significantly results in the formation of an ohmic junction near the top electrode and a Schottky junction near the bottom electrode. Thus, in the presence of an ohmic junction near the top electrode for sample 2, they observed a gradual switching behavior on engineering the top electrode. A similar phenomenon was also observed by Tang M.H. et al. [29] in Pt/ZnO/Pt and Ag/ZnO/Pt stacks devices. Digital unipolar switching behavior is observed in Pt/ZnO/Pt device and, conversely, the Ag/ZnO/Pt device exhibits analog bipolar switching. Although the paper does not discuss the detailed physics of such phenomenon, we assume that the contribution of Ag cations should play a role in achieving the analog behavior.

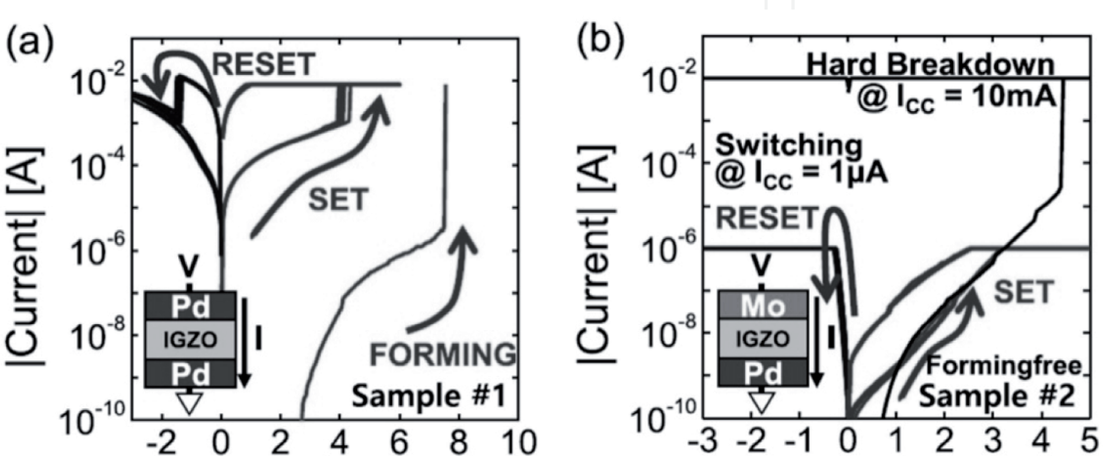

Figure 9.
Typical I-V curves of (a) Pd/IGZO/Pd (sample 1) and (b) Mo/IGZO/Pd (sample 2) reprinted from [28].

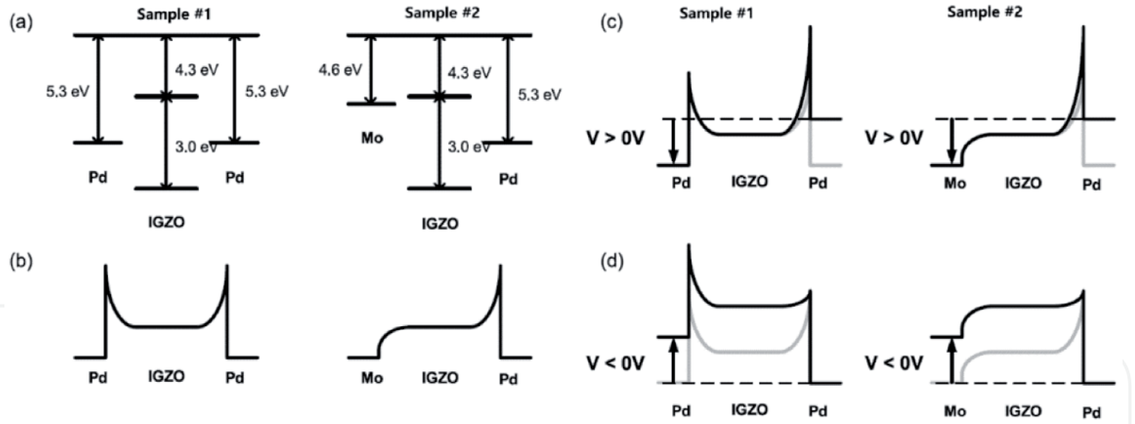

Figure 10.
The schematic of (a) flat band diagram, (b) equilibrium, (c) positive bias, and (d) negative bias energy band diagram of sample 1 and sample 2. Reprinted from [28].

Li X. et al. [30] investigated the role of inert and oxidizable top electrode materials in trilayer AlOx/TaOx/TaOy devices. The digital switching behavior is observed for the device with Pt as top electrode. The device made with Al top electrode tends to exhibit analog switching behavior. The Al top electrode interacts with the AlOx layer leading to the formation of oxygen deficient interfacial layer between AlOx and Al (top electrode). The oxygen ion migration and accumulation occur in a continuous manner and the device with Al top electrode is exhibiting gradual switching behavior during the continuous set and reset operation.

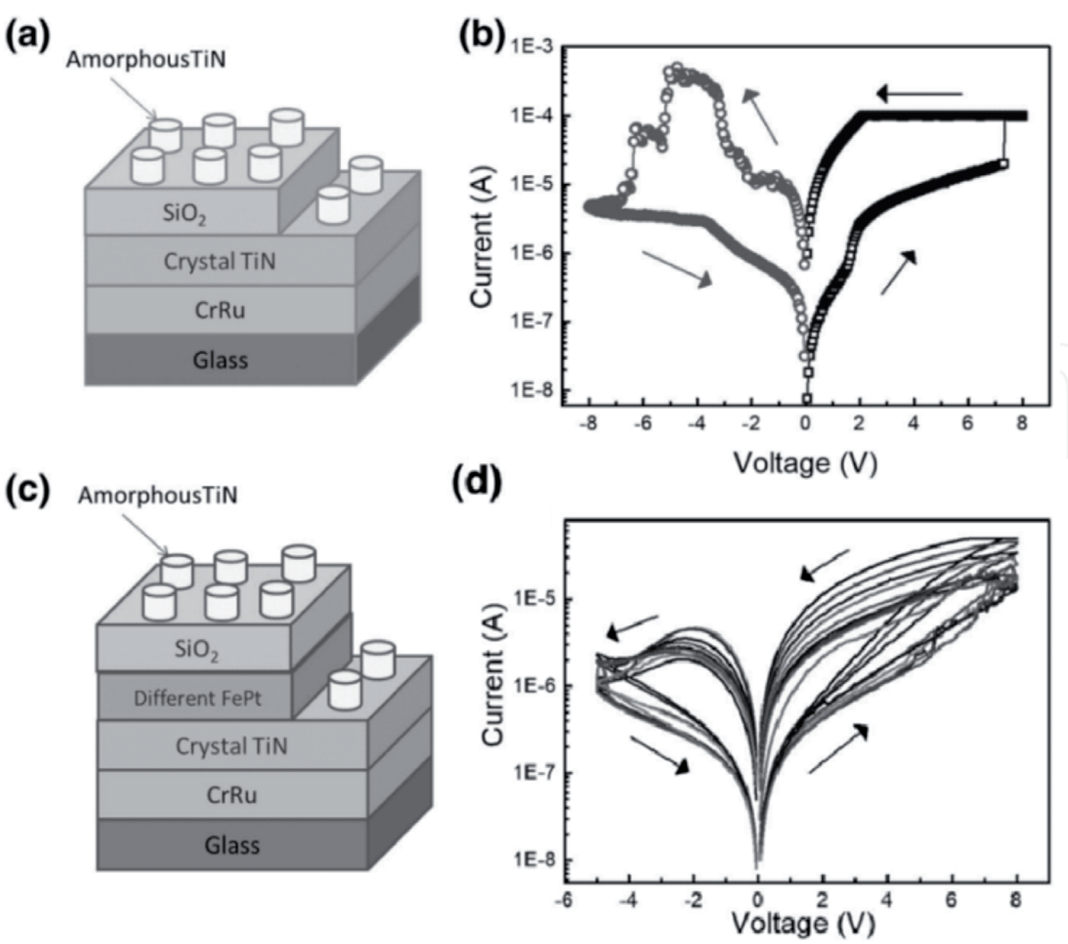

Figure 11.
The schematic and IV curve of (a) & (b) device a & (c) & (d) device B. reprinted from [31].

The method that Li X. et al. [30] proposed was further explored by C. Sun. et al. [31]. They suggest that an alloy of inert-oxidizable metal, FePt electrode, can induce analog characteristics on SiO2 based devices. The **Figure 11(a)** and **(c)** depict the schematic representation of Device A (TiN/SiO2/TiN) and Device B (TiN/SiO2/FePt/TiN). The FePt electrode act as the oxygen reservoir layer which assisting in trapping of oxygen ions during the resistive switching transformation. The barrier height of the electrode is also engineered on introducing FePt electrode which influence the switching transformation from abrupt to gradual as depicted in **Figure 11(b)** and **(d)**.

3. Conclusion

We overviewed some essential techniques to fabricate analog memristive devices. Based on the techniques that we covered here, we noticed that most of the analog memristors tend to have or work at a lower current or conduction than that of digital memristors; the resistance of the On and the Off states is higher prior to the digital-to-analog transformation. Henceforth, we can assume that the employment of low voltage or current favors the exhibition of analog behavior, and thus, the synaptic characteristics can be observed easier. We hypothesized that some other way that might work to induce digital-to-analog transformation in the memristors is to engineer the partial formation of the conductive filament; this can be done by intentionally decrease the compliance current and the voltage operation. **Table 1** summarizes the switching characteristics and synaptic behavior of several devices in reported studies. It is clear that the devices that endure digital-to-analog switching transformation often suffer from low memory window and dynamic

Device structure	Switching characteristics		Synaptic behavior		Note	References
	Analog/ digital	On/off ratio	Linearity	Dynamic range (%)		
Pt/ZnO/TiN	Analog	<10	NA	33	Bipolar switching	[10]
Pr/ZnO/TiN	Semi-analog	10	NA	12.5	Complementary switching, digital set	[10]
Cu/HfAlOx/Si	Digital	10^6	NA	125	Full reset, abrupt potentiation and depression	[10]
Cu/HfAlOx/Si	Analog	10	NA	12	Partial reset	[20]
TiN/TiO_2/TiN	Digital	>10	NA	800	Abrupt depression	[21]
TiN/TiO_2/TiN	Analog	±10	NA	26	Multibit	[21]
Cu/TaOx/TiN	Semi-analog	Unstable	0.87	150	Digital set, abrupt potentiation	[26]
Cu/TiW/TaOx/ TiN	Analog	>10	0.69	34	Multibit	[26]

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Table 1.
Several important examples of digital-to-analog switching transformation in published literature.

range. We assume that analog switching in memristor device can only work when the switching region in the cell is small or no major structural changes happen due to the repeated switching cycles or pulses.

We also addressed several challenges in the analog memristor devices that could hinder the commercialization of these devices. First, the non-linear switching modes, such as complementary and diode-like modes, have unique advantages in integrating the memristors in the array configurations; however, the synaptic reliability of the devices having these modes is still less understood, and extensive investigation is needed to study the efficacy of these modes on the synaptic plasticity. Secondly, analog memristors often suffer from short retention [14], which may not be suitable for data storage applications; however, this property opens another opportunity to modulate the long- and short-term memory plasticity of the devices that can be useful for neuromorphic computing applications. Hence, the trade-off between short retention and synaptic plasticity should be carefully managed to fit with the desired application. Third, the cycle-to-cycle operation can promote internal cell resistance variability that degenerates the analog behavior and could lead to the occurrence of digital switching [32]. Analog devices made with interfacial layer techniques may suffer from this problem due to the repeated redox reactions at the interfacial layer. Therefore, we hypothesized that a careful choice of the insertion layer plays a crucial role in achieving long cycle endurance and, thus, may prolong the exhibition of analog behavior.

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Conflict of interest

The authors declare no conflict of interest.

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