Chapter

Memristors Based on 2D Monolayer Materials

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Abstract

2D materials have been widely used in various applications due to their remarkable and distinct electronic, optical, mechanical and thermal properties. Memristive effect has been found in several 2D systems. This chapter focuses on the memristors based on 2D materials, e. g. monolayer transition metal dichalcogenides (TMDs) and hexagonal boron nitride (h-BN), as the active layer in vertical MIM (metal–insulator–metal) configuration. Resistive switching behavior under normal DC and pulse waveforms, and current-sweep and constant stress testing methods have been investigated. Unlike the filament model in conventional bulk oxide-based memristors, a new switching mechanism has been proposed with the assistance of metal ion diffusion, featuring conductive-point random access memory (CPRAM) characteristics. The use of 2D material devices in applications such as flexible non-volatile memory (NVM) and emerging zero-power radio frequency (RF) switch will be discussed.

Keywords: Two-dimensional materials, transition metal dichalcogenide, non-volatile memory, resistive switching, atomristor

1. Introduction

Memristors have been studied for several decades and a large variety of materials has been utilized in memristors. One of the most representative and well-studied materials is metal oxide, which exhibits resistive switching phenomenon and has been widely used as the active layer in resistive random-access memory (RRAM). In the recent years, two dimensional materials have been discovered and developed rapidly as the most attractive novel materials. In 2004, the first two-dimensional material, graphene (consisting of a single layer of carbon atoms), was discovered by A. Geim and K. Novoselov [1]. Since then, the remarkable and diverse electronic, optical, mechanical and thermal properties have drawn much interest and inspired a large amount of 2D materials to be identified and analyzed, including transition metal dichalcogenides (TMDs), diatomic hexagonal boron nitride (h-BN), and monoatomic buckled crystals Xenes [2]. The 2D atomic sheets can be defined as atomically thin, layered crystalline solids, featuring intralayer covalent bonding and interlayer van der Waals bonding. These materials are recognized as two-dimensional since they represent the thinnest unsupported crystalline materials that can be realized. Graphene has been utilized in electronics devices mainly as the conductive electrodes since it is a zero-gap semiconductor. The material exhibits high electron mobility at room temperature with reported values of more than 15000 $cm^2\ V^{-1}\ s^{-1}$. Nevertheless, the zero-gap nature prevents its potential

applications in field effect transistors (FET). MoS_2, a representative TMD material, has ~1.8 eV direct band gap in its monolayer form. Thus, it is suitable to be applied in FET devices [3]. In addition, hexagonal boron nitride (h-BN) also has drawn considerable attention among other 2D materials as a high band gap insulating material at ~5.9 eV, making it suitable for the production of ultrahigh mobility 2D heterostructures based on various types of 2D semiconductors [4]. Now the collection of 2D materials has been expanded to hundreds or expectedly thousands owing to more elemental and compound sheets uncovered [2, 5].

Non-volatile memory (NVM) has long been studied and developed by both academia and industry [6]. The most common non-volatile memory is flash memory [6, 7]. Although flash memory has advantages of fast read and write speed, low power consumption and less prone to damage compared with traditional hard disk drives, it has some drawbacks such as limited endurance and retention, high programming and erasing voltages, and the existing problems in small-area transistor structure like bias-temperature instability (BTI) or stress induced leakage current (SILC). In the search for the next-generation non-volatile memory, researchers have been working on various emerging alternatives, including ferroelectric random access memory (FeRAM), phase change memory (PCM), spin-transfer torque magnetic random access memory (STT-MRAM) and resistive random access memory (RRAM) [8, 9].

Among those emerging NVM, the RRAM devices show excellent endurance and retention compared with the commonly used flash memory, featuring lower power consumption, faster switching speed and better scalability [10]. The basic structure of a RRAM device is quite simple, basically a metal–insulator–metal (MIM) stacking. The conventional insulating material in RRAM is bulk metal oxides, such as SiO_2, TiO_2, or HfO_2 [11–14]. As the most common switching mechanism, conductive filaments will be formed in the insulator with external electrical bias. Depending on the formation and rupture of the conductive filament, the device can be repeatably switched between a high-resistance state (HRS) and a low-resistance state (LRS) and sustained without power supply. This is commonly referred to as the non-volatile resistance switching (NVRS) or memristive phenomenon. Recently, extensive works have been done in the development of RRAM devices not only in NVM application but also in brain-inspired neuromorphic computing due to its analog-like multi-state switching behavior [15–17].

In the past few years, motivated by the rapid development on 2D materials, researchers have found that several 2D materials also exhibit memristive phenomenon, expanding the NVRS materials to a large collection of ultrathin layered crystalline films. As a zero-gap 2D material, graphene is not suitable for resistance switching devices. On the other hand, graphene oxide has been successfully proved as the active layer in memristors [18]. MoS_2 is a representative 2D semiconductor, which has been found to show memristive effect in the form of 1 T phase [19]. In addition, Sangwan et al. reported that grain boundaries in monolayer MoS_2 film can produce NVRS in planar (horizontal) structure [20]. Nevertheless, the planar structure without 3D stacking ability has the limitation of low integration density. Another example is h-BN, a representative 2D insulator, which has been demonstrated to show the resistive switching behavior in multilayer nanosheets [21]. However, the monolayer 2D materials were not reported to exhibit the effect in vertical MIM configuration.

In this chapter, the memristors based on 2D monolayers (primarily TMDs and h-BN) are presented and discussed [22–25]. The devices (collectively labeled as atomristors) feature forming-free bipolar and unipolar switching, with relatively low switching voltages down to <1 V and large on/off current ratio of more than 10^6. Besides DC operation, the device can switch with fast switching speed by pulse

operation (< 15 ns). An atomic-resolution Dissociation-Diffusion-Adsorption model has been proposed attributing the enhanced conductance to metal atoms/ions adsorption into intrinsic vacancies, a conductive-point mechanism supported by first-principle calculations and scanning tunneling microscopy (STM) characterizations [25, 26]. Besides voltage-sweep DC measurement, other characterization method like current sweeping and constant electric stress can be employed on the 2D-based memristors and illustrates more information in the resistive switching mechanisms [27, 28]. Benefit from the ultra-thin nature of the active layer, a novel application, RF switch, is realized based on the atomristors with operating frequencies covering the RF, 5G, and mm-wave bands and exhibits superior performance compared to those of existing solid-state switches [29–31]. The results discussed in this chapter have been organized and reproduced with permissions based on several representative publications in this field.

2. Fabrication of 2D-based memristors

A dozen 2D materials have been investigated for non-volatile resistive switching, including transition metal sulfides (MS_2, M = Mo, W, Re, Sn), transition metal selenides (MSe_2, M = Mo, W, Re, Sn, Pt), a transition metal telluride ($MoTe_2$), a TMD heterostructure (WS_2/MoS_2) and an insulator (h-BN). These selected 2D materials can be readily grown as mono or few layers with unambiguous characterization of material quality and thickness, using chemical vapor deposition (CVD) or metal–organic chemical vapor deposition (MOCVD) method [32, 33].

Two device structures were used for the 2D-based memory device fabrication. First is the typical crossbar device with the advantages of small-area capability and better probing condition. The schematic and optical image of MoS_2 crossbar device are shown in **Figure 1a** and **b**. Most of the electrical measurements were performed on the crossbar devices. The other structure, the litho-free and transfer-free device, was fabricated based on the 2D materials directly on metal foils to avoid possible residues or contamination induced by lithography or transfer process (schematic shown in **Figure 1c**). The crossbar device fabrication started with bottom electrodes (BE) patterning by electron beam lithography and 2 nm Cr/60 nm Au metal stack deposition on an SiO_2(285 nm)/Si substrate. Monolayer TMD was then transferred onto the fabricated substrate using a resist-free polydimethylsiloxane (PDMS) stamp transfer method. In this method, monolayer TMD was brought into conformal contact with PDMS. The substrate-TMD-PDMS system was subsequently soaked into diluted water. Since the original SiO_2 substrate is hydrophilic, it is easy for water to diffuse into the TMD-substrate interface, which helps separate the two layers. Then, the PDMS-TMD film was brought into contact with the target substrate with BE on it. The PDMS stamp was peeled off to leave monolayer TMD films on the target substrate. CVD h-BN was transferred onto BE from the Ni foil

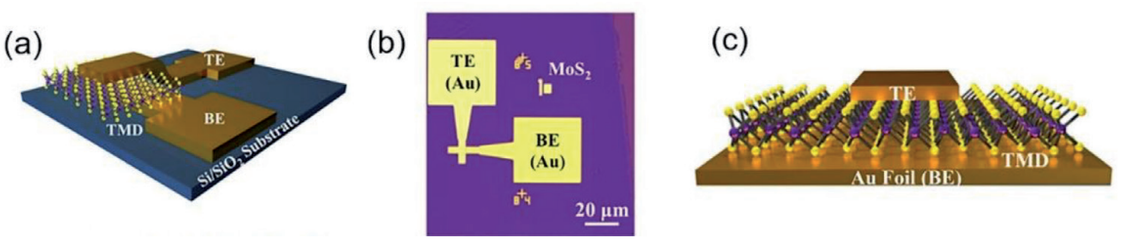

Figure 1.
(a, b) schematic and optical image of MIM structure of TMD crossbar device. (c) Schematic of TMD litho-free and transfer-free device based on MoS_2 grown on Au foil.

substrate using another poly(methyl methacrylate) (PMMA)-assisted wet transfer method. A thin layer of PMMA was spin coated onto the h-BN/Ni and then the Ni was etched away in 0.5 M ammonia persulfate solution. The PMMA/h-BN was rinsed in DI water to remove any etchant by-product before lifting by the target substrate with BE. The PMMA was then removed by immersing in acetone. For crossbar devices, top electrodes (TE) was patterned by e-beam lithography and deposited by e-beam evaporation using the same fabrication process as BE. In litho-free and transfer-free device, metal foils were used as global BE, and the TE (60 nm Au) was deposited via a shadow mask.

3. DC and pulse switching characteristics

DC electrical measurements were performed on as-fabricated devices consisting of atomic sheets with Au bottom and top electrodes and revealed memristive phenomenon in a dozen 2D systems (**Figure 2**). For instance, MoS_2, the prototypical

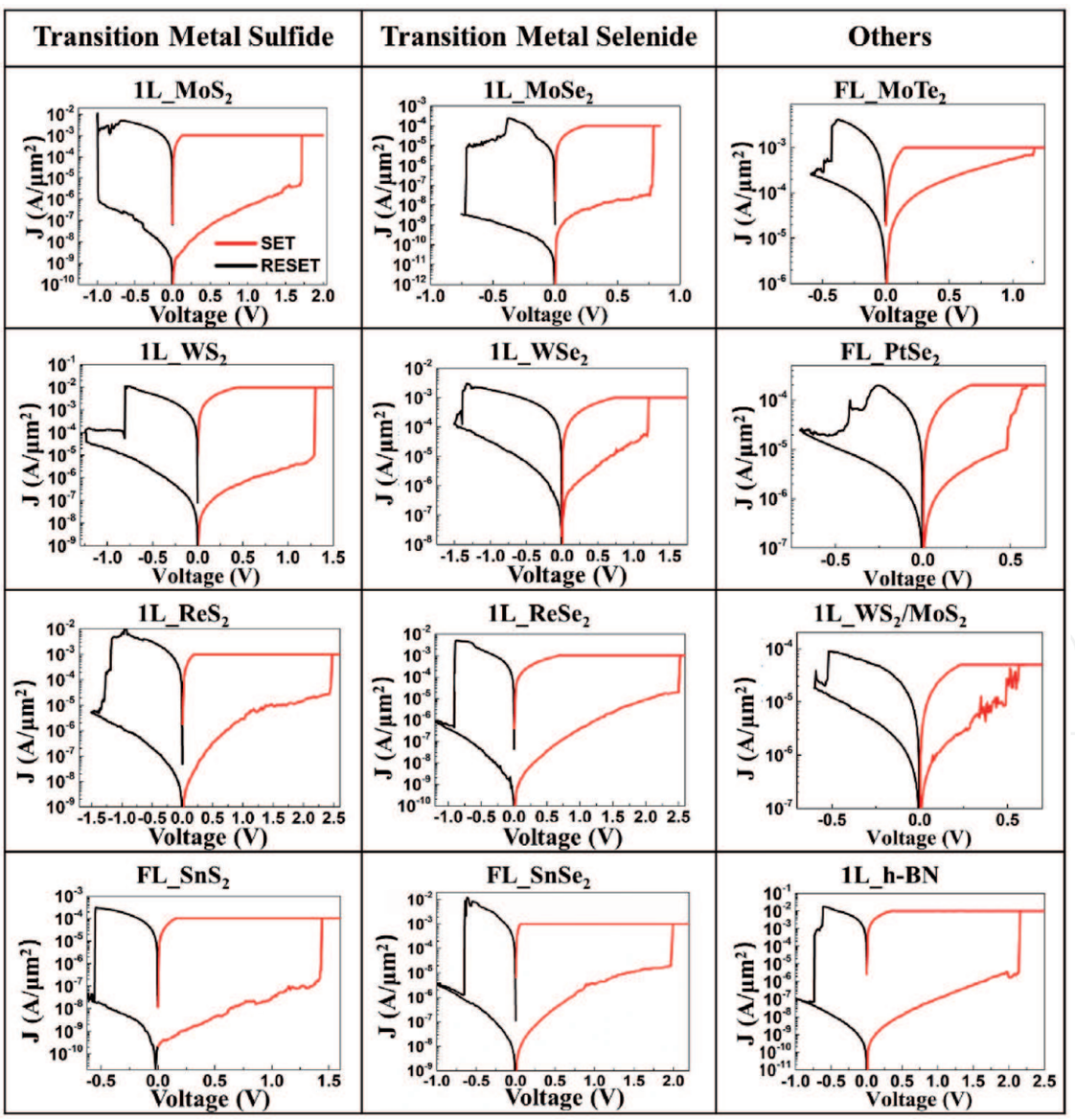

Figure 2.
Typical I-V curves of resistive switching behavior in crossbar devices for single-layer (1 L) MoS_2, WS_2, ReS_2, $MoSe_2$, WSe_2, $ReSe_2$, h-BN, and few-layer (FL) SnS_2, $SnSe_2$, $MoTe_2$, and litho-free device for monolayer WS_2/MoS_2 heterostructure, and multilayer $PtSe_2$. The y-axes are normalized as current density J.

TMD, featured low currents corresponding to a high-resistance state until the application of ~1.7 V, which "SET" the 2D-layer switch to a low-resistance state that maintains until a negative voltage is applied to "RESET" it. A compliance current is typically applied during SET process to prevent irreversible breakdown, while no compliance current is needed during RESET process. Interestingly, the monolayer non-volatile memory devices required no electro-forming step, a prerequisite in transition metal oxides (TMOs) that initializes a soft dielectric breakdown to form a conductive filament for following resistive switching operation [10]. Although some researches have shown that electroforming can be avoided by thickness scaling into the nm-regime, excessive leakage current from trap-assisted tunneling is a limiting consequence [10, 34]. Here, an ON/OFF ratio above 10^5 can be achieved in 2D NVRS devices, which highlights a defining advantage of crystalline monolayers over ultrathin amorphous oxides. These collective results of memristive phenomenon in representative atomic sheets allude to a universal effect in non-metallic 2D materials which opens a new avenue of scientific research on defects, charge, and interfacial phenomena at the atomic scale, and the associated materials design for diverse applications. Certain 2D memristors of the same MIM construction feature unipolar switching where voltage of the same polarity is used for both SET and RESET programming. Regarding the polarity dependence, the precise understanding of the factors that produce either bipolar or unipolar switching in 2D sheets is yet unclear and deserving of atomistic and unipolar switching is a complex competition among several parameters including lateral area, grain size, and modeling and microscopy studies for elucidation. A recent study in TMOs have suggested that the co-existence of bipolar compliance conditions, which may help the understanding of the phenomenon [35]. However, the underlying physics of unipolar switching has been previously established to be originated from electro-thermal heating that facilitates diffusion. A symptom of this effect is that a relatively higher RESET current is required to increase the local temperature to break the conductive link.

In most of the experiments, gold was selected as an inert electrode to rule out any switching effect that might arise from possible interfacial metal oxide formation. Furthermore, to rule out the undesirable contribution of polymer contamination from microfabrication, very clean devices including lithography-free and transfer-free devices (**Figure 3a**) were made, which also produced the memristive effect, alluding to an intrinsic origin. The lithography-free and transfer-free devices are based on monolayer MoS_2 grown directly on gold foil [36].

Previously reports have shown that line or grain boundary defects in polycrystalline 2D multi-layers play an intrinsic role in switching [37]. While it may be a possible factor in monolayers, it is not an exclusive factor as shown in **Figure 3b** from a vertical MIM device realized on a single-crystal CVD MoS_2, highlighting the potential role of localized effects. In addition, the NVRS phenomenon is not restricted to inert electrodes, since monolayer TMD with electrochemically active (Ag) electrodes can produce memristive effect as presented in **Figure 3c**. Moreover, monolayer graphene has also been demonstrated to be a suitable electrode option (**Figure 3d**).

Switching performance of retention time, DC switching cycling and variability was measured in 2D-based memristors. The NVRS devices present distinct advantages in terms of ultimate vertical scaling, down to an atomic layer thin with forming-free characteristics. By replacing metal electrodes with graphene, the entire memory cell can be scaled below 2 nm. Also, the transparency of graphene and the unique spectroscopic features of 2D materials provide the advantages of direct optical characterization for in-situ studies and in-line manufacturing testing. At an early stage, manual endurance data (**Figure 4a** and **b**) is not yet sufficient to meet the strict requirements for solid-state memory, a reflection of the nascent state of 2D atomristors compared to TMO memristors, which had similar endurance

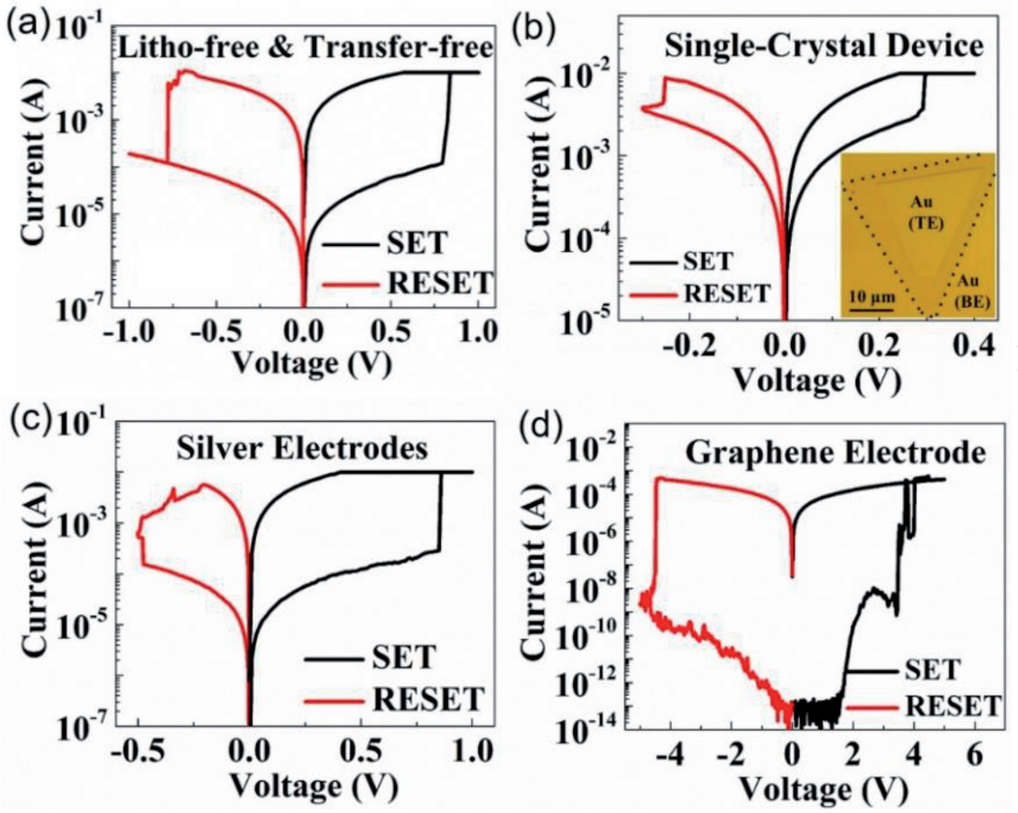

Figure 3.
Typical I-V curves of monolayer MoS_2 memristors with different device conditions, including (a) litho-free and transfer-free device, (b) single crystal device, (c) litho-free device with Ag as BE and TE, and (d) crossbar device with graphene as TE and Au as BE.

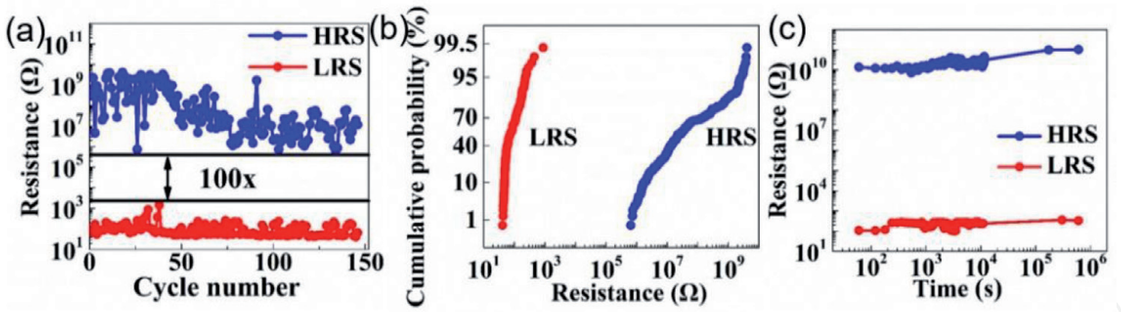

Figure 4.
(a,b) Endurance and resistance distribution of MoS_2 crossbar MIM device with 150 manual DC switching cycles. (c) Time dependent measurements of MoS_2 crossbar switch featuring stable retention over a week at room temperature.

(<10^3 cycles) in early research but has now advanced above 10^6 cycles. Oxidation by interface engineering or doping may improve endurance performance, similar to what has been observed in amorphous-carbon memory devices [38]. Preliminary retention test of non-volatile states shows up to a week (**Figure 4c**), which is already sufficient for certain neuromorphic applications involving short and medium-term plasticity [39]. In addition, the sub-nanometer thinness of monolayers is promising for realizing ultra-high densities in 3D array architecture. As an estimation, at a loose pitch of 10 nm, an atomristor density of 10^{15}/mm^3 would provide ample room to mimic the density of human synapses (~10^9/mm^3). For single-bit single-level memory storage, it corresponds to a theoretical areal density of 6.4 Tbit/in^2.

Beyond DC characterization, pulse SET/RESET is feasible for 2D-based memristors (see **Figure 5** for monolayer h-BN device). The read I-V curves before

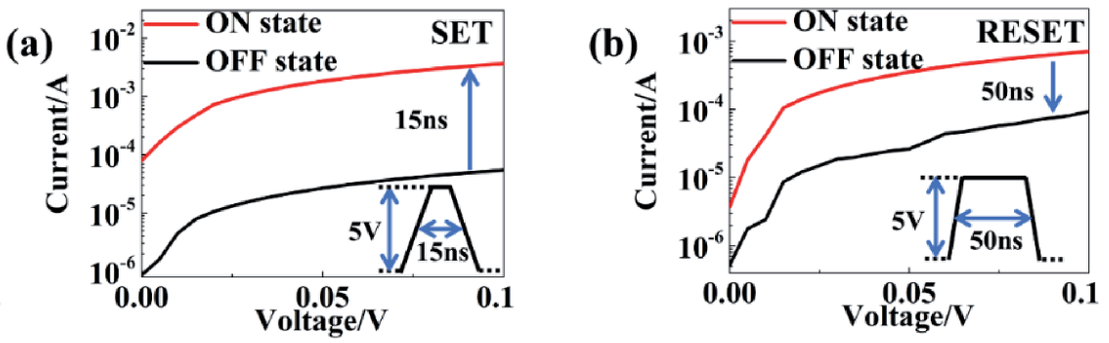

Figure 5.
(a) 15 ns SET and (b) 50 ns RESET pulse demonstration in h-BN memristor.

and after applying pulses clearly show the switching from OFF to ON state and from ON to OFF state, with 15 ns SET switching speed, and 50 ns RESET switching speed.

4. Parameter-dependent studies in 2D-based memristors

To gain more insights into the underlying mechanism(s), electrical measurements with the dependence of temperature, area scaling, compliance current, voltage sweep rate and layer thickness were performed with MoS_2 as the active layer owing to its greater material growth and characterization maturity. The low-voltage I-V characteristics at different temperatures are analyzed to explain the electron transport mechanisms at LRS and HRS. Metallic ohmic conduction can be deduced at LRS (**Figure 6a**) since the current decreases as the temperature increases, and the normalized conductance

$$G_n = (dI/dV)/(\mathrm{I}/\mathrm{V}) \tag{1}$$

is approximately one, a signature of linear transport that can be attributed to direct tunneling

$$J \propto KV \exp\left(\frac{-4\pi d\sqrt{2m^*\varphi}}{h}\right) \tag{2}$$

Where J is the current density, m^* is the effective mass, φ is the tunnel barrier height, h is Planck's constant, and K is proportional to the lateral area (A) and dependent on the barrier parameters (m, φ, d) [40]. d is the 2D barrier thickness. The direct tunneling model exhibits linear transport characteristics and is illustrated with an MIM band diagram (**Figure 6a**). Non-linear I-V characteristics are observed at HRS (**Figure 6b**), showing the current increasing as the temperature increases. The HRS data can be best fitted by the Schottky emission model with good agreement (**Figure 6c**) [40].

$$\mathrm{J} \propto A^* T^2 \exp\left[\frac{-q\left(\phi_B - \sqrt{\frac{qE}{4\pi\varepsilon_r\varepsilon_0}}\right)}{kT}\right] \tag{3}$$

$$A^* = \frac{120m^*}{m_0} \tag{4}$$

where A* is the effective Richardson constant, m_0 is the free electron mass, T is the absolute temperature, q is the electronic charge, ϕ_B is the Schottky barrier height, E is the electric field across the dielectric, k is Boltzmann's constant, ε_0 is the permittivity in vacuum, and ε_r is the optical dielectric constant. For estimation, the effective thickness of ~1 nm is used and m^*/m_0 is ~1. The extracted barrier height is ~0.47 eV at 300 K, and the refractive index n is 6.84.

Area scaling studies have also been conducted and clearly show distinct profiles with the LRS relatively flat while the HRS has a more complicated relationship (**Figure 6d**). The LRS profile is consistent with the theory of a single (or few) localized filament(s) for TMO-based RRAM [10, 41]. With the area below 100 μm^2, the HRS resistance scales inversely with area owing to uniform conduction. For larger sizes, the resistance is relatively area-invariant, which can be attributed to the presence of localized grain boundaries. Note that the average domain size of typical CVD MoS_2 monolayer is ~10^2–10^3 μm^2. The current and resistance dependence on compliance current (see **Figure 6e** and **f**) reveal a linear relation that can be explained by an increase in the cross-sectional area of a single filament or to the formation of multiple filaments [41]. From the results of the temperature-dependent conduction experiments, the existence of Schottky barrier through TMD-metal interface from literatures [42, 43], and area-dependent studies, the NVRS behavior in MoS_2 devices can be explained by the proposed model

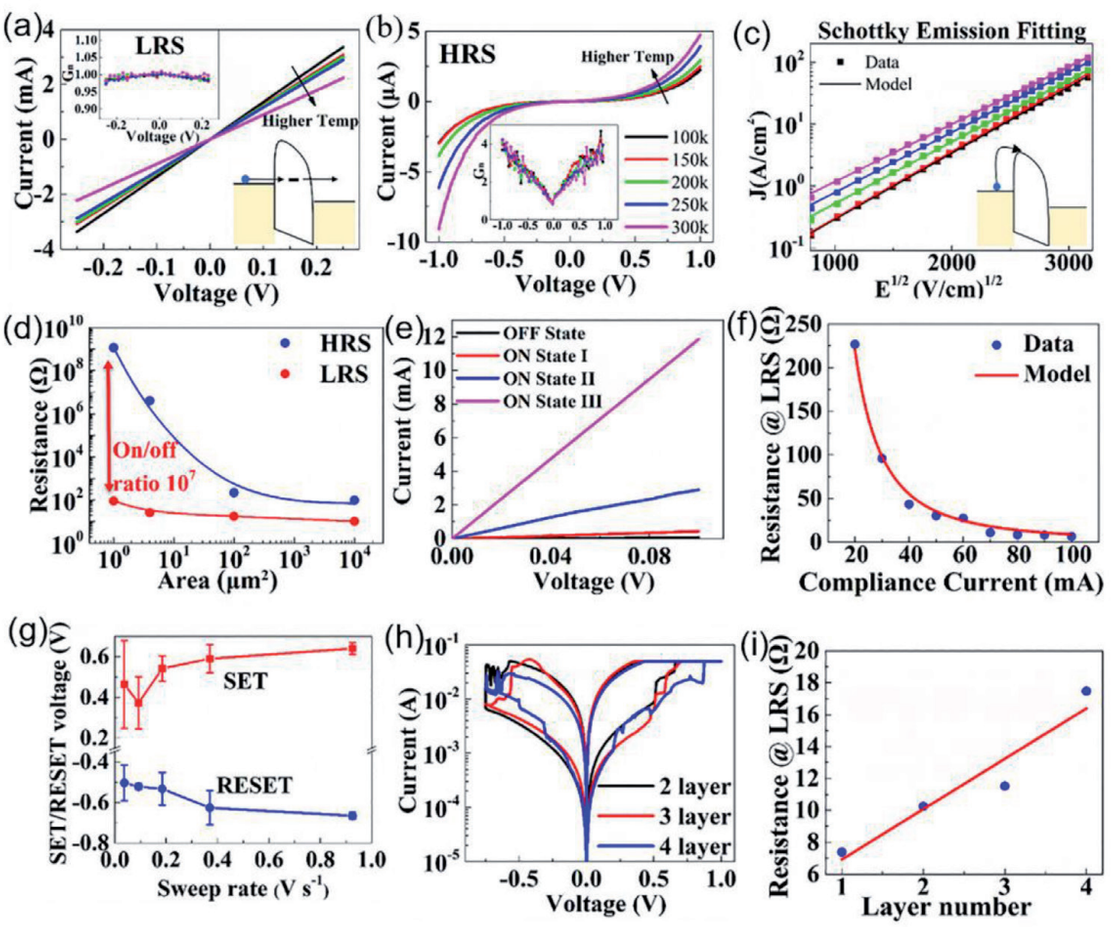

Figure 6.
Dependence of (a-c) temperature, (d) area scaling, (e, f) compliance current, (g) sweep rate, and (h, i) layer thickness of MoS_2 memristors.

that, during SET process, the electrons are transported through a filamentary-like 1D conductive link (or a virtual "conductive point"), and during RESET process, the conductive link is broken, resulting in a Schottky barrier at the device interfaces. Atomic level elucidation of the mechanisms(s) through advanced microscopy imaging and theoretical modeling is of great importance and is the focus of further research.

As to applications, the programmable resistance states are ideal for multilevel memory and neuromorphic computing. Moreover, the intrinsic low-resistance values ~5 Ω (**Figure 6f**), inspires a new application for low-power non-volatile RF switches. The dependence of the SET/RESET voltages on sweep rate (**Figure 6g**) suggests that more time is needed for ionic diffusion, which results in lower switching voltages. Layer dependent studies up to four layers demonstrate that the switching phenomena can be observed in few-layer 2D films (**Figure 6h**), with a distinction that the LRS resistance increases with layer number (**Figure 6i**).

5. Switching mechanisms in 2D-based memristors

To further elucidate the mechanism of NVRS phenomenon in 2D monolayers, a Dissociation-Diffusion-Adsorption (DDA) model has been proposed, (**Figure 7a**). In the vertical MIM structure, the symmetric electrodes choice (in most cases both TE and BE are gold) enables the formation of "conductive points" from either the top or bottom electrode. The first step is "Dissociation", which is based on the metal atom/ion dissociating from a cluster of metal atoms at the electrode-2D material interface. It is straightforward that this process depends on the choice of metal electrode. As discussed above, Au electrodes, as a noble metal, were selected to rule out potential effects from interfacial metal oxidation. It is also worth noting that Au has relatively low atomization enthalpy among various transition metals, thus can serve as an appropriate electrode [44]. First-principle calculation results have been performed and show that the dissociation energy required to move a Au atom sufficiently far from the bulk Au surface is 3.80 eV. For conventional conductive-bridge memory, the dissociation step is a common prerequisite that relies on the formation of metal ions to create a conductive filament and has been extensively investigated in previous reports, so the subsequent diffusion and adsorption steps will be the focus [45].

After Au atom/ion dissociates from the electrode, two scenarios may happen, with either directly adsorbing (chemical bonding) into a vacancy when they are close (Case 1), or it first weakly bonds to the pristine region and subsequently diffuses across the surface and finally finds a vacancy to fill and bond (Case 2). The two scenarios are illustrated in **Figure 7a**. Case 1 is a simpler scenario with only two steps "Dissociation" and "Adsorption" courtesy of the initial close position to a vacancy. On the other hand, Case 2 consists of all three steps and is expected to be more common since the adsorbed neutral Au atom (Au) or positively charged Au ion (Au^{+1}) in the pristine region are energetically favorable compared to their isolated states. Benefitting from the simplicity of Case 1, first-principle calculations for a collection of 12 materials were conducted, which have all been demonstrated to show NVRS behavior. In contrast, for the more probable Case 2, owing to the system complexity, only MoS_2 is analyzed as a prototypical monolayer in the TMD family.

In the simpler scenario Case 1, the dissociated Au is at first in an isolated state and tends to directly get adsorbed into the defect, resulting in the formation of conductive point that causes switching from HRS to LRS. It has been reported that the most common defects for 2D materials are vacancies, for example, S vacancy in MoS_2, Se vacancy in $MoSe_2$, B vacancy in BN, etc. The first-principle calculations

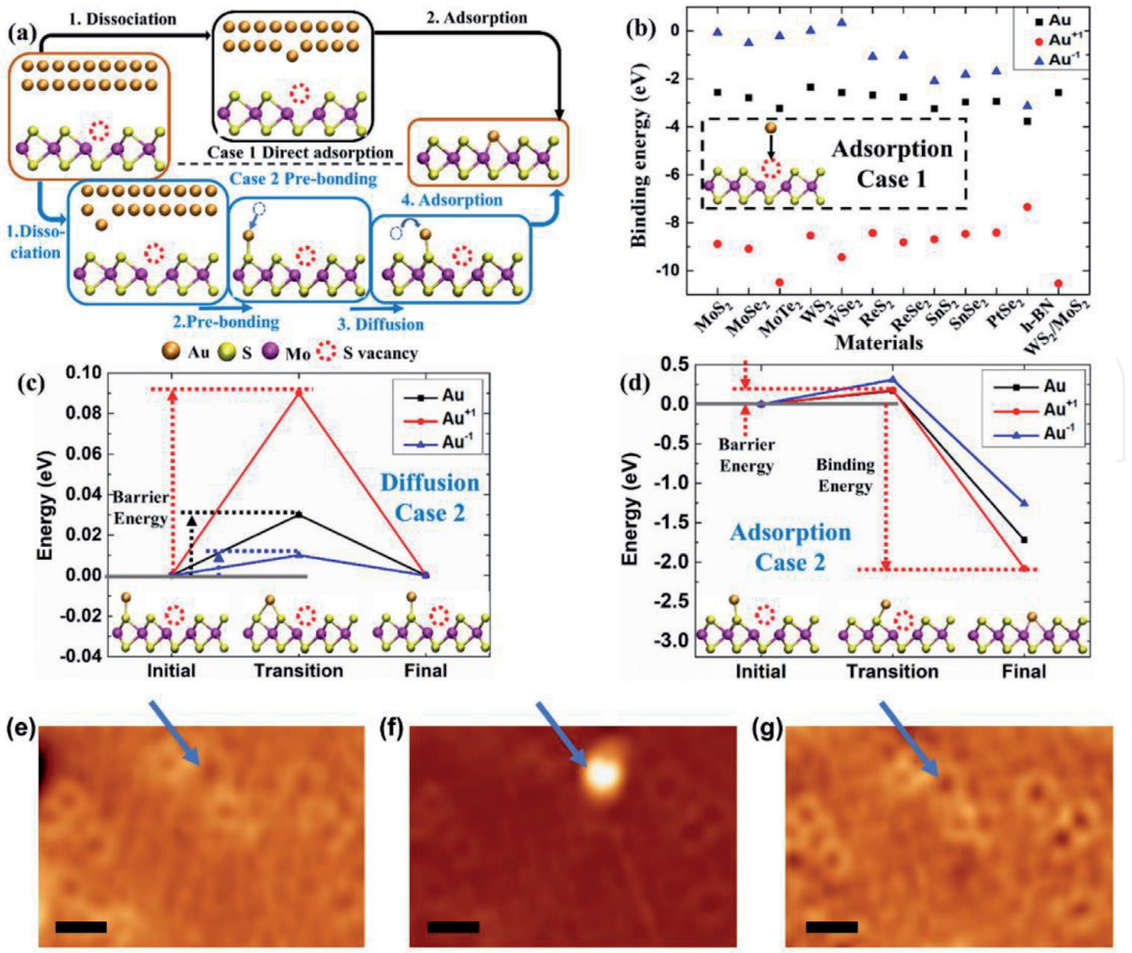

Figure 7.
(a-d) Calculated energy results and (e-g) STM observations for dissociation-diffusion-adsorption (DDA) model.

indicate that there is no barrier energy for Au to move in and bind with the defect site. This is straightforward to understand since isolated Au is unstable and the system energy tends to decrease as Au moves towards a defect site. In **Figure 7b**, the adsorption energy of Au atom/ion into a vacancy site has been calculated for various 2D materials. The negative adsorption energy (the energy difference between final state and initial state) means that adsorption is energetically favorable and releases energy, while a positive value means that the adsorption requires extra energy. Based on the calculations on diverse 2D materials, a common trend can be observed that both Au^{+1} and Au are energetically favorable to be adsorbed into defects, resulting in a SET process. To be more specific, Au^{+1} is the most favorable candidate, then neutral Au, and finally, negatively charged Au ion (Au^{-1}). A major reason for such a trend is that Au^{+1} is the most energetically unstable in its isolated vacuum state, thus releasing the most energy when covalently binding to a vacancy site, followed by the neutral Au atom and then Au^{-1}.

For the "Diffusion" step in Case 2, **Figure 7c** shows the calculated diffusion pathway and barrier energies (the energy difference between transition state and initial state) with Au moving along MoS_2 surface from the top of one S atom to the top of a neighboring S atom in the pristine region (without defects). Based on the first-principle calculations, the energy barrier for the Au atom/ion moving from one S atom site to another is quite low (< 0.1 eV), indicating that Au atom/ion can easily migrate around the pristine region at room temperature. This can be easily understood because the adsorption of Au atom/ion in the pristine region is weak, making them very mobile on the surface.

With regard to the final "Adsorption" step in Case 2, Au will diffuse to the atom close to the defect site, and eventually bind to it, since Au can easily move around the surface. **Figure 7d** shows the calculated energies for the transition and final states in the adsorption step. The low energy barrier ($\leq$ 0.18 eV) indicates that Au/Au^{+1} can adsorb from the pristine region to the defect site, especially at high temperatures due to the Joule heating from the increased electrical current. In addition, this process can release a large amount of energy ($\geq$ 1.72 eV). The low energy barrier and high energy released suggest that the adsorption of Au/Au^{+1} from the pristine region to the defect site is preferable both kinetically and energetically. However, the reversed process, for instance, the Au/Au^{+1} moving out from the vacancy site to the pristine region, has a much higher energy barrier (1.89 eV). Thus, it is much more difficult for Au/Au^{+1} to desorb from the vacancy site. As a result, Au/Au^{+1} can stably bind to the vacancy site, acting as a conducting point at LRS. During the RESET process, a high current usually passes through the conductive point, providing enough energy to overcome the barrier and driving Au/Au^{+1} away from the vacancy site. On the other hand, the Au^{-1} ion has the highest energy barrier and the smallest binding energy. As a result, the Au^{-1} ion is the least favorable to participate in the NVRS from both the kinetic and energetic viewpoints and it is not likely to play an essential role in resistive switching for both the scenarios discussed.

To provide experimental evidence to support the Dissociation-Diffusion-Adsorption model discussed above, STM measurement fitted with a gold tip was performed. STM was at first used for atomic resolution imaging of the MoS_2 surface to locate and identify the sulfur vacancies (**Figure 7e**). It was followed by a controlled physical contact of gold STM tip with the MoS_2 surface and voltage sweepings to emulate NVRS operation in a vertical MIM memory device. The STM image of the same location after SET shows a bright protrusion on the surface (**Figure 7f**). Stability of the site indicates it is not a diffusing atom. Instead, it is strongly bonded to the surface and identified as a gold atom absorbed into the sulfur vacancy [26]. RESET is realized by an opposite voltage sweeping where the gold atom is removed from the defect site (**Figure 7g**). The differences in sharpness and contrast of the STM images before and after the switching indicate that the tip apex has been changed due to the dissociation of a gold atom from the STM tip. In an extensive STM measurement, the STM tip was not only placed on top of the sulfur vacancy, but also in a pristine (defect-free) region. Compared with the I-V curves which resemble NVRS observed at the defect locations, electrical measurements on pristine regions reveal a tunneling-like I-V behavior with no switching phenomenon, suggesting the important role of defects (e.g. S vacancy) in a switching event [26].

6. Special operation methods of 2D-based memristors

To further investigate the NVRS phenomenon during SET process in the MoS_2 memristors, a current-sweep measurement method was introduced to the devices to get a more comprehensive understanding. **Figure 8a** shows the voltage–current (V-I) relationship by current-sweep method to SET a MoS_2 device. The transition starts at a HRS, followed by a gradual increase of both voltage and current. When the current reaches ~1.8 mA, the voltage suddenly decreases while the conduction current remained the same. In other words, the resistance of the device changes from a higher resistance state to a lower resistance state. Four subsequent voltage drops can be observed from 0.01 A to 0.03 A (as shown in the amplified figure). The device remains at the final lowest resistance state during and after the backward current sweeping, which indicates that a NVRS process from HRS to LRS

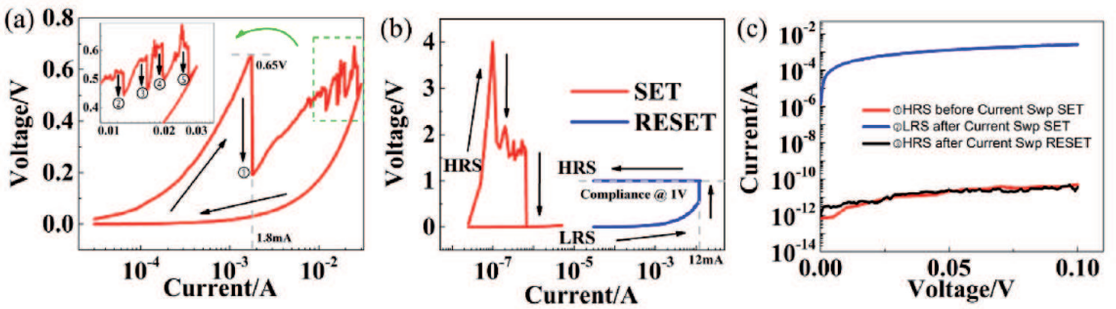

Figure 8.
(a, b) Current-sweep switching curves and (c) states reading behaviors in MoS_2 memristors.

(SET) is realized by current sweeping. Compared to the single-step SET process realized by voltage sweeping, multiple transition steps can be observed during current-sweep measurement. Note that the voltage for the first transition in current sweeping is ~0.65 V as shown in **Figure 8a**, which is very close to the SET voltage using voltage sweeping on the same device.

In **Figure 8b**, similarly, a multiple-step SET can be observed by current sweep. Moreover, the RESET process realized by current sweeping is presented in the same figure. When the current sweeps to ~12 mA, the voltage abruptly rises, suggesting a transition from LRS to HRS. This transition current is consistent with the RESET current (~10 mA) observed using voltage sweep method. Compared to RESET behavior by voltage sweeping, a compliance voltage is required in the case of current sweeping to avoid extremely high voltage across the device. Thus, it can be deduced that the RESET process is more likely to be a current/thermal-driven effect instead of voltage-driven effect. During RESET, a large amount of Joule heating can be induced by the high RESET current, which dissolves the conductive path first and then the Au ions will be migrated though porous regions or defects in the MoS_2 film, or back to the electrodes by reduction [10, 46]. This Joule heating effect is supported by the experimental observation that the transitions in voltage-sweep RESET (although sometimes with multiple steps) are sharp and sudden rather than gradual changes in 2D-based NVRS devices, a signature of Joule heating-dominated RESET process. Another evidence is that the MoS_2-based memristors can be switched in both bipolar and unipolar, which suggests it is not the electrical bias but the current level that plays a more important role in the RESET switching. **Figure 8c** shows the "READ" operations on the device before and after the current-sweep switching, which demonstrates the non-volatility of the NVRS behavior with a large on/off ratio of ~10^7. It can be observed that the resistance state after current-sweep RESET is consistent with the initial HRS state, which indicates the stable switching characteristics and alludes to a potential approach using current sweeping to improve the cycle-to-cycle variability at HRS, a long-standing issue for RRAM devices [47].

Figure 9a and **c** exhibit the switching curves of the SET process by current sweeping and RESET by voltage sweeping respectively on the same device. Similarly, the switching characteristics for current-sweep SET and voltage-sweep RESET tested on another device are shown in **Figure 9b** and **d**, respectively. Based on the statistical data of all the measured devices, a relationship can be established: normally for a device with single-step SET behavior by current sweeping (**Figure 9a**), the voltage-sweep RESET is also single-step (**Figure 9c**); on the other hand, for a device that has multiple steps during current-sweep SET (**Figure 9b**), a multiple-step RESET can be obtained by voltage sweeping (**Figure 9d**). With the

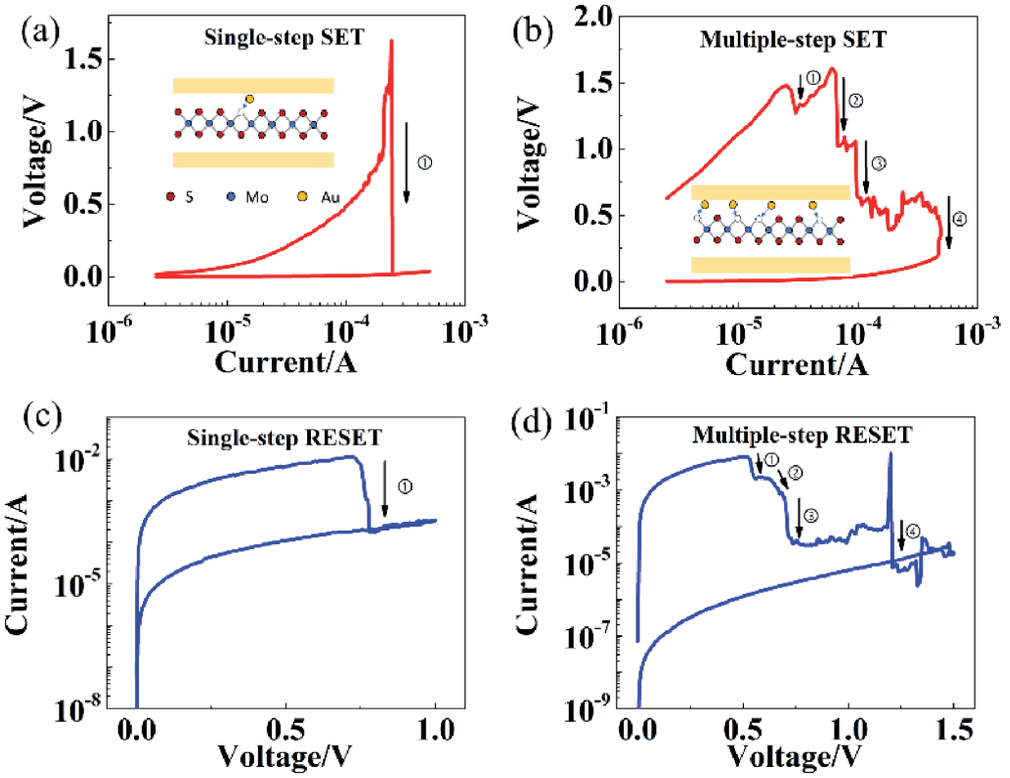

Figure 9.
The resistance switching characteristics of (a, b) current-sweep SET and (c, d) voltage-sweep RESET on the same device with similar transition behavior.

experimental results that show single or multiple transition steps, it can be inferred that multiple defect/vacancy-rich regions exist in the device area, which leads to single or multiple conductive points formation during NVRS.

Figure 10 presents the resistance evolution under constant voltage stress (CVS) on the devices at HRS. The working devices refer to the devices that exhibit stable switching characteristics and have been tested for several DC cycles and RESET to HRS before stress measurement. Then, relatively low constant voltage bias ($< V_{SET}$) is applied on the devices with positive CVS (**Figure 10a**) and with negative CVS (**Figure 10b**). It can be observed that the resistance changes from HRS to an even higher resistance state (labeled as HRS'). This phenomenon is opposite to the observation in the TMO-based devices, where the resistance is switched from HRS to LRS under CVS [48, 49]. Similar behavior has been observed with both positive and negative CVS, which can be related with the co-existence of unipolar and bipolar operations in MoS_2 memristors. Moreover, CVS test is performed on the fresh (as-fabricated) devices and shows similar HRS to HRS' transition (see **Figure 10c**). This phenomenon suggests that for both fresh devices and pre-RESET working devices, the commonly referred "HRS" is not the highest resistance, but actually an intermediate state that can still be modulated to a higher resistance state (HRS'). However, if the voltage stress goes higher than the SET voltage (**Figure 10d**), the device will switch to LRS and then fail due to high power.

The previously discussed DDA model with the assistance of metal atom/ion migration can be used to explain the NVRS phenomenon in MoS_2 memristors. The CVS test results provide more insights to this model with the tunable resistance states illustrated in **Figure 10e**. The existence of HRS' suggests that, a small portion of metal atoms may be embedded in the MoS_2 film at HRS, which could possibly

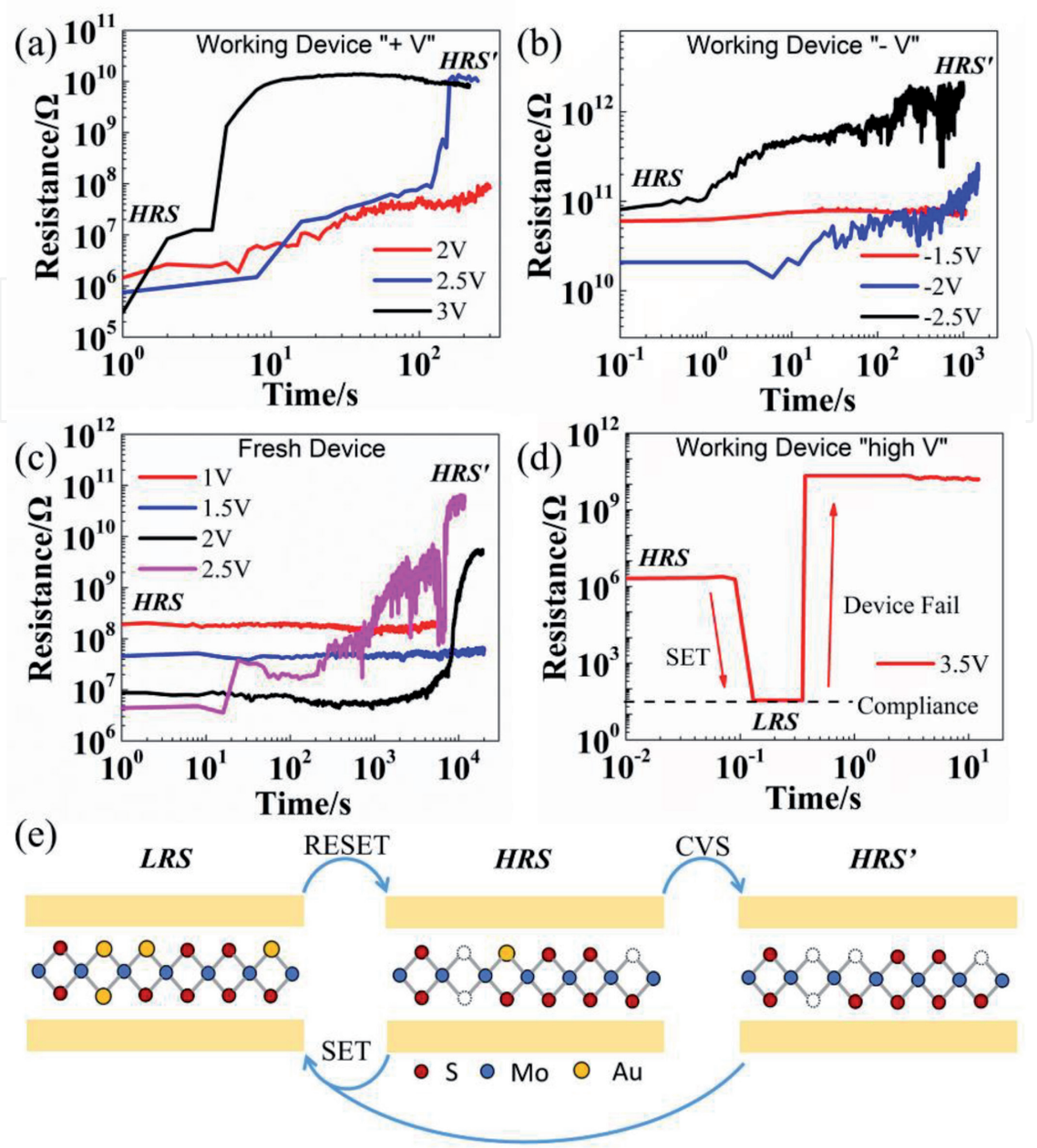

Figure 10.
(a-d) Resistance evolution under CVS MoS2-based memristors at HRS in different scenarios. (e) Illustration for the CVS process.

be induced by deposition process for as-fabricated devices or incomplete voltage-sweep RESET for working devices. Previous reports have shown experimental evidence to support this assumption that metal atoms can diffuse into the defects in 2D TMD films during the evaporation deposition process of TE confirmed by cross-sectional TEM images [50, 51]. These embedded metal atoms/ions are negligible in bulk metal oxides, but they can be important in the atomically thin MoS_2 sheets. With a relatively low voltage stress, these metal atoms tend to move out of the vacancies due to the accumulated Joule heating effect, which results in a transition to HRS'. This unique resistance evolution behavior under CVS suggests a distinct property for 2D materials. For traditional TMO-based bulk materials, the resistance state is typically controlled by the characteristics of the conductive filament and the "gap" region between the electrode and filament tip [10, 52]. While for 2D materials, the resistance state can be modulated by the interaction between atoms/ions from electrodes and interfacial vacancies, enabling atomic-level resistance control with advanced defect engineering for ultra-thin crystalline 2D materials.

7. Applications in flexible non-volatile memory and RF switch

Applications in flexible memory devices and RF switches were investigated based on 2D memristors. The high breaking strain and ease of integration of 2D materials on soft substrates can afford flexible non-volatile memory devices that can endure mechanical cycling (**Figure 11** for MoS_2-based memristor).

Non-volatile low-power RF switches represents another major application of atomristors. The low ON-state resistance values, below ~10 Ω, is critical for low-loss non-volatile RF switch circuits. The intrinsic experimental RF characteristics of monolayer MoS_2 switch show promising results of ~0.3 dB insertion loss in the ON-state (**Figure 12a**) and isolation below 20 dB in the OFF-state (**Figure 12b**) at frequencies up to 50 GHz [29]. By using monolayer h-BN as the active layer in the RF switch, the device exhibits a cutoff-frequency figure of merit of around 129 THz with a low insertion loss (≤0.5 dB) and high isolation (≥10 dB) from 0.1 to 200 GHz. In addition, it shows a high-power handling (around 20 dBm) and nano-second switching speeds, which are superior to those of existing solid-state switches [31]. This new application leads to the development of a nanoscale energy-efficient high-frequency solid-state switch technology for the rapidly growing communication systems in the 5G band and beyond.

A comparison between 2D atomristors discussed in this chapter and other representative 2D-based memory devices is presented in **Table 1**, highlighting the thinnest active layer thickness with superior switching properties and reliability as mentioned above.

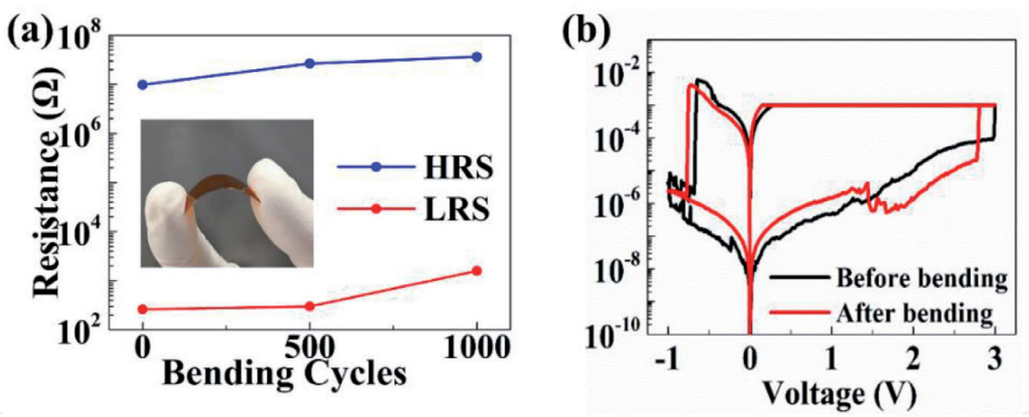

Figure 11.
(a) Stable resistance states and (b) switching behaviors after 1000 bending cycles at 1% strain.

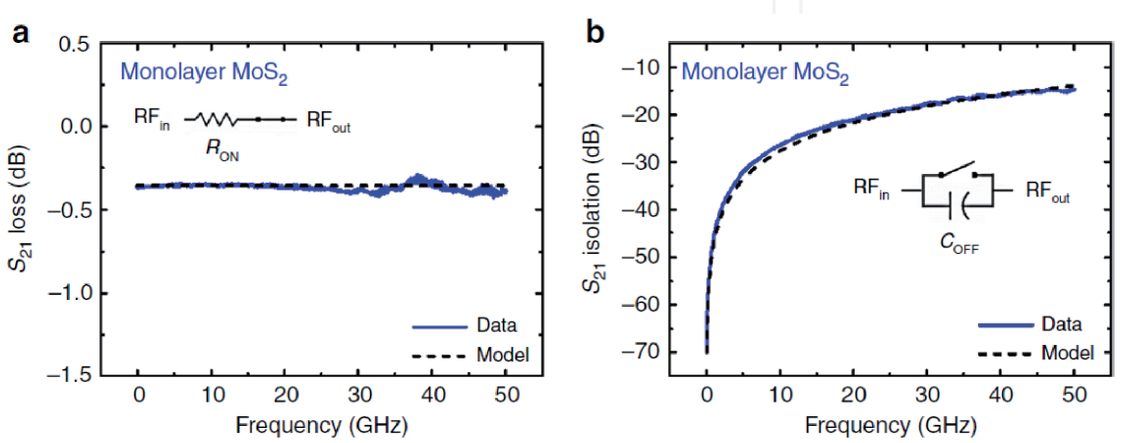

Figure 12.
Radio-frequency characterization of the MoS_2 RF switch: (a) insertion loss and (b) isolation.

Reference	Active layer materials	Active layer thickness	Forming voltage	Switching voltage	Retention time (hrs)	Endurance	On/ Off ratio	Switching speed (ns)
2D "Atomristors"	12 different 2D materials	0.3 nm–6 nm	Forming-free	0.5–4 V	>336	>240 DC cycles	$10 \sim 10^7$	15
Lee et al., Adv. Funct. Mater. 2020	MoS_2 in planar structure	~0.65 nm	Forming-free	~30 V	>24	>250 DC cycles	$10^2 \sim 10^3$	10^6
Xu et al., Nano Lett., 2019.	2 L MoS_2	~1.3 nm	Mostly Forming-free	~0.14–0.22 V	>5	>20 DC cycles	~10	N/R
Shi et al., Nat. Electron., 2018	5-7 L / 15-18 L h-BN	>1.5 nm	>1.8 V	0.1–6 V	>1	>100 DC cycles	$10 \sim 10^8$	2×10^4
Wang et al., Nat. Electron., 2018.	$MoS_{2-x}O_x$	~ 40 nm	~2 V	~1 V	>28	$>10^7$ pulse cycles	$\sim 10^2$	100
Zhao et al., Adv. Mater., 2017.	BNO_x	0.9–2.3 nm	Forming-free	0.6 V–1.7 V	>4	>100 DC cycles	$10^2 \sim 10^3$	10^6
Hao et al., Adv. Funct. Mater., 2016.	Degraded black phosphorus	~10 nm	N/R	1–2 V	>28	N/R	$\sim 3x\ 10^5$	N/R

Table 1.
Comparison of atomristors with other representative works in 2D memory.

8. Conclusion

In summary, a universal memristive phenomenon has been observed in 2D materials. These 2D-based memristors exhibit low switching voltage (<1 V), large on/off ratio (>10^6), fast switching speed (<20 ns), and forming-free characteristics. A mechanism based on metal atoms/ions adsorption into intrinsic vacancies producing an atomic-level conductive-point effect, has been proposed and supported by first-principle calculations and STM measurements. Constant voltage stress has been applied on the 2D-based memristors at high resistance state (HRS), revealing an additional higher resistance state that has not been discovered in conventional metal-oxide devices. Current sweeping method unveils the details hidden in the commonly used voltage-sweep curves, in which the transition step number could be attributed to the number of defects/vacancies. These open up a new materials space that might advance diverse applications including high-density neuromorphic computing, non-volatile memory fabrics, and zero-power RF switches.

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Conflict of interest

The authors declare no conflict of interest.

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