THE HARDWARE IMPLEMENTATION OF THE MULTI-POSITION SIGNAL DIGITAL DEMODULATORS

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ABSTRACT
There are considered the capabilities of the hardware implementation of the digital demodulators when receiving the signals of various modulation formats. It is shown that the multi-position signal processing devices can be implemented by means of the on the relatively inexpensive field programmable gate arrays.

Keywords: workstation design, work measurement, ergonomics, decision support system

1. INTRODUCTION

The digital modulation signals (PSK, QAM, etc.) are widely used in radio communication systems (Feher, 1995; Sklar, 2001; Proakis and Salehi 2007). The application of modern equipment is focused on the digital implementation of phase detectors and demodulators. Hence, in the present paper, devices are introduced requiring performing only a minimum number of simple arithmetic operations over the signal period (Chernoyarov et al. 2015-2018). Yet, software implementation of the algorithms for processing high-frequency digital modulation signals in real time when it is carried out by means of the signal processors requires too significant computational costs. In view of this, the field programmable gate arrays (FPGAs) are considered as more appropriate tools for hardware processing of the high-frequency signals in terms of the specified algorithms. Below, the resources are analyzed that are required for the implementation of the demodulators by means of the FPGAs.

2. THE MAJOR PART

An urgent task in designing the digital demodulators is to estimate hardware resources needed for their FPGA-based implementation. The most resource-intensive receiving devices are the quadrature amplitude modulation (QAM) signal demodulator (Chernoyarov, Glushkov, Litvinenko, Litvinenko and Matveev 2018) and the non-coherent demodulator of the signals phase-shift keyed in toto (Glushkov, Litvinenko, Matveev, Chenoyarov and Kalashnikov 2016; Chernoyarov, Litvinenko, Glushkov, Matveev and Salnikova 2017).
Modern FPGAs (Andina, de la Torre Arnanz and Valdes 2017) provide greater opportunities for the implementation of the digital high-frequency signal demodulators, but in this case, however, there should be designed the processing units requiring minimal computational resources.
In common studies (Chernoyarov O.V. et al. 2015-2018), the basic fast digital algorithms for coherent and noncoherent signal processing are introduced. In Fig. 1, the block diagram of the noncoherent processing algorithm is shown.
The signal from the intermediate frequency section output of the receiver is fed to the input of the 8-to 16-bit analog-to-digital converter (ADC) operated by the clock generator (CG) with the frequency $f_Q = 4f_0$. Here f_0 is the band center of the signal that may have frequency of tens of megahertz. As a result, the four samples s_{1i}, s_{i1}, s_{i2}, s_{i3} are formed over each of the i-th signal period $T_0 = 1/f_0$ as shown in Fig. 2. They are stored in the multi-bit four-cell shifter (MS4), while in the subtractors SUB_0 and SUB_1 the differences are determined of the even and odd samples forming the quadrature processing channels of the signal.

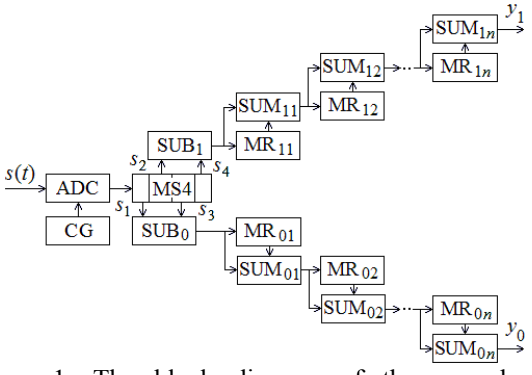


Figure 1: The block diagram of the noncoherent processing algorithm

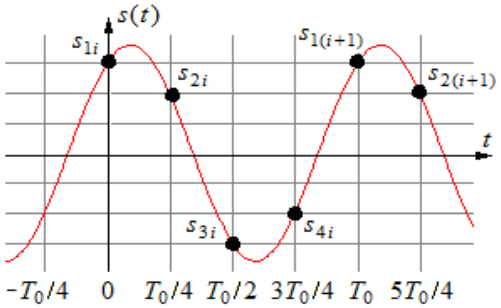


Figure 2: Time quantization diagram

The pairs of even and odd current and previous (stored into multi-bit shift registers MR_{01} and MR_{11}) differences of the samples are summarized in the summators SUM_{01} and SUM_{11}. Further, the obtained sums (two, then four, then eight, etc.) are accumulated in the subsequent summators, so that the responses of the quadrature channels are formed over the interval of the information signal duration $N = 2^n$ (where n is an integer) as follows

$$y_{0i} = \sum_{j=0}^{N-1}\left(s_{1(i-j)} - s_{3(i-j)}\right),\ y_{1i} = \sum_{j=0}^{N-1}\left(s_{2(i-j)} - s_{4(i-j)}\right).$$

The basic algorithms provide the minimum number $n = \log_2 N$ of the addition operations for accumulating the differences of the signal samples for the sample of the size N in each of the quadrature channels (Fig. 1). This also applies to the coherent algorithm (Glushkov, Litvinenko, Matveev, Chernoyarov and Salnikova 2015; Chernoyarov, Glushkov, Litvinenko, Litvinenko and Matveev B.V. 2017).

Based on these basic and coherent algorithms, various devices can be implemented for demodulating high-frequency phase-shift keyed (PSK) and differential phase-shift keyed (DPSK) radio signals.

In Fig. 3a, the block diagram is shown of the digital binary DPSK signal demodulator, while in Fig. 3b we can see the block diagram of the four-position DPSK signal demodulator (Chernoyarov, Glushkov, Litvinenko, Litvinenko and Matveev 2018).

In comparison with the basic algorithm (Fig. 1) in the demodulator circuit presented in Fig. 3a, there are supplemented the multi-bit N cell shifters $MR_{0(n+1)}$ and $MR_{1(n+1)}$, two additional summators and subtractors, two quadratic blocks (QT) performing the operations

$$z_{0i} = (y_{01i} + y_{0(i-N)})^2 + (y_{1i} + y_{1(i-N)})^2,$$
$$z_{1i} = (y_{01i} - y_{0(i-N)})^2 + (y_{1i} - y_{1(i-N)})^2,$$

as well as the substractor (SUB) and the comparator (C) forming the information symbol S_I.

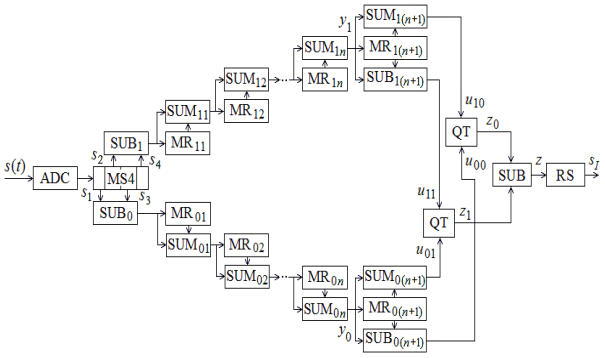
Similarly, into the four-position DPSK signal demodulator (Fig. 3b), the basic algorithm is supplemented by the computing unit (CU) that performs the operations

$$z_0 = y_{0,i}y_{0,(i-N)} + y_{1,i}y_{1,(i-N)} + y_{1,i}y_{0,(i-N)} - y_{0,i}y_{1,(i-N)},$$
$$z_1 = y_{0,i}y_{0,(i-N)} + y_{1,i}y_{1,(i-N)} - y_{1,i}y_{0,(i-N)} + y_{0,i}y_{1,(i-N)},$$

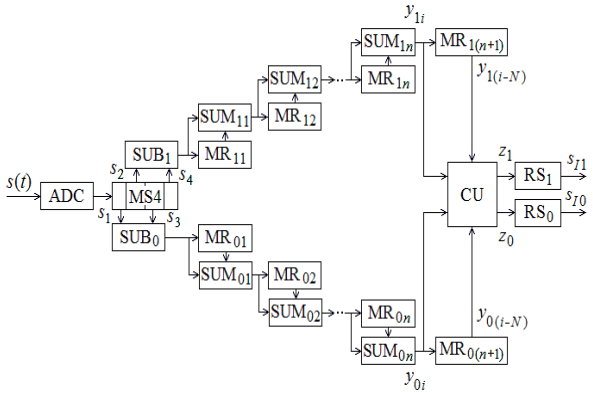
as well as the two comparators C_1 and C_2 at the outputs of which the symbols S_{I0} and S_{I1} are generated. The block diagrams of the coherent PSK and DPSK signal demodulators are much simpler than those shown in Fig. 3.

Thus, the basic digital algorithm allows us to implement various PSK signal demodulators at relatively low computational costs.

In Fig. 4a, the block diagram is shown of a more complex coherent quadrature amplitude modulation (QAM) signal demodulator (Chernoyarov, Glushkov, Litvinenko, Litvinenko and Matveev B.V. 2018). Here the responses of the quadrature channels (2) and (3) are passed to the threshold devices TD_0 and TD_1 as well as to the normalizing and synchronizing device (NSD) providing clock synchronization and the formation of the thresholds for TDs. According to the output TDs signals, in the resolver (RS) the code words are separated by which the binary code of the received multi-position symbol is formed in the decoder (DC).



a)



b)

Figure 3: The block diagrams of the fast digital algorithms for noncoherent demodulation of binary (a) and four-position (b) DPSK signals

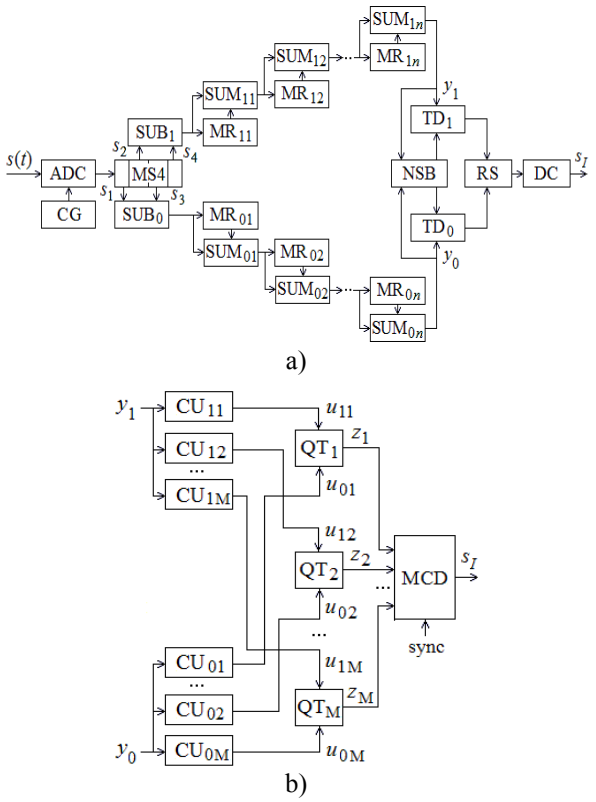


Figure 4: The block diagrams of the fast digital algorithms for noncoherent demodulation of binary (a) and four-position (b) DPSK signals

The digital demodulator of the signals phase-shift keyed in toto (Glushkov, Litvinenko, Matveev, Chenoyarov and Kalashnikov 2016; Chernoyarov, Litvinenko, Glushkov, Matveev and Salnikova 2017) requires the greatest computational cost. The block diagram of its addition to the basic algorithm (Fig. 1) is shown in Fig. 4b.

The values y_{0i}, y_{1i} are moved to the computing units CU_0 and CU_1 generating the responses u_{0m} and u_{1m} to the m-th code combination of K elements length, where $m = \overline{1,M}$ and M is the number of these code words. For the i-th signal period, at the CUs outputs we get

$$u_{0im} = \sum_{k=0}^{K-1} a_{mk} y_{0(i-kN)}, \qquad u_{1im} = \sum_{k=0}^{K-1} a_{mk} y_{1(i-kN)},$$

where $a_{mk} = \pm 1$ is the elements of the m-th code word. By the transformation

$$z_{im} = \sqrt{u_{0im}^2 + u_{1im}^2}.$$

the demodulator responses are generated for each enabled code combination, and by the largest of these responses a decision on the received code combination S_I is made by the maximum choice device (MCD).

To estimate the possibilities of designing the specified demodulators, FPGAs of various modifications have been considered produced by Xilinx (Xilinx DS160 Spartan-6 family overview 2011; 7 Series FPGAs data sheet: Overview 2018) and Altera (Parab J.S., Gad R.S. and Naik G.M. 2018). The selection criteria are the required hardware resources and the cost.

The results of the FPGA resource estimation for implementing the digital binary DPSK signal demodulator (Fig. 3a) are shown in Table 1, for the case when the ADC width is 8 bits and N=128. As we can see, a relatively simple demodulation algorithm does not require significant computational power.

In order to implement the demodulator of the signals phase-shift keyed in toto and coded by Walsh sequences (Chernoyarov, Litvinenko, Glushkov, Matveev and Salnikova 2017), FPGAs are used produced by the Xilinx, such as XilinxXC6SL25 (Spartan-6), XC7K70T (Kintex-7), XC7A100T (Artix-7). As an example, for each FPGA, an HDL code has been synthesized and implemented with the fixed parameters: the Walsh code sequence length is M = 4, the number of carrier periods is N = 64, the ADC bus width is R = 12. It is established that for the FPGA XC6SL25 the maximum possible carrier signal frequency is 144 MHz, while for the XC7A100T it is 118 MHz and for the XC7K70T – 154 MHz. The power consumption at the signal frequency of 50 MHz lies within the range from 40 to 90 mW. In Table 2, the results are presented of a quantitative estimation (as percentage of the total) of the required hardware FPGA resources.

In Table 3, the similar results are shown produced while implementing the demodulator of the two signals phase shift keyed in toto and coded by M-sequences of K elements length.

As it can be seen, there can be successfully implemented FPGA-based demodulators of the signals with the different digital modulation formats in toto.

Table 1: The estimation of the hardware overhead (per cent) of FPGAs produced by Xilinx for implementing the digital binary DPSK signal demodulator

Elements	Spartan 6	Virtex 5	Kintex 7
Flip Flops	5	<1%	<1%
LUTs	35	2%	<1%
Slices	50	3%	<1%
DSP	25	6%	<1%

Table 2: The estimation of the hardware overhead (per cent) of FPGAs produced by Xilinx for implementing the digital demodulator of the signals phase-shift keyed in toto and coded by Walsh sequences

FPGA	Elements		
	XC6SL25	XC7K70T	XC7A100T
Slice Registers	2.55	0.93	0.6
SliceLUTs	14.26	7.05	4.56
DSP	21.05	3.33	3.33

Table 3: The estimation of the hardware overhead (per cent) of FPGAs produced by Xilinx for implementing the digital demodulator of the signals phase-shift keyed in toto and coded by *M*-sequences

FPGA	Elements			
	K	XC6SL25	XC7K70T	XC7A100T
Slice Regis-ters	15	4.5	1.8	1
	31	6.6	2.5	1.6
	63	12.8	4.4	2.7
Slice LUTs	15	23	8	6
	31	39	13	9
	63	68	26	17

The possibilities of implementing the four-position QAM signal demodulator are considered in relation to Cyclone FPGAs produced by Altera. The results of the hardware cost analysis are shown in Table 4.

Table 4: The estimation of the hardware overhead (per cent) of FPGAs produced by Altera for implementing the digital QAM signal demodulator

FPGA	Elements		
	Cyclone IV E EP4CE22F17 C6	Cyclone V 5CSEBA6 U23I7DK	Cyclone 10 LP 10CL120YF780 C8G
Slice Registers	867/22320 (3.88%)	763/41910 (1.82%)	763/86800 (1.06%)
Slice LUTs	5274/12064 (43.26%)	2891/22000 (13.14%)	2891/42400 (6.81%)
DSP	4/16 (25%)	8/120 (6.66%)	8/260 (30.07%)

3. CONCLUSION

From the analysis of the obtained results, one can conclude that even relatively inexpensive modern FPGAs allow us to implement various devices for demodulating the digital keyed signals while providing rather acceptable, if not promising, technical features. Unused FPGA resources can be applied to solving other technical tasks by the same equipment.

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