International Journal of Thin Film Science and Technology

Volume 5
Issue 2 *May 2016*

Article 3

2016

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http://dx.doi.org/10.18576/ijtfst/050203

The Effect of Air-Exposed Layer on Electrical Properties of Cu/n-Si/Al Schottky Diodes

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Received: 30 Dec. 2015, Revised: 8 Mar. 2016, Accepted: 9 Mar. 2016.
Published online: 1 May 2016.

Abstract: In this work, we studied the effect of air-exposed layer on the current-voltage (I-V) capacitance versus voltage (C-V) and capacitance versus frequency (C-f) characteristics of Cu/n-Si/Al Schottky diodes. We fabricated with and without thin oxide layer Cu/n-Si/Al diodes. Firstly, n-Si wafer having (100) oriented and 15 Ω.cm resistivity was cut into eight pieces labeled Diode 1 (D1) to Diode 8 (D8). We formed the referents Cu/n-Si/Al Schottky diode (D1) which has not exposed to air. Rest of the samples, before formation of Schottky contact, was exposed to clean air at the room temperature for 2, 4, 8, 16, 32, 48 and 64 days. Therefore, Schottky contact with native oxide layer on the polished n-Si surface was obtained. From *ln*(I)-V plot of the Cu/n-Si/Al diodes, ideality factor (n), barrier height ($e\Phi_b$), the interface state density of the Schottky junctions (N_{ss}), saturation current (I_0) and series resistance (R_S) were calculated. In addition, same parameters were verified using both Cheung functions and C^{-2}-V characteristics. Moreover, the interface state densities of the Schottky junctions versus energy N_{ss}-(E_c-E_s) also was calculated and plotted. What causes to excess capacity of the space charge have also been investigated. While the value of ideality factor and series resistance increased with increasing exposure time to air, the barrier height $e\Phi_B$ value of the Schottky diode with oxide layer is smaller than those without oxide layer. This is attributed to formation oxide layer occurring between interfaces of metal and semiconductor surface.

Keywords: Exposure to air, Schottky barrier diodes, series resistance.

1 Introduction

The Metal Semiconductor contact (Schottky Diodes) in the semiconductor device technology has attracted much attention during the recent years [1-9]. It is well known that the ideality, reliability and stability of Schottky diodes are affected by interface properties and these qualities are important to the electronic devices [10]. During the fabrication process, unless specially processing, some degree of oxidation generate a thin interface oxide layer between the metal and the semiconductor [9]. In the laboratory environment, organic contamination and native oxide layer occurred on the semiconductor crystal and metal surface [11,12].

In many cases, barrier height of Schottky indicates the presence of the interfacial layer whose thickness depends on exposure time of semiconductor surface in the chemically cleaned substrates and determines the main feature of a diode [1, 3, 12-15]. It is well known fact that the semiconductor surfaces are easily oxidized when left in air for extended time [11, 12]. The existence of insulating layer converts the metal-semiconductor (MS) devices into metal-insulator-semiconductor (MIS) devices and it has a strong effect on the electrical parameter of diode [12,13]. Kumar *et al.* compared MS diode with MIS diode and concluded that the native oxide layer at Schottky rectifying contact plays an important role in the electrical parameters of device [13]. Çetiner *et al.* observed that the non ideal forward bias I-V behavior in the Au/n-GaAs Schottky diode were attributed to a change in the MS barrier height due to the interface states and interfacial layer [10]. İlbilge study the effect thermal growth oxide layer on the Al/p-Si Schottky diode and concluded that the behavior n and R_s value of Schottky diodes with oxide layer are higher than those of the Schottky diode without oxide layer while the $e\Phi_B$ value of the Schottky diode with oxit layer is smaller than those of the diode without oxide layer [10]. Ha *et al.* suggested that the simple post-oxidation processes suitable for fabrication of high-voltage GaN devices [15]. Kılıçoğlu *et al.* concluded that the values ideality factor (n) and series resistance (R_s) value and interface state density with oxide layer have been found to be higher values than sample without oxide layer [16]. Çetin and Ayyıldız obtained that oxide thicknesses and atomic concentration of oxygen quantity on the surface increased with increasing exposure time to air [17]. When the contact formed on the oxidized surface, air grown oxide did not cause the higher barrier height for Cu/n-InP contacts [17]. Çetinkara and Güder obtained that n and $e\Phi_B$ value of the air exposed Pb/p-Si Schottky diode have reached to saturation after ten days and this result can be interpreted as a saturation of the oxide

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layer thickness [11]. Özdemir *et al.* obtained that Φ_B value for interfacial layer decreased by increasing the exposure time of Au/n-GaAs Schottky diodes [5]. The values of the $e\Phi_B$ of Au/n-GaAs Schottky diodes were decreased by increasing the exposure time up to ten days. After ten days the barrier height values remains stable up to 45 days [5].

In this study, we aim to shown the effect exposure to time on the electrical characteristics of Cu/n-Si Schottky diodes.

2 Experimental procedure

In this work, we use n-Si wafers with (100) orientation, 350 μm thickness and ρ=15 Ω.cm resistivity. The samples were chemically cleaned to get rid of chemical and organic contaminations [12-18]. For this reason, sample was boiled in 10 minutes with RCA1 ($NH_4H+H_2O_2+6H_2O$) and then in ten minutes with RCA2 ($HCl+ H_2O_2+6H_2O$) Then it was etched in HF:H_2O (1:10) for 30 second and rinsed in deionised water by ultrasonic vibration [10-17]. After the cleaning progress, the n-Si wafer was cut into eight pieces. The ohmic contact at back side of samples was made by evaporating Al [19, 20] at the 10^{-6} torr pressure and heated 420 ^oC for 5 min in flowing N_2 atmosphere [10, 21]. One of the samples was immediately placed into the evaporation chamber and then rectifying contact on the front side of sample was made by evaporating cleaned Cu at the 10^{-6} torr pressure [12-17]. Thus, we made the referents Cu/n-Si/Al Schottky diode and we labeled this sample Diode 1 (D1). Reaming sample, before making Schottky contact formation, were exposed to clean air at the room temperature (300 ^oK) for 2, 4, 8, 16, 32, 48 and 64 days to obtain the samples with the native oxide layer on the polished n-Si surface [12, 17]. Then thus diodes inserted into the evaporation chamber to evaporate cleaned Cu at the 10^{-6} torr pressure on the front side to form rectifying contact. We labeled these samples as a (D2), (D3) etc...

In this study, for fabrication purpose of Cu/n-Si/Al Schottky diodes "Edwards Auto 306 Vacuum Coating Chamber With Turbo Moleculer Pumping System" device was used, for I-V measurements of diodes 'Keithley 6487 Picoammeter Voltage Source' device was used. I-V measurements were plotted as *ln(*I)-V. From *ln*(I)-V plot of the Cu/n-Si diode, we extracted the Cheung function and we obtained the interface state densities of the Schottky junctions (N_{ss}), saturation current (I_0). Using Cheung function, ideality factor (*n*), barrier height ($e\Phi_B$), and serial resistances (R_S) were calculated [12, 22].

For C-V and C-f measurements of diodes 'Agilent 4294A 40 Hz-110 MHz Precision Impedance Analiyzer" device was used. C-V measurements were performed at the room temperature (300 ^oK) for 1MHz frequency. We were plotted C-V characteristics. Using C-V plots, we plotted C^{-2}-V graph [5,10]. The C-f characteristics of Cu/n-Si/Al diodes have been studied. C-f measurements was done for 0,3 V. The excess capacity was observed at low frequencies [10].

The distribution of interface state (N_{ss}) of the Schottky junctions were determined from *ln*(I)-V characteristic [24]. We plotted the distribution of interface state according to the energy distribution [N_{ss}-(E_c-E_s)] [5,12, 13]

3 Result and Discussion

According to thermionic emission theory, Forward bias current equation for non-ideal condition can be expressed [1-13] as

$$I = I_0\left[\exp\left(\frac{eV}{nkT}\right)-1\right] \quad (1)$$

Where

$$I_0 = AR_n^{*}T^2\exp\left(-\frac{e\varphi_B}{kT}\right) \quad (2)$$

n is ideality factor, *V* is forward bias voltage, *k* is the Boltzmann constant, *T* is temperature in Kelvin, I_0 is the saturation current density, R_n^* is the Richardson constant (112 A/ cm^2 K^2 for n-type Si) [7, 18], *A* is the effective diode area (diameter is 0.8 mm), *e* is the electron charge and $e\Phi_B$ is the effective barrier height.

The *n* ideality factor is determined from slope of the linear region of the forward bias in *ln*(I)-V characteristic through the relation [15-22]

$$n = \frac{e}{kT}\frac{dV}{d(\ln I)} \quad (3)$$

Figure 1 represents the forward bias current–voltage characteristics of the Cu/n-Si/Al diodes. For ideal diode, ideality factor (*n)* equals to 1. However, ideality factor (*n*) in experiment can be greater than unity [23-29]. The values ideality factor (*n*), barrier height ($e\Phi_B$) were obtained from the *ln*(I)-V graphs [9,10]. The values of ideality factor depending on sample are changed in the range of 1.17 to 2.18. The high values of the ideality factor imply that native oxide layer occurs on interfacial layers between metal and semiconductor [14-16].

To obtain barrier height, equation (2) is rearranged and I_0 values are obtained from *lnI*-V characteristics of the diode at V=0 [14, 28,].

$$e\varphi_B = kT\ln\left(AR*T^2/I_0\right) \quad (4)$$

After inserting values of saturation current density in equation (4), the barrier height of diode can be calculated [17]. The barrier height of reference diode was obtained as 0.77 eV. Depending on how many days sample was exposure to air, the values of barrier height decreased in the range of 0.77 to 0.62 eV. All values were inserted in *Table* 1.

Distribution interface states (N_s) of junction can calculate as follows [14,18].

$$N_{ss} = \frac{1}{e}\left[\frac{\varepsilon_i}{\delta}\left(n(V)-1\right)-\frac{\varepsilon_s}{W}\right] \quad (5)$$

where ε_s is the permittivity of the semiconductor ($3.8\varepsilon_o$), ε_i is the permittivity of the interfacial layer space ($11.8\varepsilon_o$), ε_o is the permittivity of free space, W is the space charge width (5672 Å), δ is the thickness of the interfacial oxide layer δ can calculated from C-V plot using Eq. $C= \varepsilon_i\, \varepsilon_o A/\delta$ as 7 Å for reference diode and 27 Å for others diodes [19]. E_s is the energy with respect to the bottom of the conduction band at the surface of the semiconductor [12]. Ideality factor (n) can be calculated from equation (1) as follows

$$n(V) = \frac{eV}{kT}\left[\ln\left(\frac{I}{I_o}\right)\right]^{-1} \quad (6)$$

In an n-type semiconductor, the energy of the interface states with respect to bottom of the conduction band at the surface of the semiconductor, E_s, is given by [12,13]

$$E_c - E_s = e\varphi_b - eV \quad (7)$$

After inserting these values in equation (7), we calculate donor density, *Nss*.

It is well known fact that downward concave curvature of the forward bias current–voltage (*ln*I-V) plots as sufficiently large voltages is caused by the presence of the effect of R_s, apart from interface states. If the series resistance is low, the non-lineer region will be narrow. The values of R_s were calculated using method developed by Cheung [23]. According to Cheung, the forward bias can be expressed as follows [23].

$$I = I_0\left[\exp\left(\frac{e(V-IR_s)}{nkT}\right)\right], \quad (8)$$

Where IR_s is the voltage drop at the series resistance of the device. The values of the series resistance can be determined from following equations [23].

$$\frac{dV}{d(\ln I)} = \frac{nkT}{e} + IR_s \quad (9)$$

From equation (9), it is seen that the plot of ($\frac{dV}{d(lnI)}$ -I) will be linear and the slopes of ($\frac{dV}{d(lnI)}$ -I) give R_s. *Figure 2a* and *2b* show the plot of ($\frac{dV}{d(lnI)}$ -I) of Cu/n-Si/Al Schottky diodes. From *figures* 2a and 2b, the values of nkT/e is obtained at I=0 [9,13]. The slope of this graph line gives series resistant (R_s) and all values of R_s are shown in *Table* 1.

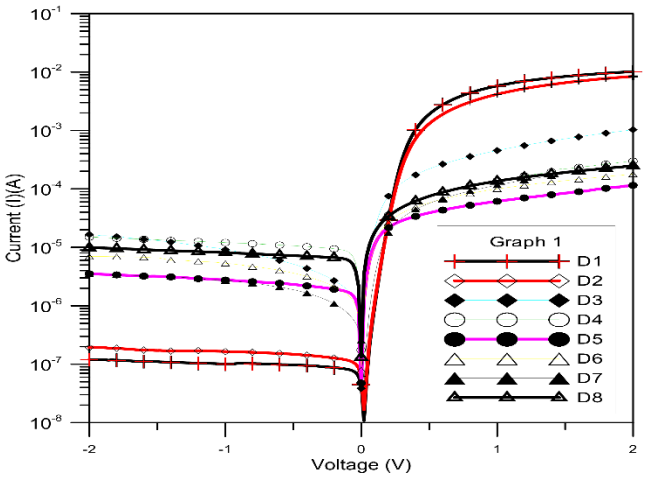


Figure 1: The forward and reverse bias current-voltage (lnI-V) characteristics of Cu/n-Si/Al Schottky diodes.

Table 1: The experimental values of parameters of Cu/n-Si/Al Schottky diodes.

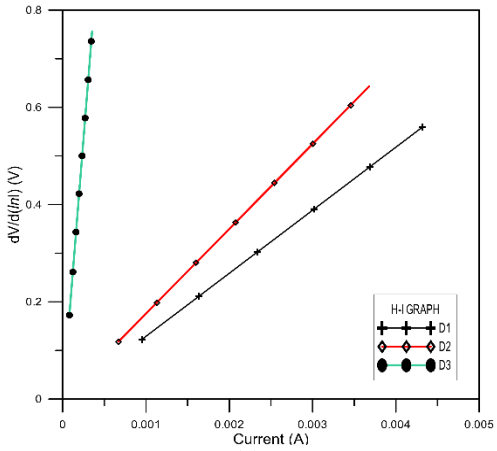
Air exposure (Days)	Samples	Ideality Factor	Barrier Height (eV)	Saturation Current (A)	Series Resistant (Ω)
Reference diode	D1	1.17	0.77	$5.75*10^{-7}$	176
2 day	D2	1.21	0.73	$8.23*10^{-8}$	1985
4 day	D3	1.34	0.66	$1.37*10^{-6}$	6164
8 day	D4	1.44	0.64	$3.37*10^{-7}$	6641
16 day	D5	1.51	0.65	$7.27*10^{-7}$	9860
32 day	D6	1.62	0.65	$7.44*10^{-6}$	8152
48 day	D7	1.87	0.62	$7.65*10^{-6}$	9645
64 day	D8	2.18	0.62	$2.18*10^{-6}$	7742

It is seen from Table1, the value of ideality factor and series resistance increased with increasing exposure to time to air, while the value of barrier height and density value of interface states decreased. After 16 day, the variation of values of ideality factor, series resistance and barrier height slowly change. This indicates that oxide layer reached saturation values after 16 days [21].

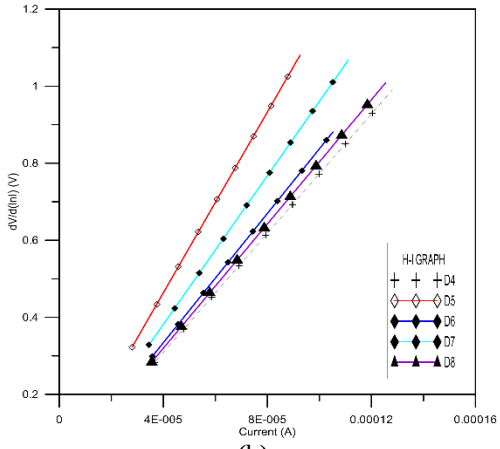
In *Figure 3*, ideality factor versus exposure time (n-day) and barrier height versus exposure to time [($e\phi_B$)-day] were plotted. It can be seen that the value of ideality factor and series resistance increased with increasing exposure time to air. Moreover, the barrier height ($e\phi_B$) value of the Schottky diodes with oxide layer is smaller than those of the diode without oxide layer. This result is in good agreement with literature [17, 27].

C-V measurements of Cu/n-Si/Al diodes were carried out for 4 MHz frequencies at room temperature at dark, and presented in *Figure 4.* As seen from figure, when diode has higher series resistance values, the peak values of capacitance get smaller values. We saw that capacity peak

was lower for diodes with high resistivity compared to the diodes with low resistivity [1,9].



(a)



(b)

Figure 2a: Cheung function plot ($\frac{dV}{d(lnI)}$ -*I)* of (D1-D3) and **Figure** 2**b** Plot ($\frac{dV}{d(lnI)}$ -*I)* of (D4-D8) of the Cu/n-Si/Al Schottky diodes.

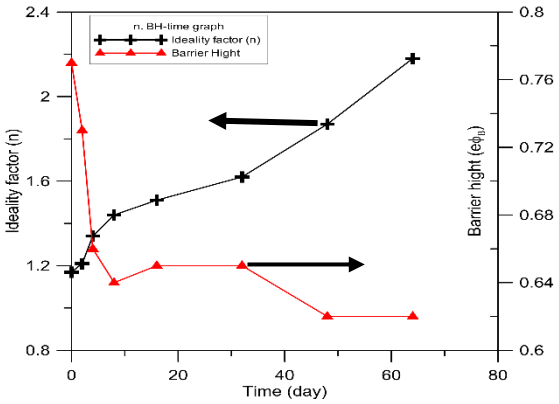


Figure 3: Ideality factor vs. exposure to time and barrier height vs. exposure to time.

In Schottky diode, the depletion layer capacitance is given as [24]

$$\frac{1}{C^2} = \frac{2(V + V_0)}{e\varepsilon_s\varepsilon_0 N_S A^2} \qquad (11)$$

Where A is diode effective area, V is the applied bias voltage, (V_0) is the diffusion potential at zero bias determined from extrapolation of the liner C^{-2}-V plot on the V-axis [27]. C^{-2}-V characteristics plots of diode were plotted at 1 MHz and shown in *Figure 5*. V_0, diffusion potential which is obtained from interception of $\mathbf{C^{-2}}$-V graph with horizontal axis, ideality factor (n) and barrier height ($e\Phi_B$) can be checked from $\mathbf{C^{-2}}$-V graph [29-32, 33].

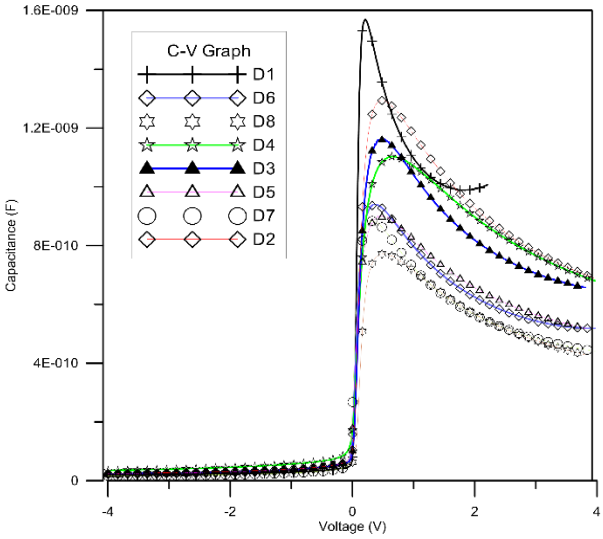


Figure 4: Current-Voltage (C-V) characteristics of The Cu/n-Si/Al Schottky diodes.

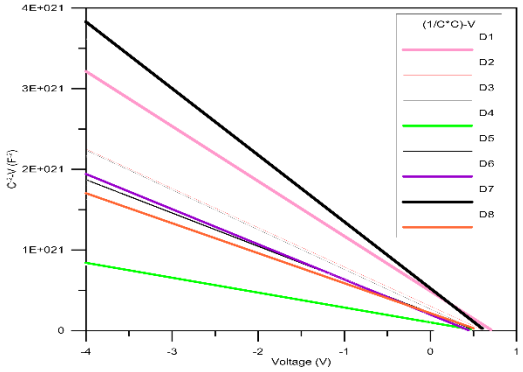


Figure 5: *Plot C^{-2}-V obtained from C-V characteristics of the Cu/n-Si/Al Schottky diodes.*

C- f measurement of the device was taken at 0.15 V and shown in *Figure 6*. From this it is seen that excess capacity was observed for every diodes at low frequencies. We saw that excess capacity was lower for diodes with high resistivity compared to the diodes with low resistivity. For all voltage values, excess capacity gets smaller values with higher frequencies and it equals to depletion region capacity at some point [9]. In literature, the reason of excess capacity at high frequencies is explained either the charges at the interface state cannot follow the alternative current signal [24] or is explained with quality of the back-ohmic contact to the bulk semiconductor substrate [9]. It was explained that excess capacity is low for diodes with perfect ohmic contact.

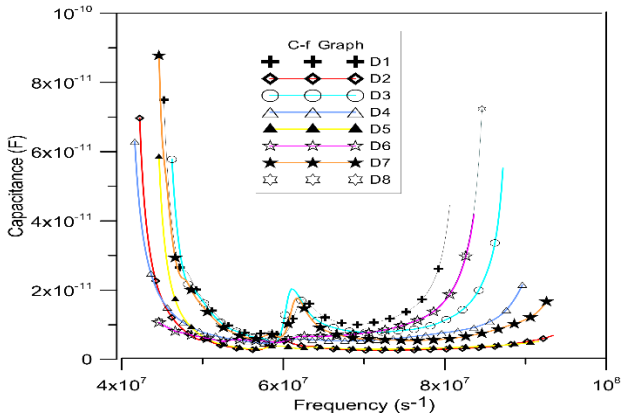


Figure 6: Plot Capacitance-frequency (C-f) characteristics of the Cu/n-Si/Al Schottky diodes.

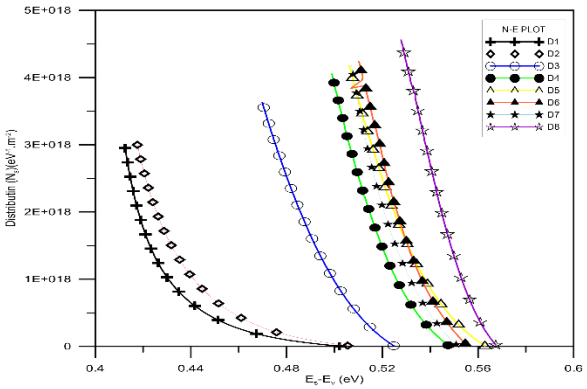


Figure 7: Plot Interface state distribution characteristics of the Cu/n-Si/Al Schottky diodes.

We show in *Figure 7*, the density value of interface states for D1 sample is lower than the samples with native oxide layer. The high values of density of interface states can be related to the existence of a thin oxide layer [23, 28]. Our experiment density values of interface states related the Cu/n-Si/Al diodes are in agreement with literature [5, 12, 18].

4 Conclusion

We performed current-voltage, capacitance-voltage and capacitance-frequency measurement to characterize the effect of native oxide layer on interfacial layer between metal and semiconductor of Cu/n-Si/Al diodes. We showed that behavior ideality factor (n) and series resistivity (R_s) value of Schottky diode with oxide layer are higher than those of the Schottky diode without oxide layer while the barrier height ($e\phi_B$) value of the Schottky diode with oxide layer is smaller than those of the diode without oxide layer. This result is agreement with as given by literature [18-29]. For Cu/n-Si/Al diode, it is seen that average values peaks with higher series resistance diodes shift to smaller values of peaks.

Excess capacity is measured for every diode at low frequencies. From C-f plot, the excess capacity is higher for diode with high resistance values than diode with lower resistance values.

The density values of interface states of the sample without the native oxide layer are smaller than the sample with native oxide layer. These results for the density value of interface states related the Cu/n-Si/Al diodes are in good agreement with literature [5,23, 28].

It is concluded that the native oxide layer has significant effect on electrical properties of Schotky diodes. The value of ideality factor and series resistance increased with increasing exposure to time to air, while the value of barrier height and density value of interface states decreased. These variations attributed to formation oxide layer on the Si crystal surface.

Acknowledgments

This work was supported by the Scientific Research Projects Unit of Yuzuncu Yil Univesity-VAN through Project No: 2014-FBE-D008.

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