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A Two-Dimensional (2D) Analytical Model for Sub-threshold Current and Sub-threshold Swing for Short Channel Triple Material Gate-Double Halo (TMG-DH) DG MOSFET

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Abstract: In this work, an analytical model for sub-threshold conduction parameters has been demonstrated for short-channel Triple Material Gate-Double Halo (TMG-DH) DG MOSFET. For sub-threshold current and sub-threshold swing models, we have utilized drift-diffusion current density equation with virtual cathode concept of DG MOSFETs. The influence of double halo technique over gate length ratio of the three channel regions under three dissimilar gate materials of the device has been investigated in depth in terms of sub-threshold current and sub-threshold swing. Also, the reliance of sub-threshold current and sub-threshold swing on different device constraints has been scrutinized. Furthermore, the problem solving capability of (TMG-DH) DG MOS device over short channel effect (SCE) has been emphasized. Using ATLAS^{TM} Silvaco tool, verification of theoretical results has been performed with respect to the proposed model.
Keywords: Triple Material Gate-Double Halo (TMG-DH) DG MOSFET, halo doping, short channel effect, sub-threshold current and sub-threshold swing.

1 Introduction

This modern era entails small sized, high speed, low power and low cost semiconductor devices. In 1965, pioneer of Intel Organization, Gordon E. Moore observed that the amount of transistors placed in an integrated circuit (ICs) would be twice over every two years. Afterwards, this law has been acknowledged as Moore's law [1]. This law is concerned to be factual even nowadays, but it is not successful to sustain perpetually, because scaling down of semiconductor ICs will soon come to an end. Scaling of complementary metal oxide semiconductor (CMOS) technology based devices beyond 100 nm leads to severe problems, such as hot carrier effect and short channel effect. Furthermore, the International Technology Roadmap for Semiconductors (ITRS) has stated that it would be a tough task to construct CMOS technology beyond 22 nm of channel length [2].

This challenge has motivated strenuous exploration for another course of action to conventional planar silicon transistors. Therefore, the subsequent generation devices will be almost dependent upon non-planar device arrangements such as dual-gate (DG) MOSFETs [3-5]. DG MOSFET's features, such as superior scalability, superior short-channel effect (SCE) quelling, abridged leakage current, enriched drive current and trans-conductance surpass those of conventionally designed MOSFETs [6]. Owing to such overpowering features, DG-MOSFETs have a great potential to be scaled down beyond the limits provided by ITRS roadmap [2]. Even though circuit performance of DG-MOSFET can be amended with scaling technique assistance, but it gives rise to reliability degradation and some leakage current [7]. To overcome such problems, and to upsurge the device rapidity and drain current with lessened short channel effects (SCEs) [8], novel device structures have to be incorporated to enrich the behavior of traditional DG MOSFETs. In this circumstance, several solutions involving various kinds of material and structural correction have been suggested [9-13]. Among numerous proposed techniques, channel engineering techniques such as, single-halo (SH) or lateral asymmetric channel (LAC) and double-halo (DH), are the protuberant ones [14-17]. SH or LAC channel engineering technique demonstrates significant suppression of SCEs.

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Also, some literatures have demonstrated the performance of LAC with their appropriate application in both digital and mixed signals [6, 17]. This technique embroils high doping at the proximity of source area and light doping close to the drain region. High doping close to the source region lessens the depletion thickness that results in the curtailed sub-threshold leakage current and improves output impedance. In addition, this technique resolves the problem of DIBL effect. Halo doping elevates the average channel doping concentration, and so increases the device operation factors, i.e. g_m/I_d, output resistance and intrinsic gain in sub-threshold region [18-19]. Thus, halo doping positive impact on device performance enabled it as the main channel engineering tool. In addition, in saturation region, halo doping leads to superior driving current and has a significantly improved threshold voltage when paralleled with uniformly doped device [19].

Moreover, to suppress the problem of hot carrier effect (HCE) generated by high electric field, gate engineering method can be implemented. This process involves replacement of gate metal by cascading different metals of different work-function that forms contacts. The greater work-function material is located on oxide layer near the source end and smaller work-function material is located for the same near the drain end. Due to the formation of contacts, step shaped potential gets induced. Hence, electric field spikes exist in the region of channel. This whole process recovers the SCE, carrier transit period and device driving ability. For further extension in gate engineering, straddle gate comprising three different materials was introduced [20]. Since side gate has lower threshold voltage than main gate, straddle technique results in abridged leakage current between source and drain.

With such motivation of straddle gate device, tri-material-gate-stack (TRIMAGS) MOSFET was further implemented in addition with the 2-dimensional analytical modelling of threshold voltage and channel potential [10]. In extension to this work, Chiang et al. [21] gave 2-dimensional model for sub-threshold current to scrutinize dispersal of potential in the channel using Poisson's equation. Moreover, by accounting a service of ATLAS™ simulation tool, Razavi et al. demonstrated the advantages of tri-material-double-gate (TM-DG) MOSFET over (DM-DG) MOSFET and DG-MOSFETs [7]. Analytical modelling of threshold voltage, sub-threshold current and sub-threshold swing for (TM-DG) MOSFET was further reported by Tiwari et al. and A. Tsormpatzoglou et al. [20, 22].

Although, several papers addressed with MOSFET gate and channel engineering technique, no paper has handled the analytical modeling of the essential parameters of MOSFETs incorporating both channel and gate engineering technique. Therefore, we have reported the channel potential and threshold voltage compact modelling for Triple-Material Gate-Double-Halo (TMG-DH) DG MOSFET structure in our previous work [23]. Moreover, with an extension to our aforementioned literature, this paper has introduced the compact and simple analytical model for sub-threshold current and sub-threshold swing of Triple-Material-Gate-Double-Halo (TMG-DH) DG MOSFET structure. In this way, switching behavior of MOSFETs can be analyzed in a better manner. All the theoretical results are verified by comparing them with simulation results attained from ATLAS™ SILVACO simulation tool.

2 Device Details

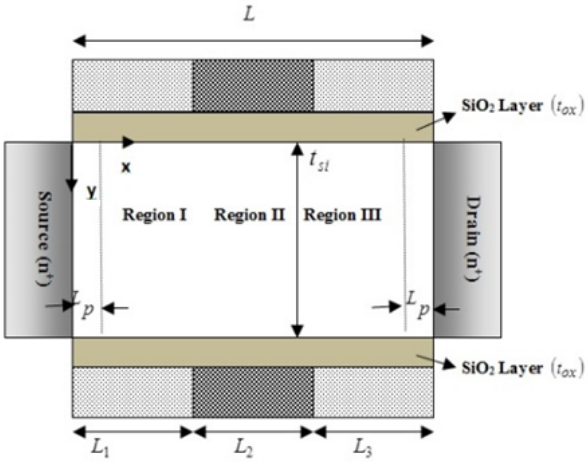

Fig. 1: Schematic of (TMG-DH) DG MOSFET, where L ($L = L_1 + L_2 + L_3$), t_{si}, t_{ox} and L_p are gate length in region I, region II, and region III; thickness of silicon channel; thickness of gate oxide and pocket length, respectively.

(TMG-DH) DG MOSFET device schematic under study is depicted in Figure 1, where length of gate is denoted by $L(L = L_1 + L_2 + L_3)$, gate oxide width is represented as t_{ox}, and t_{si} is represented as thickness of channel. Length of channel is considered along the x-direction and thickness of channel is considered along y-direction. (TMG-DH) DG MOSFET front and back gate electrodes are divided into three different sections having lengths L_1, L_2 and L_3 with work-function ϕ_{m1}, ϕ_{m2} and ϕ_{m3}, respectively ($\phi_{m1} > \phi_{m2} > \phi_{m3}$). In this work, the gate section is considered to be made up of material tungsten di-silicide (WSi_2), having the highest work-function ϕ_{m1} located near the source side. It works as control gate of the device under consideration. The gate section made up of material $Hf_{0.27}Ta_{0.58}N_{0.15}$, having intermediate work-function ϕ_{m2} is located in the middle and termed as the first screen gate. The gate section made up of material $Hf_{0.40}Ta_{0.46}N_{0.14}$, having the lowest work-function ϕ_{m3} is located near the drain side and termed as the second screen gate. All the three sections of gate are tied up together to operate device by giving the same external gate to source supply voltage (V_{GS}). At source and drain end pocket, implantation is done and termed as halo doped regions denoted by length L_p. These halo regions are heavily doped with doping concentration N_{pp} more than

other regions doped with doping concentration N_a. Therefore, channel region effective doping profile can be represented by N_{eff} given in Eq. (1) [24].

$$N_{eff} = N_a + \frac{L_P}{L}\left(N_{PP} - N_a\right) \tag{1}$$

where L is the length of gate and L_P is the pocket length.

3 Model Derivation

3.1 Subthreshold current modeling

For the analytical modeling of sub-threshold current, we have used the drift-diffusion equation with virtual cathode concept. Virtual cathode is defined as the smallest potential point in the direction of channel length. Consequently, virtual cathode plays an essential role for the purpose of device analytical modeling [20, 25-26]. At the point of virtual cathode, energy obstruction takes place. Subsequently, free electrons diffuse from the source and then are swept into the drain forming the subthreshold drain current [20, 25–26]. In our earlier work [23], virtual cathode potential ($\phi_{vc}(y)$) [20] for short channel (TMG-DH) DG MOSFET has been derived. Two-dimensional channel potential for the three sections of the channel was given as in Eq. (2) [23]-

$$\phi_n(x,y) = \left[M_n \exp(\eta x)+N_n \exp(-\eta x)-\frac{\beta_n}{\alpha}+\frac{p}{4}\left(V_{GS}-V_{fbn}\right)\right]\left(1+\frac{p}{4}\right)^{-1} \times \left[1+\frac{p}{t_{si}}y-\frac{p}{t_{si}^2}y^2\right]-\left(V_{GS}-V_{fbn}\right)y\left[\frac{p}{t_{si}}-\frac{p}{t_{Si}^2}y\right]; n = 1,2,3, \tag{2}$$

$$\phi_{cn}(x)=M_n \exp(\eta x)+N_n \exp(-\eta x)-\frac{\beta_n}{\alpha} \tag{3}$$

where $p=\frac{\varepsilon_{ox} t_{si}}{\varepsilon_{si} t_{ox}}$ is the ratio of oxide capacitance $\left(\frac{\varepsilon_{ox}}{t_{ox}}\right)$ to channel capacitance $\left(\frac{\varepsilon_{si}}{t_{si}}\right)$, where ε_{ox} and ε_{si} are the permittivity of the gate oxide and silicon. η, α and β_n are defined as-

$\eta=\sqrt{\alpha}$, $\alpha=\frac{1}{\lambda^2}$, $\beta_n=\frac{q\lambda^2 N_{eff}-\varepsilon_{si}\left(V_{GS}-V_{fbn}\right)}{\varepsilon_{si}\lambda^2}$ and λ the characteristic length related with the centre channel potential is equal to $\sqrt{\frac{t_{si}^2\left(1+\frac{p}{4}\right)}{2p}}$. M_n and N_n are unknown coefficients that have been attained with the support of boundary conditions as given from Eq. (A) to Eq. (F) -

$$M_1=\frac{1}{2\sinh\left[\eta\left(L_1+L_2+L_3\right)\right]}\left[V_{bi}+V_{ds}+\frac{\beta_3}{\alpha}-\left(V_{bi}+\frac{\beta_1}{\alpha}\right)\exp\left[-\eta\left(L_1+L_2+L_3\right)\right]+\frac{\left(\beta_1-\beta_2\right)}{\alpha}\cosh\left[\eta\left(L_2+L_3\right)\right]+\frac{\left(\beta_2-\beta_3\right)}{\alpha}\cosh\left(\eta L_3\right)\right] \tag{A}$$

$$M_2=M_1\exp\left(\eta L_1\right)+\frac{\left(\beta_2-\beta_1\right)}{2\alpha} \tag{B}$$

$$M_3=M_1\exp\left[\eta\left(L_1+L_2\right)\right]+\frac{\left(\beta_2-\beta_1\right)\exp\left(\eta L_2\right)}{2\alpha}+\frac{\left(\beta_3-\beta_2\right)}{2\alpha} \tag{C}$$

$$N_1=\frac{1}{\alpha}\left(\alpha V_{bi}+\beta_1-\alpha M_1\right) \tag{D}$$

$$N_2=N_1\exp\left(-\eta L_1\right)-\frac{\left(\beta_1-\beta_2\right)}{2\alpha} \tag{E}$$

$$N_3=N_1\exp\left[-\eta\left(L_1+L_2\right)\right]-\frac{\left(\beta_1-\beta_2\right)}{2\alpha}\exp\left(-\eta L_2\right)-\frac{\left(\beta_3-\beta_2\right)}{2\alpha} \tag{F}$$

In Eq. (4), the resultant expression for virtual cathode potential $\phi_{vc}(y)$ can be formulated as [23]-

$$\phi_{vc}(y)=\left[1+\frac{p}{4}\right]^{-1}\left[\phi_{C1\min}+\frac{p}{4}\left(V_{GS}-V_{fb1}\right)\right]\left[1+\frac{p}{t_{si}}y-\frac{p}{t_{Si}^2}y^2\right]-\frac{\left(V_{GS}-V_{fb1}\right)y}{t_{si}}\left[p-\frac{p}{t_{si}}y\right] \tag{4}$$

$n=1,2,3$

where $\phi_{c1\min}=\phi_{c1}\left(x_{0\min}\right)$ is the smallest potential point lengthwise of the channel, that can be attained by solving $\left.\frac{d\phi_{c1}(x)}{dx}\right|_{x=x_{0\min}}$ which in turn provides Eq. (5) and Eq. (6) [27].

$$x_{o\min}=\frac{1}{2}\sqrt{\frac{t_{si}^2\left(1+\frac{p}{4}\right)}{2p}}\ln\left(\frac{N_1}{M_1}\right) \tag{5}$$

$$\phi_{C1}\left(x_{0\min}\right)=\phi_{C1\min}=\left(V_{GS}-V_{fb1}\right)+2\sqrt{M_1N_1}-\frac{\lambda^2 qN_{eff}}{\varepsilon_{si}} \tag{6}$$

where V_{fbn} signifies flat band voltages, and n is the characteristic length of center potential. Now, Pao–Sah's double integral [21], the sub-threshold current I_D for short-channel (TMG-DH) DG MOSFET can be given by Eq. (7).

$$I_D=\frac{\mu\left(\frac{kT}{q}\right)\left(1-\exp\left(-\frac{qV_{DS}}{kT}\right)\right)}{\int_0^{L_1}Q_1^{-1}dx+\int_{L_1}^{L_1+L_2}Q_2^{-1}dx+\int_{L_1+L_2}^{L}Q_3^{-1}dx} \tag{7}$$

where μ is the free carrier mobility and Q_n is the charge density and can be demarcated as in Eq. (8) [26]

$$Q_n = \frac{qn_i^2}{N_{eff}} \int_0^{t_{si}} \exp\left(\frac{q}{kT}\phi_n(x,y)\right) dy \qquad n=1,2,3 \tag{8}$$

where $\frac{kT}{q} = V_T$ is the thermal voltage. For the reason that the sub-threshold leakage generally arises in the virtual cathode point, $x_{0\min}$ [25], Eq. (8) can be modified as given in Eq. (9) [20]

$$Q_n = \frac{qn_i^2}{N_{eff}} \int_0^{t_{si}} \exp\left(\frac{q}{kT}\phi_n\left(x_{0\min}, y\right) = \phi_{vc}(y)\right) dy \tag{9}$$

Due to complex nature of $\phi_{vc}(y)$, it can be said that Eq. (9) is the complex function that cannot be analytically realized. However, it is remarkable that in undoped or lightly doped channel cases, the sub-threshold carrier's conduction restricts close to the center of channel. For the given circumstance, the effective conduction path can be defined as $y = {}^{t_{si}}\!/_{4}$ [22]. Holding the benefit of the above fact, Eq. (9) can be further solved as given in Eq. (10)-

$$Q_n = \frac{2n_i^2 qt_{si}}{N_{eff}} \exp\left(\frac{q}{KT}\left[V_{GS} - V_{fbn} + \left(\frac{4}{4+P}\right) \times \frac{1}{\varepsilon_{si}}\left(2\sqrt{M_1 N_1}\varepsilon_{si} - \lambda^2 qN_{eff}\right) \times \left(1+\frac{3P}{16}\right)\right]\right)$$

(10) n=1, 2, 3

Substituting the value of Q_n into Eq. (7), we get the sub-threshold current I_D as in Eq. (11)-

$$I_D = \frac{\mu\left(\frac{kT}{q}\right)\left(1-\exp\left(-\frac{qV_{DS}}{kT}\right)\right)}{L_1 Q_1^{-1} + L_2 Q_2^{-1} + L_3 Q_3^{-1}} \tag{11}$$

Due to the inherent step potential profile in short-channel (TMG-DH) DG MOSFET, the potentials of section II and III are greater than section I and so the first term of the denominator will have more impact and Eq. (11) can be reformed as in Eq. (12)

$$I_S = 2t_{si} q \frac{\mu\left(\frac{kT}{q}\right)}{L_1}\left(\frac{n_i^2}{N_{eff}}\right) \times \left(1-\exp\left(-\frac{qV_{DS}}{kT}\right)\right) \times$$

$$\exp\left(\frac{q}{kT}\left(V_{GS} - V_{fb1} + \left(\frac{4}{4+p}\right) \times \left(2\sqrt{M_1 N_1} - \frac{\lambda^2 qN_{eff}}{\varepsilon_{si}}\right) \times \left(\frac{16+3p}{16}\right)\right)\right) \tag{12}$$

The starting material is a computer, an internet connection, and large quantity of time and coffee.

3.2 Sub-threshold swing model

As we know, sub-threshold current $I_D \propto \int n_i \exp\left(\frac{(\phi_{vc}(y) - \phi_F)}{kT/q}\right)$, where ϕ_F is the Fermi potential, sub-threshold swing S of (TMG-DH) DG MOSFET can be written as [25]-

$$S = \left(\frac{\partial \log I_D}{\partial V_{GS}}\right)^{-1} = \ln 10 \left(\frac{\partial \ln I_D}{\partial V_{GS}}\right)^{-1} = \frac{kT}{q} \ln 10 \times \left(\frac{\partial \phi_{VC1}(y)}{\partial V_{GS}}\right)^{-1} \tag{13}$$

The effective conduction path d_{eff} of the sub-threshold conduction is at $y = \frac{t_{si}}{4}$ and $\frac{3t_{si}}{4}$, Eq. (13) can be generalized as [28]-

$$S = \frac{kT}{q} \ln 10 \times \left(\frac{\partial \phi_{VC1}\left(y = \frac{t_{si}}{4}\right)}{\partial V_{GS}}\right)^{-1} \tag{14}$$

Now, Eq. (6) is differentiated with respect to V_{GS}, we obtain Eq. (15)-

$$\frac{\partial \phi_{VC1}\left(y = \frac{t_{si}}{4}\right)}{\partial V_{GS}} = \left(\frac{\frac{\partial \phi_{C1\min}}{\partial V_{GS}} + \frac{p}{4}}{1+\frac{p}{4}}\right)\left(1+\frac{3p}{16}\right) - \frac{3p}{16} \tag{15}$$

where,

$$\frac{\partial \phi_{C1\min}}{\partial V_{GS}} = 1 + \frac{1}{\sqrt{M_1 N_1}}\left(\left(N_1 - M_1\right)\left(\frac{\left(\exp(-\eta L)-1\right)}{2\sinh(\eta L)}\right) - M_1\right) \tag{16}$$

By utilizing Eq. (14) and Eq. (16), sub-threshold swing (S) for short-channel (TMG-DH) DG MOSFET can be written as in Eq.17.

$$S = \frac{kT}{q} \ln 10 \times \left(\frac{1 + \frac{1}{\sqrt{M_1 N_1}}\left(\left(N_1 - M_1\right)\left(\frac{\left(\exp(-\eta L)-1\right)}{2\sinh(\eta L)}\right) - M_1\right) + \frac{p}{4}}{1+\frac{p}{4}}\left(1+\frac{3p}{16}\right) - \frac{3p}{16}\right)^{-1} \tag{17}$$

3 Results and Discussion

This section involves detailed analysis and discussion of the double halo technique and its impact on the performance of (TMG-DH) DG MOSFET. In this paper, we have investigated, analyzed and compared the theoretical results of sub-threshold current and sub-threshold swing of (TMG-DH) DG MOSFET structure with its numerical simulation results utilizing the ATLAS™ simulation tool [29]. For transportation of carriers, drift diffusion models are involved because they are simple and appropriate for Nano-channel devices [20, 30]. In addition, Poisson's equation with recombination model and constant field mobility model are also employed for the analysis of electric field distribution. Parameters taken for the designing of (TMG-DH) DG MOSFET are described in Table. 1.

Figure 2 depicts the impact of gate length ratio ($L_1:L_2:L_3$) on sub-threshold current (I_D) with respect to gate to source voltage (V_{GS}). The result indicates that the control gate length L_1 increases, and a significant decrement occurs in the sub-threshold leakage current due to the involvement of long channel properties caused by an extended control gate length. Moreover, we have compared the theoretical results of (TMG-DH) DG MOSFET structure with the

numerical data. They showed consistency with each other. In Figure 3, we have scrutinized the behavior of sub-threshold current (I_D) with respect to V_{GS} on the variation of channel length (60 nm, 90 nm, 120 nm) of the device. For such investigation, we have fixed the gate length ratio ($L_1:L_2:L_3$) to (1:1:1), t_{si} to 10 nm, t_{ox} to 2 nm and drain to source voltage (V_{DS}) to 0.1 volt. The graph shown in Figure 3 exemplifies that as we increase the channel length L, sub-threshold leakage current slope increases and value decreases. This qualifies the device for better switching applications. Furthermore, we have compared the theoretical results of (TMG-DH) DG MOSFET structure with the numerical data at various channel length L. They showed consistency with each other. In Figure 4, we have examined the mutation in sub-threshold current (I_D) with respect to V_{GS} by varying thickness of the gate oxide from 2 nm to 3 nm. In this case, we have kept gate length ratio ($L_1:L_2:L_3$) to 1:1:1, t_{si} to 10 nm, drain to source voltage (V_{DS}) to 0.1 volt and L to 60 nm. The result manifests that large value of t_{ox} pushes the sub-threshold leakage current to the highest value. The fact behind this behavior is that as t_{ox} broadens, the control of gate over channel weakens because of the deterioration of gate electrostatics in the channel region. In Figure 5, by keeping the same parameters as taken in Figure 4 and fixing t_{ox} 2 nm, we have varied the thickness of silicon channel from 15 to 20 nm. It is quite evident that as sub-threshold leakage increases, current increases due to abated channel electrostatics and lower threshold voltage [23].

In scaled devices, the drain control over the charges of channel region upsurges resulting in enlarged sub-threshold swing. Also, Tiwari *et al.* [20] reported that DM-DG MOSFETs have greater sub-threshold swing than TM-DG MOSFETs so they are more susceptible to SCE. Thus, TM-DG MOSFETs have been recommended since then. However, there is some plausibility of SCE in TM-DG MOSFETs that can be abridged by halo technique. Single halo improves the SCE up to some more extent as reported by [14]. For further augmentation, when double halo technique was incorporated, it gave a noticeable declination in sub-threshold swing. Thus, the overall device performance improved.

Moreover, from Figure 6 to Figure 8, we have observed the behavior of sub-threshold swing in scaled TM-DG-DH MOSFET. In Figure 6, oxide thickness is varied from 2 nm to 3 nm against gate length L by fixing $L_1:L_2:L_3$ to 1:1:1, t_{si} to 20 nm, V_{DS} to 0.1 volt and other doping parameters to the same value as illustrated in Table 1. The graph indicates that greater value of t_{ox} results in high sub-threshold swings; that is exactly the same as the impact of t_{ox} on TM-DG MOSFETs [20]. Therefore, it can be understood that (TMG-DH) DG MOSFET accomplishes long channel characteristics at somewhat lesser channel length compared to the MOS device with wider gate oxide.

Table 1: Parameters involved for the designing of (TMG-DH) DG MOSFET.

S. N.	Parameter	Value
1.	ϕ_{m1} (work-function of control gate material WSi_2)	4.8 eV
2.	ϕ_{m2} (work-function of first screen gate material $Hf_{0.27}Ta_{0.58}N_{0.15}$)	4.6 eV
3.	ϕ_{m3} (work-function of second screen gate material $Hf_{0.40}Ta_{0.46}N_{0.14}$)	4.4 eV
4.	N_a (p-type uniformly doped surface concentration)	$1*10^{16}$ cm^{-3}
5.	N_{pp} (peak pocket doping concentration)	$2*10^{18}$ cm^{-3}
6.	$N_{S/D}$ (doping concentration of the source and drain regions)	$1*10^{20}$ cm^{-3}

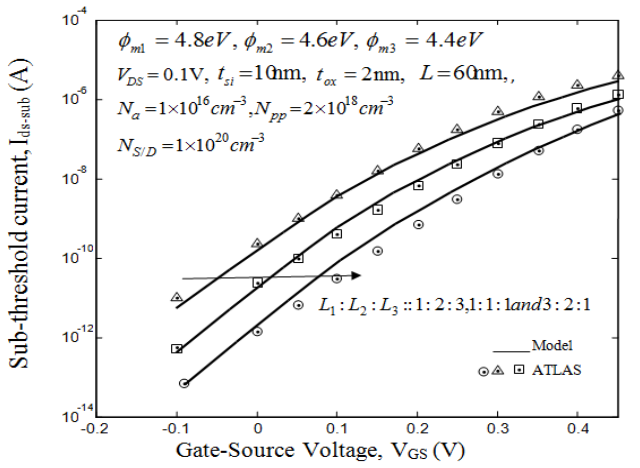

Fig. 2: Subthreshold current (I_D) variation with gate to source voltage (V_{GS}), with L_1:L_2:L_3 as a constraint.

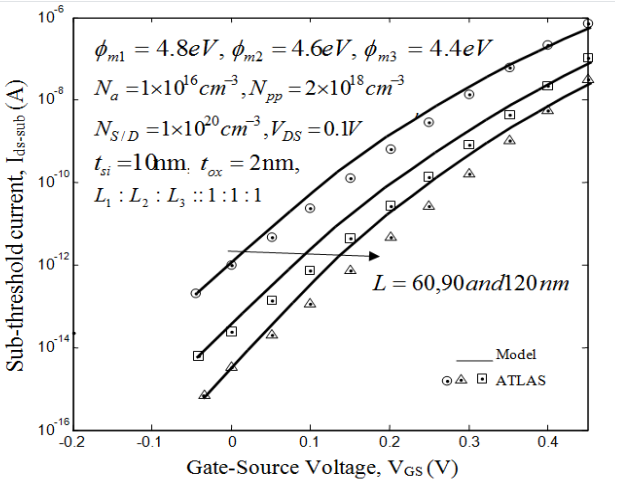

Fig. 3: Demonstration of subthreshold current (I_D) with gate to source voltage (V_{GS}), with channel length L as constraint.

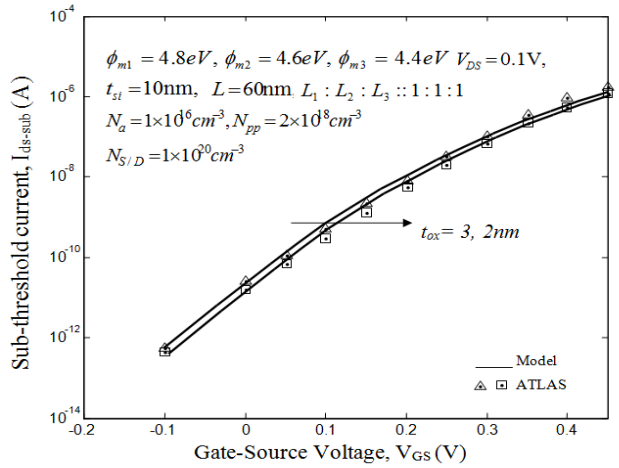

Fig. 4: Subthreshold current (I_D) variation with gate to source voltage (V_{GS}) for different gate oxide thickness t_{ox}.

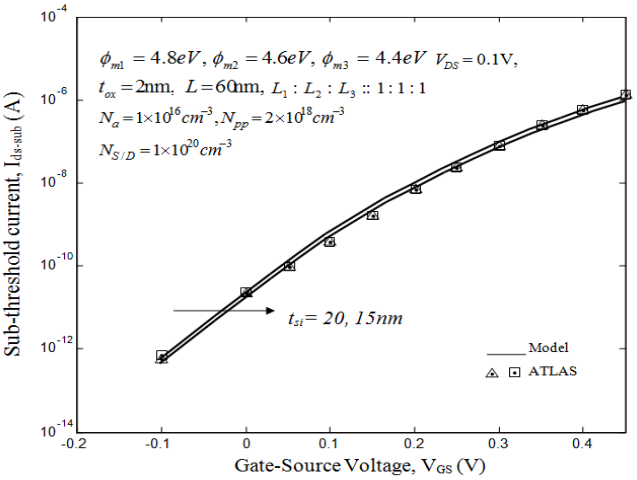

Fig. 5: Subthreshold current (I_D) variation with gate to source voltage (V_{GS}) for different silicon channel thickness t_{si}.

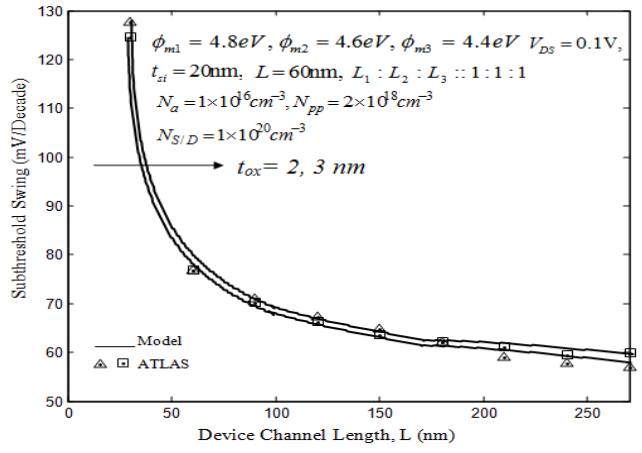

Fig. 6: Subthreshold swing variation (S) with channel length L for different gate-oxide thickness t_{ox}.

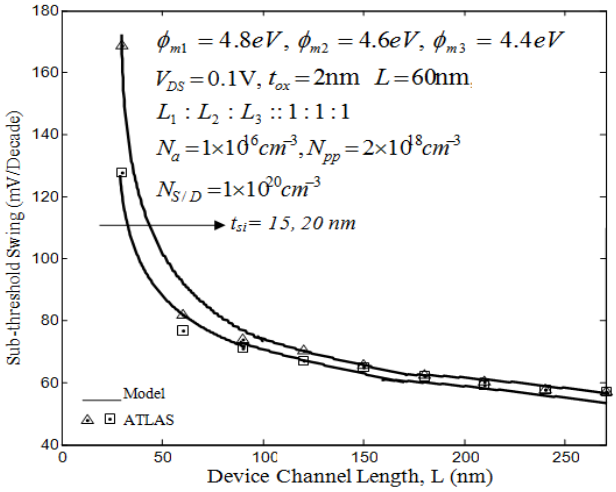

Fig. 7: Subthreshold swing variation (S) with channel length L for different silicon channel thickness t_{si}. Thicker silicon body is responsible for degrading the switching characteristics.

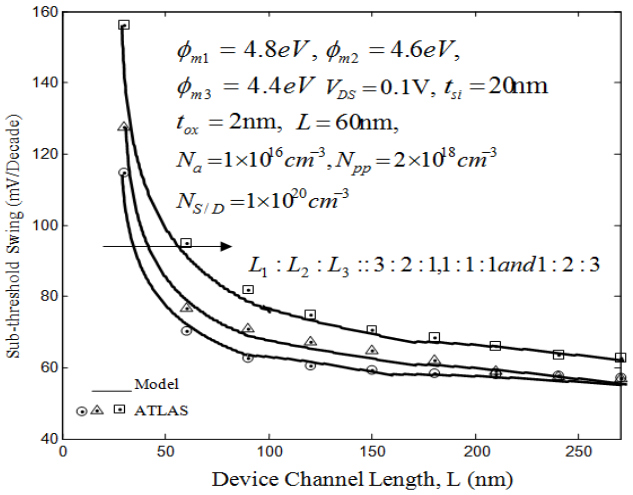

Fig. 8: Demonstration of subthreshold swing variation (S) with channel length (L) with L_1:L_2:L_3 as a variable parameter.

Thinner t_{ox} is required for better switching characteristics. Similarly, Figure 7 indicates that there are somehow the same reasons for high sub-threshold swing at high value of t_{si} by fixing some parameters, such as t_{ox} = 2 nm and L_1:L_2:L_3:: 1: 1: 1. Furthermore, Figure 8 depicts the impact of gate length ratio (L_1:L_2:L_3) on sub-threshold swing (I_D) with respect to device channel length (L). At higher gate length ratio, sub-threshold swing diminishes. Also, the analytical models are consistent with the theoretical results in all the cases considered above for proper scrutiny.

For the MOS device having gate length less than or equal to

10 nm, it becomes inevitable to tunnel the electrons from source end to drain end through channel [31, 32]. As a consequence, transport of carrier on this length scale is basically ballistic. However, we have designed the device comprising the model having minimum channel length of 30 nm. Therefore, the present device does not account the effect of source to drain tunneling. Nevertheless, for the present model, it is one of the seeming limitations. In addition, the present model for sub-threshold swing and sub-threshold current of TM-DG-DH MOSFET does not contain the channel doping effect because we have considered $d_{eff}=\frac{t_{si}}{4}$ [10, 26], which only depends upon t_{si} in this model, but it varies with the channel doping concentration, as well.

5 Conclusions

In this paper, we have demonstrated the model of sub-threshold current and sub-threshold swing for (TMG-DH) DG MOSFET. The influences of double halo technique on sub-threshold parameter have been explored in depth. After appropriate investigation of the MOS device under study, we can conclude that for favorable sub-threshold conduction behavior, control gate length should be greater than length of screen gates. Also, we have found that the present model consistent with the theoretical results of the device. Moreover, to generate fully-analytical model for the present device, it was supposed that conduction of sub-threshold current is along the halfway point of the upper and lower of the channel, i.e. $y=\frac{t_{si}}{4}$ and $y=\frac{3t_{si}}{4}$, respectively. Quantum–mechanical effects (QME) are not involved in the current model because it is inappropriate for silicon channel thickness greater than or equal to 10 nm.

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