UNIVERSITAT POLITÈCNICA DE CATALUNYA
BARCELONATECH
Departament d'Enginyeria Electrònica

Low-Power Read-Out ICs for Smart Electrochemical Sensors

Joan Aymerich Gubern

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Resum

En els últims anys s'ha produït una ràpida expansió dels sensors electroquímics en comparació amb altres tecnologies químiques de sensat gràcies al seu potencial per generar dispositius analítics precisos, selectius, miniaturitzats i econòmics. Aquestes característiques satisfan l'actual creixent demanda de sistemes de sensat d'un sol ús, on la usabilitat, la portabilitat i el preu són els factors més importants, permetent detectar evidència analítica per qualsevol persona, en qualsevol lloc i en qualsevol moment, sense limitacions en termes de calibratge o de temps de vida útil. En particular, un dispositiu electroquímic ha d'incloure una interfície electrònica intel·ligent aparellada per estimular específicament la cèl·lula electroquímica, adquirir senyals, realitzar la conversió de dades i comunicar les mesures a través d'una interfície digital estàndard, tot sota restriccions severes de mida, cost i potencia consumida.

Aquesta tesi descriu el desenvolupament d'una nova plataforma de detecció electroquímica, econòmica, d'un sol ús, d'alt rendiment i fàcil d'utilitzar, que combina la intel·ligència de circuits integrats CMOS amb la flexibilitat de l'electrònica impresa.

Es presenten dues realitzacions de circuits integrats de lectura en tecnologies CMOS de 65-nm i 0.18-μm amb un consum de l'ordre de μW, específicament optimitzades per a la polarització potenciostàtica i la lectura amperomètrica de sensors electroquímics. Les interfícies proposades ofereixen implementacions CMOS molt elegants i compactes, ja que reutilitzen les propietats dinàmiques del mateix sensor per implementar moduladors Delta-Sigma ($\Delta\Sigma$M) mixtes en temps continu. Les topologies inclouen potenciòstats diferencials per ampliar el seu rang. A més, permeten aconseguir un límit baix de detecció mitjançant la implementació d'un nou mecanisme de cancel·lació del soroll de baixa freqüència provinent de la retroalimentació digital-analògic del modulador $\Delta\Sigma$M electroquímic. El xip inclou una interfície digital estàndard basada en I^2C per controlar l'extensa configuració del sistema i també per reduir el nombre de connexions externes de cara al seu muntatge de baix cost sobre substrats flexibles. Es presenten resultats experimentals de les proves tant elèctriques com electroquímiques i es comparen amb altres interfícies de sensors electroquímics d'última generació.

Finalment, es proposa una interfície híbrida rendible, on s'imprimeix directament el sensor electroquímic sobre un substrat PEN flexible que també allotja la interfície CMOS integrada de lectura a nivell de dau de silíci sense encapsular. Els tres elèctrodes del sensor i tota la connectivitat s'aconsegueixen gràcies a la tecnologia d'impressió d'injecció de tinta de baix cost. Així mateix, s'investiguen els adhesius conductors anisotròpics com un enfocament emergent per al contacte mecànic i elèctric entre la matriu del circuit integrat CMOS i les tintes conductores per tal d'obtenir un dispositiu sensorial electroquímic flexible d'un sol ús.

Abstract

Electrochemical sensors are expanding rapidly over other chemical sensoring technologies because of their potential to generate precise, selective, miniaturized and cost-effective analytical devices. These features satisfy the emerging global demand for disposable testing systems at the point-of-need, where usability, portability, and price counts most, enabling to detect critical analytical evidence by anyone, anywhere and at any time, without concerning about recalibration and limited shelf life. In particular a disposable electrochemical device must include a paired smart electronic interface to specifically bias the electrochemical cell, acquire signals, perform data conversion and communicate measurements through a standard digital interface, all under severe restrictions of size and power consumption.

This thesis describes the development of a novel, cost-effective, disposable, high-performance and user-friendly electrochemical sensing platform that combines the smartness of CMOS integrated circuits (ICs) with the flexibility of printed electronics.

Two practical μW-range readout integrated circuit (ROIC) realizations in 65-nm and 0.18-μm CMOS technologies are presented and specifically optimized for the potentiostatic biasing and amperometric read-out of electrochemical sensors. The proposed frontend architectures yield very elegant and compact CMOS implementations by reusing the dynamic properties of the sensor itself to implement continuous-time mixed electrochemical delta-sigma modulators ($\Delta\Sigma$M). The topologies include differential potentiostats to extend its range. Furthermore, low limit of detection (LOD) values can be achieved by implementing a novel cancellation mechanism of the flicker noise coming from the feedback DAC of the electrochemical $\Delta\Sigma$M. A standard interface based on I^2C is included on-chip not only to control the extensive system configuration but also to limit the number of IC pads towards a low-cost flip-chip assembly on flexible substrates. Experimental results from both electrical and electrochemical tests are presented and compared to other state-of-the-art electrochemical sensor frontends.

A cost-effective hybrid electronics interfacing approach is proposed, where the electrochemical sensor is directly printed on a flexible PEN substrate that also hosts the CMOS ROIC as a bare die without wire bonding. Low-cost inkjet printing technology is employed for the development of a three-electrode sensor and all the required connectivity. Anisotropic conductive adhesives are investigated as an emerging approach for mechanical and electrical contact between the IC die and printed inks in order to obtain a disposable flexible smart electrochemical sensory device.

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A/D analog to digital . . . 10
ACA anisotropic conductive adhesive . . . 23
ADC analog-to-digital converter . . . 13
AFE analog frontend . . . 15
ASIC application specific integrated circuit . . . 24
CPE constant phase element . . . 4
BDI buffered direct injection . . . 14
CDS correlated double sampling . . . 12
CE counter electrode . . . 7
CMOS complementary metal-oxide-semiconductor . . . 2
CT continuous time . . . 17
CV cyclic voltammetry . . . 9
DAC digital-to-analog converter . . . 30
DC direct current . . . 12
DFB distributed-feedback . . . 31
DIL dual in-line . . . 93
DOD drop-on-demand . . . 20
DRC design rule checking . . . 58
DR dynamic range . . . 109
ΔΣM ΔΣ modulator . . . 26

DT discrete time 17
EA error amplifier 71
ECG electrocardiogram 24
EDL electrical double layer 4
EIS electrochemical impedance spectroscopy 7
EKV Enz-Krummenacher-Vittoz 50
ELD excess loop delay 35
EMI electromagnetic interference 10
FF feed-forward 32
FHE flexible hybrid electronics 19
HDL hardware description level 69
I/F current-to-frequency 15
I/V current-to-voltage 12
IC integrated circuit 2
IMB-CNM Institut de Microelectrònica de Barcelona 42
IPT inkjet printing technology 25
LHP left-half plane 14
LOD limit of detection 1
LVDS low-voltage differential signaling 110
LVS layout versus schematic 58
MCU microcontroller 40
MOSFET metal-oxide-semiconductor field-effect transistor 50
SHE standard hydrogen electrode 7
NMOS n-channel MOS 14
NTF noise transfer function 31
OSR oversampling ratio 31
PCB printed circuit board 19
PDF probability distribution function 106
PDMS polydimethylsiloxane 21
PECVD plasma enhanced chemical vapour deposition 88
PEN polyethylene naphthalate 21
PET polyethylene terephthalate 21
PGA programmable gain amplifier 12
PI Kapton polyimide 21
PMOS p-channel MOS 14
PMU power management unit

POR power on reset 63
PSD power spectral density 103
PTAT proportional to absolute temperature 50
PVT process, voltage and temperature 12
PWM pulse width modulator 15
RDL redistribution layer 22
RE reference electrode 7
RHP right-half plane 35
ROIC readout integrated circuit 2
RMS root-mean-square 40
RTL register transfer level 69
S/H sample and hold 13
SAR successive approximation register 15
SCL serial clock line 67
SC switched-capacitor 13
SDA serial data line 67
SNDR signal-to-noise-and-distortion ratio 17
SNR signal-to-noise ratio 29
SoC system on chip 72
SPI serial peripheral interface 110
SPT screen printing technology 25
SQNR signal-to-quantization-noise ratio 16
TIA transimpedance amplifier 11
UV ultraviolet 83
VCCS voltage controlled current source 58
VCVS voltage controlled voltage source 58
WE working electrode 7
ZIF zero insertion force 81

Introduction | 1

1.1 Motivation

Electrochemical sensors are used in a wide range of key applications such as control of food quality and safety (e.g. freshness, GMO, E. Colim, Cholera toxin) [14–18], environmental monitoring (e.g. NO, NO_2, CO, CO_2, and SO_2) [19, 20], as well as in health care monitoring and diagnosis (e.g. glucose, hepatitis, DNA and proteins) [21–23].

Despite their intrinsic limitations in terms of speed and lifetime, electrochemical sensors have achieved considerable success over other sensing technologies due to their good limit of detection (LOD), the inherent facility to interact with living organisms at microscopic scale [24] and also the possibility of increasing sensor selectivity by the functionalization of their surface to detect a particular chemical compound [25]. Furthermore, electrochemical sensors have been studied on a large scale in the last years with the intention of extending their sensing capabilities into biochemical domains by combining a bio-receiver attached on the surface of the electrochemical sensor [26]. In this sense, Fig. 1.1 illustrates the different fields where these electrochemical sensors are typically applied.

Due to the high demand of the world market and the human interest for having a device to continuously monitor the concentration of chemical species, the new generation of electrochemical sensors will require important improvements on the developement of new low-power, cost-effective, high resolution, real time, portable and even flexible smart sensory systems to meet the future needs in diversity of applications. As electrochemical sensors usually suffer from a limited number of readout cycles, new trends come to split such smart sensory systems in two parts:

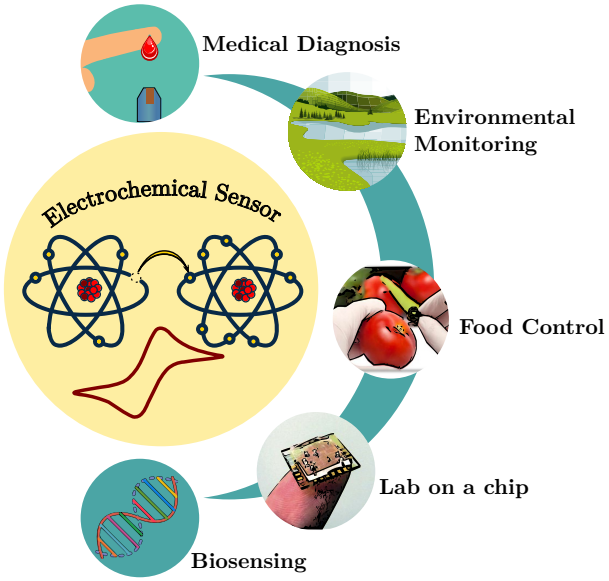

Figure 1.1 | Electrochemical sensor typical applications.

one device realized by cost-effective materials and fabrication manners for disposable use and another composed of relatively expensive components for repeatable applications [27]. Fig. 1.2 depicts this system concept from the electrochemical transduction up to the data capture and visualization on smartphones. By combining the smartness of advanced complementary metal-oxide-semiconductor (CMOS) integrated circuits (ICs) technology and the low cost of printed electronics, a very powerful, versatile and cost-effective solution for disposable sensor devices can be achieved. In this sense, the disposable device features, in a single flexible substrate a printed electrochemical sensor with inexpensive compositions of conductive inks, whereas a very compact high-performance readout integrated circuit (ROIC) is directly attached as a bare die without any costly wire bonding. The development of this ROIC introduces new design challenges, since it must integrate in a compact Silicon area advanced functions like sensor bias cotrol, signal conditioning, data conversion and digital configurability, all under strict power budgets. The total cost of the disposable electrochemical device is expected to not overcome the estimated budget of Table 1.1. At the other end, the nondisposable rigid dongle, constituted of few discrete electronic components, is employed as controller for programming, memory and communications. Finally, the reuse of the smartphone offers portable and autonomous graphical interface and opens the possibility to benefit from cloud-based services for ubiquitous data flow.

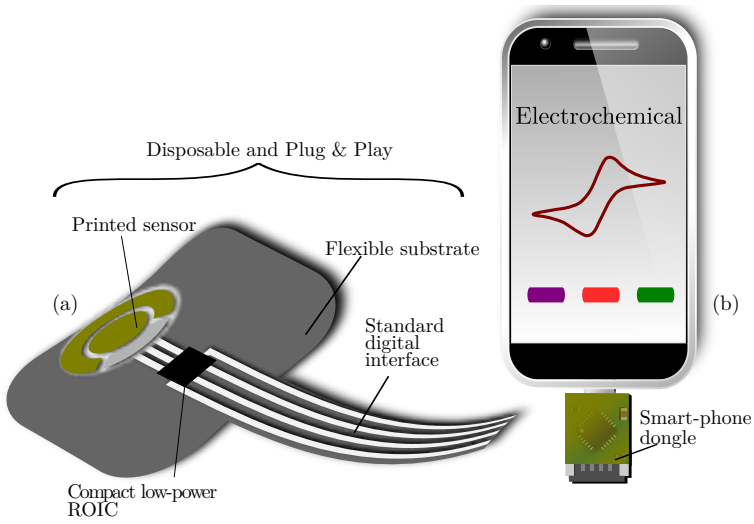

Figure 1.2 New smart electrochemical sensor concept: disposable device (a) and end-user interface (b). Drawing not to scale.

Material	**Cost [€]**
Flexible substrate	0.10
Printed electrochemical sensor	0.30
Printed contacts and interconnections	0.10
CMOS ROIC	0.20
Flip-chip assembly	0.05
Total	0.75

Table 1.1 Estimated unit cost of the disposable electrochemical sensing device of Fig. 1.2(a) for mass production (> 1 million units/year).

1.2 Electrochemical Sensing Principles

Electrochemical methods are analytical techniques that involve a series of highly practical measurements [28]. A key feature of these techniques consists of an electrode that provides an interface where charge transfer processes take places. Such charge transfer process leads to potentials and/or currents that can be electron-

ically measured and the resulting data may be related to the concentration of a target analyte. Generally, these methods can be classified into two main groups: measurements that do not comprise current flow, referred as potentiometric, and measurements that comprise current at an electrode through potential control, referred as amperometric or voltammetric. Amperometric and voltammetric methods are the main focus of this thesis, and typically consist of three functional components:

1. Analyte, the substance that is of interest, whose chemical constituents are being identified and measured, such as acid ascorbic, ferricyanide, ferrocene, bacteria, etc.

2. Transducer or electrode, in contact with an electrolyte solution, which converts the electrochemical response to a measurable electrical signal proportional to the concentration quantity of analytes.

3. Instrumentation, generally comprised of electronic circuitry, that senses, amplifies, quantifies and records the signals from the transducer.

When an electrode is immersed in a solution, a charge separation occurs across the interface and electrical double layer (EDL) is established, in much the same way as charge gathers on the two plates of a parallel plate capacitor. Fig. 1.3 shows the electric charge and potential distribution in the EDL on the electrode surface. The charge developed at the electrode surface is balanced by the solution across a small volume consisting of both adsorbed ions and ions in solution. Overall, this volume extends over a distance d of a few nanometers, where (most of) the electrode potential is developed and electron transfer between the electrode and species in solution takes place [28, 29]. The outter region, known as the diffuse layer extends up to the bulk of the solution and is composed of solvated anions and cations. These alternating layers of charges have the ability to store electrical energy, and are named as the capacitive double layer (C_{dl}). Indeed, C_{dl} is very thin and functions similarly to a capacitor with a capacitance of approximately 10 to 100 $\mu\mathrm{Fcm}^{-2}$ of electrode surface. However, the effects on the electrode surface, like inhomogeneity and roughness, may influence the behaviour of C_{dl}. In this sense, C_{dl} may behave like a constant phase element (CPE) [28], resulting in a phase angle close but different from 90°. Additionally, it may has a non-linear behaviour in that the capacitance of the layer may vary with the external potential applied to the system.

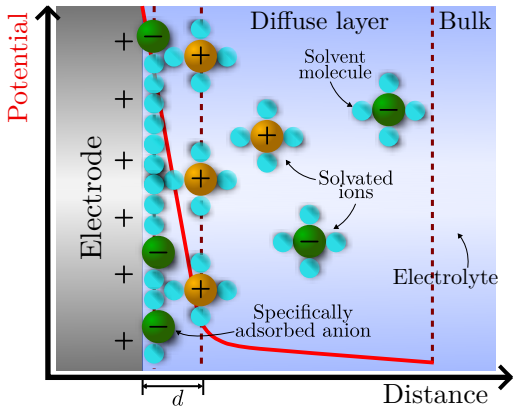

Figure 1.3 Electric charge and potential distribution in the EDL of the electrode-electrolyte interface for the case of positively-charged solid electrode [1].

1.2.1 Electrode-Electrolyte Interface

The principle of electrochemical sensing is the study of the interface between the metal electrode and the electrolytic solution. The interaction of the electrode-electrolyte interface can be classified according to:

1. Faradaic process, consisting in electron transfer across the electrode-electrolyte interface as a result of a reduction (gain of electrons) or oxidation (loss of electrons), generally known as redox reaction. Since such reactions are governed by Faraday's law, the amount of chemical reaction (mass) caused by the flow of current is proportional to the total charge passed through the electrode-electrolyte interface [28].
2. Non-faradic process, which gives rise to a current that is not attributed to any redox process occurring at the electrode surface.

The charge transfer of a Faradaic process is controlled by a potential applied to the interface. The consequent current corresponds to the oxidation or reduction of the target analyte at the measurement potential. Equation (1.2) describes the simplest form of a redox reaction:

$$\mathrm{Ox} + n\mathrm{e}^- \rightleftharpoons \mathrm{Red}, \tag{1.1}$$

where Ox and Red are the oxidized and reduced forms of the electrochemical species, respectively, and n is the number of electrons involved in the redox re-

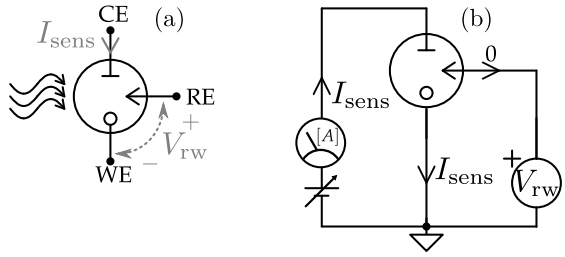

Figure 1.4 | Three-electrode electrochemical cell (a) and typical potentiostatic amperometric measurament setup (b).

action. The required potential value for the redox activation mostly depends on the chemical species present in the solution. This quantitative relationship is expressed in the Nernst equation as folows:

$$E = E^{0'} + \frac{RT}{nF} ln \frac{C_{\mathrm{O}}}{C_{\mathrm{R}}}, \tag{1.2}$$

where C_{O} and C_{R} are the analyte concentrations in the solution bulk, R is the gas constant, T is the temperature, F is the Faraday constant and $E^{O'}$ is the formal potential, which is the potential measured for a couple at equilibrium in a system where the concentration ratio of Red/Ox is unity and with specific solution conditions. Although generally the Faradaic processes are the main interest of an electrochemical investigation, the effect of non-Faradaic processes must be taken into account as well. Actually, the non-Faradaic process, also called double-layer currents, does not involve any chemical reactions (charge transfer). It is basically the current due to the accumulation (or removal) of electrical charges on the electrode and in the electrolyte solution near the electrode. In other words, there is always some capacitive current flowing when the potential of an electrode is changing, and the capacitive current is generally zero when the potential remains constant. These non-Faradaic currents are also commonly referred to as the background currents.

1.2.2 Electrochemical Cell

The family of voltammetric/amperometric sensors (from now on referred to as amperometrics sensors) is very appealing due to the simple structure of their electrochemical cell [30], acting as a transducer. The three-electrode configuration in Fig. 1.4(a) is the most common form of an amperometric transducer. In contrast to the two-electrode configuration, the three-electrode system eliminates sources of distortion in the measurements and reference potential shifts while passing current

through the resistive electrolyte [28]. The working electrode (WE) is the surface where the electrochemical reaction of interest takes place. The conditions at this electrode are accurately controlled in order to favor detection of the analyte of interest. The second electrode, the reference electrode (RE), is designed to develop a well defined potential at the WE. In general, Ag/AgCl RE materials are used in microsystems and there is an extensive literature describing the manufacture and characterization of miniature Ag/AgCl electrodes [31–33]. This typical RE has a standard potential value of 0.197 V vs. standard hydrogen electrode (SHE) RE. For some systems, a pseudo-RE can be employed as a simple metal wire (e.g., Ag or Pt). However, since their reference potential may vary with the composition of the solution, is necessary to know the experimental conditions. Thus, the potential can be calculated and the electrode can be used as a reference. The third electrode, the auxiliar or counter electrode (CE), is in charge of supplying the current required for the electrochemical reaction at WE. Since CE is typically larger than the WE, the process occurring at WE should not limit I_{sens}. CE is usually made from an inert material like Pt or Au. A schematic representation of such a simple experimental setup is presented in Fig. 1.4(b). For the purpose of an accurate control of the potential solution V_{rw}, the current through the RE electrode should ideally be zero, avoiding any undesirable electrode polarization effect. Then, under these specific potentiostatic condition, the redox current I_{sens} can be readout as the measurement of the current flowing through CE and WE.

Taking into account the three-electrode structure, and the potentiostatic amperometric readout method, the electrochemical cell model in terms of electronic behaviour can be incorporated. Electrochemical impedance spectroscopy (EIS) is a very powerful tool to measure the impedance of a system in dependence on the AC potentials frequency [34]. It allows to simplify the electrochemical processes by transforming them into the combination of electrical elements. This technique is performed by applying a small sinusoidal voltage signal to the WE interface. The Randles equivalent circuit depicted in Fig. 1.5(a) is one of the simplest possible models describing processes at the electrochemical interface [28]. In this model, the electrode-electrolyte interface is constituted by the interfacial double-layer capacitance C_{dl}, in parallel with a second branch that accounts for the Faradaic process. The Faradaic process consists of two components: a resistor R_{ct}, which represents the charge transfer process, and a Warburg element Z_{w} due to difussion of the chemical reactants in solution. The Warburg impedance does not significantly contribute to the overall impedance, since its effects are evident only at very low frequencies usually far from the bandwidth of interest. Next, in series with this parallel branch, there exists the solution resistance R_{s}, usually some orders of magnitude lower than R_{ct} counterpart, that represents the non-null resistivity of the electrolyte. A similar circuit can be drawn for the CE. Under potentiostatic operation, that is fixed potential between RE and WE and no current flowing

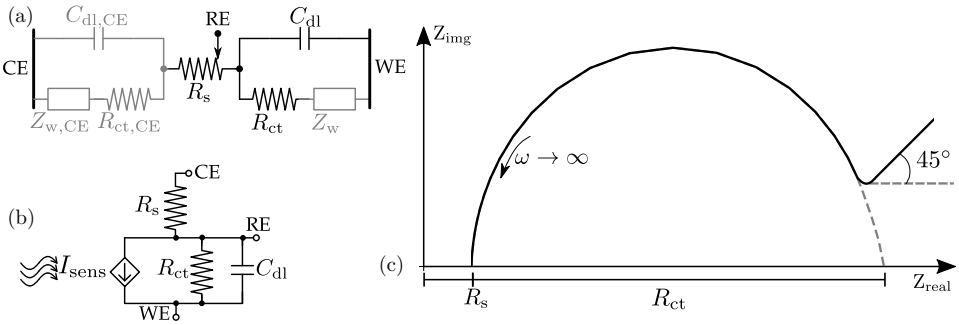

Figure 1.5 Randles equivalent circuit of the electrochemical cell impedance seen between CE and WE (a), small signal model (b) and Nyquist plot (c).

into RE, the contribution of the auxiliary and reference electrode are typically neglected and the equivalent circuit can be approximated by the first-order linear model of Fig. 1.5(b), where I_{sens} stands for the current change caused by the sensor impedance variation due to the chemical transduction.

The equivalent circuit components are commonly obtained by analyzing the imaginiary versus the real parts of the cell impedance in the Nyquist plot, shown in Fig. 1.5(c). This diagram is comprised by a series of points, each of which represents the magnitude and direction of the impedance vector of a specific frequency. Since the resistors consist only of a real part, they appear in the real axis intersections. The semicircle nature of the Nyquist plot comes from the parallel of the charge transfer resistance R_{ct} with C_{dl}, where the resulting diameter represents R_{ct}. The Warburg impedance appears as a diagonal line with a 45-degree slope.

1.2.3 Voltammetry and Amperometry

Distinct sensing modalities are determined depending on the input voltage applied to the potentiostat of Fig. 1.4(b). The controlled V_{rw} potential can be a constant, triangular or pulse waveform. Techniques using constant voltages are generally called amperometry, while those with voltage that vary over time are called voltammetry [28, 29, 35]. A key aspect of these techniques is that the initial potential must be such that non-overall Faradaic current is observed. In other words, the initial potential should be close to the open circuit potential. This facilitates that the current measured during the experiment is due to the main process of interest alone.

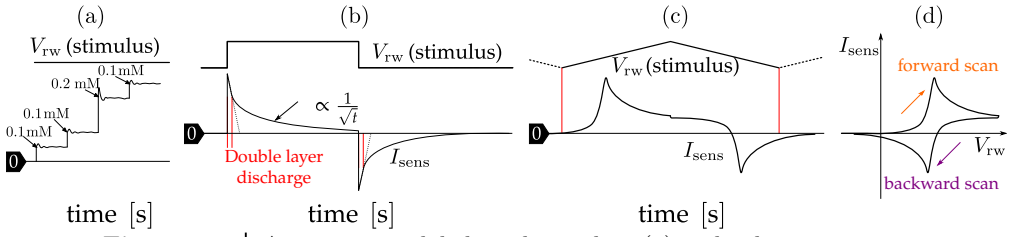

Figure 1.6 Amperometry labeling the analyte (a) and voltammetries including chronoamperometry (b), current-time CV (c) and current-potential CV (d).

Fig. 1.6(a) shows a typical amperometric measurement response to successive addition of a target analyte. Here, the sensor current is measured as a function of time for a constant stimulus voltage V_{rw}. Fig. 1.6(b), (c) and (d) represent the potential functions and current responses corresponding to voltammetric techniques. In a simple potential step experiment, also called chronoamperometry, the transient current at the WE is monitored while V_{rw} is stepped to the measurement potential, as sketched in Fig. 1.6(b). During the first part of the experiment, the current corresponds to the charging or discharging of the electrical double layer. Depending on the electrode size, material and structure, this charging current may last for up to several milliseconds, during which the underlying Faradaic current is much weaker and hard to detect. Once the double layer is discharged, the remaining current corresponds to Faradaic processes and can be measured more safely. Another well-established voltammetric method is called cyclic voltammetry (CV). In this method, the stimulus varies in the form of a triangle waveform instead of a step while the current response I_{sens} is recorded, as indicated in Fig. 1.6(c). However, I_{sens} is normally viewed as a function of V_{rw} instead of time, as recorded in Fig. 1.6(d). Therefore, the potentials at which the redox occur, indicated by the forward and reverse current peaks, respectively, may be easily discerned. The analysis of these current responses also provides qualitative information about electrochemical reactions, allowing to analyze the electrochemical sensors performance and offering rapid location of the redox potentials of the analytes. The scan rate also provides access to additional information in the time domain.

An important validation parameter for the measurement of electrochemical signals is called the LOD. In terms of magnitude, LOD is formally defined as:

$$y_{LOD} = y_{blank} + k\sigma_{blank}, \tag{1.3}$$

where y_{blank} is the mean value of replicates of blank (sample identical to the one to be measured but without analyte) measurements, σ_{blank} is the standard deviation

of the blank signal and $k = 3$ ensures, with a confidence level of 99.86 %, that the lowest concentration of analyte signal is equal or bigger than the blank plus three times the standard deviation of the blank signal.

1.3 State-of-the-Art CMOS ROIC

After the sensor transduces electrochemical information into the electrical domain, the corresponding signals can be measured by electronic systems that also provide the potentiostatic biasing levels to drive the electrochemical reactions. These read-out systems can be fabricated in standard CMOS processes, improving reliability and reducing cost, power and size. Consequently, most of the recent electrochemical sensory systems are designed in CMOS technologies, and thus, this state-of-the-art study is limited to this scope.

Smart CMOS ROICs for amperometric sensors are required to fulfill the three main functions defined as follows: (i) potentiostatic biasing, to set the cell operating voltage V_{rw}; (ii) current read out, to measure the readox current I_{sens}; and (iii) digitalization function, to provide built-in analog to digital (A/D) conversion.

1.3.1 Potentiostatic Operation

Three-electrode potentiostat configurations are usually divided into two categories [2]: floating-WE and fixed-WE. The fixed-WE topologies, as depicted in Fig. 1.7(a), are the most popular configuration and have been widely used [10, 36, 8, 37, 38, 11, 39] because of its simplicity. The purpose of the voltage follower A_1 is to accomplish the potentiostatic control, i.e avoid any current flowing through electrode RE and set the potential V_{rw} at RE. The output of A_1 is connected to CE and the electrochemicall cell provides a path to the WE potential for the further measurement of the sensor current I_{sens}. On the contrary, in the floating-WE scheme, CE is fixed at a constant potential and the sensor current is sensed through CE, as shown in Fig. 1.7(b). This configuration is more complex and rarely used [2, 40], since the potentials at RE and WE can both vary with time, requiring of circuitry to ensure that V_{rw} is equal to the applied V_{pot}. However, floating-WE may improve the current measurement in cases in which shielding and screening the WE connection from external electromagnetic interference (EMI) are needed [2].

The potentiostats of Fig. 1.7 are single-ended topologies, so the progressive supply-voltage downscaling of modern CMOS technologies can dramatically limit the full scale of the programmability applied at V_{rw}. In order to address this issue, the fully-differential potentiostat of Fig. 1.8 has been proposed [3]. In contrast to

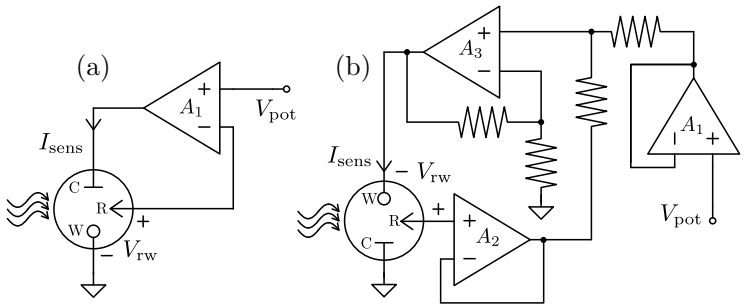

Figure 1.7 | Single ended fixed-WE (a) and floating-WE (b) potentiostat circuit topologies [2].

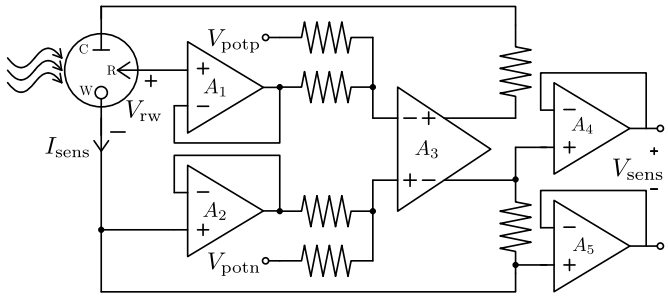

Figure 1.8 | A fully-differential fixed-WE potentiostatic with I/V conversion [3].

single-ended circuits, fully-differential potentiostats can dynamically control the voltages on both the RE and WE to ideally double the V_{rw} full scale for the same supply voltage. However, this solution comes at the cost of more Silicon area, power consumption and design complexity.

1.3.2 Electrochemical Current Read-Out

In a three-electrode amperometric sensor, the current flowing in CE is the same but in opposite direction than the current flowing through WE. Therefore, the current readout block can be adopted for potentiostats using either the fixed-WE or the floating-WE architectures.

Several IC implementations exist for measuring the cell current. The use of a transimpedance amplifier (TIA) for an intermediate current-to-voltage conversion is the most common solution [4]. In this approach, the TIA sets a virtual potential

at the WE (or at the CE when a fixed-CE architecture is employed) and converts I_{sens} into an equivalent readout voltage (V_{sens}).

In the resistive TIA shown in Fig. 1.9(a), the operational amplifier develops the required V_{sens} such that the current from the sensor flows through the feedback resistor R_{f}. Nevertheless, this method demands extremely large values of R_{f} (>10 MΩ) for the measurement of very low currents, which should be avoided since R_{f} integration would be too expensive in terms of Silicon area. The use of off-chip resistors is feasible, but it comes at the cost of extra pads. Also, the current in the feedback loop may decrease to the point that it becomes comparable with the input bias current of the operational amplifier, causing non-linearities. In addition, lower resistor values results in higher input referred current noise. It has been reported in [41] that this TIA can only achieve an accuracy in the nA-range for 10-kHz bandwidth.

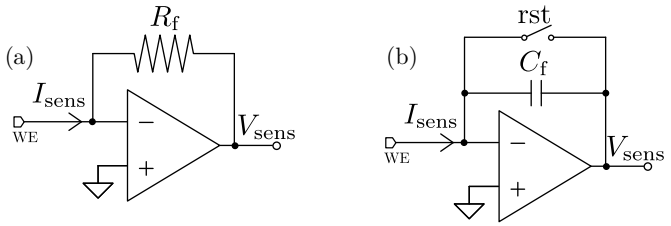

Figure 1.9 | Resistive (a) and capacitive (b) TIA for current-to-voltage readout. [4]

A higher sensitive readout can be achieved by replacing the resistive feedback element in the feedback with a capacitor (C_{f}), as shown in Fig. 1.9(b). Basically, the feedback capacitor C_{f} is charged during a fixed integration time T_{int} by the current to be measured I_{sens}. Under almost direct current (DC) operation (i.e. sampling frequencies higher than sensor bandwidth) the output voltage V_{sens} is proportional to the integration time and the input current following:

$$V_{\text{sens}} = -\frac{T_{\text{int}}}{C_{\text{f}}} I_{\text{sens}}. \tag{1.4}$$

The use of a capacitive element allows to reduce the area occupation of the current-to-voltage (I/V) interface as capacitor size can be downscaled through integration time when measuring small currents. Furthermore, CMOS capacitors benefit from better linearity and less process, voltage and temperature (PVT) variations respect to resistive devices. However, a sustained current would soon saturate the integrator, so some sort of reset strategy is needed [10, 36, 6, 42–44, 5]. A classic capacitive-based readout that also performs correlated double sampling (CDS) is shown in Fig. 1.10 [36, 6, 5]. The scheme in (a) features a programmable gain amplifier (PGA) built around A_2. Here, during the reset phase ϕ_1, circuit noise

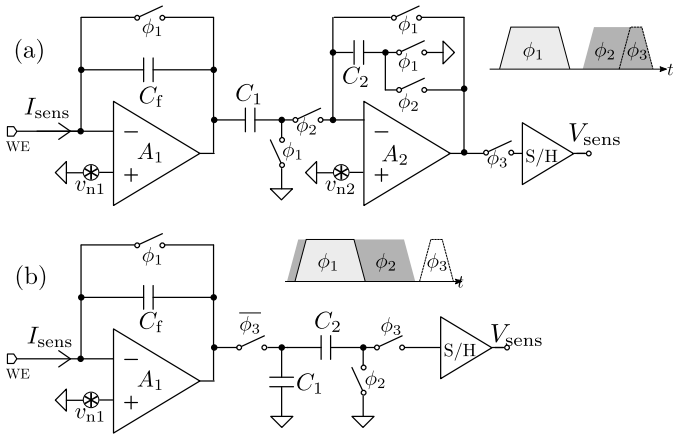

Figure 1.10 | Capacitive TIA readout with built-in CDS with (a) [5] and without (b) [6] PGA.

sources v_{n1} and v_{n2} are sampled respectively onto C_1 and C_2. In the integration phase ϕ_2, the signal follows the integration and the amplification stages together with the curent values v_{n1} and v_{n2}, which now contributes with the opposite sign. Noise sample differentiation of the CDS techniques is thus readly implemented. At the end of ϕ_2, the sample and hold (S/H) phase ϕ_3 delivers the processed output V_{sens} to the following A/D stage. Scheme (b) follows the same philosophy as (a) but without PGA stage [45]. While capacitive-based readout chains offer the switching frequency as a valuable degree of freedom to the designer, specially to avoid integration of large resistors on chip, the achievable resolution is affected by several issues specific to switched-capacitor (SC) circuits, such as: switch noise (kT/C) folding, amplifier noise, charge injection, clock feed-through and reset switch leakage at the integrator stage. Noise folding can be cut down by setting relatively large values of C_1 and C_2. As detailed in [46] and references therein, amplifier noise can be embodied into kT/C noise as a form of excess noise that can be limited by a proper design. In practice, values of C_f in the order of 100 fF are sufficient to make kT/C noise contributions smaller than the subsequently analog-to-digital converter (ADC) resolution. Charge injection and clock feed-through can be reduced through fully-differential architectures, dummy switches [47] and advanced layout techniques [48]. Leakage of the reset MOS switch can be limited to sub-fA range by using specific switch configurations [49].

Another well-known amperometric readout technique is based on current mirror amplifiers [7, 8, 38, 50–54], such as those shown in Fig. 1.11. The idea is to interpose a circuit in the path of the sensor to generate a copy of the sensor current

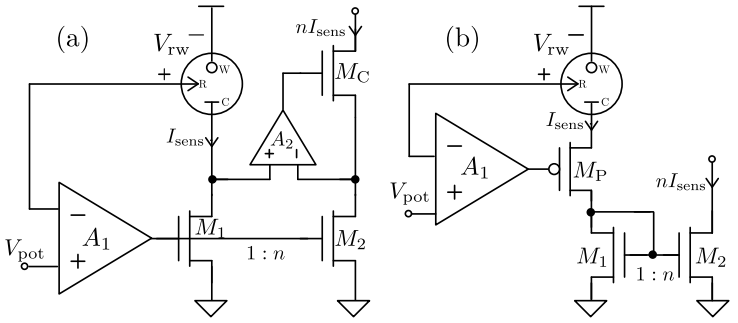

Figure 1.11 | Current-mirror based readout circuits with NMOS current buffer (a) [7] and PMOS BDI (b) [8].

and thus, measure the copied current instead of the sensor current itself. It can be performed either by passing the current through a resistor or by integrating the current through a capacitor. Current-mirror readout circuit can be very compact since only few transistors are used for current measurement, whereas in the previous implementation, at least one capacitor or resistor and one operational amplifier are used. Moreover, the power consumption is expected to be lower than that of the previous circuits, since the operational amplifier does not need to provide a large output current. The added current consumption is equal to the mirrored sensor current, which can be negligible for low aspects ratios. However, mismatch in the mirror transistors may cause gain uncertainty. Additionally, these current mirrors only measure the sensor current in one direction, requiring extra circuitry for bidirectional measuring. In Fig. 1.11(a), the mirror is embedded in the amplifier, and current is precisely copied with the help of an auxiliary amplifier A_2 and a regulated cascode transistor M_{C} [7]. The sensor current is amplified thanks to the geometrical scaling factor n of the current mirror. The large double-layer capacitance of the electrode interface C_{dl} makes the dominant pole of this loop. For the purpose of achieving good loop stability, the first non-dominant pole (i.e. from A_1) is pushed to high frequencies. Stability could be further enhance by introducing a left-half plane (LHP) zero in a feed-forward signal path around M_1, as proposed in [8]. Configuration in Fig. 1.11(b) employs a p-channel MOS (PMOS) transistor M_{P} acting as a common drain stage rather than a common source stage, thus providing buffered direct injection (BDI) between the control loop and the current mirror to improve stability. While both topologies are attractive for high-bandwidth applications and for compactness, noise performance can be of concern since 1/f components of M_1 and M_2 are not filtered through the impedance of the sensor and they sum up directly to I_{sens}.

1.3.3 Digitization Circuits

On smart electrochemical sensory systems, the analog voltage waveform from the analog frontend (AFE) needs to be A/D converted. Many customized ADCs arquitectures have been used for the digitalization of amperometric signals, such as:

1. Current to frequency (I/F) ADCs [8, 6, 52, 54–58, 9]
2. Integration ADCs [10, 49, 59–61]
3. Successive approximation register (SAR) ADCs [62]
4. Delta-Sigma moduladors [11, 50, 51, 60, 63, 12].

In current-to-frequency (I/F) modulators, the readout current is converted into a square-wave signal whose frequency is proportional to the sensed current amplitude. The topology of Fig. 1.12 [9] performs the I/F conversion through a simple relaxation oscillator constraining V_{c} between $V_{\mathrm{ref,H}}$ and $V_{\mathrm{ref,L}}$. Here, I_{sens} is injected into the I/F modulator through a current-mirror based readout, such as those in Fig. 1.11. Basically, capacitor C is alternatively charged and discharged by the sensor current I_{sens} and a constant current I_{ref}. As a result, the timing of the pulse width modulator (PWM) can be written as:

$$T_1 = \frac{CV_{\mathrm{DD}}}{2I_{\mathrm{sens}}} \qquad \text{and} \qquad T_2 = \frac{CV_{\mathrm{DD}}}{2I_{\mathrm{ref}}}. \tag{1.5}$$

Hence, the ratio of the two duty cycles is linear with the sensed current and independent from PVT deviations:

$$\frac{T_2}{T_1} = \frac{I_{\mathrm{sens}}}{I_{\mathrm{ref}}}. \tag{1.6}$$

The dual-slope configuration in Fig. 1.13 proposes an I/V conversion employing a capacitive-based TIA stage, whose input is fed atlernatively by the I_{sens} current and a reference discharge current I_{ref}. During the integrating phase, I_{sens} charges C_{f} either to cause a positive or negative ramp of V_{C}. The total integrated charge is $T_{\mathrm{int}}I_{\mathrm{sens}}$. At the end of this phase, the comparator decides the polarity of I_{sens} in order to determine if I_{ref} needs to be sourced or sinked during the controlled discharge phase. A digital counter, embedded in the digital control backend, starts to run until the comparator reverts to its initial state. At this point, I_{ref} stops integrating onto C_{f}, thus the charge variation during this phase is $T_{\mathrm{dis}}I_{\mathrm{ref}}$ in magnitude, and its sign is opposite with respect to the charge accumulated during integration.

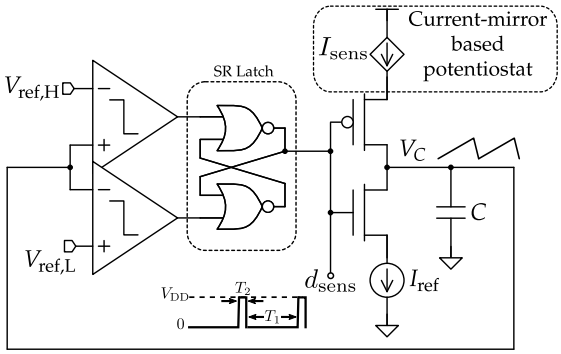

Figure 1.12 | I/F ADC for amperometric readout [9].

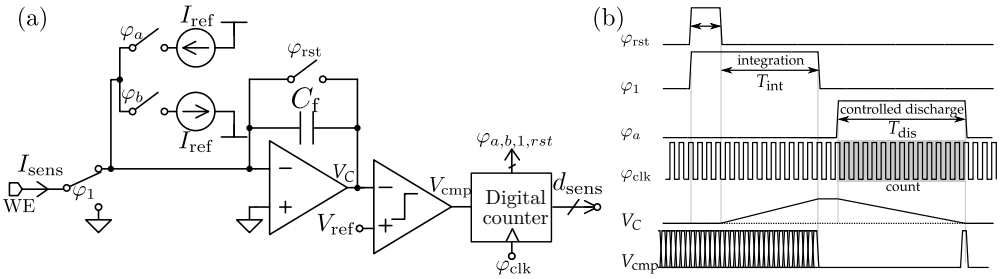

Figure 1.13 | Dual-slope ADC for amperometric readout topology (a) and operation (b) [10].

Since the comparator triggers at the same voltage level, the net charge change over C_f in the current conversion cycle is zero ($T_{int}I_{sens} = T_{dis}I_{ref}$), and the counter output can be represented by the digital value of:

$$d_{sens} = f_{clk}T_{dis} = f_{clk}T_{int}\frac{I_{sens}}{I_{ref}}. \tag{1.7}$$

Among high-resolution ADCs arquitectures, ΔΣMs tend to give the best performance while remaining compact and consuming only micro-Watts of power. Oversampling ΔΣMs are particularly well suited to measure slow electrochemical signals because their internal quantization noise shaping can be fully exploited [64]. Indeed, high signal-to-quantization-noise ratio (SQNR) in the bandwidth of interest (typically Hz range) can be achieved since the ΔΣM loops pushes most of this noise contributions to high frequencies.

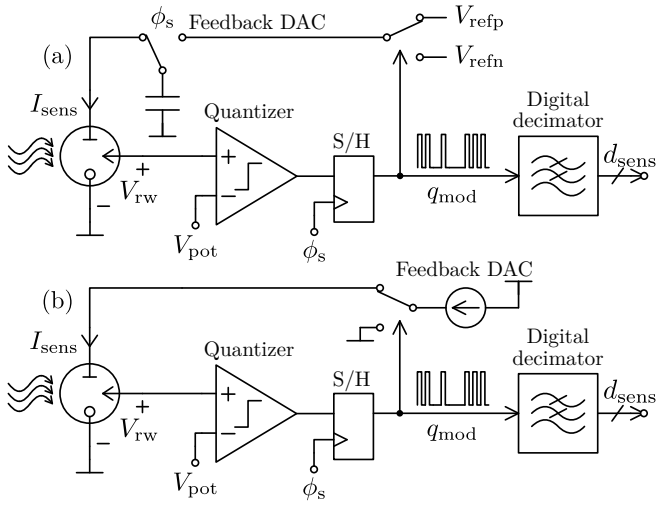

Figure 1.14 | DT (a) [11] and CT (b) [12] potentiostatic-amperometric ΔΣM based on the sensor-in-the-loop concept.

Important power savings can be foreseen by the fusion of the potentiostatic AFE and the amperometric ADC stages. An interesting concept related to this target scenario is the reuse of the sensor dynamics inside the ΔΣM for implementing the quantization noise shaping itself. This sensor-in-the-loop idea has been already applied to thermal [65], MEMS [66] and piezoelectric [67] sensors. In the case of electrochemical sensors, previous attempts have relayed on single-bit first-order ΔΣMs using the electrode-electrolyte capacitance C_{dl} for noise shaping, like in Fig. 1.14, with either discrete time (DT) switched-capacitor feedback [11] or continuous time (CT) current feedback [12]. Unfortunately, these minimalistic ΔΣMs suffer from quantization noise correlation, idle tones and poor potentiostatic linearity due to signal dependent gain of the single-bit quantizer [64].

A performance summary of state-of-the-art potentiostatic CMOS ROICs for electrochemical sensors is provided in Table 1.2. The ΔΣM based potentiostats tend to have the best signal-to-noise-and-distortion ratio (SNDR) values of any class of ADC architecture while remaining compact with a remarkable low-power operation. In terms of potentiostatic range, the differential control of [3] demonstrates that the potentiostat programmability can be extended beyond the supply voltage limit.

	[68]	[3]	[10]	[69]	[11]	[12]	[8]	[70]	[71]	[72]	
ADC architecture	Analog output	Analog output	Dual Slope	I/F off-chip	SC CT ΔΣM	SI CT ΔΣM	I/F	SAR	Async ΔΣM	Dual Slope	
AFE architecture	Current conveyor	- -	Capactive TIA	- -	Sensor-in-the-loop	Sensor-in-the-loop	Current mirror	Resistive TIA	Capactive TIA	Capacitive TIA	
Technology	5000	180	250	180	600	2500	180	65	180	350	nm
Supply voltage	±5	1.8	2.5	1.8	5	5	1.8	2.5	1.8	1.2	V
Pot. range	-	3.2	1.25	0	4	3	<1.8	<2.5	<1.8	<1.2	V
Full scale	0.1 to 3.5	-	±0.25	±11.6	±0.1	+2 to +32	-	-	±10	±0.01 to ±1	μA
Sensitivity	100	0.02	0.24	-	-	-	1	-	0.01	0.01	nA_{rms}
Bandwidth	-	500	2500	100	10	2	-	<2	1.8	0.5	Hz
Sampling Rate	-	-	2.5	-	125	1	-	0.002	-	0.125	kHz
$SNDR_{max}$	-	63	54	<50*	68	71	-	-	-	77	dB
Dynamic range	31	63	56	155	68	71	120	-	160	97	dB
Num. of channels	2	-	16	-	24	1	1	3	1	4	
Area	0.53	-	0.9	0.09	0.03	6.4	0.02	3	0.2	-	mm^2
Power	<2000	15800	>10000	5220*	1040	25	70	15000	295	48	μW
Target	Glucose	Dopamin	DNA	Alamethicin	DNA	$Fe(CN)_6$	Glucose	-	-	$Fe(CN)_6$	

Table 1.2 Performance comparison of state-of-the-art potentiostatic-amperometric CMOS ROICs.
*without including off-chip ADC

1.4 Flexible Hybrid Electronics

During last decade, some sensory electronic platforms have started their mutation from traditional rigid and rectangular printed circuit boards (PCBs) towards more elaborated structures such as flexible, stretchable and bendable substrates [73–76]. By taking advantage of the latest printed electronics techniques, these new hybrid electronics enable large-area low-cost applications that can be manufactured in high volumes [77, 78]. However, flexible printed electronics developments are still in early stages, and they present important drawbacks whose improvement is challenging, like short lifetime, high-power consumption and low speed. On the other hand, CMOS ICs are much more reliable and performing, but with higher costs and larger design cycles. Flexible hybrid electronics (FHE) come to merge rigid ROICs, supplying the required smartness, with printed electronics, capable of customizing low-cost large-area stretchable devices, leading to flexible, cost-effective and powerful sensory electronics platforms. An interesting strategy is the usage of tiny bare IC dice directly attached to these printed electronics. Although these tiny ROICs are still rigid, their small size maintains flexibility at any realistic bending radius. Furthermore, the small-area Silicon die together with the wire-bonding free direct attachment of these ROICs tend to keep the costs of the CMOS fabrication and packaging at the same level as of the printed electronics part. In practice, sensors may be made by printed electronics alone, where ROICs allow the signal conditioning and data processing. Fig. 1.15 illustrates an example of electrochemical flexible hybrid electronics (FHE) for sensing applications, where several printed electronic components and a rigid ROIC, as a bare die, become hybrid on a single flexible substrate. In this FHE example, the large-area devices, such as sensors, energy harvester, passive components and antennas are realized by printed electronics, while the intelligent functions such as precision readout, power management and high performance computation circuits are integrated by compact and low-power CMOS technologies in the ROIC.

1.4.1 Printed Electronics

Methods for printed electronics include, but are not limited to, screen printing [79], gravure [80], offset printing [81], flexographic printing [82], and inkjet printing [83]. These technologies are eminently being developed to promote scalable and effective electronic manufacturing [84]. The selection of the printing method is fundamental to obtain the optimum hybrid solution for each application case. In the sensory field, the emergence of wearable flexible devices has spread the use of screen printing and inkjet printing technologies [85]. For this reason, only these two printing technologies will be considered in this thesis.

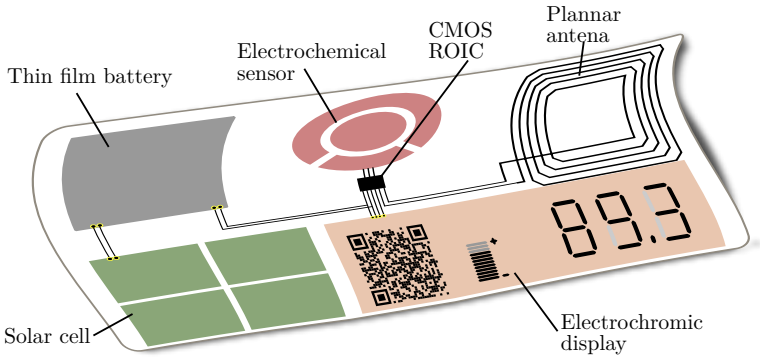

Figure 1.15 | Typical building blocks of a flexible hybrid system.

Inkjet printing is one of the fastest growing techniques reported in literature [83, 86]. With the virtue of its low cost, high resolution, increased scalability, and potential to meet the rising market demand for customized FHE solutions, inkjet printing is expected to be one of the leading technologies in the printed electronics market. Some of the major benefits of this technique are contactless procedure, minimum-size features, flexibility on ink composition and reproducibility. In inkjet printing, a bitmap geometry stored in a digital format is transferred to the substrate following an additive process by the accurate deposition of materials through a micrometer sized inkjet nozzle head, without the use of masks and without any contact between the print head and the substrate. Generally, the most prominent mechanisms for actuation of inkjet nozzles is the drop-on-demand (DOD) piezoelectric inkjet system [73], shown in Fig. 1.16(a). This method loads and expels ink based on the applied bias. Since each drop can be controlled in real time, ink consumption is extremely low. No special processing conditions are required. Inkjet printing distinguishes itself for being a one-step process, with a simple functional principle. Drawbacks of inkjet compared to other methods are related to the speed. The raster motion process and possible clogging of the nozzles may slow down the printing process [87].

As a potential alternative, screen printing is a fast high-volume printing technique. Screen printing is a stencil-like process where the desired pattern is placed in a fine mesh material stretched over a frame, leaving the pattern open and blocking off all unwanted areas. Ink is deposited on one edge of the pattern and a rubber-edged tool called squeegee, push the ink through the holes in the mesh, transferring the pattern onto the substrate, as shown in Fig. 1.16(b). Thickness is generally on the order of dozens of μm and it is usually determined by several parameters,

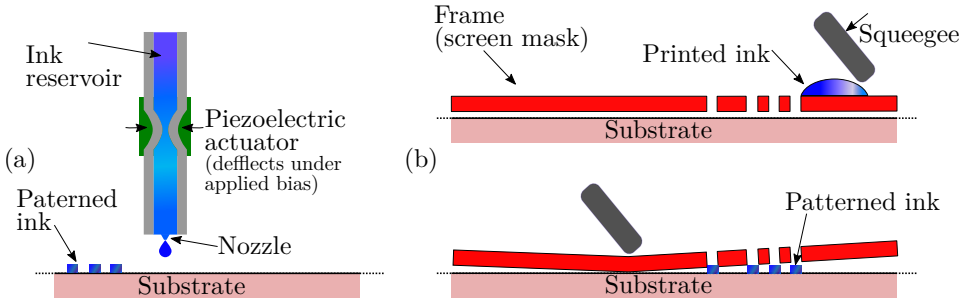

Figure 1.16 | Simplified schematics of DOD inkjet (a) and screen (b) printing techniques.

such as ink viscosity, squeegee pressure, and mesh height. Screen printing may be a great choice for printing interconnects and passive circuit elements such as resistors, capacitors, and inductors. However, screen printing is not suited for early prototyping work because changing the design requires purchasing a new custom screen.

1.4.2 Flexible Substrates

The most common substrates for flexible printed electronics are plastic (polymer) films, such as polyethylene terephthalate (PET) and polyethylene naphthalate (PEN) [73, 74]. These substrates present many advantages that make them appropriate for high-performance printed electronics: low cost, variety of thicknesses, very low surface roughness (typically nm-range), good optical transmittance, mechanical flexibility, and toughness. Nevertheless, plastic substrates are temperature sensitive. Considering that any target FHE requires of chip bonding to the printed substrate, a relatively high temperature is demanded if solder is used for this purpose [88]. Solder reflow temperature can be as high as 204 °C for SnPb, which is above the glass-transition temperature of PET. The heat capability improves for PEN and much more for Kapton polyimide (PI), at the cost of transparency losses, larger surface roughness and more expensive fabrication. There are other options of flexible substrates for printed electronics, such as paper. The major benefit of paper substrates is their low cost and that are environmental friendly thanks to their biodegradability. The challenge of using paper arises from its porous, permeable and roughness surface. Also, the complex surface chemistry and absorptive nature further complicate its usage [89]. Silicone elastomers polydimethylsiloxane (PDMS) are also favorable as stretchable and flexible substrates. Table 1.3 summarizes the main properties of the above flexible substrates.

Substrate	PEN	PET	PI	Paper	PDMS	
Thickness	12 to 250	16 to 100	12 to 125	20 to 250	5 to 1500	μm
Transparency	90	87	-	-	92	%
Transition temperature	80	120	410	-	125	°C
Process temperature limit	120	155	300	130	-	°C
Young's modulus	2.8	3	2.5	0.5 to 3.5	0.57 to 3.7	GPa
Density	1.4	1.4	1.4	0.6 to 1	125	g/cm^2

Table 1.3 | Comparative characteristics of flexible substrates compatible with printed electronics.

1.4.3 Flip-Chip Bonding

IC assembly technologies have a growing demand for innovation at the same pace as the evolution of the chips themselves. For a long time, wire bonding techniques [90] have been the main stream to create the interface between chips and substrates. However, with the upcoming trends of system integration in terms of miniaturization and complexity (number of chip pads) alternative assembly schemes are extensively demanded. Among these techniques, flip-chip bonding can be considered as the key enabler for fine-pitch hybrid electronics [91]. The name of flip-chip refers to the joining process that involves face down bonding of chips to substrates. In contrast to wire bonding, flip-chip bonding offers many advantages, like a wider variety of substrates, better noise control, shorter possible leads, smaller device footprints and higher density. In addition and thanks to the direct interconnection between die and substrate, issues related to the parasitic inductance and capacitance associated with bond wires are minimized.

The common way of converting a wirebond die into a flip-chip die generally requires a redistribution layer (RDL) in order to redistribute the I/O pads to bump pads without changing the I/O pads placement. As shown in the cross section of Fig. 1.17, RDL is an extra metal layer consisting of wiring on top of core metals that makes the I/O pads of the die available for bonding out other locations such as bump pads. The typical flip-chip assembly is formed via the solder bumps between the chip and substrate by reflowing the solder [92], as shown in Fig. 1.18. In this process, the dice are flipped and positioned so that the solder bumps are facing the conductive bond pads on the substrate following Fig. 1.18(a). The solder bumps are then remelted, typically employing hot air reflowing as in Fig. 1.18(b). After the chip is assembled, an electrically insulating adhesive if dispensed into the gab between the chip and the substrate to achieve Fig. 1.18(c). However, these solder materials cannot be applied to temperature-sensitive components, such as low-cost

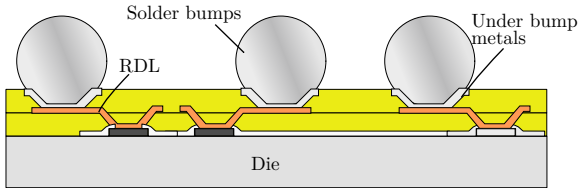

Figure 1.17 | Cross section of a typical flip-chip die with RDL.

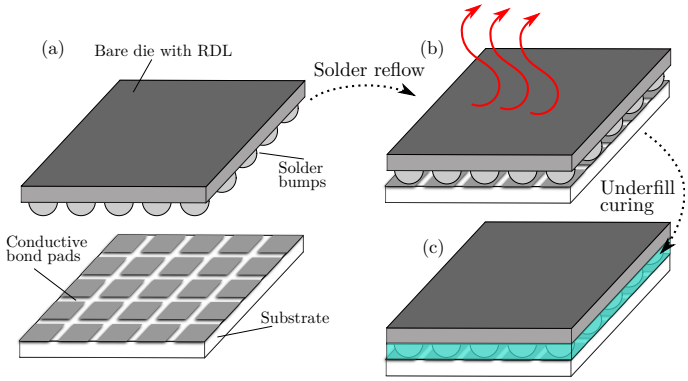

Figure 1.18 | Typical flip-chip process flow: dice alignment (a), reflowing (b) and refilling (c).

flexible substrates, since the solder reflow process is performed at a relatively high temperature. Consequently, the bonding methods of interconnection formed by curing are widely used for temperature-sensitive components.

Flip-chip bonding using anisotropic conductive adhesives (ACAs) has been utilized for decades in the area of glass substrates [93, 94]. Over the past few years, a growing interest in utilizing this technology on flexible substrates has emerged. Indeed, ACAs are promising materials for their low temperature process, simple, lead-free, ultra-fine capability as well as low-cost assembly processes, because they do not require of soldering and underfill processes [95–98]. They are also called z-axis conductive adhesives for the reason that they are conductive between the pads of the chip die and substrate in the vertical direction and nonconductive in the horizontal direction. ACAs are thermocompression bondings and they usually consist of mixtures of Au, Ag, Ni, or Au/Ni spherical conductive particles of 3 μm to 20 μm in size, which are randomly dispersed throughout an insulating polymeric matrix resin with a filling ratio of 5 % to 20 %. The anisotropic electrical conductivity of ACAs comes from the trapped conductive particles between the conductive pads on the die IC and the corresponding pads on the substrate. The density of particles

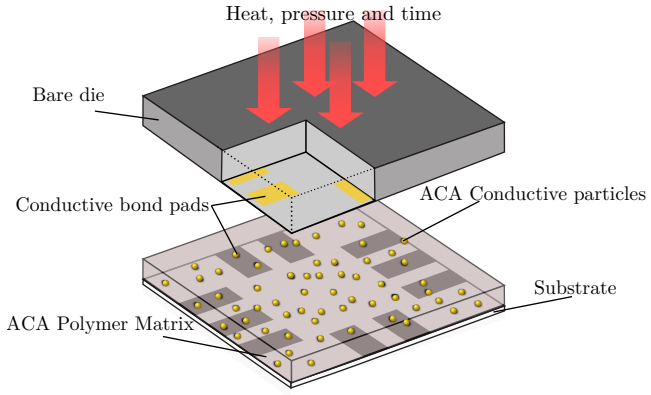

Figure 1.19 | Typical ACA-based flip-chip assembly.

is controlled in such a manner that just sufficient particles are present to guarantee reliable electrical conductivity in the z-direction, while concentration is much lower than a critical value to complete a conduction path in the x–y plane [99].

Fig. 1.19 illustrates the typical flip-chip assembly process of ACAs. First, a layer of the ACA is deposited between the die and the substrate. Electrical conduction between the adherents is achieved through the conductive particles when heat and bonding pressure are applied together. The die and substrate are mechanically bonded through the resin matrix of the ACA. Once it is cured, the external pressure can be removed.

1.4.4 FHE Applications

There are many application examples of FHE in recent published literature, particularly in the areas of wearable health, industrial and environmental monitoring. Nevertheless, most of the applications are making use of a great number of discrete electronics components, which may occupied extra available area and demand higher power consumption compared to application specific integrated circuits (ASICs). The work in [100] reports a wireless health monitoring approach with discrete circuit components. It consists of inorganic stretchable wires for flexible and stretchable electronic circuits in a thin PDMS substrate that can softly laminate onto the surface of the skin for physiological monitoring. The wearable electrocardiogram (ECG) monitor of [88] is another example of FHE implementation, where inkjet printing sensors are integrated with discrete circuit components on a PI substrate. In the prototype of [101], printed electronics components are deposited on a flexible 50μm-thick polyimide substrate along with an IC fabricated in

standard 130-nm CMOS technology. The assembly is then achieved through sheet lamination and a noncontact electrical interfacing through inductors and capacitors [102]. However, the interface requires careful engineering and challanges new innovations for enabling efficient coupling through the subsytem architectures. A smart wristband in [103] integrates an array of biochemical sensors in one sensor platform and performes amperometric and potentiometric measurements to monitor potassium, glucose, lactate and sodium concentrations in sweat. Here, the sensor array is connected to a PCB that hosts surface mount components to process and transmit the sensor data over Bluetooth. However, flexible PCB solutions have limitations such as low flexibility, non-transparency and high cost. The interconnects are not printed but are usually etched from a laminated copper sheet using photolitography. In [104] a custom "cut-solder-paste" laminating process is proposed to overcome the difficulties of soldering directly on polymer substrates. They use tattoo form factor electrodes with discrete electronics components for monitoring ECG and skin hydration. The system implements a NFC protocol for transmitting sensor data.

Table 1.4 provides an overview of the literature on printed electrochemical sensors for FHE applications, where healthcare monitoring shows to be the biggest application area. Flexible and stretchable printed electronics can mold to the shape of the body in a manner that the rigid electronics cannot. Most of such printed sensors take the advantage of the inkjet or screen printing techniques, and some combine both of these cost-effective techniques.

REF	**Sensor Type**	**Main Target**	**Printing**	**Substrate**
[105]	Capacitive Pressure	Breathing + Heart rate	SPT	PDMS
[106]	Capacitive Pressure	Human skin	IPT	PEN
[107]	Optical	Electromagnetic spectrum	IPT	PI
[108]	Humidity	–	IPT	PI
[109]	Gas	Ammonia	SPT + IPT	PET
[88]	Potentiometric	ECG	IPT	PI
[110]	Electrochemical cell	H_2O_2	IPT	Paper
[111]	Electrochemical cell	Polyphenolic antioxidants	SPT + IPT	PET
[112]	Electrochemical cell	Glucose	IPT	PDMS
[113]	Electrochemical cell	Glucose	SPT	Paper
[114]	Electrochemical cell	TMPD	SPT	PET
[114]	Electrochemical cell	Cholesterol	SPT + IPT	Polyester
[115]	Electrochemical cell	Human papillomavirus	SPT + IPT	Polyurethane

Table 1.4 | Comparison of state-of-the-art sensors based on flexible printed electronics.

1.5 Objectives and Scope

The main objective of this thesis is to develop a disposable electrochemical sensing smart device that combines the best profits of printed electronics on plastic flexible substrates with the performance of novel low-power reconfigurable CMOS ROICs. The proposal is to provide a very attractive alternative and versatile technology for the new emerging electrochemical applications in fields such as wearable health, industrial and environmental sensing.

The working hypothesis of this PhD thesis is that all the electronic frontend smartness required by an electrochemical sensor (i.e. potentiostatic control, amperometric readout, A/D conversion, power management and standard digital interface) can be embedded in a μW-range mm^2-size CMOS IC, which in turn can be directly attached to a flexible substrate where the sensor is printed. The goals demanded to fully verify the above working hypothesis are summarized in the following expectations statements:

- Experimentation with state-of-the-art electrochemical sensors to discern the behavior and limitations of electrochemical cells. Deep understanding and modeling of the transducer operating principle may allow to exploit its use not only for sensing but also for signal processing.
- Proposals for new specific $\Delta\Sigma$ modulator ($\Delta\Sigma$M) architectures that should allow the fusion of the potentiostatic AFE and amperometric ADC, the reduction of the circuit flicker noise impact and also the extension of potentiostatic programmability beyond the supply voltage.
- Design of ROICs for electrochemical sensors incorporating the above architectures and all necessary auxiliary functions using low-power and compact CMOS analog and mixed-signal circuits.
- Integration of the ROIC designs in two CMOS nodes of different nominal supply voltage in order to demonstrate the technology scalability of the proposed $\Delta\Sigma$M architectures and related circuits.
- Experimental validation of the developed ROICs both electrical and electrochemial levels with a variety of procedures (e.g. amperometry and voltammetry).
- Exploration of low-cost ROIC assembly and sensor printing techniques on flexible substrates towards true disposable smart electrochemical devices.

The document of this PhD thesis is structured as follows:

- **Chapter 1** has already introduced the motivation, the required background in terms of state-of-the-art electrochemical sensors, CMOS readout circuits and flexible hybrid electronics, as well as the target objectives.
- **Chapter 2** describes in detail how potentiostatic AFE and the amperometric ADC stages can be fused by using CT $\Delta\Sigma$Ms. Novel architectures based on this concept are described at system level with the aim of improving the overall performance in terms of noise impact and potentiostatic range. A discrete circuit implementation as an initial proof of concept is presented.
- **Chapter 3** collects these novel electrochemical $\Delta\Sigma$M architectures and presents their low-power and compact circuit implementation in two distinct CMOS technologies.
- **Chapter 4** proposes a single substrate disposable FHE solution to exploit and merge the ROIC capabilities of the electrochemical $\Delta\Sigma$M and the benefits of the low-cost inkjet printing technology.
- **Chapter 5** validates the manufactured CMOS ROICs not only at electrical level but also electrochemically and it compares to state-of-the-art frontends. Finally, the disposable smart electrochemical sensor of Chapter 4 is presented and electrochemically validated.
- **Chapter 6** summarizes the contributions arising from the results and points towards possible future work.

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  SNF Sinergia 177255 funding.
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- IP4SS:
  IP-blocks for Smart Sensors Bloques IP para Sensores Inteligentes.
  IMB-CNM (CSIC) funding.

The Potentiostatic Amperometric Delta-Sigma Modulator | 2

As discussed in the previous chapter, conventional amperometric ROICs consist of a potentiostat, as the AFE, followed by an ADC. This chapter discusses in detail how both of these two functions can be merged using CT Delta-Sigma modulators by reusing the sensor dynamics inside the $\Delta\Sigma$M loop for implementing the quantization noise shaping. Furthermore, novel architectures based on this concept are presented and further analyzed.

The current chapter is structured as follows. First, design considerations of such electrochemical *sensor-in-the-loop* $\Delta\Sigma$Ms at system level are introduced, placing emphasis on stability, signal-to-noise ratio (SNR) and potentiostatic performance. Then, a proof of concept is built in discrete electronics as a preliminary validation of the architecture. Finally, the design of a novel mixed electrochemical-electronic CT $\Delta\Sigma$M is presented, with the aim of extending the potentiostatic range and the amperometric LOD.

2.1 Mixed Electrical-Electrochemical Noise Shaping

2.1.1 Sensor-in-the-Loop Concept

The reuse of the sensor double-layer capacitance C_{dl} inside the $\Delta\Sigma$ loop as an integrator stage for noise shaping leads to a very elegant and compact circuit implementation: not only it naturally adapts the bandwidth of the system to the

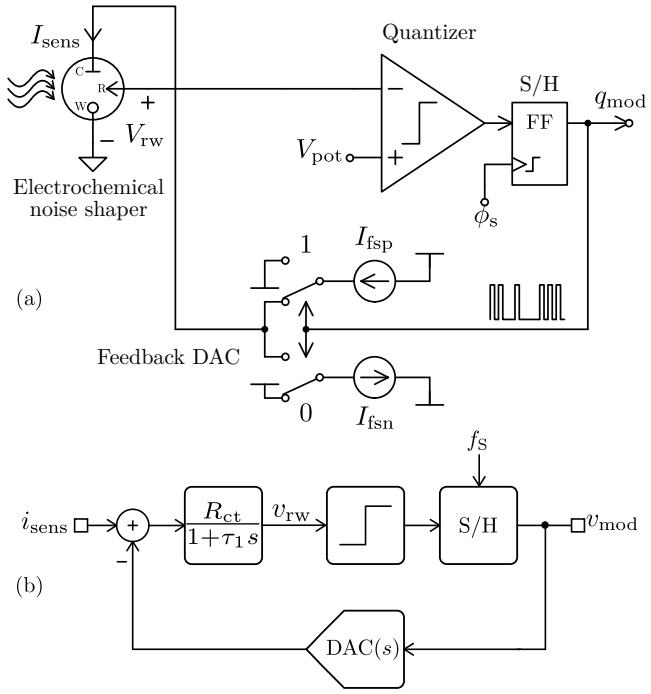

Figure 2.1 Fixed-WE potentisotatic-amperometric single-bit first-order CT sensor-in-the-loop ΔΣM architecture (a) and equivalent signal processing model (b).

speed capabilities of the electrochemical sensor (i.e. self anti-aliasing), but it also avoids the need for an active electronic integrator. Fig. 2.1 presents the architectural description of this concept.

Basically, the electrochemical stimulus generates a change in the sensor current, which is compared with the prediction coming from the feedback digital-to-analog converter (DAC) whose bidirectional full scale range is defined by $[-I_{fsn}, +I_{fsp}]$. In practice, the bidirectional current doubles the total chemical current range and enables not only amperometry but also voltammetry measurements for Redox processes. The resulting error current is then integrated by the electrochemical impedance itself and translated into a voltage error in V_{rw}. The comparator performs its single-bit quantification to be oversampled (ϕ_s) and held by the flip-flop in order to update the digital prediction q_{mod}. As a result, q_{mod} bit stream is ΔΣ modulated by the chemical input and most of the power of the single-bit quantization error is pushed to high frequenciy thanks to the filtering properties of the elec-

trochemical impedance. As for the potentiostatic function, the negative feedback and large DC gain of the ΔΣM loop tends to keep V_{rw} close to the programmable RE-WE potential V_{pot}. From the signal processing point of view, the equivalent model is despicted in Fig 2.1(b), where the expression of the noise shaping time constant for the electrochemical lossy integrator τ_1 is given by:

$$\tau_1 = R_{\mathrm{ct}} C_{\mathrm{dl}}. \tag{2.1}$$

2.1.2 First versus Second Order Architectures

Single-bit first-order ΔΣMs, like the one shown in Fig 2.1, present important drawbacks that may affect the performance of such amperometric data converters. The first undesired effect is that they suffer from tones and pattern noise due to the well known correlation between the quantizer error and the quantizer input signal [116], thus degrading the overall SNDR figures. Secondly, the potentiostat voltage V_{rw} is not well established, as will be explained in this section. Furthermore, due to the leakage introduced by the sensor charge-transfer resistance R_{ct}, the ΔΣM may require of higher oversampling ratios (OSRs) in order to attenuate the resulting dead zones of the transfer function [117].

All these issues can be addressed by introducing an electronic integration stage into the ΔΣ loop. However, this solution increases the number of poles of the loop filter, or number of zeros in the noise transfer function (NTF), making the ΔΣM unstable. Therefore, a zero must be added for the purpose of compensating the phase shift and so stabilizing the overall feedback loop. In this sense, the two common architectures of Fig. 2.2 are typically selected for the purpose of introducing this zero in the loop filter. In a distributed-feedback (DFB) second-order topology, like Fig. 2.2(a), the zero is built by adding a feedback path that bypasses the first integrator at high frequencies. The transfer function of the open loop can be expressed as:

$$H_{\mathrm{FB}}(s) = (1+a)\frac{1+\frac{a}{1+a}\tau_1 s}{(1+\tau_1 s)\tau_2 s} \qquad \text{and} \quad f_z = \frac{1+a}{2\pi a \tau_1}, \tag{2.2}$$

where f_z stands for the zero location in frequency. This architecture presents some major drawbacks that complicate its practical implementation for the proper operation of such electrochemical sensors. Firstly, variations in the electrochemical sensor time constant tend to move the loop filter zero location through τ_1, leading to an undesired noise shaping profiles or even the instability of the system. Secondly, one extra current DAC is required, increasing overall complexity and power

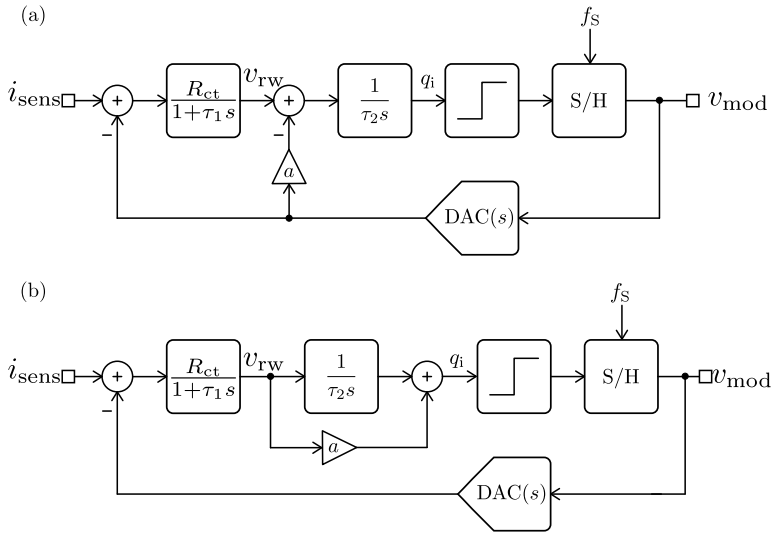

Figure 2.2 | Signal block diagrams of DFB (a) and FF (b) single-bit second-order CT ΔΣM topologies.

consumption. Furthermore, the potentiostat voltage $v_{rw} = V_{rw} - V_{pot}$ is strongly influenced by the input signal, as clearly shown in Fig. 2.3. This is because the sum of the two input paths, the potential v_{rw} and the feedback signal multiplied by the feed-in coefficient a, are controlled to be zero over time. Therefore, v_{rw} must contain a DC component to counteract the feedback signal. The DC potentiostatic characteristic of the first-order ΣΔM from [11, 12] is also shown in the same figure. In this case, v_{rw} coincides with q_i, driving directly the quantizer, which on the other hand must compensate for i_{sens}, resulting in a correlation of v_{rw} with i_{sens}. On the other hand, in the feed-forward (FF) second-order topology of Fig. 2.2(b), the loop filter zero is placed by providing a FF path that bypasses the second integrator at high frequencies. The transfer function of the open loop can be expressed as:

$$H_{FF}(s) = \frac{1 + a\tau_2 s}{(1 + \tau_1 s)\tau_2 s} \qquad \text{and} \quad f_z = \frac{1}{2\pi a \tau_2}. \tag{2.3}$$

This topology is much more attractive for its circuit implementation, since the location of the zero depends on the electronic integrator and the FF coefficient but not on the sensor time constant τ_1. In addition, as seen in Fig. 2.3 and unlike in the DFB topology, the RE-WE potential does not contain any significant part of the input signal, since the second integrator forces its input v_{rw} to have DC zero component, optimizing the overall potentiostatic function.

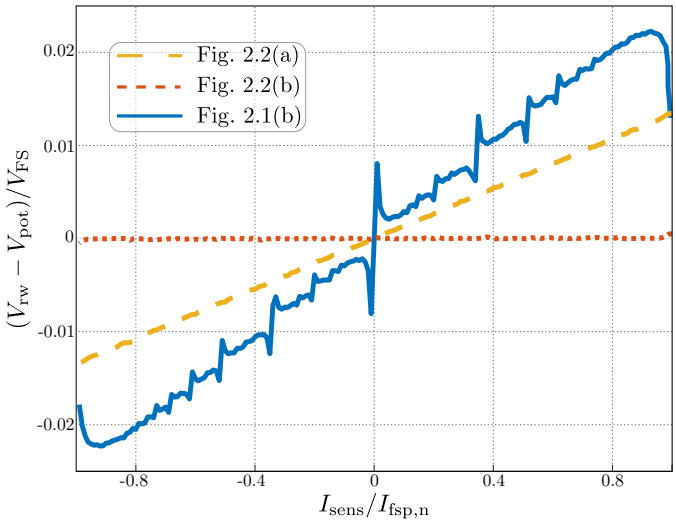

Figure 2.3 | DC simulation comparison of the second-order potentiostat behavior for OSR = 250 and $\tau_1 = 0.15\,\mathrm{s}$.

In conclusion, the single-bit second-order FF modulator architecture of Fig. 2.2(b) is selected here to avoid iddle tones, pattern noise and enhance the potentiostatic performance. Extending the sensor-in-the-loop concept of Fig. 2.1, the mixed electrochemical-electronic second-order $\Delta\Sigma$M architecture of Fig. 2.4(a) is proposed. The resulting architecture is named fixed-WE due to the predetermined potential of the working electrode. The principle of operation is similar to the first-order described previously in Section 2.1.1, but with the included benefits of the FF second-order topology of Fig. 2.2(b).

In general, the summation at the input of the quantizer may increase circuit complexity and power dissipation. In this perspective, the FF path is simplified here by providing a direct path from the reference electrode to the positive input of the single-bit quantizer, i.e. a≡1 in Fig. 2.2(b), combined with the negative sign of the electronic integrator such that the differential input of the quantizer is equal to the summation of the integrated and FF signals. The equivalent small-signal circuit is shown in Fig. 2.4(a) with the following open-loop transfer function:

$$L_1(s) = -R_{\mathrm{ct}} G_{\mathrm{mf}} \frac{1+\tau_2 s}{(1+\tau_1 s)\,\tau_2 s} \text{ and } \quad \tau_2 \doteq \frac{C_2}{G_{\mathrm{m2}}}. \tag{2.4}$$

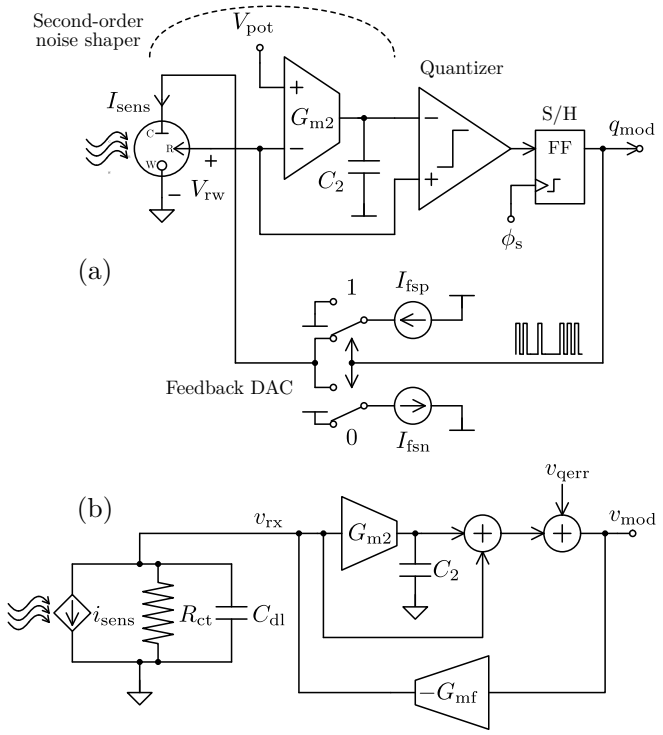

Figure 2.4 | Proposed fixed-WE potentisotatic-amperometric single-bit second-order FF CT ΔΣM architecture (a) and small-signal model (b).

2.1.3 Stability, Noise and Reference Voltage Ripple Analysis

Stability Analysis

The small-signal stability of the FF ΣΔM in Fig. 2.2(b) can be analyzed using the root-locus method [118], which supplies a graphical procedure for examining how the closed-loop poles change as a function of the quantizer gain. By definition, the stability is ensured as long as there are non-empty range of inputs for the quantizer gain for which all the roots of the system reside in the LHP of the imaginary axis in the s-plane.

Fig. 2.5 shows the linear model of the proposed modulator, including the electrochemical sensor equivalent impedance and the electronic integrator with FF compensation, being K the linear gain of the sampled quantizer. The DAC feedback

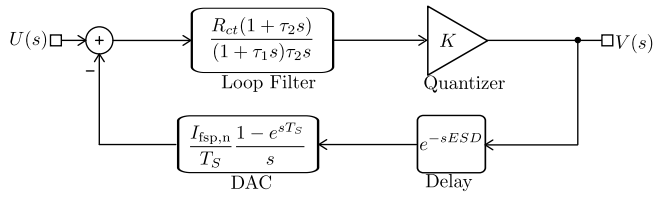

Figure 2.5 | Linear model of the single-bit second-order FF electrochemical CT ΣΔM of Fig. 2.4.

impulse response has the typical function of a zero-order hold:

$$\mathrm{DAC}(s) = \frac{I_{\mathrm{fsp,n}}}{T_{\mathrm{s}}}\frac{1-e^{-sT_{\mathrm{S}}}}{s}, \tag{2.5}$$

where T_{s} stands for the sampling period. It is well known that the single-bit quantizer has intrinsic non-linear gain, which is statistically signal dependent as explained in [116]. The excess loop delay (ELD), defined as the time delay between the quantizer clock edge and the time when a change at the DAC output occurs, is represented by a pure CT delay block. The loop transfer function of this model is determined to be:

$$L(s) = 1 + K\frac{R_{\mathrm{ct}}(1+\tau_2 s)}{(1+\tau_1 s)\tau_2 s}\frac{I_{\mathrm{fsp,n}}}{T_S}\frac{1-e^{-sT_{\mathrm{s}}}}{s}e^{-s\mathrm{ELD}}. \tag{2.6}$$

Since traditional root locus requires rational polynomial functions, third-order Padé approximant [119] have been used to fit the exponential terms in (2.6). The root locus of the system characteristic as a function of the gain factor K for different ratio values of $f_{\mathrm{z}}/f_{\mathrm{s}}$ is plotted in Fig. 2.6. The ELD effect has been mitigated due to the very low-frequency operation of the ΔΣM. It is worth noting that the poles move into the unstable region, i.e. into the right-half plane (RHP), with increasing quantizer gain K. The poles come back into the LHP if the gain is decreased. Therefore, the worst-case scenario is when this gain is maximum, which occurs for input signal levels close to zero. The innermost pole trajectory in Fig. 2.6 is for $f_{\mathrm{z}}/f_{\mathrm{s}} = 3/(2\pi)$. This system is of no usage since it is unstable for any quantizer gain, i.e. for any input signal value. As seen, increasing $f_{\mathrm{z}}/f_{\mathrm{s}}$ improves the system stability.

Exhaustive behavioural simulations at system level has been carried out to find the stable region of the modulator as a function of $f_{\mathrm{z}}/f_{\mathrm{s}}$. The plots of Fig. 2.7 have been calculated extracting the information from root locus analysis. Considering $\tau_1 >> \tau_2$, the stability of the modulator is affected by the relative location of the

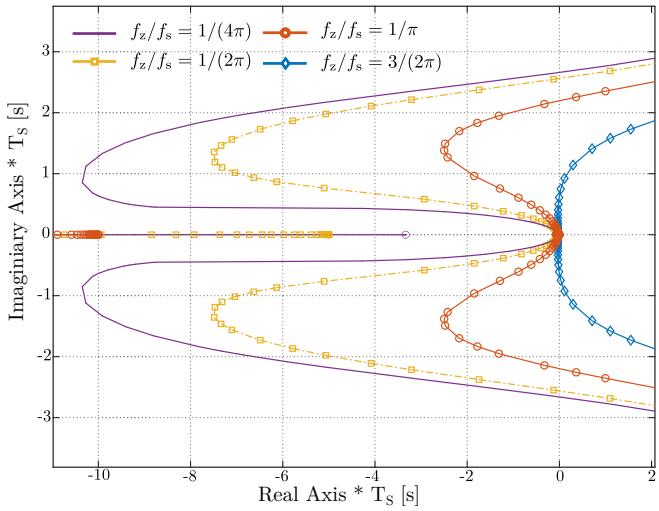

Figure 2.6 Root locus of the single-bit second-order FF CT ΣΔM model of Fig. 2.4 as a function of the quantizer gain K, for several values of f_z/f_s.

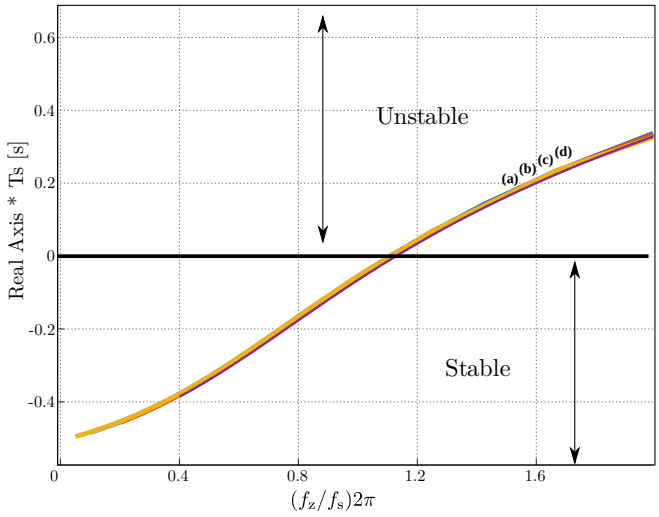

Figure 2.7 Stability region of the root locus of Fig. 2.6 as a function of f_z/f_s for OSR = 125 (a), 250 (b), 500 (c) and 1 k (d) considering $\tau_1 >> \tau_2$.

zero f_z with respect to the sampling frequency f_s such as:

$$\frac{f_z}{f_s} \leq \frac{1}{2\pi} \text{ or, equivalently } \tau_2 \geq T_s. \tag{2.7}$$

Since the loop filter zero placement can vary due to mismatch and process variations, it is advised to locate the zero far enough from the above stability boundary. However, moving the zero to lower frequencies lead to a first-order like behavior. This loss of second-order range is highlighted in Fig. 2.8(a), where several power spectrum densities (PSDs) of SQNR with different locations of the loop filter zero are compared. The design (2) is more insensitive to instability, but has a less aggressive noise shaping. Conversely, the design (3) behaves more like a pure second-order ΔΣM although with a less safe stability margin. Moving the zero to higher frequencies leads to a useless distorted unstable system, as clearly shown by (1). Fig. 2.8(b) depicts how the quantization spectrum is affected when the transducer bandwidth is increased. The hundredfold of τ_1 between (4) and (5) causes the visible increased of in-band noise floor due to the insurgence of the first-order noise shaping. In this region, the electrochemical leaky integrator is not contributing to the noise shaping, and the 20 dB/dec slope relies only on the contribution of the electronic integrator. This effect is prevented by decreasing T_s (and so τ_2), ensuring a high OSR, being:

$$\text{OSR} \doteq \frac{f_s}{2 \cdot \text{BW}} = \pi \frac{\tau_1}{T_s}. \tag{2.8}$$

Noise Analysis

There are several types of noise sources that contaminate the output of a ΔΣM ADC converter, such as quantization noise, device noise, clock jitter, reference noise and supply interfernces, among others. This analysis is focused on the two main noise contributors in the context of electrochemical sensors. The first one is the well-known quantization noise [116], which has been already considered in the analysis of previous sections through the SQNR. The power of the quantization noise is spread over the wide sampling frequency range, falling only a small part of it inside the band of interest. In addition, this noise is further suppressed by the loop gain. The measurement of slow chemical signals facilitates the use of high oversampling ratios, giving higher attenuation of the quantization noise in the signal band. As already shown in Fig. 2.8, limited-bandwidth electrochemical signals, typically in the sub-Hz range, combined with a second order loop filter already allow to achieve very high SQNR values with sampling frequencies in the kHz range. The other noise source comes from the device itself, i.e. the analog circuitry used in the building blocks of the ΔΣM. Indeed, due to the extremely low frequencies of operation associated with electrochemical sensors, CMOS flicker noise usually dominates in-band contributions and so it can be the main SNDR limiting factor.

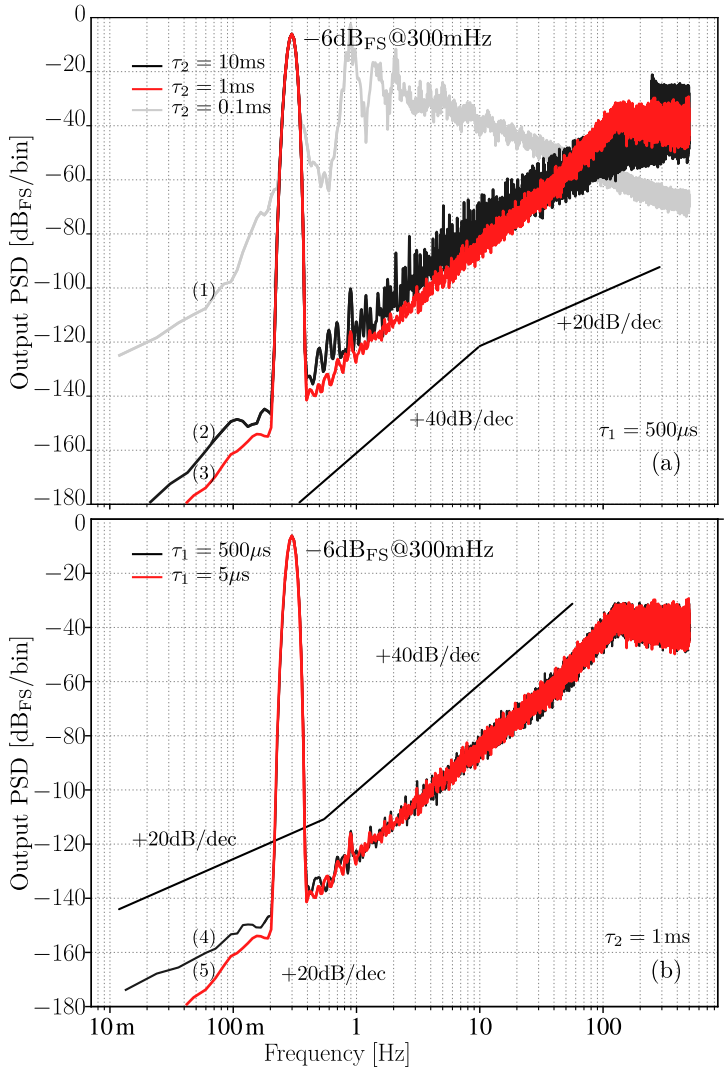

Figure 2.8 | Simulated SQNR of the ΔΣM proposed in Fig. 2.6 for $Ts = 1$ms. First-order leakage effect in outerband (a) and first-order leakage in baseband (b).

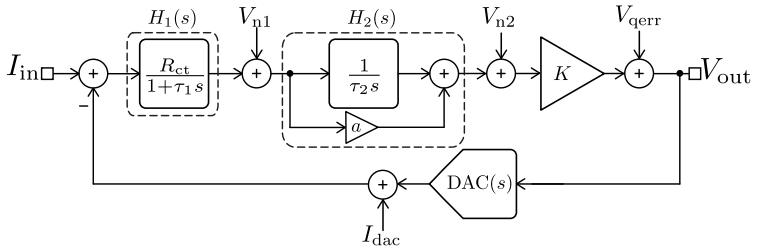

Figure 2.9 | Linear noise model of the single-bit second-order FF electrochemical CT ΔΣM of Fig. 2.4.

Fig. 2.9 shows the linear model of the FF ΔΣM with the included quantization and device noise contributions. The signal transfer function (STF) of the modulator together with the NTFs of the quantization noise V_{qerr}, first integrator noise V_{n1}, second integrator-noise V_{n2}, and feedback DAC noise V_{dac} can be expressed as follows:

$$\begin{cases} \mathrm{STF}(s) = \dfrac{V_{\mathrm{out}}(s)}{V_{\mathrm{in}}} = \dfrac{H_1(s)H_2(s)K}{1+H_1(s)H_2(s)K} \approx 1 \\ \mathrm{NTF}_{\mathrm{qerr}}(s) = \dfrac{V_{\mathrm{out}}(s)}{V_{\mathrm{qerr}}} = \dfrac{1}{1+H_1(s)H_2(s)K} \approx \dfrac{1}{H_1(s)H_2(s)K} \\ \mathrm{NTF}_{\mathrm{n1}}(s) = \dfrac{V_{\mathrm{out}}(s)}{V_{\mathrm{n1}}} = \dfrac{H_2(s)K}{1+H_1(s)H_2(s)K} \approx \dfrac{1}{H_1(s)} \\ \mathrm{NTF}_{\mathrm{n2}}(s) = \dfrac{V_{\mathrm{out}}(s)}{V_{\mathrm{n2}}} = \dfrac{K}{1+H_1(s)H_2(s)K} \approx \dfrac{1}{H_1(s)H_2(s)} \\ \mathrm{NTF}_{\mathrm{dac}}(s) = \dfrac{V_{\mathrm{out}}(s)}{V_{\mathrm{dac}}} = \dfrac{-H_1(s)H_2(s)K}{1+H_1(s)H_2(s)K} \approx -1 \end{cases} \tag{2.9}$$

Notice that while the input signal is transferred with a gain of nearly unity, the quantization noise is further attenuated by the gain of the overall loop filter. The noise added by the electronic integrator, used as second stage in the ΔΣ loop, is also mitigated thanks to the loop gain imposed by the sensor itself. Conversely, the noise coming from the feedback DAC is not shapped at all by the ΔΣ loop but directly added to the input signal path. Therefore, the in-band noise coming from the feedback DAC alone suffices to be considered, as illustrated by the flicker noise cancellation mechanism proposed in Section 2.3.

Reference Electrode Voltage Ripple

The ΔΣM proposal of Fig. 2.4 has to fulfill further requirements related to the potentiostat operation. For instance, the magnitude of the reference electrode voltage ripple may be required to be kept below a certain amount. Depending on the digital output, the integrating double-layer capacitance C_{dl} is charged or discharged by the feedback current DAC $I_{\mathrm{fsp,n}}$ over a sampling period prior to being sampled. This voltage change on C_{dl} causes voltage ripple at RE with the following relationship:

$$\frac{\Delta V_{\mathrm{rw}}}{V_{\mathrm{rw}}} \propto \frac{I_{\mathrm{fsp,n}}/C_{\mathrm{dl}}}{I_{\mathrm{fsp,n}} R_{\mathrm{ct}} f_{\mathrm{s}}} = \frac{1}{\tau_1 f_{\mathrm{s}}}. \tag{2.10}$$

In practice, root-mean-square (RMS) values as low as few mV are allowed without triggering any redox process at the RE liquid interface [28]. For one-bit quantization, the sampling frequency is the only degree of freedom in order to minimize the magnitude of this voltage ripple, since $I_{\mathrm{fsp,n}}$ and C_{dl} are fixed by the electrochemical sensor full scale and dynamics themselves. Therefore, the ripple voltage at RE is improved by properly chosing the OSR. Conclusively, the sampling frequency, apart from its direct effect on the stability of the system and the SQNR performance, must also be chosen based on the maximum ripple allowed at the reference electrode. Hence, both figures can be improved by increasing the sampling frequency at the cost of power consumption. Once the OSR is chosen for a satisfactory SQNR and RE ripple considerations, f_{z} must be set to comply with stability condition (2.7).

2.1.4 Proof-of-Concept Discrete Implementation

As a preliminary validation, the second-order electrical-electrochemical ΔΣM proposal of Fig. 2.4 is first designed and implemented using discrete electronic components prior being integrated onto CMOS technologies. Fig. 2.10(a) depicts the discrete circuit implementation for the proof of concept. The negative ΔΣ loop is closed through the sensor, the RC electronic integrator as τ_2, the microcontroller (MCU) as quantizer and S/H, and the resistor R_{FS} as current feedback DAC. The unity-gain FF path to stabilize the loop is accomplish through the electronic integrator itself.

$$V_{\mathrm{int}}(t) = V_{\mathrm{r}}(t) + \frac{1}{R_{\mathrm{int}} C_{\mathrm{int}}} \int V_{\mathrm{r}}(t) - V_{\mathrm{pot}}\, dt. \tag{2.11}$$

Its principle operation can be described as in Section 2.1.1 but with the added benefits of the electronic integrator. Here, the electrochemical input current I_{sens} is

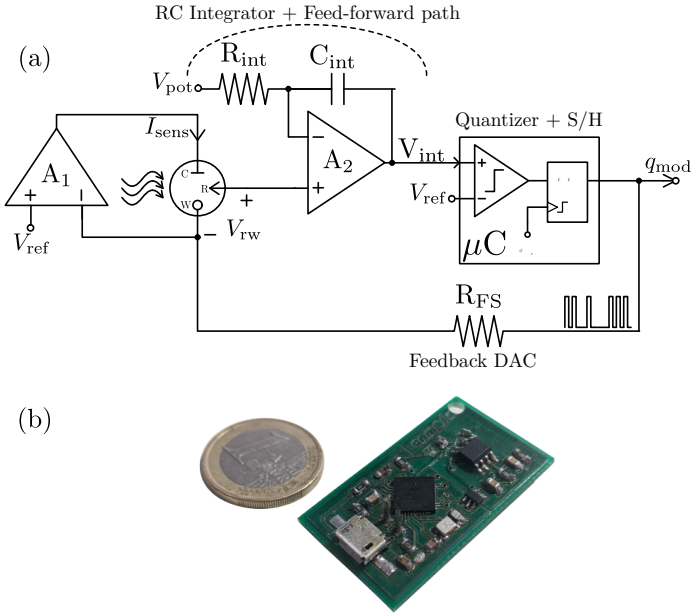

Figure 2.10 | Proof of concept of the architecture proposed in Fig. 2.4. Discrete circuit solution (a) and PCB (size: 38.5 mm × 22.5 mm) (b).

compared to the single-bit prediction coming from the feedback DAC $\frac{1}{R_{\mathrm{FS}}}(q_{\mathrm{mod}} - V_{\mathrm{ref}})$. The resulting error current is integrated in the sensor leaky impedance and translated into an error voltage at V_{rw}. The low-frequency error is further amplified by the integrator built around the operational amplifier A_2 in form of a charge stored in C_{int}. The voltage output of A_2, holding the information of the error charge according to (2.11), is connected to the MCU comparator input port. Periodically, at a pace provided by the MCU sampling clock, the accumulated error is assessed to be either positive or negative. Consequently, the MCU output digital drivers set the voltage across the R_{FS}, thus forcing I_{sens} to compensate for the accumulated error. The same loop also provides the correct potentiostatic DC voltage since any difference between V_{pot} and V_{rw} in (2.11) is also accumulated into the electronic integrator and then corrected by the $\Delta\Sigma$ loop. Besides, the WE voltage is set to half the supply, by the local negative feedback loop built around operational amplifier A_1 and the corresponding value of V_{ref}. This feedback loop compensates for the current I_{sens} at the WE, counteracting at CE. This condition is reinforced by using ultra-low input currents operational amplifiers (both A_1 and A_2), which avoid parasitic charge flows, specially at the RE.

Fig. 2.10(b) shows the extremely compact mounted printed circuit board (PCB), which it has been both electrically and electrochemically validated. A Pt 3-electrode linear array was used as pseudo-reference, working and counter electrodes. This electrodes set was fabricated on a Si substrate at the Institut de Microelectrònica de Barcelona (IMB-CNM) clean room facilities, according to a previously described photolithographic process [120]. Electrical characterization of the sensor, following the Randles model of Fig. 4.5 is fundamental to estimate the intrinsic sensor time constant. For this purpose, experimental EIS measurements of the sensor were performed using Solartron SI 1287 potentiostat coupled with Solartron 1260 impedance/gain-phase analyzer module both from Ameteck Inc., USA. The fabricated Pt 3-electrode linear array presented $R_{\mathrm{ct}} = 56\ \mathrm{k}\Omega$ and $C_{\mathrm{dl}} = 1.5\ \mu\mathrm{F}$.

In order to measure the instrumentation noise floor, a dummy electrical $R_{\mathrm{ct}}C_{\mathrm{dl}}$ sensor emulator with zero input condition was used to acquire the q_{mod} recording that resulted in the power spectrum of Fig. 2.11(a). Two regions are clearly visible: thermal flat noise dominates up to approximately 80 Hz, while for the higher frequencies the noise profile is dominated by the second-order (i.e. 40 dB/dec) shaped quantization noise.

For the electrochemical tests, the discrete implementation has been characterized through CV experiments of the $\mathrm{Fe^{III}(CN)_6^{3-}/Fe^{II}(CN)_64^-}$ couple. Fig. 2.11(b) shows the results for a 1 mM Ferri-Ferro in 150 mM KCl at different scan rates. The results are satisfactory compared to desktop comercial potentiostat equipments. Data is extracted by first recording the digital signal q_{mod} and after applying digital averaging using a third-order Butterworh low-pass filter as digital decimator with cut-off frequency of 2.5 Hz. Finally, it is worth to highlight that these preliminary experimental results are shown for the only purpose of validating the proof of concept, but their absolute performance is not indicative of the CMOS circuit implementations proposed in Chapter 3.

2.2 Differential Wide Potentiostatic Range

The fixed-WE ΔΣM architecture proposed in Fig. 2.4 shows an ideal programmable range of $0 < V_{\mathrm{pot}} < V_{\mathrm{DD}}$, where V_{DD} stands for the nominal IC supply voltage. From the potentiostat viewpoint, it would be interesting to extend such a programmability to $V_{\mathrm{rw}} \in (-V_{\mathrm{DD}}, +V_{\mathrm{DD}})$ not only because of electrochemical reasons (e.g. cyclic voltammetries) but also for the portability of the design to downscaled CMOS technologies with low V_{DD} values (e.g. 1.2 V).

In contrast to the fixed-WE architecture, the programmable-WE proposal of Fig. 2.12(a) is introduced to differentially control the voltages of both the working and

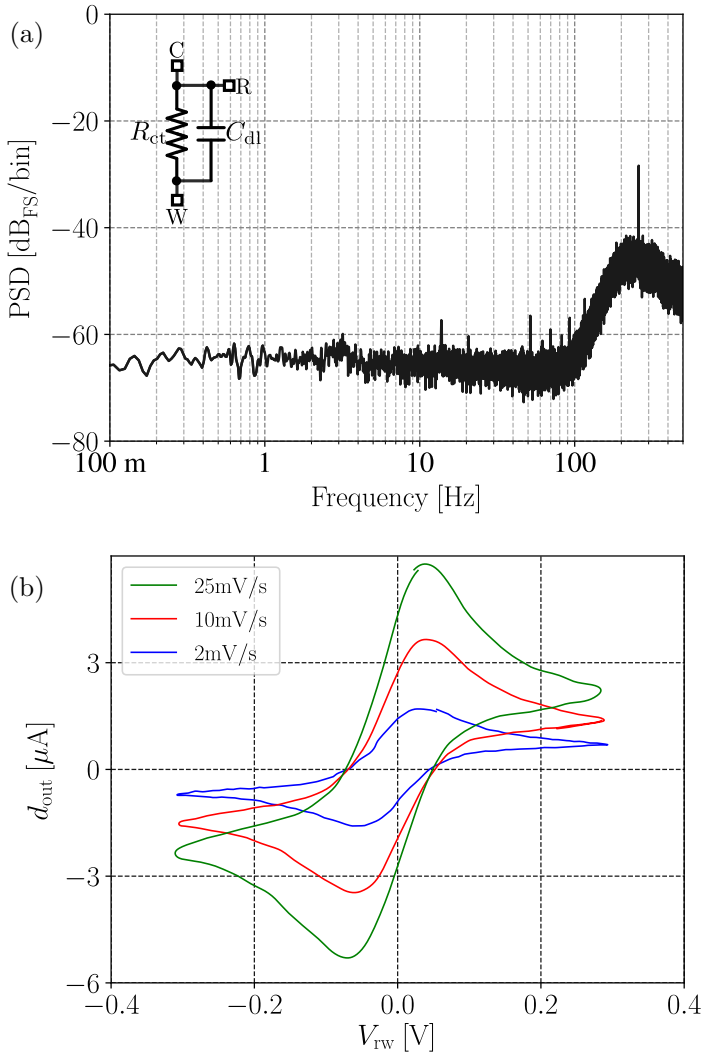

Figure 2.11 Electrical zero-input (a) and electrochemical cyclic voltammetries (b) measurements of the proof of concept of Fig. 2.10 with $R_{FS} = 330k\Omega$.

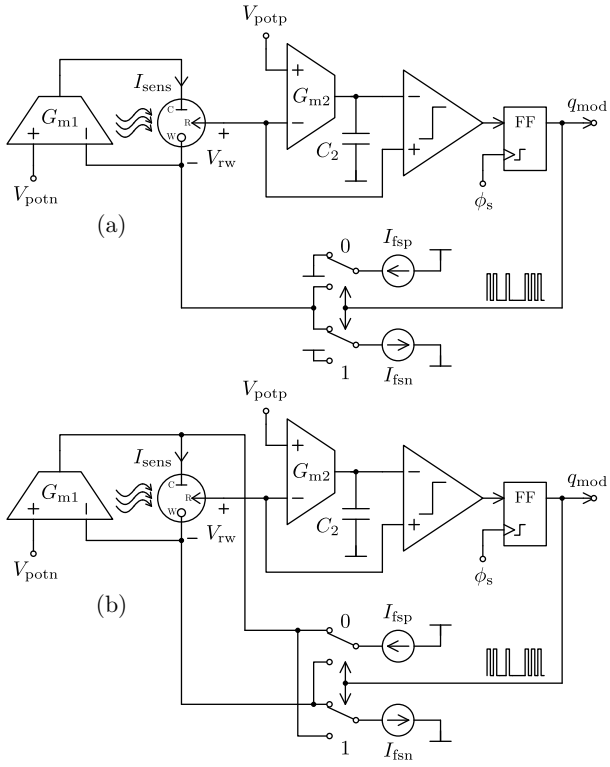

Figure 2.12 Proposed programmable-WE (a) and differential-DAC (b) potentiostatic electrochemical single-bit second-order FF CT ΔΣM architectures.

reference electrodes as:

$$V_{\text{pot}} = V_{\text{potp}} - V_{\text{potn}}, \tag{2.12}$$

and so to extend the potentiostatic range virtually up to double the supply voltage, like in [3]. Its equivalent linear model is shown in Fig. 2.13(a) with:

$$L_2(s) = -G_{\text{mf}} \left(\frac{G_{\text{m1}} R_{\text{ct}} - 1}{G_{\text{m1}}} \right) \frac{1 - \frac{\tau_1}{G_{\text{m1}} R_{\text{ct}} - 1} s}{1 + \tau_1 s} \frac{1 + \tau_2 s}{\tau_2 s}, \tag{2.13}$$

$$L_2(s) \longrightarrow L_1(s) \quad \text{for} \quad G_{\text{m1}} \gg \frac{1}{R_{\text{ct}}}. \tag{2.14}$$

Unfortunately, this architecture imposes severe power requirements on the transconductor G_{m1} to push the RHP zero to high frequency. The differential-DAC alterna-

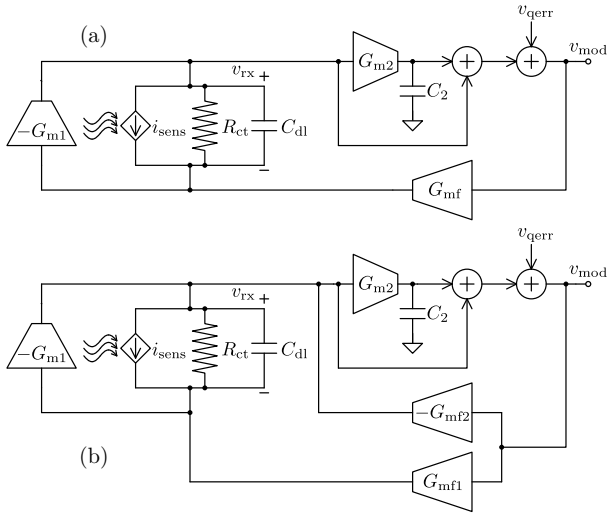

Figure 2.13 | Small-signal model of the programmable-WE (a) and differential-DAC (b) ΔΣM architectures of Fig. 2.12

tive of Fig. 2.12(b) comes to solve the above issue while maintaining the potentiostatic wide range. In such a case, the equivalent small-signal circuit of Fig. 2.13(b) returns:

$$L_3(s) = -G_{\mathrm{mf1}} \left(\frac{R_{\mathrm{ct}}}{1+\tau_1 s} - \frac{1-\frac{G_{\mathrm{mf2}}}{G_{\mathrm{mf1}}}}{G_{\mathrm{m1}}} \right) \frac{1+\tau_2 s}{\tau_2 s}, \tag{2.15}$$

$$L_3(s) \equiv L_1(s) \quad \text{for} \quad G_{\mathrm{mf1}} = G_{\mathrm{mf2}} \doteq G_{\mathrm{mf}}. \tag{2.16}$$

Hence, the effect of the RHP zero can be canceled. Indeed, this cancellation is always perfect because G_{mf1} and G_{mf2} do not actually exist as separated physical transconductors. In this sense, both I_{fsp} and I_{fsn} current sources must be seen as a single biphasic transconductance, whose output is steered between the two paths. For example, in the event of any current offset between I_{fsp} and I_{fsn}, the same offset would be applied through the two G_{mf1} and G_{mf2} signal paths. As a positive side effect, the G_{m1} transconductor current requirements are now relaxed, as it only has to cope with the I_{fsp} and I_{fsn} mismatching.

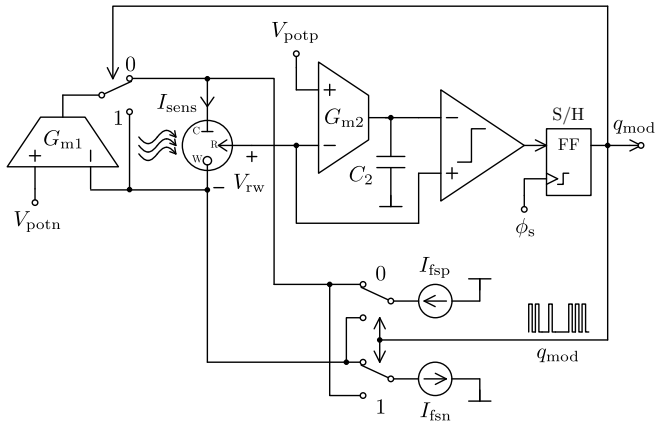

Figure 2.14 | Proposed wide-range potentiostatic second-order electrochemical ΔΣM with flicker noise cancellation.

2.3 Flicker Noise Cancellation

As already pointed in the noise analysis of Section 2.1.3, the main low-frequency noise contributions in Fig. 2.12(b) come from the CMOS current sources of the feedback DAC, whose flicker noise is not shaped by the ΔΣM loop. Therefore, to guarantee a high resolution for such slow electrochemical signals while preserving small dimensions of the feedback DAC transistors, the ΔΣM variation architecture of Fig. 2.14 is proposed. In order to explain the flicker noise cancellation mechanism, the comparative analysis of Fig. 2.15 is supplied. When the 1/f noise cancellation mechanism of Fig. 2.14 is not activated, the I_{fsp} and I_{fsn} noise currents are either bypassed to G_{m1} or integrated into V_{rw} depending on the output digital state. In the scenario of very weak chemical signals, the averaged probability of 0's and 1's symbols is equalized in the q_{mod} output bit stream, resulting in a 6-dB attenuation of the I_{fsp} and I_{fsn} intrinsic noise levels. The G_{m1} switching mechanism of Fig. 2.14 is proposed in order to promote further cancellation of the low-frequency noise currents injected by the feedback DAC. Again, the corresponding noise circulation is depicted in Fig. 2.15(b). Now, the flicker contributions coming from the I_{fsp} source are always bypassed to G_{m1}, while the counterparts from the I_{fsn} source are biphasically integrated into the electrochemical sensor impedance. Obviously, the cancellation of the latter becomes optimum when q_{mod} shows equal probability of 1's and 0's symbols, which is the common case of very weak signals. Hence, the proposed noise reduction scheme aims to improve the chemical LOD of the overall ΔΣM for electrochemical measurements over extended periods.

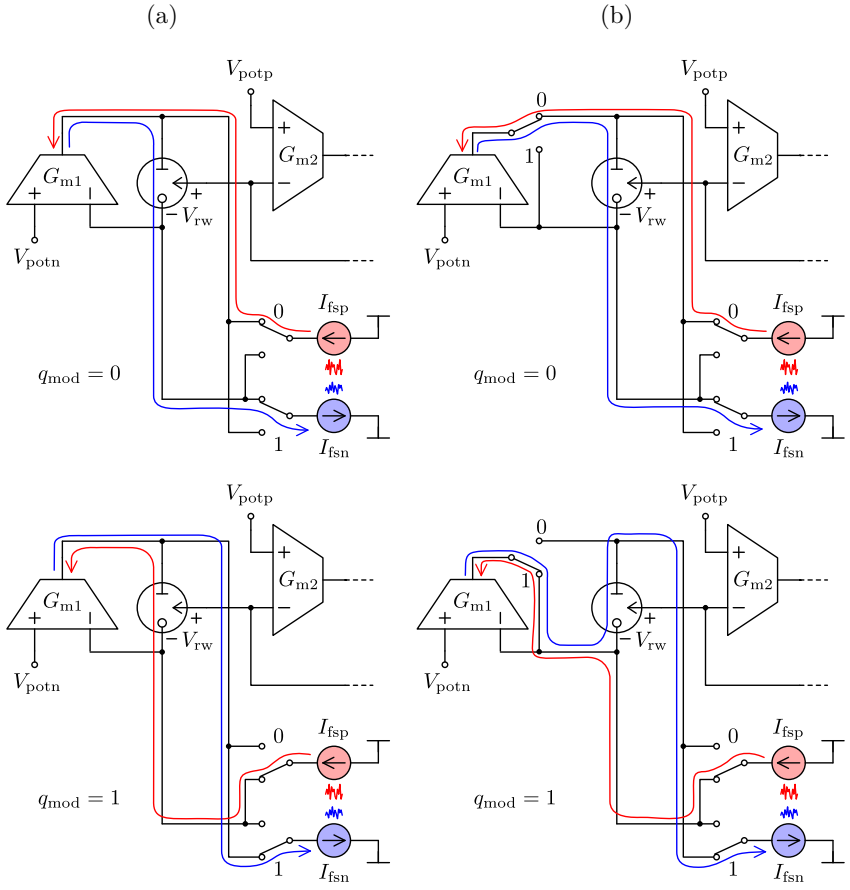

Figure 2.15 Feedback DAC I_{fsp} (red) and I_{fsn} (blue) noise current circulation without (a) and with (b) the proposed G_{m1}-switching flicker cancellation method of Fig. 2.14 for all output data cases of q_{mod}.

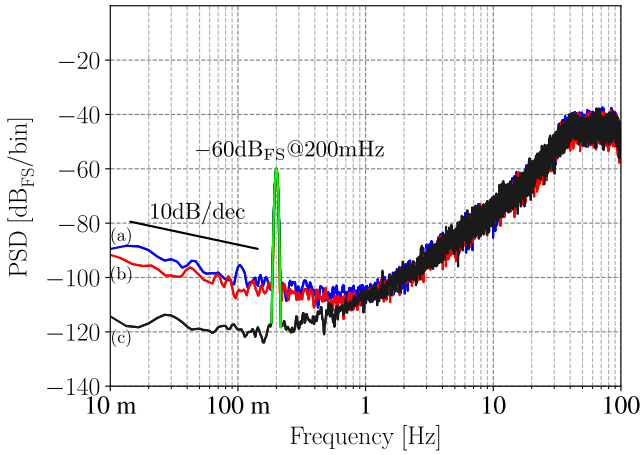

Figure 2.16 Electrical model simulation output PSD comparison: fixed-WE (a), differential-DAC (b) and G_{m1}-switching (c) for weak inputs. Response to -65 $\mathrm{dB_{FS}}$ 200 mHz sinusoidal input. Configuration is $(V_{\mathrm{potn}} - V_{\mathrm{potp}}) = 0$ V and ±100-nA full scale.

Fig. 2.16 illustrates the efficiency of this technique through transistor-level noise simulations. Here, the electrical model output PSD accounting with flicker noise in the feedback DAC is simulated and compared to the fixed-WE (a), differential-DAC (b), and G_{m1}-switching (c) architectures for weak input signals.

In conclusion, the proposed flicker noise cancellation mechanism is well suited for scenarios with equiprobability between the two output symbols '1' and '0', like the case of LOD. On the contrary, its effectiveness may be reduced when such a balance is broken due to large signals with strong asymmetric input waveforms.

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Modern electrochemical sensory applications demand portable, and even wearable, high-resolution smart systems featuring compact, lightweight, energy-efficient and cost-effective circuit frontends. In this scnearios, ICs in CMOS technologies can supply the required smartness at reduced power and size (cost).

This chapter collects the new potentiostatic-amperometric ΔΣM architectures of Chapter 2 to propose optimized mixed-signal circuit implementation in popular cost-effective performance mixed-signal CMOS technologies. Indeed, two μW-range practical integrated circuit realizations in 180-nm and 65-nm CMOS nodes (3 steps in Moore's Law) are presented with the aim of proving architecture scalability. First, a design in 1.2-V 65-nm CMOS technology of the novel low-power extended-DR potentisotat-amperometric ΔΣM architecture of Fig. 2.12(b) is designed. Subsequently, a smart mixed-signal front-end of the proposed architecture of Fig. 2.14 is designed in 1.8-V 0.18-μm CMOS technology and customized for the low-cost assembling technology of Chapter 4. The chapter ends up with a comparison of both integrated implementations at electrical simulation level.

3.1 Low-Power CMOS Circuits

Thanks to the fusion of the potentiostatic AFE and the amperometric ADC, the main analog blocks to be designed for the proposed minimalistic ΔΣMs presented in Chapter 2 are reduced to the $G_{\mathrm{m1,2}}$ transconductors, the current feedback DAC and the quantizer comparator. In practice, the main bottleneck for their CMOS circuit implementation comes from the wanted wide-range potentiostatic programmability.

Differential signal range is not an issue in our case because the system will be usually designed for low-amplitude ripple at V_{rw}. However, and specially in those sub-micrometer CMOS technologies where the threshold voltages have not been scaled down at the same ratio as the supply voltage, the extended swing of both V_{potp} and V_{potn} does impose challenging input and output common-mode range specifications for the G_{m2} and G_{m1} transconductors, respectively. Furthermore, the wide programmability also affects the input common-mode range of the quantizer comparator and the operation for the current feedback DAC, requiring of low-headroom operation.

3.1.1 Rail-to-Rail One-Times Current Transconductor

In the case of $G_{\mathrm{m1,2}}$, the well-known one-times current mirror topology [13] circuit of Fig. 3.1(a) is selected for the purpose of keeping $I_{\mathrm{biasp}} + I_{\mathrm{biasn}}$ (so transconductance) constant regardless the input common-mode level. In other words, when the complementary input differential pairs M1-M2 and M3-M4 supplying G_{mn} and G_{mp} is operating in weak inversion saturation, according to the Enz-Krummenacher-Vittoz (EKV) metal-oxide-semiconductor field-effect transistor (MOSFET) model [121]:

$$G_{\mathrm{m}} = G_{\mathrm{mn}} + G_{\mathrm{mp}} = \frac{I_{\mathrm{biasn}}}{nU_{\mathrm{t}}} + \frac{I_{\mathrm{biasp}}}{nU_{\mathrm{t}}}, \tag{3.1}$$

where n and U_{t} stand for the subthreshold slope and the thermal potential, respectively. Hence, by keeping the sum $I_{\mathrm{biasn}} + I_{\mathrm{biasp}}$ constant, the combined transconductance can be equalized for the wide input common-mode range. This task is done by M5, which steers the tail current depending on the input common-mode referred to V_{ref}. This topology is combined with a folded-cascode output stage, where the biasing levels of the cascode devices have been optimized to maximize the output voltage swing [122], allowing to limit the amplitude loss at each rail to only two saturation voltages. Furthermore, proportional to absolute temperature (PTAT) bias currents can be used for I_{biasn} and I_{biasp} in order to compensate the thermal dependency in (3.1).

3.1.2 Rail-to-Rail Latched Quantizer

A latched-type dynamic comparator is an ideal option for the implementation of the single-bit quantizer of the $\Delta\Sigma$M due to their full output swing, high input impedance and absence of static power consumption [123]. However, traditional latch comparators suffer from limited common-mode input range. A strategy similar to the complementary-input transconductors of Fig. 3.1(a) is proposed in

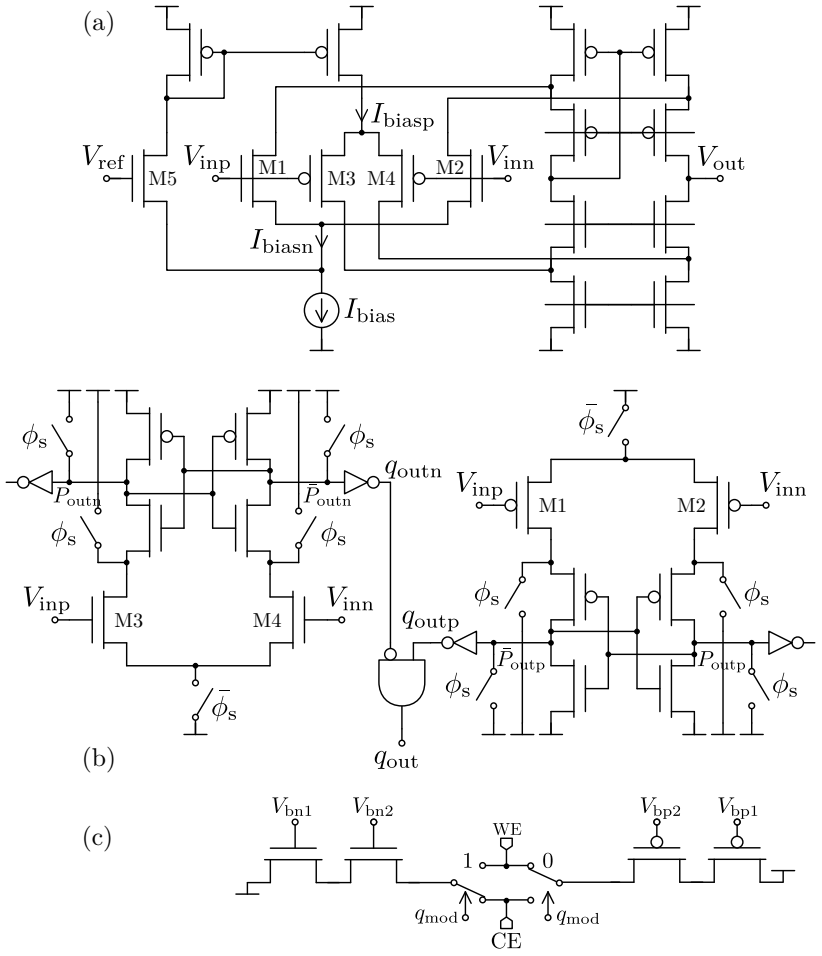

Figure 3.1 CMOS rail-to-rail one-times current transconductor [13] (a), rail-to-rail latched quantizer (b) and single-bit feedback DAC (c) for the proposed ΔΣM architectures of Fig. 2.12(b) and Fig. 2.14.

Fig. 3.1(b) but in the digital domain. The output of two complementary latched comparators are logically combined following Table 3.1. Basically, during the reset phase ($\phi_s = 1$), switches pre-charge $\{P_{\text{outn}}, \bar{P}_{\text{outn}}\}$ and discharge $\{P_{\text{outp}}, \bar{P}_{\text{outp}}\}$ nodes to V_{DD} and V_{SS}, respectively. In the comparison phase ($\phi_s = 0$) the input differential voltage ($V_{\text{inp}} - V_{\text{inn}}$) is converted into a differential current and mirrored to the regenerative latch. Positive feedback enables the regeneration of a small differential voltage to a full swing differential voltage. In the event where the PMOS-input latch is off (input common-mode close to V_{DD}), $\{P_{\text{outp}}, \bar{P}_{\text{outp}}\}$ nodes remain at the negative rail regardless of ϕ_s. The output inverter ensures a logic 1 in one of the AND inputs, and so q_{out} follows $\bar{q}_{\text{outn}}$. On the other hand, when NMOS-input latch is off (input voltage close to V_{SS}), $\{P_{\text{outn}}, \bar{P}_{\text{outn}}\}$ nodes remain charged to the positive supply V_{DD} and two inverters ensure a logic 1. Therefore, q_{out} follows q_{outp}. Lastly, when both are operating simultaneosly, q_{out} follows $q_{\text{outp}} \cdot \bar{q}_{\text{outn}}$

$\frac{V_{\text{inp}}+V_{\text{inn}}}{2}$	q_{outp}	q_{outn}	q_{out}
close to V_{DD}	1	$\text{sign}(V_{\text{inn}} - V_{\text{inp}})$	$\bar{q}_{\text{outn}}$
otherwise	$\text{sign}(V_{\text{inp}} - V_{\text{inn}})$	$\text{sign}(V_{\text{inn}} - V_{\text{inp}})$	$q_{\text{outp}} \cdot \bar{q}_{\text{outn}}$
close to V_{SS}	$\text{sign}(V_{\text{inp}} - V_{\text{inn}})$	0	q_{outp}

Table 3.1 Electrical to logic transfer function of the rail-to-rail comparator proposed in Fig. 3.1(b).

3.1.3 Differential-Current Feedback DAC

A switched-current source circuit is implemented for the differential single-bit feedback DAC, as shown in Fig. 3.1(c). A current cascode is preferable for both I_{fsn} and I_{fsp} as it boosts the output impedance, it shields the current source from spikes and reduces kick-back interference to the bias lines [124]. The biasing levels can also easly be optimized for low-headroom operation, allowing to limit the amplitude loss at each rail to only two saturation voltages.

3.1.4 All-MOS Subthreshold Current Reference

The main CMOS building blocks presented in previous sections require a supporting current reference for the generation of the bias current of each analog block and for supplying the full-scale levels of the feedback DAC. In general, it is desirable

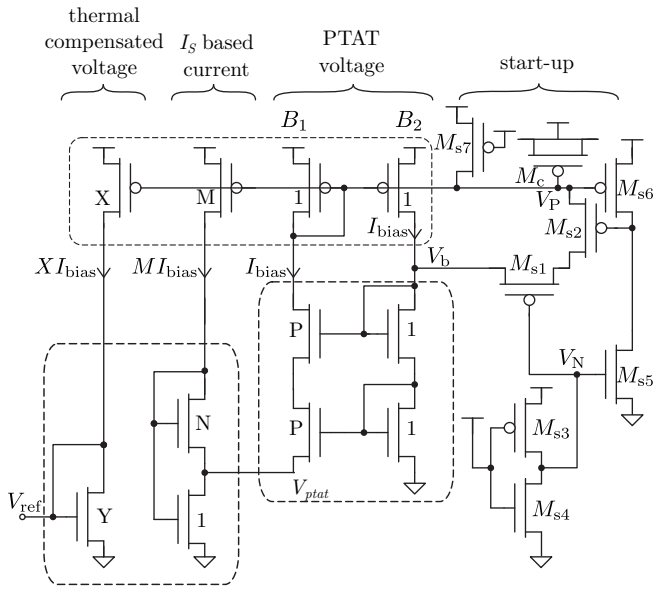

Figure 3.2 Low-voltage all-MOS circuit topology for the generation of I_S-based biasing currents and thermally compensated voltage references.

to avoid any off-chip analog components, specially for high precision and low cost. Moreover, an all-MOS solution is preferred over particular alternatives based on bipolar junction transistor (BJT) devices to avoid technology specific requirements. The self-bias circuit of Fig. 3.2 is based on a single-threshold all-MOS devices circuit to generate voltage reference thermally compensated and biasing currents based on MOS specific current (I_S) [125]. In what follows, the bulk terminal of each MOS device is connected to the corresponding supply voltage. Basically, the generator is composed of three cascaded sections: the PTAT voltage core (1:P), the specific current generator (M:N) and the thermally compensated output voltage reference itself (X:Y)

The principle of operation of the proposed voltage reference can be also split in the three stages of Fig. 3.2. Firstly, the 1:P matched pair is operated in weak inversion (i.e. subthreshold) saturation. In what follows, channel length modulation effects are neglected. According to the EKV model [126], the drain current expression for this region of operation is:

$$I_D = I_S e^{\frac{V_{GB}-V_{TO}}{nU_t}} e^{-\frac{V_{SB}}{U_t}} \quad \text{and} \quad I_S = 2n\beta U_t^2, \tag{3.2}$$

where I_S is the specific current, V_{TO} is the well known threshold voltage, while β is the current factor. The symmetry of the current mirror 1:P cause:

$$V_{ptat} = U_t \ln P. \tag{3.3}$$

Secondly, I_{bias} is obtained from the equivalent non-linear load attached to V_{ptat}. For such a purpose, 1:N matching group is operated in strong inversion saturation (upper) and conduction (lower) according to [126]:

$$I_D = \frac{\beta}{2n}(V_{GB} - V_{TO} - nV_{SB})^2, \tag{3.4}$$

$$I_D = \beta\left[V_{GB} - V_{TO} - \frac{n}{2}(V_{DB} + V_{SB})\right](V_{DB} - V_{SB}). \tag{3.5}$$

Taking into account both M and N scaling factors:

$$\begin{cases} MI_{bias} = \dfrac{N\beta_7}{2n}(V_{bias} - V_{TO} - nV_{ptat})^2, \\ (M+1)I_{bias} = \beta_7\left(V_{bias} - V_{TO} - \dfrac{n}{2}V_{ptat}\right)V_{ptat}, \end{cases} \tag{3.6}$$

the resulting biasing current is proportional to the specific current:

$$I_{bias} \doteq QI_S, \tag{3.7}$$

$$Q = \left[\frac{\ln P}{2(M+1)}\left(\sqrt{\frac{M}{N}} + \sqrt{\frac{M}{N} + M + 1}\right)\right]^2. \tag{3.8}$$

Thirdly and last, I_{bias} is X scaled through the mirror output and driven to the Y active load operating in strong inversion saturation as described by (3.4). The final voltage reference is found to be:

$$V_{ref} = 2n\sqrt{\frac{QX}{Y}}U_t + V_{TO}. \tag{3.9}$$

It is well known that the MOSFET threshold voltage exhibits a negative thermal coefficient (NTC) following the general model [127]:

$$V_{TO}(T) = V_{TO}(T_O) - \alpha\left(\frac{T}{T_O} - 1\right), \tag{3.10}$$

where α, T_{O} and T are the thermal coefficient for the particular CMOS technology, the reference and the working temperatures, respectively. Hence, combining the NTC behavior of V_{TO} in (3.10) with the PTAT law supplied by U_{t} in (3.9), thermal drifts in V_{ref} can be canceled. In particular, the design constraint for such an ideal thermal compensation is:

$$\sqrt{\frac{QX}{Y}} = \frac{1}{2n}\frac{\alpha}{U_{\mathrm{t}}(T_{\mathrm{O}})}, \tag{3.11}$$

resulting in the temperature independent reference:

$$V_{\mathrm{ref}} \equiv \alpha + V_{\mathrm{TO}}(T_{\mathrm{O}}). \tag{3.12}$$

An important issue in self-bias current sources is the existence of degenerate bias points. When the supply is turned on, all devices may remain off indefinitely because the positive feedback loop formation in branches B_1 and B_2 can also support a zero current state. This problem can be addressed by employing the start-up circuit of Fig. 3.2 that helps driving the circuit to the desired state. Considering the initial state, i.e. V_{DD} at 0 and MOS capacitor $\mathrm{M_c}$ uncharged, when V_{DD} starts to go up, V_{P} and V_{N} follows V_{DD}, and so $M_{\mathrm{s1,2}}$ start conducting and shunting charge from V_{P} to V_{b}. This shunting raises V_{b} so current starts flowing and the circuit starts up. Subsequently, when V_{DD} reaches the V_{TO} of M_{s4}, V_{N} goes to zero, thus switching off the start up circuit by turning off M_{s2}.

3.2 A 1.2-V 65-nm CMOS Electrochemical ΔΣM

The proposed extended-DR wide-range potentiostat-electrochemical ΔΣM of Fig. 3.3 has been integrated in TSMC 1.2-V 65-nm 1-poly 9-metal CMOS technology, available through the Europractice IC service [128]. Table 3.2 summarizes some of the main characteristics of this technology.

3.2.1 Full-Custom Schematic and Physical Design

Fig. 3.4 illustrates the CMOS building blocks at schematic level, including the transistors size and biasing details.

As stated in the design methodology of Chapter 2, the design parameters of the potentiostatic-amperometric ΔΣM must be determined in accordance with the

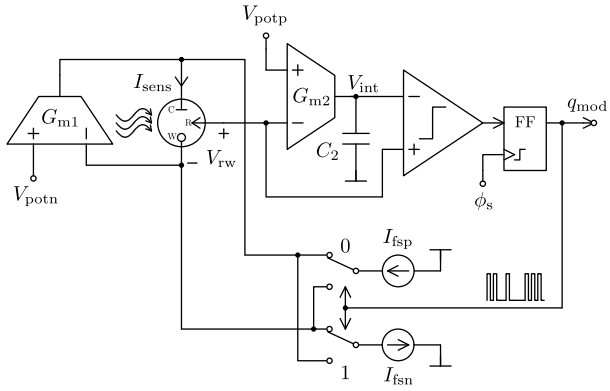

Figure 3.3 Extended-DR wide-range potentiostat second-order single-bit CT $\Delta\Sigma$M architecture integrated in TSMC 1.2-V 65-nm CMOS technology.

Process	Name	TSMC65
	Critical dimension	65 nm
	Triple well	Yes
	Number of metals	9
	Supply voltage	1.2 V / 2.5 V
Devices	N/P MOSFET regular V_{T0}	+0.31 V / −0.34 V
	N/P MOSFET low V_{T0} (LV)	+0.17 V / −0.23 V
	N/P Specific current (W/L)=1	660 nA / 230 nA
	Capacitor type	MiM
	Capacitor density	2 fF/μm^2
	Other options	Zero V_{T0}
	MOSFET model	BSIM3v3

Table 3.2 Main characterstics of the TSMC 1.2-V 65-nm 1P9M CMOS technology.

sensor specifications, i.e. τ_1 and I_{sens} full scale. In this sense, special attention is given to extend not only the potentiostatic range but also the amperometric dynamic range. For the latter, the biphasic current full scale of the feedback DAC is designed to be digitally programmable from $\pm$100 nA to $\pm$1.5 μA in 200-nA steps. Moreover, the electronic integrator time constant $\tau_2 = C_2/G_{m2}$ can be also tunnable from 0.5 ms to 3.3 ms in 0.4-ms steps by digitally controlling the current biasing of G_{m2} from $\pm$0.8 nA to $\pm$8 nA, respectively. To that extend, large variations in the electrochemical time constant τ_1 can be counterbalanced by properly setting the sampling frequency f_s, the electronic integrator time constant τ_2 and the biphasic current full scale, as referred in Section 2.1.3.

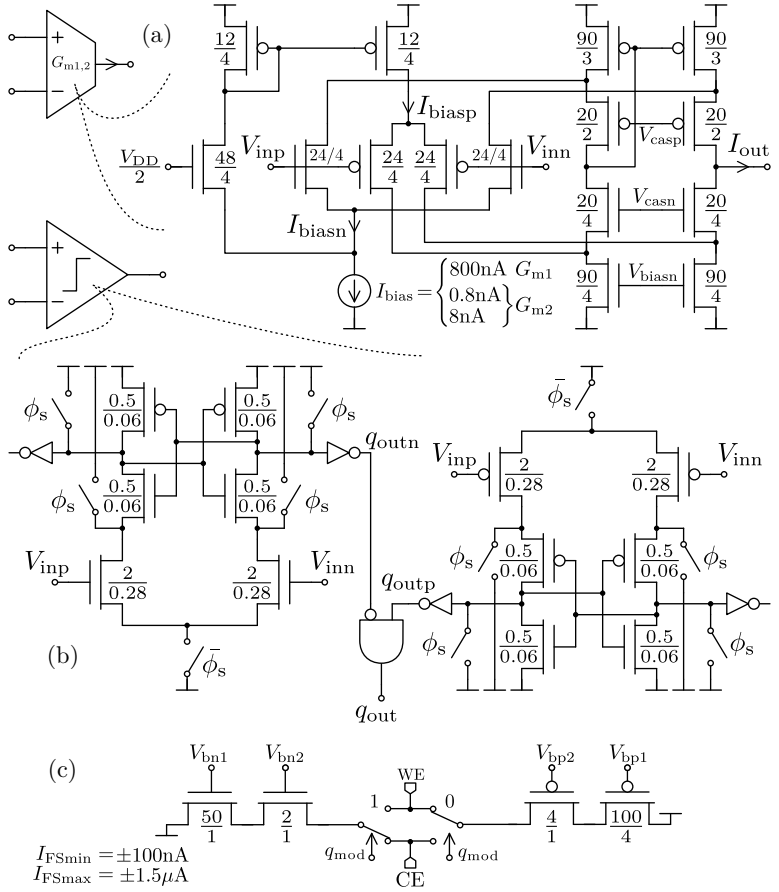

Figure 3.4 CMOS schematics of the rail-to-rail one-times current transconductor (a), rail-to-rail latched quantizer (b) and single-bit current feedback DAC (c) for the electrochemical ΔΣM of Fig. 3.3 in TSMC 1.2-V 65-nm CMOS technology. All devices dimensions are in μm.

The design of the electrochemical $\Delta\Sigma$M of Fig. 3.3 has been optimized for timming, performance, area and power, following the top-down design flow of Fig. 3.5. The full custom schematic and physical design were performed through the Cadence Virtuoso® [129] suite. Scientific Python (SciPy) [130] was also used in parallel to speed up data processing of the simulations results:

1. The top-down design starts with the electrical behavioral domain of the electrochemical $\Delta\Sigma$M of Fig. 3.3. All individual blocks are replaced by ideal Verilog-A [131] and SPICE [132] behavioral blocks such as voltage controlled voltage source (VCVS), voltage controlled current source (VCCS), S/H, capacitors and resistors, among others.

2. The electrical behavioral model is then simulated to verify that the design specifications are achieved. Further details to this electrical model are added and verified in terms of limited voltage operation, noise and second-order effects such as finite gain and slew rate are taken into account for a better approximation.

3. At the circuit level, a suitable circuit topology is carefully assigned to each of the system block. First, each block at transistor level is verified as an independent unit against specifications and not in the context of the entire system. Once verified separately, the blocks are then combined and verified together.

4. All circuit variables are fine-tuned and optimized to meet the performance targets. Mismatch and process effects are carefully assessed through Montecarlo analysis, and overall system functionality secured for PVT variation effects.

5. Next step involves the full-custom mask layout design accounting general matching rules and decoupling guidelines for better optimization.

6. Physical verification such as design rule checking (DRC) and layout versus schematic (LVS) are performed and finally, detailed circuit level simulations are carried out with extracted layout parasitics, thus completing the top-down methodology. If the design does not satisfy the design specifications, reiterations are required to revert back to previous design steps.

Fig. 3.6 shows the detailed layout of the proposed electrochemical $\Delta\Sigma$M of Fig. 3.3 for the TSMC 1.2-V 65-nm CMOS technology. The overall circuit area, excluding I/O pads, is around 0.07 mm^2. It is clear that most of the Silicon area is occupied by the second stage of the noise shaper (G_{m2}-C_2) due to the large time constants involved. The large-size devices present in both transconductor differential pairs

G_{m1} and G_{m2} are for matching purpose with the aim of minimizing potentiostatic shifts. As discussed in Section 2.1.3, the main noise contributions come from the CMOS current sources of the feedback DAC, whose flicker noise is not shaped by the ΔΣ loop. Unfortunately, the architecture in Fig. 3.3 does not benefit from a flicker noise cancellation mechanism. Thus, the large area occupied by the current feedback DAC (6480 μm^2) and its current bias (on-chip current reference of Fig. 3.2) responds to the need of minimizing their low-frequency noise contribution.

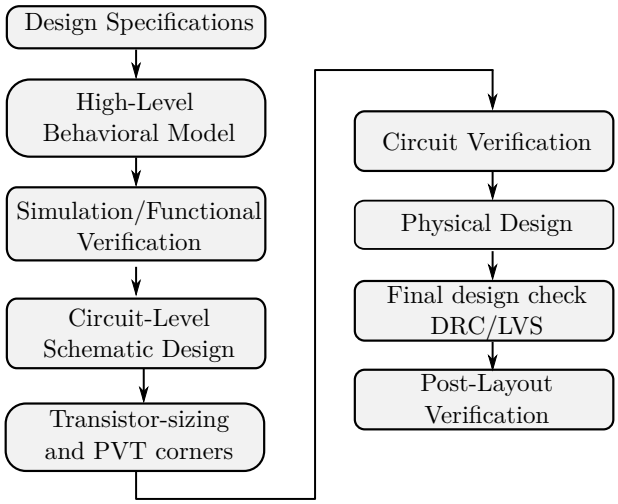

Figure 3.5 | Full-custom analog IC design flow and methodology employed for the electrochemical ΔΣM of Fig 3.3.

3.2.2 Simulation Results

The post-layout simulation results presented in this section have been obtained for a typical electrochemical sensor impedance $R_{ct} = 500$ kΩ and $C_{dl} = 300$ nF [12]. Experimental EIS measurements of the sensor were performed using Autolab PGSTAT302N potentiostat coupled with Eco Chemie FRA32M impedance analysis module [12] from Metrohm Autolab B.V., The Netherlands. Considering $\tau_1 = 0.15$ s, the following design parameter values are chosen: $G_{m1} = 9$ μS, $G_{m2} = 20$ ns, $C_2 = 66$ pF ($\tau_2 = 3.3$ ms). Stability constrains impose $f_s \geq 300$ Hz, so $f_s = 512$ Hz is finally selected, which is equivalent to OSR = 256 for 1-Hz bandwidth.

The simulated transient response of Fig. 3.7 shows how the electrochemical ΔΣM response under a 200-mHz harmonic stimulus with single 1.2-V supply. Fig. 3.7(a)

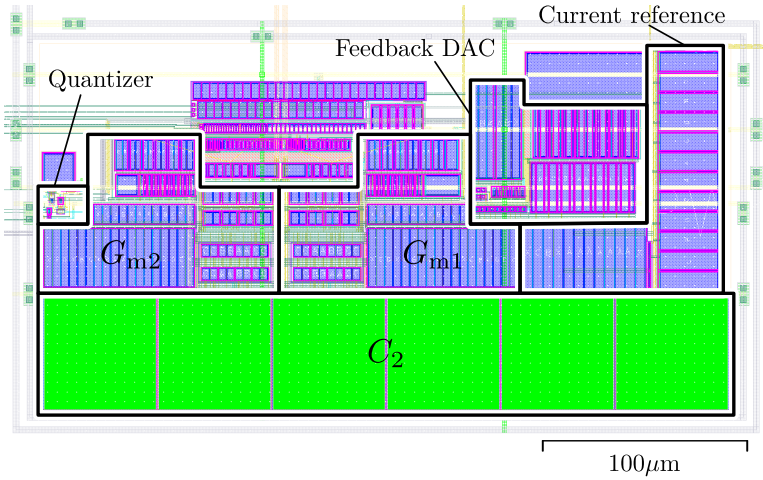

Figure 3.6 Physical layout of the electrochemical ΔΣM of Fig. 3.3 in TSMC 65-nm 9-metal CMOS technology. Core bounding box is 350 μm × 200 μm (0.07 mm^2).

plots the modulated signal q_{mod} and its digital average d_{out} after applying a third-order Butterworh low-pass filter as digital decimator. In Fig. 3.7(b), it can be noticed how the negative feedback loop around the trasconductance G_{m1} forces V_{w} to follow $V_{\mathrm{potn}} = V_{\mathrm{DD}}/2 = 0.6$ V. The ns-range spikes are due to switching artifacts. Furthermore, the ΔΣM feedback loop forces V_{r} and V_{int} to follow $V_{\mathrm{potp}} = V_{\mathrm{DD}}/2 = 0.6$ V, the ripple at the reference electrode V_{r} obeys expression (2.10).

Fig. 3.8 demonstrates the potentiostatic wide programmable range under low-voltage supply. Thanks to the differential control of the proposed architecture, the voltage between the working and reference electrodes V_{rw} is forced out to be the same as $V_{\mathrm{potp}} - V_{\mathrm{potn}}$. Simulation revels that a 2-V_{pp} potential window can be achieved under single 1.2-V supply. The top and bottom limits emanate from the output range of the current feedback DAC, which requires two over-drive voltages to maintain the cascode transistors in saturation operation. Since they are biased in weak inversion, the overdrive voltage is limited down to $3U_{\mathrm{t}}$, i.e. about 75 mV at room temperature.

The individual (g_{mn}, g_{mp}) and total (g_{mt}) transconductances over the common-mode input voltage V_{cm} of the rail-to-rail one-times current mirror biased in weak inversion of Fig. 3.4(a) is simulated in Fig. 3.9. Here, V_{cm} is swept from 0 to V_{DD} and the three regions are clearly visible. When V_{cm} is close to V_{DD}, the bias current I_{bias} flows entirely into the n-type pair. Since the tail current of the p-type

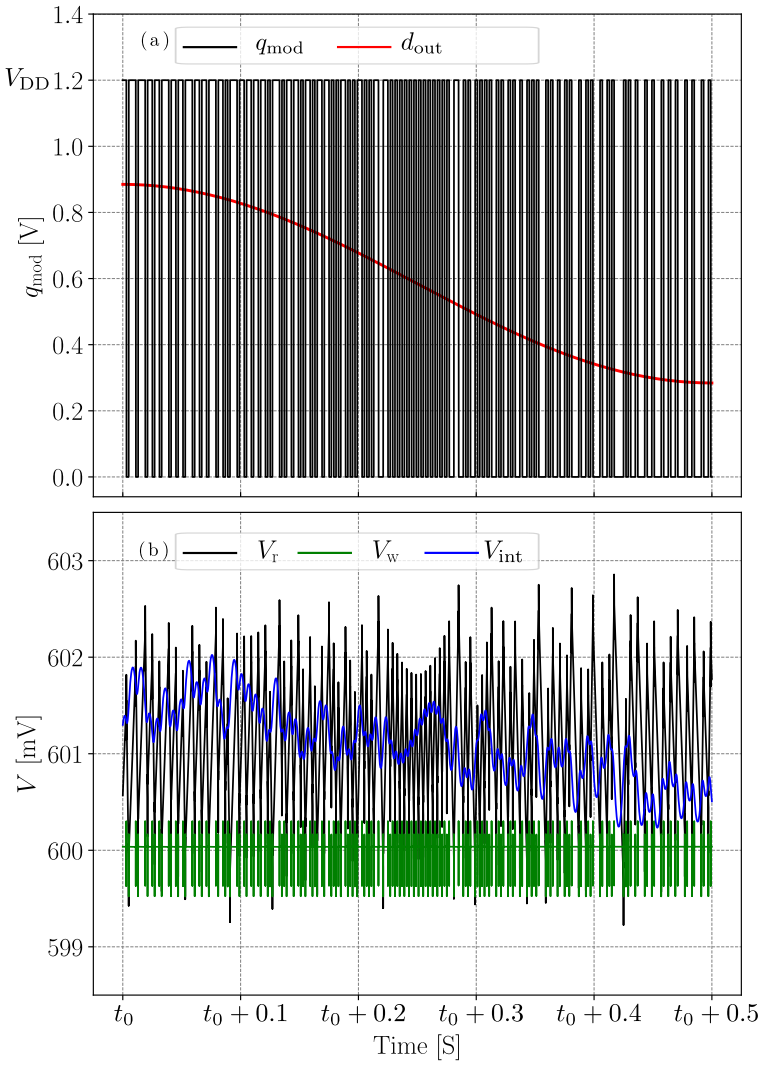

Figure 3.7 Simulated transient response of modulated (a) and internal (b) signals of the TSMC 1.2-V 65-nm electrochemical ΔΣM of Fig. 3.3. Configuration is $V_{\text{potn,p}} = V_{\text{DD}}/2 =$ 0.6 V and ±1.5-μA full scale.

channel is zero, g_{mt} is equal to g_{mn}. In the mid-supply stage, part of the current bias from the n-type is taken and steered it to the p-type pair through the one-times current mirror. As the sum of both tail currents is equal to I_{bias}, the total g_{mt} is kept constant. In the low range of V_{cm}, the bias current flows completely through the p-type pair. Since the current through n-type pair now is zero, and the sum of both tail currents is still equal to I_{bias}, the net g_{mt} is again kept constant. There is 'bump' in the middle of the g_{mt} plot corresponding to the transition of the complementary pairs.

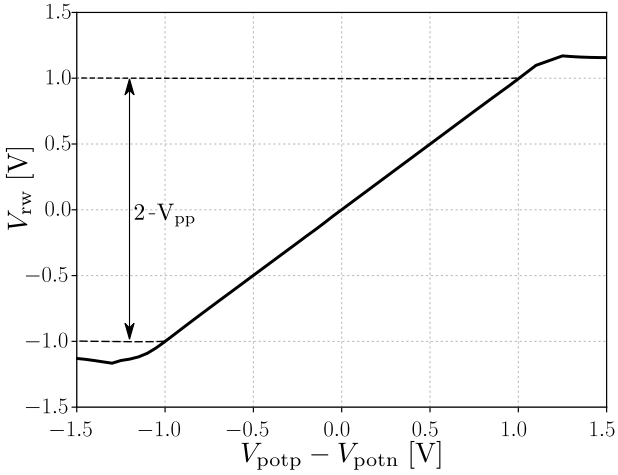

Figure 3.8 | Simulated potentiostatic range for the TSMC 1.2-V 65-nm electrochemical ΔΣM of Fig. 3.3.

Fig. 3.10 compares the output spectrum of the electrochemical ΔΣM of Fig. 3.3 with and without electronic transient noise, for the same -6 $\mathrm{dB_{FS}}$ 200 mHz sinusoidal input at 512 Hz and ±100-nA full scale. It can be observed that the high-frequency part of the spectrum, above the band of interest is preserved as it is dominated by the quantization noise. In the case of accounting the device noise, flicker noise is noticeably added to the low-frequency portion of the spectrum, giving a typical slope of -10 dB/decade.

The amperometric dynamic range extension concept is shown in Fig. 3.11, where the simulated signal-to-noise-distortion ratio (SNDR) curves at the minimum, half and maximum programmable DAC full-scale levels are plotted. With sustained $\mathrm{SNDR_{max}}$ values around 80 dB for each full scale, simulations revel a combined electrochemical current dynamic range of up to 105 dB.

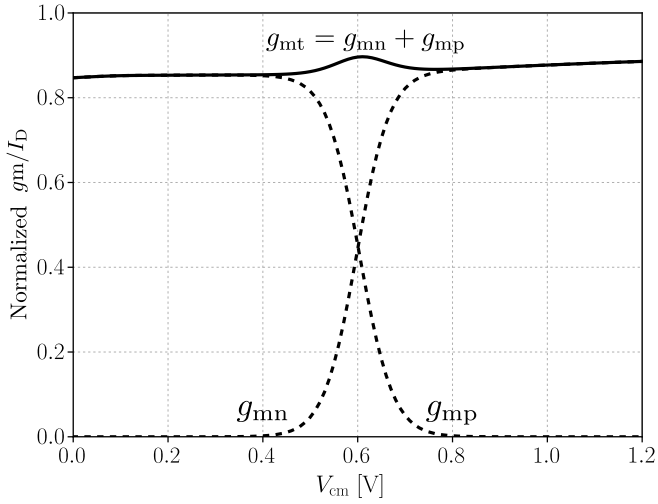

Figure 3.9 Normalized transconductance versus the common-mode input volatge of the rail-to-rail transconductors of Fig. 3.4(a) used in the TSMC 1.2-V 65-nm electrochemical $\Delta\Sigma$M of Fig. 3.3.

3.3 A 1.8-V 0.18-μm CMOS Electrochemical Smart Frontend

The proposed wide-range potentiostatic electrochemical $\Delta\Sigma$M with the flicker noise cancellation mechanism of Fig. 3.12 has been integrated in XFAB 1.8-V 0.18-μm 1P6M CMOS technology also available through the Europractice IC service [128]. Table 3.3 summarizes some of the main characteristics of this technology.
Apart from the electrochemical $\Delta\Sigma$M blocks and the current bias generator itself of Section 3.1, the following on-chip auxiliary modules have been also integrated in the smart sensor frontend of Fig. 3.12(b):

1. I^2C bus interface for both digital programming-in and read-out.
2. 7-bit pseudo-random address generation for the I^2C individual slave address assignment.
3. Power management unit (PMU) consisting on a 1.8-V capacitor-less (capless) linear regulator with PTAT voltage reference and power on reset (POR).
4. Two digitally programmable voltage sources for both potentiostatic references V_{potp} and V_{potn}.

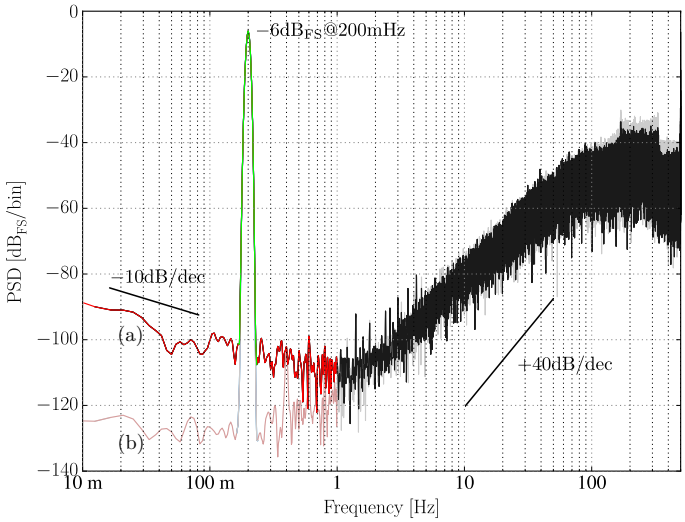

Figure 3.10 Post-layout simulation comparison of the output PSD with (a) and without (b) electronic transient noise of the electrochemical ΔΣM of Fig. 3.6. Configuration is $V_{\mathrm{potn,p}} = 0.6$ V and ±100-nA full scale.

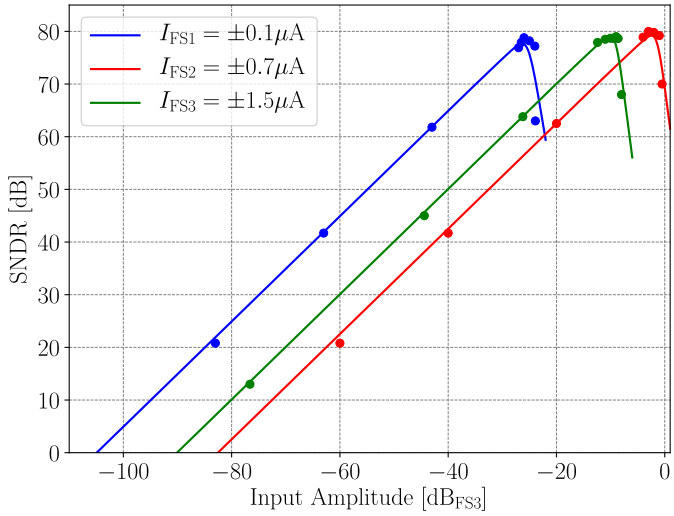

Figure 3.11 Post-layout simulated output SNDR for three programmable full scale values of the electrochemical ΔΣM of Fig. 3.6. Response to 200-mHz input and integrated in-band noise from 10 mHz to 1 Hz.

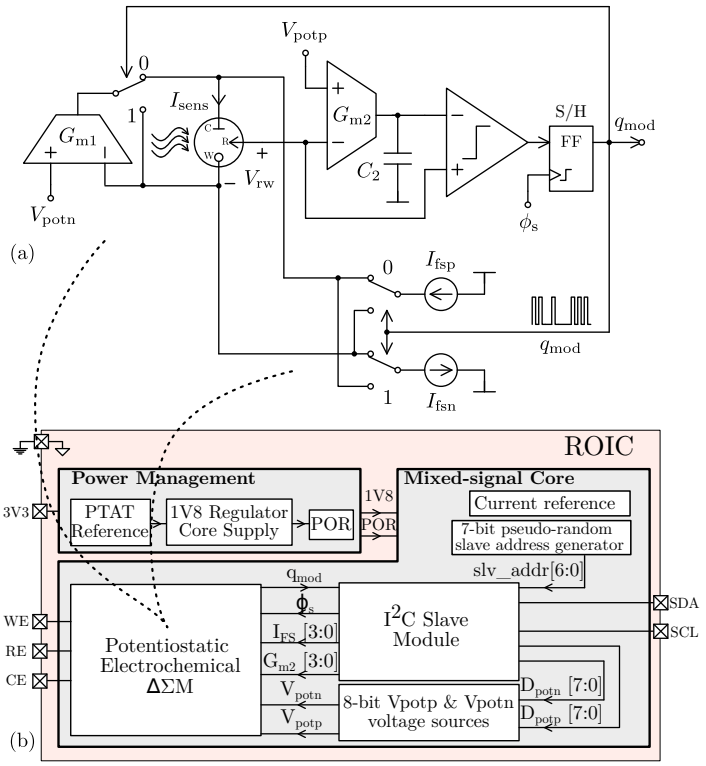

Figure 3.12 Proposed wide-range electrochemical potentiostatic ΔΣM with flicker noise cancellation architecture (a) and 7-pin SoC block diagram (b) integrated in XFAB 1.8-V 0.18-μm CMOS technology.

3.3.1 Mixed-signal Schematic and Physical Design

Fig. 3.13 depicts the CMOS building blocks introduced in Section 3.12, with the particular transistors size and biasing details for the smart electrochemical frontend of Fig. 3.12. Compared to the previous design of Section 3.2, the one-bit feedback DAC is scaled down in size. This reduction in transistor area proportionally increases the flicker noise coming from the feedback DAC sources, but it is revoke here thanks to the low-frequency noise cancellation mechanism.

The mixed-signal smart-sensor frontend includes a standard Inter-Integrated Circuit I^{2}C interface bus [133]. This synchronous, multi-slave, serial digital I/O protocol allows to decrease the number of pads for the programming-in and read-out

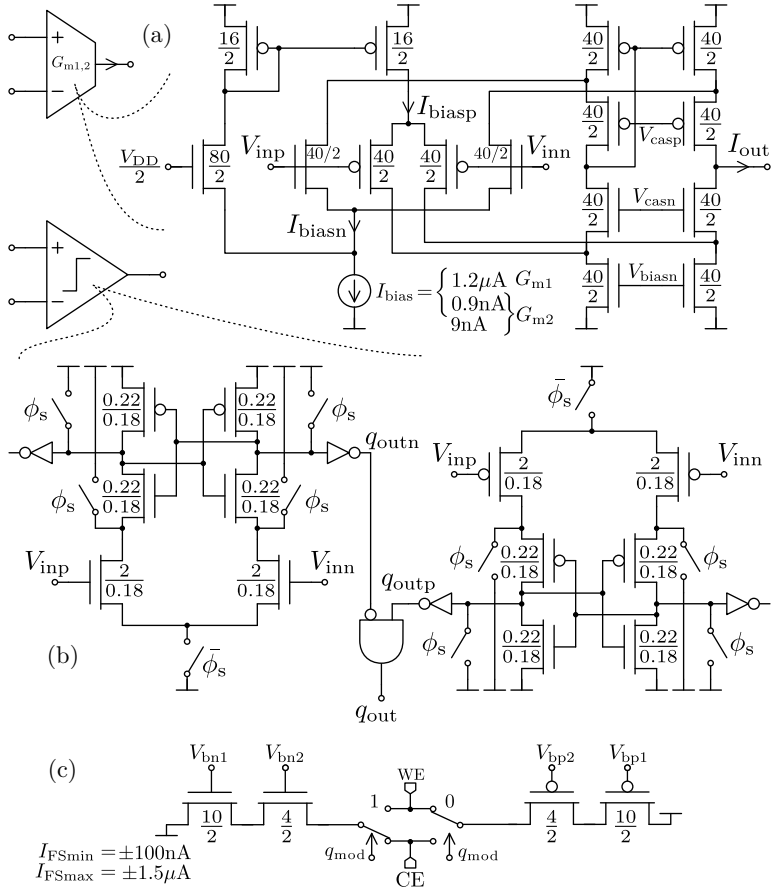

Figure 3.13 CMOS schematics of the rail-to-rail one-times current transconductor (a), rail-to-rail latched quantizer (b) and single-bit current feedback DAC (c) for the electrochemical $\Delta\Sigma$M of Fig. 3.12(a) in XFAB 1.8-V 0.18-μm CMOS technology. All devices dimensions are in μm.

Process	Name	XFAB-XH018
	Critical dimension	0.18 μm
	Triple well	Yes
	Number of metals	6
	Supply voltage	1.8V / 3.3V
Devices	N/P MOSFETregular V_{T0}	+0.58 V / −0.6 V
	N/P MOSFET low V_{T0} (LV)	+0.17 V / −0.23 V
	N/P Specific current (W/L)	495 / 285 nA
	Capacitor type	MIM
	Capacitor density	1 fF/μm^2
	Resistor type	High-Ω Poly
	Resistor density	6.7 kΩ/□
	Other options	Zero V_{T0}
	MOSFET model	BSIM3v3

Table 3.3 Main characteristics of the XFAB 1.8-V 0.18-μm 1P6M CMOS technology.

comunication, which is of special interest for the low-cost assembly proposals of Chapter 4. The general idea is to translate serial data line (SDA) and serial clock line (SCL) into a simple series of 8-bit read/write commands for accessing a set of user-defined registers in the smart frontend. As a result, only two bus lines are required to control the extensive system configuration. These registers are defined as either configuration registers (read/write) or status registers (read-only). The I^2C slave consists of two main blocks as described in Fig. 3.14(a) called I^2C Control Unit and Configuration/Status register banks.

The Control Unit is a state machine that continuously monitors the state of the SCL and SDA bus lines and generates the appropriate control signals. Basically, to begin a data transfer, the state machine waits for a start condition and compares whether or not the slave address on the bus corresponds to the 7-bit slave address *slv_addr*. If the slave address does not match, then the slave will not acknowledge the master and it will revert back to its idle state waiting for the next start condition. Once the controller has been addressed correctly, the master may send either a register write or a register read to the slave. The I^2C command sequence understood by the slave controller is summarized in Fig. 3.14(b).

The configuration and status registers of Fig. 3.14(a) are 8-bit wide with up to 128 in each bank. In the case of configuration registers, they are read/write addressable and four are employed here to configure the electrochemical ΔΣM parameters, according to the mapping of Table 3.4. As it can be seen, two registers are dedicated to set the 8-bit potentiostatic signals V_{potp} and V_{potn}, one register to program both

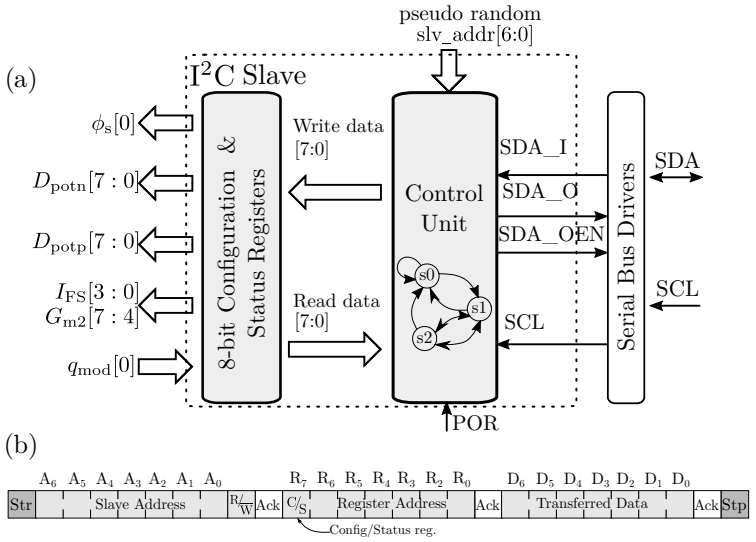

Figure 3.14 | I²C slave serial interface controller architecture (a) and command sequence (b) as included in the electrochemical smart frontend of Fig. 3.12(b).

the biphasic current full scale $I_{fsp,n}$ from ±100nA to ±1.5μA in 200-nA steps and the electronic integrator time constant τ_2 range from 0.5ms to 3.3ms in 0.4-ms steps, and a last register is used to provide the 1-bit sampling clock frequency f_s to the ΔΣM. As for the status registers, they are read-only and one is assigned for reading out the single bit electrochemical modulated signal q_{mod}.

Address	Symbol	Function	Programmability
03h	I_{FS}[0:3]	Current full scale	±100 nA/±1.5 μA (200 nA/step)
03h	G_{m2}[7:4]	Time constant τ_2	0.5 ms/3.3 ms (0.4 ms/step)
43h	f_s[0]	Sampling clock	Externally through "general call"
07h	D_{potn} [0:7]	V_{potn} signal	0 V/1.6 V (12.5 mV/step)
08h	D_{potp}[0:7]	V_{potp} signal	0 V/1.6 V (12.5 mV/step)

Table 3.4 | I²C dedicated configuration registers description employed for the control of the smart electrochemical frontend of Fig. 3.12.

The I^2C interface is customized to address every device connected to the I^2C bus at the same time by using a "general call" (address 0). However, if a device does not need any of the data supplied within the general call structure, it can ignore this address. If a device does require data from a general call, it behaves as a slave-receiver [133]. This feature is of especial interest when multiple slaves (front-ends) share the same I^2C bus. Being the $\Delta\Sigma$M sampling frequency generated by toggling one bit from one of the I^2C configuration registers, a general call can well be employed to simultaneously provide the f_s to each of the individual slaves that are connected to the same I^2C bus. This solution allows to monitor simultaneosly a ROICs network by using only two general-purpose I/O pins per chip.

The design of the I^2C slave interface has been optimized for area, timing and power, following the design flow of Fig. 3.15.

1. The top-down design starts with the synthesizable hardware description level (HDL) the register transfer level (RTL) employing Verilog [131]. This is first verified for functional correctness by logic simulation.
2. The Verilog HDL is then synthesized with Cadence Genus® [129] tool to be converted down to a gate-level description and mapped into the standard-cell digital library of the target CMOS technology.
3. The gate-level netslist obtained from the synthesis tool now is passed through the Verilog simulator. The output of the gate-level simulation is compared against the simulation output of point 1 in order to verify that the implementation is correct.
4. The already verified gate-level netlist is then imported into Cadence Innovus® [129] tool for physical place and route. The main steps carried in the layout design flow are:
   (a) Floorplanning: definition of the core area (containing the cells arranged in rows) and I/O area (containing power/ground rings and I/O pins).
   (b) Placement: I/O ports and cells placed in the allotted rows.
   (c) Clock tree: to minimize skew and insertion delay.
   (d) Signal routing: cells and I/O pins connected together by routing the circuit nets.
5. Physical verification of the final layout design, which includes, but not limited to, DRC, LVS and antenna rule checking.

The semi-custom digital IC design methodology of Fig. 3.15 employed for the I^2C slave of Fig 3.14 was done in collaboration with the research group Centro de

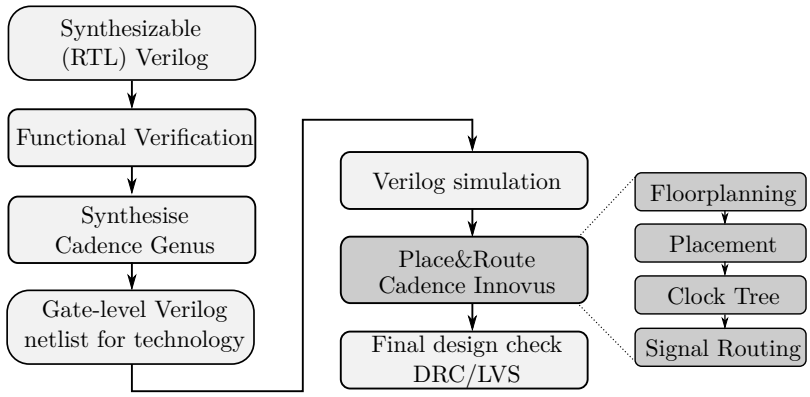

Figure 3.15 | Semi-custom digital IC design flow and methodology employed for the I^{2}C slave of Fig 3.14.

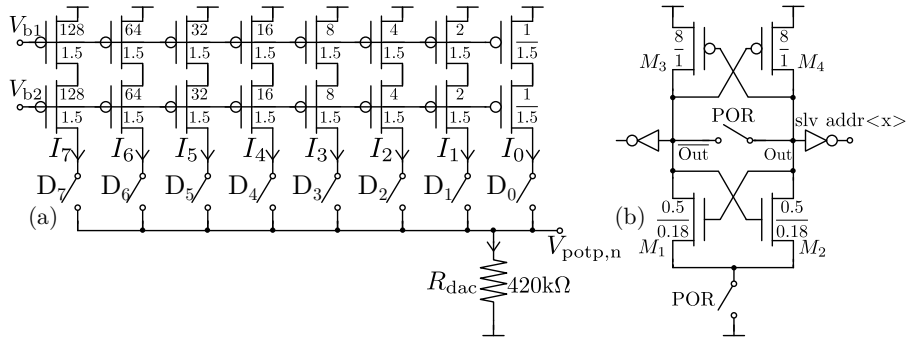

Figure 3.16 | CMOS 8-bit binary-weighted switched-current DAC for $V_{potp,n}$ references (a) and bit slice of the I^{2}C pseudo-random slave address generator (b) as used in the SoC of Fig. 3.12(b). All device dimensions are in μm.

Micro y Nanoelectrónica del Bicentenario (CMNB) from the Instituto Nacional de Tecnología Industrial (INTI), Argentina.

Concerning the supporting blocks of the smart frontend of Fig. 3.12(b), two 8-bit binary-weighted current-steering DAC with a resistive load are integrated on-chip to supply the potentiostat with both analog references V_{potp} and V_{potn}, as illustrated in Fig. 3.16. Their potential can be either kept constant for a certain time or scanned over a potential range, allowing different waveform signals to stimulate the cell in CV, square-wave voltammetry or chronoamperometry. Each input bit

D drived through the I^{2}C slave configuration register of Fig 3.14 controls a binarly weighted current with respect to a unit value. D_0 stands for the least significant bit (LSB) and D_7 the most significant bit (MSB). The current sources are scaled up by a factor of two from one bit to the next. The $V_{\mathrm{potp,n}}$ resolution is then defined by:

$$V_{\mathrm{LSB}} = \frac{1}{2^8 - 1} R_{\mathrm{dac}} \sum_{x=0}^{7} I_x. \tag{3.13}$$

The I^{2}C slave address is 7-bit wide and it is bitwise randomly generated by the circuit proposed in Fig. 3.16(b), which is based on a regenerative dynamic latched comparator [134]. First, POR is low, thus shorting both output nodes (Out and $\overline{\mathrm{Out}}$), and precharging them to the supply voltage. Then, POR changes to high to trigger the positive feedback of the latch, which unbalances the outputs and holds the resulting complementary state. Based on the influence of technology mismatch, one of the inverters will tend to be faster than the other, resulting in more ones/zeros generated at its output. PVT variations or coupled noise can disrupt this behavior by introducing biases that favor resolution towards one particular state. For this reason, transistors M_1 and M_2 are minimum in size to assure the technology mismatch variations dominate over other factors.

A fully integrated on-chip linear regulator is also implemented in the smart frontend of Fig. 3.12(b) to provide a regulated 1.8-V core supply from the 3.3-V external supply. Linear regulators are one of the most important blocks in any PMU. They are used where a stable voltage supply must be guaranteed regardless of any changes in the current load and the input supply [135]. Fig. 3.17(a) shows the topology of a CMOS linear regulator without external capacitor, also known as capless voltage regulator. It consists of an error amplifier (EA), a feedback resistor network formed by R_1 and R_2, a pass transistor M_{P}, and a voltage reference V_{ref}. The EA is reponsible of comparing the reference voltage with the output voltage obtained by the resistive feedback and driving M_{P} as a function of the comparison result. Assuming an infinite loop voltage gain, the output voltage is then determined by the ratio of the output resistors R_1 and R_2, and by the voltage reference:

$$V_{\mathrm{out}} = (1 + \frac{R_1}{R_2}) V_{\mathrm{ref}}. \tag{3.14}$$

Conventional linear regulator usually requires of an external capacitor to have an acceptable transient response over load current transitions and to guarantee the stability of the feedback loop. However, this solution is usually bulky and it consumes valuable area and pad count in system on chip (SoC) devices. For all these reasons, a fully integrated on-chip capless linear regulator is preferred. Fig. 3.17(b) shows the schematic view of this linear regulator including all device sizing for

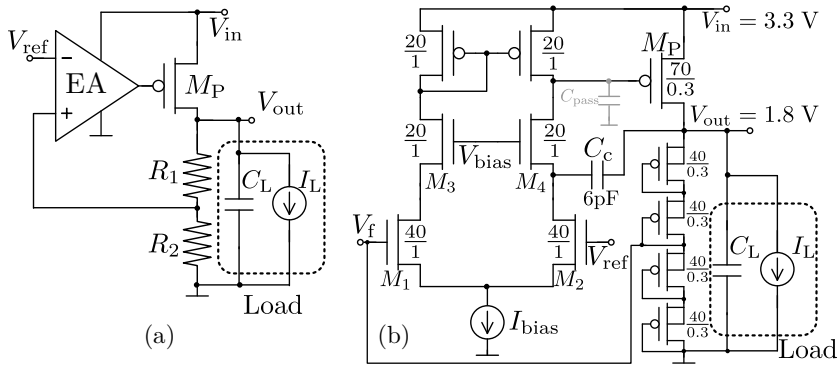

Figure 3.17 CMOS capless linear voltage regulator topology (a) and schematic (b) employed in the smart electrochemical frontend of Fig. 3.12(b). All devices dimensions are in μm.

XFAB 1.8-V 0.18-μm CMOS technology. Basically, it consists of a telescopic n-type differential-pair as EA, a p-type pass transistor M_P and a diode-connected feedback network. The use of a diode-connected network [136] allows important area savings compared to the resistive network of Fig. 3.17(a), which can demand large area when low-current consumption is required. In the diode-connected feedback network, the bulk-terminal of each transistor is connected to their corresponding source, so that all show identical I/V characteristics. As the same current flows through all transistors, the voltage V_f can be easily fixed. For example, sizing the transistors identically, each device drops the same voltage V_{ds} (V_{gs}), due to the same current operation. Hence, the voltage will divide evenly $V_f = V_{out}/2$. In terms of stability, the regulator is being stabilized with a cascode compensation technique [137], formed by the common-gate transistor M_4, acting as a current buffer, and the compensation capacitor C_c. Compared to Miller compensation, it provides better pole splitting and stability response, since it creates a LHP instead of a RHP zero.

Apart from ensuring a regulated supply voltage to the electrochemical $\Delta\Sigma$M of Fig. 3.12(a), the other purpose of this regulator is to coupe with the fast load current transitions of the digital I^{2}C interface of Fig. 3.12(b). The standard I^{2}C interface operates with a minimum clock of 100 kHz and so its fast spiky current consumption may result in large voltage transients at the output of the regulator, affecting the proper operation of the overall system or even overcoming the breakdown limits of the transistors. Consequently, the voltage regulator is designed with enough closed-loop bandwidth and slew rate to fulfill the required dynamic response imposed by the mixed-signal SoC.

The full custom analog and mixed-signal IC design methodology employed for the above supporting blocks has already been described in Section 3.2.1. Fig. 3.18(a) shows the physical layout of the smart sensor frontend in XFAB 1.8-V 180-nm CMOS technology. All main blocks are highlighted for comparison purpose. The overall core area is around 0.18 mm^2. Thanks to the synthesis and mapping processes of the I^{2}C slave, the design is optimized in terms of minimum area by having lesser number of cells and by replacing multiple cells with single cell that includes the same logical functionality. Consequently, the I^{2}C module can be condensed inside an area of 0.016 mm^2, which represents less than 10% of the overall size.

The complete chip exhibits a total size of 1.5 mm $\times$ 1.5 mm (2.25 mm^2) and it contains 10 I/O pads, distributed as follows: three analog pads for the electrochemical sensor, two analog pads for the external 3.3-V power supply and two digital bidirectional pads for the standard I^{2}C bus. The remaining three pads are not required for the performance and are only added for testing purposes. As it can be easily noticed in the floorplan of Fig. 3.18(b), the pad area and spacing have been extended to meet custom requirements of the low-cost IC assembly strategies described in detail in Chapter 4.

3.3.2 SoC Simulation Results

The load regulation capabilities of the linear regulator of Fig. 3.17(b) are evaluated considering the worst-case scenario, i.e. during the I^{2}C module operation with high-speed clocking. Fig. 3.19 shows the load transient response to abrupt load current changes, mostly demanded by the digital I^{2}C switching signals. The response time Δt_r (Δt_1, Δt_2) of the linear regulator is not only affected by the closed-loop bandwidth but also by the slew-rate as a consequence of the parasitic capacitor C_{pass} at the gate of the pass transistor M_{P} of Fig. 3.17. Since these current transitions are outside of the time response, the regulator cannot react to the load change. Consequently, the load transient response is degraded with voltage overshoots Δv_+ and undershoots Δv_- at the supply rail.

The results in terms of loop gain magnitude and phase of Fig. 3.20 are simulated for both minimum and maximum load current conditions (i.e. 0 and 2 mA) along with the equivalent load capacitance $C_{\text{L}} = 3$ pF imposed by the I^{2}C module and the remaining SoC blocks. Simulation results show that the DC gain is barely influenced by the current load. Furthermore, the overall loop stability is well ensured with a constant 57° phase margin, since the non-dominant pole p_2 does not depend on the current load and it causes no change on the phase margin. The main performance figures of the capless linear regulator of Fig. 3.18(a) are summarize in Table 3.5

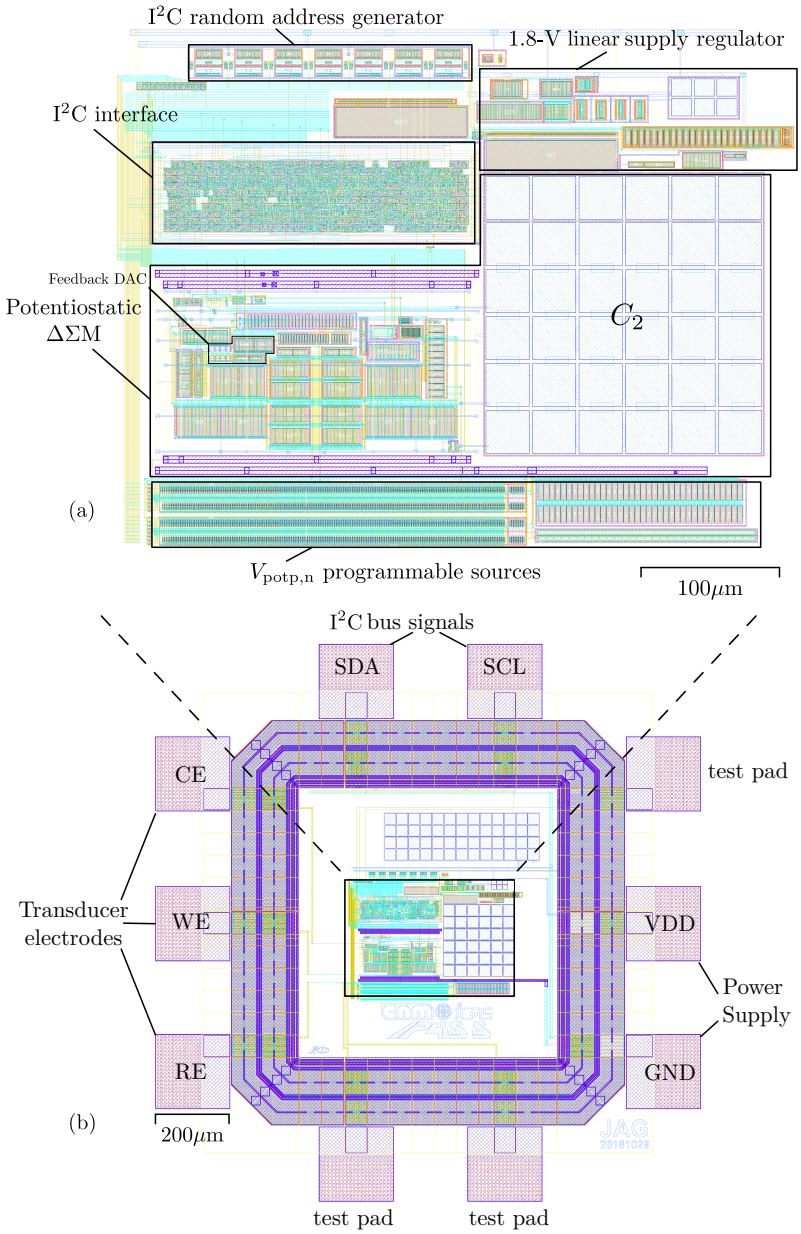

Figure 3.18 Physical layout of the core (a) and custom pad ring (b) of the smart-sensor frontend of Fig. 3.12 in XFAB 0.18-μm 6-metal CMOS technology. Chip size is 1.5 mm × 1.5 mm (2.25 mm^2). Core bonding box is 480 μm × 370 μm (0.18 mm^2)

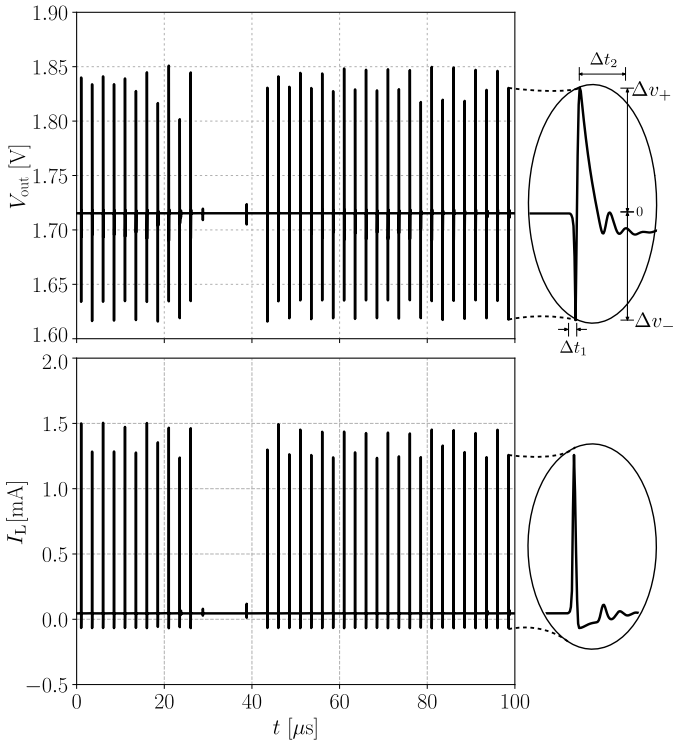

Figure 3.19 Post-layout simulation of the load transient response of the 1.8-V linear supply regulator of Fig. 3.18(a) when the I^2C interface is operating at 400-kHz clock.

Fig. 3.21 shows a 3-V_{pp} CV simulation example of the smart sensor frontend of Fig. 3.18 under 1.8-V voltage supply after applying digital averaging using a third-order Butterworh low-pass filter as digital decimator with cut-off frequency of 2.5 Hz. To carry out this mixed-signal simulation, a Verilog-A model of the electrochemical sensor was built as a look-up table of experimental current and potential V_{rw}-I_{sens} data.

Fig. 3.22(a) and (b) illustrate the efficiency of the proposed flicker noise cancellation for weak input signals. A complete different scenario is reported in Fig. 3.22(c), where the spectral response at half full-scale input is shown in order to highlight the overall good linearity of the proposed electrochemical $\Delta\Sigma$M of Fig. 3.18.

Fig. 3.23 compares the simulated SNDR curves at the minimum and maximum programmable DAC full-scale levels between the electrochemical $\Delta\Sigma$M design of

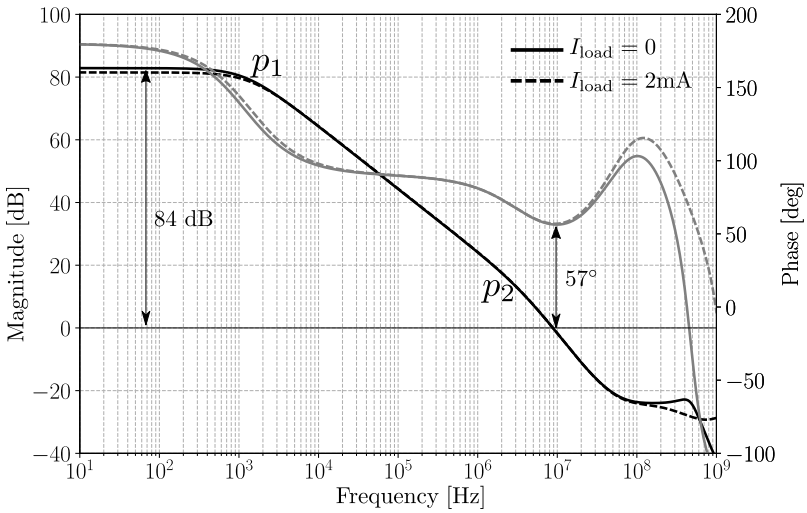

Figure 3.20 Post-layout bode simulation of the loop gain for the 1.8-V linear supply regulator of Fig. 3.18(a) at no-load ($I_{load} = 0$) and full-load ($I_{load} = 2$ mA) current conditions.

Parameter	**Typical**	**Units**
Supply voltage (V_{in})	3.3	V
Output voltage (V_{out})	1.8	V
Drop-out voltage (V_{do})	1.5	V
Quiescent current (I_q)	90	μA
Load current min ($I_{L_{min}}$)	0	μA
Load current max ($I_{L_{max}}$)	2	mA
Load current edge time ($t_{rise/fall}$)	2	ns
Load capacitance (C_L)	3	pF
Load transient regulator ($\Delta V_{out}+\Delta v$)	4.5	%
Phase margin (PM)	57	◦
Gain margin (GM)	22	dB

Table 3.5 Main performance characteristics of the capless linear regulator of Fig. 3.18(a)

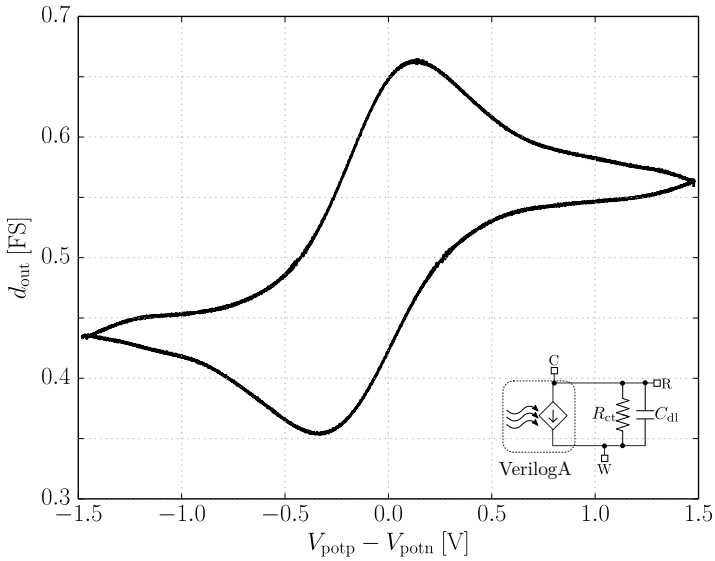

Figure 3.21 Post-layout simulation of a CV example at 15-mV/s scanning rate and ± 200-nA full scale for the smart sensor front of Fig. 3.18

Fig. 3.18 in XFAB 1.8-V 0.18-μm CMOS technology and of Fig. 3.6 in TSMC 1.2-V 65-nm CMOS technology. Although the 65-nm CMOS design exhibits higher SNDR_{max} values around 80 dB for input amplitudes close to the full-scale, the design in 0.18 μm CMOS along with the G_{m1} switching mechanism for the flicker noise cancellation achieves a higher dynamic range but it presents lower SNDR_{max} absolute values. This is due to the fact that the 1/f noise cancellation mechanism becomes more optimum for weaker signals, as stated in Section 2.3.

Finally, a quantitative comparison between the XFAB and TSMC electrochemical $\Delta\Sigma$M designs is presented in Table 3.6. As it can be observed, the TSMC design exhibits lesser potentiostatic voltage range, this refers to its lower supply voltage 1.2-V operation, when compared with the 1.8-V of the XFAB design. The larger area occupied by the current feedback DAC of the TSMC design responds to the need of minimizing their flicker noise contribution. Although the TSMC design brings higher SNDR_{max}, the 1/f cancellation mechanism of the XFAB design further extends the dynamic range up to 110 dB. The higher power consumption exhibited by the mixed-signal XFAB core design arises from the additional on-chip auxiliary modules, which increases overall SoC supply current consumption.

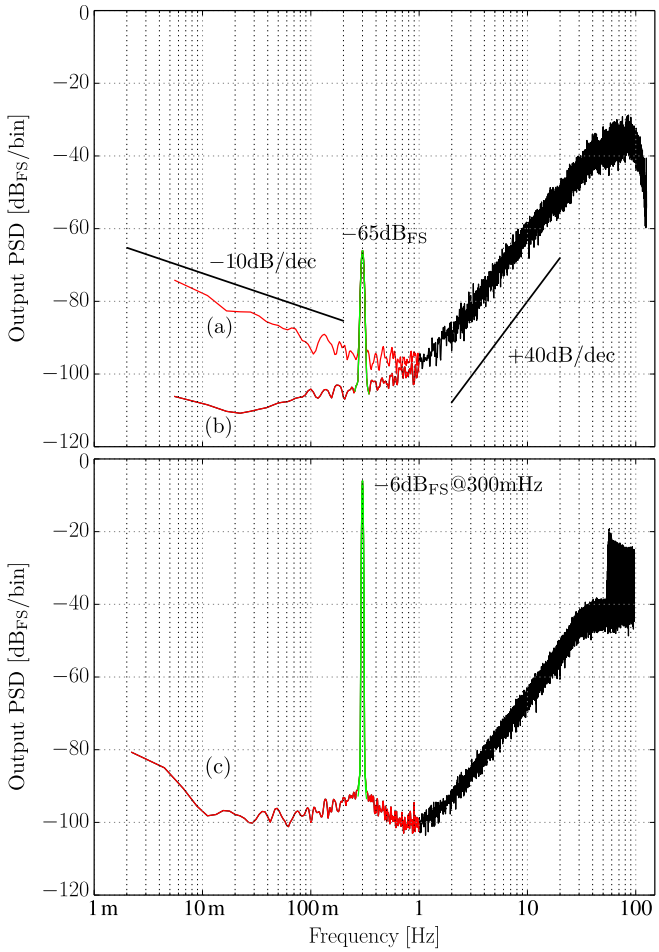

Figure 3.22 Post-layout simulation output PSD without (a) and with (b) the flicker noise mechanism for weak inputs for the smart sensor frontend of Fig. 3.18. Response to -6 $\mathrm{dB_{FS}}$ 200-mHz sinusoidal input (c). Configuration is $V_{\mathrm{potn,p}} = 0.9$ V and $\pm$100-nA full scale.

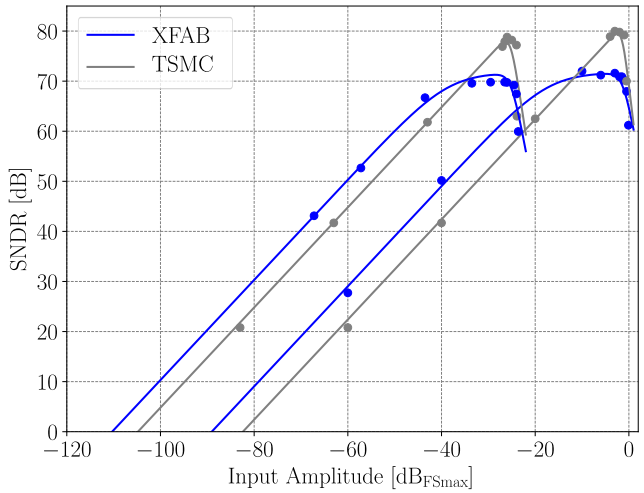

Figure 3.23 Post-layout simulated output SNDR comparison between XFAB G_{m1} switching $\Delta\Sigma$M of Fig. 3.12 and the TSMC 1.2-V $\Delta\Sigma$M design of Fig. 3.3. Response to 200-mHz input for minimum $\pm$100 nA and maximum $\pm$1.5 μA programmable full-scale levels.

Parameter		**TSMC**	**XFAB**	**Units**
Input	max. full scale	$\pm$1.5	$\pm$1.5	μA
	full-scale prog.	200	200	nA/step
	bandwidth	1	1	Hz
Potentiostat	voltage range	$\pm$1	$\pm$1.6	V
	voltage prog.	N/A	12.5	mV/step
	voltage ripple	<20	<20	mV_{pp}
	voltage offset ($\pm\sigma$)	N/A	10	mV_{rms}
ADC	$SNDR_{max}$ FS =$\pm$100nA	78	70	dB
	$\pm$1.5μA	79	72	
	composite DR	105	110	dB
	oversampling ratio	256	256	
Power	supply voltage	1.2	1.8	V
	core consumption	15	72	μW_{rms}
Silicon area	core	0.07	0.18	mm^2
	feedback DAC	6480	900	μm^2

Table 3.6 Post-layout simulation results comparison between the 1.2-V 65-nm CMOS TSMC design of Fig. 3.6 and the 1.8-V 0.18 μm XFAB design of Fig. 3.18

Low-Cost Flexible Hybrid Integration | 4

This chapter presents a single-substrate FHE solution intended for disposable electrochemical smart sensory devices, which exploits the ROIC capabilities of the electrochemical ΔΣMs presented in Chapter 3 together with the benefits of the inkjet printing technology. In order to achieve this objective, assembly trials with distinct dummy dice and custom flexible substrates have been conducted not only to test the electrical and mechanical ROIC attachment but also to explore intermediate testability, such as electrical performance and reproducibility. Indeed, multi-step processing flows for both the fabrication of an all-inkjet electrochemical cell and the wire-bonding free assembly of CMOS dice are presented. Furthermore, the three-electrode printed electrochemical cell is characterized in order to extract its equivalent impedance model. The chapter concludes with ACA-based flip-chip assembly trials of the dummy chips onto flexible substrates with a custom bonder setup for proper alignment, pressure and temperature control.

4.1 Flexible All-Inkjet Printed Electronics

The target disposable electrochemical smart sensor concept is shown in Fig. 4.1. It consists of an all-inkjet three-electrode electrochemical sensor directly printed onto a single low-cost PEN substrate that holds the electrochemical ΔΣM SoC bare die of Fig. 3.18(b) and hosts all required printed contacts and interconnections. In addition, the 1-mm pitch flexible flat connections allow to externally supply, via a 4-pin zero insertion force (ZIF) connector, the required power (i.e. VDD and GND) and standard I^2C communication (i.e. SDA and SCL) to the ROIC.

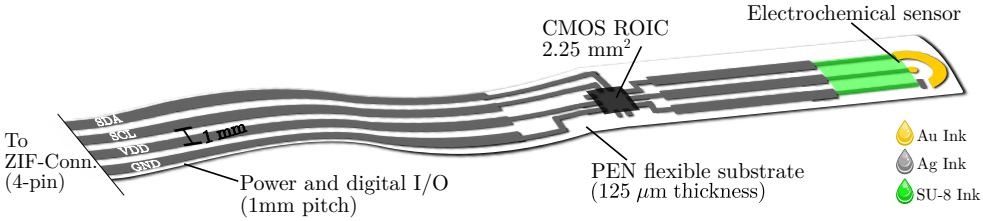

Figure 4.1 | Illustrative view of the target disposable smart sensor prototype. Approximate size is 10 cm × 0.4 cm. Not to scale.

The success of the inkjet printing in the FHE firmly relies on the availability of functional materials. Concerning the flexible substrate, PEN films are promising candidates for disposable devices because of their attractive benefits in terms of flexibility, low-cost and availability. However, all demanded manufacturing processing steps have to be performed at low temperatures (<160 °C) due to their limited heat capabilities. In this sense, the FHE prototype is constructed in a 10 cm × 0.4 cm 125μm-thick PEN polymeric film Q65HA from DuPont Teijin Films Ltd., USA. The long aspect ratio is chosen to demonstrate the entire system flexibility.

The equipment employed for printing the ink layers of Fig. 4.1, such as IC contact pads, conductive layers and the sensor three electrodes, is the CeraPrinter X-Series, a piezoelectric DOD printer fabricated by MGI Digital Graphic, France. All layout features have been printed using 10 pL and 1 pL inkjet cartridges from FUJIFILM Dimatix Inc., USA, with a 16-nozzle print head. Concerning the conductive inks, the most frequent solutions are based on metal nanoparticles [138]. These inks consist of colloidal suspensions of nanoparticles that can be produced in significant amounts, spread in high concentrations and produce good conductivity. Nevertheless, sintering is generally required, in which the structures are heated in order to evaporate solvents and fuse individual particles into a dense structure with high conductivity [139]. The silver-based nanoparticle ink Orgacon TM SI-J20x from Agfa-Gevaert, Belgium, is chosen here for printing the contacts and interconnections, as shown in grey in Fig. 4.1, due to its low-cost, high conductivity, resistance to oxidation, low curing temperature, and good adhesion with substrates. The metal electrode materials commonly used in electrochemical sensors are noble metals like Ag and Au because of their good chemical stability and electrical conductivity [28]. Concurrently, these metals have also been reproduced into inks suitable for inkjet printing. For the manufacturing of the three-electrode electrochemical sensor, the silver-based nanoparticle ink is also selected for the geometry of the pseudo-RE. Besides, the low-temperature curing Au nanoparticle ink Drycure Au-JB 1010B from C-INK, Japan, is employed to print the 200μm-

diameter WE and also the CE. For the passivation of all electrodes the SU-8 ink 2002 from MicroChem, USA, is selected. All these inks exhibit DOD inkjet compatible specifications, which are shown in Table 4.1.

Nanoparticle Ink	**Ag**	**Au**	**SU-8**	
Particle size	100	-	-	nm
Surface tension	40	32.8	30	mN/m
Curing process	>120 °C	>120 °C	UV	
Density	1.3	1.13	1.12	g/cm^3
Shelf life	6	6	12	months

Table 4.1 Main parameters of the nanoparticles inks employed for the development of the disposable and flexible smart electrochemical sensor of Fig. 4.1.

4.2 Sensor-on-Flex Technology

4.2.1 All-Inkjet Printing Process

The all-inkjet three-electrode 0.2mm^2-WE electrochemical sensor of Fig. 4.1 has been fabricated following a similar manufacturing process to that described in [140]. Fig. 4.2 depicts the flow and steps carried during the inkjet printing. The initial step is the printing of the Ag nanoparticle ink for the development of the pseudo-RE layout and the signal connectivity of the three-electrode structure. After the Ag deposition step, the ink cartridge is replaced by another cartridge containing the Au nanoparticle ink for the layout of the WE and CE. Thermal treatments are employed for both printed inks. The ink layers are first dried at 100°C for 5 min to remove all solvents and then sintered at 150°C for 30 min to ensure electrical conductivity. This two-step process is particularly crucial in the case of the gold ink. If the Au ink is not previously dried and cured directly at 150°C, intense crack formation may appears along the layer, reducing its conductivity [140]. The active electrode and the connections areas are precisely delimited by printing an insulating layer formed by SU-8 ink dielectric on top, as illustrated in Fig. 4.2(c). Indeed, SU-8 is a photoresist ink, which has been found to be a very good candidate for passivation of electrochemical sensors as it helps to prevent device degradation against environmental conditions, it exhibits a high chemical resistivity, favorable thermal stability, low temperature curing and also optical transparency [141]. Finally, the curing of the SU-8 layer is completed in two steps, as shown in Fig. 4.2(d): first it is heated at 100 °C for 5 min for solvent evaporation, and subsequently is cured by ultraviolet (UV) treatment for 15 s.

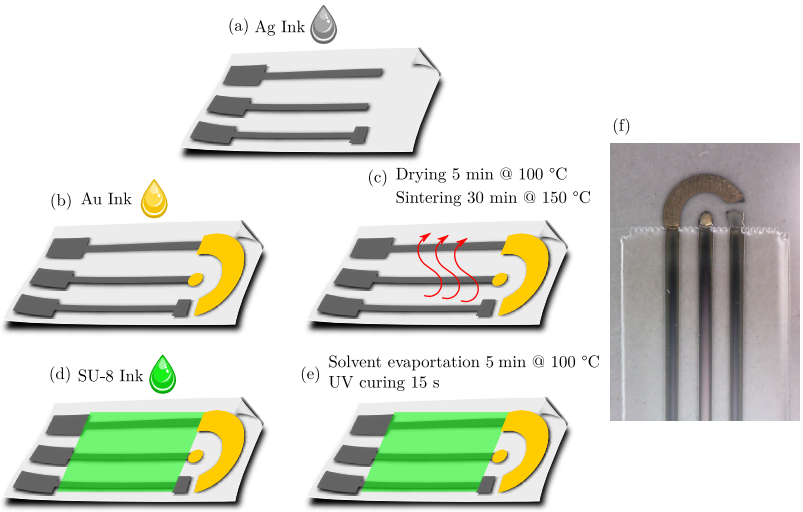

Figure 4.2 Inkjet-printed manufacturing process for the three-electrode electrochemical sensor. Ag (a) and Au (b) depositions, thermal drying and sintering of Au and Ag (c), SU-8 deposition (d) curing (e) and sample example (f). WE diameter is 0.2 mm^2. Drawings not to scale.

4.2.2 Electrochemical Cell Characterization

The characterization of the all-inkjet electrochemical cell of Fig. 4.2(f) was carried out by combining CV and EIS analysis techniques. The use of such electrochemical measurements enables a better understanding of the redox process and brings a well approximation of the equivalent impedance of the electrochemical cell without causing distress to the overall operation. The CV experiment was performed using μAutolabIII/FRA2 potentiostat from Metrohm Autolab B.V, The Netherlands. The impedance spectra measurements were performed using a Solartron Analytical SI 1287 potentiostat coupled to a Solartron Analytical 1260 impedance/gain-phase analyzer module both from Ametek Inc., USA.

Prior to the impedance measurements, the electrochemical response of the inkjet-printed cell of Fig. 4.2(f) was analyzed by CV with an equimolar solution of 2 mM ferri/ferrocyanide in 0.1 M KCl, as shown in Fig. 4.3(b). Ferri/ferrocyanide is one of the best redox species for electrochemical characterization due to the fact that has a well-known electrochemical behavior, it is soluble in aqueous solutions, it has a redox potential close to 0 V vs. Ag/AgCl and the redox pair is highly reversible [28]. The peak position and current density were compared with the

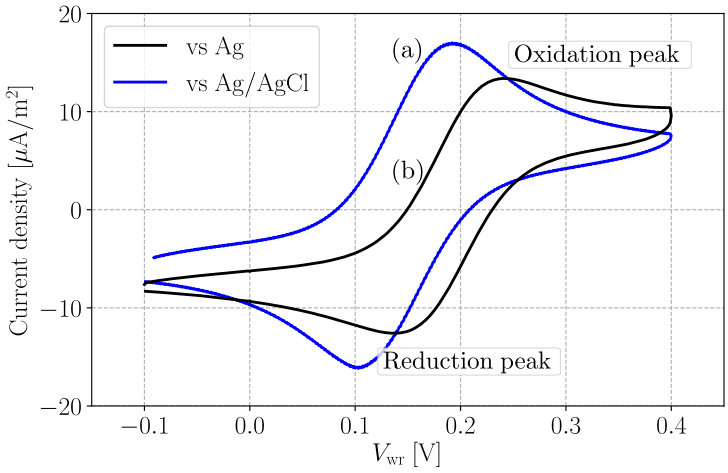

Figure 4.3 Experimental CV at 80 mV/s for 0.1M KCl and 2-mM equimolar mixture using commercial desktop instruments. Comparison of Ag-RE 0.2mm^2-WE of Fig. 4.2(f) (a) against standard Ag/AgCl-RE 1mm^2-WE (b).

response of an standard three-electrode cell, shown in Fig. 4.3(a), constituted by a conventional Ag/AgCl (KCl 3 M) as RE and Pt as CE and 1mm^2-WE. A potential sweep was performed from −0.1 to 0.4 V with 80 mV/s of scan rate for both electrochemical cells. The inkjet printed Ag pseudo-RE exhibited a small potential shift (around 40 mV) compared with the classical Ag/AgCl RE. The CV response of the inkjet-printed cell of Fig. 4.3(b) indicates that the ferri/ferrocyanide solution was oxidized at the potential of 0.25 V. In the reverse scan, a reduction peak was easily observed at 0.15 V, obtaining a standard reduction potential value of 0.19 V (vs. pseudo-Ag). Evidently, since the WE area is smaller for the inkjet printed cell, the current values obtained are much lower compared to those obtained for the conventional cell. For this reason, both responses were compared in current density, taking into account the area of both WEs. The lower peak values given by the inkjet printed cell could be related to imperfections on the electrode surface, reducing its effective area.

Once the DC redox potentials are properly identify, the EIS is performed. The main reason to perform the EIS tests after the CV is to be able to estimate the cell equivalent Randles circuit accounting the impedance related to the Faradaic and non-Faradaic processes of the electrochemical system (e.g. the resistance of the solution and the double layer capacitance). By performing EIS biased at the redox potential, the Faradaic impedance is triggered and, consequently, the charge

transfer resistance may be evaluated. The extracted EIS data of the electrochemical cell is represented through the Nyquist and Bode plots of Fig. 4.4. EIS is recorded in the frequency range of 10 mHz to 0.5 MHz (at 10 steps/dec) for an AC amplitude of 10 mVrms and a DC potential V_{wr} of 0.25 V corresponding to the oxidized peak observed in the CV of Fig. 4.3. The simplified expression for the Randles equivalent spectral impedance of the electrochemical sensor is:

$$Z(\omega) = (R_{\mathrm{s}} + R_{\mathrm{ct}}) \frac{j\omega R_{\mathrm{s}} \frac{R_{\mathrm{ct}} C_{\mathrm{dl}}}{R_{\mathrm{s}} + R_{\mathrm{ct}}} + 1}{j\omega R_{\mathrm{ct}} C_{\mathrm{dl}} + 1} \tag{4.1}$$

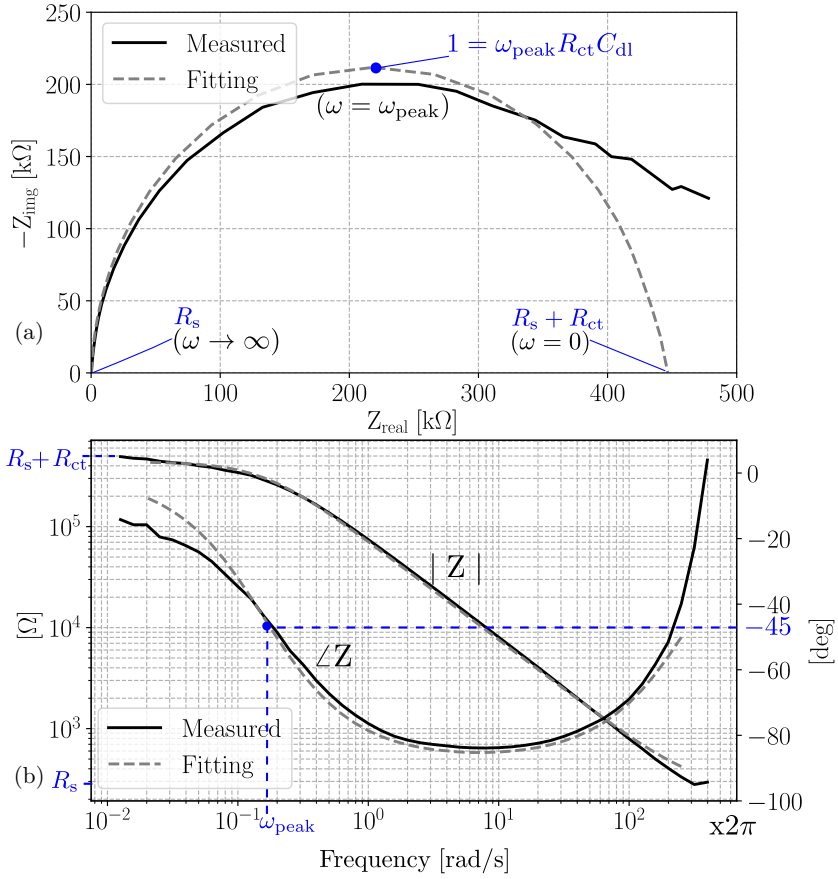

Figure 4.4 | Experimental EIS data in the form of Nyquist (a) and Bode (b) plots of the electrochemical cell of Fig. 4.2(f) using standard desktop instruments.

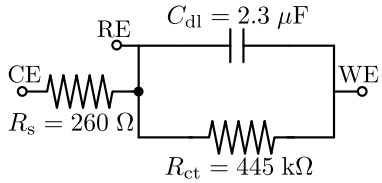

Figure 4.5 | Equivalent Randles cell parameters extracted from the EIS data fitting of Fig. 4.4.

In the Nyquist plot of Fig. 4.4(a), each point represents the impedance at one frequency. For convenience, the imaginary impedance $\mathrm{Z_{img}}$ is inverted due to the fact that all values are less than zero. The resulting semicircle behaviour is associated to the charge transfer process (redox), because at the electrode surface the transfer of charge R_{ct} takes places in parallel with the charging of the double layer capacitance C_{dl}. The solution resistance R_{s} is found by looking the $\mathrm{Z_{real}}$ value at the x-axis intersection near the origin of the plot, which is equivalent to evaluate (4.1) at $\mathrm{Z}(\infty)$. The $\mathrm{Z_{real}}$ value at the right intersection of the same axis is the sum of the charge transfer resistance R_{ct} and R_{s} or Z(DC). Consequently, the semicircle diameter is equivalent to R_{ct}. The peak of the semicircle occurs when $\omega_{\mathrm{peak}} R_{\mathrm{ct}} C_{\mathrm{dl}} = 1$, so C_{dl} can be calculated knowing R_{ct} and ω_{peak}. This is where the Bode plot of Fig. 4.4(b) comes useful. Since the Bode plot refers the impedance magnitude and phase angle as a function of frequency, the ω_{peak} of the time constant $R_{\mathrm{ct}} C_{\mathrm{dl}}$ can be easily estimated. The same data could also be interpreted in the Bode plot. At low frequency, the total impedance of the circuit equals to the summation of R_{ct} and R_{s}. As frequency increases, the impedance tends towards R_{s} with a magnitude slope of -20 dB/dec and a phase shift of 45°/dec due to the pole $-\omega_{\mathrm{peak}}$. In a single pole, the phase starts to change one decade before the pole and stops to shift one decade after. ω_{peak} can be then easily determined by looking the center frequency at which the phase shift is at 50% of its range (i.e. -45°/dec). The highest frequency region exhibits a LHP zero at $\frac{R_{\mathrm{s}}+C_{\mathrm{dl}}}{R_{\mathrm{s}} R_{\mathrm{ct}}}$ due to the series resistance R_{s}, which brings the phase back to 0 °and equalize the impedance magnitude to R_{s}.

The measurements of Fig. 4.4 were performed under conditions in which the Warburg part of the impedance, associated with the diffusion of redox species to the surface of the electrode, could not be determined with sufficient quality since its effects seems to be evident at very low frequency (<10 mHz). The impedance spectra were fitted using complex non-linear least square method to extract the equivalent Randles circuit. The impedance software employed for the characterization was ZView [142] from Scribner Associates Inc, USA. The equivalent simplified Randles circuit extracted from the data fitting of Fig. 4.4 is shown in Fig. 4.5.

4.3 Chip-on-Flex Assembly

4.3.1 Test Vehicles

In order to validate the flip-chip mounting process prior the actual ROIC assembly, two distinct sets of flexible substrate patterns and test dice with appropriate conductive metal structures were designed for measuring the contact integrity of interconnections. These test vehicles can provide valuable information about the bonding process in terms of repeatability, ease of manipulation, sensitivity to temperature, pressure and time, as well as alignment accuracy between die and substrate.

Fig. 4.6 shows the metal structures of the dice and their respective flexible substrates to be attached to. These substrates provide larger outlying pads which can be easily contacted by standard instruments. The design in Fig. 4.6(a) consists of a padring of 10 pads, each being 200 μm $\times$ 200 μm in size, distributed on a chip area of 1.5 mm $\times$ 1.5 mm (2.25 mm^2), so it is a phantom of the electrochemical $\Delta\Sigma$M chip floorplan of Fig. 3.18(b). The pattern of the die is designed in a manner that it electrically interconnects the flexible substrate. This enables to determine subsequent satisfactory assembly and information about labelled with 1 and 2. On the other hand, the design in Fig. 4.6(b) contains a padring of 12 pads sized at 160 μm $\times$ 160 μm in the same total area of 1.5 mm $\times$ 1.5 mm (2.25 mm^2). The daisy-chain layout of this test die is designed in such a way that compliment the patterns on the flexible substrate, forming contacts in series. When current-driving probes are contacting the pads labelled with In and Out, a current is driven throughout the chain. The measured resistance value is the resulting summation of all resistances in the path of the current. Also, open circuits can be easily detected with this pattern.

The dummy dice of Fig. 4.6 were manufactured on Silicon at the IMB-CNM clean room facilities. In this sense, Fig. 4.7 shows the multiple-step processing sequence during their fabrication. Initially, the surface of the Silicon wafer substrate was prepared with a passivation layer of Silicon oxide SiO_2 before the adhesion of the light-sensitive chemical (photoresist) material to the substrate, as shown in Fig. 4.7(a). A standard photolithography technique was then applied to selectively remove parts of the thin film following Fig. 4.7(b). It employs light to project the desired pattern through a reticle (photomask) and a lens to the photoresist onto the wafer surface. The photoresist that was exposed to the light was then chemically removed (i.e. positive photoresist) and a thin film of Al/0.5%Cu was deposited by evaporation and patterned by lift-off to form the structures of the contact pads and inner connections. After the metal structures were patterned, a passivation layer of SiO_2 was deposited on top by plasma enhanced chemical

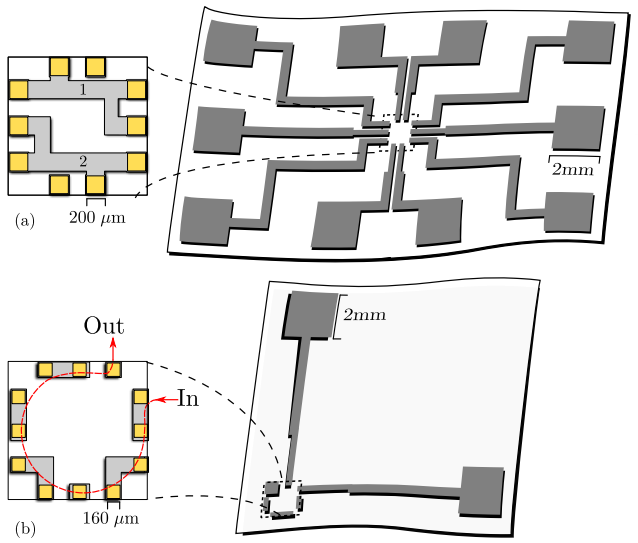

Figure 4.6 Silicon test dice (1.5 mm × 1.5 mm) and inkjet printed patterns on flexible substrates for chip-on-flex characterization. Short-circuit (a) and daisy-chain (b) patterns. Drawings not to scale.

vapour deposition (PECVD) as in Fig. 4.7(e). Steps (a) to (c) were repeated and combined with wet etching to open the contact pads, as seen in Fig. 4.7(f). Finally, in a similar repeated cycle, a thin film of Ni/Au was deposited onto the contact pads, as illustrated in Fig. 4.7(g).

4.3.2 Custom ACA-Based Flip Chip

The wire-bonding free flip chip was carried out using the anisotropic conductive epoxy adhesive 126-37 [143] from Creative Materials Inc, USA. Bonding temperature and time were determined according to the curing guidelines of the product specifications, choosing 60 min @ 160 °C for the best compromise between good adhesion and acceptable thermal damage of the flexible substrate.

In general, application of a controlled bonding force and temperature are essential during ACA bonding to ensure good mechanical and electrical contact between the two metal surfaces. For this purpose, the custom bonder setup of Fig. 4.8 was constructed, which can monitor alignment and apply heat and pressure. The stack includes (from bottom to top) a 4-axis mechanical micro-positioner stage

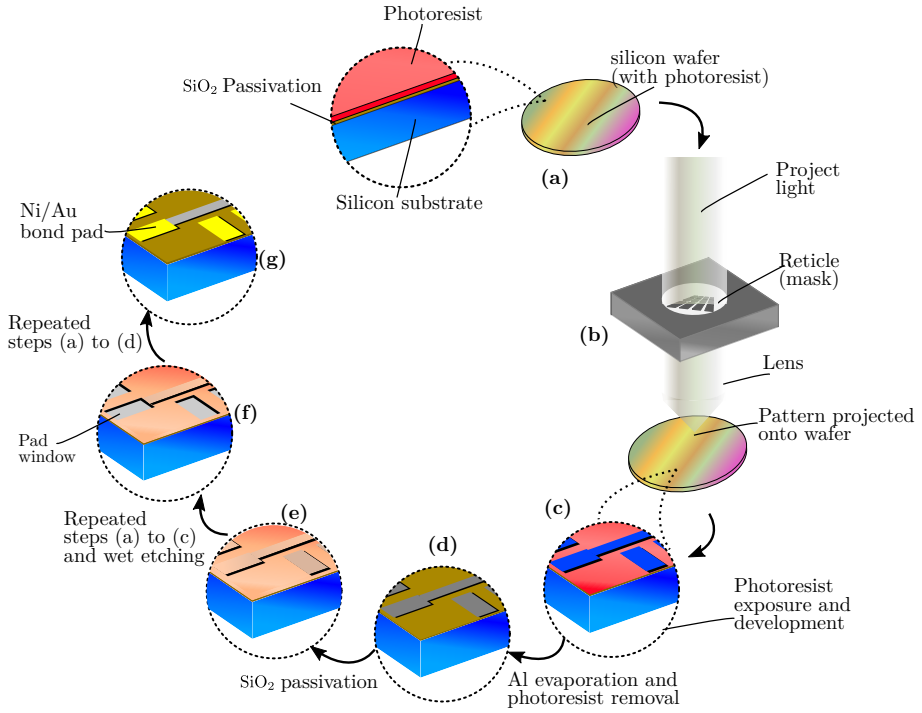

Figure 4.7 | Process flow for the fabrication of the dummy dice of Fig. 4.6 at the IMB-CNM clean room.

with vacuum holding capability for die alignment, the dummy die (upside), an ACA thickness layer of about 100 μm, 125-μm thick PEN flexible substrate, 5-mm thick Al frame with a 4-mm thick borosilicate glass window, a heater platform that can achieve temperatures up to 160 °C, and an optical alignment system based on a digital microscope.

The operation principle of the experimental set-up is as follows: the microscope is set up to view the translucent flexible substrate through the borosilicate glass for a precise die alignment on the substrate as the 4-axis stage is elevated (y-axis) and the chip (upside), with the ACA layer applied, is pushed against the substrate. The pressure is then controlled by checking the contact resistance in real-time, i.e. pressure is progressively increased until contact resistance is formed between the corresponding pads. Once the die is electrically connected to the substrate, pressure is kept constant and heat is applied, through the custom heater, for curing the ACA material. More than twenty test chips have been bonded onto

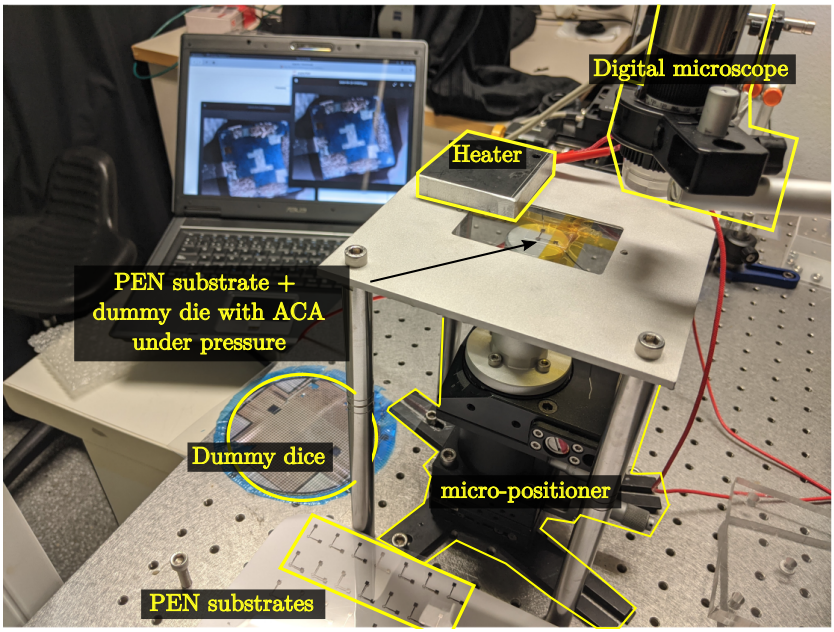

Figure 4.8 | Experimental custom setup for the ACA flip-chip bonding.

the PEN flexible substrates by using this custom flip-chip bonding setup described above. Different bonding temperatures and time combinations have been tested. With 160 °C for 1 hour, curing appearance still looked sticky. A proper yield (4/5) was found after applying 160 °C for 3 hours and letting it cool for 8 hours. Currently we are in contact with Creative Materials in order to further optimize the assembly. Finally, Fig. 4.9(a) shows the test vehicle of Fig. 4.6(a) once assembled, while Fig. 4.9(b) illustrates the bottom view through the transparent PEN flexible substrate, showing the Ag inkjet pads and the dummy Silicon IC. In Fig. 4.9(c) it can be observed how spherical conductive particles about 10 μm in size are randomly dispersed through the die. Around 100 particles are trapped between the mating interconnect pads to create the z-axis electrical connection.

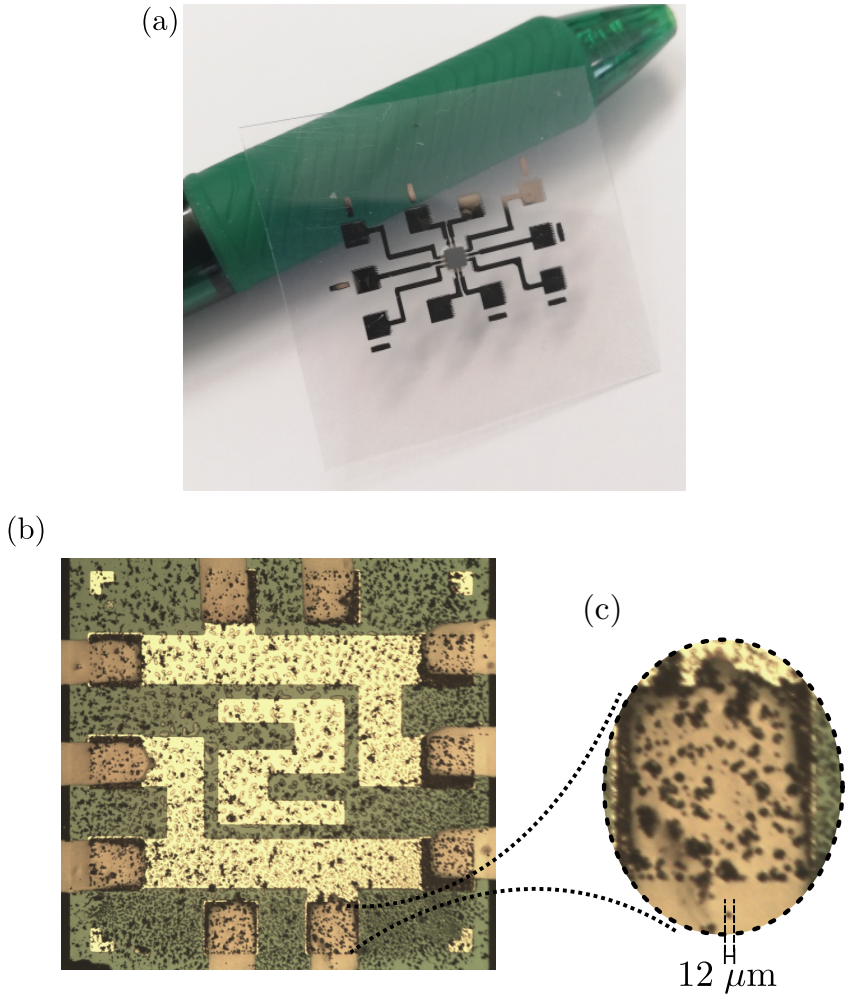

Figure 4.9 ACA assembled test vehicle of Fig. 4.6 (a), bottom view through transparent PEN substrate showing the Ag inkjet pads and the dummy Silicon IC (b), and zoom-in to reveal ACA particles size (c).

Experimental Results | 5

The aim of this chapter is to validate the manufactured CMOS ROICs previously described in Chapter 3 not only at electrical level but also electrochemically with state-of-the-art sensors. In this sense, the novel potentiostatic-amperometric CMOS ΔΣM frontend circuits are first electrically tested by emulating the equivalent electrochemical cell impedance with discrete components. The experimental measurements obtained from these tests are then compared and validated with reference to post-layout simulation results. Once the test chips are electrically verified, they are subjected to a full electrochemical characterization by employing distinct sensing modalities. For this purpose, the standard ferri/ferrocyanide redox couple is used for comparing the voltammetry and amperometry behaviours respect to commercial benchtop instruments. The measured performance of the proposed ROICs is finally contrasted with existing state-of-the-art CMOS circuit frontends for electrochemical sensors.

The chapter ends up by presenting and verifying the proposed disposable smart electrochemical sensor, which exploits CMOS ROICs together with the benefits of the inkjet printing technology.

5.1 A 1.2-V 65-nm CMOS ΔΣM Frontend for Electrochemical Sensors

Fig. 5.1 shows the test chip of the electrochemical ΔΣM frontend proposed in Fig. 3.6 once integrated in TSMC 1.2-V 65-nm 1-poly 9-metal CMOS technology. The 1-mm^2 chip die contains 23 I/O pads distributed according to the list of Table 5.1 and it is wired-bonded to standard 24-pin dual in-line (DIL) ceramic package.

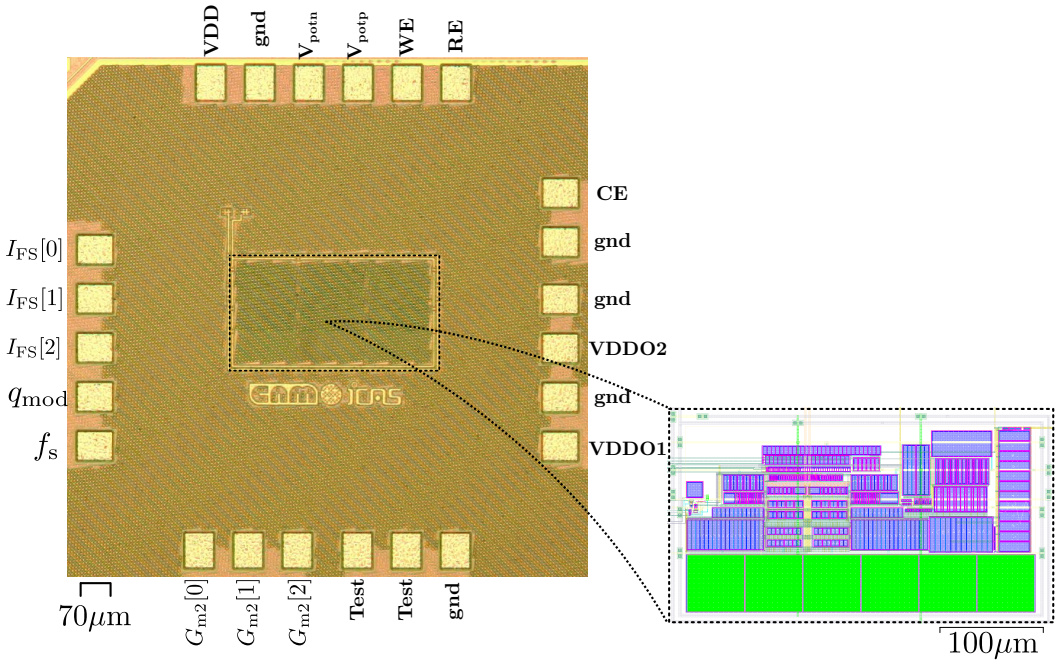

Figure 5.1 Test chip photo and core floorplan detail of the electrochemical ΔΣM of Fig. 3.6 in TSMC 1.2-V 65-nm 9-metal CMOS technology. Chip size is 1 mm × 1 mm (1 mm^2) and core bonding box is 480 μm × 370 μm (0.18 mm^2).

PAD name	Type	Description
I_{FS} [0 : 3]	Digital In	Current full scale programmablity
G_{m2} [0 : 3]	Digital In	Electronic time constant τ_2 programmablity
f_{s}	Digital In	Sampling clock
q_{mod}	Digital Out	Electrochemical ΔΣM output
$V_{\text{potp,n}}$	Analog In	Potentiostatic references
WE, CE, RE	Analog In	Electrochemical sensor
VDD	Power Cell	1.2-V Core supply
VDDO1	Power Cell	1.2-V I/O digital drivers supply
VDDO2	Power Cell	2.5-V I/O ring power supply

Table 5.1 Pad list of the 1.2-V 65-nm CMOS ΔΣM test chip of Fig. 5.1.

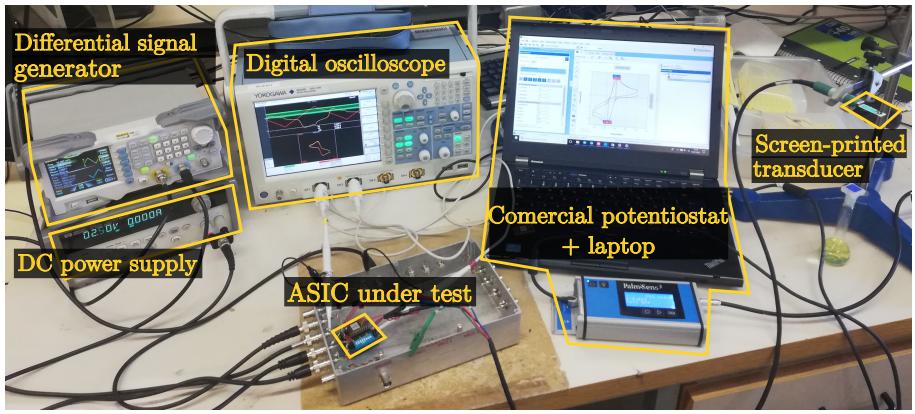

Figure 5.2 | Laboratory setup for the electrical and electrochemical tests of the 1.2-V 65-nm CMOS ΔΣM of Fig. 5.1.

Fig. 5.2 shows the custom setup for the characterization of the ASIC prototype of Fig. 5.1. In this arrangement, power is supplied through the E3641A source from Hewlett Packard, USA, while the potentiostatic references $V_{\mathrm{potp,n}}$ are controlled through the DG1062 differential signal generator from Rigol, China. The single-bit ΔΣM output q_{mod} is captured through the DL9140L digital oscilloscope from Yokogawa, Japan. When coupled also with the differential signal generator, it allows the cyclic voltammetries to be plotted directly. The low-cost screen-printed disposable sensor employed for the electrochemical characterization can be also coupled with the PalmSens[3] handheld potentiostat from PalmSens VC, The Netherlands, for a direct comparison between the proposed ΔΣM frontend and the commercial system under the same conditions. The handheld potentiostat is connected to a laptop equipped with PSTrace 4 software from the same manufacturer.

5.1.1 Low-Cost Screen-Printed Electrochemical Sensor

The manufacturing steps to build the screen-printed electrochemical sensor of Fig. 5.1 are illustrated in Fig. 5.3. The low-cost sensor was designed for a WE area of 0.44 mm^2 using Vectorworks software from Vectorworks Inc., USA, and printed on PET substrates Autostat CT4 from MacDermid Autotype Ltd., UK, using a 90 thread cm^{-1} yellow Nylon mesh screen from Paymser SL, Spain. Silver tracks, contact pads, and pseudo-reference electrodes were printed first with conductive polymer Loctite EDAG 725S from Henkel AG., Germany, follow by graphite for working and auxiliary electrodes with C2030519P4 ink from Gwent Electronic Materials Ltd., UK. Last, the UV curable dielectric paste Loctite EDAG PF-455B was employed to protect silver tracks and define the electrode geometries [144].

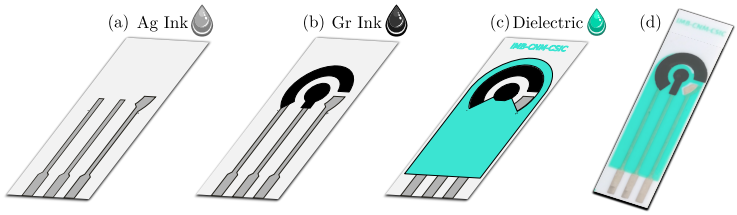

Figure 5.3 Manufacturing steps (a-c) and photo (d) of the screen-printed sensor employed in the experimental setup of Fig. 5.2. The WE area is 0.44 mm^2.

The resulting screen-printed sensor was characterized before the ASIC test itself for the purpose of extracting the equivalent RC impedance model of the electrochemical cell. This characterization was carried out through the Autolab PGSTAT302N potentiostat coupled to the EcoChemie FRA32M impedance analysis module. In this sense, the 0.44 mm^2 screen-printed sensor, immersed in an equimolar mixture of ferri/ferrocyanide (0.1 M) in 0.1 M KCl, showed $R_{\rm ct} = 14.0(\pm 1.3)$ kΩ and $C_{\rm dl} = 32(\pm 3)$ μF (10 samples) at open circuit potential, resulting in an electrochemical time constant $\tau_1 = 0.445$ s.

5.1.2 Electrical Tests

Based on the typical impedance values of the screen-printed sensors described above, the parameters of Table 5.2 were chosen during the design of the 1.2-V 65-nm CMOS $\Delta\Sigma$M frontend of Fig. 5.1. The stability constrains in (2.7) impose $f_s > 300$ Hz, so $f_s = 512$ Hz is finally selected, which is equivalent to OSR = 256 for 1-Hz bandwidth. According to these parameters, behavioral simulations of the proposed $\Delta\Sigma$M return satisfactory $V_{\rm rw}$ ripple amplitudes of < 1.6 mV at $\pm$100-nA full scale and $\text{SQNR}_{\rm max}$ values exceeding 110 dB.

Parameter	Typical	Units
τ_1	0.445	s
$G_{\rm m1}$	9	μS
$G_{\rm m2}$	20	nS
C_2	66	pF
τ_2	3.3	ms
f_s	512	Hz

Table 5.2 Design parameters of the 1.2-V 65-nm electrochemical $\Delta\Sigma$M of Fig. 5.1 for the screen-printed sensors of Fig. 5.3.

Before the validation of the proposed electrochemical ΔΣM with the screen-printed sensors, the chip of Fig. 5.1 has been exhaustively tested for quantitative SNDR and dynamic range measurements under ideal electrical harmonic stimulus. For this purpose, the electrochemical current has been generated through the equivalent RC impedance model of the electrochemical sensor of Fig. 5.3 together with an equivalent Thévenin voltage source using the 100-dB distortion-free function generator DS360 from Stanford Research Systems, USA.

Fig 5.4 and 5.5 show some examples of the experimental results obtained from these electrical tests. In the first case, the measured output PSD returns the expected second-order quantization noise shaping and good matching with the post-layout simulations (except for the 50-Hz grid coupling). From the same figure, it is clear that the proposed ΔΣM exhibits very low distortion, being the SNDR up to 1-Hz bandwidth limited in practice by noise. Indeed, the main in-band contributions do not come from quantization errors or device thermal noise but from the DAC low-frequency 1/f flicker noise. The experimental dynamic range extension concept is demonstrated in Fig 5.5, where the measured SNDR curves at the minimum and maximum programmable DAC full-scale levels are plotted. With sustained $\mathrm{SNDR}_{\mathrm{max}}$ values around 80 dB for each full scale, the combined electrochemical current dynamic range is extended up to 105 dB.

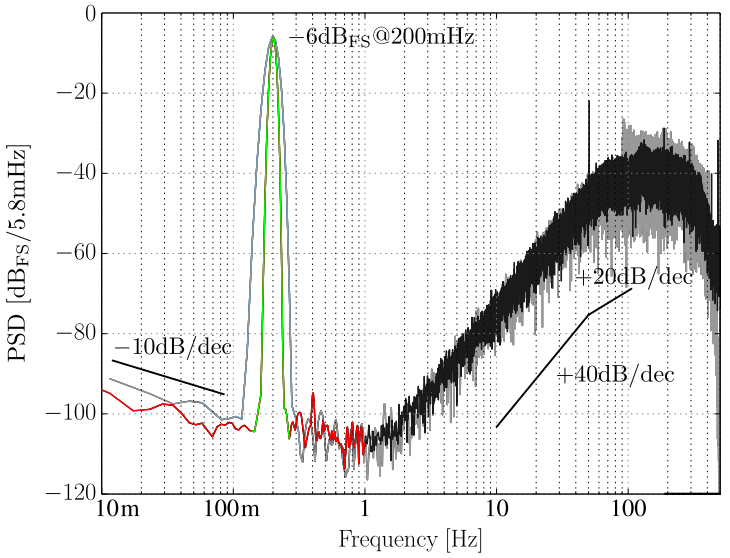

Figure 5.4 Comparison between experimental (colored) and simulated (greyed) output PSD of the electrochemical ΔΣM of Fig. 5.1 under electrical stimulus at half full-scale input for $I_{\mathrm{FS}} = \pm 1.5\ \mu\mathrm{A}$ and $V_{\mathrm{potp,n}} = 0.6$ V.

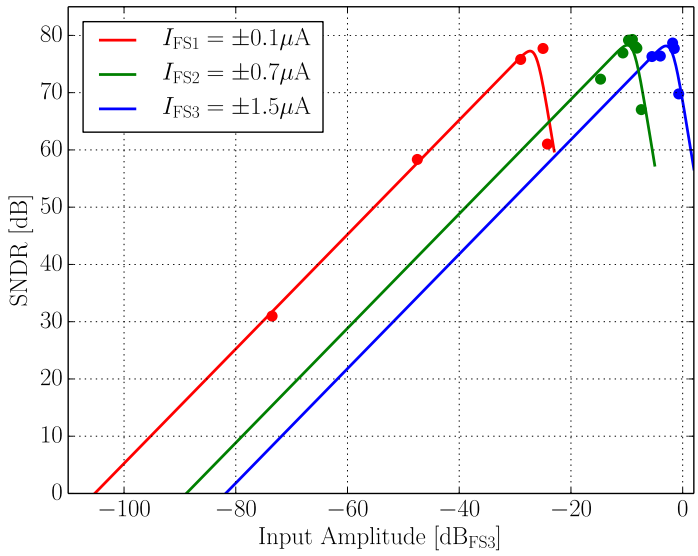

Figure 5.5 Experimental output SNDR of the electrochemical ΔΣM of Fig. 5.1 at 200-mHz input and 1-Hz BW for three programmable full-scale values with $V_{\text{potn,p}} = 0.6$ V.

5.1.3 Electrochemical Tests

Once characterized at electrical level, the CMOS ΔΣM of Fig. 5.1 is tested in 1 mM equimolar mixture of ferri/ferrocyanide solution to demonstrate its potentiostatic operation. In this experiment, 0.1 M KCl and 1 mM ferri/ferrocyanide in 0.1 M KCl solutions were used. Fig. 5.6(a) shows the background current measured in the supporting electrolyte solution (0.1 M KCl). This CV demonstrates that the range of the potentiostatic controls can span up to 1.8 V, showing in this case the capactive (background) current associated to the electrode-solution system. On the other hand, Fig. 5.6(b) corresponds to the CV of a 1 mM equimolar mixture of ferri/ferrocyanide solution. In this typical one-electron redox reaction, the ferricyanide ion $[Fe(CN)_6]^{3-}$ is the oxidized form and the ferrocyanide ion $[Fe(CN)_6]^{4-}$ is the reduced form, following the redox reaction:

$$Fe(CN)_6^{3-} + e^- \rightleftharpoons Fe(CN)_6^{4-}. \tag{5.1}$$

As the potential $V_{\text{potn}} - V_{\text{potp}}$ (V_{wr}) is scanned positively (forward scan), the oxidation of ferrocyanide ion ($Fe(CN)_6$ $^{4-}$) starts at 0.1 V, and an oxidation peak is observed at around 0.28 V. From that point, the potential sweep direction is reversed (backward scan) in the negative direction, and the current due to the ferricyanide ion ($Fe(CN)_6$ $^{3-}$) flows out, reaching the reduction peak at around 0.05 V. The data shows very good agreement between the ASIC and the commercial potentiostat equipment. The trace from the electrochemical ΔΣM output has been plotted after applying a 2.5-Hz third-order Butterworth low-pass digital filter as decimator. It is worth noting that thanks to the differential architecture of Fig. 3.3, the 1.8-V_{pp} potentiostatic control range can be achieved under single 1.2-V CMOS supply.

Comparative amperometry stair experiments were performed for the same test analyte and buffer solution as shown in Fig. 5.7. The sensor was immersed initially in 25 mL of buffer solution. Aliquots from 1.2 mM ferrocyanide solution were sequentially added to the initial buffer under soft stirring. The spiking sequence executed in six steps through a micropipette was: $vseq$ =(50 μL, 75 μL, 100 μL, 100 μL, 100 μL), to approximate a uniform distribution of points in the calibration curve. At each step k, the concetration of the analyte [A], in the test solution is calculated through the following simple formula:

$$[\text{A}](k) = \frac{v_{\text{test}}(k-1)[\text{A}](k-1) + v_{\text{seq}}(k)1.2\text{ mL}}{v_{\text{test}}(k)}, \tag{5.2}$$

where

$$v_{\text{test}}(k) = v_{\text{test}}(k-1) + v_{\text{seq}}(k). \tag{5.3}$$

No significant differences in the calibration curve parameters (i.e. slope and offset) nor linearity are observed between the ASIC prototype and the reference commercial handheld potentiostat.

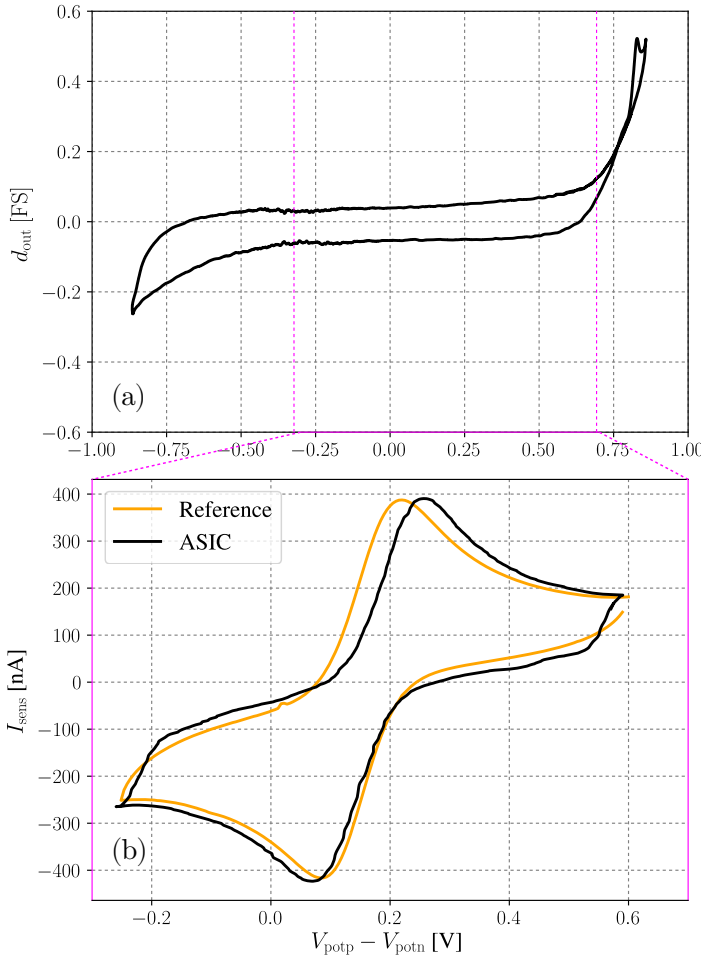

Figure 5.6 Experimental CVs versus Ag pseudo-RE of the electrochemical ΔΣM of Fig. 5.1 at 50 mV/s and ±0.7-μA full scale for 0.1-M KCl buffer (a) and 1-mM equimolar mixture of $[Fe(CN)_6]^{4-/3-}$ ions compared to the commercial PalmSens[3] potentiostat equipment of Fig. 5.2.

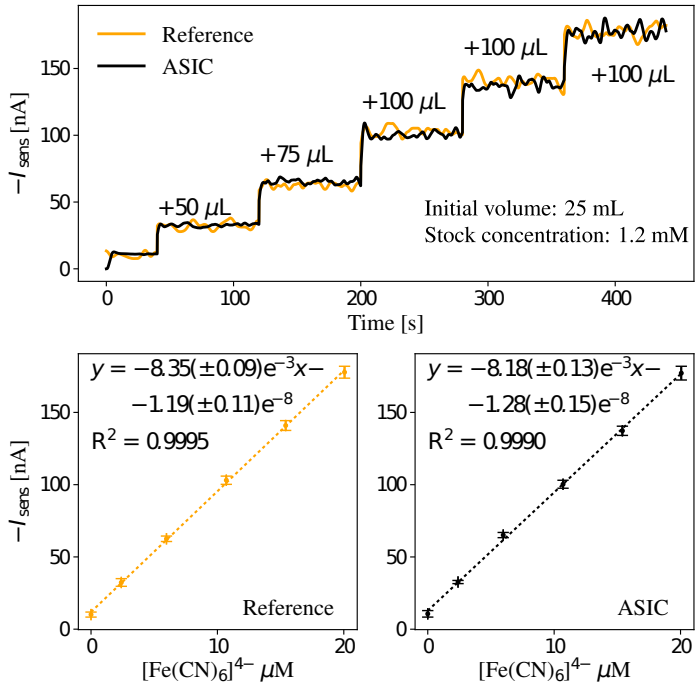

Figure 5.7 Comparative experimental amperometry measurement and calibration curves for a spiking sequence of $[Fe(CN)_6]^{4-}$ ion between the ASIC of Fig. 5.1 and the commercial PalmSens[3] potentiostat of Fig. 5.2.

5.2 A 1.8-V 0.18-μm CMOS Smart System for Electrochemical Sensors

Fig. 5.8 shows the test chip photo of the smart-sensor frontend proposed in Fig. 3.18 integrated in XFAB 1.8-V 0.18-μm 1-poly 6-metal MiM CMOS technology and customized for low-cost IC assembly. Some fabricated dice were wired-bonded to a 16-pin DIL ceramic package for electrical/electrochemical characterization purposes only. The complete chip exhibits a total area of 1.5 mm^2 $\times$ 1.5 mm^2 (2.25 mm^2) and it contains 10 I/O pads, distributed according to the list of Table 5.3.

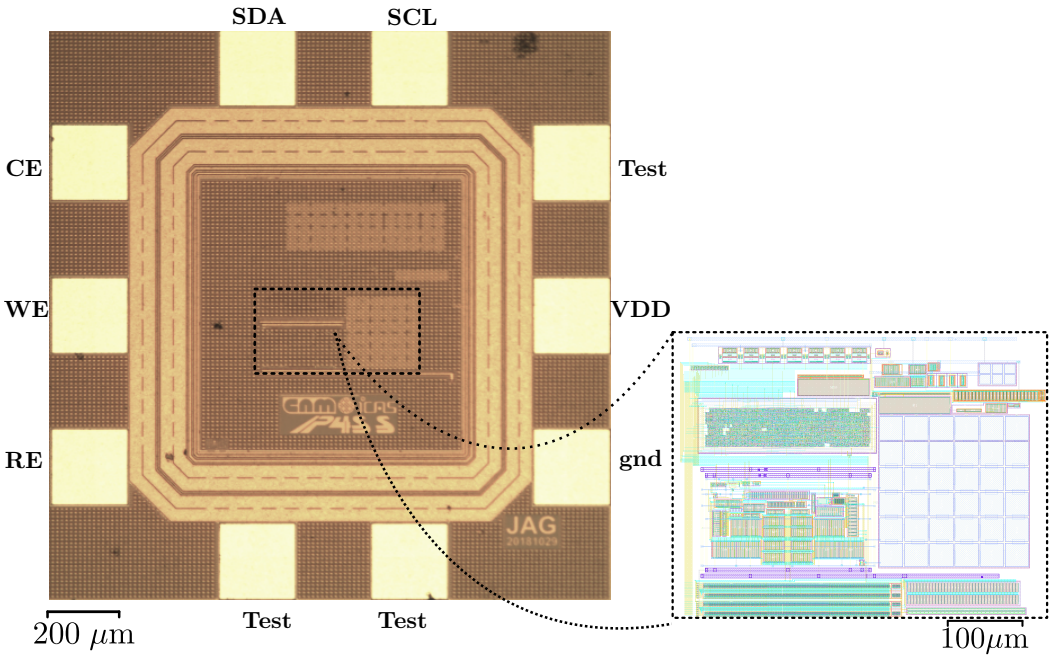

Figure 5.8 Test chip photo and core floorplan detail of the smart-sensor frontend of Fig. 3.18 in XFAB 1.8-V 0.18-μm 6-metal CMOS technology. Chip size is 1.5 mm^2 $\times$ 1.5 mm^2(2.25 mm^2) and core bounding box is 480 μm $\times$ 370 μm (0.18 mm^2).

PAD name	Type	Description
SCL	Digital In/Out	I^2C serial clock line
SDA	Digital In/Out	I^2C serial data line
WE, CE, RE	Analog In	Electrochemical sensor
VDD	Power Cell	3.3-V I/O ring and core regulator supply
Test	-	Testing purposes

Table 5.3 Pad list of the 1.8-V 0.18-μm CMOS smart system test chip of Fig. 5.8.

5.2.1 Electrical Tests

The performance of the smart frontend of Fig. 5.8 is first electrically evaluated under the design parameters of Table 5.2. Similar to the experimental setup of Fig. 5.2, the electrochemical current has been stimulated through the equivalent impedance RC model of the electrochemical sensor of Fig. 5.3 together with an equivalent Thévenin voltage source using the same 100-dB distortion-free function generator DS360.

Each of the consequent experimental averaged power spectral density (PSDs) shown in Fig. 5.9 have been obtained after acquiring data during a 7-hour window and 10-times frequency averaging for the purpose of discerning the contributions at low frequency. Results in Fig. 5.9(a) and (b) demonstrate the effectiveness of the proposed G_{m1} switching technique (2.3) for the cancellation of the CMOS flicker noise. With the cancellation mechanism activated, Fig. 5.9(b) shows no evidence of the 1/f noise even within the sub-mHz range. A less effective cancellation is shown in Fig. 5.9(c) and (d) for a sinusoidal input closed to full scale (-6 dB_{FS} at 200-mHz). The -84 dB_{FS} second harmonic located at 400-mHz is originated when input amplitudes are approaching the full-scale limit and the G_{m1} switching technique is activated. SNR and SNDR peak values were compared, returning a difference of < 1 dB. Therefore, the effect of this odd harmonic can be actually disregarded.

Fig. 5.10 plots the experimental SNDR curves at the minimum and maximum programmable DAC full-scale levels with and without the proposed G_{m1} witching technique. It is worth to highlight that the 1/f noise cancellation mechanism improves the SNDR performance in about 10 dB for the lower range of input amplitudes. Interestingly, the $SNDR_{max}$ does not show the same behaviour due to the fact that noise cancellation degrades with increasing amplitude because of the resulting output code asymmetry, already illustrated in Fig. 3.23. Anyway, the proposed flicker noise cancellation proposal extends the overall dynamic range and the LOD figure, as validated in next section.

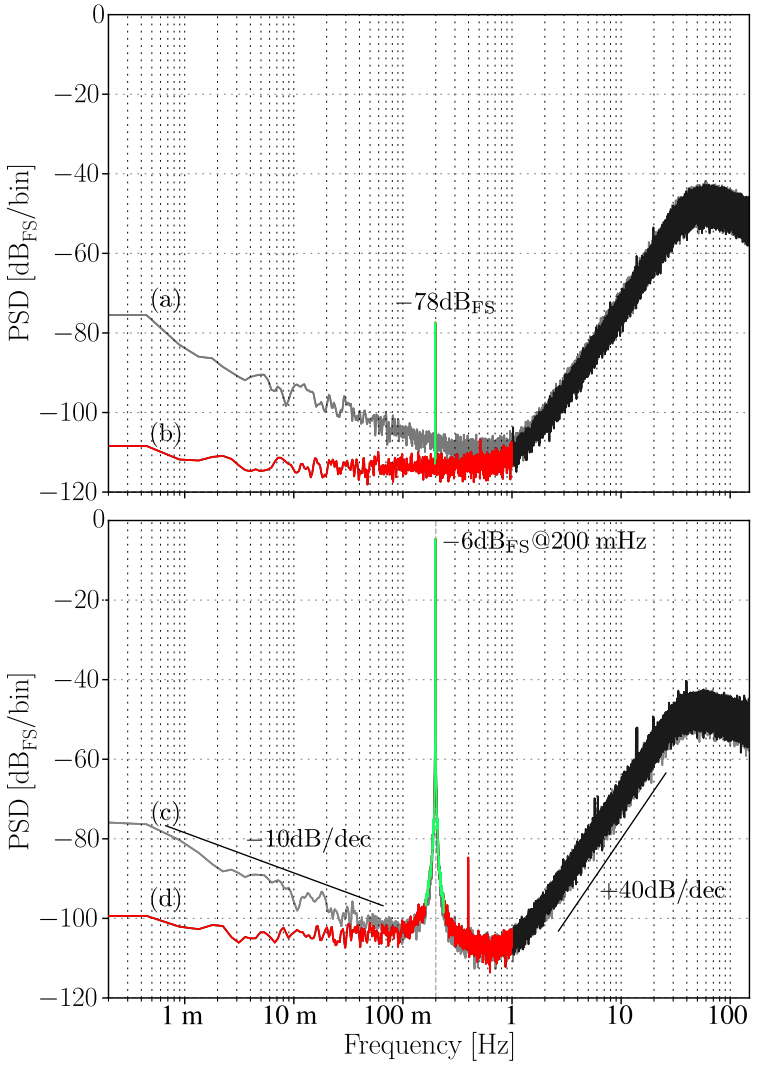

Figure 5.9 Experimental output PSD of the smart sensor frontend of Fig. 5.8 without (a) and with (b) the flicker noise cancellation mechanism for weak electrical stimulus, and response at half full-scale input (c). Configuration is $V_{\mathrm{potn,p}} = 0.8$ V and ± 1.5-μA full scale. Obtained from a 7-hour acquisition window after 10-times PSD bin averaging.

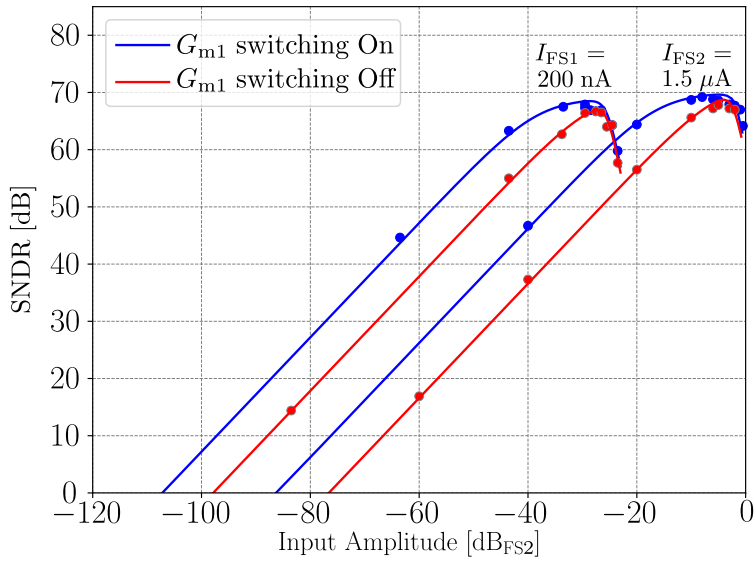

Figure 5.10 Experimental output SNDR curves of the smart frontend of Fig. 5.8 with and without the G_{m1} switching technique for the minimum and maximum programmable full-scale values and $V_{potp} = V_{potn} = 0.8$ V. Input stimulus at 200 mHz and integrated in-band noise from 10 mHz to 1 Hz.

5.2.2 Electrochemical Tests

The electrochemical characterization of the smart frontend of Fig. 5.8 is tested employing the screen-printed sensor of Fig. 5.3 in an equimolar mixture of ferri/ ferrocyanide in 0.1 M KCl as analyte.

The typical chronoamperometry response as a result of different ferri/ferrocyanide concentrations (1 μM, 4 μM, 8 μM, 10 μM, 20 μM and 40 μM) is shown in Fig. 5.11(a). Initially, the WE versus Ag pseudo-RE (i.e. $-V_{rw}$) is held at a potential of 0.02 V, some mV after the reduction peak potential observed in the CV of Fig. 5.6, assuring the reduction of ferricyanide ions. The higher electrochemical currents resulting from the oxidation of ferrocyanide ions in the surface area of the WE were acquired stepping the potential to 0.3 V which was observed beginning at $t = 0$ in Fig. 5.11. This figure clearly shows that the electrochemical current recorded increases with increasing analyte concentration. The exponential decay Faradaic current was shown in the curve due to the exhaustion of the concentration of ferricyanide around the surface of the WE, as described in the Cottrell equation:

$$I_{\text{sens}}(t) = \frac{nFAC_o\sqrt{D}}{\sqrt{\pi t}}, \tag{5.4}$$

where n is the number of electrons to reduce one molecule, F is the Faraday's constant (i.e. 96152 C/mol), A is the area of the electrode, D is the diffusion coefficient, C_o is the initial concentration and t is time. After about 70 s, the electrochemical current reaches the steady stage as the mass transport limit is achieved to approximate a uniform distribution of points in the calibration curves of Fig. 5.11(b). No significant differences in the calibration parameters (i.e. slope and offset) nor linearity are observed between the ASIC of Fig. 5.8 and the reference commercial handheld potentiostat.

The benefits of employing the proposed CMOS flicker noise cancellation technique are demonstrated in Fig. 5.12 for both time domain and frequency domain. The time domain representation of Fig. 5.12(a) is plotted after applying a 3-mHz second-order Butterworth low-pass digital filter as decimator. It can be noticed that without activating the G_{m1} switching mechanism, the flicker noise causes a slowly changing function as time goes on. Flicker noise can accumulate to very large numbers over time. Therefore, if this continues to zero frequency, the integrated fluctuation would be infinite or arbitrarily large, exceeding the full scale values and so bringing the $\Delta\Sigma$M towards saturation. The PSD of Fig. 5.12(b) illustrates the frequency domain representation of the $\Delta\Sigma$M output signal with and without the noise cancellation mechanism. The resulting electrochemicall PSD returns the expected second-order quantization noise shaping constituted by the combination of both the sensor dynamics and the electronic integrator.

The experimental time domain measurement of the blank (0.1 M KCl) shown in Fig. 5.12(a) is replicated 3 times for the purpose of observing their statistical representation and quantifying the equivalent LOD. The LOD figure indicates the smallest signal that can be distinguished from the absence of the analyte with a certain stated confidence level as described in (1.3). Indeed, Fig. 5.13 shows the probability distribution function (PDF) of the electrochemical current steady stage values extracted from the experimental time domain measurement, like in Fig. 5.12(a). Both profiles, with and without activating the G_{m1} switching mechanism, present Gaussian distributions. Note that the RMS value of the representations are the standard deviation σ of the electrochemical current distribution. Conclusively, the G_{m1} switching mechanism for the cancellation of the flicker noise clearly improves the LOD for applications requiring continuous measurement over extended periods, like real-time sweat monitoring in athletes. Results prove that the LOD can be improved about 4 times when the cancellation technique is activated.

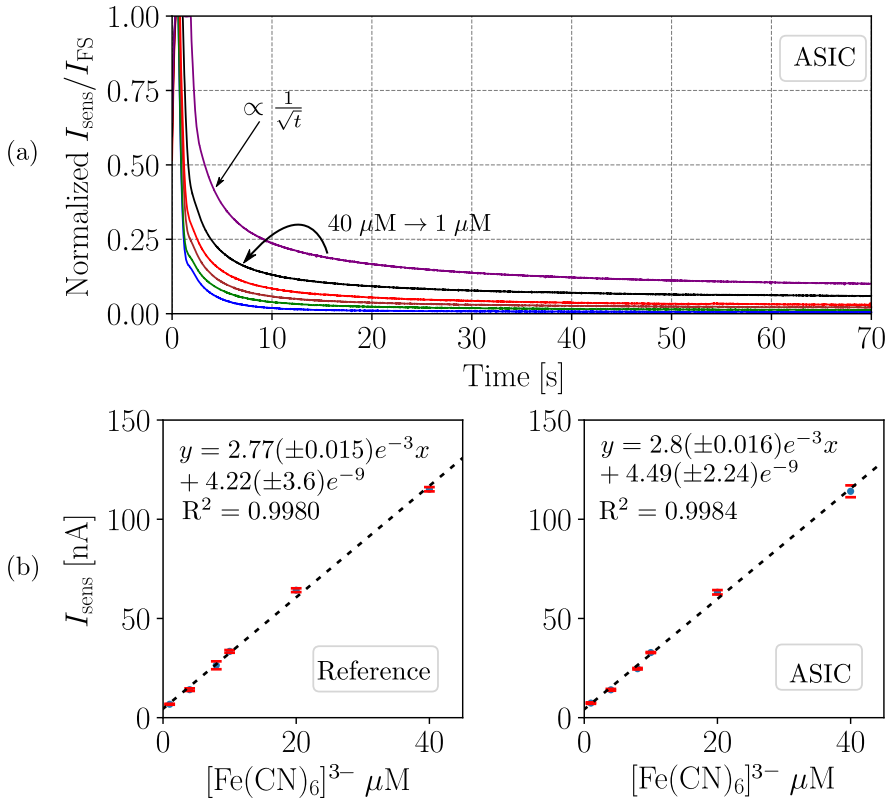

Figure 5.11 Experimental chronoamperometry curves of the smart sensor frontend of Fig. 5.8 for different ferri/ferrocyanide concentrations, from 1 μM to 40 μM in 0.1 M KCl (a) and linear fitting correlation current-concentration curves between the steady electrochemical currents acquired at 70 s (b) compared to the commercial PalmSens[3] potentiostat equipment of Fig. 5.2.

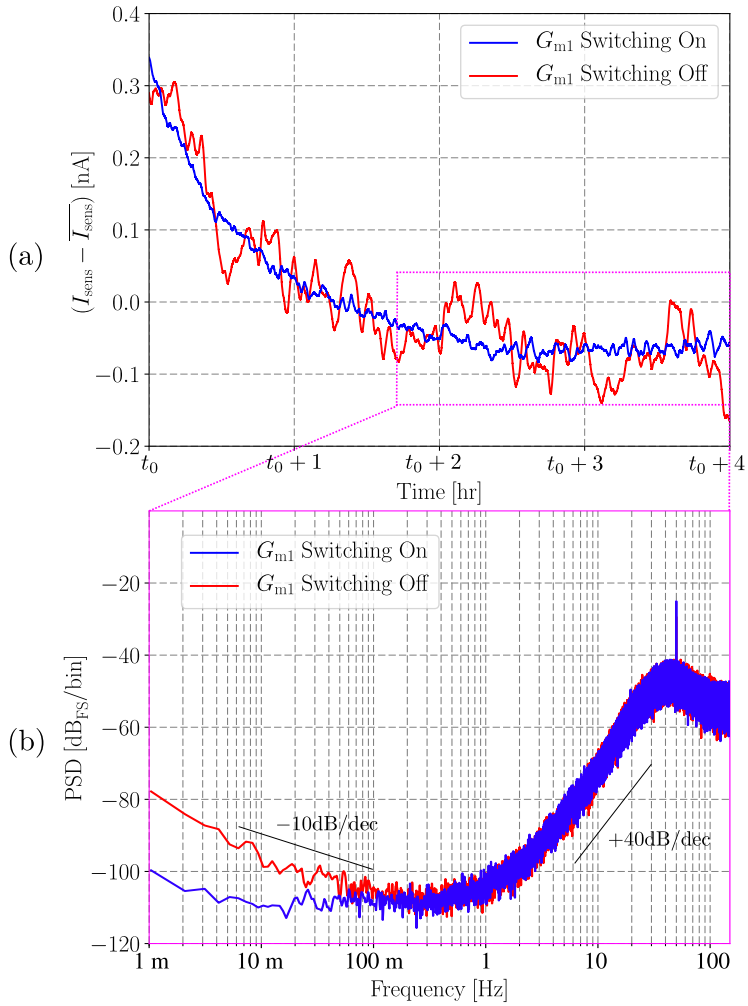

Figure 5.12 Experimental time-domain (a) and frequency-domain PSD (b) responses of the smart frontend of Fig. 5.8 with and without the flicker noise cancellation mechanism in 0.1 M KCl buffer. Configuration is $V_{\text{potn}} = 0.8$ V and $V_{\text{potp}} = 0.5$ V, and ± 1.5-μA full scale.

Finally, Table 5.4 compares the performance of the presented ROICs to the state-of-the-art CMOS circuit frontends for electrochemical sensors available in literature. The proposed solutions are contrasted to reference works showing similar metrics such as bandwidth and readout architectures. The proposed designs exhibit a remarkable low-power operation while maintaining very competitive SNDR_{max} and dynamic range (DR) values. Whilst the power consumption for the demonstrated ROIC of Fig. 5.8 is higher than other works, the chip operates with an internal linear regulator capable of supplying both the potentiostat and the on-chip I^2C digital interface. Furthermore, and thanks to the G_{m1} switching technique for the cancellation of the flicker noise, the obtained LOD is comparable to the lowest LOD state-of-the-art designs. In addition, the differential control of the potentiostatic voltage of the presented designs can exploit the potentisotatic range beyond the supply voltage, specially for the chip of Fig. 5.8 that faces a down-scaled supply voltage of 1.2 V.

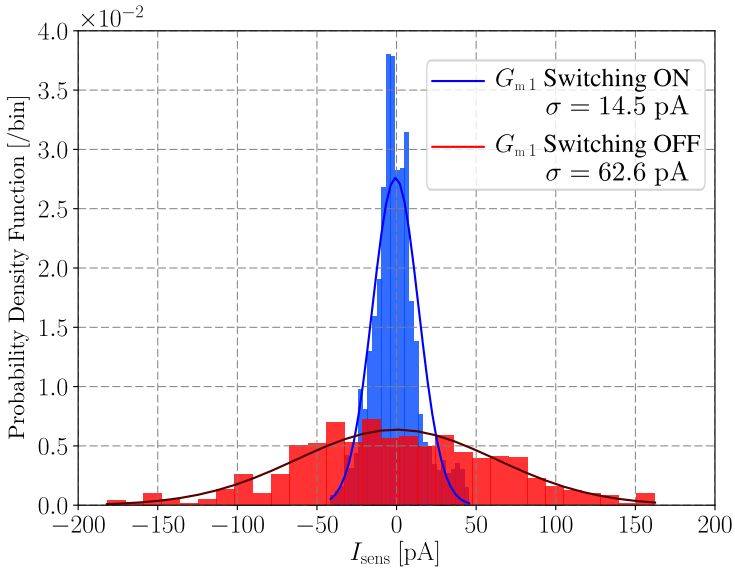

Figure 5.13 Observed PDF with and without activating the G_{m1} switching mechanism for the smart sensor frontend of Fig. 5.8 in 0.1 M KCl buffer.

	This work								
	Sec. **5.1**	Sec. **5.2**	**[12]**	**[11]**	**[71]**	**[145]**	**[146]**	**[147]**	
ADC architecture	SI CT ΔΣM	SI CT ΔΣM	SI CT ΔΣM	SC CT ΔΣM	Async ΔΣM	Dual Slope	SC CT ΔΣM	CD ΔΣM	
AFE architecture	Sensor-in-the-loop	Sensor-in-the-loop	Sensor-in-the-loop	Sensor-in-the-loop	Capacitive TIA	Capacitive TIA	Current Mirror	Capacitive TIA	
On-Chip digital interface	No	I^2C	Yes	No	No	SPI	No	LVDS	
Technology	65	180	2500	600	180	350	130	250	nm
Supply voltage	1.2	1.8	5	5	1.8	1.2	3/1.5	5	V
Pot. range	1.8	3	3	4	<1.8	<1.2		<5	V_{pp}
Full scale	±0.1 to ±1.5	±0.1 to ±1.5	+2 to +32	±0.1	±10	±0.1 to ±1	±0.01 to ±1000	±0.0125	μA
Bandwidth	0.01-1	0.01-1	2	10	1.8	125	10000	0.1-20	Hz
$SNDR_{max}$ fullscale	78 @0.1μA 80 @0.7μA 79 @1.5μA	68 @0.1μA 69 @0.7μA 69 @1.5μA	71	68	160	73			
DR	105	110	71	68	93		147	93	dB
LOD		43.5 (14.5_{rms})			70	10_{rms}	91.7_{rms}	0.28_{rms}	pA
Power	15 @0.1μA 19 @0.7μA 25 @1.5μA	*280	25	1040	295	12	39.3/14.1	† 0.25	μW
Area	0.07	0.18	6.4	0.03	0.2	2.56			mm^2

Table 5.4 Comparison of CMOS potentiostatic frontends for electrochemical sensors.
*the full integrated system (e.g. supply regulator).
† power per channel and without accounting 1 mW from the resistive heater.

5.3 Disposable Smart Electrochemical Sensor

The disposable smart electrochemical sensor prototype is shown in Fig. 5.14(a). The single flexible PEN substrate solution follows the development procedure described previous in Chapter 4. Firstly, the all-inkjet three-electrode electrochemical sensor is directly printed onto the low-cost PEN substrate together with all required printed contacts and interconnections. Finally, the smart frontend CMOS ROIC of Fig. 5.8 is attached, as a bare die, to the inkjet printed silver pads by utilizing the custom ACA flip-chip bonding setup of Fig. 4.8.

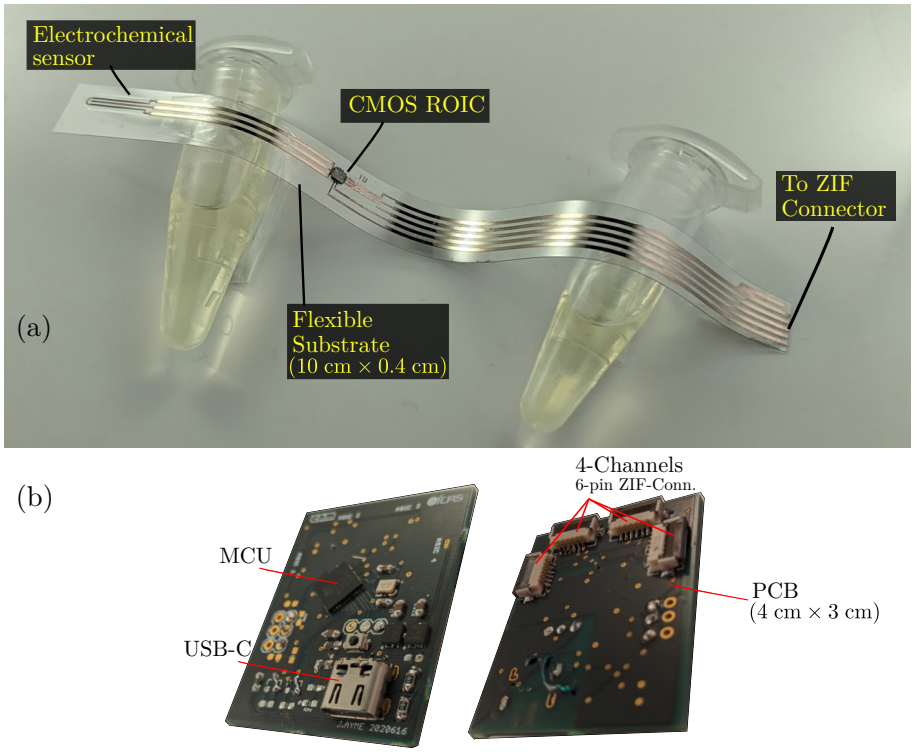

Figure 5.14 | Disposable smart electrochemical sensor prototype (a) and smartphone dongle for up to 4 channels (b).

The compact PCB shown in Fig. 5.14(b) is employed as a nondisposable dongle for smartphones. It is constituted of few discrete electronic components and allows to establish communication, through ZIF connectors, up to 4 disposable devices.

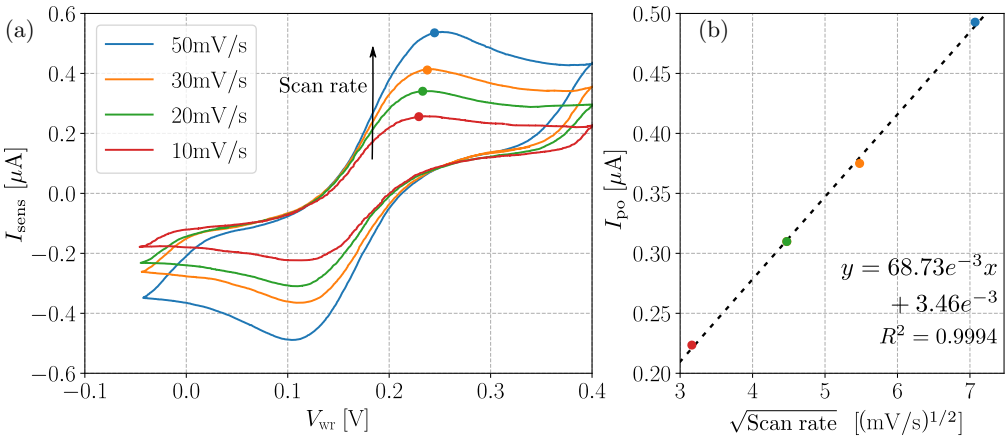

Figure 5.15 Experimental CVs versus Ag pseudo-RE of the electrochemical sensor of Fig. 5.14(a) at different scan rates for 2 mM $Fe(CN)_6]^{3-/4-}$ in 0.1-mM KCl (a) and linear representation of oxidation peak current versus square root of the scan rate (b).

The electrochemical operation is demonstrated through CV experiments at different scan rates with a 2 mM equimolar solution of the pair ferri/ferrocyanide in 0.1 M KCl. Data was extracted recording the digital signal q_{mod} sampled at 1 kS/s. For the third-order digital Bessel filter used here, the critical frequency at phase response midpoint has been set to 0.5, 1, 1.5 and 2.5 Hz for the scan-rates of 10, 20, 30 and 50 mV/s, respectively. Fig. 5.15(a) illustrates the obtained CVs. For a reversible redox process like ferri/ferrocyanide, the peak currents follow the Randles–Sevcik equation:

$$I_{\text{po,pr}} = 0.4463nFAC_o\sqrt{\frac{nFvD}{RT}}, \tag{5.5}$$

where v is the scan rate, R is the gas constant 8.314 j/(mol·K) and T is the absolute temperature.

A plot of the oxidation peak current, I_{po} versus the square root of the scan rate is shown in Fig. 5.15(b). From their linear dependence, it can be concluded that the electrochemical reaction behaves as a standard diffusion-controlled process [28]. In this sense, the diffusion coefficient of the electroactive species is calculated from (5.5), returning in $4.2e^{-6}$ cm^2/s, which is comparable to the values obtained in [148]. The reversibility of the system can also be corroborated, since the ratio between the oxidation/reduction yields a peak current ratio close to unity.

Conclusions | 6

6.1 Contributions

This last chapter presents the major contributions arising from the results of the research activities carried out in order to verify the main hypothesis given in Chapter 1:

> all the electronic frontend smartness required by an electrochemical sensor (i.e. potentiostatic control, amperometric readout, A/D conversion, power management and standard digital interface) can be embedded in a μW-range mm^2-size CMOS IC, which in turn can be directly attached to a flexible substrate where the sensor is printed.

Based on the above major milestone, the most relevant contributions of this PhD thesis can be summarized as follows:

- Experimental electrochemical characterization with state-of-the-art electrochemical sensors is performed for an accurate cell modeling, exploiting its use not only for sensing but also for signal processing.
- The advantage of the sensor-in-the-loop concept in novel electrochemical $\Delta\Sigma$M architectures is unveiled, leading to a very compact circuit implementation thanks to the the sensor double-layer capacitance C_{dl} reused as integrator stage inside the $\Delta\Sigma$M.
- A compact second-order electrochemical $\Delta\Sigma$M is proposed to improve the overall performance such as pattern noise suppression and precise potentiostatic operation.

- A low-frequency noise cancellation mechanism is introduced to cancel the flicker noise contributions coming from the CMOS current sources of the $\Delta\Sigma$M feedback DAC, improving the LOD by a factor of 4 down to 43 pA.
- Differential control of the potentiostatic voltage range is developed to further extend its programmability beyond the IC supply rails (e.g. 1.8-V_{pp} potentiostatic range under single 1.2-V CMOS supply).
- Biphasic current sensing capability with programmable multi-scaling (e.g. $\pm$100 nA to $\pm$1.5 μA) for multi-target detection and dynamic range extension.
- Integration of the proposed electrochemical $\Delta\Sigma$Ms and all the required auxiliary circuits into μW-range mm^2-size cost-effective ROICs in 65-nm and 0.18 μm CMOS technologies.
- Three-electrode inkjet-printed electrochemical cell fabricated, characterized and validated on a single flexible substrate for disposable devices.
- Low-cost assembly of the smart ROICs in the disposable flexible substrate by the use of anisotropic conductive adhesives.

The intention of this work is also to share as much as possible the results with the scientific and engineering community. In this sense, several publications in high impact journals as well as in international conferences have been achieved during the PhD thesis period.

Journals:

- J. Aymerich, A. Márquez, X. Muñoz-Berbel, F. J. Del Campo, G. Guirado, L. Terés, F. Serra-Graells, and M. Dei, "A 15-μW 105-db 1.8-Vpp Potentiostatic Delta-Sigma Modulator for Wearable Electrochemical Transducers in 65-nm CMOS Technology," in *IEEE Access*, vol. 8, pp. 62127–62136, 2020. https://doi.org/10.1109/ACCESS.2020.2984177
- A. Márquez, J. Aymerich, M. Dei, Rodríguez-Rodríguez R, M. Vázquez-Carrera, J. Pizarro-Delgado, P. Giménez-Gómez, Á. Merlos, L. Terés, F. Serra-Graells, C. Jiménez-Jorquera. C. Domínguez, and X. Muñoz-Berbel, "Reconfigurable Multiplexed point of Care System for Monitoring Type 1 Diabetes Patients," in *Biosensors and Bioelectronics*, vol. 136, pp. 38–46, 2019. https://doi.org/10.1016/j.bios.2019.04.015
- M. Dei, J. Aymerich, M. Piotto, P. Bruschi, F. J. Del Campo, and F. Serra-Graells, "CMOS Interfaces for Internet-of-Wearables Electrochemical Sensors: Trends and Challenges," in *Electronics*, vol. 8, 2019. https://doi.org/10.3390/electronics8020150

- J. Aymerich, A. Márquez, L. Terés, X. Muñoz-Berbel, C. Jiménez, C. Domínguez, F. Serra-Graells, and M. Dei, "Cost-Effective Smartphone-Based Reconfigurable Electrochemical Instrument for Alcohol Determination in Whole Blood Samples," in *Biosensors and Bioelectronics*, vol. 117, pp. 736–742, 2018. https://doi.org/10.1016/j.bios.2018.06.044

Conferences:

- J. Aymerich, M. Dei, L. Terés, and F. Serra-Graells, "A 72-μW 90-dB Wide-Range Potentiostatic CMOS $\Delta\Sigma$ Modulator with Flicker Noise Cancellation for Smart Electrochemical Sensors," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–5, Sapporo, Japan, 2019. https://doi.org/10.1109/ISCAS.2019.8702135

- J. Aymerich, M. Dei, L. Terés, and F. Serra-Graells, "A 6.5-μW 70-dB 0.18-μm CMOS Potentiostatic Delta-Sigma for Electrochemical Sensors," in *Proc. 14th Conf. Ph.D. Research in Microelectronics and Electronics (PRIME)*, pp. 25–28, Prague, Czech Republic, July 2018. https://doi.org/10.1109/PRIME.2018.8430329

- J. Aymerich, M. Dei, L. Terés, and F. Serra-Graells, "Design of a Low-power Potentiostatic Second-order CT Delta-Sigma ADC for Electrochemical Sensors," in *Proc. 13th Conf. Ph.D. Research in Micro- electronics and Electronics (PRIME)*, pp. 105–108, Taormina, Italy, June 2017. https://doi.org/10.1109/PRIME.2017.7974118

6.2 Future work

The final disposable smart electrochemical sensor prototype of this work has been tested and validated, and the findings are promising enough to conduct further research and experiments in this direction. Indeed, some optimization can be still explored to enhance the overall performance. In particular:

- The Silicon area of the ROICs could be further reduced by decreasing the size of the second stage of the $\Delta\Sigma$M noise shaper. Techniques such as extremely-low G_{m} [149], current division [150] and impedance scaling [151] could be contemplated.

- Although the synchronous standard I^2C interface allows to simplify the number of pads for the low-cost ROIC assembly, research could be conducted into ultra-low power asynchronous communication standards allowing wireless communications.
- Multi-channel architectures will be investigated for multi-electrode systems.
- End-user GUI interface on smartphone apps for data capture and visualization and cloud-based computing is expected to be developed.

The proposed ROIC for electrochemical sensors will be adapted and used in further projects such as *Wearable Sweat Biomonitoring Technology for Real-Time Personalized Diagnosis and Preventive Health (WeCare)* [152], which is a promising opportunity for applying and adding value to all the research presented here. The project aims to provide a decisive step forward towards understanding the important of sweat for a continue assessment of athletic fitness level.

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