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Development of Analogue circuits for the BETA ASIC HERD-FIT detector

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Abstract

The Electronics Instrumentation Service of the Insittute of Cosmos Science of the University of Barcelona (ICCUB-SiUB) is focused on developing ultrafast readout electronics for high-energy physics and medical imaging. In the framework of the HERD project (High Energy Cosmic-Radiation Detector) the group has developed the readout BETA-ASIC to push the limits of dark matter radiation research. Thus, the aim of this Master Thesis is to contribute to the ASIC design.

This project presents a low power comparator that will be used for detection triggering as well as internal path selecting of a multi gain system. The comparator has input rail-to-rail and hysteresis feedback. The power consumption is around 60 μW, the gain is 76 dB and the hysteresis amplitude is about 5.75 mV. The single-photon SNR is around 10, the delay is 15 ns and jitter is below 100 ps for input energies higher than 10 pe (photoelectrons). These simulations prove the fulfilment the requirements for the ASIC, and a first prototype has already been sent to be manufactured in April.

Acknowledgements

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Finally, I would like to thank Xavier Aragones for being the co-advisor of my Master Thesis.

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1. Introduction

The aim of this thesis is to contribute to the development of analogue circuitry for a High Energy Cosmic-Radiation Detector (HERD), which is destinated to be one of the several space astronomy payloads onboard of the future China's Space Station (CSS). The scientific goals of HERD are to address fundamental key problems in physics: (1) to search for signatures of the annihilation/decay products of dark matter, (2) to measure precisely the energy spectra, composition of primary cosmic rays (from 30 GeV to 50 PeV) and (3) to provide wide field of view for monitoring of the high energy gamma-ray.

The HERD facility includes several detectors where the scintillating Fibre Tracker (FIT) is the baseline tracking system. ICC-UB is in charge of the design of the Front-End ASIC, referred to as BETA (fi**B**re track**E**r readou**T** **A**sic), which will be used for the Silicon Photo-Multiplier (SiPM) readout of the FIT. Recently, the BETA ASIC has also been chosen to generate the trigger signal for the plastic scintillator detector (PSD).

Besides the involvement of Chinese institutions, led by CSU and IHEP, several European institutes have expressed significant interest and provided scientific contribution to the project. They include researchers from Italy (Universities of Bari, Florence, Lecce, Pisa/Siena, Pavia, Perugia and Istituto Nazionale di Fisica Nucleare (INFN) and Gran Sasso Science Institute), Spain (CIEMAT Madrid) and Switzerland (University of Geneva and École Polytechnique Fédérale de Lausanne (EPFL)).

In this context, the core of the Master Thesis has been dedicated to the design of an *input Rail-to-Rail Hysteresis Comparator* for the BETA ASIC. Complementary to this, a *Current DAC* has also been designed for biasing the comparator. Finally, partial design of other biasing blocks has been done for the sake of further practice.

1.1. Challenge

After a century since the discovery of gamma rays, there is still long way from answering fundamental questions about their nature. Although, some large ground-based experiments (AUGER, IceCube and HESS/MAGIC) and space-borne missions (PAMELA, FERMI, AMS and DAMPE) have taken place, large systematic uncertainties were observed in indirect detection and unexpected features in the flux of cosmic ray electrons, protons and light ions have been observed recently in direct detection, which could indicate some missing pieces in the current cosmic ray acceleration and propagation models.

At present, there are very few individual flux measurements around the "knee" region (~1 PeV), but it is precisely in this region that interesting features in the total flux are being observed by ground-based experiments. Therefore, a new space instrument with ~10 times larger acceptance compared to the current generation of missions is needed to measure precisely the spectrum and the elemental composition [1].

1.2. HERD Project

In the baseline design, HERD is composed of a deep 3-D cubic imaging calorimeter (CALO) made of LYSO crystals with an innovative design that ensures the same accuracy in the energy measurement and e/p separation for particles entering the detector from five out of the six sides. As *Fig. 1* shows, on the top and on the four sides of the calorimeter, from outside to inside, there are a silicon charge detector (SCD) for the nuclei identification, a plastic scintillator detector (PSD) for veto and charge measurements and a scintillating fibre tracker (FIT). A Transition Radiation Detector (TRD), located on one of the lateral sides, is used for the energy calibration of TeV nuclei. The total weight of the HERD payload will be <3 tons, within a dimension envelope of $\cong 2\ x\ 1.7\ x\ 1.2 m^3$ (L x W x H) [1].

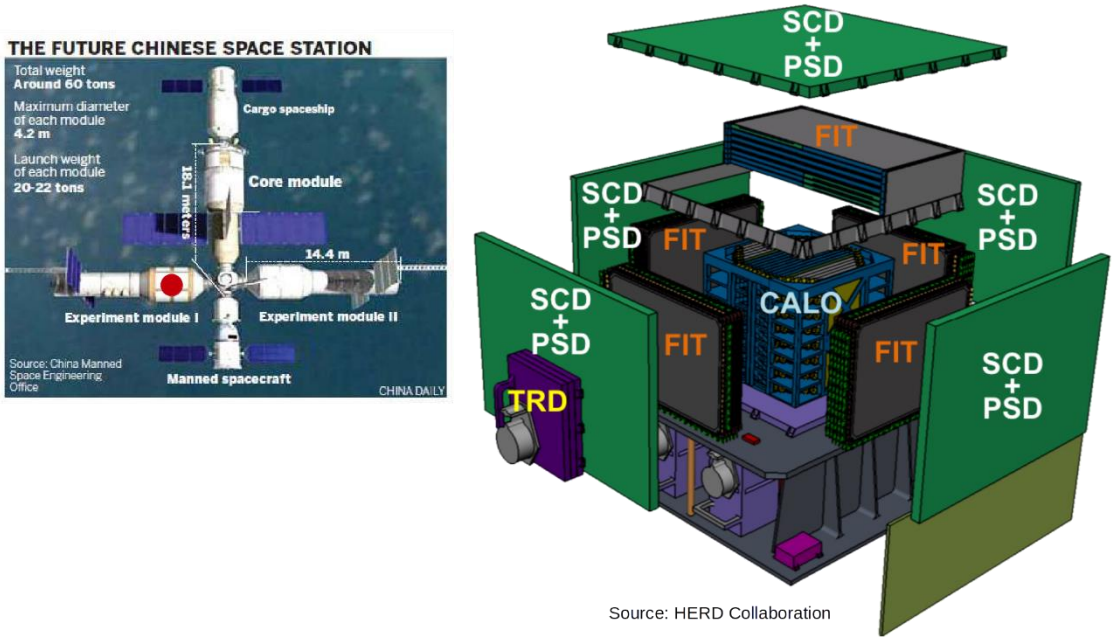

Fig. 1 The HERD detector onboard the "Experiment module I" of the Chinese Space Station

The sensor baseline solution is the use of Silicon Photomultiplier Arrays, that can stand the temperature, mechanical stress and radiation levels. The initial solution is based on the SciFi detector ones [2]. The already designed device has been redesigned to cope with the required dynamic range and number of cells for high energy signal measurement and needed energy resolution. Because of this, the current number cells used for SciFi detector (104) have been increased to around 1750 ($15x15\mu\ m$ cell size) or 4000 ($10x10\ \mu m$ cell size).

The SiPM can be electrically modelled as shown in *Fig. 2*. In this model we distinguish between two type of cells: firing cells, or cells that have been hit by a photon, and passive cells, cells that have not been hit and remain inactive. The single microcell is a single-photon avalanche photodiode (SPAD) that operates in Geiger mode and later quenched by an integrated resistor.

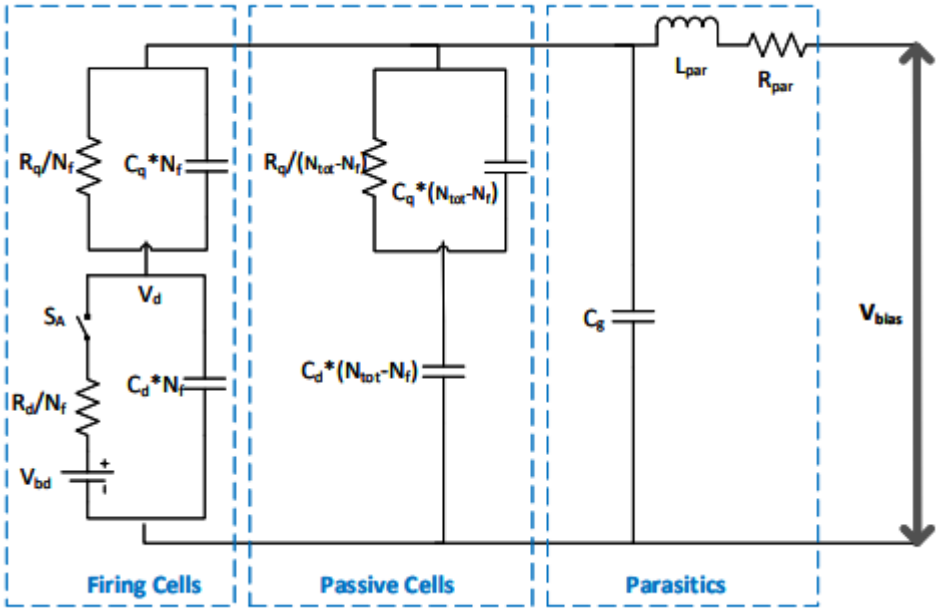

Fig. 2 Electrical model for SiPM (Figure taken from [3] *)*

The electrical model of each cell, which is biased slightly above the breakdown voltage (over-voltage), includes the diode resistance R_d and capacitance C_d, the quenching resistance R_q and a small capacitance C_q and a switch S_A that closes the circuit when photons hit the sensor. Parasitic components are taken into account with L_{par}, C_g and R_{par}.

Initially, C_d is charged to SiPM bias voltage V_{bd}. When a photon hits a cell, S_A closes making the start of a breakdown event (N_f corresponds to the number of cells fired). C_d discharges through R_d, with a time constant $R_d(C_d + C_q)$ (($R_d \ll R_q$)), and intermediate node voltage V_d decreases rapidly. At the same time, this generates a current that flows through the quenching resistor. This rapid current increase is the responsible for the fast rising edge of the readout current. As the quenching capacitor charges, the current flowing through the quenching resistor decreases, until it reaches a predefined threshold quenching current I_q and the bias of the SPAD is restored. This is modelled by opening the switch. This reset phase is determined by the discharging by two time constants: (1) when the avalanche is over, C_d is charged again to the biasing voltage V_{bd} with a fast time constant $R_{load}C_{tot}$[1]. (2) During the recharging of the diode, the current through the quenching resistor starts decreasing exponentially with a slow time constant $R_q(C_q + C_d)$. The reset phase ends when $V_D = V_{bias}$. *Fig. 3* illustrates the working principle of the SiPM [3].

[1] $C_{tot} = C_g + N_{tot}(C_d + C_q)$ and R_{load} is associated to the input impedance of the chip.

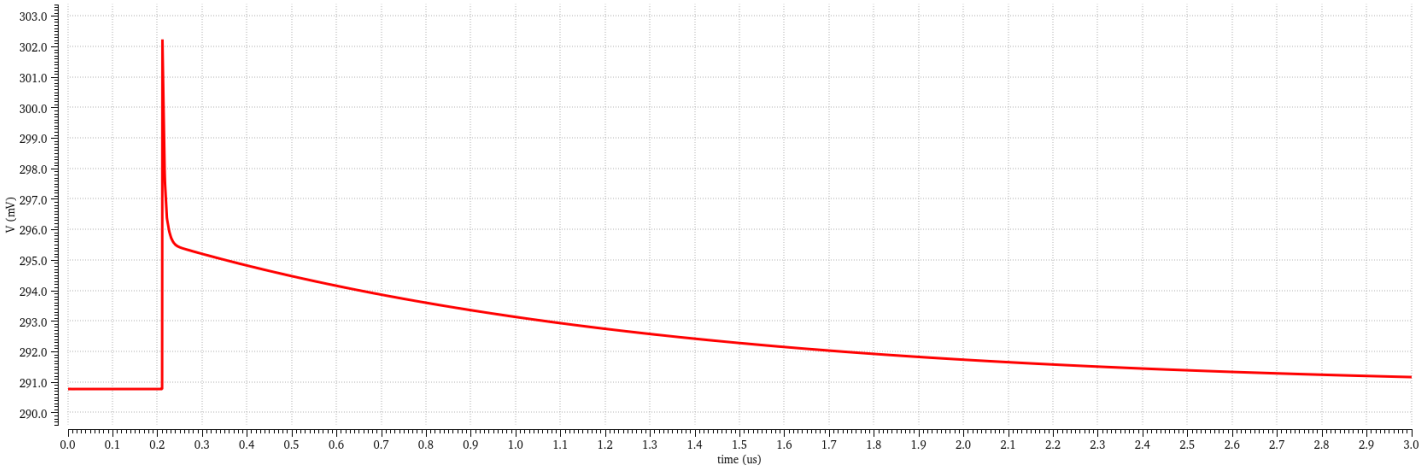

Fig. 3 Avalanche and reset phase in the fired cells of the SiPM

1.2.1. HERD –ASIC (BETA)

The main objective of the BETA ASIC is to perform the signal processing with very low power consumption, large dynamic range and a good signal to noise ratio (SNR) at the single photo-electron level. The 16-channel[2] ASIC is designed in a CMOS 130 nm technology with a total area of 3.38 x 1.96 mm^2. It includes a trigger signal for the incoming photons and the measurement of charge captured by the SiPM, which is provided by a digitalized serial output. *Fig. 4* shows the block diagram of the chip's analogue Front-End.

The key parameter requirements are low power (**500 $\mu W/ch$**), a high dynamic range of **12 *bits*** (**676 *MIP*** or **18748 *phe***), radiation hardness of at least **80 *Gray***[3] and ***SNR*** larger than **5 (linear)** for operation. The chip must operate in a temperature range between **-20 ºC** and **50ºC**. *Table 1* sums up the ASIC requirements.
This ASIC has been developed in TSMC **130 *nm*** technology, a technology that is already qualified for higher radiation levels at CERN and it is used for the PACIFIC chip [4].

Specification	Target
Channels	64
Input rate	1 kHz (max)
Power draw	0.5 mW/ch (1.2 V supply)
Radiation Hardness	80 Gray
Dynamic Range	676 MIP (18748 phe) or 12 bits
Minimum detectable charge	0.1 MIP (2 phe)

[2] The first prototype has 16 channels, and the final prototype will include 64 channels
[3] It is defined as the absorption of one joule of radiation energy per kilogram of matter

Slow control	I2C
SNR for operation	> 5 (to set 3.5phe threshold)

Table 1 FIT ASIC specification

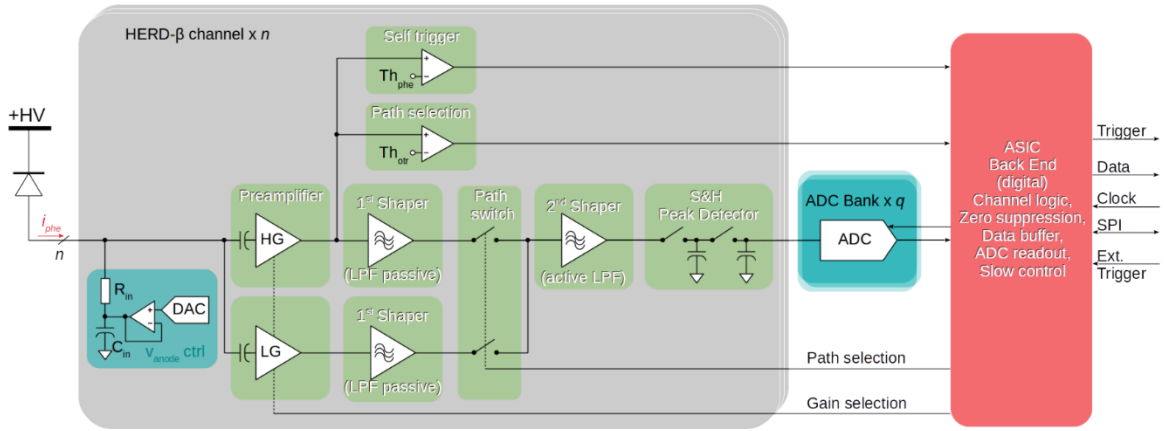

Fig. 4 Block diagram of the BETA ASIC

The Front-End architecture is based on a multi-gain system that reads the input current from each SiPM and converts it into voltage by means of a resistor divider circuit, one for each preamplifier. The output of the *High-Gain Amplifier* is used for triggering an incoming event and for selecting internally the gain path depending on the number of detected events. This multi-gain system intends to provide good amplification for low number of photons, as SNR is required for 1 photon. However, when hundreds of electrons are detected, the *High-Gain Amplifier* saturates the whole dynamic range available at the output. In order to prevent this, the *Low-Gain Amplifier* is selected by means of a path selection comparator.

The signal measurement is performed in several stages. A shaping stage is divided into an initial first-order LPF for each of the HG and LG preamplifiers. This LPF slows down the signal to give time to the digital circuitry to select between HG and LG signal paths by means of an analogue switch. The selected signal path is again filtered by a second-order LPF using a Sallen-Key topology. The peak amplitude is captured by a Track and Hold (T&H) circuit and the digitalization is made by means of a Wilkinson ADC.

1.3. Objective

The main objective of the thesis is to design a voltage comparator that will perform two different functionalities inside the chip: signal triggering and selection of the path to implement the multi-gain channel processing scheme. The target is to design a comparator

that can operate at different threshold levels along all dynamic range of the input signal. This is why a Rail-to-Rail input is required.
Due to the power source limitation of onboard electronic applications, the comparator power consumption will be limited to 50 μW. The gain should be maximized for this power consumption.
Comparators are susceptible from small variations around the reference level due to the external and electronic noise. Thus, a hysteresis comparator has been proposed to provide robustness against noise variation. The hysteresis amplitude should be between 4 and 6 mV.

The trigger comparator needs to be fast enough to follow the incoming events on the chip, so the desired delay will be around 15 ns . Also, the desired jitter is the minimum possible but, as it is a low power comparator, big jitter is inevitable at low energies. Even though, the target jitter below 100 ps at 10 events is fixed, which was required for the plastic scintillator detector. Finally, a single-photon $SNR = 5$ $(linear)$ has been required.

The path selection comparator does not have particular constraints for the jitter, but it is important to select the gain path before the first shapers load the output. Although the delay is crucial for the correct performance of the ASIC, the comparator delay differ in one order of magnitude from the shaper delay (~250 ns in nominal configuration).

The specs are summarised in *Table 2*.

Specification	Target
Power Supply	< 50 μW
Gain	Maximise
Hysteresis amplitude	$4 - 6mV$
Delay **Jitter**	< 15 ns < 100 ps at 10 pe
SNR	5 (linear)

Table 2 Comparator specifications

Finally, the current DAC will be designed to provide the current bias of the comparator. This DAC will be configurable, leaving the option to modify the current consumption if needed. The initial target DC output current is 1 μA.

1.4. Gantt diagram

Fig. 5 shows the summary of the project main phases. It has taken around 9 months to complete it.

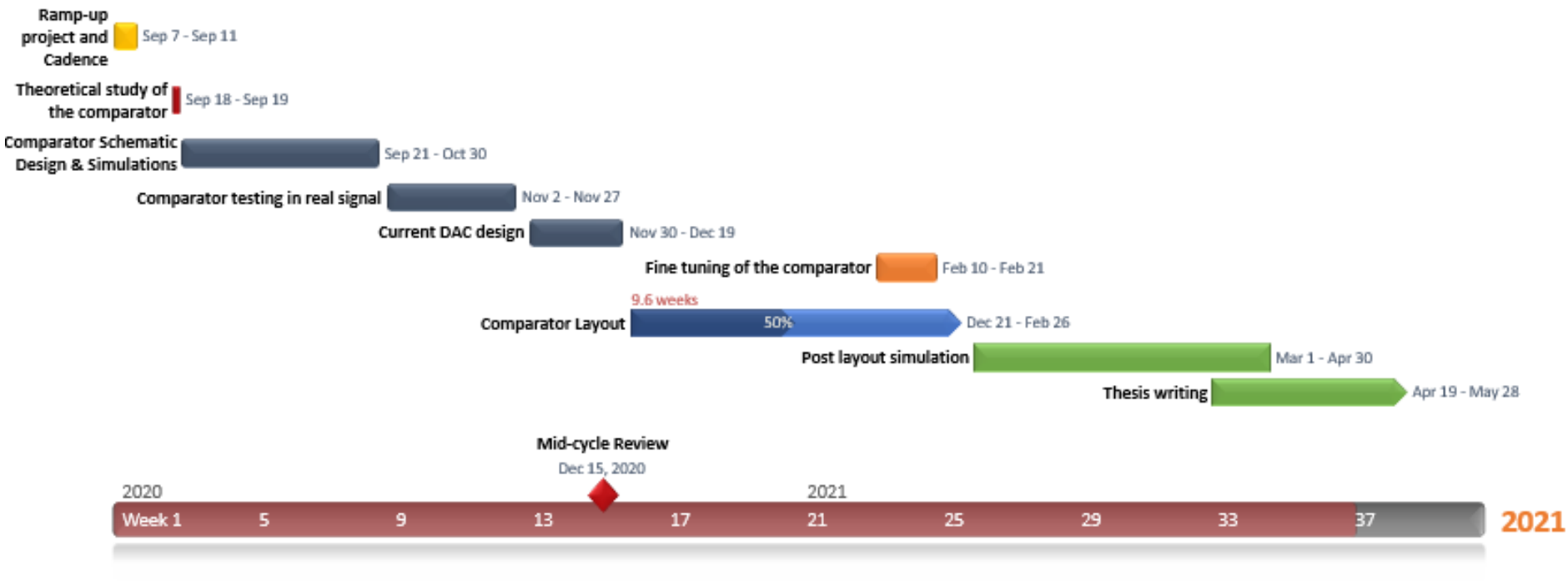

Fig. 5 Gantt diagram

2. Theoretical analysis of the comparator

The Rail-to-Rail (R2R) Hysteresis Comparator is designed to perform a double functionality inside the chip: acting as a trigger comparator and selection of the path to implement the multi-gain channel processing scheme.

Fig. 6 shows the signal waveforms expected after each block. The SiPM models the incoming photons in an exponential shaped signal, and the *High-Gain Amplifier* and *Low-Gain Amplifier* amplify, as well as invert, the signal according to their respective gains. The first low pass filter eliminates the high-frequency components, making the output signal slower. The comparators come into picture during the time the low-pass filter is shaping the signals.

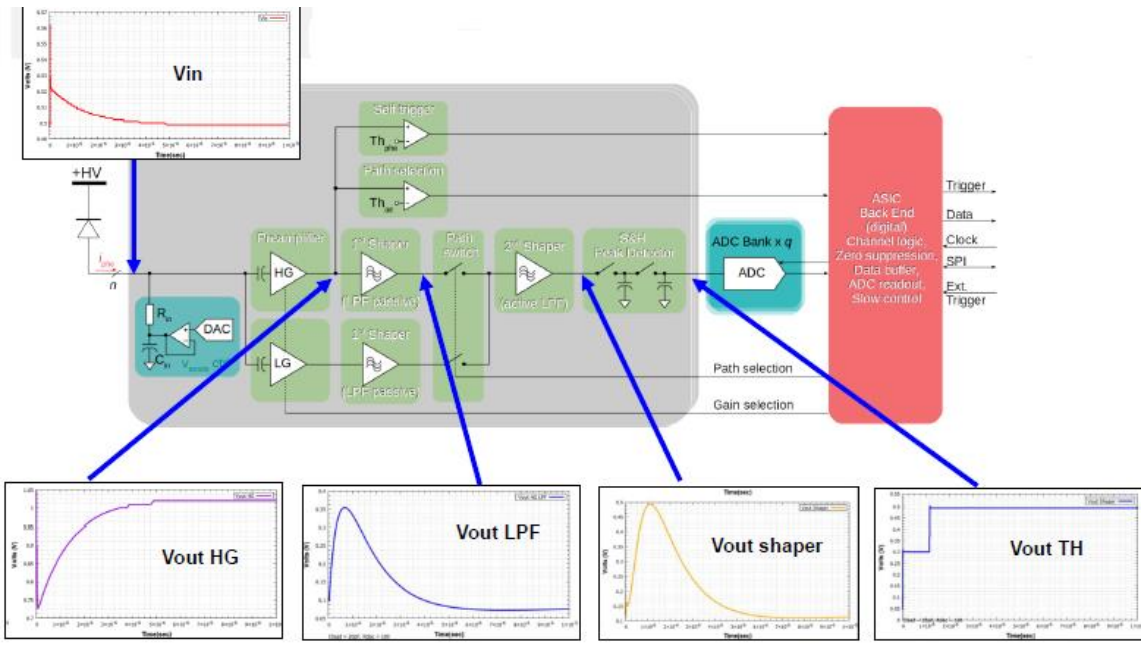

Fig. 6 Block diagram with input and output signals

As it can be seen in *Fig. 6,* the input signal at the comparators is the one at the output of the *High-Gain Amplifier*. It is an inverted exponential pulse, which baseline (input DC level) is at $1\,V$. The amplitude at the output of the *High-Gain Amplifier* depends linearly on the number of photons, where the amplitude increases about 5 mV with each photon.

Fig. 7 shows the input signal at the comparator in case of different number of photons (or events).

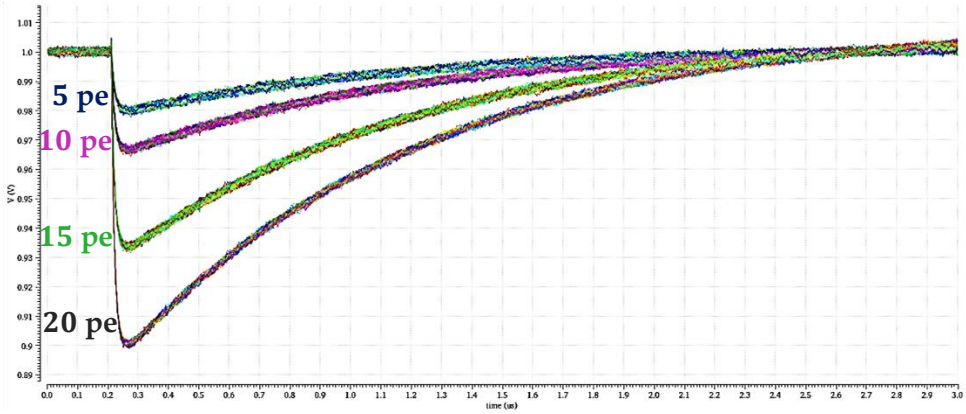

Fig. 7 Comparator input signals mixed with noise

Fig. 8 illustrates the principle of working of the comparator. The incoming signal is mixed with noise, which produces the timing variation in the output response. This time variations will be approached in the next chapter, when we study the noise in the comparator.

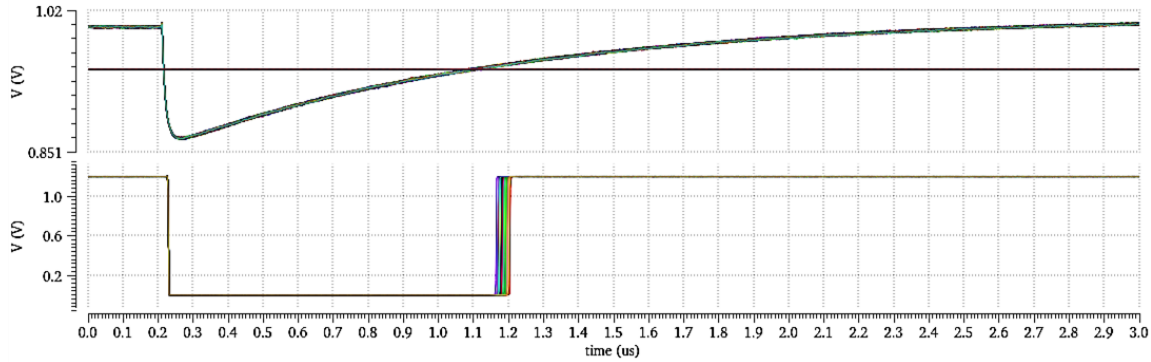

Fig. 8 Comparator input and output signals mixed with noise

Designing a single comparator means that it will need to work for very different input common mode voltages: the reference voltage of the trigger comparator will be near the DC level of the input signal whereas the reference of the path selection comparator will be very far.

The trigger comparator is responsible for sending a pulse to the digital backend when an event is detected. The threshold voltage level will be set according to the minimum number of events that can be detected. However, in order to prevent triggering due to Dark Count[4] a safety margin needs to be left. For the correct operation and synchronization among the rest of the blocks, this comparator has certain specifications that have been explained in the previous section.

On the other hand, the path switching comparator is responsible to switch from the *High Gain* path to the *Low-Gain* path when the input energy level is high enough. The reason for

[4] Dark Count is an undesired effect of SiPMs, where spontaneous electron-hole pairs are generated due to the thermal noise. The frequency at which these e/h pairs appear is called *Dark Count Rate.*

this is that the the chip has a multi-gain system, where both paths amplify and shape the signal. The high gain is needed to detect low number of photons, but when higher energies are detected the *High-Gain Amplifier* saturates the whole dynamic range (power supply 1.2 V) available. At this time, the path switching comparator sends a command to the backend so that it chooses the signal coming from the *Low-Gain* path. Although this comparator is not as demanding as the trigger comparator, the time response is critical here, because it needs to switch before the low pass filter modifies the signal. *Fig. 9* illustrates an example of gain path switching. In this example the path should be switched when 200 events are detected.

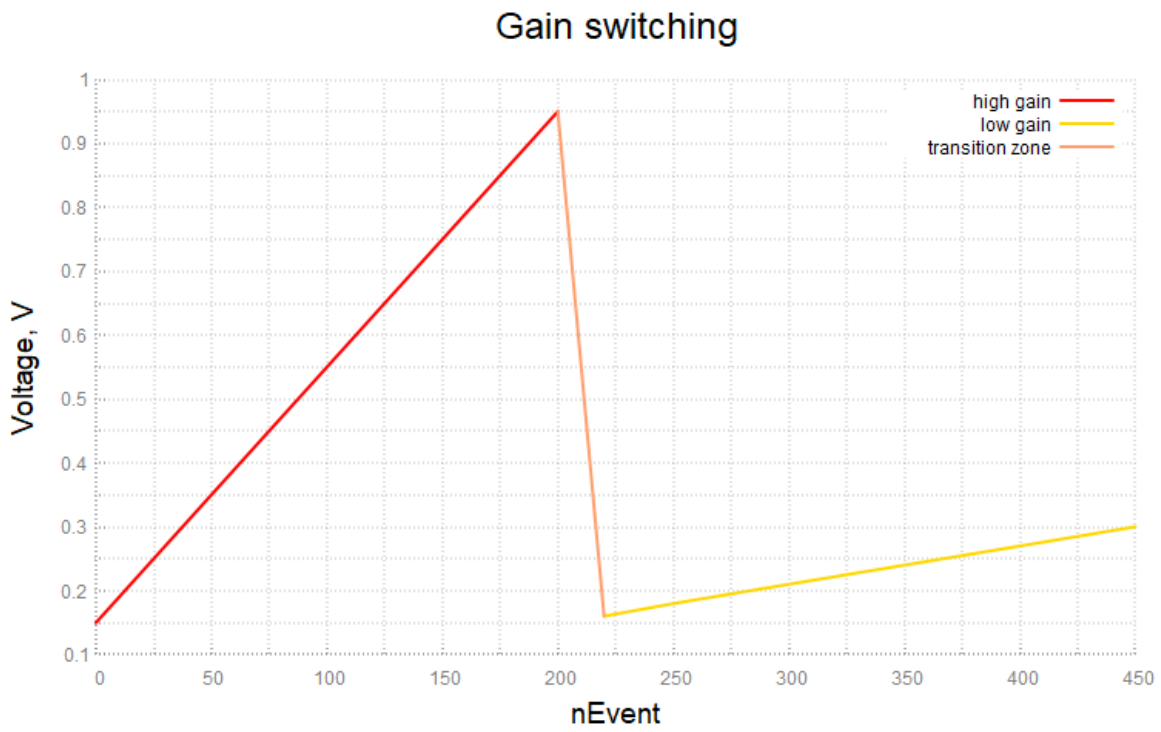

Fig. 9 Example of gain switching

As the baseline of the incoming exponential signal will be 1 V, the threshold of the trigger comparator will be around 900 mV, while in the path selection comparator it will be around 100 mV. As the first one is the most demanding, the next sections will be devoted to its study.

The design of this comparator is entirely based on topologies used in other readout ASICs, such as FASTIC and HREFLXTOT. However, the design for HERD-BETA has been done at 130 nm node (TSMC), whereas FASTIC and HREFLXTOT have been manufactured at 65 nm (TSMC) and 180 nm (XFAB) [7] respectively. Another novelty is that low power requirements for the comparator (power supply 1.2 V), same as in FASTIC, while HREFLXTOT was fed with 1.8 V.

The comparator consists of four cascaded stages, including an enable bit buffer.

The first stage is a R2R input Fully Differential Amplifier (FDA) and the second stage is a basic FDA. The aim of the first two stages is to amplify the difference between the input signals, since the comparators work with high differential voltages. The reason we want

R2R input is that the baseline of the incoming signal is fixed at 1 V, and depending on the signal energy level, the input pulse may cover all the dynamic range. The second stage input does not need to be rail to rail, since the output of the first stage is not Rail-to-Rail and thus only a simple FDA with nMOS differential pair is used. Finally, the third stage is a hysteresis comparator, necessary to prevent the output oscillates due to the input signal fluctuations -mainly due to noise- around the threshold level. A NOR gate provides the possibility to set the output to zero and thus disable the comparator.

Fig. 10 shows the comparator is composed by 4 stages (from left to right):

- Rail to rail fully differential amplifier
- Classical fully differential amplifier
- Comparator with hysteresis
- Output NOR gate

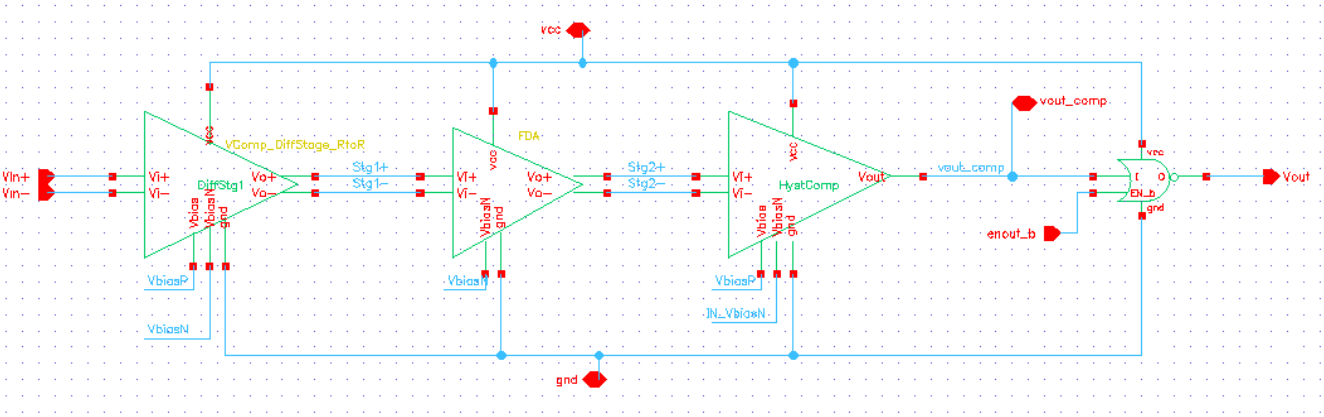

Fig. 10 Comparator Stages

For ease of convenience, the theoretical analysis will begin with the FDA, as the first stage is in practice an enhancement of it.

2.1. Fully differential amplifier with resistive load

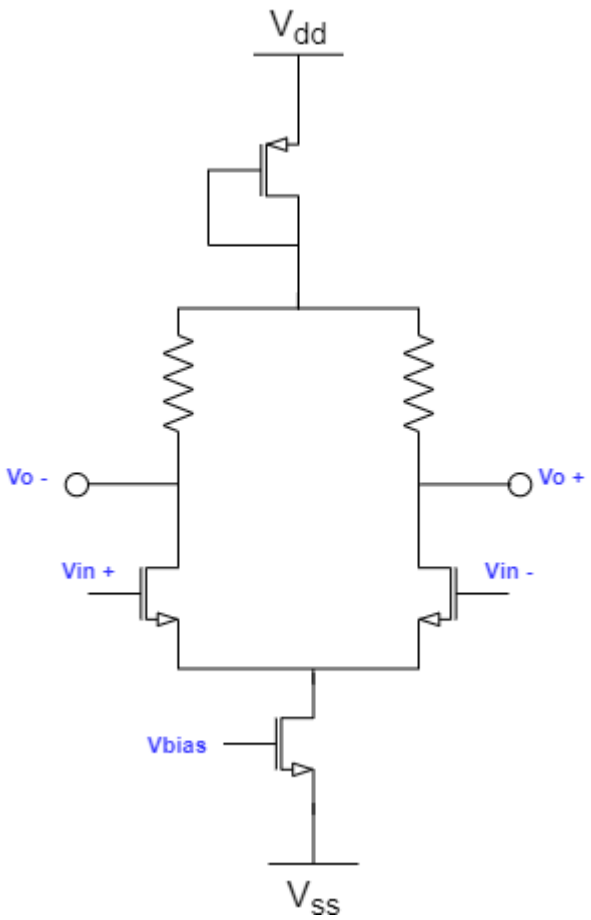

Fig. 11 Simple fully differential amplifier

Working principle

The basic fully differential amplifier topology consists of a differential pair biased with a current source and loaded with resistors. In this case, the sources are biased with the current generated by the tail transistor, while the resistors convert the tail current into voltage producing a differential output voltage. The circuit is closed by a diode connected pMOS transistor, which helps to decrease the DC output voltage level. This is a method to ensure that next stage does not need input Rail-to-Rail. The initial circuit analysis does not include this diode, so in the end the general equation is modified to take into account the effects it may produce. The analysis carried out in this section is based on the subject *Advanced Analog Circuit Techniques* by Xavier Aragones.

Fig. 12 ***¡Error! No se encuentra el origen de la referencia.*** sketches the output differential v oltage dependence on the differential input as a consequence of DC currents I_{D1} and I_{D2} above.

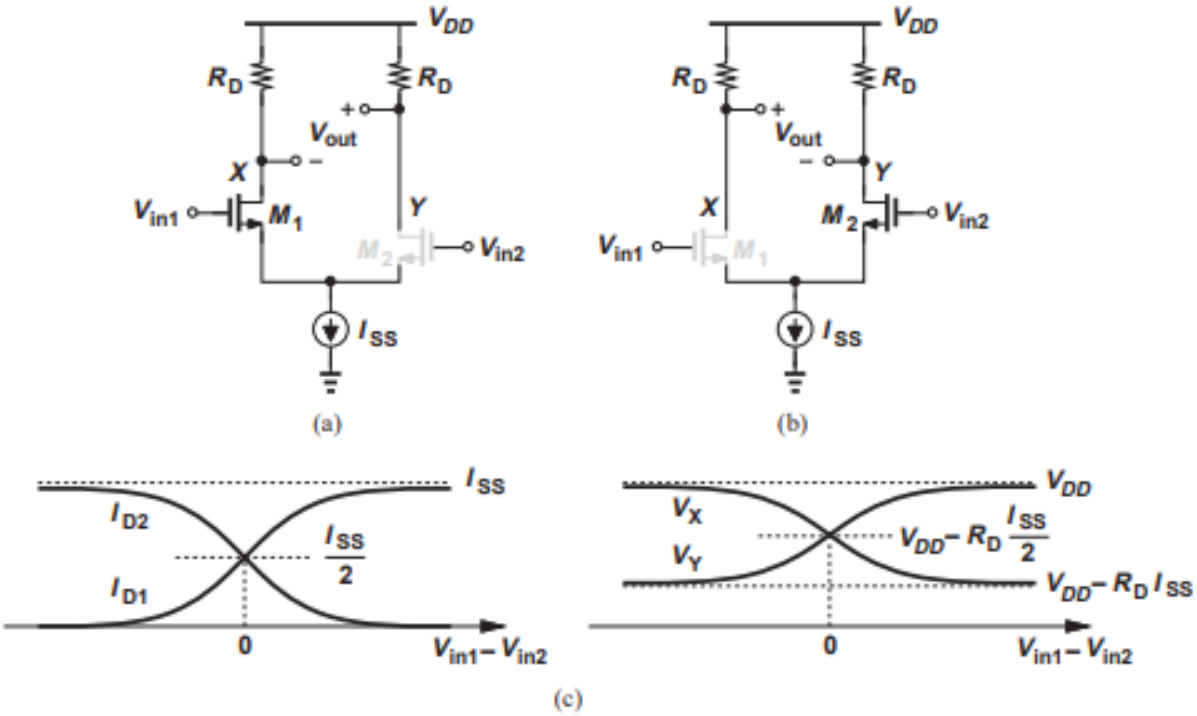

Fig. 12 (a) Response of MOS differential pair to very positive input, (b) response of MOS differential pair to very negative input, (c) qualitative plots of currents and voltages. (Figure from B. Razavi, Fundamentals of Microelectronics)

This circuit can operate in two different regimes. As small-signal amplifier or as a comparator. For amplification, the region of interest is the linear region of the amplifier output response, thus, small differential voltages. In case we want a comparator, this is, obtaining either a "large" or "small" signal depending on the input values, we should operate with large differential signals.

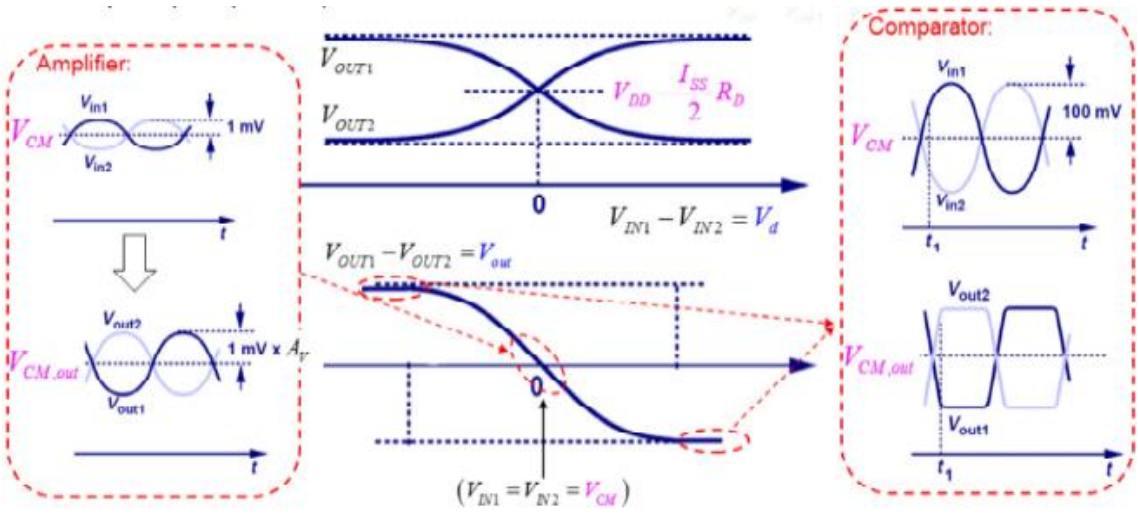

Fig. 13 Circuit behaving as amplifier or as comparator (Figure from B. Razavi, Fundamentals of Microelectronics)

DC analysis

For a linear operation, we need transistors M1 and M2 polarized in the saturation region, which limits the maximum common-mode input voltage, as shows *Fig. 14*:

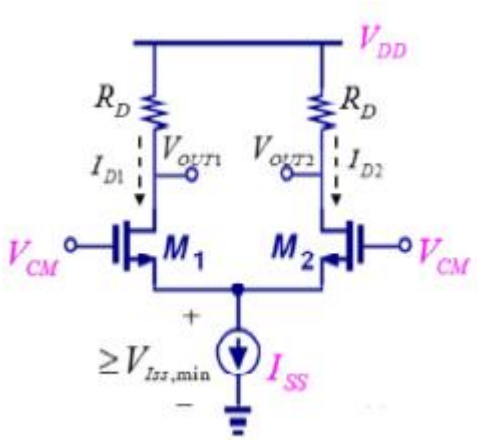

Fig. 14 Basic fully differential amplifier (Figure from B. Razavi, Fundamentals of Microelectronics)

$$V_{DS} \geq V_{GS} - V_T$$

$$V_D \geq V_G - V_T$$

$$V_{CM} = V_G \leq V_D + V_T$$

$$V_{CM} \leq V_{DD} - \frac{I_{SS}}{2} R_D + V_T$$

We need to leave room for the signal, so:

$$V_{CM} + v_{in} \leq V_{DD} - \left(\frac{I_{SS}}{2} + i_d\right) R_D + V_T$$

Where v_{in} and i_d are the positive value of the differential signal amplitude and differential current, respectively.

In our case, the diode connected transistor changes slightly the equation

$$V_{CM} + v_{in} \leq V_{DD} - \left(\frac{I_{SS}}{2} + i_d\right) R_D + V_T - V_{DS_{sat,diode}}$$

The minimum common-mode voltage is set by the current source:

$$V_{CM} - V_{GS} \geq V_{I_{SS,min}}$$

$$V_{CM} \geq \sqrt{\frac{I_{SS}}{K}} + V_T + V_{I_{SS,min}}$$

Actually

$$V_{CM} - v_{in} \geq \sqrt{\frac{I_{SS}}{K}} + V_T + V_{I_{SS,min}}$$

The circuit thus behaves linearly for small values of ΔV_{in} and becomes completely nonlinear for $\Delta V_{in} \geq \Delta V_{in,max}$. In other words, $\Delta V_{in,max}$ serves as an absolute bound on the input signal levels that have any effect on the output.

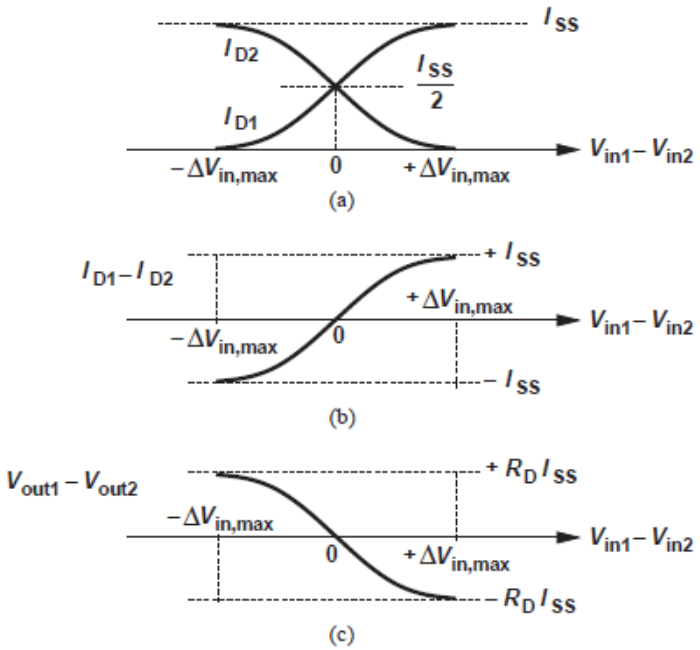

Fig. 15 Variation of (a) drain currents, (b) the difference between drain currents, and (c) differential output voltage as a function of input. (Figure from B. Razavi, Fundamentals of Microelectronics)

AC analysis

Fig. 16 shows the small signal equivalent circuit, which can be simplified by observing that node VSS is a virtual ground. This simplification comes from the observation that as far as the differential variation V_d is small and circuit symmetry is preserved, the current variation in M1 will be fully absorbed by the current variation in M2.

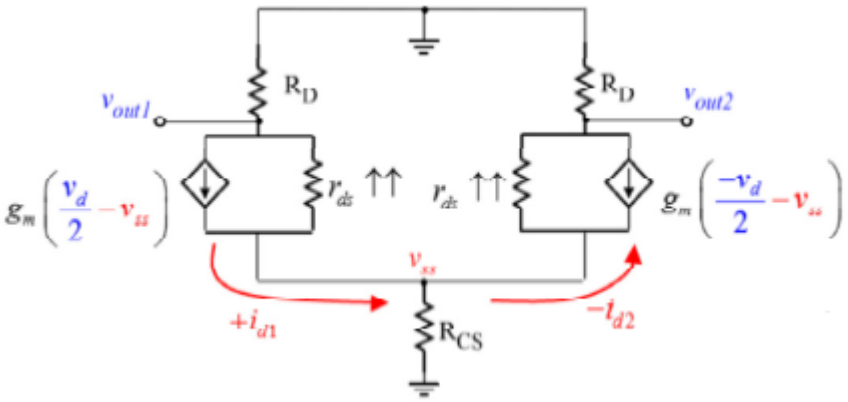

Fig. 16 small signal model of the FDA (Figure from slides of AACT subject, X. Aragonés)

This observation greatly simplifies the analysis of the former small-signal equivalent, which now reduces to two independent sub circuits, that can be analysed separately.

Circuit analysis with virtual ground is straightforward.

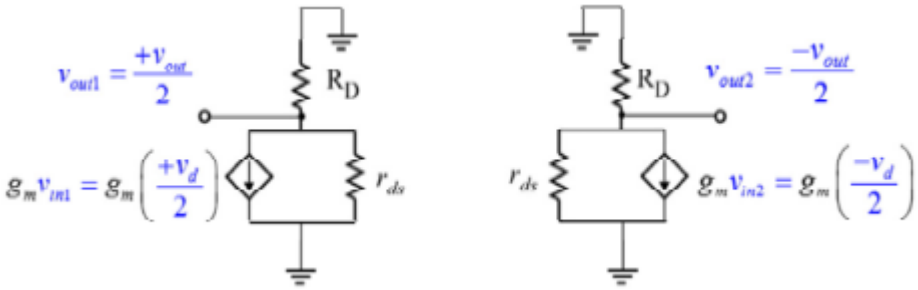

Fig. 17 simplified half circuit FDA (Figure from slides of AACT subject, X. Aragonés)

$$v_{out1} = -g_m \frac{v_d}{2}(r_{ds}||R_D)$$

$$v_{out2} = g_m \frac{v_d}{2}(r_{ds}||R_D)$$

$$A_{v_d} = \frac{v_{out}}{v_d} = \frac{v_{out1} - v_{out2}}{v_d} = -g_m(r_{ds}||R_D) \cong -g_m R_D$$

The obtained result for the gain is the same as that of the single-ended differential amplifier, but the total I_{SS} is doubled now. Also, note the 180° phase inversion can be easily removed just by reversing the definition of the positive and negative output terminals, i.e. $v_{out} = v_{out2} - v_{out1}$.

Adding load capacitances C_L at the output nodes, BW can be estimated. Virtual node and half circuit analysis can still be used, as far as symmetry is preserved. Again, the same expression as in a single-ended common-source stage are obtained (*Fig. 18*).

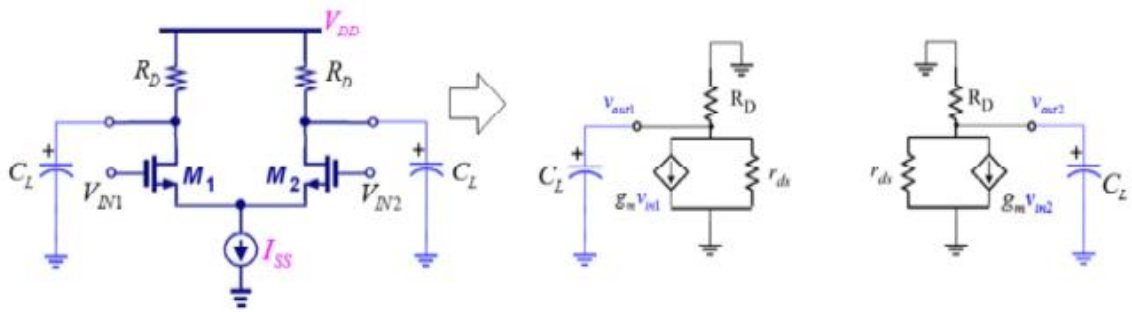

Fig. 18 Adding capacitances at output, for BW estimation. (Figure from slides of AACT subject, X. Aragonés)

$$A_{v_d} = -g_m\left(R_D \,||\, Z_{C_L} \,||r_{ds}\right) = \frac{-g_m(R_D \,||r_{ds})}{1 + j\omega(R_D \,||r_{ds})C_L}$$

$$BW \cong \left|\omega_{pout}\right| = \frac{1}{(R_D \,||r_{ds})C_L} \cong \frac{1}{R_D C_L}$$

Looking again back to *Fig. 11* the pMOS diode placed on top does not alter the expressions for the gain and the bandwidth, as the drain node could be considered as virtual ground. The only effect this diode will produce is to decrease the output DC voltage level of the amplifier.

2.2. Rail-to-Rail Fully Differential Amplifier

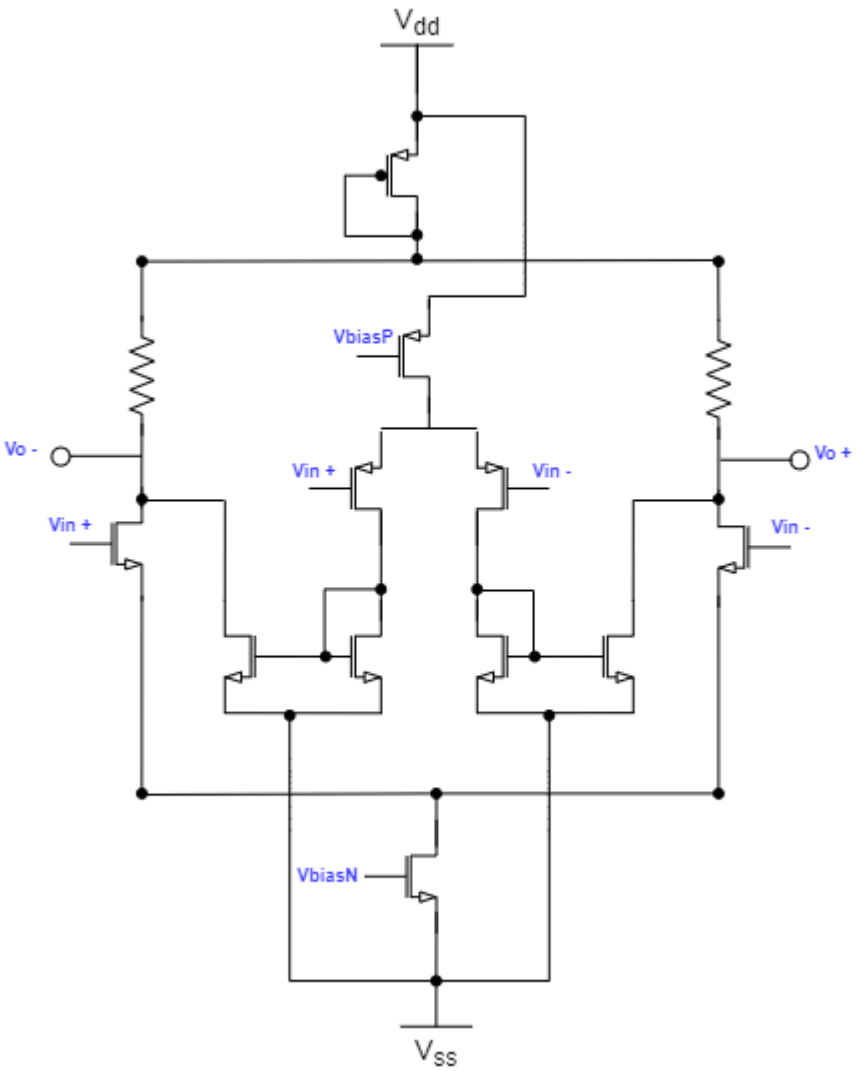

Fig. 19 R2R FDA used in the first stage

The architecture in *Fig. 19* is similar to previously analysed amplifier. The only difference is that a pMOS differential pair is added, and the amplified signal is copied by a simple

current mirror. The transistor above the differential pair acts as a current source. As already said, the diode connected transistor limits the voltage excursion at the output.

DC analysis

The common mode range that covers the nMOS pair has already been studied. For the pMOS differential pair a similar derivation can be made.

The minimum common mode that operates the pMOS pair is determined by the current mirror:

$$|V_{DS}| \leq |V_{GS}| + |V_{TP}|$$
$$V_D \leq V_G + |V_{TP}|$$
$$V_{CM} = V_G \geq V_D - |V_{TP}|$$
$$V_{CM} \geq V_{GS_{mirr}} - |V_{TP}|$$

We need to leave room for the signal, so:

$$V_{CM} - v_{in} \geq V_{GS_{mirr}} - |V_{TP}|$$

Where v_{in} is the positive value of the differential signal amplitude.

The maximum common-mode voltage is set by the pMOS tail transistor.

$$V_{CM} + |V_{GS}| \leq V_{DD} - V_{I_{SS_P}}$$

Using the relation $|V_{GS}| = \sqrt{\frac{I_{SS_p}}{K_p}} + |V_{TP}|$

$$V_{CM} \leq V_{DD} - V_{I_{SS_P}} - \sqrt{\frac{I_{SS_p}}{K_p}} - |V_{TP}|$$

Leaving room for the signal,

$$V_{CM} + v_{in} \leq V_{DD} - V_{I_{SS_P}} - \sqrt{\frac{I_{SS_p}}{K_p}} - |V_{TP}|$$

In summary,

For pMOS:

$$V_{CM} - v_{in} \geq V_{GS_{mirr}} - |V_{TP}| \quad ; \quad V_{CM} + v_{in} \leq V_{DD} - V_{I_{SS_P}} - \sqrt{\frac{I_{SS_p}}{K_p}} - |V_{TP}|$$

For nMOS:

$$V_{CM} - v_{in} \geq \sqrt{\frac{I_{SS_n}}{K}} + V_{TN} + V_{I_{SS_n}} \quad ; \; V_{CM} + v_{in} \leq V_{DD} - \left(\frac{I_{SS_n}}{2} + i_d\right) R_D + V_{TN} - V_{DS_{sat,diode}}$$

For the R2R Amplifier, the lower bound of the common mode is set by the pMOS pair and the upper bound is set by the nMOS pair.

AC analysis

The AC analysis is also similar to the previous FDA. This time, however, we should add a parallel drain-to-source resistance corresponding to the transistor that copies the current flowing from pMOS branches. The drain-to-source resistance should be parallel-connected to nMOS differential pair r_{ds}. And the result of this, in parallel with R_D and diode resistance.

$$R_{out} = \left(r_{ds_{mirror}} || \, r_{ds_{diff}}\right) || \, R_D$$

To calculate the differential gain, we can use the expression for common-source configurations: $g_m \cdot R_{out}$. In this case, the transconductance is contributed by nMOS differential pair and its counterpart pMOS differential pair. Both transconductances are added, so that the overall transconductance is $g_m = g_{m_n} + g_{m_p}$.

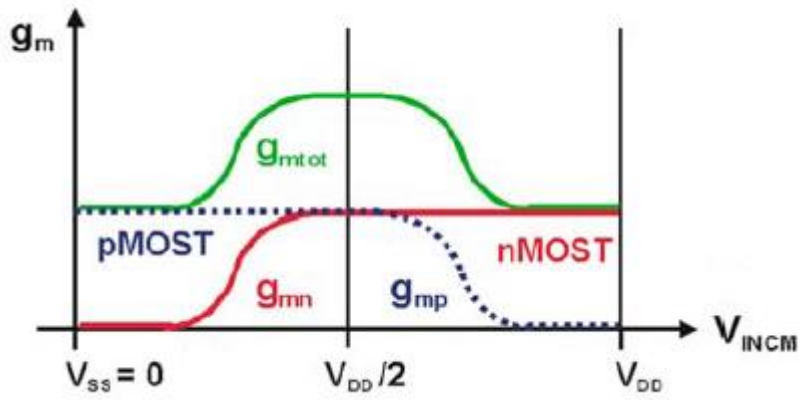

Fig. 20 Unequalized g_m for differential pairs (Image taken from Willy Sanse, Analog Design Essentials)

Fig. 20 illustrates the fact that when a differential pair is off, their corresponding transconductance goes to zero, obviously. Now the overall transconductance of the circuit is no longer constant at the extreme common modes, which causes compensation problems[5]. This will make the transistor behave different in all the common modes. However, this is not critical for the design, as the comparator will work for fixed common mode voltages. Adding an equalization solution would make the power consumption increase and the benefit we would obtain is not that important.

[5] Willy Sansen's book *Analog Design Essentials* proposes an ingenious solution to equalize the overall circuit transconductance. However, as it is not used in this topology, this part will be skipped.

Finally, the bandwidth of the R2R amplifier, in case we analyse it individually:

$$BW \cong |\omega_{pout}| = \frac{1}{R_{out}C_L} \cong \frac{1}{R_{out}C_L}$$

Although cascading amplifiers the voltage gain is multiplied, the bandwidth decreases.

2.3. Hysteresis Comparator

The hysteresis comparator is the core element of the comparator block, as it is responsible for detecting differences between incoming signals. This comparator is enhanced with hysteresis, which will provide robustness against variations caused by noise, ripple or other signal integrity faults. The following explanation is taken from Allen, and Holberg's book, *CMOS analog circuit design* [5].

Working principle: basics of hysteresis

One of the issues a comparator may face is the input signal fluctuations around the reference voltage level as a consequence of the noise. If the comparator is fast enough to follow the noise at the input, the output will show undesired glitches that do not correspond to the input signal change.. In this situation, hysteresis is needed in the comparator.

Hysteresis is the quality of the comparator in which the input threshold changes as a function of the input (or output) level. For instance, if the incoming signal surpasses the reference (threshold) level, and hence cause a transition at the output, the threshold voltage will be subsequently reduced or increased so that no transition happens unless the signal returns beyond this "new" threshold. This upper/lower reference levels are named *trip points*, which can be set by design. In practice, we could understand hysteresis as a guard zone around the threshold voltage that prevents the output from transitioning when the signal oscillates inside these guard zones.

This can be illustrated much more clearly with the diagram shown in *Fig. 21*. As the input starts negative and goes positive, the output does not change until it reaches the positive trip point, V_{TRP}^{+}. At this point, the effective trip point is moved to V_{TRP}^{-}, which means that the comparator will not switch state again until the input voltages decreases below this new trip point.

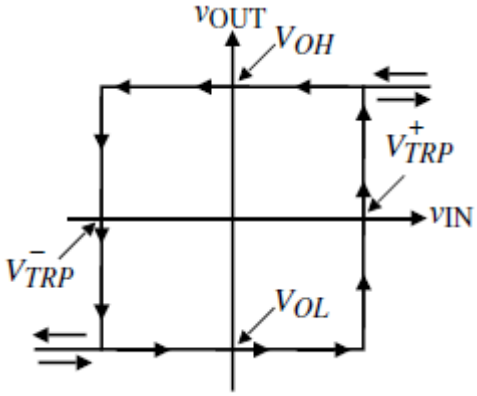

Fig. 21 Comparator transfer curve with hysteresis

The robustness of the hysteresis comparator is proved in *Fig. 22*, where glitches due to signal variations are eliminated.

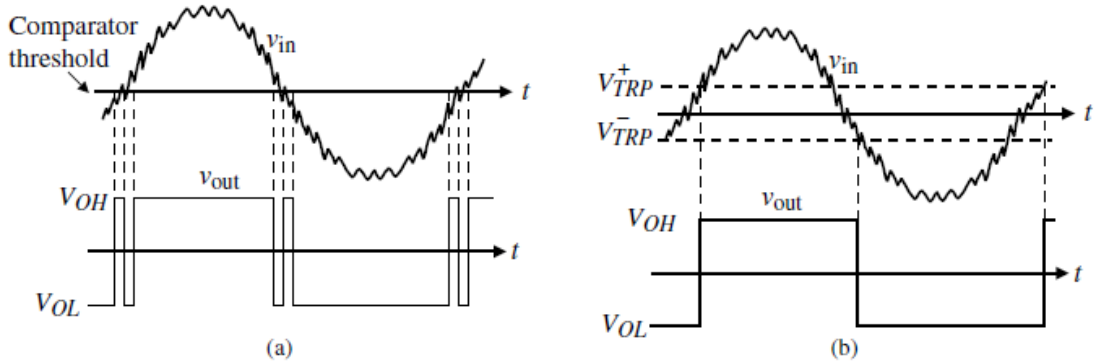

Fig. 22 (a) Comparator response with noisy input. (b) Comparator response to a noisy input when hysteresis is added

Hysteresis can be implemented using various methods in a comparator, but all of them make use of positive feedback. The positive feedback can be introduced externally or internally. For convenience, only internal feedback will be analysed, since it is the topology that is implemented in the circuit we are interested in.

Working principle: hysteresis comparator

Fig. 23 shows the architecture of a comparator using internal feedback, where there are two paths of feedback. The first one, is current series feedback through the common source node of transistors M1 and M2, which is a negative feedback path. The second one, is the voltage shunt feedback through the gate–drain connections of transistors M6 and M7, which is a positive feedback path.

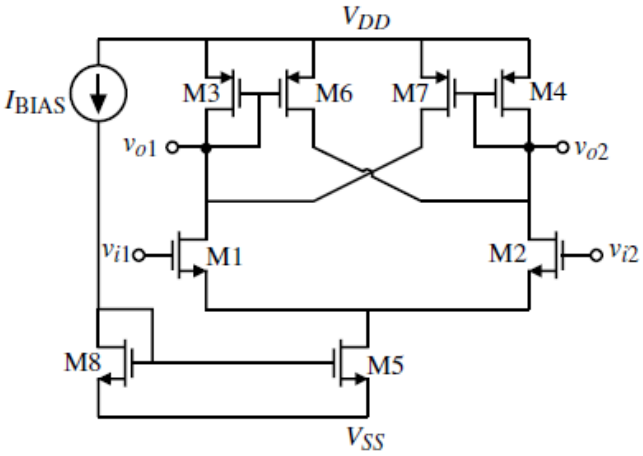

Fig. 23 Implementation of hysteresis using internal positive feedback in the input stage of a high-gain, open-loop amplifier

The positive feedback factor needs to be higher than the negative feedback factor in order to have hysteresis, which is achieved by making the ratio β_6/β_3 higher than one.

The following analysis shows the equations needed to associate the trip point values with transistor operating values and sizes.

Initially, we will assume that plus and minus supplies are used, and M1 is tied to ground and M2 has a variable voltage source. When the input of M2 is much less than zero, M1 is on and M2 is off. As M1 is on, M3 will also turn on. As M2 is off, there is no current flowing through M4, M7 neither M6. However, while M4 and M7 are off ($v_{gs} = 0$), M6 is actually on (v_{gs}~v_{th}). The reason why M6 is not giving current is because it is in deep ohmic region. Specifically, if $i_{d_2} = i_{d_4} + i_{d_6}$, $i_{d_6} = 0$ by force. The possibility is that M6 is in deep ohmic ($v_{ds_6} = 0$).

As a consequence, all of the tail current i_5 starts flowing from M1 and M3, so v_{02} is pulled high (remember $v_{gs_4} = 0, or\ v_{ds_6} = 0$). The resulting circuit is shown in *Fig. 24(a)*.

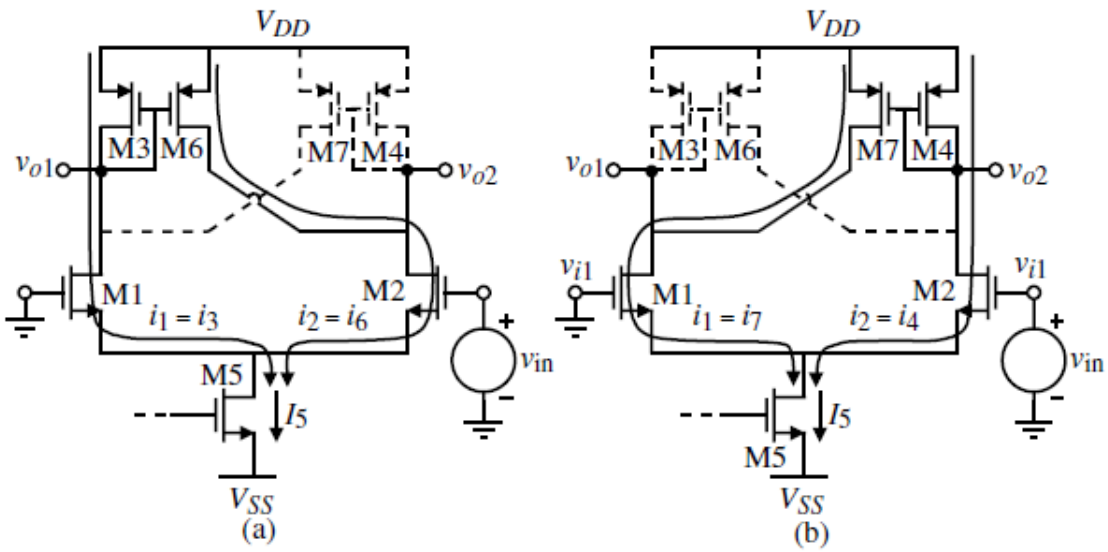

Fig. 24 (a) Comparator of Fig. 23 where v_{in} is very negative and increasing towards V_{TRP}^{+}.
(b) Comparator of Fig. 23 where v_{in} is very positive and decreasing towards V_{TRP}^{-}.

When v_{in} starts to increase, some current starts flowing through M6, and some drain-to-source voltage will appear in M6. At this point M6 is still in ohmic, but its v_{ds_6} will be increasing towards saturation region, following the behaviour of $I_D - V_{DS}$ curve. On the contrary, M4 will remain in deep subthreshold region until some charge starts accumulating in its gate. Indeed, v_{o2} starts decreasing slightly and the inflection point produces when M6 enters in saturation and copies the whole current of M3. Just beyond this point the comparator switches state.

To approximately calculate one of the trip points, the circuit must be analysed right at the point where i_2 equals i_6. Mathematically this is:

$$i_2 = i_6 = \frac{(W/L)_6}{(W/L)_3} i_3 = \frac{\beta_6}{\beta_3} \cdot i_3 = \frac{\beta_6}{\beta_3} \cdot i_1$$

$$i_{SS} = i_5 = i_1 + i_2 = \left(1 + \frac{\beta_6}{\beta_3}\right) \cdot i_1$$

This is, i_1 is lower than $\frac{i_{SS}}{2}$. If we take $\frac{\beta_6}{\beta_3} = 3$, $i_1 = \frac{i_{SS}}{4}$ and $i_2 = 3 \cdot \frac{i_{SS}}{4}$

Knowing the currents in both M1 and M2, it is easy to calculate their respective v_{GS} voltages. Since the gate of M1 is at ground, the difference in their gate–source voltages will yield the positive trip point as given below:

$$v_{GS1} = \left(\frac{2i_1}{\beta_1}\right)^{1/2} + V_{T1} \tag{1}$$

$$v_{GS2} = \left(\frac{2i_2}{\beta_2}\right)^{1/2} + V_{T2} \tag{2}$$

$$V_{TRP}^{+} = v_{GS2} - v_{GS1}$$

Once the trip point is reached, the comparator changes state: v_{0_1} changes from low to high and v_{o_2} changes from high to low. During this short interval of time, the current in M1 decreases dramatically until there is no gate-to-source voltage in M1 nor M3 neither in M6. M6, however, continues in saturation during this time so, the current through M2, which was $i_2 = i_6 + i_4$, turns to be $i_2 = i_4$.

Finally, when v_{in} starts decreasing towards the threshold value, M7 will start conducting the same way M6 did previously, until it reaches saturation, when the comparator will switch state again, returning to the initial point.

The equivalent circuit in this state is shown in *Fig. 24(b)*. To calculate the trip point, the following equations apply:

$$i_7 = \frac{(W/L)_7}{(W/L)_4}\, i_4$$

$$i_1 = i_7$$

$$i_5 = i_2 + i_1 \qquad (i_2 = i_4)$$

Therefore,

$$i_4 = \frac{i_5}{1 + [(W/L)_7/(W/L)_4]} = i_2$$

$$i_1 = i_5 - i_2$$

Using Eqs. (1) and (2) to calculate v_{GS}, the trip point is

$$V_{TRP}^{-} = v_{GS2} - v_{GS1}$$

Note these equations do not take into account the effect of channel length modulation.

The differential stage described thus far is generally not useful alone and thus requires an output stage to achieve reasonable voltage swings and output resistance. There are a number of ways to implement an output stage for this type of input stage. One of these is given in *Fig. 25*. Differential-to-single-ended conversion is accomplished at the output and thus provides a Class AB type of driving capability.

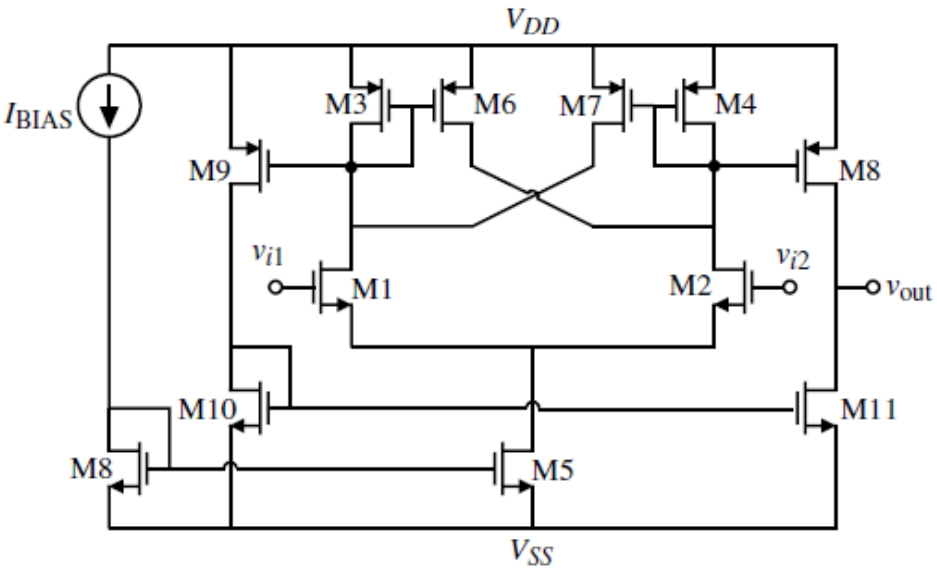

Fig. 25 Complete comparator with internal hysteresis including an output stage

Fig. 26 illustrates the comparator actually being used in chip

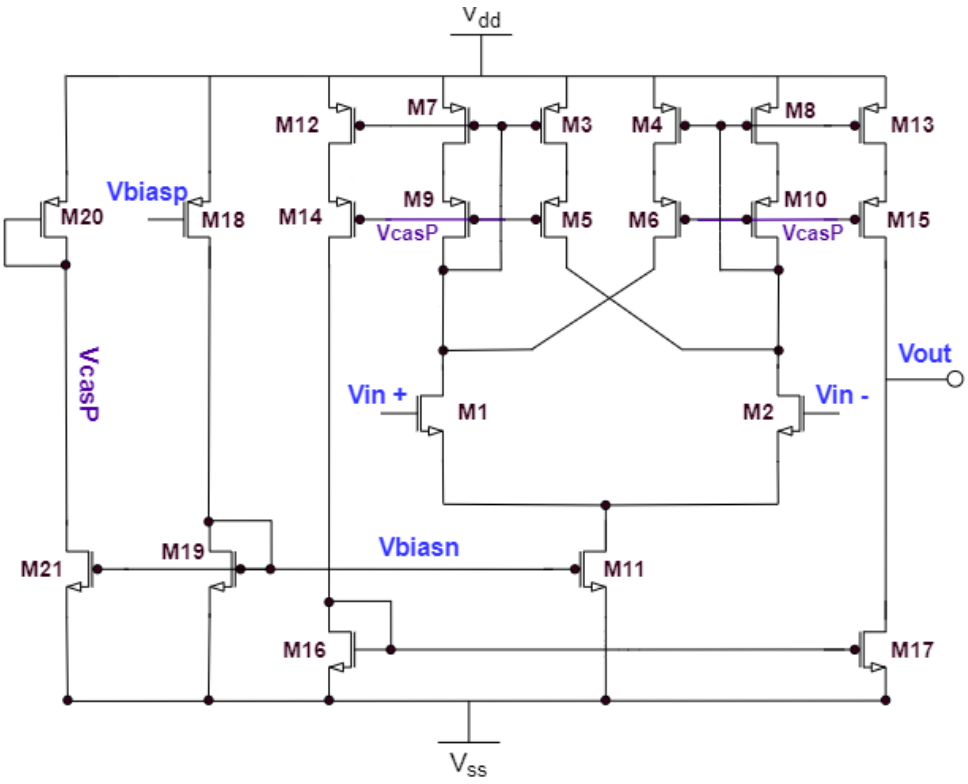

Fig. 26 Hysteresis comparator

Indeed, our circuit uses a similar architecture, with some differences. One of the main differences is that it uses pMOS cascode transistors (M5, M9 and M6, M10) in the positive feedback path. The currents flowing through the voltage-shunt feedback transistors are copied to the first stage output by means of low-voltage current mirror configuration, which minimises the voltage necessary to keep the transistors in saturation and make it suitable for low power applications. First output differential signals are copied to the second stage. Finally, M16 copies the current to M17 with another current mirror, so that both differential signals are summed.

The circuit is biased externally through M18 and the input current is copied to tail transistor M11. The input current is also copied to M21 so that diode connected transistor M20 generates the biasing voltage for the cascode transistors current mirrors.

2.4. Output NOR gate

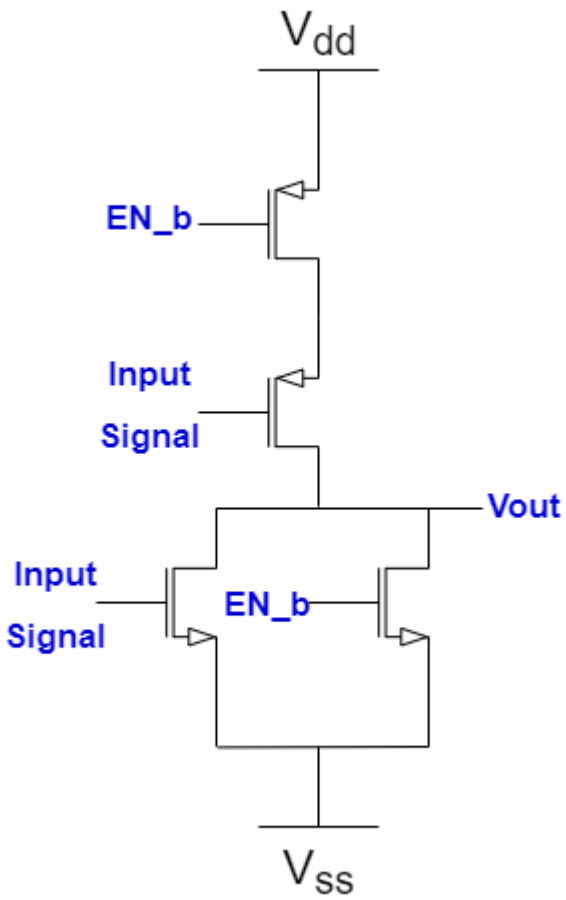

Fig. 27 NOR gate

The NOR gate is a well-known logic gate that does not require further explanation. In our specific case it acts as a buffer that can be controlled with an enable (EN) bit. If $EN = 1$, the output is off and if $EN = 0$ the buffer will follow the input signal value, which will be high or low.

The load it will attack is very little, since the gate is connected to the digital backend. However, the signal path will add a considerable capacitance. A suitable sizing of the transistors that take into account the path load is required.

2.5. Current DAC

As a complementary task, the design the current DAC is proposed. The current DAC consists of a digital-to-analogue converter that copies the current from a current reference. The digital-to-analogue converter gives an output current that corresponds to the bits selected externally. The generated current is copied through a current mirror and introduced in the comparator.

The digital-to-analogue converter is an IP block that has been already designed. It is a binary weighted 8 bit-DAC, which gives an output DC current of 1 μA.

The current mirror that copies the current is a low-voltage cascode current mirror, which is shown in *Fig. 28*. However, in this topology the cascode transistors are biased directly at the same voltage as the drain.

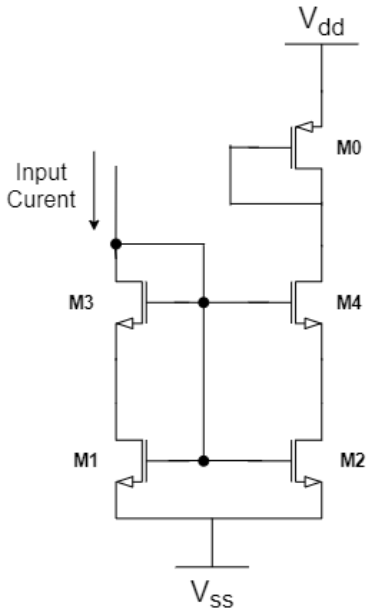

Fig. 28 Low voltage current mirror

One of the limitations of simple current mirrors are the nonidealities due to V_{DS} difference between M1 and M2. *Fig. 29* shows that $I - V_{DS}$ curve is not actually constant due to channel length modulation. So, differences in V_{DS} introduce variations in the current copy.

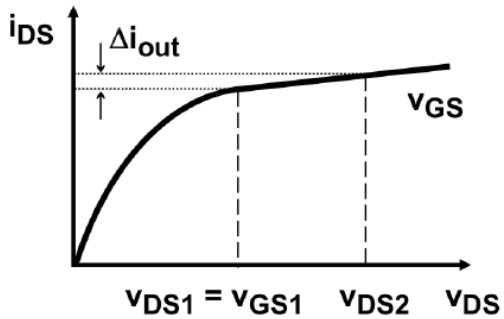

Fig. 29 Copy error due to V_{DS} difference (Figure taken from MND course)

The slope of the curve in saturation region is inversely dependent on the output resistance of the current mirror, i.e., the larger the output resistance the lower the slope will be and hence the copy error will be minimised. Therefore the cascode topology is introduced in the architecture.

Another requirement for current mirrors is that they need a minimum output voltage to operate. As we will see in next section, we will be operating in moderate inversion region, which makes it hard to calculate manually the operating points. Therefore, we will check the proper saturation of the current mirror in Section 4.2.

3. Methodology / project development

Following the discussion about the important aspects of the comparator, the comparator has been designed at transistor level. So, this section will be devoted to explaining the design procedure, and the followed criteria to choose the transistor dimensions. After this section, the rest of the chapter is dedicated to the simulations.

3.1. Transistor level design of the comparator

As we know, one of the most important challenges of this comparator is its low power consumption. As the power consumption is limited to 50 μW and power supply is 1.2 V, the total current consumption will be 41.6 μA.

The core block of the comparator is the hysteresis comparator, so it seems reasonable to provide more current to this block. The next most important block would be the R2R Amplifier and finally the 2nd stage FDA. For an initial approximation, around half of the available current will be allocated to the hysteresis block, and the rest will be shared with the rest of the amplifiers:

$$I_{stg3} = 20\ \mu A$$

$$I_{stg2} = 8\ \mu A$$

$$I_{stg1} = 12\ \mu A$$

As the procedure to choose the transistor dimension, a current density sweep will be done, which is equivalent to analyse the transistor through the inversion regions. Concretely, a testbench will be generated where gate and drain voltages will be fixed. A DC current source will act as biasing current of the transistor. As we sweep this current value the source voltage will adapt to the current, and therefore we can extract the gate-to-source and drain-to-source voltages (and of course ensure the saturation of all transistors). These voltages will vary with transistor width and length. *Fig. 30* shows the testbench for the nMOS transistor characterization. The gate and drain voltages have been fixed to 1.2 V, and the width and length are variable. Also, an equivalent testbench is made for a pMOS transistor.

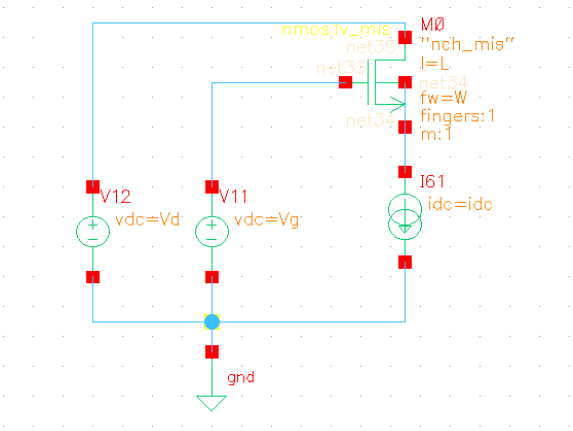

Fig. 30 transistor characterization testbench

The first decision is to choose the region of inversion in which the transistor will operate. Plotting $\frac{g_m}{I_d}$ for a wide bias current range, we can distinguish these regions of inversion.

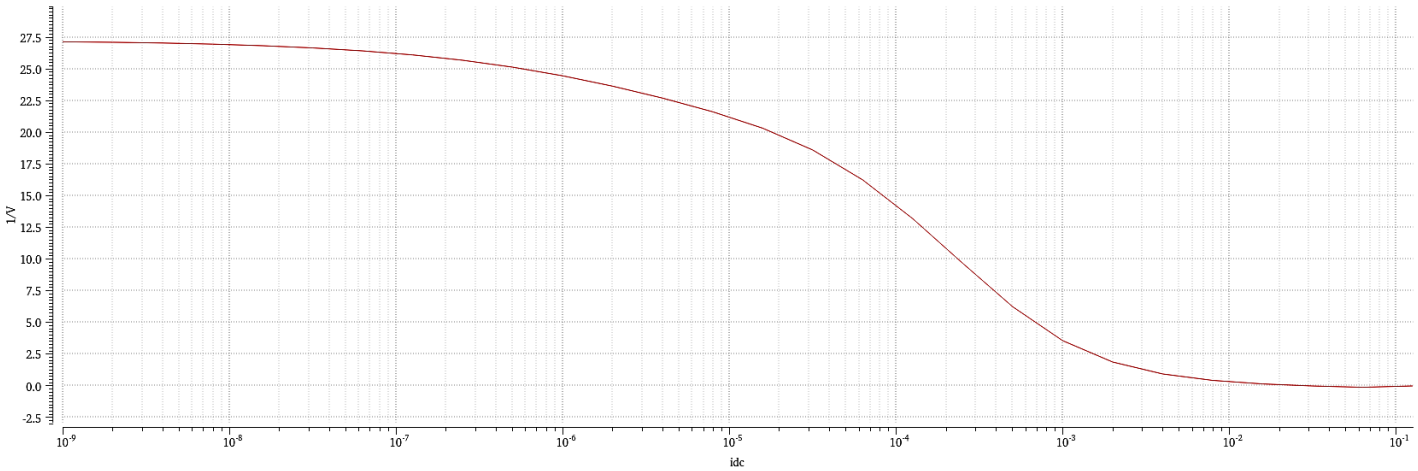

Fig. 31 $\frac{g_m}{I_d}$ characteristic, from 1 nA to 10 mA

The weak inversion is the region where $\frac{g_m}{I_d}$ is constant, strong inversion region is where $\frac{g_m}{I_d}$ is minimum and the moderate inversion is the transitioning region. Clearly, the circuits in the comparator will operate in moderate inversion ($\sim 40\ \mu A$).

The election of channel length is critical as well. In general, long channels are preferred where large impedances are needed, e.g. current mirrors. Short channels are more suitable if we care for switching speeds and low power designs. So, as a rule of thumb, the tail transistors will be long channel and the transistors where the signal travels will be short channel.

The width is also important: normally a bigger transistor has bigger transconductance, but it may switch slower as it includes more parasites.

For an initial design, the input DC voltages will be assumed at 0.6 $V$and the master current will be a current mirror with a large channel transistor for a good copy $\left(\frac{W}{L}\right)_{mirror} = \frac{2\ \mu m}{2\ \mu m}$.

The stages will be designed in order, so that the output voltages coincide with the following input voltages.

As the total current for the first stage is set to 12 μA, and we are designing for 0.6 V common mode, each tail transistor will drive 6 μA. Later, in simulations this ratio will probably be modified since we are interested in $1\,V$ common mode. However, for an initial approximation we will set $\left(\frac{W}{L}\right)_{M9} = \frac{12\ \mu m}{2\ \mu m}$ and $\left(\frac{W}{L}\right)_{M10} = \frac{12\ \mu m}{2\ \mu m}$.

Looking into I-V curves in *Fig. 32* and *Fig. 32*, we can look which is the needed V_{GS} and V_{DS} voltages to drive 12 μA: $V_{GS} = 400\ mV$, $V_{DS} = 400\ mV$, $V_{DS_{sat}} = 142\ mV$ in case of pMOS. $V_{GS} = 320\ mV$, $V_{DS} = 320\ mV$, $V_{DS_{sat}} = 80\ mV$ in case of nMOS.

Each differential pair should drive 3 μA and the transistors are sized according to this requirement. Besides, it is very convenient to maximise the transconductance, because the voltage gain depends directly on g_m. Finally, the transistor sizes are important, a big width will guarantee good g_m but will include many parasites as well. The length will be minimum since we want a fast comparator. Taking this into account $W_{M1} = 6\ \mu m$ seems a reasonable compromise, with $g_{m,M1} = 70\ {}^{\mu A}/_{V}$. $V_{GS} = 300\ mV$ and $V_{DS} = 300\ mV$, there is room for the differential pair polarization. For pMOS differential pair we can operate in a similar way. $g_{m,M3} = 60\ {}^{\mu A}/_{V}$

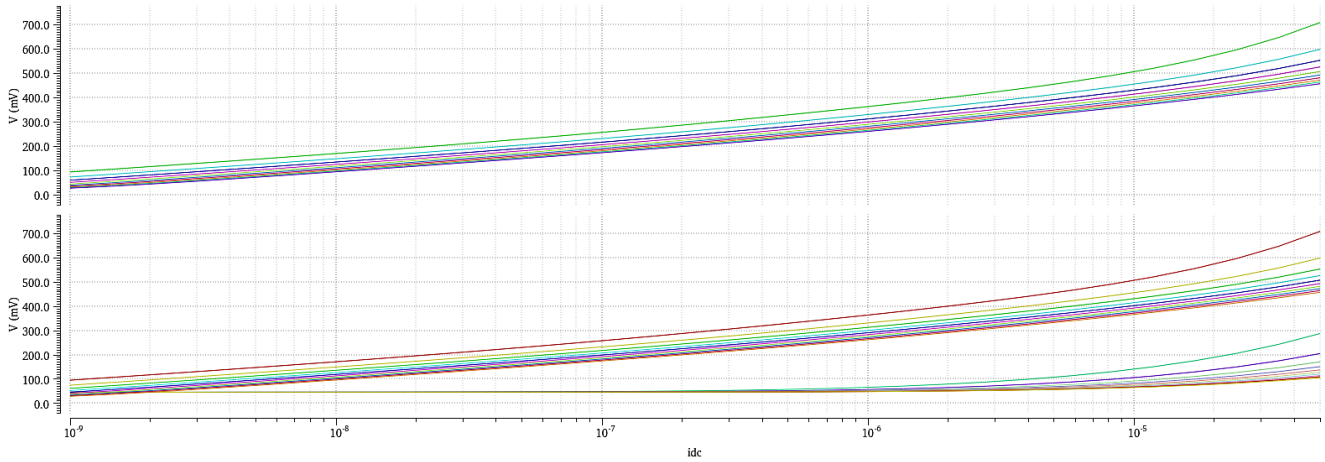

Fig. 32 V_{GS} and V_{DS} voltages for different transistor sizes

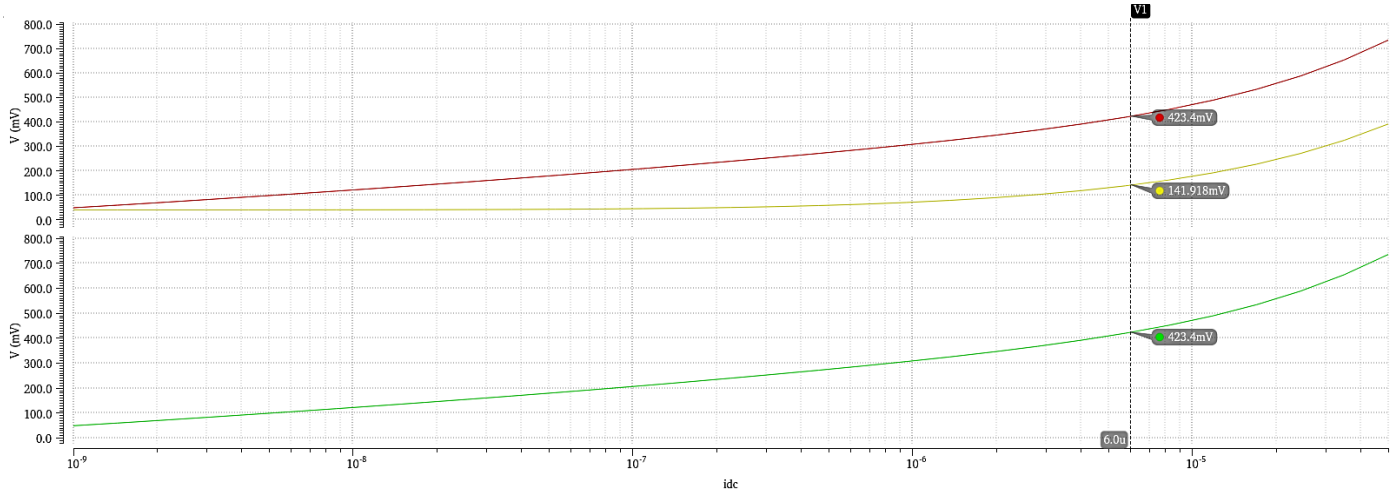

Fig. 33 parameter values for 24 μm width pMOS

The other parameter that determines the gain is the output impedance of the amplifier, which is dominated by R_D. This should be a rather big resistance, but taking into account that too big transistors ($> 50\ k\Omega$) may introduce distortion in the layout.

The mirror transistors will be designed with the same sizes as the differential pairs, with the risk that they can have an important V_{DS} mismatch, and hence a poor current copy. This voltage drop can be controlled with the resistor value. The resistor value will be quite large in order to compensate the small transconductance.

Finally, the pMOS diode will drive the whole 12 μA and will limit the voltage excursion at the output. A drain-to-source voltage drop around 330 mV will be chosen, so that the output does not reach the top rail. The initially chosen values will be the following:

$$\left(\frac{W}{L}\right)_{M1} = \left(\frac{W}{L}\right)_{M2} = \frac{6\ \mu m}{130\ nm}$$

$$\left(\frac{W}{L}\right)_{M3} = \left(\frac{W}{L}\right)_{M4} = \frac{6\ \mu m}{130\ nm}$$

$$\left(\frac{W}{L}\right)_{M5} = \left(\frac{W}{L}\right)_{M6} = \left(\frac{W}{L}\right)_{M7} = \left(\frac{W}{L}\right)_{M8} = \frac{6\ \mu m}{130\ nm}$$

$$\left(\frac{W}{L}\right)_{M9} = \left(\frac{W}{L}\right)_{M10} = \frac{12\ \mu m}{2\ \mu m}$$

$$\left(\frac{W}{L}\right)_{M11} = \frac{10\ \mu m}{130\ nm}$$

$$R_D = 40\ k\Omega$$

Fig. 34 shows the 1st stage circuit with approximate DC node voltages.

As studied in Section 2.1 the voltage gain is $g_m R_D$. The overall transconductance is the sum of $g_{m,M1} + g_{m,M3} = g_m = 130\ {}^{\mu A}/_{V}$. The expected gain is $A_v = 5.2$ (14.3 dB)

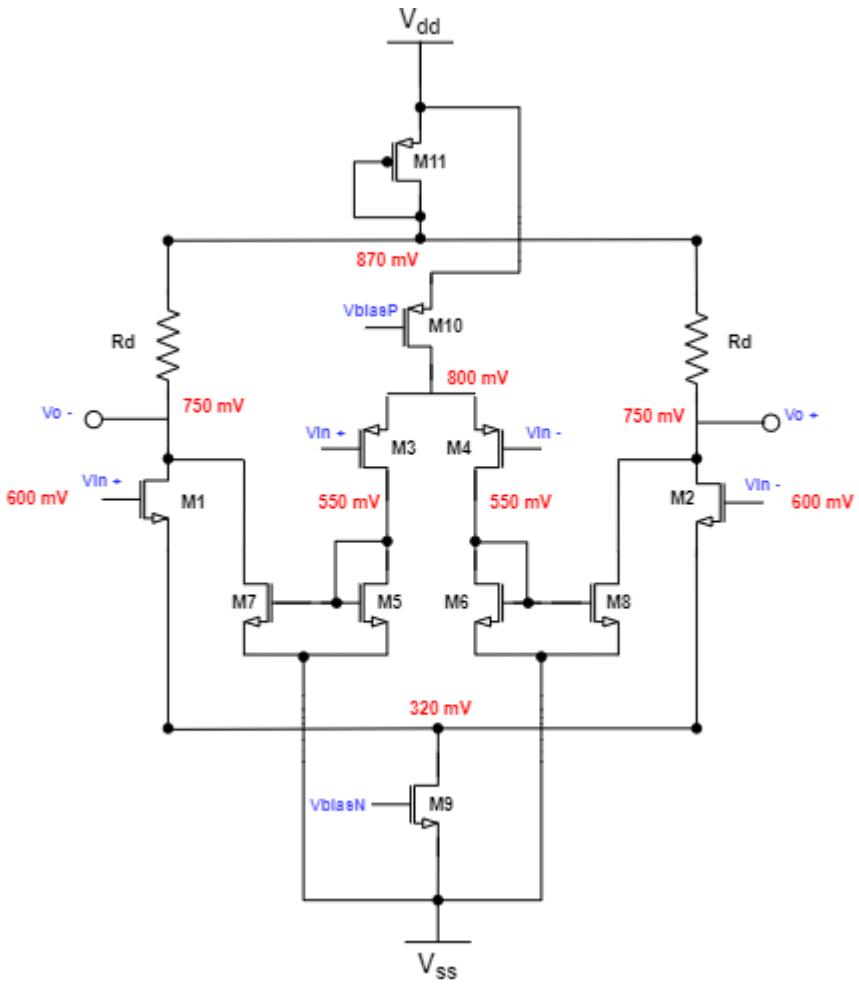

Fig. 34 1st stage design

For the design of the second stage, we will follow the same considerations. The current that will drive the 2nd FDA is 8 μA, which requires $W_{M3} = 16\ \mu m$ and $L_{M3} = 2\ \mu m$. As we want a good transconductance with little parasitics, we choose $W_{M1} = 5\ \mu m$ with $g_{M1} = 90\ {}^{\mu A}/_{V}$. The diode connected transistor is designed using the same criteria. Finally, the resistance will be maximised to provide proper gain. The chosen dimensions are:

$$\left(\frac{W}{L}\right)_{M1} = \left(\frac{W}{L}\right)_{M2} = \frac{5\ \mu m}{130\ nm}$$

$$\left(\frac{W}{L}\right)_{M3} = \frac{16\ \mu m}{2\ \mu m}$$

$$\left(\frac{W}{L}\right)_{M4} = \frac{10\ \mu m}{130\ nm}$$

R_D = 50 kΩ

Fig. 35 shows the 2nd stage circuit with approximate DC node voltages.

The expected gain is $A_v = 4.5\ (13\ dB)$

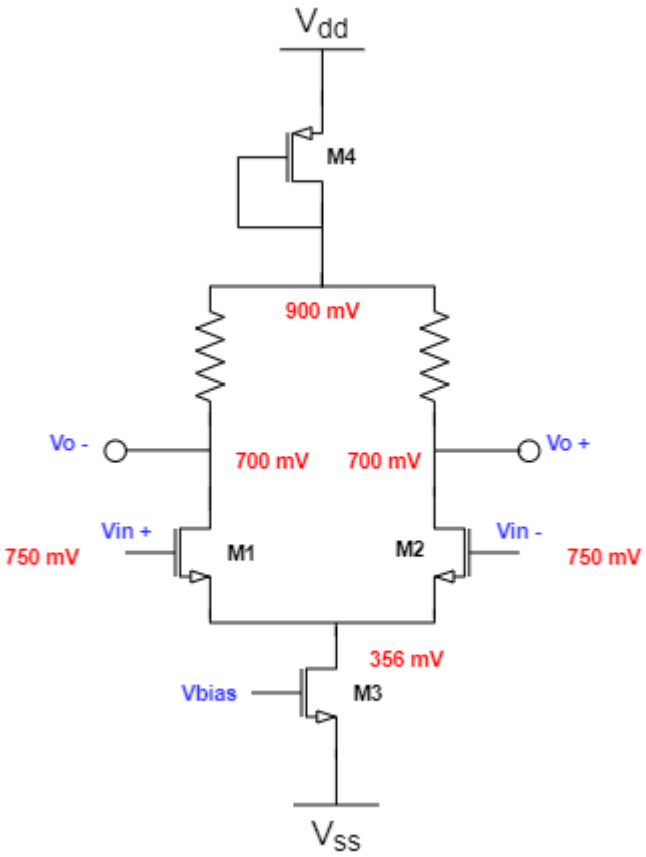

Fig. 35 2nd stage design

Following the 2nd stage, the hysteresis block is designed.

M18 will copy the current from the current reference and M19 replicates this current into the tail transistor. Also, the current will be replicated in M21, so that M20 can generate the necessary voltage to bias the cascodes in the current mirror. M18 and M19 will be identical to the mirror transistor in the master. M21 will also be the same size, as it is copying the current from the adjacent branch: $\left(\frac{W}{L}\right)_{M18} = \left(\frac{W}{L}\right)_{M19} = \left(\frac{W}{L}\right)_{M21} = \frac{2\ \mu m}{2\ \mu m}$.

The tail transistor needs to drive 20 μA current, but output branches need to be taken into account as well. However, only one output branch will drive current each time the comparator switches state. Hence, the tail current will be allocated 10 μA. $W_{M11} = 20\ \mu m$ and $L_{M11} = 2\ \mu m$. The biasing branches would consume 1 μA each but we will omit it.

The differential pair will provide the transconductance of the circuit. Again, only one of the pairs will drive the total tail current (the same way as the outputs). Considering the input capacitance of the pairs needs to be minimised: $W_{M1} = 6\ \mu m$ and $L_{M1} = 130\ nm$ with $g_m = 216\ {}^{\mu A}/_{V}$.

The voltage drop in the current mirrors that implement the positive feedback is around $500\ mV$. Assuming the drain-to-source voltage will be equally divided and they can not be too large because the speed of the comparator depends on how fast M3 and M5 enter in saturation, we choose $W_{M7} = W_{M9} = 5\ \mu m$. Although they act like current mirrors, the speed is more important than an exact current copy. Hence, short transistor is used. $V_{GS,M9}$ is around $350\ mV$, which means $V_{casp} \approx 600\ mV$. Hence, we choose $W_{M20} = 1\ \mu m$ and $L_{M20} = 2\ \mu m$, so that it has the required V_{DS} drop. Also, to provide hysteresis, β_3 and β_5 need to be higher than β_7 and β_9, so as an initial value, we will double the widths and then calculate the resulting hysteresis with simulations. For a good current copy, M16 and M17 will be long channel.

The rest of the rest of the calculations are straightforward. In summary, the transistor sizes are the following ones. *Fig. 36* shows the DC node voltages at the block.

$$\left(\frac{W}{L}\right)_{M1} = \left(\frac{W}{L}\right)_{M2} = \frac{6\ \mu m}{130\ nm}$$

$$\left(\frac{W}{L}\right)_{M3} = \left(\frac{W}{L}\right)_{M4} = \left(\frac{W}{L}\right)_{M5} = \left(\frac{W}{L}\right)_{M6} = \frac{10\ \mu m}{130\ nm}$$

$$\left(\frac{W}{L}\right)_{M7} = \left(\frac{W}{L}\right)_{M8} = \left(\frac{W}{L}\right)_{M9} = \left(\frac{W}{L}\right)_{M10} = \left(\frac{W}{L}\right)_{M12} = \left(\frac{W}{L}\right)_{M13} = \left(\frac{W}{L}\right)_{M14} = \left(\frac{W}{L}\right)_{M15} = \frac{5\ \mu m}{130\ nm}$$

$$\left(\frac{W}{L}\right)_{M16} = \left(\frac{W}{L}\right)_{M17} = \frac{5\ \mu m}{2\ \mu m}$$

$$\left(\frac{W}{L}\right)_{M18} = \left(\frac{W}{L}\right)_{M19} = \left(\frac{W}{L}\right)_{M21} = \frac{2\ \mu m}{2\ \mu m}$$

$$\left(\frac{W}{L}\right)_{M20} = \frac{1\ \mu m}{2\ \mu m}$$

$$\left(\frac{W}{L}\right)_{M11} = \frac{20\ \mu m}{2\ \mu m}$$

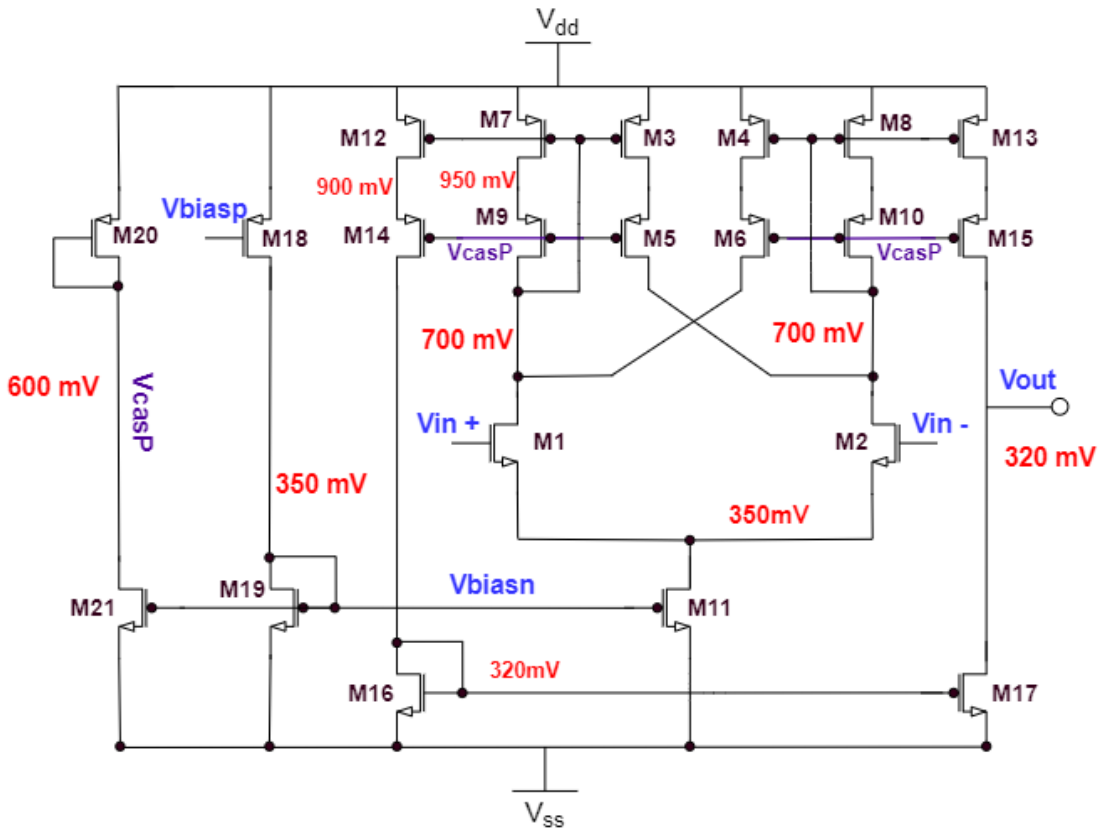

Fig. 36 Hysteresis block design

As many transistors are quite big, they have been resized using fingers and multipliers.

Finally, the NOR gate is designed. This logic gate will act as a buffer and will regenerate the output of hysteresis block. As an initial attempt nMOS width of 1 μm and pMOS width of 3 μm is chosen. The pMOS is made wider to compensate the fact that holes have less mobility than electrons. The length will be minimum.

3.2. Transistor level design of the current DAC

In this section, an initial calculation of the transistor sizes has been done, in the same fashion as in previous section.

M0 is the original transistor that biases the pMOS branches of the comparator. Its dimensions are well known, $\left(\frac{W}{L}\right)_{M0} = \frac{2\ \mu m}{2\ \mu m}$. The cascode transistors (M3 and M4) can be made in minimum length because their role is to increase the output impedance of the current mirror. On the contrary, M1 and M2 need to have long channels to ensure a good transistor copy. The widths will be chosen considering the driving current and voltage drop the transistors need to operate. So, the transistor sizes are proposed in the same fashion as we did in the previous section. *Fig. 37* shows the estimated DC node voltages.

$$\left(\frac{W}{L}\right)_{M0} = \frac{2\ \mu m}{2\ \mu m}$$

$$\left(\frac{W}{L}\right)_{M1} = \left(\frac{W}{L}\right)_{M2} = \frac{5\ \mu m}{2\ \mu m}$$

$$\left(\frac{W}{L}\right)_{M3} = \left(\frac{W}{L}\right)_{M4} = \frac{4\ \mu m}{130\ nm}$$

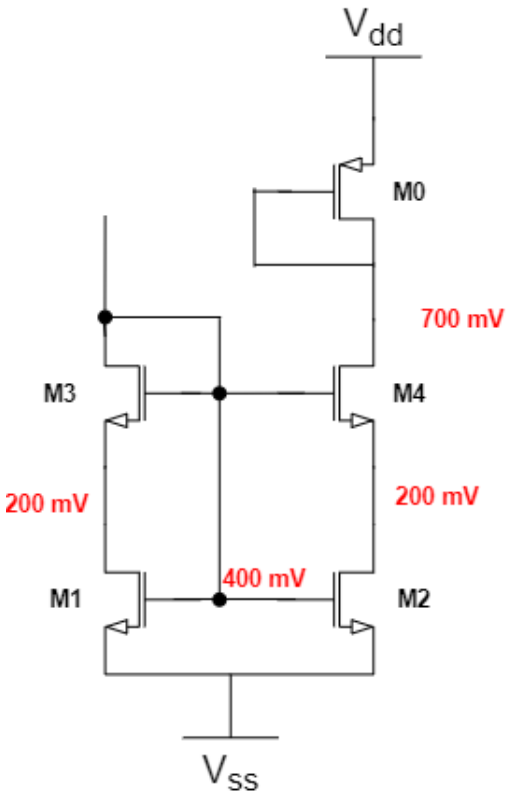

Fig. 37 DC node voltages current mirror

After an initial calculation, the next step has been to simulate the comparator and make changes with respect to the calculated values. For the development of the design, Cadence software has been used. This is a reference Electronic Design Automation (EDA) tool for professional VLSI designers (there are others like Synopsys, Magma and Mentor Graphics). In our case, we are using Cadence Virtuoso Analog Design Environment, which is a specific framework for full custom analogue design. It includes schematic entry, electrical simulations using Spectre, layout design and parasitic extraction.

Initially, the comparator is designed and tested with ideal input signals. Later, the comparator has been integrated in the system in order to test it with a realistic model of the input signal [3]. Next, the layout of the comparator is designed, and finally, compared the initial results with the extraction.

3.3. Analysis compared with ideal signal

For the first steps in the design, three main analysis have been used: transient signal analysis, DC analysis and AC analysis. The transistor level design has been done to accomplish some initial approximated specs. The most important ones are the delay, hysteresis amplitude, the power consumption and the gain.

3.3.1. Transient analysis

For simulation, both inputs are fed with the same common mode signal, and a differential signal is introduced in the positive terminal. This differential signal is generated out of an ideal pulse generator which gives a rectangular pulse with variable amplitude, pulse width, period and rising/falling times. In other words, the incoming signal is introduced in the positive input and the reference signal or the threshold is introduced in the negative terminal. The output is loaded by a $50\,fF$ capacitor. As for all the following tests, the comparator is biased with an ideal current mirror initially, but as the project developed a current DAC replaces the ideal current mirror. The objective has been to test the comparator in the most realistic conditions.

The comparator is tested sweeping all common modes from 0 to VDD with a step of 100 mV. The outputs are configured to see input and output signals of each stage and measure the delay, the rising and falling times, the DC power dissipation, current flowing through relevant nodes and transistor operating points. *Fig. 38* shows the used testbench.

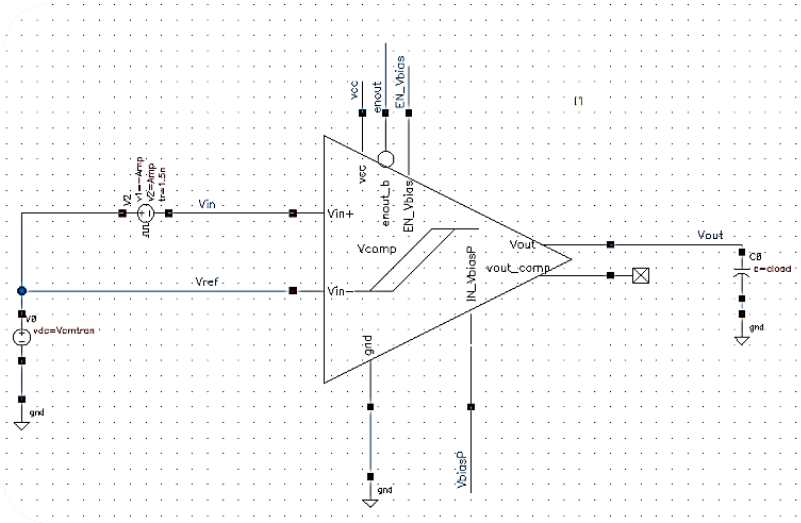

Fig. 38 Transient analysis testbench

Delay measurement has been done by calculating the difference between the time when reference level cuts the input signal and the comparator output signal reaches half power supply voltage level. *Fig. 39* illustrates it graphically.

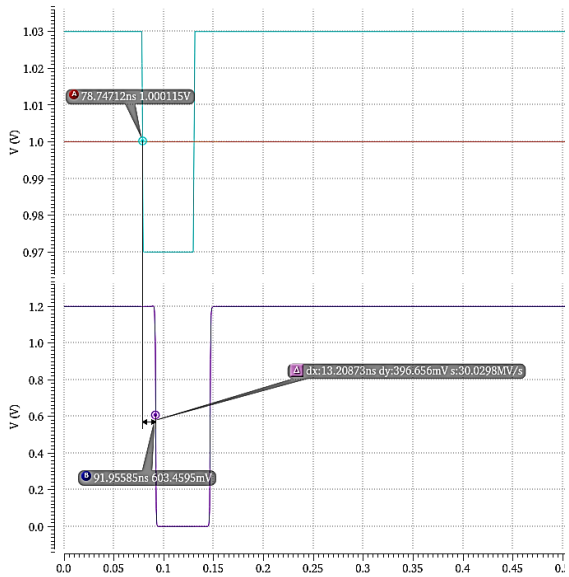

Fig. 39 Delay measurement illustrated graphically

Rising and falling times are calculated as the time takes the signal to go from 10% VDD to 90% VDD, and vice versa.

3.3.2. DC analysis

For this analysis, *Vin* design variable is chosen, which represents the amplitude of the differential signal introduced in the positive input of the comparator, as made in transient analysis. The amplitude is swept from $-300\ mV$ to $300\ mV$ with a step size of $250\ \mu V$.

The DC operating points are saved, to see directly in the screen all transistors are in proper saturation. Finally, the hysteresis sweep is enabled as we are interested in measuring the internal hysteresis loop.

Similar to the previous testbench, the comparator is fed with a common mode DC signal where we introduce a differential signal in the positive terminal. *Fig. 40* shows the used testbench.

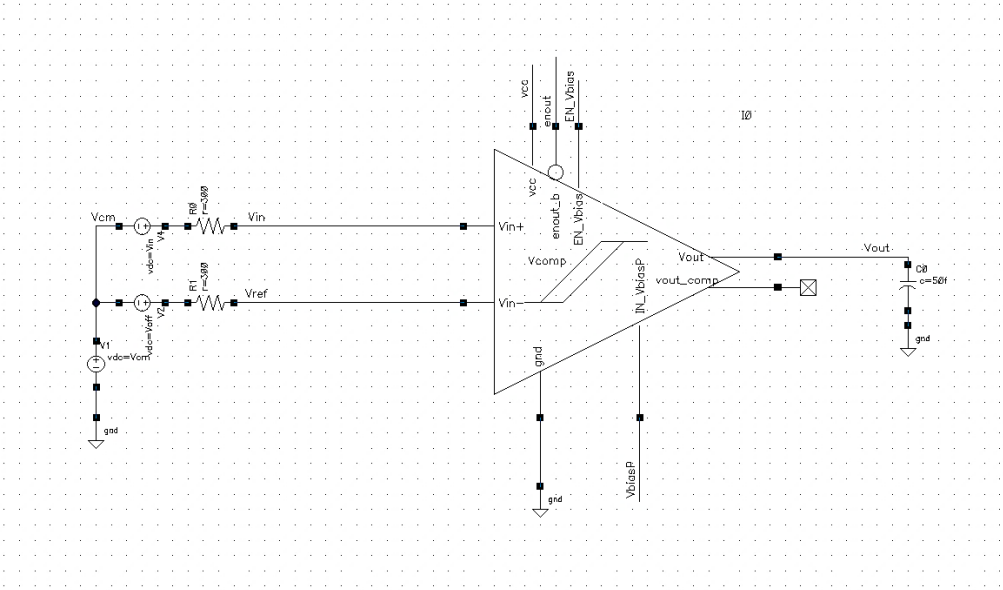

Fig. 40 DC analysis testbench

Power consumption is calculated simply by multiplying the all the DC current flowing through the comparator and the power supply voltage level.

Input-referred offset is an important figure of merit of differential amplifiers. This is a shift in the X-axis of the amplifier transfer curve, because of the mismatch in the current flowing through the differential pair. DC analysis will make an initial calculation of the offset across the stages. However, these results will not be meaningful since the mismatch on transistor and other circuit components varies statistically. So, offset will be studied when we analyse the mismatch with Monte Carlo simulations in Section 3.3.4.

The hysteresis amplitude is calculated as the difference between the rising and falling edges when they reach half of V_{DD}, as the *Fig. 41* shows.

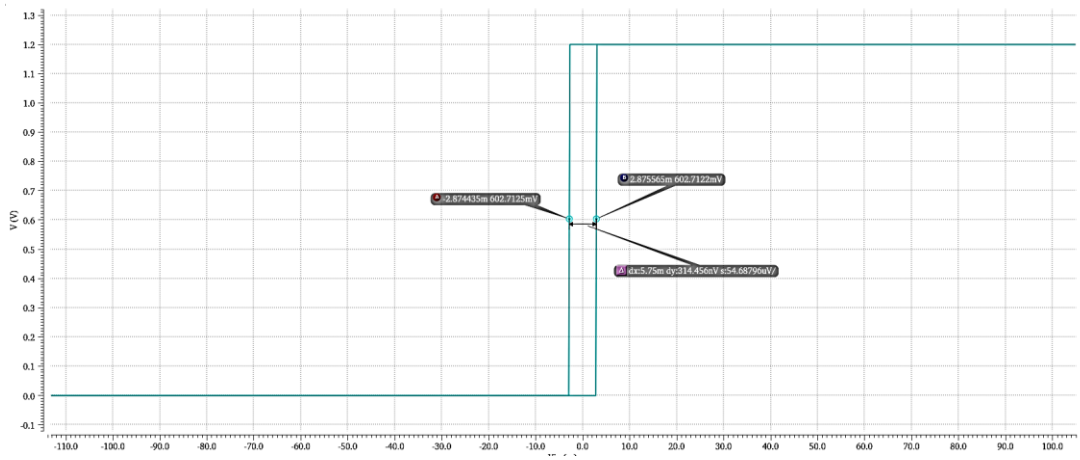

Fig. 41 Hysteresis at comparator output

In parallel with simulations, DC operating points are constantly being checked. The operating points have been checked directly in the circuit, as *Fig. 42* shows, as well as in the ADEXL testbench (this last one specially to ensure proper saturation of all transistors). As an extension to this, and to ensure the circuits are robust against process, time and power variations, special attention will be paid to the DC operating points in Section 3.3.4.

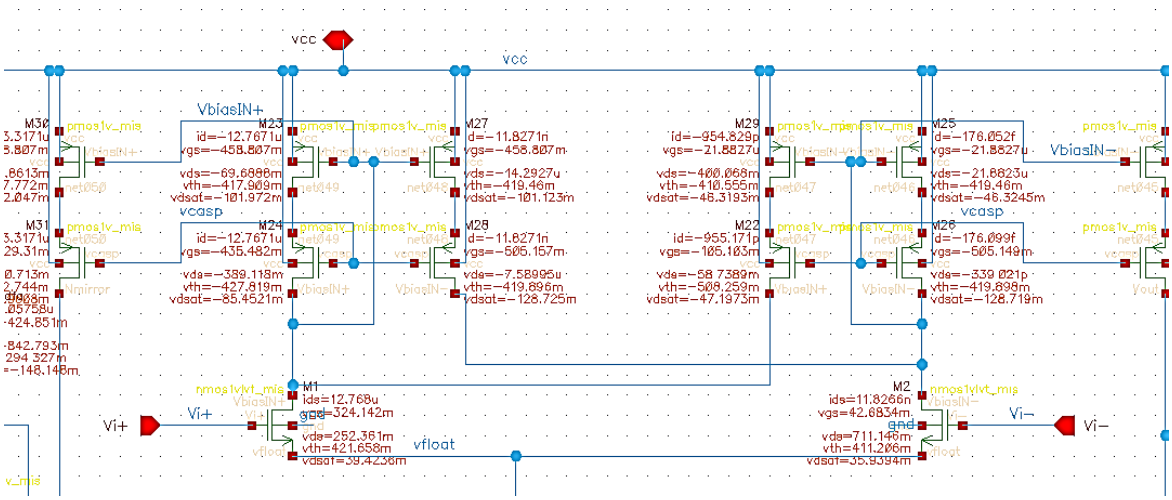

Fig. 42 Operating points in the hysteresis comparator block

3.3.3. AC analysis

The comparator is configured in negative RC feedback loop in the testbench. This trick is used to characterise the comparator. We want to measure the voltgae gain with two equal inputs, because small deviations at the input would produce miscalculation of the operating points. Thus, the feedback loop is used to stabilise the circuit.

The positive differential input is fed by a variable DC common mode voltage, and an AC signal of 1 V is added. The measured magnitudes are the gain and the bandwidth. *Fig. 43* shows the used testbench.

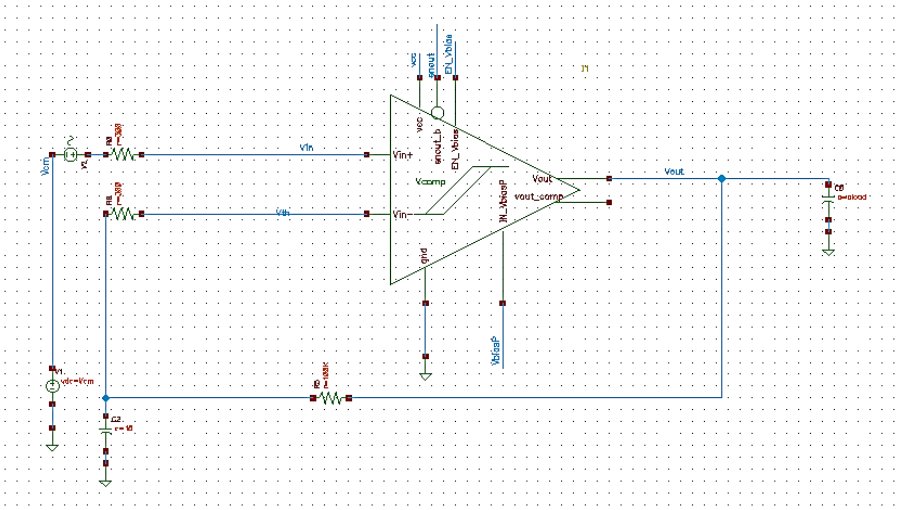

Fig. 43 AC testbench configuration

3.3.4. Process and Mismatch

The transistors are sensitive to variations in the manufacturing process since it is a physical process and hence not free of errors. These manufacturing failures may lead to a performance decrease or important faults in chips. Therefore, it is necessary to simulate the components of the chip in various conditions of voltage supply, temperature and process variations.

The process variations refer to the variations of transistor components from their nominal value, such as the channel length, threshold voltage and oxide thickness, that make the transistor faster or slower. Apart from that, there are environmental variations that could change the chip's partial behaviour. These are voltage and temperature variations.

There are two ways of testing the variations: corners and Monte Carlo simulations.

Corner analysis simulates the chip in extreme conditions, this is, using a configuration of lowest/highest process variation values is unlikely to happen. It is a worst-case analysis. The advantage of process corners is that the manufactured circuits under all possible consideration, but it overdesigns the circuit. In *Fig. 44* image the process corners are sketched.

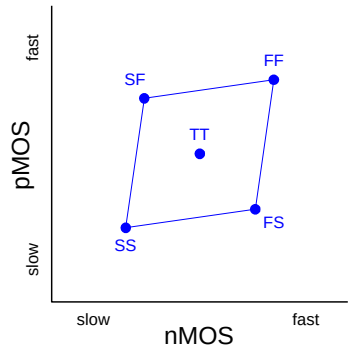

Fig. 44 Process corners

On the other hand, Monte Carlo simulations are based on statistical distributions. It randomly simulates every parameter according to a statistical distribution model on each run. This is a more realistic analysis and shows the region the circuit will work most of the time with the corresponding yield. The drawback of Monte Carlo is the large number of simulations required to have acceptable results. *Fig. 45* shows an example of probability distribution of a transistor channel length.

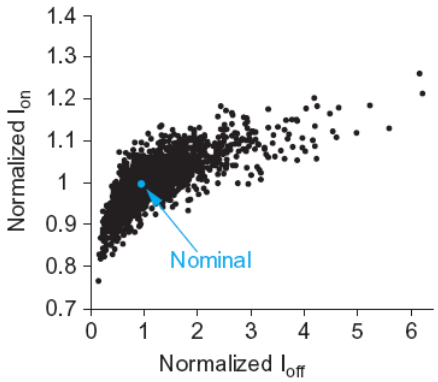

Fig. 45 Monte Carlo simulation example

In this technology, the manufacturer does not provide the means to perform the process analysis through Monte Carlo Simulation, so process variations are simulated with corners. These process variations are also cross checked with temperature and power supply variations:

- Process variations: SS SF TT FS FF
- Temperature: -20 ºC, 0 ºC, 20 ºC and 50 ºC
- Power supply: 1.1 V, 1.2 V and 1.3 V (10% of variation)
- Common mode voltage: $0 - 1.2\ V$

This is accomplished with the help of a model file which the manufactures supplies. With corners, comparator specs have been also checked to see how much the results diverge from nominal.

Monte Carlo simulations have been used to measure mismatch effects on the comparator specs. The sampling method used is the Latin Hypercube and the number of points 100.

Besides, as already said in Section 3.3.2 the DC operating points have been cross checked using corners. Once the circuit is properly working, a fine tuning of transistor dimensions

is necessary to ensure they operate in saturation region when varying the process, voltage and temperatures.

It is worth mentioning the design of the low voltage cascode current mirrors above the differential pair in the hysteresis block, which is sketched in *Fig. 46*. The current mirror is a particularly susceptible subcircuit because the hysteresis amplitude, the gain and delay partially depend on its configuration.

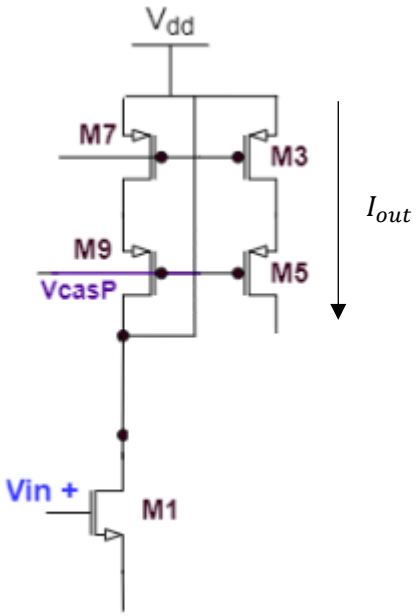

Fig. 46 Tuning DC operating points of the wide swing current mirror

It has been observed that M7 and M9 change from saturation to linear in some PVT corners, so the last part of the schematic design has been dedicated to play with the cascode voltage, transistor aspect ratio and the current flowing through the current mirror. The differential pairs have been re-dimensioned and the tail current has been slightly increased. In the end, a satisfactory voltage drop has been accomplished, which guarantees an proper drain-to-source voltages for all transistors. The corners that were particularly sensitive were the FF at 50ºC and SS at -20ºC, where the cascode (M9) and mirror (M7) transistors entered in ohmic region, respectively. It has been particularly useful the paper "Dynamic range of low-voltage cascode current mirrors" from E. Bruun and P. Shah on IEEE [6].

3.4. Analysis in real signal

This section is dedicated to analyse the noise performance of the comparator. The comparator is tested with the SiPM model and the preamplifier, in order to simulate in realistic conditions.

As showed in the *Fig. 47*, a preamplifier is introduced before the comparator. The preamplifier is the preceded by the SiPM. A RC-ladder is placed convert the input current pulse into voltage.

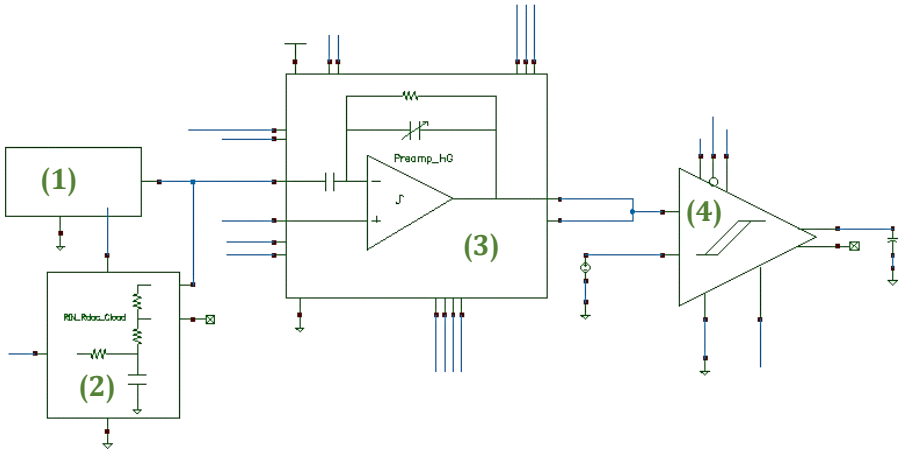

Fig. 47 (1) SiPM (2) RC ladder (3) HG Preamplifier (4) Hysteresis comparator

To simulate the noise, pseudo randomly generated oscillations are introduced on top of the signal, for each iteration. For this design, it is assumed that 100 iterations give a result which is accurate enough.

The SiPM generated pulse looks like an exponential pulse. After the amplification, the preamplifier inverts the signal. Input signals with different photon number are shown in *Fig. 48*.

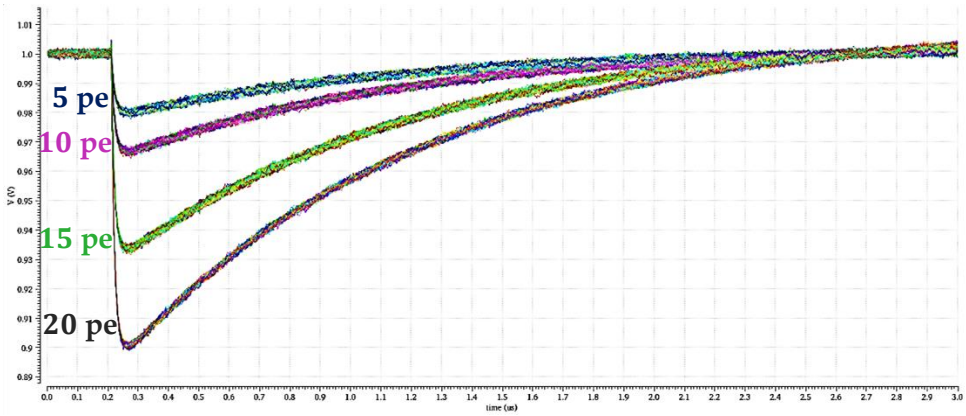

Fig. 48 Comparator input signals

Fig. 49 and *Fig. 50* show the operation of the comparator and the input and output signals and the different switching time, respectively. Each iteration, the input signal will cut the threshold in a different moment, so we will collect one delay value per iteration

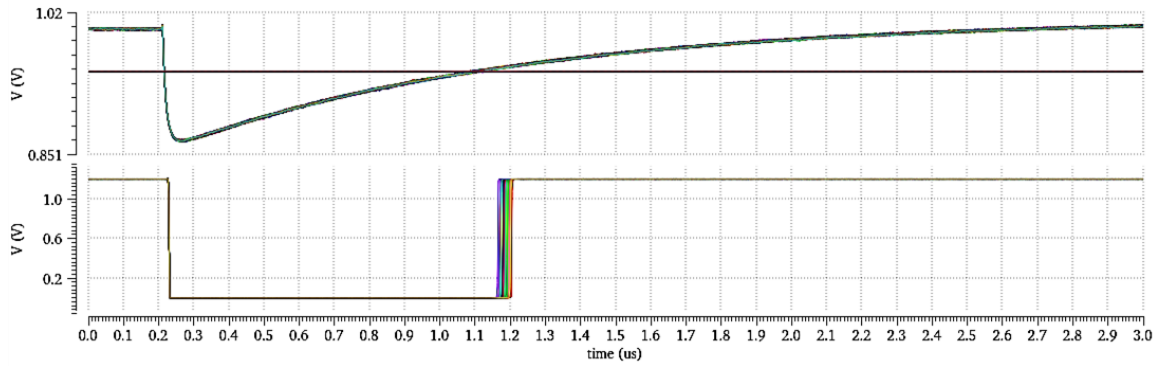

Fig. 49 Input and output of the comparator

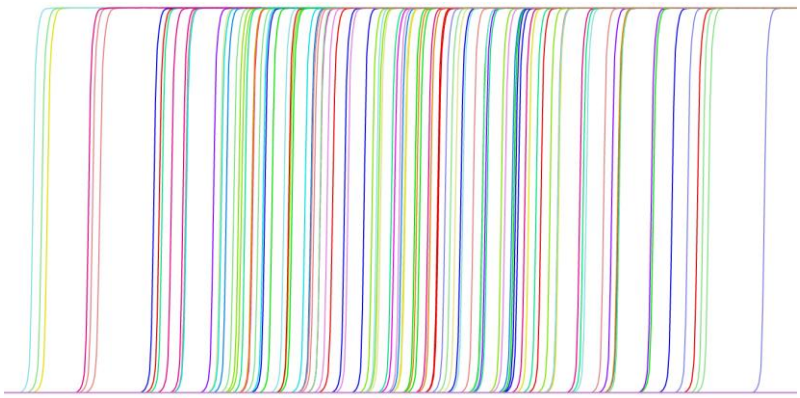

Fig. 50 Comparator switches in different moments each iteration

To analyse the effect of the noise at the comparator we will measure the delay and jitter.

The nominal value of the delay is calculated with the root mean square of all the delays.

The standard deviation of the delay is known as *jitter*. By definition, jitter is the time variation of the delay with respect to its nominal value.

Fig. 49 shows the delay variation more visually along 100 pseudorandom noise iterations, for 1 to 30 events. It can be observed that the delay decreases as more photons hit the comparator and so does the jitter as well. As more photons pile up in the SiPM cells, the output signal slew rate increases. Jitter is the ratio between the amount of noise and slew rate $\left(\frac{noise}{SR}\right)$ so it is expected the jitter reduces with the number of detected photons [3].

Fig. 51 delay vs noise iteration

Additionally, the signal-to-noise ratio is measured in case of one photon. *Fig. 52* shows this is accomplished by sweeping the threshold level along the signal dynamic range and counting the number of transitions at the output. The number of transitions will go from zero to 100%, building a S-shaped graph called S curve (*Fig. 53*). S curves are very useful tool for signal processing, as it gives an approximate idea of the noise level, when differentiated. The first derivative of the S curve is a Gaussian curve and the noise statistics can be derived from there. The SNR is calculated as the distance between the mean values (the mean corresponds to the average threshold when the transition of the comparator occurs, i.e., the middle point of the S curve) with respect the standard deviation of 0 photons, i.e., the noise. The detected SNR should be around 10 (linear).

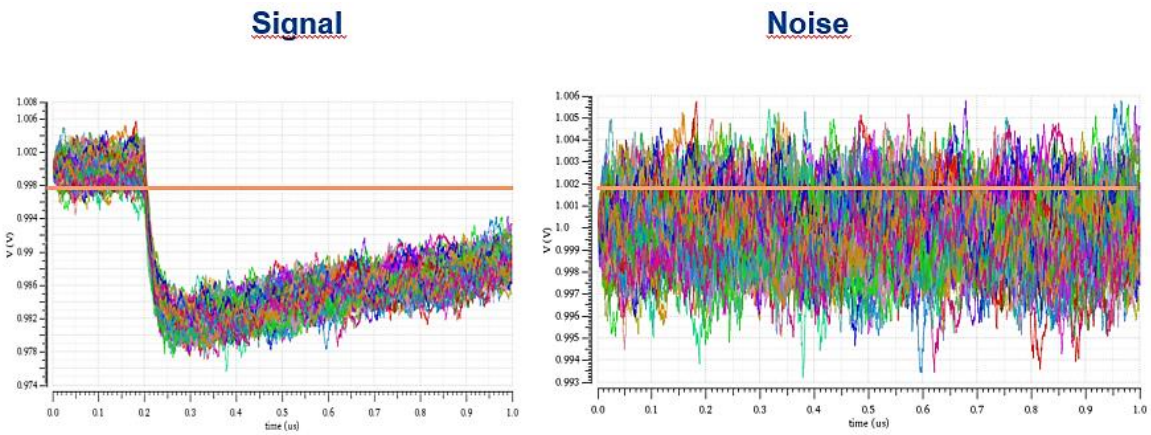

Fig. 52 Threshold sweep for 1 photon signal and noise

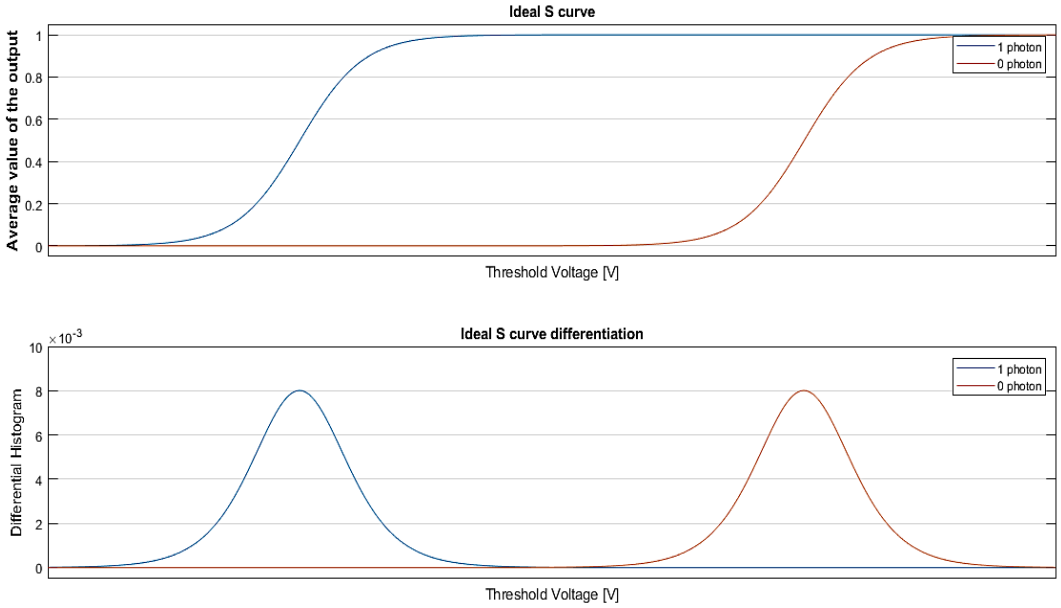

Fig. 53 S curves and differentiation

3.5. Layout

The layout of the four stages of the comparator has been designed. The criteria followed has been to maximize the space using in Y-axis -with a maximum of 59 μm, counting on the implants. 59 μm is defined as the height of occupied for the whole channel (complete processing of each input).

Some basic techniques of layouting have been utilised. The transistors using various multipliers have been alternated to preserve common centroid. Also, they have the same orientation along the wafer in order to prevent mismatch. In addition, the resistors have been placed using interdigitated structure [7].

The position of the gates has been defined on the top, and protection diodes have been used to protect the gates. These diodes help to expel the excess of charge accumulated at the gates during the chip manufacturing.

Dummies are transistors connected as a capacitor, i.e., shorting drain and source. They are placed at the end of a group of transistors to improve the matching between them. The goal is to obtain the most identical behaviour as possible, so that transistors nearby do not behave differently and thus avoiding significant mismatch in the intrinsic parameters. Besides, these dummies are reused as decoupling capacitors, to filter the noise on nodes not susceptible to capacitance variations, i.e., nodes with DC signals. For instance, gates controlling a tail current (biasing nodes).

For noise prevention, each device is shielded with guard rings. Also, the guard rings permit having more contacts to the substrate, and thus minimise the resistance of the active devices.

The order of used metals is important as well. For the layout of the comparator blocks, only Metal 1, Metal 2 and Metal 3 have been used. For the routing Metal 2 has been used

horizontally and Metal 3 vertically. The rest of the metals have been left for higher hierarchies. This way we maximise the layouting resources.

Finally, calibre tool is used to pass DRC (Design Rule Check) and LVS (Layout-versus-Schematic).

3.6. Parasitic extraction and comparison with schematic

The extraction is also made with PEX (Parasitic Extraction) tool from Calibre.

The results are compared with the schematic. The most important figures (delay, gain, hysteresis, power consumption) of merit are evaluated here. Delay and jitter are the bottleneck for the triggering comparator, so special attention is paid to these magnitudes, because if they deteriorate too much, the design needs to be adjusted. However, ensuring the operating points work fine, it is likely that this is not necessary.

In the end, the whole channel is simulated in extraction to have the most realistic results.

3.7. Comparator in the channel

Finally, the noise analysis of the comparator is repeated at channel level (in schematic and extracted). The results from this simulation are the definitive ones, and it will show how much the jitter and delay deviate from the standalone measurements. In principle, the channel results should not deviate too much from standalone simulations since the comparator has been previously adjusted.

Fig. 54 shows the entire channel with the digital control and common-biasing blocks.

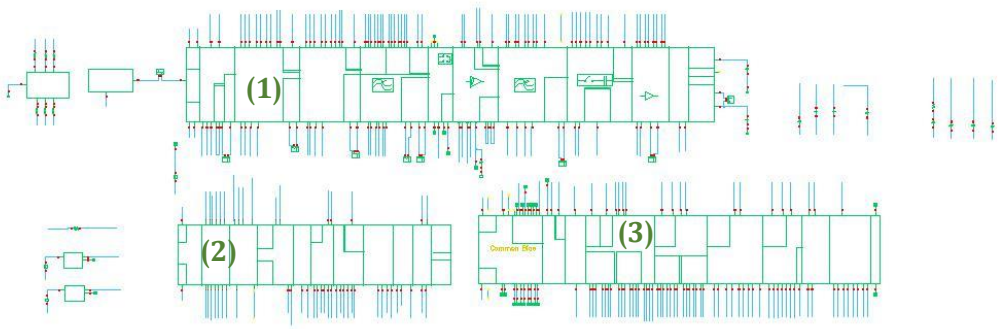

Fig. 54 (1) Channel (2) Digital Control Block (3) Common Bias Block

4. Results

4.1. Transistor level design of the comparator

In this section, *Fig. 55, Fig. 56, Fig. 57* and *Fig. 58* show the definitive values of the comparator design. Regarding to the initial values, some changes have been introduced. The first stage has increased its current consumption in exchange of a decrease in resistor value. The resistor value was decreased to improve the output dynamic range. Also, the pMOS differential pair is made bigger so that it can follow better the common modes near the middle point. The diodes of the first and second stage have been made bigger to decrease its V_{DS} drop.

The third stage has been the most modified block. The tail current has been increased to ensure proper voltage drop in the low voltage current mirrors. The width ratios in the current mirrors have also been tuned to ensure equal V_{DS} drop at the cascode and mirror transistors. The differential pairs have also been increased to guarantee saturation at all the corners. Finally, the diode transistor has been changed to generate a proper cascode biasing voltage. As it is a nonlinear circuit, the hysteresis block has been the most difficult block to adjust for all the process and temperature corners.

Finally, the NOR gate has been resized by making a sweep of the widths and choosing the most convenient one to drive a 200 fF load. This capacitance is the load that has been observed in previously manufactured FASTIC chip.

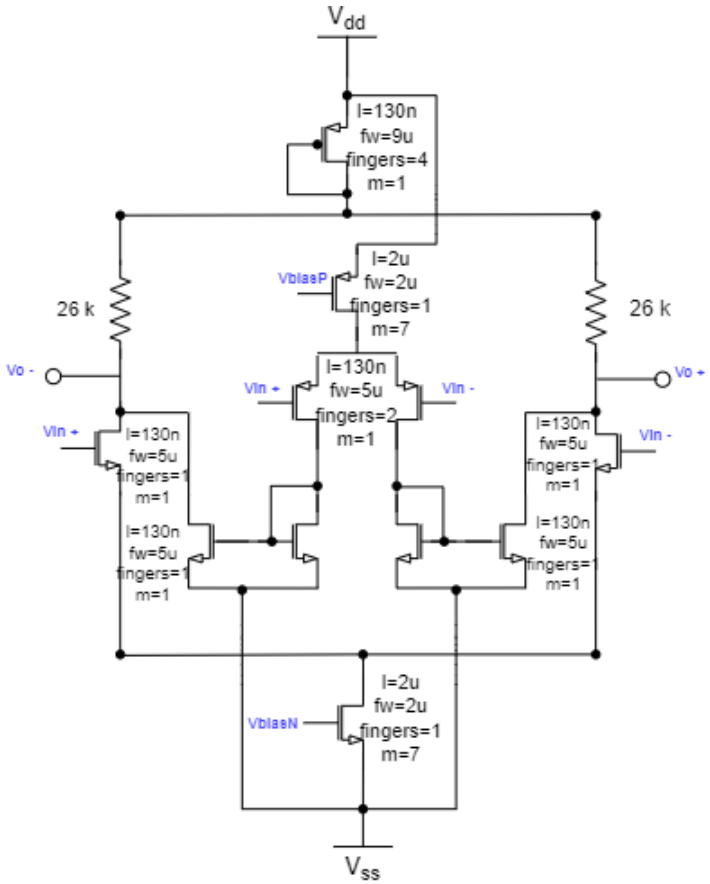

Fig. 55 1st stage definitive design

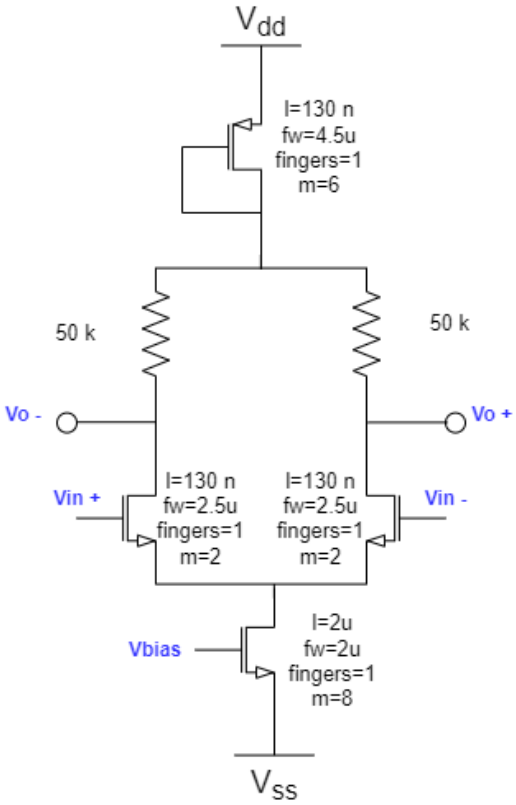

Fig. 56 2nd stage definitive design

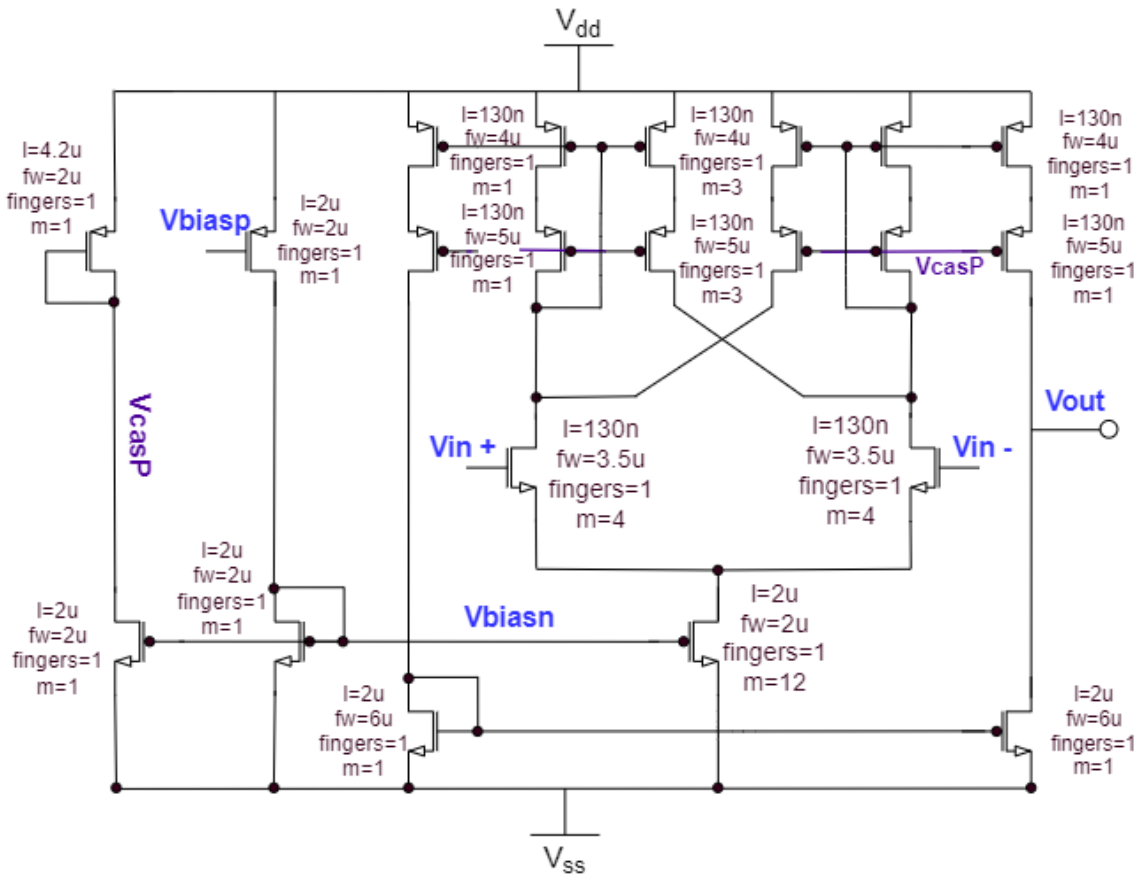

Fig. 57 Hysteresis comparator definitive design

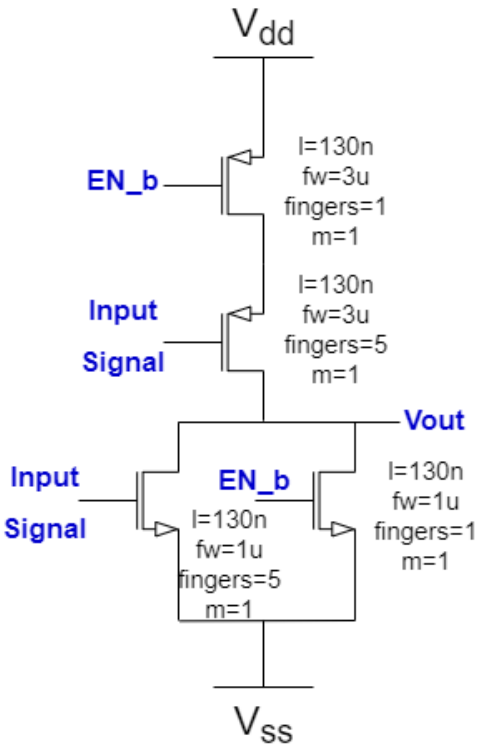

Fig. 58 NOR gate definitive design

4.2. Transistor level design of the current DAC

Once entered the initial values on the schematic, a sweep of lengths and widths of cascode and mirror transistor has been made. The lengths of the cascodes and the mirror have been slightly increased to improve the current copy. The widths also have been adjusted, using various fingers and multipliers, to adjust the V_{DS} mismatch and keep all the transistors in saturation. The optimal sizes have been chosen simulating Monte Carlo and measuring the current and V_{DS} mismatch between mirror transistors. Finally, Monte Carlo simulations are shown in *Fig. 59*. The definitive values of the current mirror are *Fig. 60*.

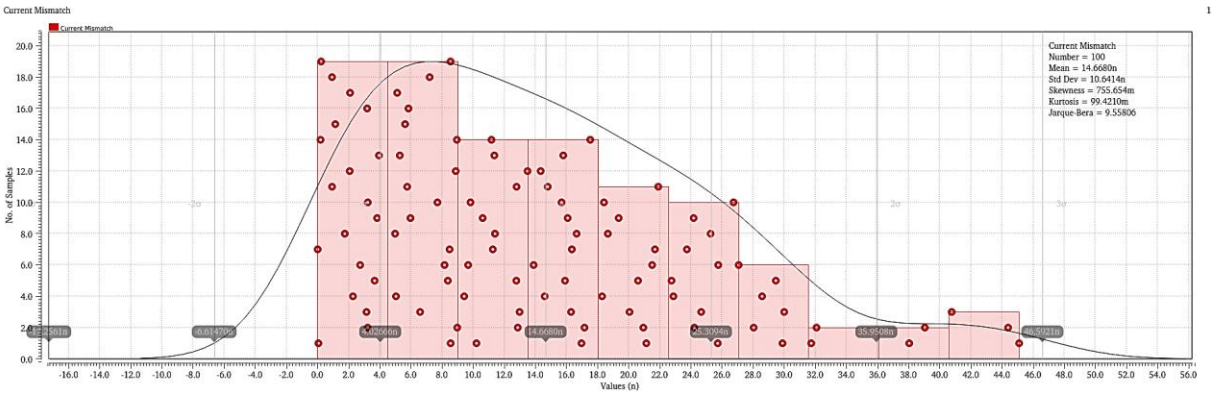

Fig. 59 Current mismatch statistics with Monte Carlo

Due to statistical mismatch, the mean copy error is 14.7 nA with a standard deviation of 10.6 nA. This means that the worst case would be an error of 25 nA, which is an error of 2.5 %.

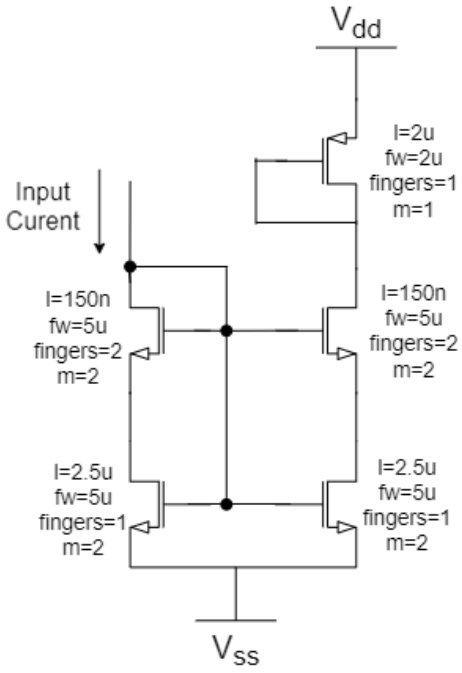

Fig. 60 current mirror definitive values

4.3. Comparator compared with ideal signal

The common mode we are interested in is 1V because the baseline is fixed at that voltage level, and the reference signal for triggering will be near the baseline. Besides, the path selection comparator is less demanding, as its only function is to switch from one comparator to the other. On the contrary, the triggering comparator has some time constraints to accomplish.

4.3.1. Transient analysis

Fig. 61 shows the comparator works as expected and follows well the signal shape at the output.

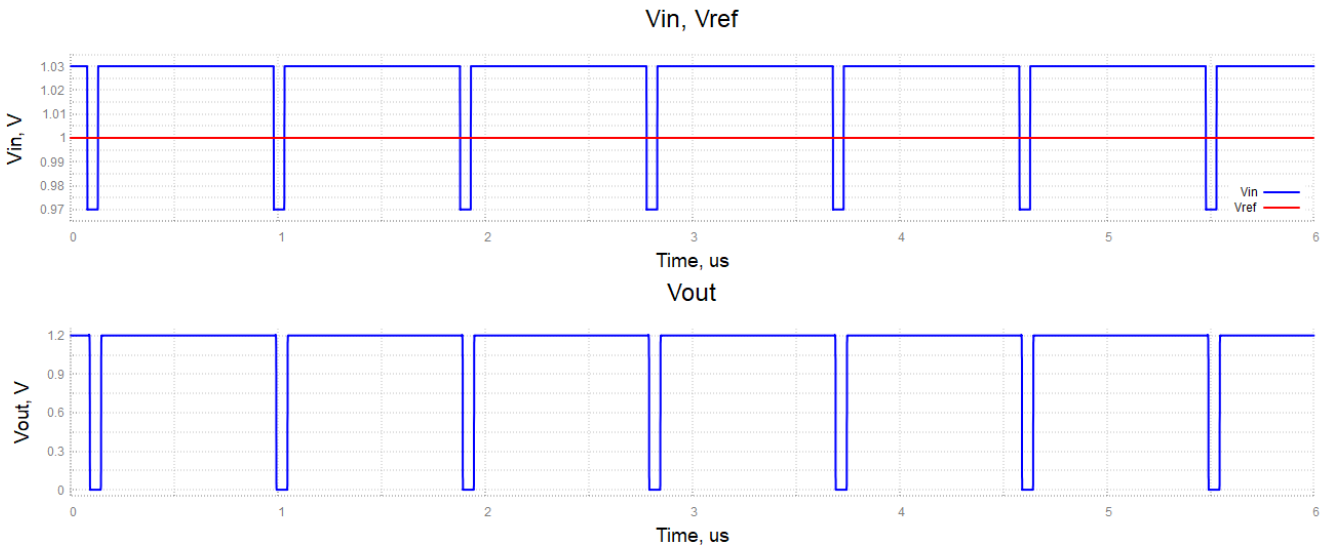

Fig. 61 Input, reference and output signals

Fig. 63 and *Fig. 62* show the signal evolution at the output of each stage.

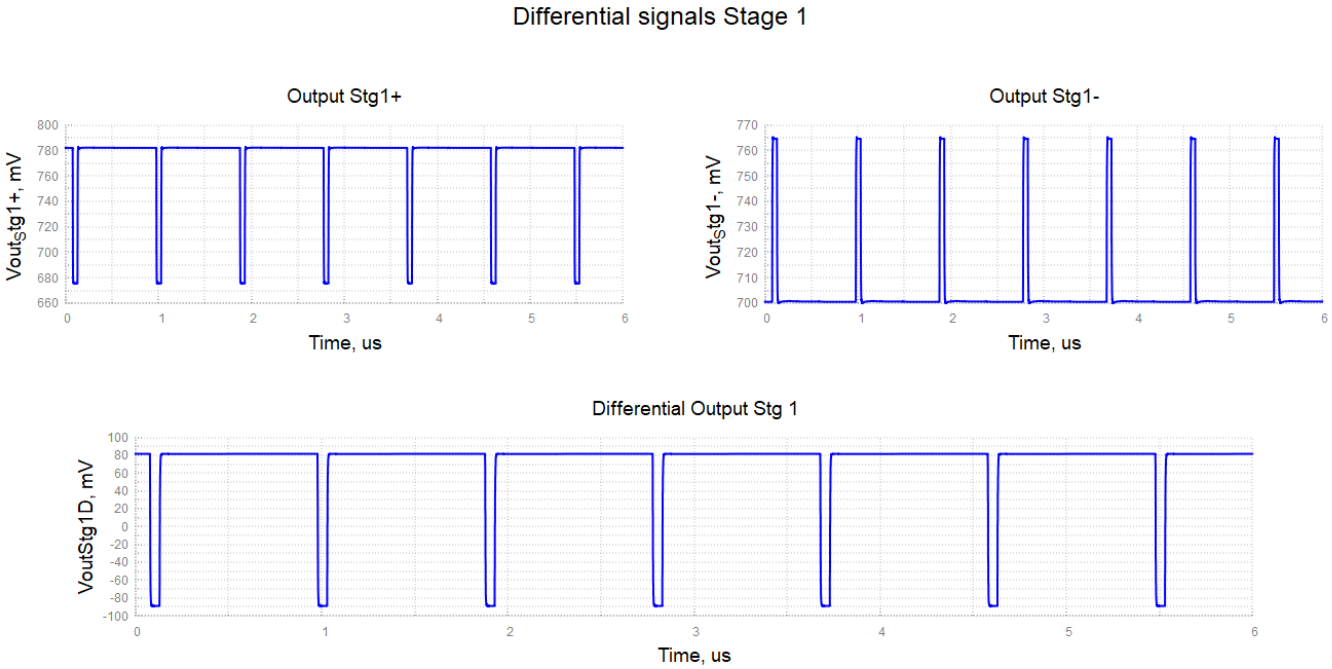

Fig. 63 Stage 1 diferential signals

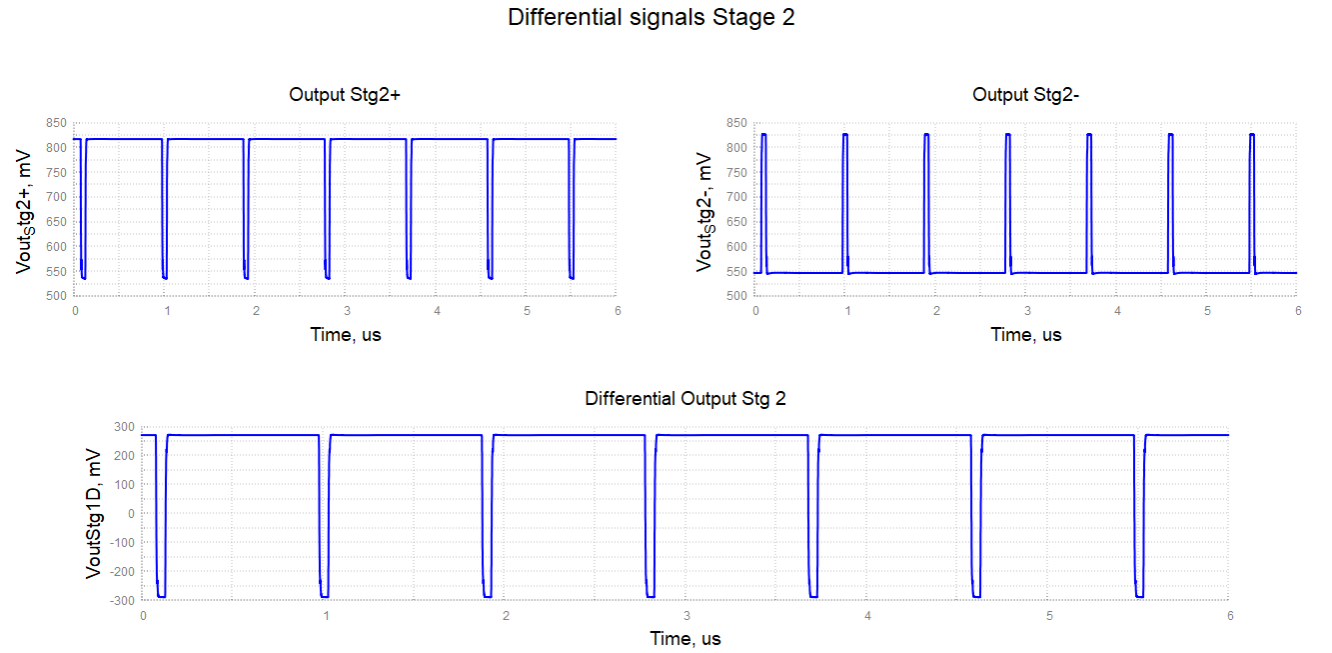

Fig. 62 Stage 2 differential signals

Clearly we see that the differential amplitude increases from 30 mV (at the input) to 160 mV (first stage output) and 500 mV (second stage output). This is consistent with the gain we will see at AC and DC analyses. In *Fig. 64* the signal evolution is recognisable.

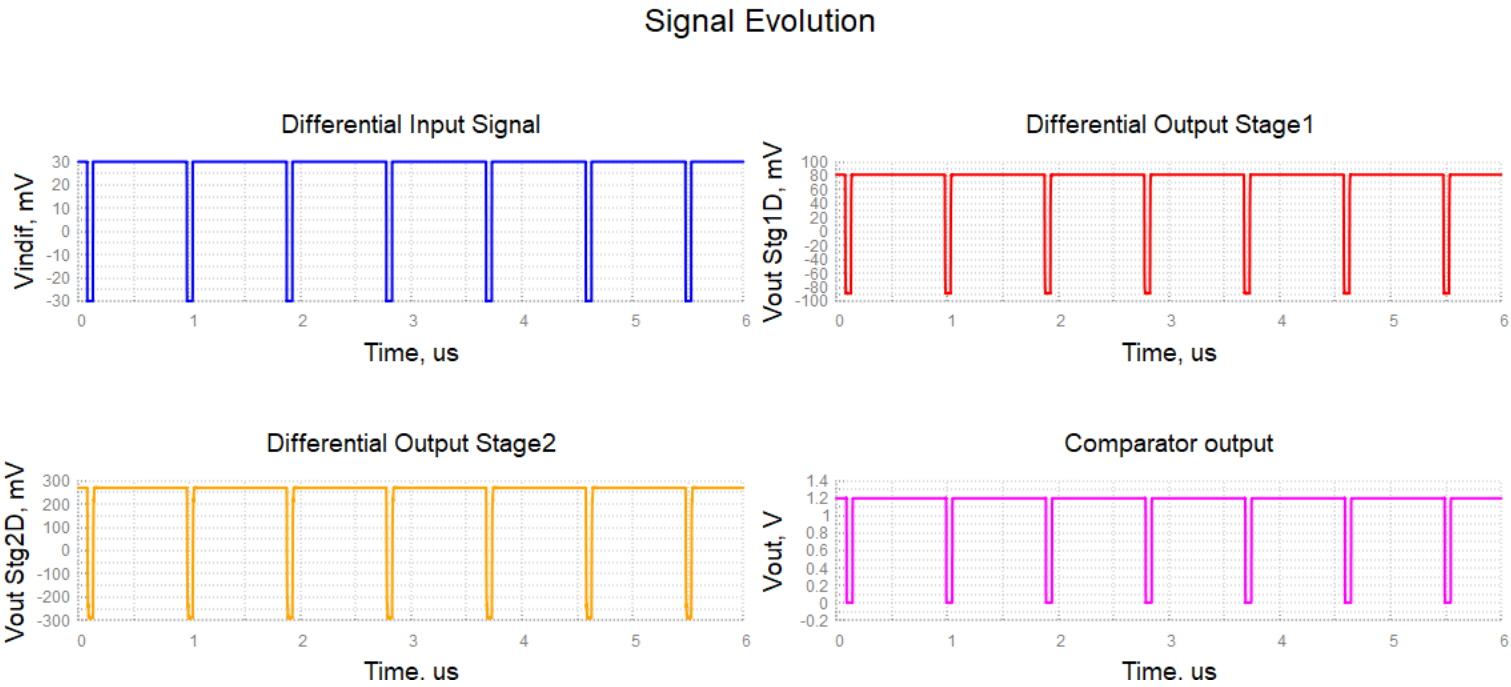

Fig. 64 Differential outputs

Finally, we notice the function of the output logic gate, which restores the shape of the hysteresis block output.

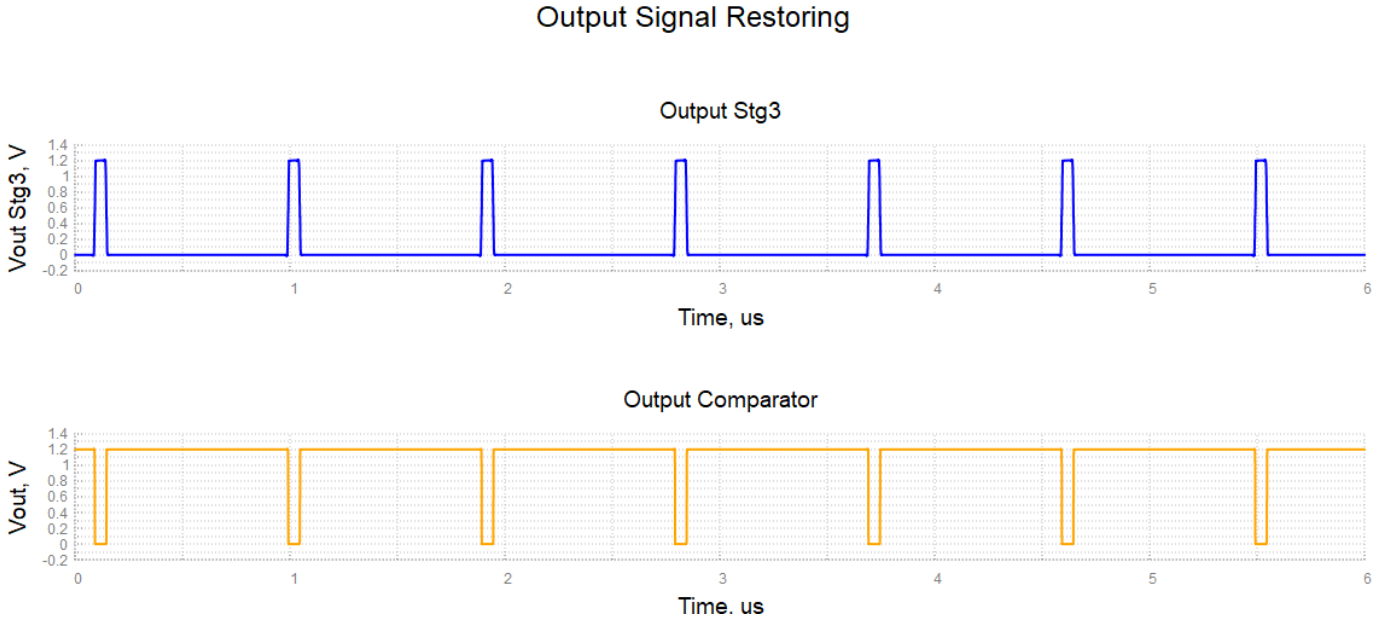

Fig. 65 Output signal restoring

The delay is the difference between the time when reference level cuts the signal and the comparator output reaches 0.6 V in the transition. As said earlier, the target delay is around 15 *ns* at most, which is accomplished at all common modes in general. As *Fig. 66* illustrates, the general trend is that the performance is constant at the central common modes. At the extreme common modes there is no a great divergence which means that the comparator will operate in a similar way regardless of the common mode.

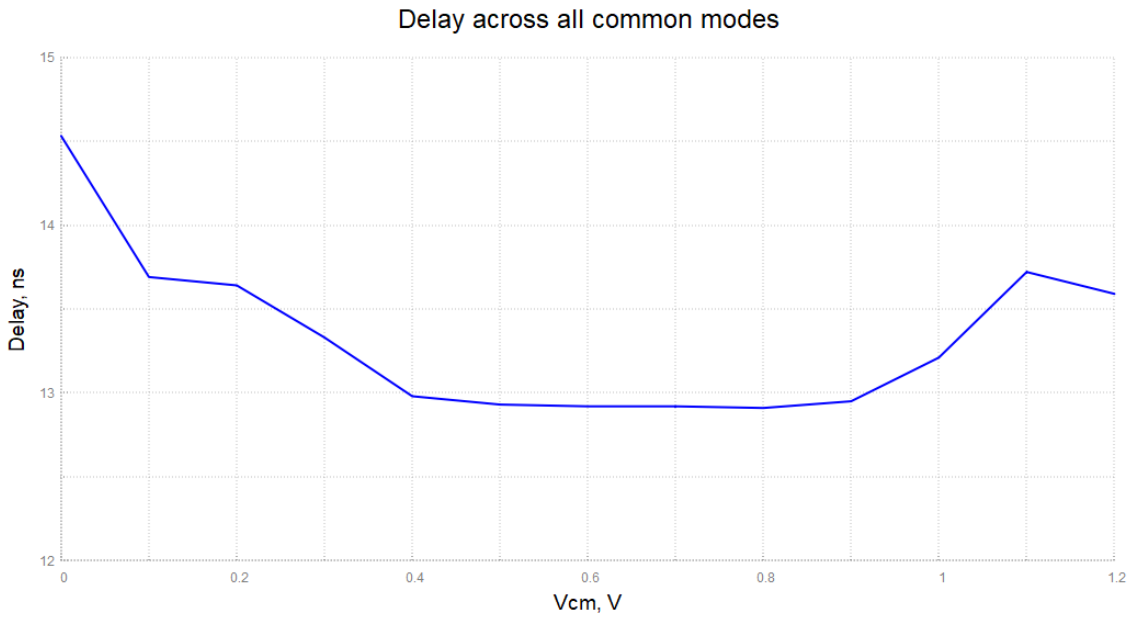

Fig. 66 Delay

Fig. 67 shows output rise and fall times. The behaviour along the common modes is similar to the delay measurement. The NOR gate has been resized to equalise the rise/fall times at the output of the comparator.

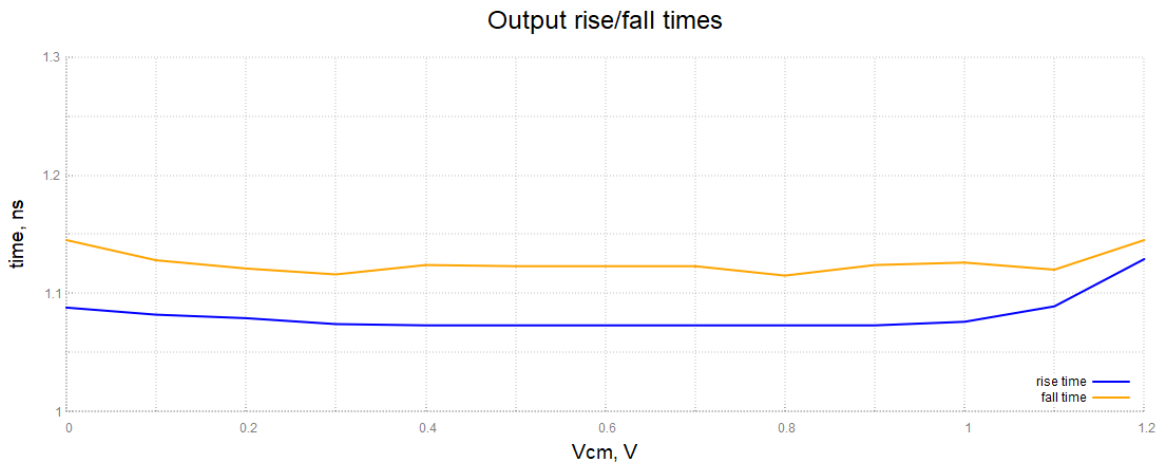

Fig. 67 Output rise/fall times

4.3.2. DC analysis

The signal response follows the trend of the typical differential amplificator curves and hysteresis appears at the output of the hysteresis block. *Fig. 68* shows the DC input and output signals at the comparator. To see the hysteresis at the output we must enable hsyteresis sweep in DC analysis configuration.

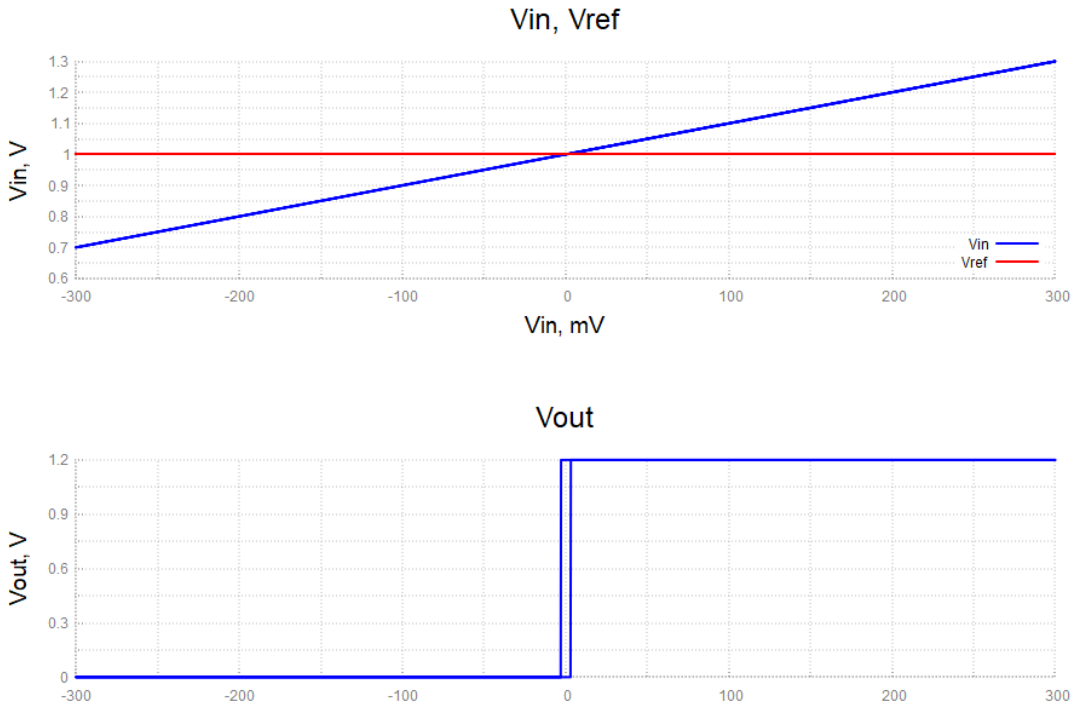

Fig. 68 DC input and output signals

Fig. 69 shows the output response of the first stage.

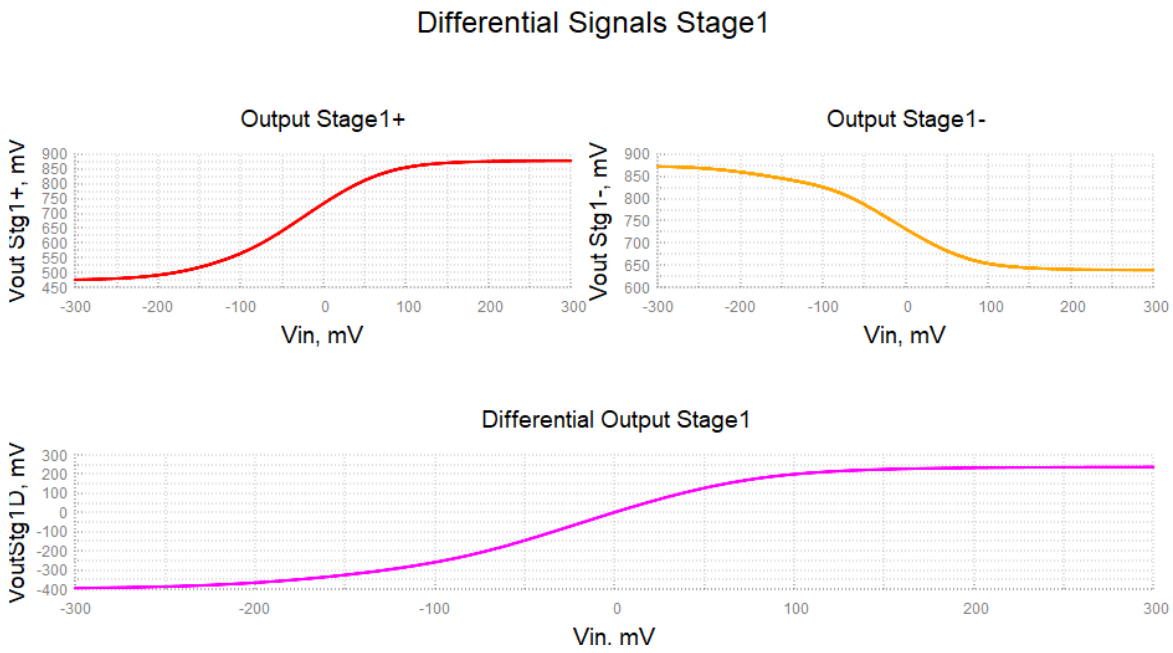

Fig. 69 Stage 1 differential signals at 1 V

We may notice that, the differential signals in the output of the first stage are not symmetrical. This is because the operating point of the circuit ($1\ V_{CM}$) is very near the power rail, so when introducing a positive variation above the common mode the output the output dynamic range is saturated.

Indeed, if we look to the output response at the central common mode it is perfectly equalised. *Fig. 70* shows the output reaches the same voltage level than in the previous case because it is the top of the output dynamic range.

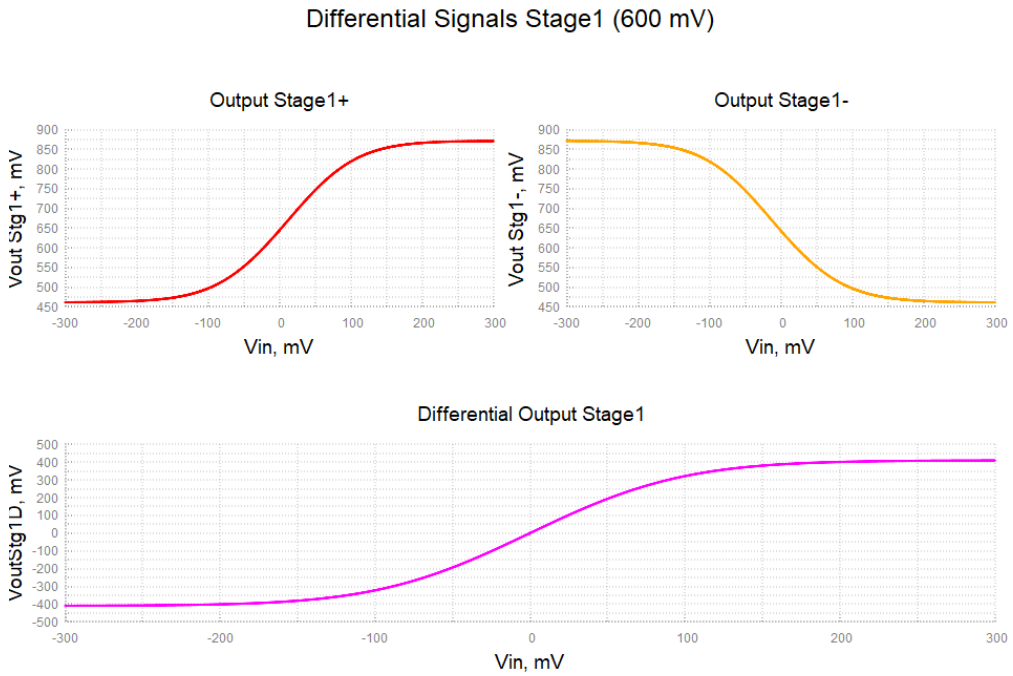

Fig. 70 Stage 1 output differential signals at 600 mV

As *Fig. 71* shows, the second amplifier response is symmetrical, since the input signal is no longer rail-to-rail.

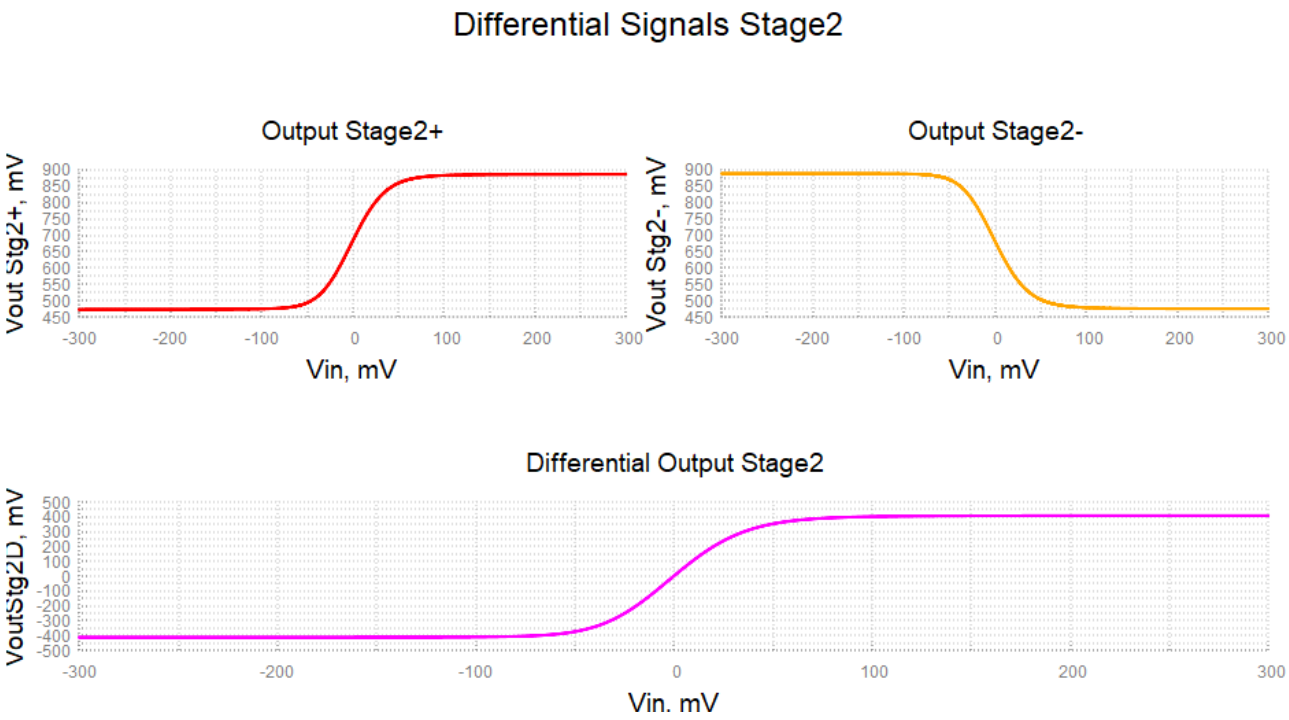

Fig. 71 Stage 2 differential signals

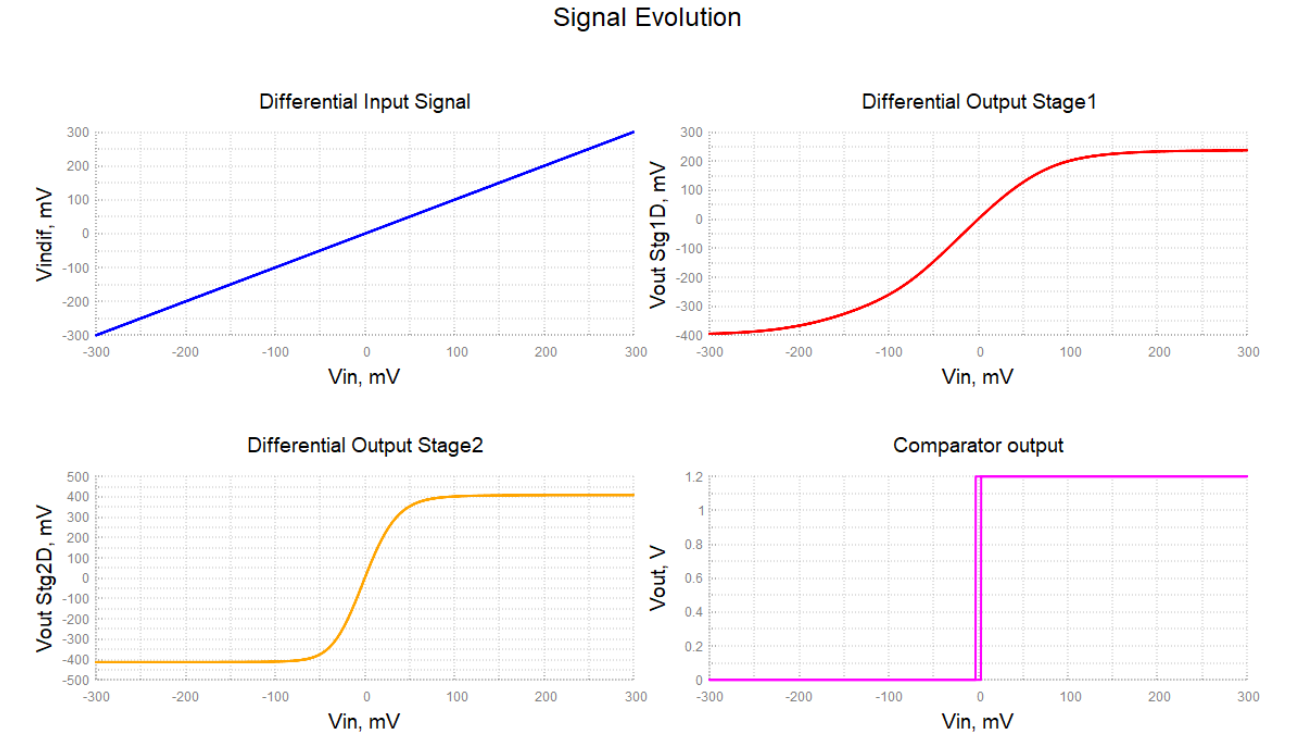

Fig. 72 Output signals

The most important measurement here is the hysteresis amplitude. Around 6 mV of hysteresis is necessary for the comparator to be robust against the noise. *Fig. 73* shows the desired hysteresis at central common modes and 1 V common mode.

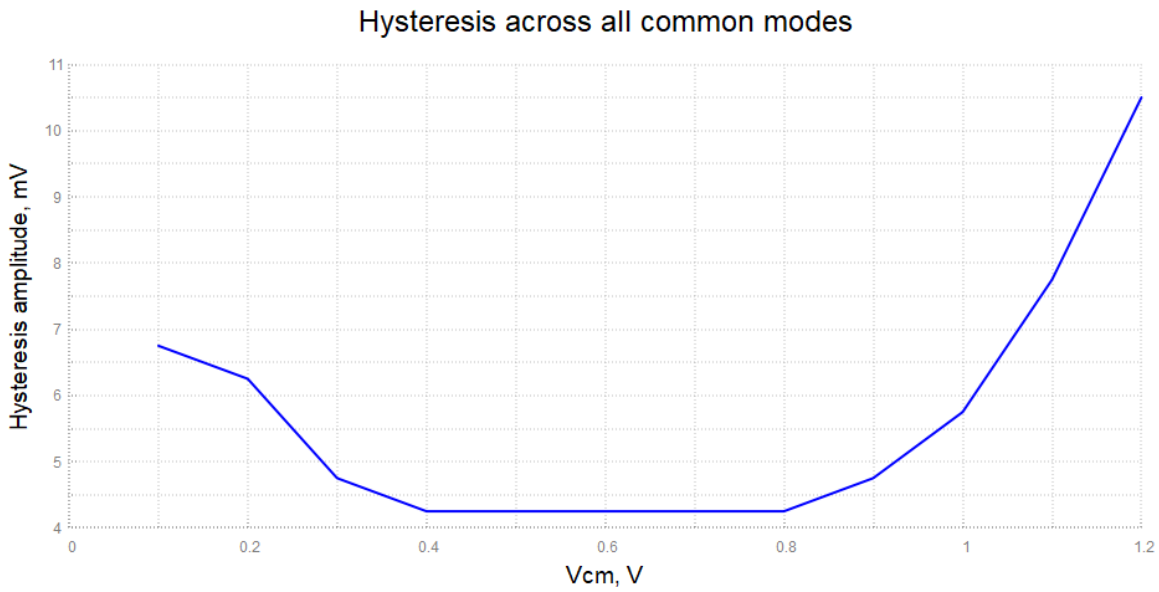

Fig. 73 Hysteresis amplitude

Plotting the DC gains, which is nothing more the derivative of the output differential signal, we see the results are consistent with the transient analysis. *Fig. 74* again shows the same problem as *Fig. 70.* The amplifier can not follow the input positive differential voltage, so it has a smaller slope in the positive side of the transfer function. This implies a limitation in the achievable gain and the maximum can not be centered at $V_{in} = 0\ mV$.

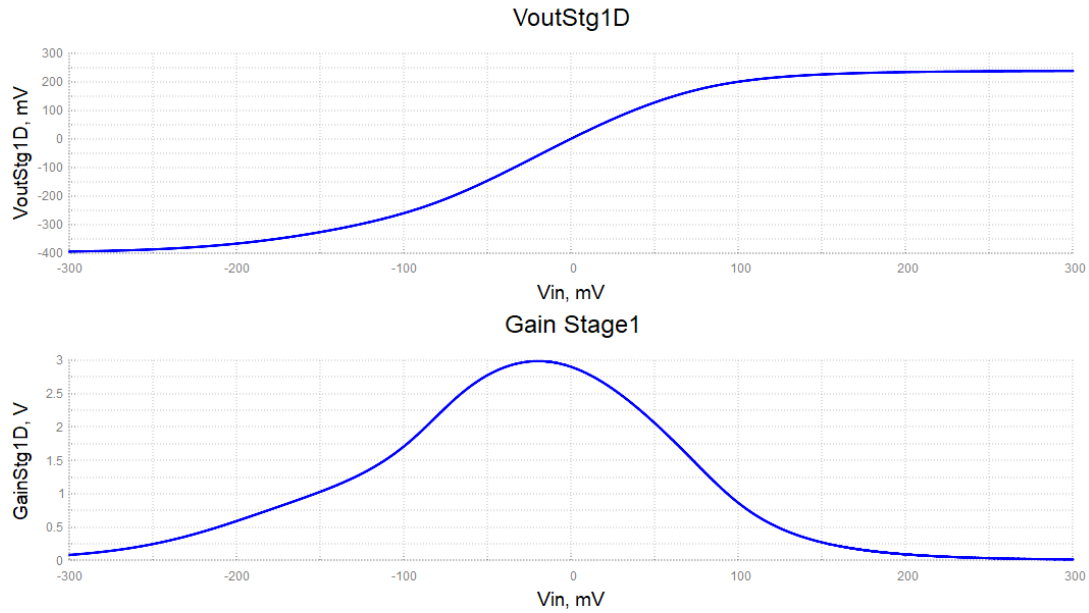

Fig. 74 Stage 1 output gain

On the other hand, we see in *Fig. 75* that in case of 600 mV the gain is higher, because there is more dynamic range available, and it is centered at $V_{in} = 0\ mV$.

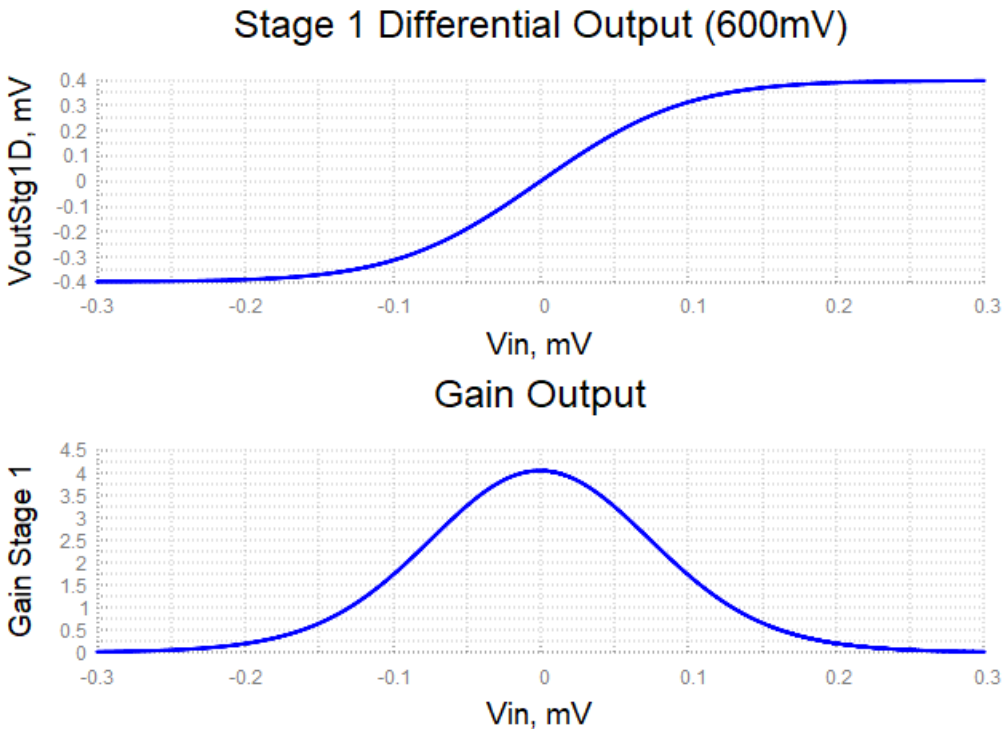

Fig. 75 Stage 1 output gain at 600 mV

Fig. 76 verifies that the output dynamic range is no longer saturated.

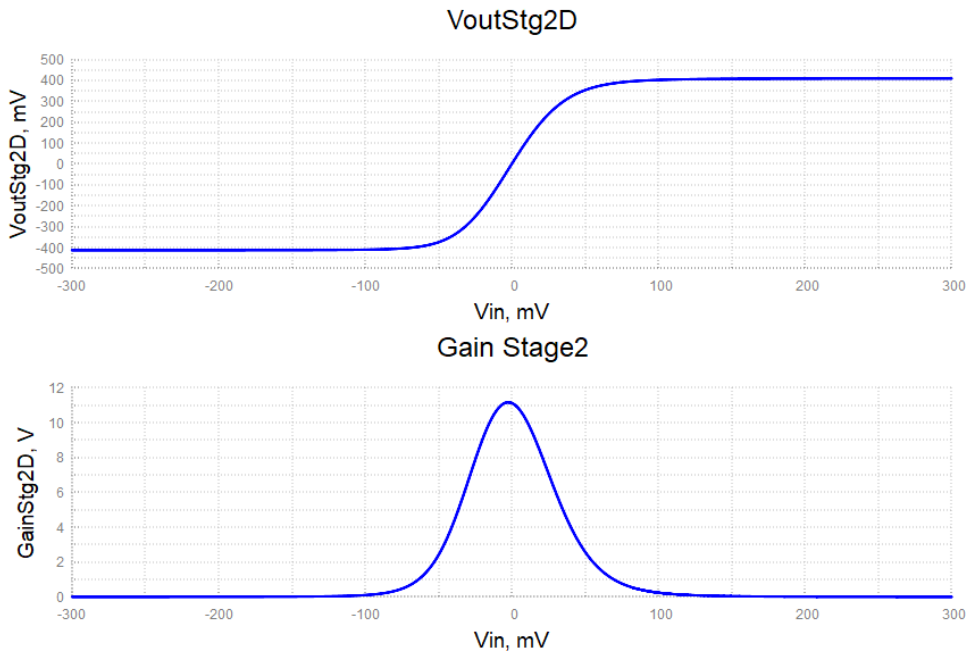

Fig. 76 Stage 2 output gain

Finally, the output of stage 3 and stage 4 and their derivatives in *Fig. 77* and *Fig. 78*.

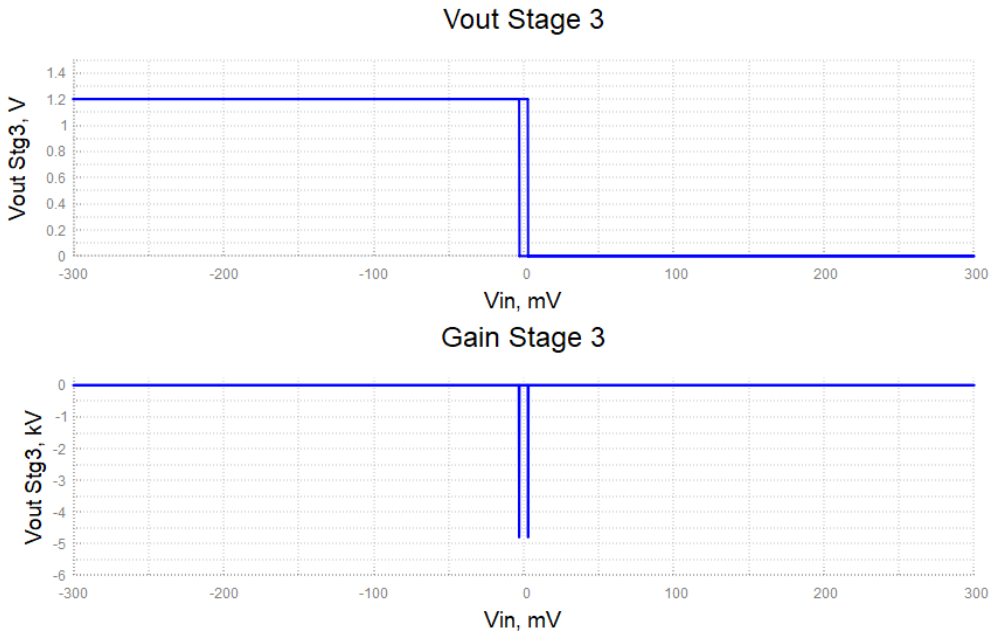

Fig. 77 Gain output stage 3

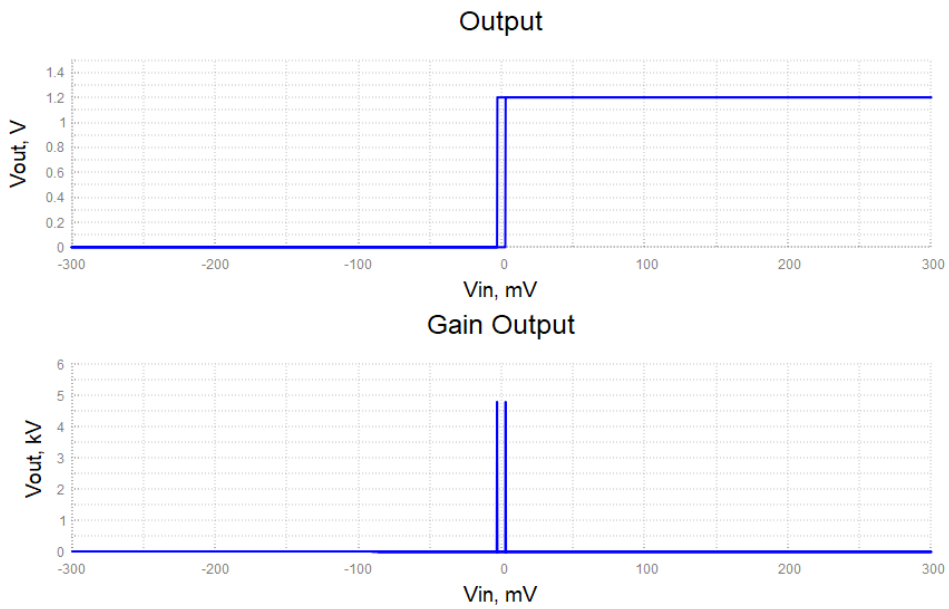

Fig. 78 Gain output of the comparator (stage 4)

The input referred offset tested in ideal signal of both amplifiers is very low: $-355\,fV$ at the first stage, $3.286\,pV$ at the second and $2.75\,mV$ at the third stage. However, when simulating mismatch with Monte Carlo the mismatch starts to be significative, which will be discussed in Section 4.3.4 of this chapter.

Finally, the total power consumption is shown in *Fig. 79*.

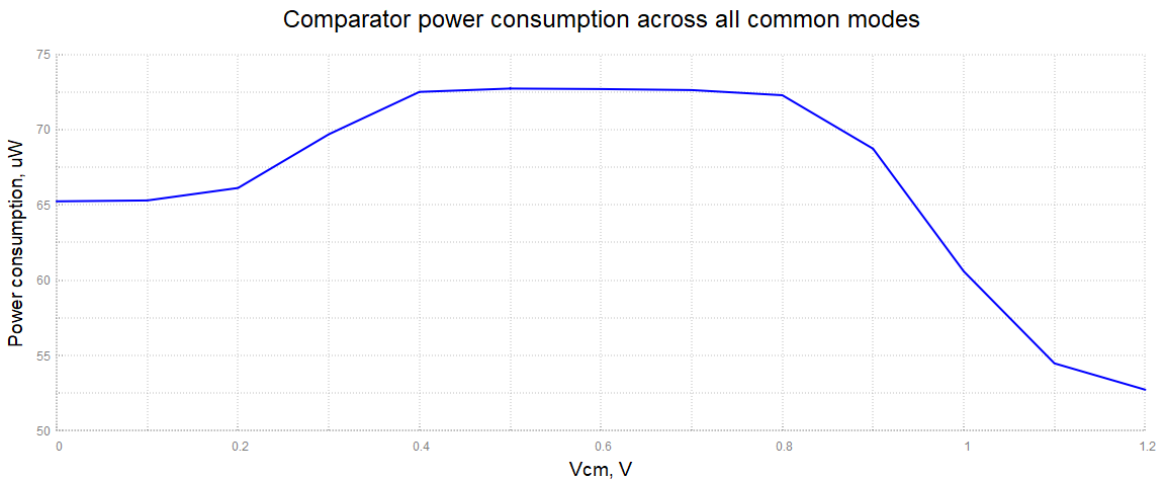

Fig. 79 Power consumption along the common mode

The power consumption has been adjusted around 50 μW for the circuit operation point (1 V). At 1 V the circuit consumes 60 μW, which is good enough for the application.

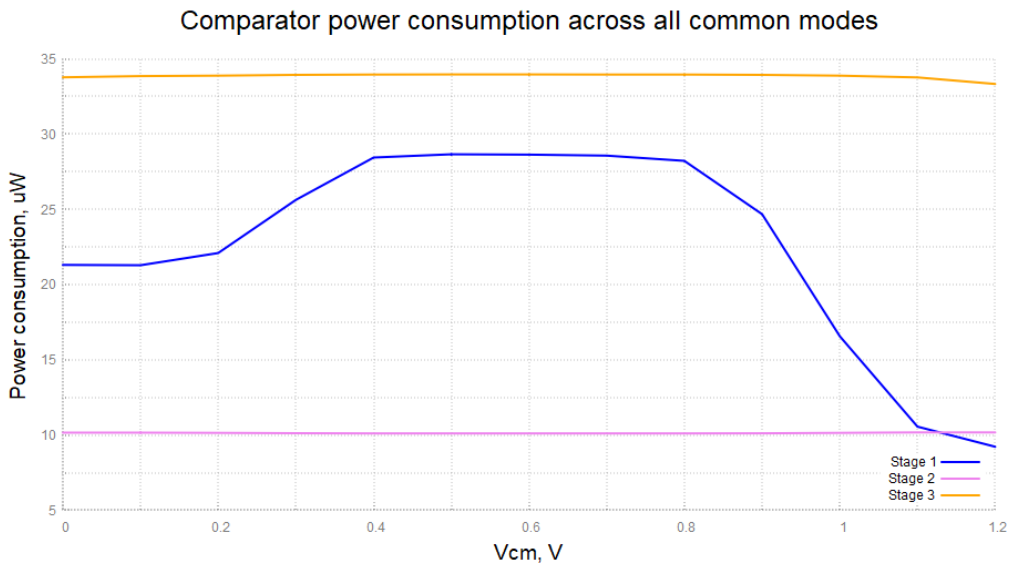

Fig. 80 Power consumption of each stage along all the common mode

Fig. 80 shows the power consumption of each stage. Hysteresis block is the most consuming part of the comparator, as it is the core block of the architecture. The next most consuming block is the input R2R amplifier, followed by the 2nd stage FDA and the output logic gate (which consumes very little). The variation in 1st stage consumption is because low common modes switch off the nMOS differential pairs, whereas high common modes switch off the pMOS differential pair.

As we increase the common mode towards 1.2 V the consumption decreases more than at low common modes. The responsible of this inequality are the current mirrors on the pMOS branch. At low common modes, the pMOS differential pair is ON, so more current flows through the current mirrors than at higher common modes (pMOS differential pair

OFF). Also, this additional current consumption even increases due to the V_{DS} difference in the current mirrors. *Fig. 81* and *Fig. 82* show the operating points at 200 mV and 1 V common modes, respectively.

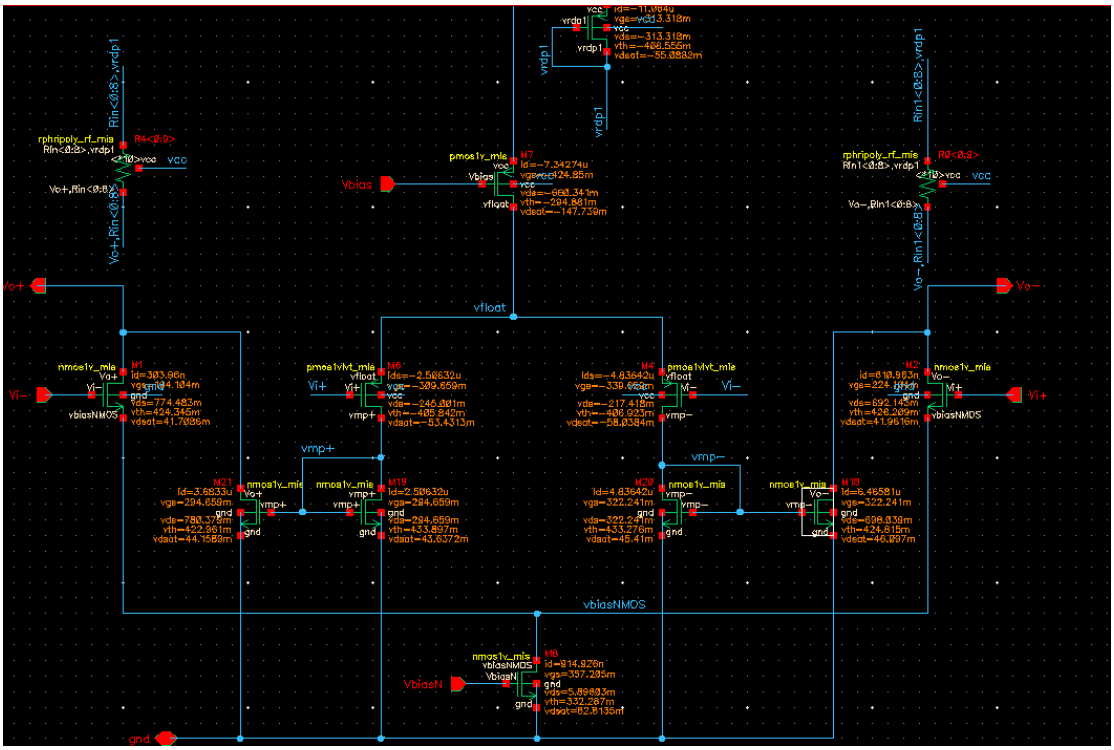

Fig. 81 Operating points 1st stage at 200 mV common mode

In figure above, an increment of current consumption is shown, which makes this stage more consuming than at 1 V common mode.

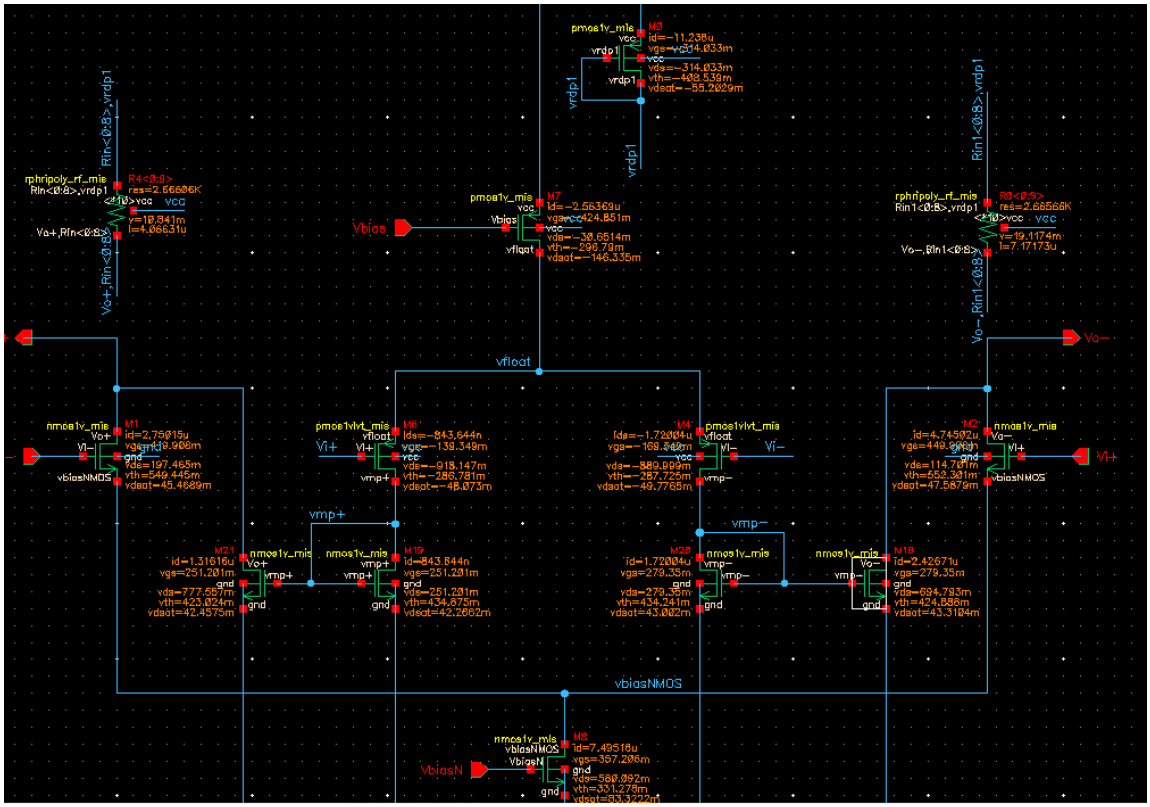

Fig. 82 Operating points 1st stage at 1 V common mode

4.3.3. AC analysis

Next plots show the output AC gain of each stage. Again we verify the consistency of previous measurements in gain.

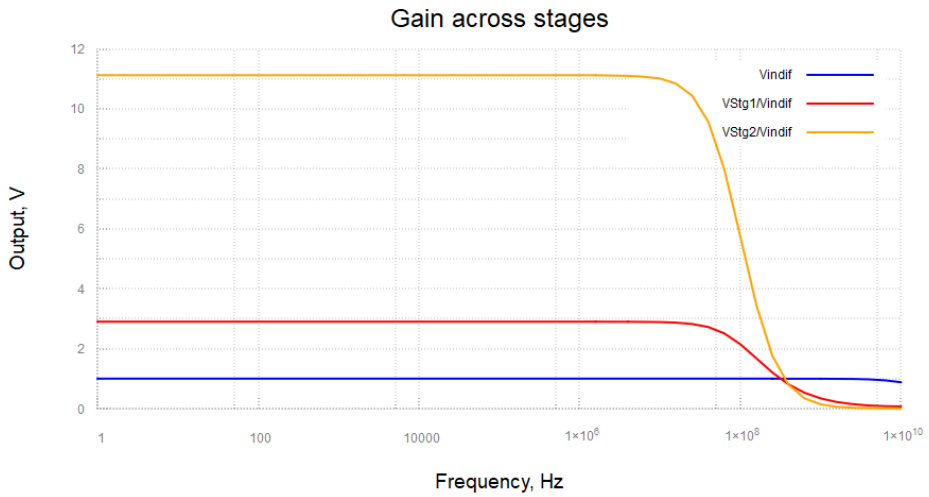

Fig. 83 Gain-bandwidth curves of input and intermediate AC signals

In *Fig. 83*, we notice the FDA gain in the second stage is higher than in the first stage. Although 2nd stage consumes less, the load resistance is higher, which explains this

difference. Stage 3 is definitively the block that provides gain due to higher current consumption *(Fig. 84)*.

We can also compare the previous gains with the one after the logic gate (*Fig. 85*). However, this has little interest since the signal is already in digital domain.

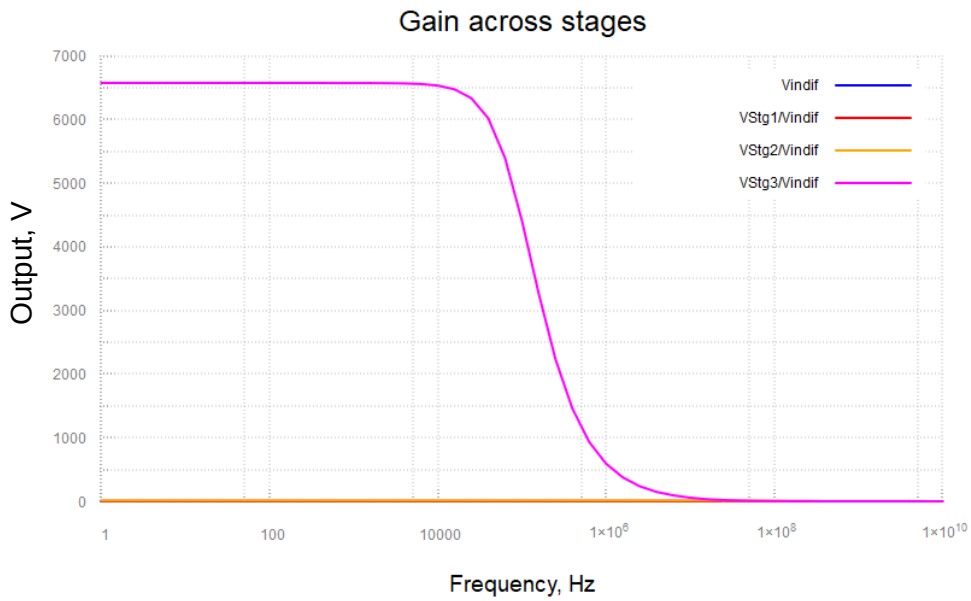

Fig. 84 Comparison of third stage gain, with respect to the previous stages

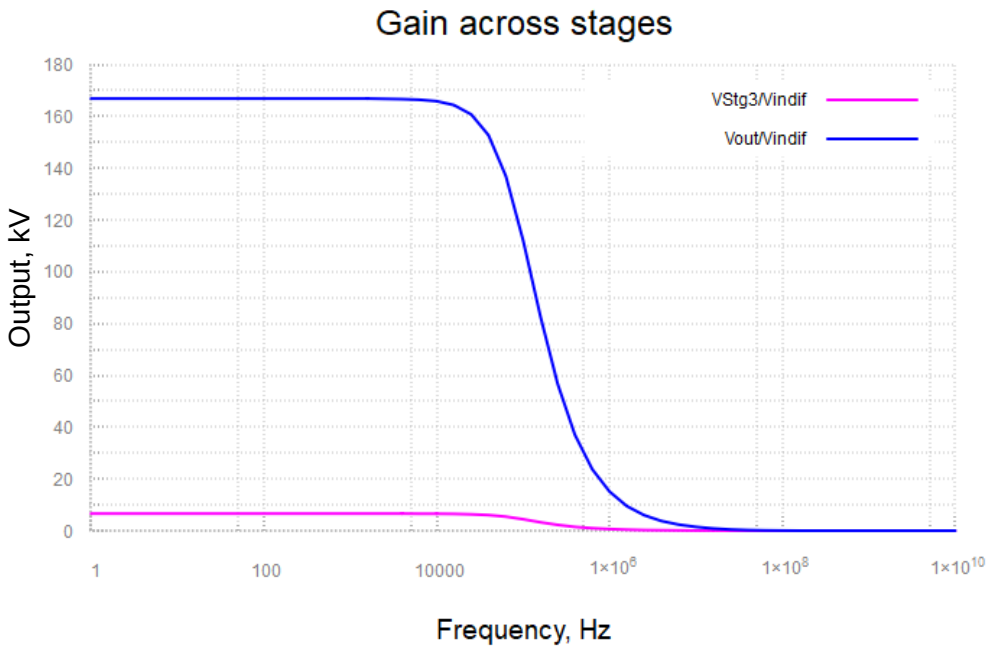

Fig. 85 Comparison of gain after the NAND gate with the hysteresis block

We can also see that the bandwidth of the signal is lower as the gain is higher, verifying the GBW product remains constant.

Finally, *Fig. 86* provides results of the gain across all common modes in dB.

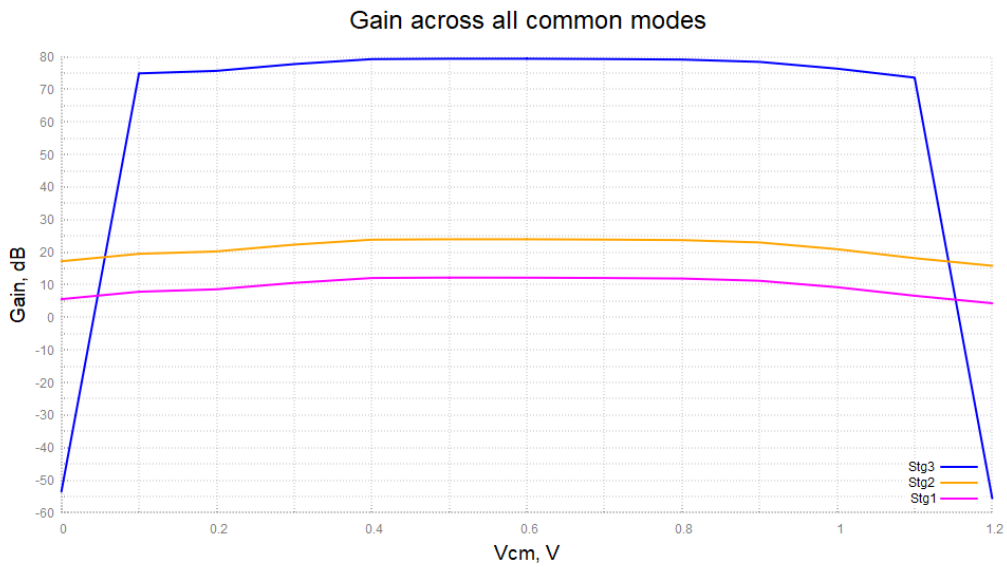

Fig. 86 Gain in all common modes in dB

To finish the first part of the analysis in standalone, *Table 3* sums up some results obtained in the simulations, at 1 V common mode.

Specs	Actual Result (1 V_{CM})	Target Result
Delay	*13.21 ns*	*around 15 ns*
Rise time	*1.076 ns*	/
Fall time	*1.116 ns*	/
Power Consumption Stg1	16.56 μW	/
Power Consumption Stg2	*10.14 μW*	/
Power Consumption Stg3	*33.88 μW*	/
Total Power Consumption	*60.59 μW*	*around 50 μW*
Total gain	*76.35 dB*	Maximise
Hysteresis amplitude	*5.75 mV*	4 *mV* – 6 *mV*
Gain Stg1	9.25 *dB*	/
Gain Stg2	11.68 *dB*	/
Gain Stg3	55.43 *dB*	/
Bandwidth Stg1	*112 MHz*	/
Bandwidth Stg2	*65 MHz*	/
Bandwidth Stg3	*91 KHz*	/
GBW	*97.5461 MHz*	/

Table 3 Comparator standalone results vs. initial specs

4.3.4. Process and Mismatch

In this section, comparator performance will be studied first using worst-case corners and second, taking into account component mismatches due to statistical variations.

4.3.4.1. Corners

Here, the most important specifications are cross checked with process corners temperature. For the sake of simplicity, measurements at 1 V common mode and power supply 1.2 V are displayed in the following figures.

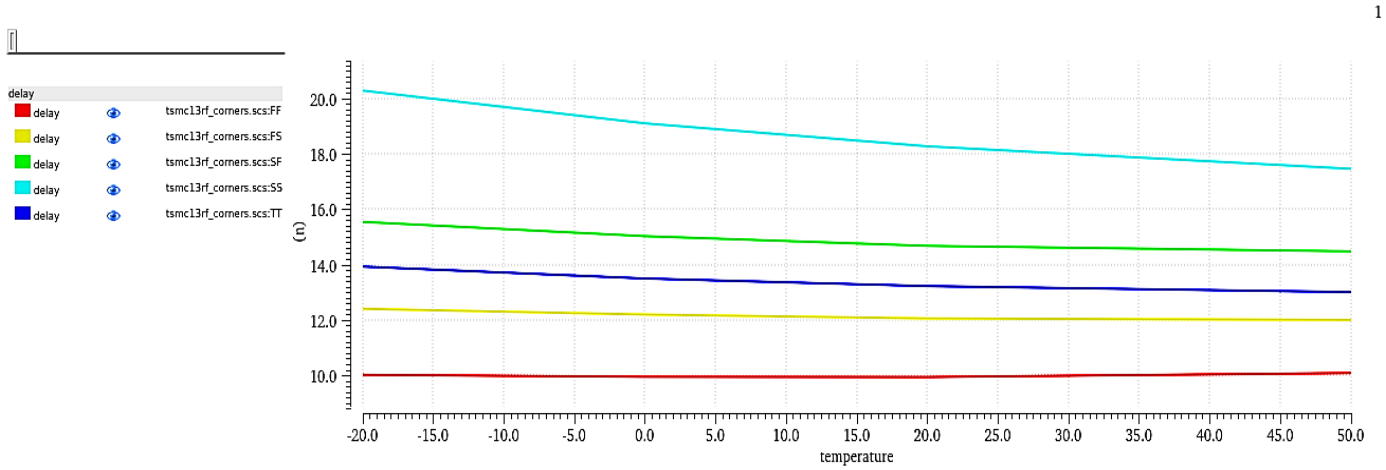

Fig. 87 Delay with corners

From *Fig. 87,* it is clear that delay improves as faster the transistors are. However, there is a slight difference between SF (slow nMOS – fast pMOS) and FS (fast nMOS – nmos pMOS) corners. It appears the comparator is faster when nMOS transistors are faster. This makes sense if we take into account that in the R2R amplifier nMOS pair is the one that follows the signal, since we are operating at 1 *V* common mode. But probably it is the hysteresis block that contributes more to the switching speed. hysteresis comparator input are nMOS transistors as well, and therefore the faster they are, the faster they will switch state.

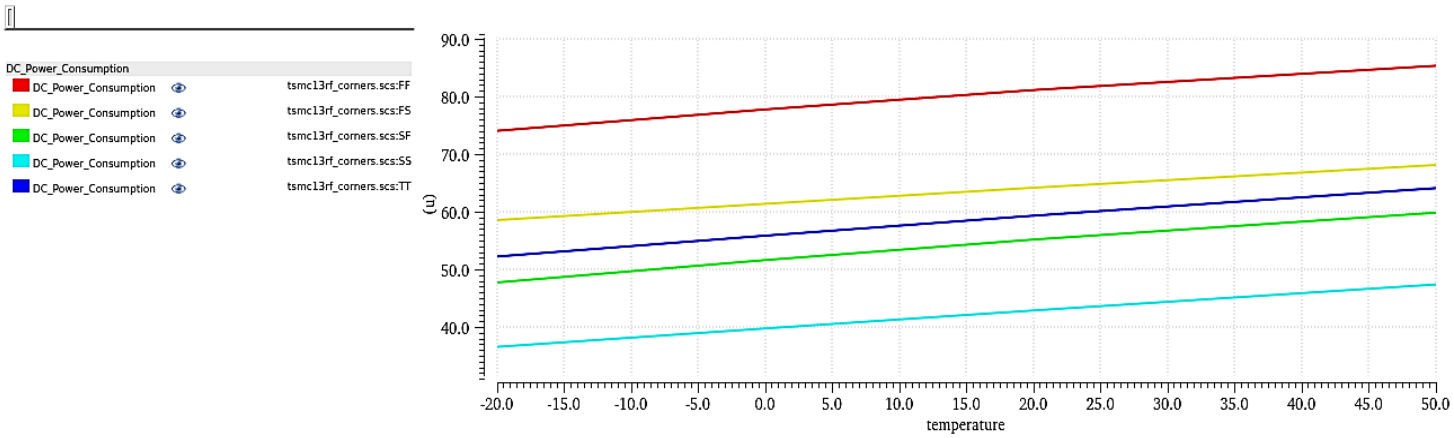

Fig. 88 DC power consumption with corners

A similar reasoning can be followed in order to understand why faster transistors, and specifically faster nMOS, consume more. Simply, it can be said the faster is the comparator the more it will consume, as it is shown in

Fig. 88.

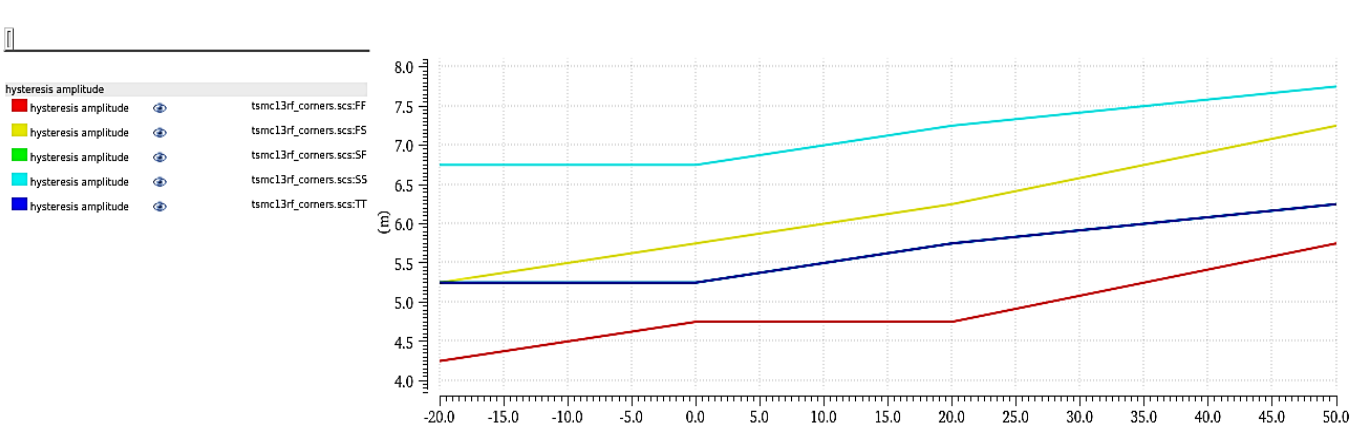

Fig. 89 Hysteresis amplitude with corners

Fig. 89 shows slower transistors increase hysteresis amplitude. The hysteresis comparator switches state when the output of the current mirror enters in saturation and copies the whole current of the input of the current mirror[6]. This is done by a pMOS transistor, so it makes sense to have more amplitude at FS corner, than at SF corner.

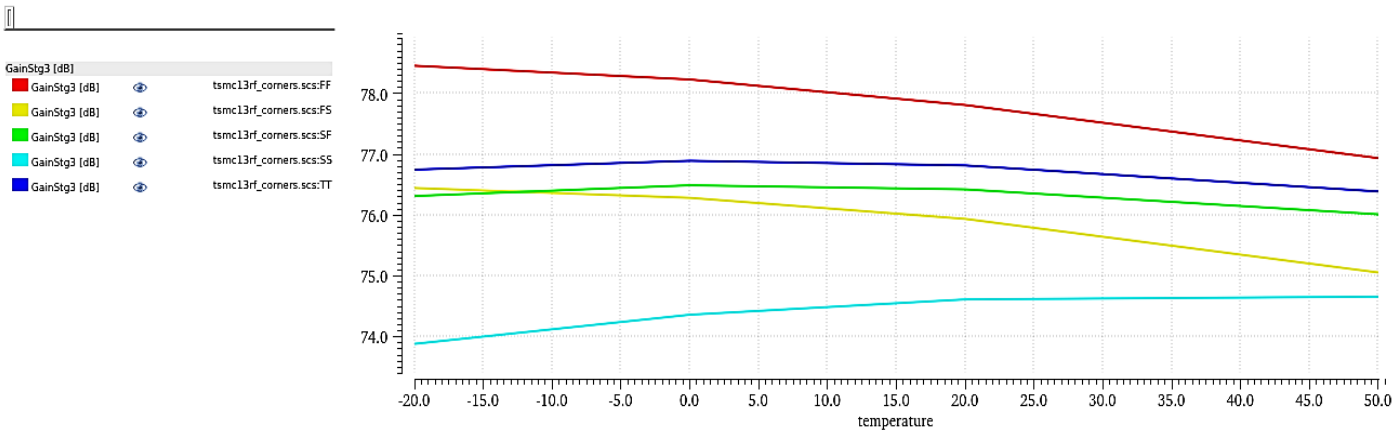

Fig. 90 Comparator gain with corners

Finally, *Fig. 90* shows SF corner has more gain than FS corner. To understand this, we recall that the gain in the amplifiers is linearly dependent on the output resistance. The output resistance is $R_D \,||\, r_{ds,nMOS}$, in both amplifiers. Drain-to-source resistance depends on transistor length ($r_{ds} = \frac{1}{\lambda \, I_d}$), and if slow corner means longer transistor, it makes sense SF corner has bigger gain than FS corner.

Finally, the operating points are working fine for the corners. This guarantees that the comparator will not suffer important performance variations even in the worst conditions.

[6] See Section 2.3.

Fig. 91 illustrates the operating points of the hysteresis block in Typical Transistor corner in room temperature at 1.2 voltage supply.

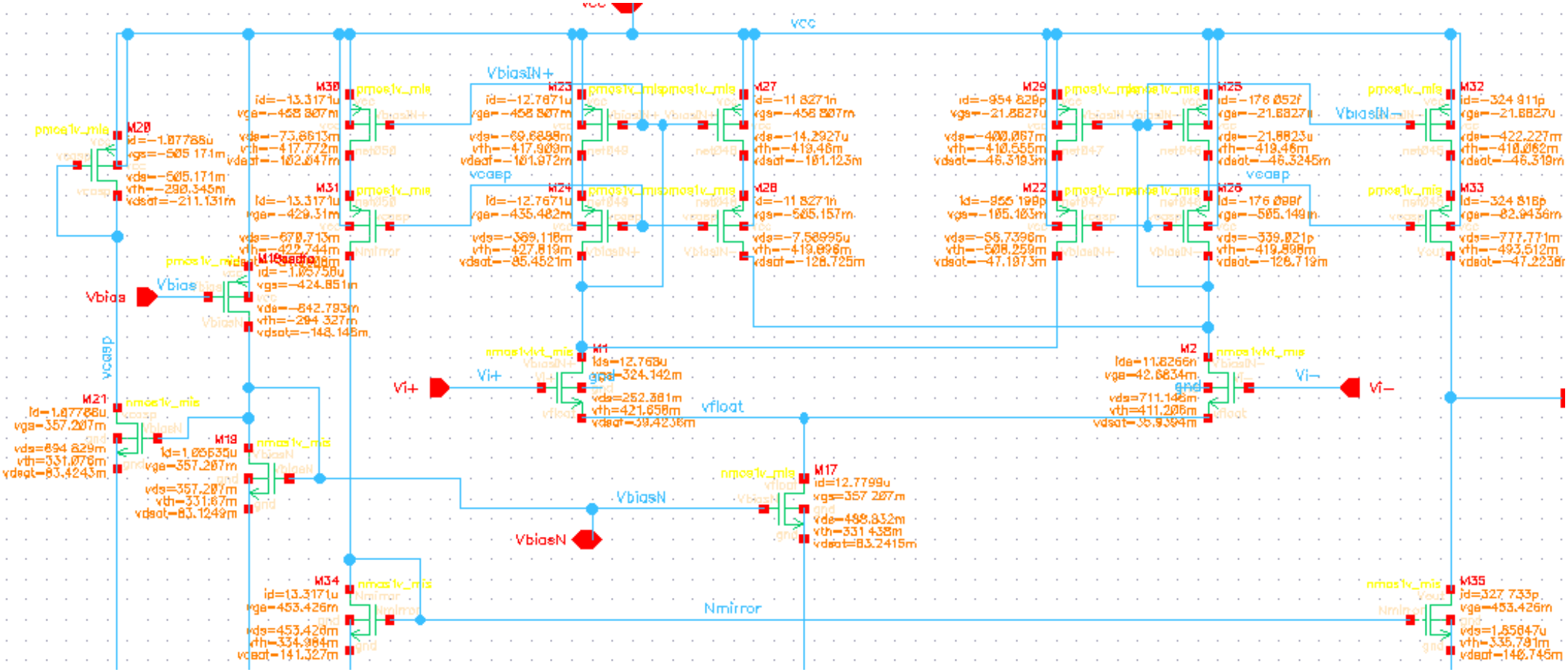

Fig. 91 Operating points of hysteresis block at TT

4.3.4.2. Monte Carlo simulations

As already said in previous chapter, the mismatch is measured using Monte Carlo simulations. *Fig. 92* to *Fig. 95* show the mismatch effects on the delay, hysteresis, power consumption and gain using Monte Carlo simulation histograms.

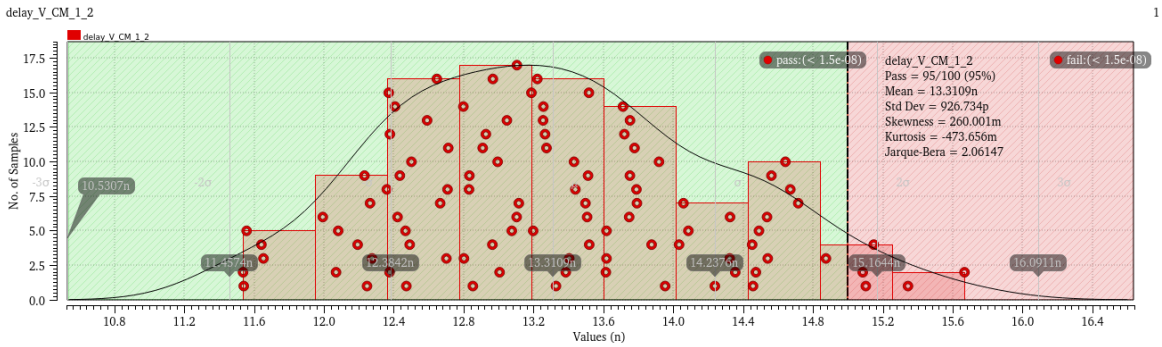

Fig. 92 Mismatch effect on delay

The mean delay is 13.31 ns and standard deviation is 926.73 ps.

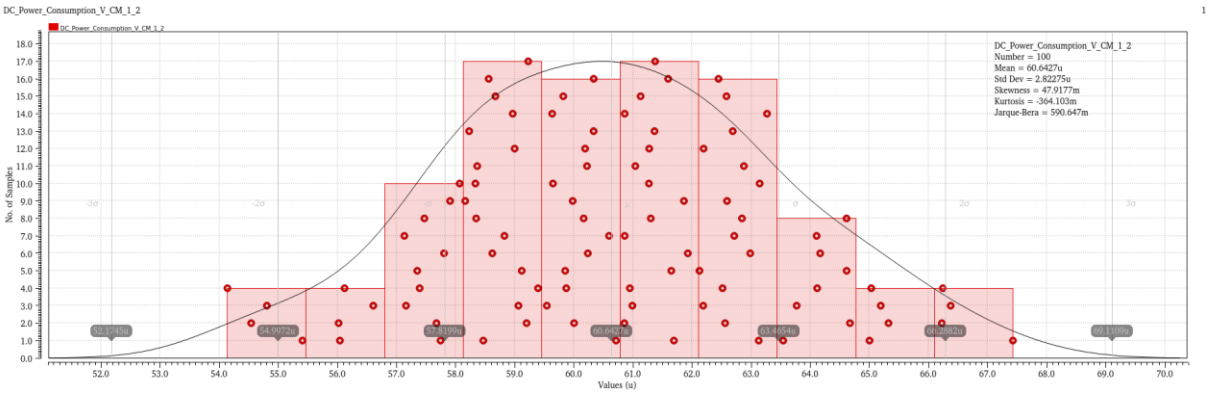

Fig. 93 Mismatch effect on power consumption

The mean power consumption is 60.64 μW and standard deviation is 2.45 μW.

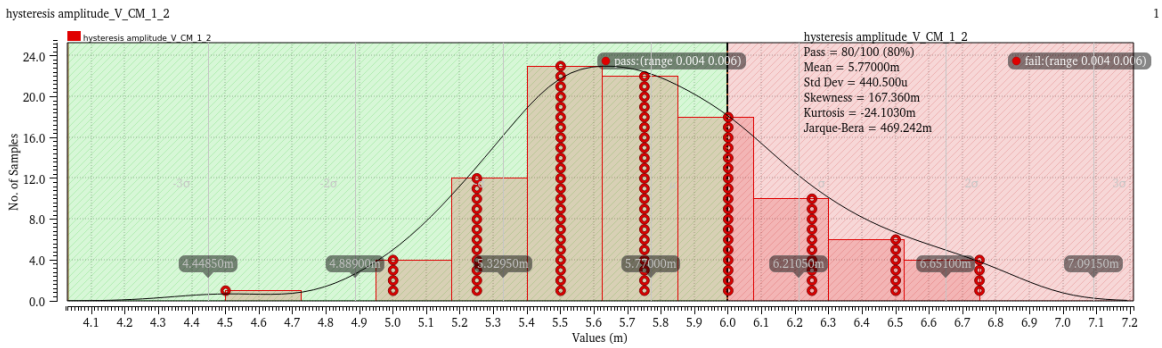

Fig. 94 Mismatch effect on hysteresis amplitude

The mean hysteresis amplitude is 5.77 mV and standard deviation is 440 μV.

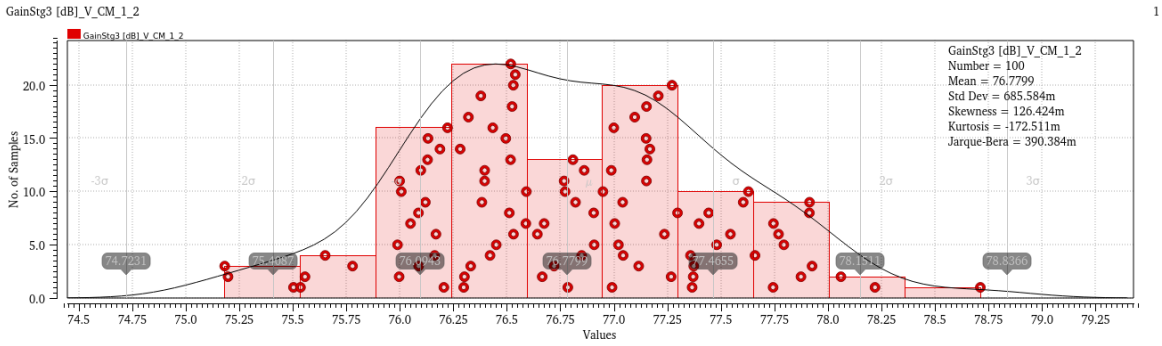

Fig. 95 Mismatch effect on gain

The mean gain is 13.31 ns and standard deviation is 926.73 ps.

We can conclude that the deviations are totally assumable for the ASIC application.

The offset of the comparator against mismatch has also been studied with Monte Carlo simulations. *Fig. 96* to *Fig. 98* the effect of mismatch on the offset of each stage.

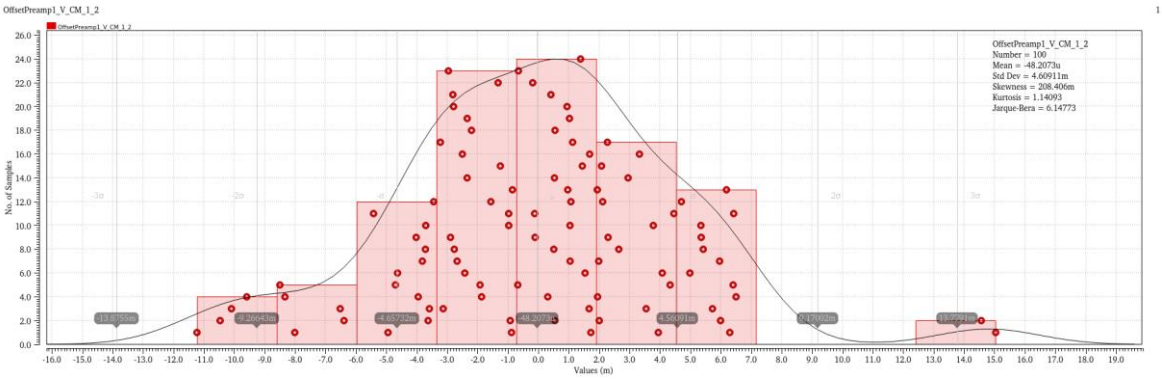

Fig. 96 Mismatch effect on R2R amplifier offset

At the output of first stage, input-referred mean offset is $-48\ \mu V$, with a standard deviation of 4 mV.

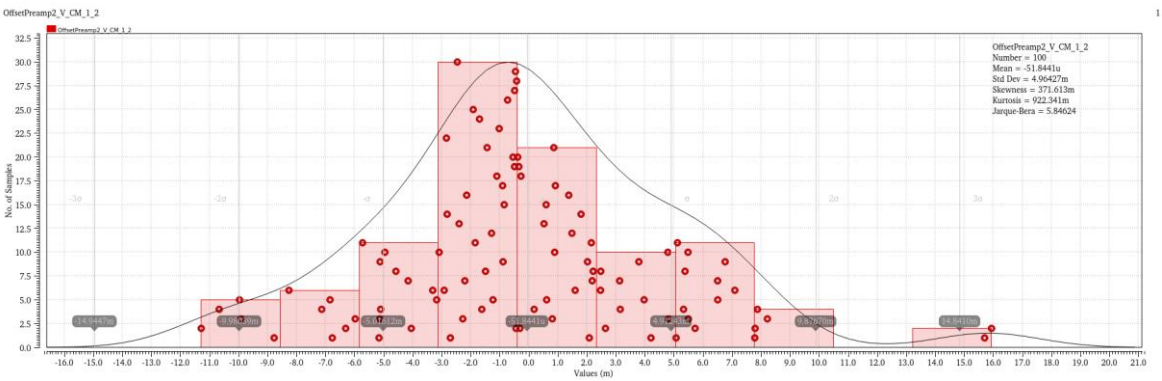

Fig. 97 Mismatch effect on 2nd amplifier offset

At the output of the second amplifier, input-referred mean offset is $-51\ \mu V$, with a standard deviation of 4.96 mV.

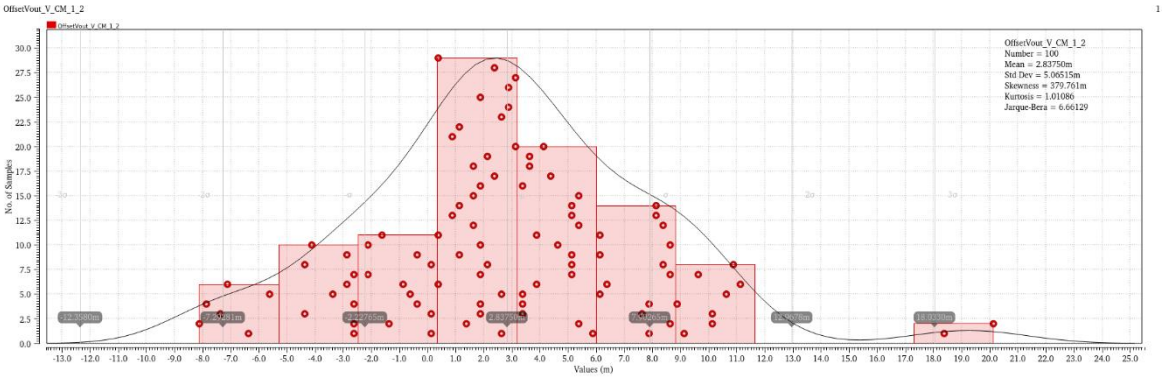

Fig. 98 Mismatch effect on comparator offset

At the output of the comparator, the input-referred mean offset is 2.83 mV, with a standard deviation of 5.06 mV.

Obviously, the mean offset increases in the last stage due to hysteresis. So, the observed offset corresponds to the hysteresis amplitude plus the deviation due to mismatch. Although the offset is significant, this does not imply any resolution loss because the threshold voltage is generated from a DAC which can be calibrated.

4.4. Comparator in real signal

As mentioned in the previous chapter, the noise characterization of the comparator has been done calculating the SNR for 1 photon and measuring the delay and jitter at the output. In this section, the schematic results will be presented, and in Section 4.6.2 the results will be compared with the parasitic extraction. Before that, an example of the signal evolution is illustrated in *Fig. 99-Fig. 102*. Concretely, it is an example of 10 photon input and threshold at 990 mV.

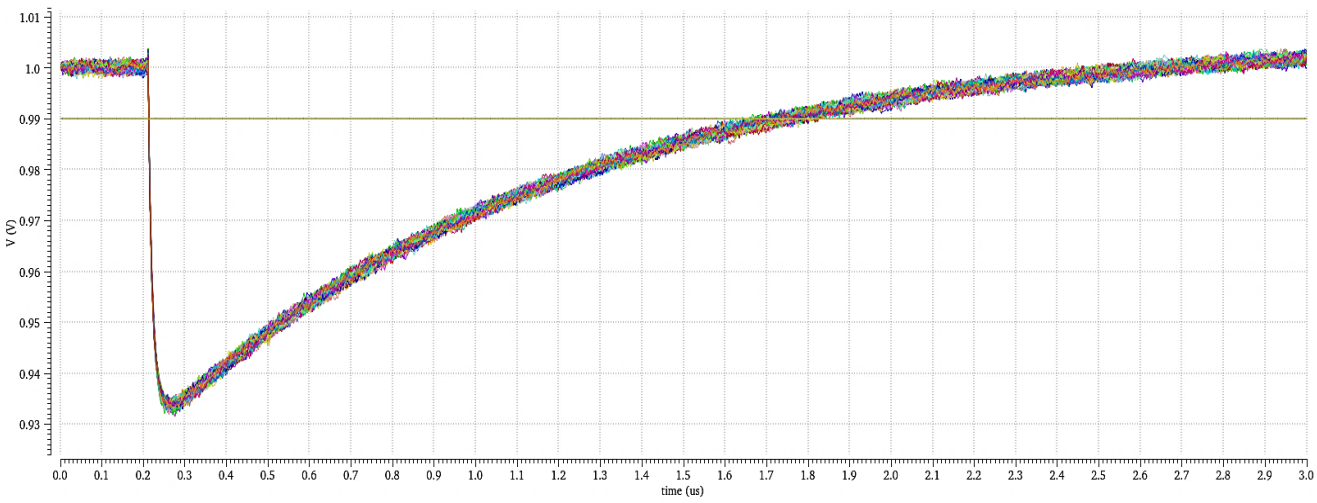

Fig. 99 Input and reference signals

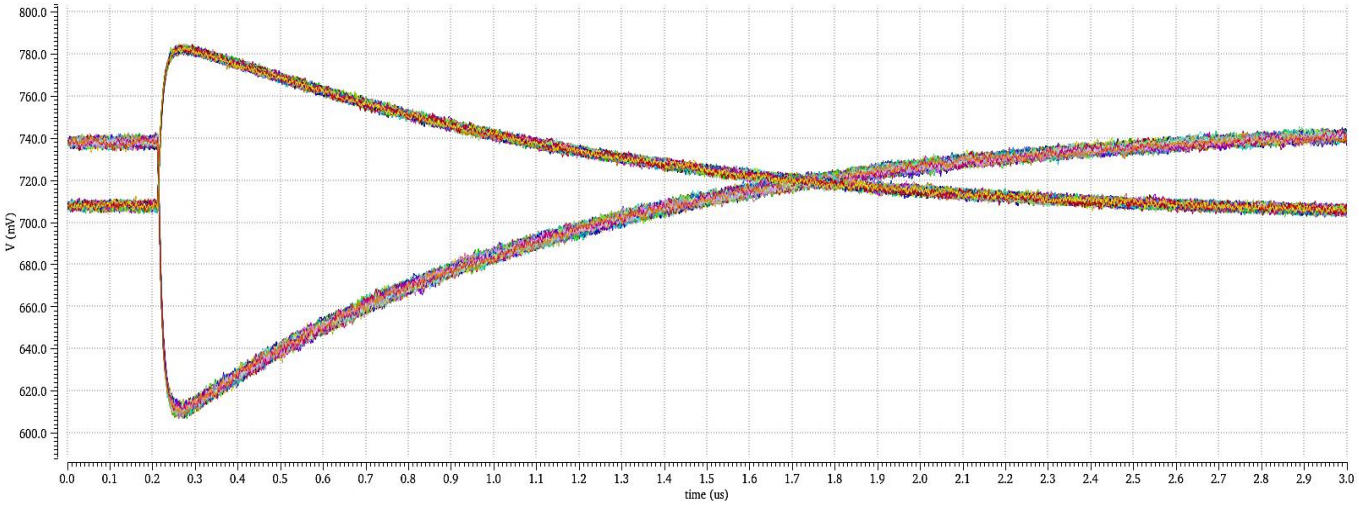

Fig. 100 Stage 1 output differential signals

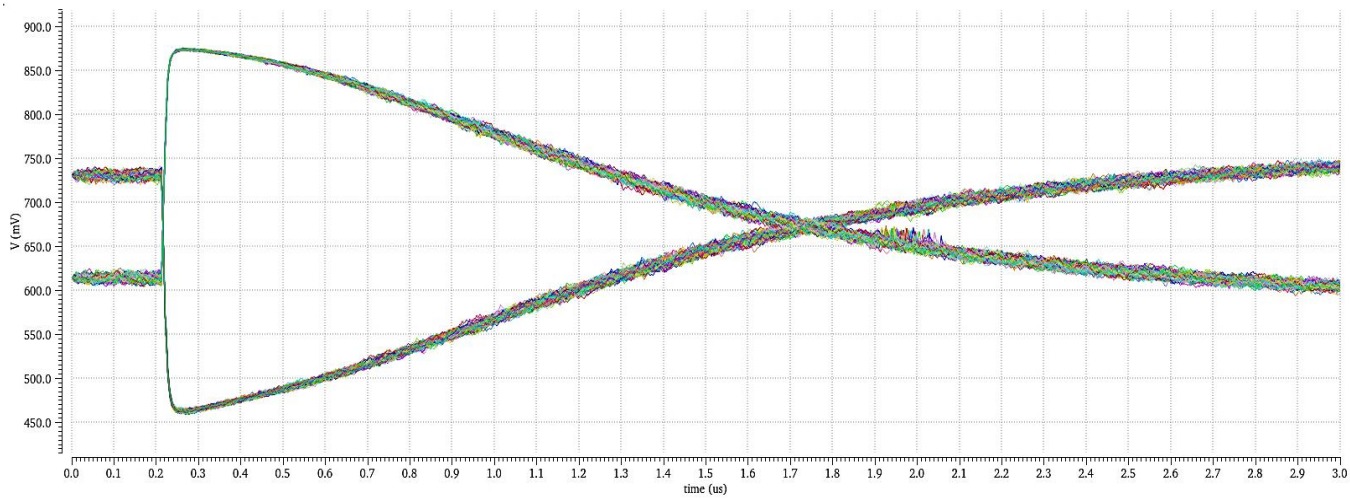

Fig. 101 Stage 2 output differential signals

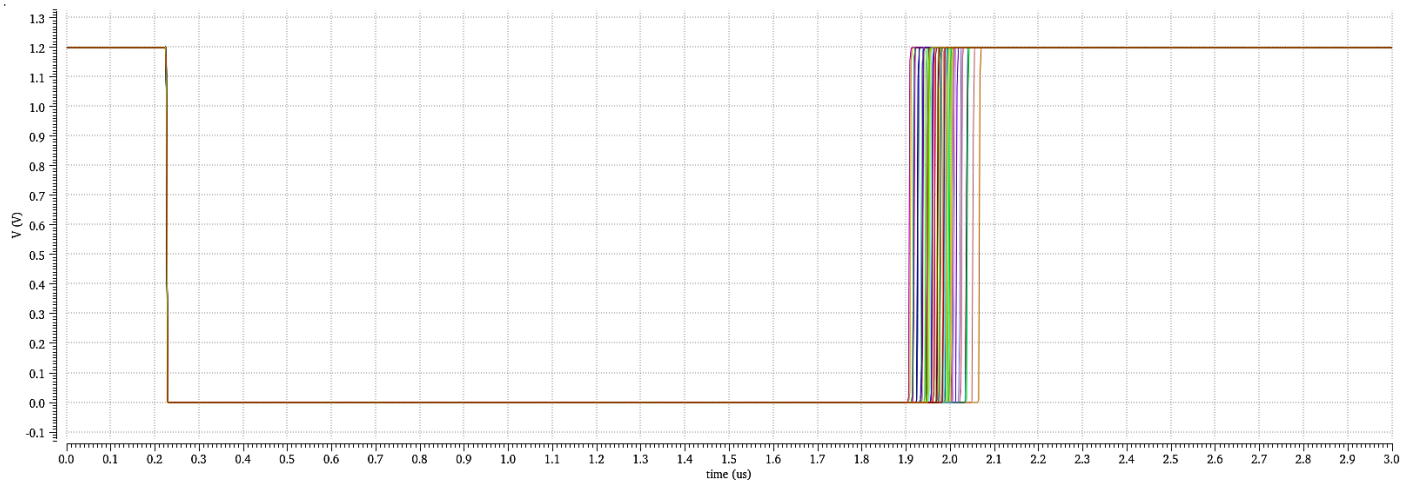

Fig. 102 Comparator output signal

4.4.1. SNR

In the previous chapter, the computing of the SNR to detect 1 photon is explained in detail. The results obtained from the simulations are shown in *Fig. 103*.

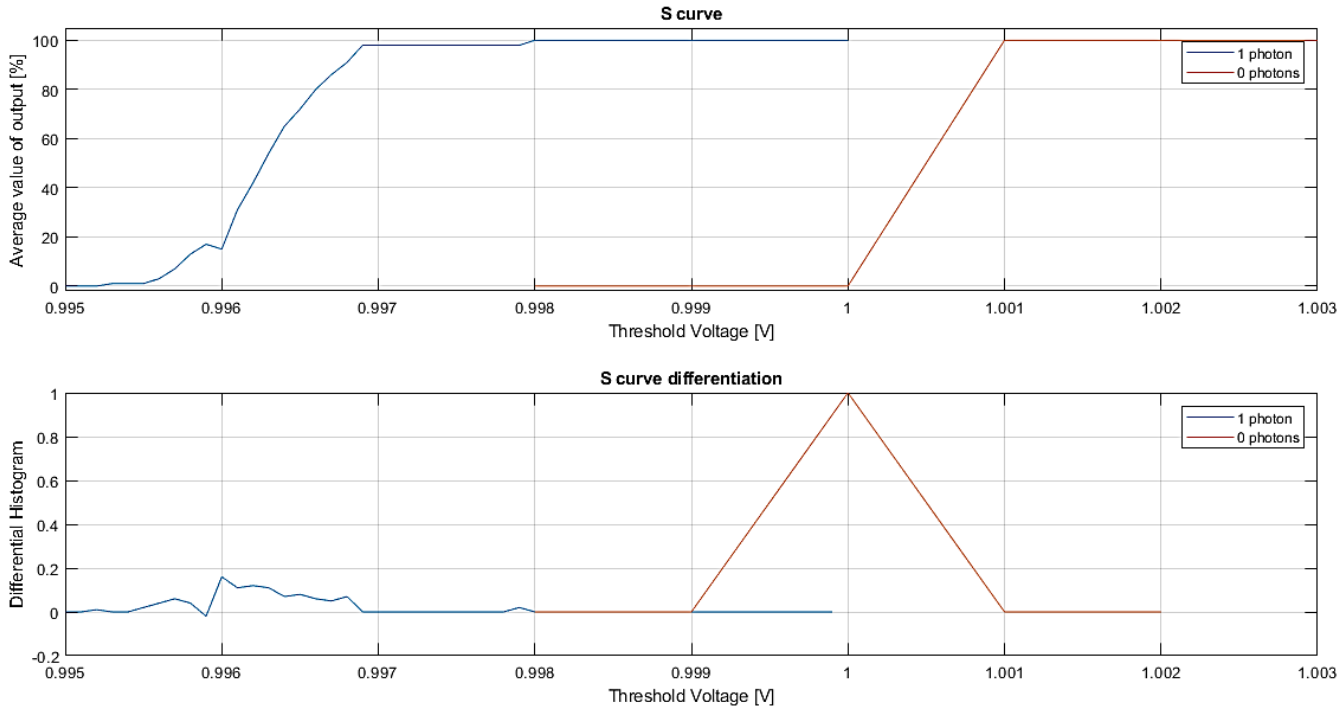

Fig. 103 S curves and differential histogram

The real simulations do not look like the ideal S curves shown in previous paragraph. This is mainly because the timing limitations of the comparator due to its low consumption. However, an approximation can be made to derive the noise statistics, fitting the hsitograms to a normal distribution (*Fig. 104*). The distance between means is $4\,mV$, and assuming the standard deviation of the noise is 0.5, we have an $SNR = 8$, which is more than the minimum required[7].

[7]Actually $SNR \geq 5$ is required for 3.5 photons, so the margin we have is more than enough.

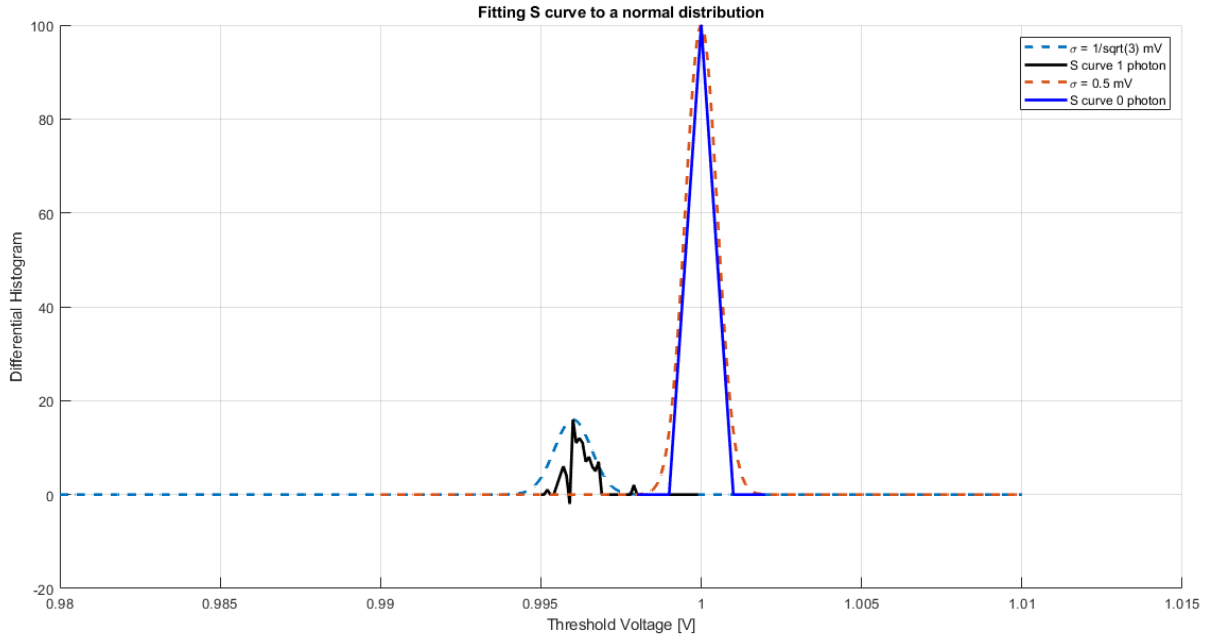

Fig. 104 S curves fitted into normal distribution

4.4.2. Delay and Jitter

First, a threshold scan has been made in order to find the best minimum jitter possible. Second, some threshold values have been fixed -taking into account we want to detect the lowest- the number of events has been swept.

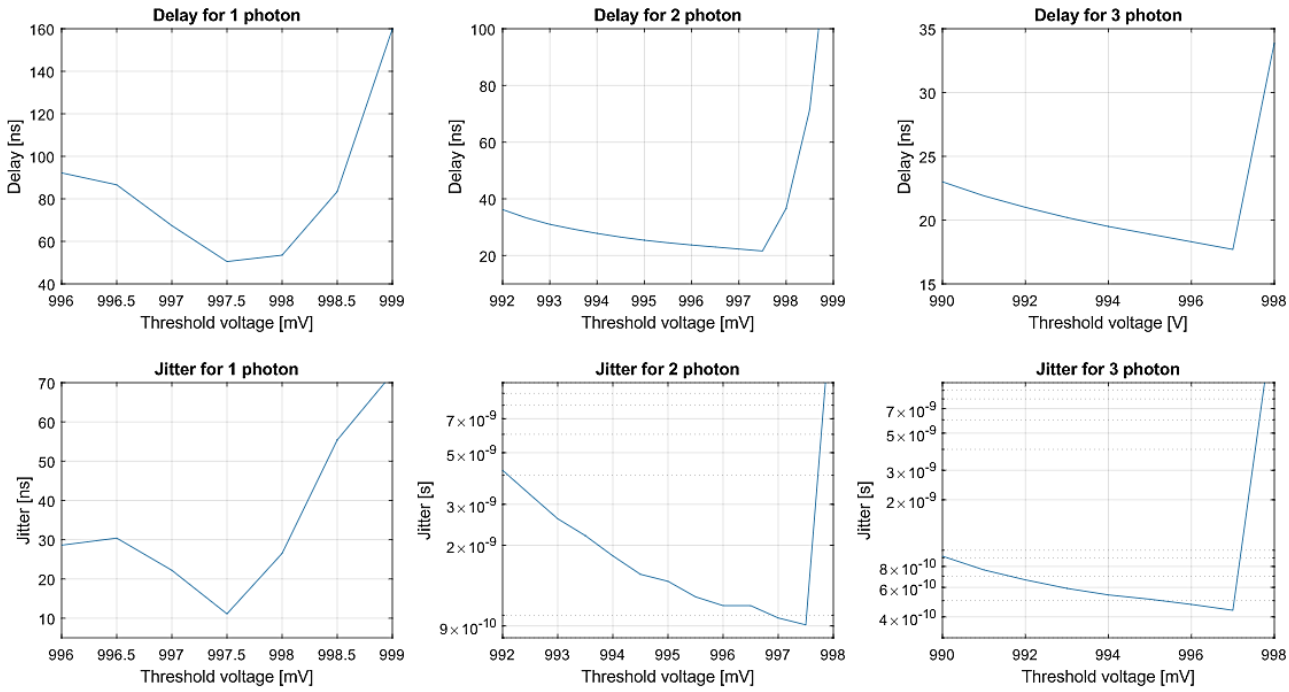

Fig. 105 Threshold scan for 1, 2 and 3 photons

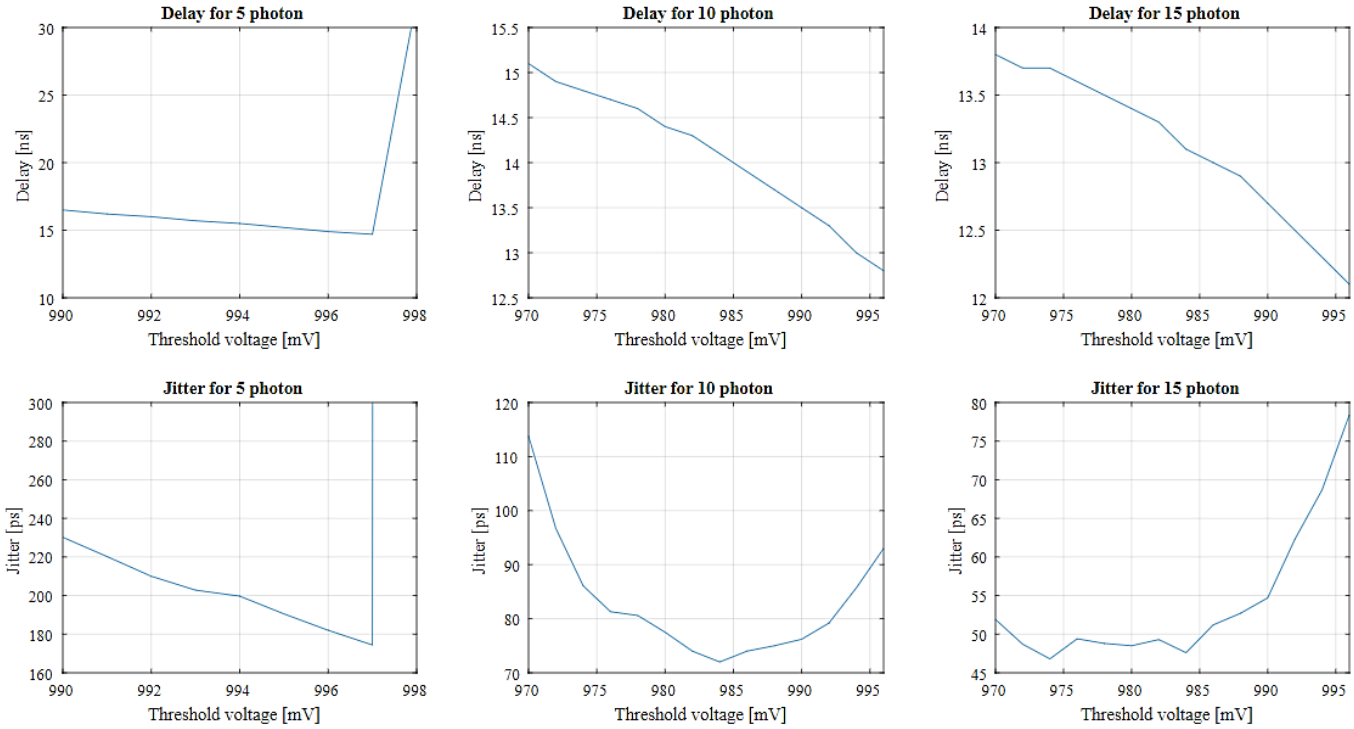

Fig. 106 Threshold scan for 5, 10 and 15 photons

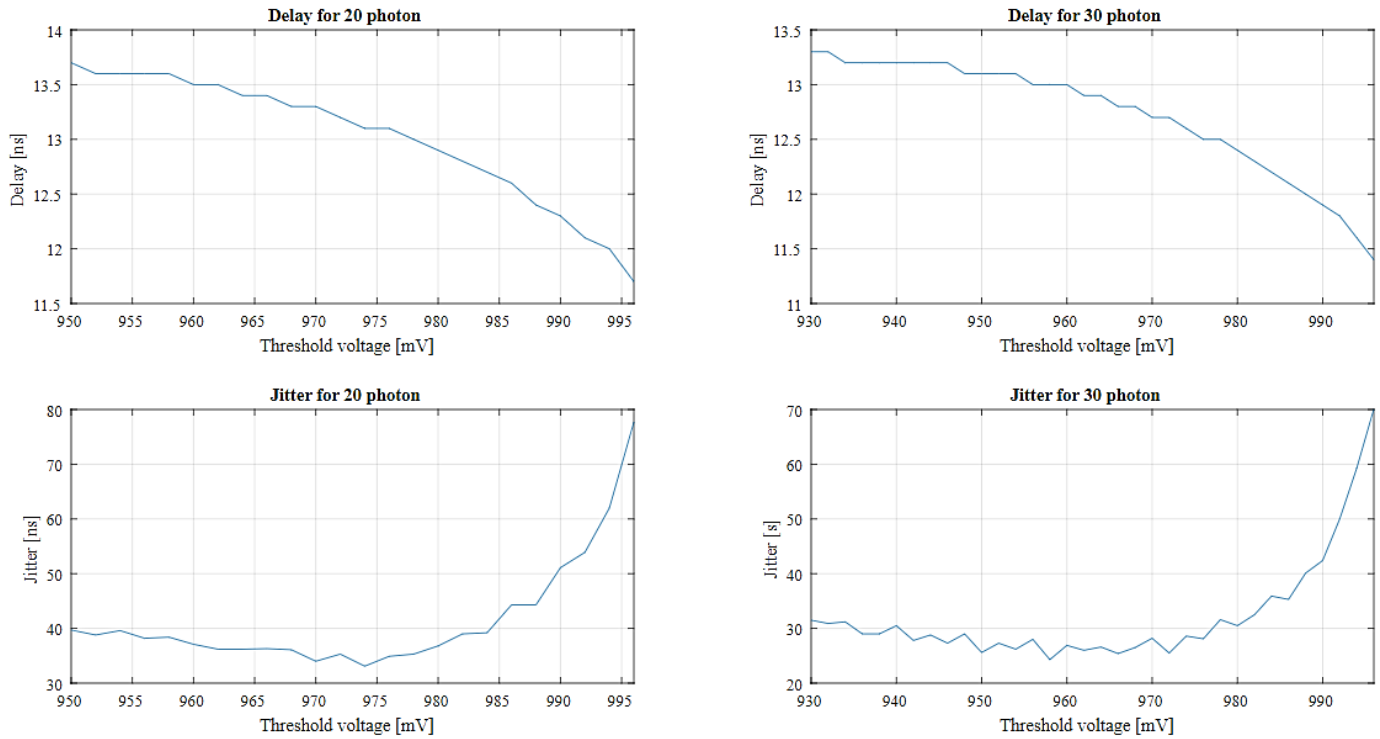

Fig. 107 Threshold scan for 20 and 30 photons

From *Fig. 105, Fig. 106* and *Fig. 107* we learn that for low energies, the delay and jitter are very high, which is understandable since we are playing with a low power comparator. For energies higher than 10 photons, delay decreases below 15 ns, and the jitter is below 100 ps which accomplishes the specifications.

In the second part of the analysis the number of events is swept choosing some relevant threshold voltages.

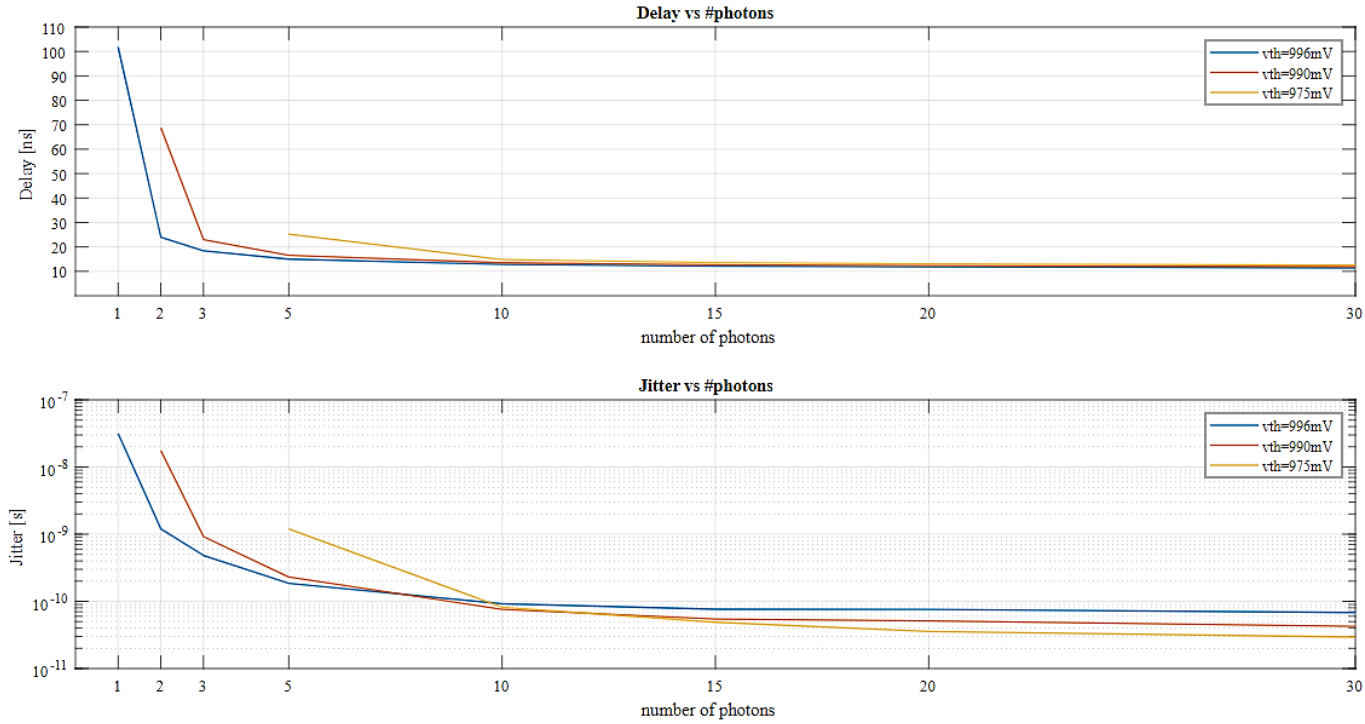

Fig. 108 Delay and Jitter for different threshold voltages

Fig. 108 shows 975 mV threshold is more appropriate for higher number of events. However, the threshold is required to be nearer the baseline in order to detect the lower energies. Besides, all threshold values guarantee the jitter is below 100 ps at 10 events.

Finally, the following *Table 4* sums up the most meaningful results.

	$V_{th} = 975mV$		$V_{th} = 990\ mV$		$V_{th} = 996\ mV$	
nEvent	**Delay**	**Jitter**	**Delay**	**Jitter**	**Delay**	**Jitter**
1	/	/	/	/	101.8 ns	31.4 ns
2	/	/	68.7 ns	17.5 ns	24 ns	1.2 ns
3	/	/	23 ns	920.9 ps	18.4 ns	483.5 ps
5	25.2 ns	1.2 ns	16.5 ns	230.2 ps	15 ns	184.7 ps
10	14.8 ns	81.6 ps	13.5 ns	76.2 ps	12.8 ns	92 ps
15	13.6 ns	48.9 ps	12.7 ns	54.7 ps	12.1 ns	76.4 ps
20	13.1 ns	35.6 ps	12.3 ns	51.1 ps	11.8 ns	75.9 ps
30	12.6 ns	29.4 ps	11.9 ns	42.4 ps	11.4 ns	68.1 ps

Table 4 Summary of results for delay and jitter

4.5. Comparator Layout

Fig. 109 and *Fig. 110* show first stage schematic and layout, respectively. The area of the layout is 41.63 x 30.53 μm^2 (height x width).

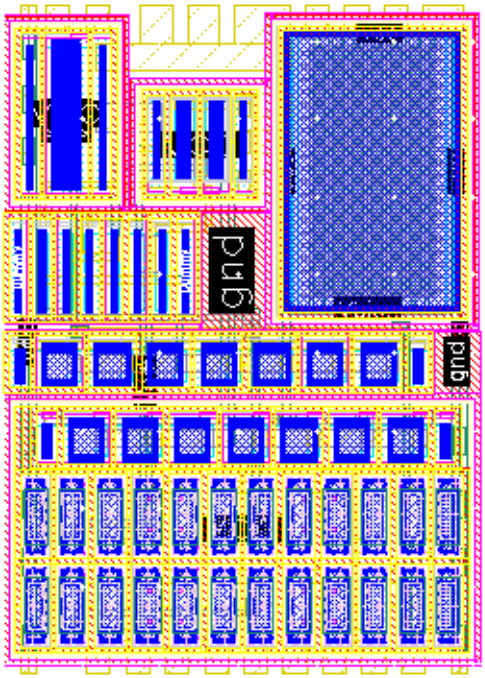

Fig. 110 R2R input FDA (1st Stage) layout

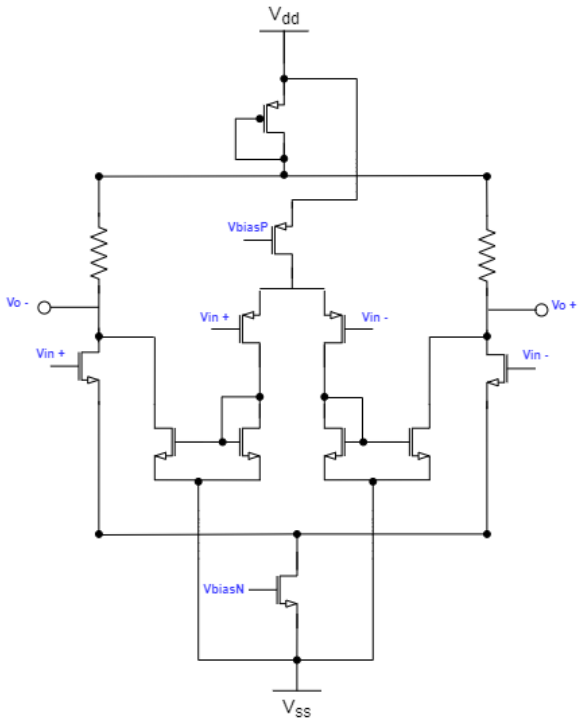

Fig. 109 First stage schematic

Fig. 111 and *Fig. 112* show the schematic and layout of the 2nd stage, respectively. The total area of the layout is 58.38 x 20.82 μm^2.

Fig. 113 and *Fig. 114* show the layout and schematic of the hysteresis block, respectively. The total area of the layout is 58.92 x 23.58 μm^2.

Fig. 115 and *Fig. 116* show the layout and schematic of the hysteresis block, respectively. The total area of the layout is 9.65 x 5.97 μm^2.

Fig. 117 illustrates the whole comparator layout. The total area it takes is 58.97 x 75.78 μm^2.

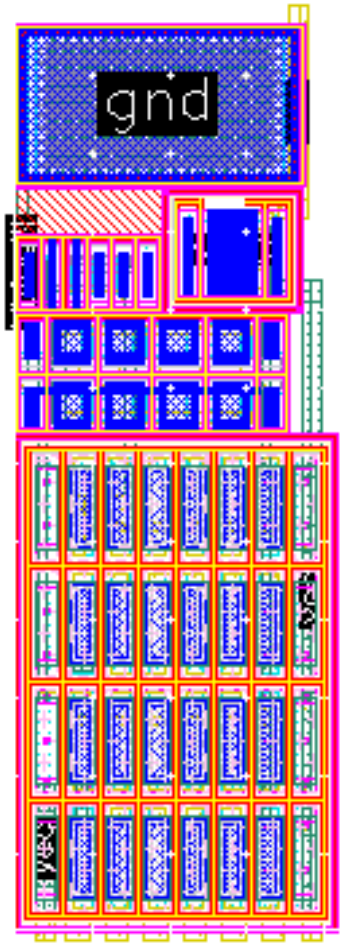

Fig. 112 FDA (2nd Stage) layout

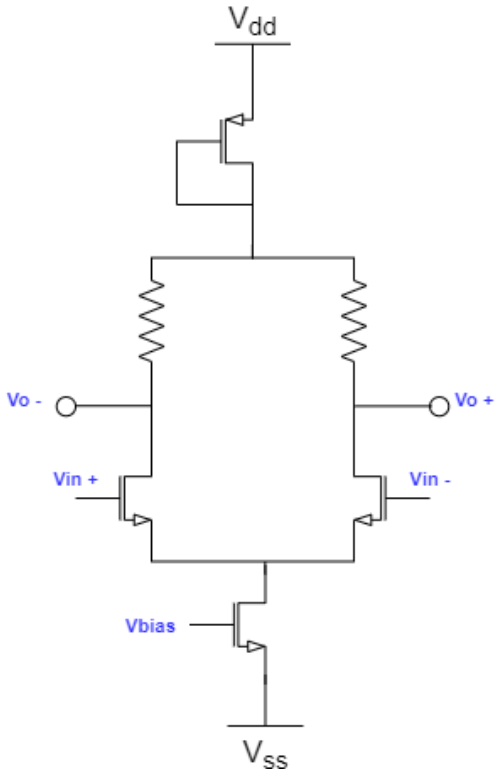

Fig. 111 2nd stage schematic

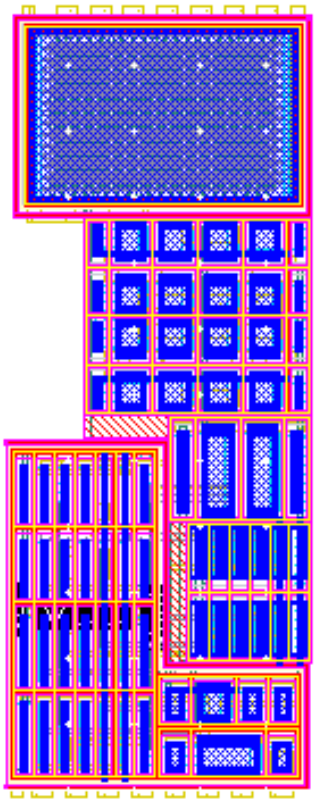

Fig. 114 Hysteresis comparator layout

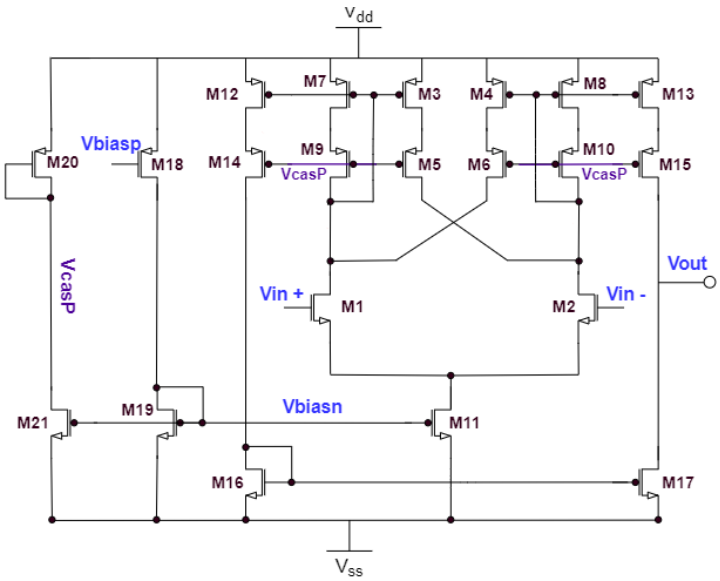

Fig. 113 hysteresis block schematic

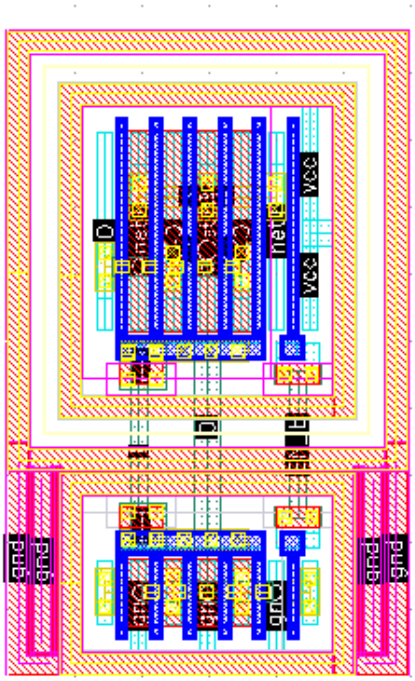

Fig. 116 NOR gate layout

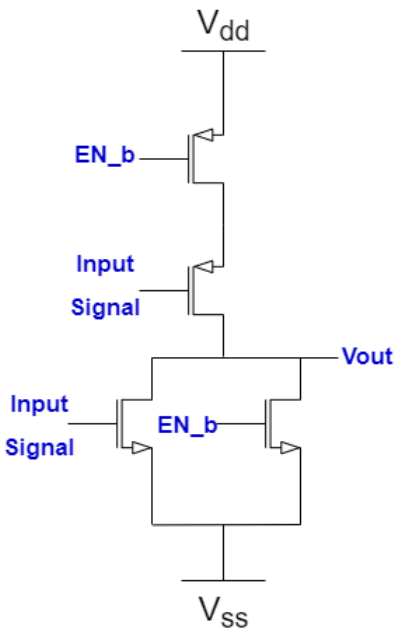

Fig. 115 NOR gate schematic

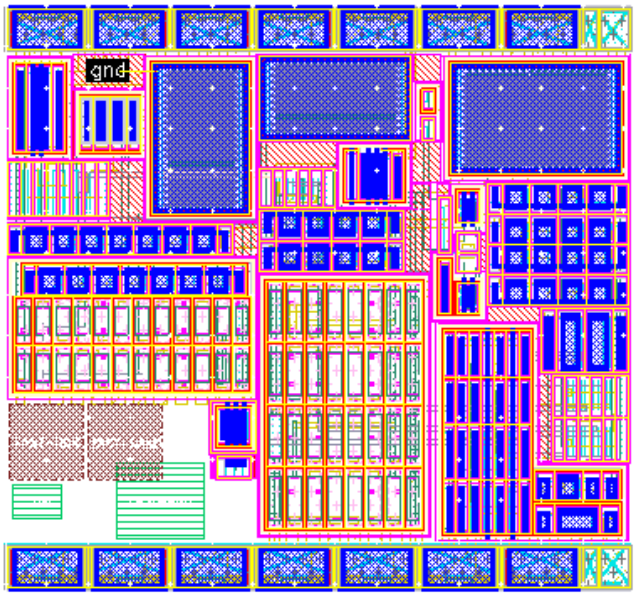

Fig. 117 Whole comparator layout

4.6. Comparator in extraction

4.6.1. Standalone

Table 5 illustrates the deviation of the specs with respect to the schematic nominal values. Although we see that the delay is higher than 15 ns, the trigger comparator is accurate enough for the ASIC application. The rest of parameters change very little, which is a positive conclusion.

Specs	Schematic	Extracted
Delay	*13.21 ns*	*15.17 ns*
Rise time	*1.076 ns*	*1.335 ns*
Fall time	*1.116 ns*	*1.478 ns*
Power Consumption Stg1	16.56 μW	/
Power Consumption Stg2	*10.14 μW*	/
Power Consumption Stg3	*33.88 μW*	/
Total Power Consumption	*60.59 μW*	*60.61 μW*
Total gain	*76.35 dB*	*76.84 dB*
Hysteresis amplitude	*5.75 mV*	*5.75 mV*
Gain Stg1	9.25 *dB*	*9.384 dB*
Gain Stg1to2	11.68 *dB*	*11.91 dB*
Gain Stg2to3	55.43 *dB*	*55.46 dB*
Bandwidth Stg1	*112 MHz*	*99.89 MHz*
Bandwidth Stg2	*65 MHz*	*50.39 MHz*
Bandwidth Stg3	*91 KHz*	*66.19KHz*
GBW	*97.5461 MHz*	*83.6424 MHz*

Table 5 Comparison specs in schematic and extracted

4.6.2. Real Signal

In this section, the effect of parasites on previously computed noise measurements is discussed. The *SNR* measurement is illustrated in *Fig. 118* and *Fig. 119.*

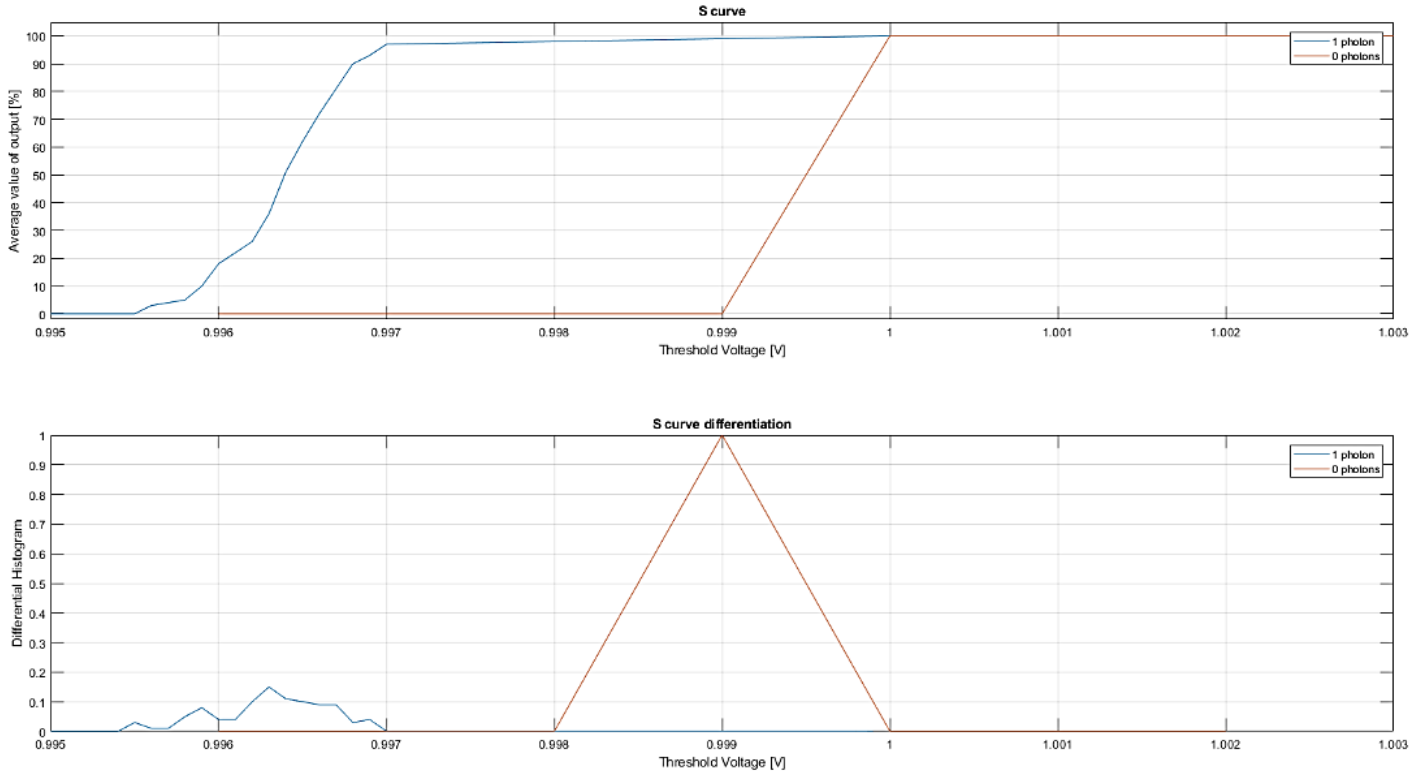

Fig. 118 S curve and differential histogram of the comparator with extracted parasitics

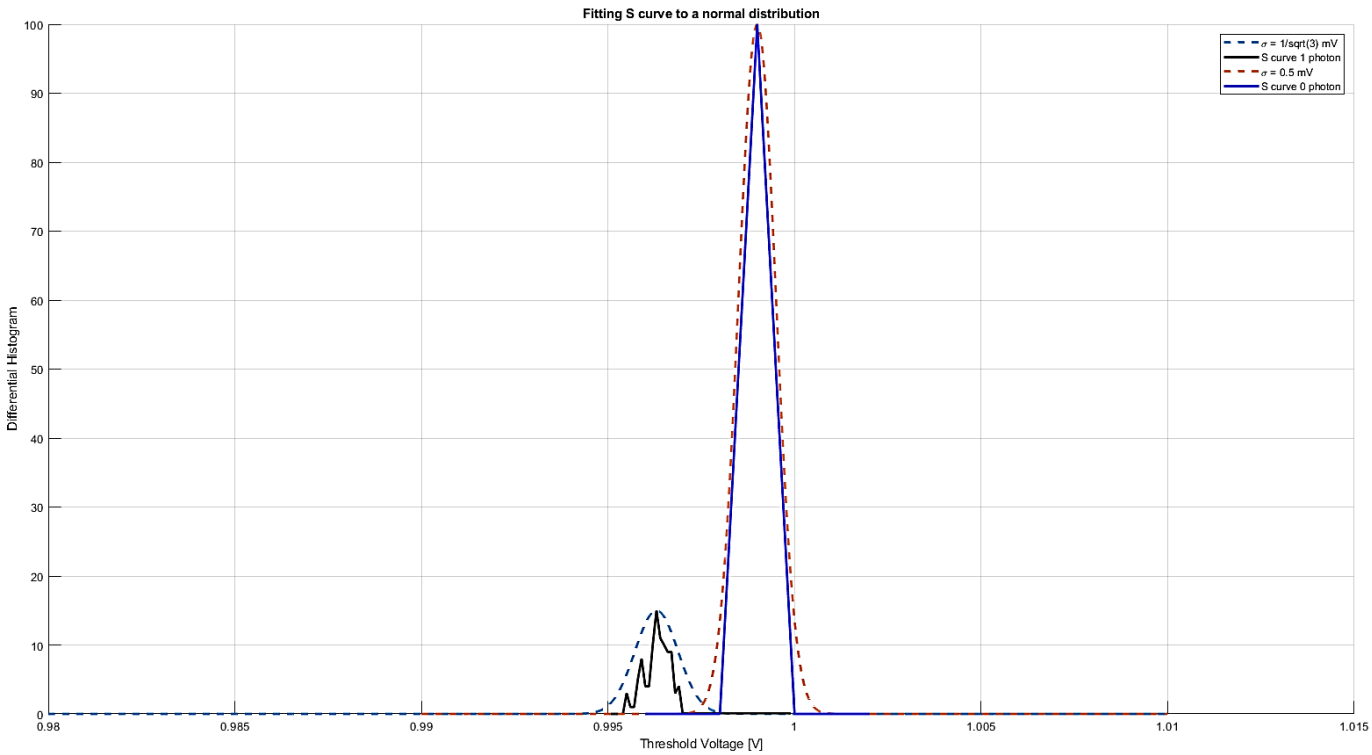

Fig. 119 Fitting histogram to a normal distribution

The distance between means is 3 mV, and assuming the standard deviation of the noise is 0.5, we have an $SNR = 6$.

Finally, delay and jitter are for 975 mV, 990 mV *and* 996 mV threshold.

Table 6, *Table 7* and *Table 8* show the comparison between the schematic and extracted results for jitter and delay.

Vth = 975 mV				
nEvent	Schematic		Extracted	
	Delay	Jitter	Delay	Jitter
1	/[8]	/	/	/
2	/	/	/	/
3	/	/	/	/
5	25.2 ns	1.2 ns	28.6 ns	1.5 ns
10	14.8 ns	81.6 ps	16.7 ns	95.6 ps
15	13.6 ns	48.9 ps	15.4 ns	55.9 ps
20	13.1 ns	35.6 ps	14.9 ns	46.7 ps
30	12.6 ns	29.4 ps	14.3 ns	38.5 ps

Table 6 Jitter and delay for $v_{th} = 975mV$

Vth = 990 mV				
nEvent	Schematic		Extracted	
	Delay	Jitter	Delay	Jitter
1	/	/	/	/
2	68.7 ns	17.5 ns	81.3 ns	21.3 ns
3	23 ns	920.9 ps	25.8 ns	1.1 ns
5	16.5 ns	230.2 ps	18.5 ns	221.7 ps
10	13.5 ns	76.2 ps	15.3 ns	81.2 ps
15	12.7 ns	54.7 ps	14.4 ns	61.6 ps
20	12.3 ns	51.1 ps	14 ns	54.8 ps
30	11.9 ns	42.4 ps	13.6 ns	47.2 ps

Table 7 Jitter and delay for $v_{th} = 990\ mV$

For 975 mV delay increases by an amount of 13%. The jitter increases 30% for 5, 20 and 30 photons, and 15% for 10 and 15 photons.

For 990 mV delay increases by an amount of 13% as well. There is no a recognisable pattern on the jitter, but it increases between 10 to 20%.

[8] Not detected

Vth = 996 mV				
nEvent	Schematic		Extracted	
	Delay	Jitter	Delay	Jitter
1	101.8 ns	31.4 ns	99 ns	23.3 ns
2	24 ns	1.2 ns	26.8 ns	1.1 ns
3	18.4 ns	483.5 ps	20.6 ns	443.9 ps
5	15 ns	184.7 ps	16.9 ns	177.9 ps
10	12.8 ns	92 ps	14.5 ns	93.3 ps
15	12.1 ns	76.4 ps	13.8 ns	78.1 ps
20	11.8 ns	75.9 ps	13.4 ns	73.6 ps
30	11.4 ns	68.1 ps	13.1 ns	67.2 ps

Table 8 Jitter and delay for $v_{th} = 996\ mV$

For 996 mV delay increases by an amount of 13% as well. The jitter is so similar that the variation may be due to statistical error in simulation.

4.7. Comparator in Channel

Finally, there has been time to analyse the noise of the comparator inside the channel.

Fig. 120 and *Fig. 121* show the single-photon SNR measurement.

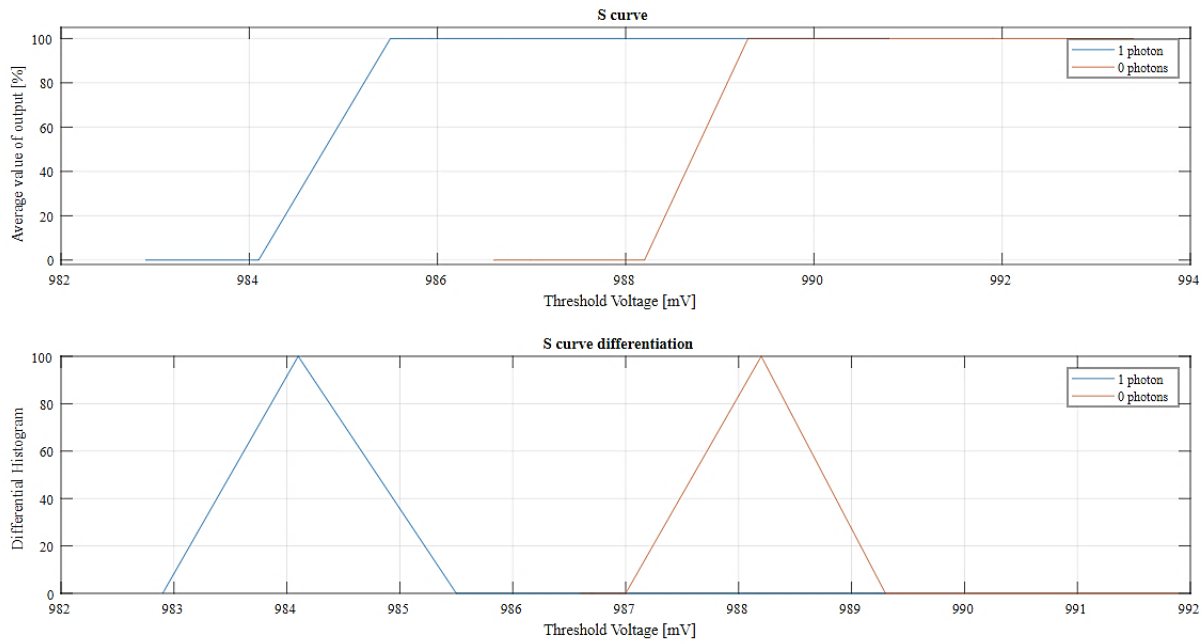

Fig. 120 S curves in channel schematic

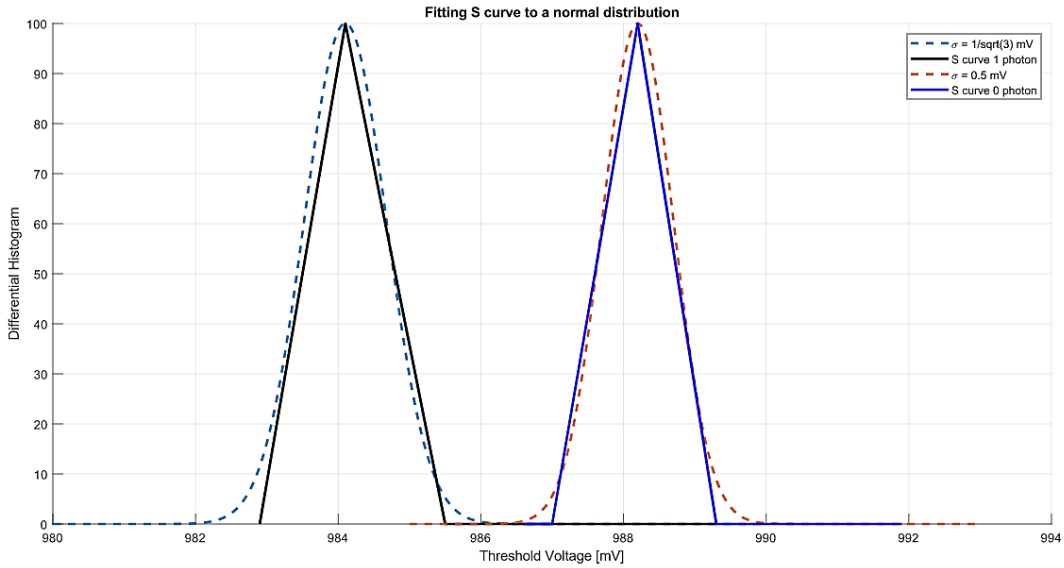

Fig. 121 Fitting to a distribution in channel schematic

The distance between means is 4 mV, and assuming the standard deviation of the noise is 0.5, we have an $SNR = 8$, which is more than the minimum required.

Table 9 shows the results of delay and jitter for the channel in schematic

	$V_{th} = 975mV$		$V_{th} = 990\ mV$		$V_{th} = 996\ mV$	
nEvent	**Delay**	**Jitter**	**Delay**	**Jitter**	**Delay**	**Jitter**
1	/	/	/	/	*224 ns*	/
2	/	/	*85.6 ns*	*23 ns*	*25.3 ns*	*2.3 ns*
3	/	/	*26.8 ns*	*2.8 ns*	*18.2 ns*	*550.4 ps*
5	*35.9 ns*	*6.4 ns*	*16.3 ns*	*271.9 ps*	*14.8 ns*	*166.4 ps*
10	*14.4 ns*	*95.3 ps*	*13.4 ns*	*66.7 ps*	*12.9 ns*	*78.5 ps*
15	*13.2 ns*	*42.9 ps*	*12.7 ns*	*50.2 ps*	*12.3 ns*	*68.2 ps*
20	*12.8 ns*	*36.7 ps*	*12.4 ns*	*44.1 ps*	*12 ns*	*62.8 ps*
30	*12.4 ns*	*31.4 ps*	*12 ns*	*38.3 ps*	*11.7 ns*	*61.1 ps*

Table 9 Delay and jitter in channel (Schematic)

In general, the delay and jitter follow the same trend as the results in standalone.

On the other hand, channel extraction gives the most realistic results possible, and we are glad the noise performance does not degrade too much for the application the ASIC is required.

Fig. 122 and *Fig. 123* repeat the SNR measurement with the channel in extraction.

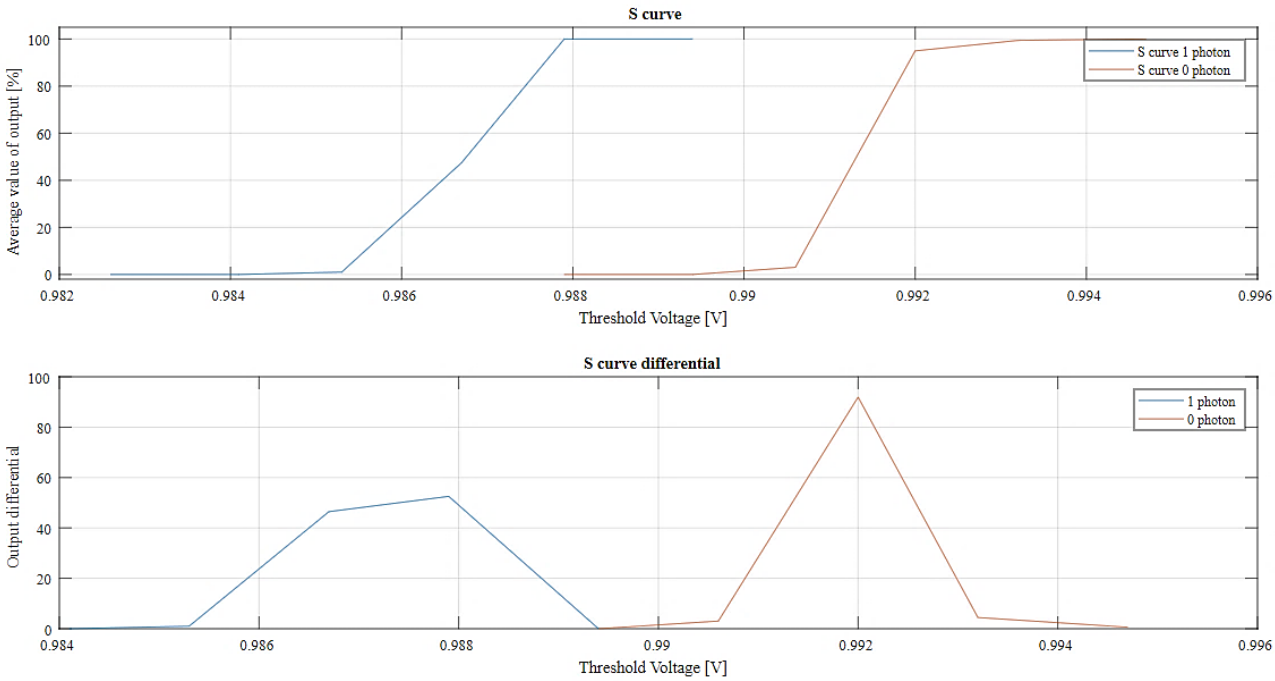

Fig. 123 S curves channel in extraction

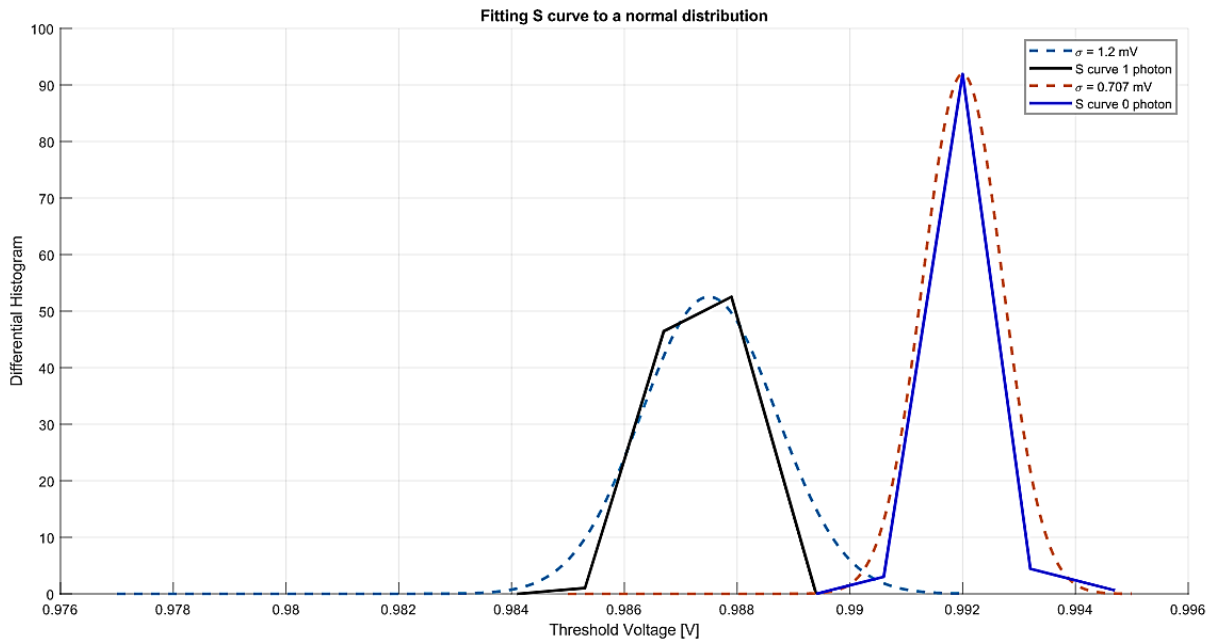

Fig. 122 Distribution fitting for channel in extraction

The distance between means is around 5 mV, and assuming the standard deviation of the noise is 0.5, we have an $SNR\ around$ 10. These results have some uncertainty, though: the resolution of the DAC that generates the threshold voltage is bigger than 1 mV and the comparators speed to follow the noise is limited. However, the qualitative information we can obtain is useful, to verify that the single-photon SNR measurement follows the same trend as in standalone noise analysis. Finally, *Table 10* and *Table 11* show the delay and jitter of the comparator inside the channel considering parasites.

	Vth = 975 mV				Vth = 990 mV			
nEvent	Channel (schematic)		Channel (schematic)		Channel (extraction)		Channel (schematic)	
	Delay	Jitter	Delay	Jitter	Delay	Jitter	Delay	Jitter
1	/	/	/	/	/	/	/	/
2	/	/	/	/	85.6 ns	23 ns	90.3 ns	25.7 ns
3	/	/	/	/	26.8 ns	2.8 ns	40 ns	2.2 ns
5	35.9 ns	6.4 ns	30.4 ns	1.6 ns	16.3 ns	271.9 ps	19.68 ns	558.7 ps
10	14.4 ns	95.3 ps	17.61 ns	101.6 ps	13.4 ns	66.7 ps	16.4 ns	76.59 ps
15	13.2 ns	42.9 ps	16.19 ns	61.6 ps	12.7 ns	50.2 ps	15.56 ns	56.34 ps
20	12.8 ns	36.7 ps	15.67 ns	44.7 ps	12.4 ns	44.1 ps	15.17 ns	48.01 ps
30	12.4 ns	31.4 ps	15.23 ns	33.23 ps	12 ns	38.3 ps	14.81 ns	44.51 ps

Table 10 Jitter and delay for $v_{th} = 975mV$ $v_{th} = 990mV$

Vth = 996 mV				
nEvent	Channel (schematic)		Channel (extraction)	
	Delay	Jitter	Delay	Jitter
1	*224 ns*	*/*	*/*	*/*
2	*25.3 ns*	*2.3 ns*	*33.94 ns*	*3.819 ns*
3	*18.2 ns*	*550.4 ps*	*22.71 ns*	*869.3 ps*
5	*14.8 ns*	*166.4 ps*	*18.21 ns*	*238.4 ps*
10	*12.9 ns*	*78.5 ps*	*15.77 ns*	*87.99 ps*
15	*12.3 ns*	*68.2 ps*	*15.01 ns*	*66.93 ps*
20	*12 ns*	*62.8 ps*	*14.64 ns*	*65.8 ps*
30	*11.7 ns*	*61.1 ps*	*14.27 ns*	*64.25 ps*

Table 11 Jitter and delay with $v_{th} = 996mV$

As expected, the final results in extraction are worse than in the schematic. However, they do not diverge in a significant way. These results reaffirm the validity of previous measurements made in standalone.

5. Conclusions and future development

In this Master Thesis, a low power comparator has been designed for the BETA ASIC that will go onboard the HERD experiment. The ASIC has been designed in TSMC **130 *nm*** technology. The comparator has a rail-to-rail input and hysteresis feedback. The main requirements are the minimum delay possible, maximised the gain, a hysteresis amplitude around $4 - 6\ mV$ and a consumption around 50 μW. As an extension, the basing circuit of the comparator has also been designed, the current DAC.

The theoretical analysis and initial transistor level design is followed by the simulations with ideal input signals. The specifications mentioned above have been considered for all the common modes to ensure similar operation. Moreover, the comparator has been tested with a realistic model of the SiPM to measure the single-photon SNR and noise jitter.

After the measurements, the comparator has been adjusted to guarantee uniform behaviour against variations in process (corner simulations), temperature, voltage supply and mismatch.

The layout has been designed using different techniques to avoid nearby transistors behave different and the routing has been done in lower metals to maximise the available resources.

The post layout simulations reaffirm the previous simulation results, because there are no important deviations from standalone simulations. Despite the power limitation, the comparator has a 76 dB gain and the delay is around 15 ns for input energies higher than 10 pe. The jitter is below 100 ps for energies higher than 10 pe, as well.

After the complete characterization of the comparator and the rest of the blocks in the ASIC, an initial 16-channel prototype was sent to manufacture in April. The final version, consisting of 64 channels, will be delivered after the verification of the initial prototype, with the corresponding adjustments. Since the delay and the jitter have only been tested for TT corner, further tuning of the comparator may be possible analysing the noise for more corners. In any case, with the results we have it can be said that the comparator works with a high degree of reliability.

During the 9 months that the project has taken, I have assisted to regular weekly meetings with ICC staff. Besides, I participated in occasional meetings with other research centres involved in the project, and even briefly exposed simulation results and relevant comments about the performance of the comparator.

6. Bibliography

[1] A. Comerma, D. Gascon, S. Gomez, and A. Sanmukh, HERD-FiBre TrackEr ReadouT Asic (BETA) Specifications Document Revision History VER 1.0 Initial Version, 2019.

[2] P. Hopchev, *SciFi: A Large Scintillating Fibre Tracker for LHCb*, Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip. **845**, 481 (2017).

[3] D. Sanchez, S. Gomez, D. Gascon, L. Garrido, R. Graciani, R. Manera, J. Mauricio, A. Sanmukh, and P. Garcia, *Multimodal Simulation of Large Area Silicon Photomultipliers for Time Resolution Optimization*, in *2019 IEEE Nuclear Science Symposium and Medical Imaging Conference, NSS/MIC 2019* (Institute of Electrical and Electronics Engineers Inc., 2019).

[4] D. Gascon, H. Chanal, A. Comerma, S. Gomez, X. Han, J. Mazorra, J. Mauricio, N. Pillet, F. Yengui, and R. Vandaele, *PACIFIC: A 64-Channel ASIC for Scintillating Fiber Tracking in LHCb Upgrade*, J. Instrum. **10**, C04030 (2015).

[5] A. Phillip E. Allen, Douglas R. Holberg, *Allens Book*, in *CMOS Analog Circuit Design* (2002), p. 725.

[6] E. Bruun and P. Shah, *Dynamic Range of Low-Voltage Cascode Current Mirrors*, in *Proceedings - IEEE International Symposium on Circuits and Systems*, Vol. 2 (IEEE, 1995), pp. 1328–1331.

[7] A. Hastings, *The Art of Analog Layout* (Prentice Hall, 2005).

Glossary

ICC-UB	Institut de Ciències del Cosmos-Universitat de Barcelona
HERD	High Energy Cosmic-Radiation Detector
FIT	Scintillating Fibre Tracker
CSS	China's Space Station
CSU	Central South University
IHEP	Institute of High Energy Physics
INFN	Istituto Nazionale di Fisica Nucleare
CIEMAT	Centro de Investigaciones Energéticas Medioambientales y Tecnológicas
EPFL	École polytechnique fédérale de Lausanne
DAC	Digital-to-Analogue Converter
R2R	Rail-to-Rail
FDA	Fully Differential Amplifier
MIP	Minimum Ionizing Particle
DRC	Design Rule Check
LVS	Layout-versus-Schematic
PEX	Parasitic Extraction
SiPM	Silicon Photo-Multiplier
GBW	Gain-Bandwidth