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Design of an Integrated System for On-line Test and Diagnosis of Rotary Actuators

Leonardo B. Piccoli[1] · **Renato V. B. Henriques**[2] · **Tiago R. Balen**[1]

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Abstract

In this paper, the design of an on-chip Fault Detection and Diagnosis System for Condition Based Maintenance of electromechanical actuators is presented. The proposed system is based on signal processing algorithms integrated in a customized *Application Specific Integrated Circuit* (ASIC). The design was synthesized using a 90nm CMOS standard cell library. As a case study, post-synthesis simulations were performed using signals acquired from a real electromechanical valve, using torque and vibration sensors considering both fault-free and defective situations for the actuator. Results show the effectiveness of the system in performing real-time fault detection and identification, with low power consumption and low silicon area utilization.

Keywords Condition-based maintenance · Fault detection · Fault prediction · Diagnosis · Electric valves · On-line test · Electromechanical actuators

1 Introduction

On-line fault detection, prediction and diagnosis in mechanical systems is of significant importance, as, for instance, in pipelines for oil or gas transportation and other related industry activities [7, 8]. When considering oil or gas transportation, electromechanical valves are widely used in complex pipelines. Therefore, due to the safety and financial-critical nature of such activities, the fault-free operation of electric valves is crucial. This demands strategies for test and predictive maintenance, which, in electromecanical systems, requires autonomous and continuous monitoring of signals acquired in mechanical structures or electric parts of the monitored machines.

Several techniques for health monitoring of mechanical equipment have been proposed in the last years. They are usually based on signal processing (using, for example, Wavelet and Fourier transforms and adaptive filtering), artificial intelligence networks and machine learning, as for example, [6, 9, 13]. Such techniques are implemented in personal computers (PC), resulting in large footprints and power-hungry systems. Some other techniques are implemented in Field Programmable Gate Arrays (FPGAs), as for example, [3], in which a fault diagnosis for steam turbine systems, was proposed. In [2], an on-board real-time system to detect and isolate critical faults in an electromechanical actuator of aircraft is proposed. A real-time FPGA-based fault monitoring system of power electronics interfaces in wind energy systems was presented in [12].

Few works deal with health monitoring in electrical valves. An FPGA implementation of a fault detection and diagnosis method for an electric valve was proposed in [5], using self organizing maps for fault detection. Additionally, part of the system was implemented in a PC.

Most of the aforementioned methods present limitations regarding physical dimensions of the system platform, power consumption and real-time operation issues. Techniques based on high performance computing, such

Responsible Editor: K. K. Saluja

✉ Leonardo B. Piccoli
leonardo@piccoli.eng.br

Renato V. B. Henriques
rventura@ece.ufrgs.br

Tiago R. Balen
tiago.balen@ufrgs.br

[1] Graduate Program on Microelectronics, Federal University of Rio Grande do Sul, Porto Alegre, RS, Brazil

[2] Graduate Program on Electrical Engineering, Federal University of Rio Grande do Sul, Porto Alegre, RS, Brazil

as machine learning, and high complexity signal processing will often need to be performed in PCs or dedicated processor-based systems. Additionally, complex methods may demand to be performed off-line [9], while some other techniques allow on-line fault detection [11, 15] and some are real-time techniques [2, 3, 12].

With these concerns in mind, we propose, in this paper, a fault detection and diagnosis system for electromechanical rotary actuators implemented in an *Application Specific Integrated Circuit* (ASIC), featuring both low-power operation and miniaturization. The considered case study is an electric valve in which the implemented *Fault Detection System* (FDS) collects information obtained from strain and vibration sensors. A second block, called *Fault Detection Index* (FDI) performs data compaction at the same time that allows fault classification and diagnosis. The feasibility of the used algorithms was proved in [10] considering a software implementation of a preliminary version of the system.

The system was synthesized using a 90nm CMOS standard cell library. A functional BIST module, with a test-pattern generator, was included in the design, allowing a simple periodical self-test. The validation is performed by post synthesis simulations with real signals acquired from an electric valve in different damage scenarios. Results show the ability of the system in performing fault detection and diagnosis, allowing low-power and on-line operation.

2 The Proposed System

The proposed system follows the *Open Systems Architecture for Condition-Based Maintenance* (OSA-CBM) model [14]. One or more indicators are produced by the CBM, in order to indicate if/when the system needs maintenance. Such maintenance strategy relies on monitoring the current condition and predicting the future condition of machines, during system operation.

The proposed system applies the first four layers of OSA-CBM model: 1) Data Acquisition; 2) Data Manipulation; 3) State Detection and 4) Health Assessment.

The main task of the FDS is to detect any change in magnitude or frequency of the signal obtained from sensors installed in the actuator, identifying particular patterns associated to the health condition of mechanical parts. However, the FDS scheme should have enough resolution to detect small changes in the system, because this allows the detection of incipient faults before the occurrence of catastrophic failures.

Considering the case study electrical valve, mechanical damage results in a change in stiffness and damping, which reflects in mechanical properties, as variations in frequencies, amplitude of vibration and damping ratio. However, small degradation do not cause significant modification of these signals. For this reasons, the FDS operates with dual capability of processing, related to the signal amplitude: approximation coefficient and detail coefficient, which, in this work, are used to process torque and vibration signals, respectively.

The main blocks of the proposed system are depicted in Fig. 1 in which the hardware implemented algorithms perform the following steps:

1. In each sampling period, the input of the system is a sample of the signal coming from sensors.
2. A *Discrete Wavelet Transform* (DWT) block decomposes the input signal into two sub-bands (approximation and detail coefficient), each of which is then down-sampled by a factor of 2, obtaining the low frequency (or approximation) sub-band, and the high frequency (or detail) sub-band.
3. Depending on the desired analysis, the approximation sub-band (a), with signal acquired from strain sensor, or the detail sub-band (d), with vibration signal as system input, are sent to the block POWER, in which the signal energy is calculated.
4. Afterwards, a *Least Mean Squares* (LMS) adaptive filter is used to predict values of the power signal. The adaptation parameter μ (step-size) controls the speed of convergence, stability, and steady state performance of the adaptive filter and also defines the needed sensitivity to detect transient variations in the signal. In this application, the output signal of the LMS filter, (i.e. the steady state error), is used to identify the occurrence of a fault in the system.
5. The final step is accomplished by the FDI block that produces information about the current health status. This block shows if an error occurs and allows to

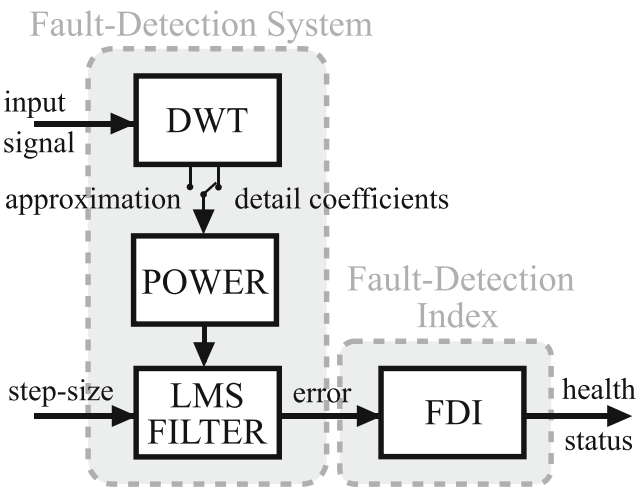

Fig. 1 Block diagram of the proposed system

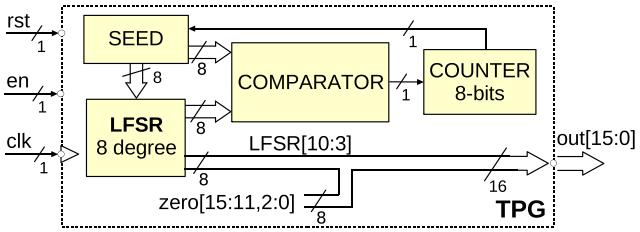

Fig. 2 Test Pattern Generation for the system

classify the fault by evaluating the number of error occurrences in a given set of samples from the error signal. This result may be used to represent the severity of the damage. The FDI output samples may be used to build an histogram graph, which can indicate a trend or pattern in the FDI outcome series over a period of time (examples are shown in Section 4), allowing to perform diagnosis.

Assuming that the transfer function of the monitored system is unknown, a 5-coefficient representation is used to model the system. Thus the FDS algorithm block is composed of a 5-tap FIR-LMS adaptive filter, one 9/7 lifting-based DWT filter [1] and a block that calculates the signal power and performs an estimate of the energy over a limited time frame.

The Fault Detection Index calculation evaluates the number of samples in which a fault is detected by the FDS block. The signal amplitude of the FDS outcome is between *0* and *1*, which is compared with a preconfigured threshold (0.25 in this case) at the FDI block, in a way that a flag indicates a detection. The FDI sums up the number of detected errors in a given set of samples (frame) of size N (256 in this work). Since the FDI output is also a compacted signal (if comparing its data rate with the one of the FDS signal), it eases the data analysis and allows power and bandwidth savings for data transmission. The addition of this block also allowed to reduce the number of "false positive" interpretations (caused by the uncertainty of data coming from sensors). The FDI algorithm is defined as follows:

$$FDI[j] = \sum_{k=N\times j}^{N\times(j+1)-1} FD[k] \quad (1)$$

where FD[k] is a flag that indicates if a fault is detected (when the error signal exceeds the defined threshold) in each sample of FDS outcome, k is the current time point, N is the number of discrete measurements and j is the frame of size N. This process is similar of that proposed in [12].

The outputs of FDS and FDI blocks are intended to be zero when no fault is detected, in such a way that these signals shall remain unaltered during very long time periods. Therefore, considering that the system may be employed in safety-critical applications, a periodic self test is desirable to check if the FDI and FDS blocks are still able to generate the proper outputs when a fault occurs in the electromechanical system.

For this purpose, a simple functional BIST is embedded into the system, which generates a pseudo-random sequence to emulate a defective behavior in the sensed signal. Thus, in the test mode, a multiplexer is switched to deliver this generated signal to the FDS block instead of that coming from the sensors when in normal operation.

This test signal is generated by an 8^{th}-degree primitive *Linear Feedback Shift Register* (LFSR), which is able to produce a $2^n - 1$ length sequence (all possible values except the zero state). Figure 2 shows the designed TPG (*Test Pattern Generator*), while Fig. 3 shows how this TPG is connected to the FDS block.

In the adopted TPG a comparator is used to detect when all states of the LFSR are generated, so that the seed value of the LFSR is repeated. This is achieved by comparing the current value of LFSR and its initial value. When the result of this comparison is *true* a new seed value is generated, by incrementing the previous value in one unit. This is done to avoid a cyclic pattern during the test application.

3 Design Implementation and Synthesis Results

The implementation of the lifting operation for the DWT, in the FDS block, requires no extra memory buffer, by exploiting the in-place computation feature. Hence, the multiplier can be replaced by a limited quantity of shift registers and adders.

To reduce utilization of logic resources, considering the constant coefficient multipliers, the partial product of a variable can be generated by shift operation, which reduces

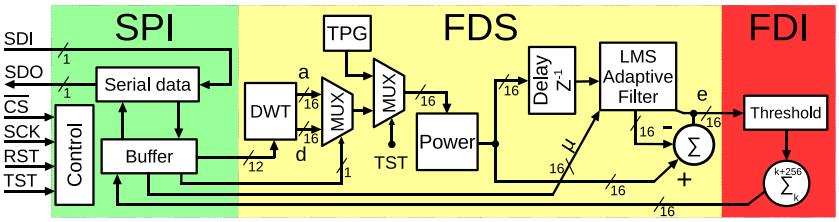

Fig. 3 Functional block diagram for the ASIC implementation

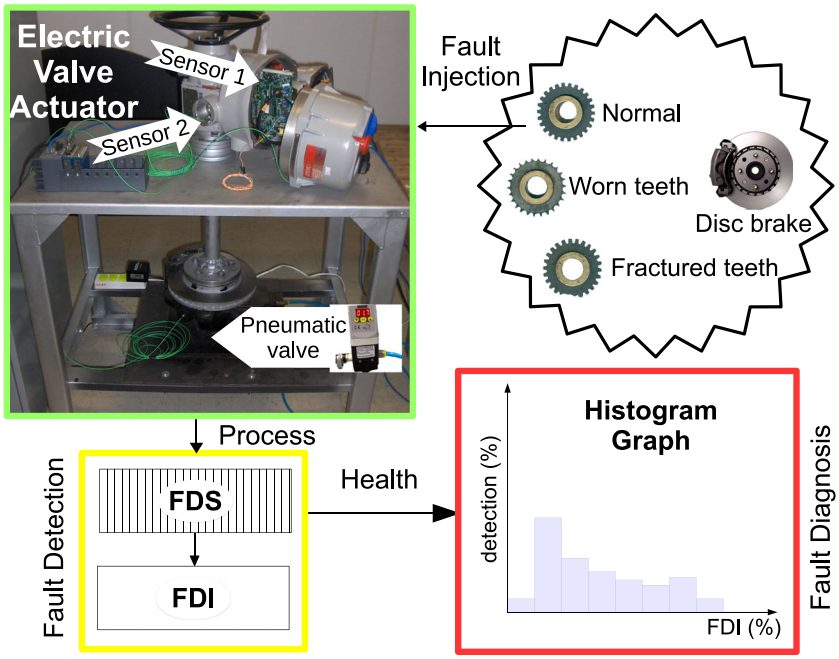

Fig. 4 Experimental setup and sensors arrangement with fault injection, detection and diagnosis system

the necessary multiplier units. This is possible because the samples are quantized in fixed point representation, consequently, reducing power consumption and enhancing the computational capability of the hardware.

The block diagram of the RTL implementation of the system is shown in Fig. 3. The system interface is a *Serial Peripheral Interface* (SPI) block. The digitized data from the sensors are loaded to the system by means of the *Slave Data Input* (SDI) port. The *Slave Data Output* (SDO) is used to carry out the FDI data. The other pins are the *Chip Select* (CS), *clock* (CLK), *reset* (RST) and test mode activation (TST).

Two commands can be transmitted by the master controller to configure the hardware via SDI terminal. The most significant bit (b15) selects if data input is from sensor (operation) or the adaptation parameter μ (configuration phase). Bit b14 selects the used DWT coefficient (detail or approximation coefficients). Bits b13 and b12 are not used and the other 12 bits represent the fixed-point data.

Results of synthesis and static timing analysis of the design have been analyzed in order to evaluate timing constraints. Since one of the desired characteristics of the system may be low-power consumption, dynamic evaluation was performed considering a 4096 Hz clock, which is sufficient to allow the required processing, since the sampling rate of the sensor signals is 256 Hz with a 12-bit wide sample (12-bit ADC).

This sampling frequency is suitable to capture most of the energy associated with system dynamics. In our case, the valve axis rotates at 42 rpm and the motor speed is 3600 rpm. In other words, the fundamental frequencies of interests are 0.7 Hz and 60 Hz.

The core area of the proposed system is 143197.46 μm^2. The maximum propagation delay of the critical path is due to the SPI block (5.95 ns). Thus, the maximum operating frequency of the circuit is 168.07 MHz.

Due to the low minimum clock frequency required and the implemented clock gating, low dynamic power consumption is achieved (654.39 μW). The leakage power

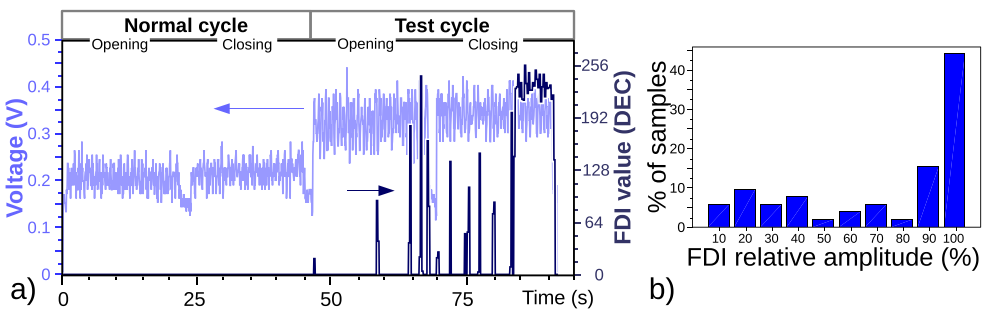

Fig. 5 Torque sensor signal, FDI output **a** and resulting histogram **b** for 1 bar of pressure applied on the valve mechanism

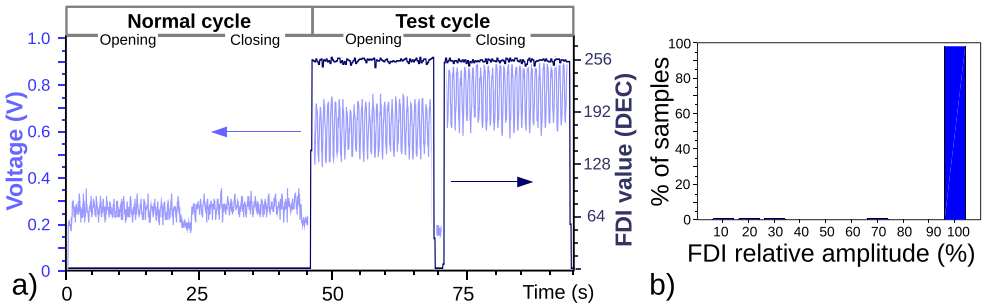

Fig. 6 Torque sensor signal, FDI output **a** and resulting histogram **b** for 3 bar of pressure applied on the valve mechanism

is dominant in this design, with static power being 654.37 μW and dynamic power is 26.61 nW.

4 Results and Discussion

The post-synthesis obtained system was simulated with acquired signals of a pair of sensors (strain gauge and accelerometer) installed in a real fluid flow control valve.

The physical setup considers a real scenario of field application with faults in some components of the valve. Faults were injected in mechanical parts, firstly by installing a brake system in the open/close mechanism of the valve to simulate mechanical efforts. The brake is installed on the actuator stem, and it was driven and regulated by means of a pneumatic valve controlled by an auxiliary actuator, as shown in Fig. 4, allowing to monitor the torque effort delivered by the actuator. In a second moment the gears of the system were substituted by defective ones emulating typical initial failure situations on the mechanical parts of the valve.

The collected signals from the sensors were quantized in 12 bit. The adaptation parameter of LMS filter was set as $\mu = 0.1$. Both the step size and sensor gain must be adjusted, depending on the sensor and the mechanical system parameters. In this version of the ASIC, the calibration is performed once when the sensors are installed and the associated register at the LMS adaptive filter is loaded with the corresponding step size. However a self-calibration circuit may be considered in future implementations.

The first fault emulation campaign considers situations with pressure applied through the brake set, emulating faults that can be sensed evaluating the valve actuator torque. The energy of the signal is extracted by the FDS using the approximation coefficients of the Wavelet transform.

Figure 5a shows the input signal provided by the sensor (scale on left axis) and the FDI output signal (right axis), for a fault-free (normal cycle) and a faulty signal, obtained while applying 1 bar of pressure with the brake system. This figure evidences a fault detection by the changing in behavior of the FDI signal, while the histogram (Fig. 5b), presents an interpretation of the fault behavior. The histogram shows the percent occurrence of FDI outcome samples against the normalized amplitude of the FDI Signal (represented also in percent).

One can notice that both the FDI signal and the histogram (besides the FDS output itself) can be used to determine the presence of a fault. The criteria may be either a threshold value on the FDI signal or a threshold value of the number of occurrences higher than a certain value of the FDI signal.

Figure 6 shows results of fault injection applying 3 bar of pressure to the brake system. In this case, the intensity of the mechanical defect generates a different FDI signature, which can be easily identified by the histogram plot, which can be used to perform diagnosis.

To exemplify what the histograms represent, it can be seen in the histogram of Fig. 6b (rightmost bin) that more than 95% of the 256 samples of the FDI signal are near the maximum normalized value (100%) during this fault emulation. This can be confirmed in Fig. 6a, in which it is possible to see a saturation of the FDI signal (value 255),

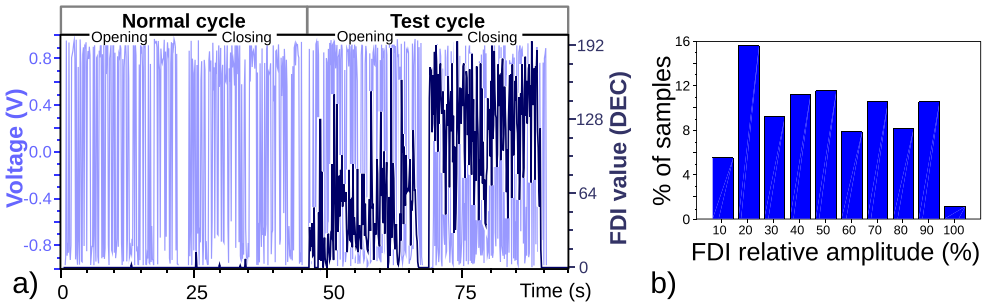

Fig. 7 Accelerometer sensor signal, FDI output **a** and resulting histogram **b** replacing valve gears by aged ones

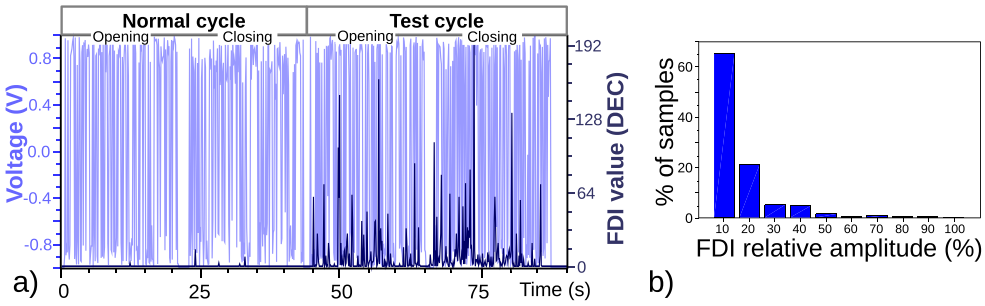

Fig. 8 Accelerometer sensor signal, FDI output **a** and resulting histogram **b** with fractured teeth gears

during almost all test phase. On the other hand, histogram of Fig. 5b shows that the values of the FDI samples spread along its full scale (0 to 255), as can be seen in the FDI signal in the figure.

In the second fault emulation experiment, open/close test cycles of the valve were executed changing the gears of the actuator by aged and fractured teeth gears. In this case, the energy of the input signal was extracted using the detail coefficients by the FDS block.

Figure 7 shows the results when the valve presents two gears with aged teeth, while Fig. 8 presents results for the fractured teeth condition.

Finally, the BIST module was simulated, by setting the test mode ($TST = 1$). Figure 9 shows the generated test signal, composed of 65280 samples (255 states of LFSR multiplied by 256, which is the counter limit). While the test vector generation is embedded in the circuit, the signature check is performed by observing the final histogram of the FDI data. The histogram shown in Fig. 9 reveals that the system is able to perform the analysis of a defective signal.

Table 1 shows a comparison of the solution presented in this work with previous ones, showing the contribution to the state-of-art advance. Besides being the first presented ASIC for fault detection in mechanical applications, allowing low-power and miniaturization, the ability of performing diagnosis and functional self-test are also important contributions.

The power consumption of an ASIC is several magnitude orders smaller than for FPGA and PC-based solutions. Additionally, the data compaction performed by the FDI block also reduces the power needed to transmit the data.

5 Conclusion

This paper presents an ASIC implementation of a fault detection and diagnosis system for rotary actuators. The system is validated by using an electromechanical valve as case study. The proposed integrated circuit presents low-power and low silicon area, besides enabling real-time fault detection. The system also incorporates a functional Built-In Self-Test block, which allows to asses the FDS and FDI correct functioning in periodical self-test sequences, performed in field.

The hardware was synthesized using the *SAED 90 nm* standard cell library [4] from Synopsys and is able to process sensor data with a clock as low as 4 kHz (allowing the low power feature) and can be used to detect several types of mechanical faults.

The low required clock allows its fabrications in mature (an cheaper) technologies, as for example 0.6μm, significantly reducing the final cost of the ASIC (one of the main drawbacks of ASIC implementation). This block may also be embedded in smart sensors (containing the transductors and ADCs) and high-volume production may reduce the cost per part.

The synthesized hardware was evaluated by simulation, considering signals from a fault injection campaign in a commercial electromechanical valve. Results show that the system is able to perform on-line detection of parametric an catastrophic faults, associated to several mechanical defects. The different types of faults can be classified, allowing diagnosis besides fault detection.

Although the case study of this work is focused on an electric valve actuator, most machines to which fault

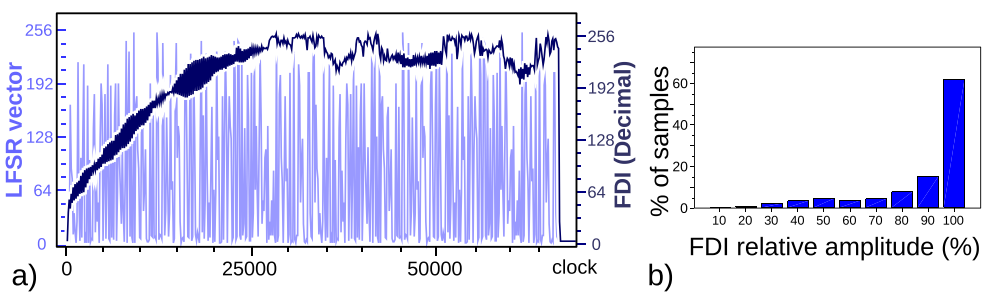

Fig. 9 Simulation of BIST scheme

Table 1 Comparison with similar solutions on literature

Work	Platform	Operation	Low-power
[5, 6, 9, 11, 13, 15]	PC	off/on-line	no
[2, 3, 12]	FPGA	real-time	no
This work	*ASIC*	real-time	yes

detection systems are proposed operate at similar frequency ranges and have gears and mechanical components that may result in similar defective behaviors and system failures. Some of these possible applications may benefit from miniaturization and low power features allowed by an ASIC implementation.

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Leonardo B. Piccoli received his M.Sc in Mechatronic Engineering from Pontifical Catholic University of Rio Grande do Sul - PUCRS, Brazil (2004), M.Sc in Electrical Engineering from PUCRS (2006) and Ph.D. in Microelectronic Engineering from Federal University of Rio Grande do Sul - UFRGS (2018). His current research interest includes hardware system design and intelligent maintenance.

Renato V. B. Henriques received his B.Sc. in electrical engineering from Pontifical Catholic University of Rio Grande do Sul, Brazil (1992) and M.Sc. in electrical engineering from the University of São Paulo - USP, Brazil (1996) and Ph.D. in mechanical engineering from Federal University of Minas Gerais - UFMG, Brazil. He is currently a professor at Federal University of Rio Grande do Sul (UFRGS) teaching electrical engineering with emphasis in electrical process automation and electronics industry, focusing on the following topics: position control, cooperative robots, robotic welding, intelligent maintenance, Kalman filters, manufacturing systems and distributed control and Educational Robotic.

Tiago R. Balen received his Electrical Engineering degree, in 2004, from Federal University of Rio Grande do Sul (UFRGS), Porto Alegre, Brazil, where he started his academic career working at the Prototyping and Test Laboratory. In 2006 and 2010, respectively he received the MSc degree and the PhD degree from UFRGS. In 2012, he received an important award from FAPERGS (Rio Grande do Sul State Research Fomentation Agency) for the innovative contributions of his PhD thesis. His research interests include analog and mixed-signal test, built-in-self test, programmable analog devices, fault tolerant circuits and radiation effects on electronic systems. In the past years he has published papers on these topics in important conferences and journals, receiving a "Best Paper Award" for one of his contributions. Currently, he is associate professor at the Electrical Engineering department and researcher, advisor and coordinator of the graduate program on Microelectronics (PGMICRO) of the Federal University of Rio Grande do Sul (UFRGS).