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Comparing the Impact of Power Supply Voltage on CMOS- and FinFET-Based SRAMs in the Presence of Resistive Defects

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Abstract
CMOS technology scaling has reached its limit at the 22 nm technology node due to several factors including Process Variations (PV), increased leakage current, Random Dopant Fluctuation (RDF), and mainly the Short-Channel Effect (SCE). In order to continue the miniaturization process via technology down-scaling while preserving system reliability and performance, Fin Field-Effect Transistors (FinFETs) arise as an alternative to CMOS transistors. In parallel, Static Random-Access Memories (SRAMs) increasingly occupy great part of Systems-on-Chips' (SoCs) silicon area, making their reliability an important issue. SRAMs are designed to reach densities at the limit of the manufacturing process, making this component susceptible to manufacturing defects, including the resistive ones. Such defects may cause dynamic faults during the circuits' lifetime, an important cause of test escape. Thus, the identification of the proper faulty behavior taking different operating conditions into account is considered crucial to guarantee the development of more suitable test methodologies. In this context, a comparison between the behavior of a 22 nm CMOS-based and a 20 nm FinFET-based SRAM in the presence of resistive defects is carried out considering different power supply voltages. In more detail, the behavior of defective cells operating under different power supply voltages has been investigated performing SPICE simulations. Results show that the power supply voltage plays an important role in the faulty behavior of both CMOS- and FinFET-based SRAM cells in the presence of resistive defects but demonstrate to be more expressive when considering the FinFET-based memories. Studying different operating temperatures, the results show an expressively higher occurrence of dynamic faults in FinFET-based SRAMs when compared to CMOS technology.

Keywords CMOS · FinFET · SRAMs · Resistive defects · Power supply voltage · Test

1 Introduction

During the last decades, advances in Very Deep Sub-Micron (VDSM) technology allowed the technology miniaturization according to Moore's law, which predicted the number of transistors in the same area to double every eighteen months. However, the nature of scaling has already changed [29], causing tectonic shifts, such as the switch to parallelism rather than clock frequency as the primary driver of performance in microprocessors.

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There is a growing concern that scaling of devices in any form is slowing down, and there is a good chance that it will eventually become infeasible to cost-effectively manufacture devices below a certain feature size [29]. In this context, the scaling roadmap for ICs has been extrapolated from the current Moore's law regime into three main domains, namely 1) "More-Moore"; 2) "Beyond CMOS"; and 3) "More-than-Moore". The first domain is expected to deal with traditional silicon Complementary Metal-Oxide Semiconductors (CMOS) and its scalability, in other words, the continuation of Moore's Law is known as the "More Moore" domain [20]. The "Beyond CMOS" domain consists of various nanotechnologies beyond ultimately scaled CMOS (e.g., carbon nanotubes, Si nanowire, spintronics, etc.), which can potentially replace silicon and CMOS in the future. The "More-than-Moore" domain encompasses various disruptive device paradigms such as flexible electronics, nanoelectromechanicals (NEMS), biochips, heterojunction devices, solar cells, fuel cells, etc. Note that the devices in the "More-than-Moore" domain are not necessarily nanoscale, and

they often provide auxiliary functions that cannot easily be realized in CMOS technology. Considering the "More-Moore" domain, the continuous evolution of Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) technology has been enabling miniaturization and aggressive technology integration. However, due to the increase of leakage current and short-channel problems in this technology, it was not feasible to shrink feature size below 22 nm [19] using MOSFET. To continue the scaling down of technology nodes, Fin Field-Effect Transistors (FinFETs) were introduced as an alternative transistor technology to replace CMOS devices. FinFET is built as a multi-gate transistor. In other words, the FinFET channel has the shape of a fin and is involved by the gate, all placed on top of oxide. This design approach improves the electrostatic control of the transistor's channel [21] and hence solves some of the before mentioned problems evolving CMOS technology for nodes beyond 22 nm. In more detail, leakage current, Short-Channel Effects (SCE) and Random Dopant Fluctuations (RDF) are mostly eliminated as doping levels are reduced to a minimum in FinFETs [34]. Consequently, the majority of microelectronic companies are gradually replacing CMOS transistors by FinFETs in their state-of-the-art processors. With the introduction of FinFET technology and the subsequent changes to technological paradigms, several circuit devices needed to be redesigned, tested, and evaluated. In parallel, due to the always-increasing need to store more and more information on chips, Static Random-Access Memories (SRAMs) have become the main contributor to the overall area of Systems-on-Chips (SoCs) [36] and hence are cited as particularly important, representing this work's focus. Further, SRAMs are designed at the dimensional limits of technology, being statistically more likely to be affected by manufacturing defects [5], generating the expressive need for intensive test procedures during the manufacturing stage. Therefore, SRAMs require efficient testing, i.e., tests with high fault coverage and low cost. Resistive defects have traditionally been a concern in the CMOS technology test scenario. More recently, this concern shifted towards weak resistive-open and weak resistive-bridge defects as their probability of occurrence may increase in nanometer technologies due to the ever-growing number of interconnections between layers [13]. With the scaling down of technological nodes, resistive defects are likely to be one of the main reliability challenges in IC design [30]. These defects have been modeled and studied in CMOS technology and are known to generate dynamic faults, which require a sequence of at least two consecutive read operations to be sensitized [4]. However, detection of weak resistive defects and, therefore, dynamic faults may not be trivial. In fact, open/resistive vias are the most common origin of test escapes in deep-submicron technologies [28]. Thus, a complete understanding of this specific type of defect and the faults it stimulates is essential to improve manufacturing test procedures. Commonly, dynamic faults have been related to two aspects: the physical position and size of the defect. Varying defect positions have been evaluated for planar SRAM cells and the classification into either resistive-open, a resistor between two circuit nodes that share a connection, or resistive-bridge, a resistor between two nodes that should not be connected was established [13, 16]. Regarding defect size, it can be used to estimate the fault's strength. As previously mentioned, weak defects are defects able to sensitize dynamic faults; simulating different defect sizes allows to identify the specific resistance necessary to start sensitizing a certain defect at logic level. This resistance, known as critical resistance, defines the threshold between a fault-free and faulty behavior. In [15] a study comparing physical and electrical characteristics of 6 T and 8 T SRAM cells designed based on a FinFET technology library of 20 nm and a CMOS technology of 22 nm has been performed. The comparison confirms that FinFET-based SRAMs are less susceptible to process variation and present lower leakage power consumption, hence possess higher robustness and reliability with respect to the CMOS version. Two studies about the impact of Stuck-Open Faults (SOFs) in FinFET devices have been performed in [8, 33]. The papers report that the classical SOF behavior is modified by the increased transistor off-state leakage current and smaller node capacitances in nanometer technologies. The IC SOF response is a mix of classical and non-classical responses that are functions of fan-out, fan-in, clock period, local leakage environment, noise, VDD, and temperature. The work presented in [8] proposes two vector strategies to improve the robustness of SOF detection in the presence of leakage currents. The works presented in [3, 30] propose fault models for FinFET devices injecting open and shorts defects in logic gates, an INV and a NAND, using the Independent Gate (IG) configuration and the Shorted Gate (SG), also called Tied Gate (TG). In [32], the authors demonstrate that most opens and shorts in FinFET logic circuits have corresponding fault models in planar CMOS. However, opens on the back gate with the intended signal at the front gate cause delay and leakage problems, which are unique to FinFETs, owing to the strong dependence of threshold voltage on the back-gate bias, thereby compounding the role of the deice/layout parasitics. Note that the absence of a unified fault model for back-gate cuts in IG FinFETs poses a testing challenge, due to the diversity of output behaviors. In [23], several types of defects on FinFET logic circuits have been studied. Three different defects have been injected in the fins: stuck-on, stuck-open, and gate oxide shorts. The paper concludes that different numbers of fins result in different faulty behaviors. The proportion of defective fins determines if the device can be regarded as fault-free or not. When the number is large enough, it manifests itself as stuck-open fault or delay fault. Furthermore, when multiple gates are influenced by defects such as back gate open or fin stuck-on faults at the same time, new test strategies are required. In [22], Gate Oxide Short (GOS) effects in FinFETs have been investigated. The paper concludes that GOS faults in FinFETs are more complex to detect than those in planar bulk MOSFETs. For TG FinFETs, the fault

behavior with respect to the decrease of saturation drain current becomes much less obvious. For IG FinFETs, the fault behavior of the GOS at the front and back gate completely differ from each other. For detecting GOS faults, the authors propose two different test strategies. One is for TG FinFET-based while the other is for IG FinFET-based SRAMs. Both methods are able to detect usually undetectable GOS. The effects of open defects, the logic and dynamic behavior, located inside the gate of FinFET of logic cells has been studied in [26]. The location of defects in the gate influences the fault behavior. For some positions the fault is similar to planar CMOS, and for others the behavior differs. The paper reports that the detection of open defects in FinFET cells is more difficult than in planar CMOS. In addition, a study aiming to model FinFET-specific faults and synthesizing test algorithms has been proposed in [18, 19]. The paper [19] shows that FinFET-based SRAMs are more prone to dynamic faults and is more stable to no-defect related failures associated to process variation. Furthermore, the paper shows that static coupling faults are typical for both FinFET- and planar-based SRAMs. In [25], the impact of temperature on the dynamic fault behavior has been analyzed showing how test procedures for FinFET memories can benefit from properly adjusting the operating temperature to detect resistive defects and avoid test escapes.

In this context, the main goal of this work is to evaluate the impact of different power supply voltages on the behavior of defective CMOS- and FinFET-based SRAM cells. In addition, this paper proposes to compare the behavior of CMOS- and FinFET-based SRAM cells under resistive defects considering different temperatures aiming the identification of a fault range, based on three pre-selected operating temperatures. The evaluation proposed in this paper adopts a CMOS-based SRAM modeled using a 22 nm Predictive Technology Model (PTM) [27] and a FinFET-based SRAM designed using a 20 nm Low Power PTM [27]. The behavior of the defective SRAM cells operating at different power supply voltages has been investigated through electrical simulations using HSPICE™ from Synopsys. It is important to point out that this paper provides an additional analysis with respect to the one proposed in [10], where we compared the behavior of a CMOS- and a FinFET-based SRAM cell with resistive defects considering different operating temperatures. The results presented in this paper will provide substantial information regarding the best scenario for easily propagating faults associated to resistive defects. In addition, the paper also points out the main difference between defective CMOS- and FinFET-based SRAM cells under different operating conditions allowing the understanding by test engineers if the test strategies used for CMOS-based SRAMs can be also used for testing FinFET-based SRAM cells. Note that the paper also presents a pre-analysis considering different operating temperature. These experiments have been performed in order to properly identify the defect size range where faults are observed. Finally, it is important to mention that we decided to use a 22 nm technology library for the CMOS-based SRAM instead of the 65 nm technology node in order to provide a more technology node independent comparison, since the FinFET-based SRAM adopts a 20 nm technology library. Besides that, a new set of simulations has been performed in order to map and compare the impact of power supply voltage variation on defective SRAM cells, analyzing each defect individually.

This paper is organized as follows: Section II presents the background related to CMOS and FinFET technology, the main characteristics related to the design of CMOS- and FinFET-based SRAM cells. It further summarizes the targeted set of resistive defects with their corresponding fault models. Section III describes the adopted experimental setup, while section IV discusses the obtained results. Finally, section V draws the conclusions.

2 Background

This Section presents an introduction to the main differences between CMOS and FinFET technologies. Moreover, Section II introduces important aspects related to the design of CMOS- and FinFET-based SRAM cells. The Section further describes the fault model related to resistive defects.

A. *Basics of CMOS and FinFET Technology*

CMOS is one of the main technologies used in the manufacturing process of integrated circuits throughout the last decades. Using this technology, the gate, responsible for controlling the channel conductance by means of the field effect, is planar. With the continued advancements of CMOS technology and its technology scaling, CMOS has proven unable to keep up the technology shrinking trend predicted by Moore's law [19] due to being more prone to Short Channel Effect (SCE) and an increased leakage current at nanometer scale, caused by the poor electrostatic control of the channel conductance by a planar gate.

FinFETs are non-planar, multi-gate transistors consisting of thin vertical slices of silicon, known as fins, which are wrapped by the gate, and finally placed on top of oxide [21]. There are different ways to construct FinFETs, and each way results in a distinct final structure [12]. In Silicon-over-Insulator (SOI) FinFETs, fins are built over Buried Oxide (BOX) and are isolated from the substrate. In Bulk FinFETs, the fin passes through the oxide and is connected directly to the substrate layer, and a Shallow Trench Isolation (STI) of oxide is formed on the side.

Besides these differences, FinFET technology inherits many manufacturing process steps from CMOS, making it a favorable choice as a substitute [35]. The fundamental design

parameters of a FinFET are its fin's height (H_{FIN}) and thickness (T_{FIN}), replacing the Weight (W) from planar CMOS, as well as its channel length (Lg). Other parameters, such as Gate Oxide Thickness (T_{OX}), Gate Work Function, Body Doping, Gate/Source Doping, and Supply Voltage complete the typical parameters of a FinFET [30]. Fig. 1 shows the main structure of a CMOS transistor [6] and a FinFET, as well their parameters. The main advantage of FinFET technology is related to the reduced SCE due to the electrostatic control of the channel made on multiple sides by the gate, consequently providing a better control than planar transistor structures. This also reduces leakage currents, opening up the possibility for even smaller transistor, boosting technology's miniaturization even further.

B. *SRAM Cell Design*

A standard 6-T SRAM cell is composed of six transistors; four of them form two cross-coupled inverters (M1 & M2, M3 & M4), while the other two acts as pass gates (M5 and M6), providing read and write access to the cell. The word line (WL) controls the two pass-through nMOS transistors, the pass gates, which are connected to their respective Bit Lines (BL and $\overline{BL}$). The value stored in the cell corresponds to the digital representation of the voltage on Q ('1' for V_{DD}, '0' for 0 V). Miniaturization of conventional CMOS-based SRAMs is limited due to random variations of threshold voltage (V_{TH}) caused by Random Dopant Fluctuation. As high doping is not required in FinFETs due to their enhanced SCE, Random Dopant Fluctuation is expressively reduced, which diminishes V_{TH} variations and allows V_{DD} to be scaled down. In the context of SRAM cells, reduced Random Dopant Fluctuation also improves the Static Noise Margin (SNM) and consequently the cell's robustness [2]. Moreover, improved sub-threshold swing allows not only lower V_{TH} for a given off-state leakage current, but also enhances the on-state current per device width. Such improvements shorten the read and write access times on SRAM cells. Thus, the FinFET technology can bring many specific advantages to SRAM memories' performance and stability. The schematic of a 6 T CMOS- and a FinFET-based SRAM cell are illustrated in Fig. 2.

Throughout published works, distinct configurations of FinFET-based SRAM cells have been proposed and designed. Mainly, they differ in the number of fins used in each part of the cell: pass gates as well as pull-up and pull-down of each inverter. These variations have a direct impact on the robustness of the cell, as well as the need for additional write and read assist. Note that in this work, a high-density configuration presented in [7] was adopted. Both inverters and pass gates are designed using one fin in order to maximize the density of cells in the array.

C. *Fault Model Associated to Resistive Defects*

Due to imperfections on the manufacturing process, memory cells may be affected by manufacturing defects such as resistive-open and/or resistive-bridge defects that can compromise the correct behavior of them. These defects can be characterized as strong or weak: strong defects cause static faults, while weak defects are associated to dynamic faults. Faulty behaviors can be specified using Fault Primitive (FP), which characterize the sensitizing sequence, the faulty behavior observed, and the output of read operations [17]. A non-empty set of fault primitives is known as a Functional Fault Model. According to the Functional Fault Model (FFM) for memories presented in [31], static faults occur when one or no operation in the memory cell is enough to sensitize the faulty behavior at logic level. In contrast, dynamic faults occur when it is necessary to perform at least two consecutive operations to sensitize the fault at logic level.

Furthermore, an FFM can also be classified by the number of cells involved: single-cell and multi-cell FFMs. In a single-cell FFMs, faulty behaviors are observed in the defective cell

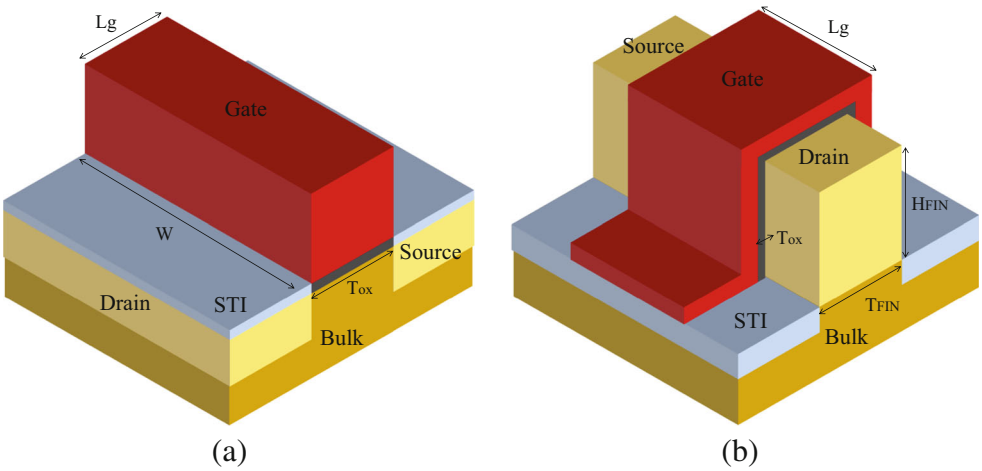

Figure 1. Main strucutre of (a) CMOS transistor, (b) FinFET and its parameters.

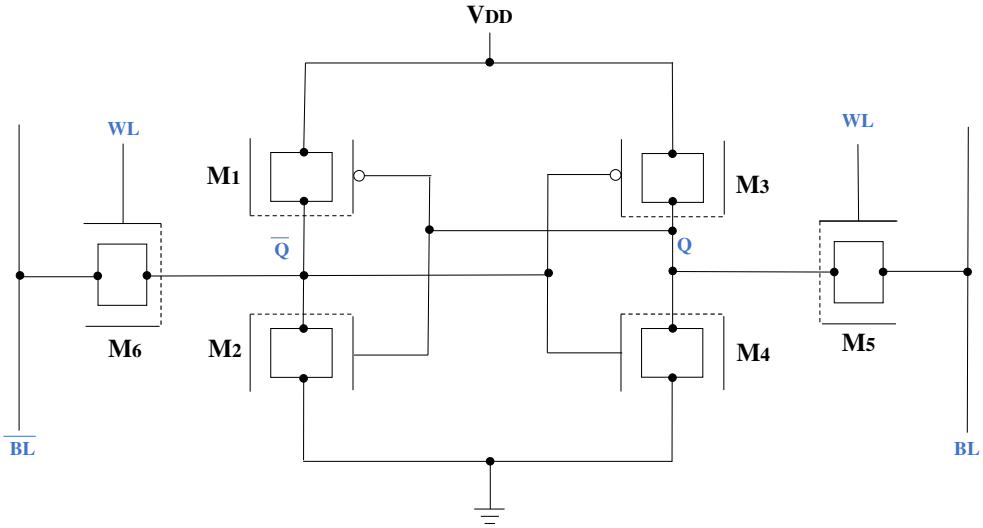

Figure 2. 6-T CMOS- and FinFET-based SRAM cell schematic.

only. In multi-cells FFMs, also known as coupling-faults, two cells (or two groups of cells) interact to produce a fault. The cell that suffers the faulty behavior is the victim (v-cell), while the cell that triggers the fault is the aggressor (a-cell). It is important to note that resistive defects can be present either in the a-cell and/or in the v-cell [17, 31]. Fig. 3 depicts the resistive defects analyzed in this work, including resistive-opens (DFOn) and resistive-bridges (DFBn). In more detail, Fig. 3 (a) and Fig. 3 (b) show the resistive defects injected in the CMOS-based SRAM cell and Fig. 3 (c) the ones injected in the FinFET-based SRAM cell. It is Important to mention that for the FinFET-based SRAM cell an extra defect, named

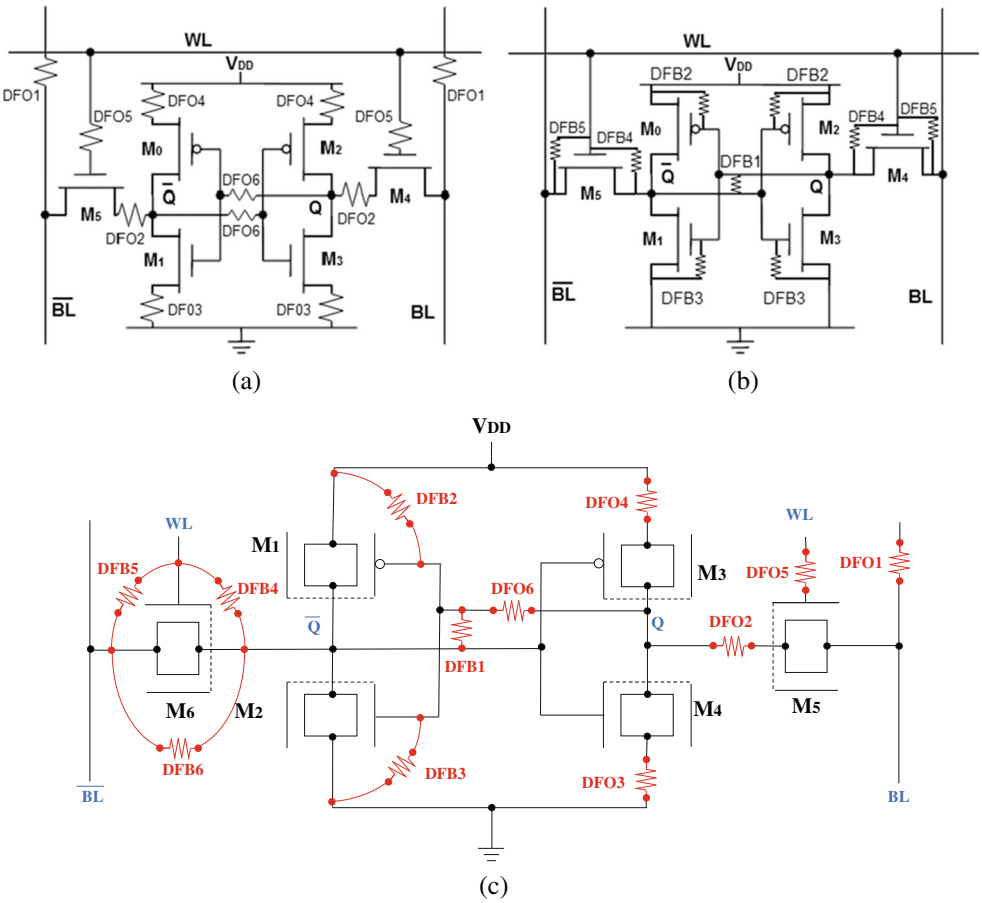

Figure. 3. Set of resistive defects affecting (a) and (b) a 6 T CMOS- and (c) a FinFET-based SRAM cell, incluidng resistive-opens and bridges defects.

DFB6, has been considered. DFB6 is a specific defect associated to FinFET technology [19]. Note that due to cell's symmetry, only one instance of each defect is necessary to analyse their impact on cell's behavior.

Thus, based on the injection of the resistive defects shown in Fig. 3, the fault model considered in this work represent the set of the following faulty behaviors:

- *Stuck-at Fault (SAF)* [11]*:* This fault occurs when the cell can only store one logic value '0' or '1';
- *Weak Read Fault (WRF)* [16]*:* This fault occurs when the cell cannot produce a difference of voltage in the BLs over 10% of V_{DD};
- *Read Destructive Fault (RDF)* [1]*:* This fault occurs when a read operation performed on the cell causes the value stored to flip, returning an incorrect value on the output. If the fault is observed after *n* previous successful read operations, the cell is said to have a dynamic RDF (dRDF) [31];
- *Deceptive Read Destructive Fault (DRDF)* [1]*:* This fault occurs when a read operation performed on the cell outputs the correct value, however, changes the stored value. If the fault is observed after *n* previous successful read operations, the cell is said to have a dynamic DRDF (dDRDF) [31];
- *Incorrect Read Fault (IRF)* [31]*:* This fault occurs when a read operation returns the incorrect value, however, the correct value is still stored in the cell. When the read operations on a cell occur immediately one after another, the fault is defined as dynamic Incorrect Read Fault (dIRF) [31];
- *Read Disturb Coupling Fault (CFir)* [32]*:* A cell is said to have a CFir when a read operation on a *v-cell* (a defect-free cell) returns the incorrect value on the output if a given value is present in an *a-cell* (a defective cell). If the fault presents a dynamic behavior, it is classified as dynamic CFir (dCFir) [31].

3 Experimental Setup

To provide the analysis proposed in this work, electrical simulations using HSPICE™ considering a CMOS- and a FinFET-based SRAM have been performed. The SRAM blocks are composed of 512 lines by 512 columns designed using a 22 nm CMOS PTM and of 1024 lines by 1024 columns designed using a 20 nm Low Power FinFET PTM [27]. In more detail, the CMOS-based SRAM cell has been designed adopting an *L* equal to 24 nm and a *W* equal to 71 nm for all transistors within the cell. For the FinFET-based SRAM, the transistors feature a *Lg* of 24 nm, H_{Fin} of 28 nm and a Fin Width (W_{Fin}) of 15 nm. Note that the effective width is calculated using the following equation:

$$W_{eff} = H_{Fin} + 2*W_{Fin} = 71nm \quad (1)$$

It is important to mention that for guaranteeing a more precise and fair comparison, the CMOS-based SRAM cell was designed considering the same parameters used in the FinFET-based SRAM cell. Moreover, the nominal power supply adopted is of 0.95 V for the CMOS block and of 0.9 V for the FinFET memory. Both memory blocks were connected to other functional blocks, such as sense amplifier, decoders and output latch, which are based on traditional SRAM designs [25]. The clock signal was set to operate with a frequency of 1GHz. To simplify the design, in both blocks, only 8 lines consisting of 8 columns each were implemented, while the remaining cells were emulated by loading WLs and BLs with equivalent capacitances.

Finally, the design of an SRAM cell is divided into three parts, in which a proper notation (PU: PG: PD) is used to describe its configuration, where PU, PG, and PD stand for Pull-Up, Pass Gate, and Pull-Down. The considered FinFET-based SRAM uses the High-Density configuration (1:1:1), with the unitary value as the number of fins in the transistors, as explained in [7]. For the CMOS-based SRAM a similar configuration has been adopted in order to guarantee a comparable scenario.

A. *Modelled Resistive Defects*

Fig. 3 shows the resistive-open and resistive-bridge defects modelled in the CMOS- and FinFET-based SRAM cell. The defect models are retrieved from [28, 30], considered classic references for modelling resistive-open and restive-bridge defects in CMOS-based SRAMs. As observed in Fig. 3 (c) these same defects are used for the FinFET-based SRAM, though adding an extra defect (DFB6). It is important to note that, based on the results reported in [9, 24], the following seven resistive defects presented a dynamic behavior: DFO2, DFO3, DFO4, DFB2, DFB3, DFB4, and DFB5. Thus, three of them are resistive-open defects (DFO2, DFO3 and DF04) and are modelled as non-designed resistances between two nodes that have a connection [14]. The other four defects represent resistive-bridge defects (DFB2, DFB3, DFB4 and DFB5) and are modelled as resistive connections between nodes that, upon design, did not share a connection [16]. Note that the dynamic behavior associated to DFO4 has been observed at high temperatures (125 °C) or when the defect has been modelled with expressively big resistances. However, DFB5 only caused dynamic coupling faults on defect-free cells that share a connection, such as same BLs, with a cell affected by this defect. Thus,

based on these results it is possible to observe the frequency regarding the occurrence of dynamic faults, being a real challenge when thinking about manufacturing test procedures.

B. *Fault Mapping*

To identify defect sizes that cause faults on SRAM cells, the automated tool presented in [9] was adopted. The tool performs an extensive mapping process by simulating defective cells with progressively stronger defects until an inconsistent behavior is detected. The tool analyses static faults with the cells without operation and through simple read and write operations: *0w0, 0w1, 1w0, 1w1, 0r0, and 1r1*. To find the resistance that results in dynamic faults, a write sequence is executed and successive read operations are performed: $0w0(r0)^n$, $0w1(r1)^n$, $1w0(r0)^n$, *and* $1w1(r1)^n$, where *n* is the number of consecutive operations.

Applying this methodology, the critical resistance, which is defined as the weakest defect able to sensitize any fault, is obtained. For resistive-open defects, this represents the smallest resistance causing faults. For resistive-bridge, the opposite applies, and the greatest resistance able to sensitize faults is considered as the critical resistance.

4 Results and Discussion

This Section summarizes the main results gathered during the HSPICE simulations. In more detail, the results show the relation between the faulty behavior associated to resistive defects and the power supply voltage adopted. It is important to mention that the work presented in [10] adopted a 65 nm technology node for the CMOS-based SRAM cell and in order to provide a more technology independent comparison we decided to change the technology and adopted a 22 nm technology node for designing the CMOS-based SRAM, since the FinFET version adopts a 20 nm technology node. In addition, we extended the analysis of the operating condition impact on defective SRAM cells, which was focused on operating temperatures in [10], additionally including the power supply voltage as one of the players. First, an evaluation of the critical resistances considering three different operating temperatures is presented. Further, a fault analysis of every resistive defect considering a range of power supply voltages has been performed, providing a more complete overview of the operating conditions impact on the SRAM cell faulty behavior when compared to the conclusions presented in [10]. Basically, the nominal voltage has been varied around 0.2 V, assuming a step of 0.05 V. This means that for the FinFET-based

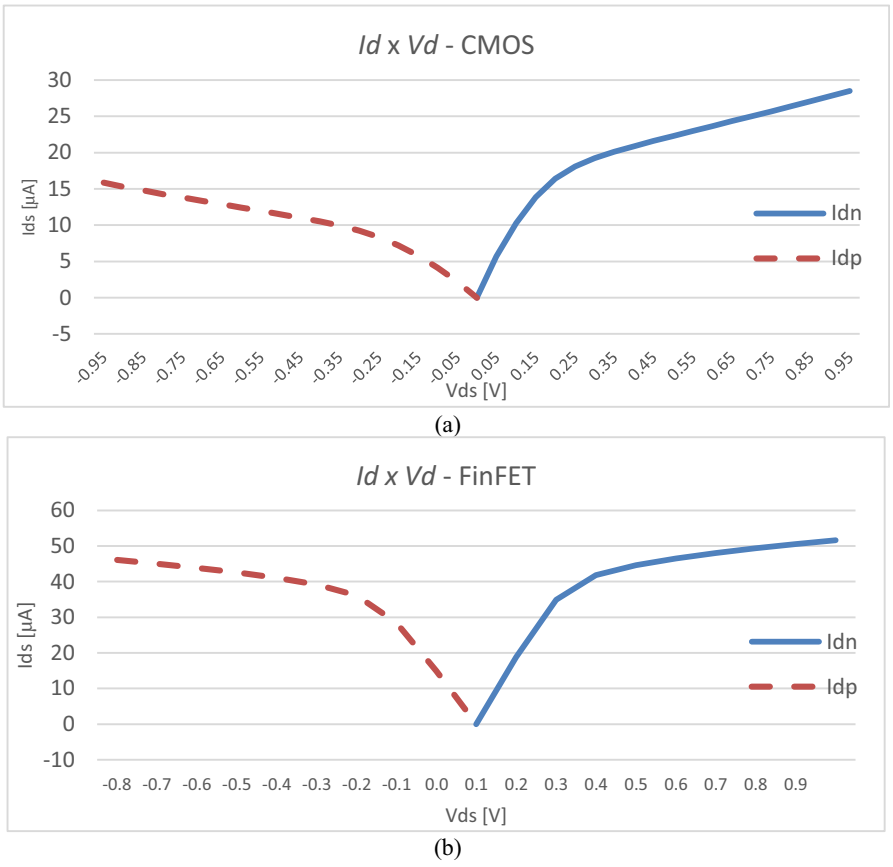

Figure. 4. Id x Vd curves for (a) a CMOS transistor and (b) a FinFET.

SRAM, the power supply voltage varied from 0.7 V to 1.1 V. However, the power supply voltage for the CMOS-based SRAM varied from 0.9 V to 1.15 V only, since the circuit lost its synchrony when operating at a power supply voltage smaller them 0.9 V. Thus, the experiments performed aim to provide a functional analysis of the SRAM cells, at a certain power supply voltage, varying the defect size until a fault occurs.

Fig. 4 compares the *Id* x *Vd* curves of the transistors used to form the coupled inverters of the studied SRAM blocks. The comparison relies on the CMOS transistors and FinFETs used at the SRAM cells. The gate voltage was kept constant at the nominal voltage (*Vdd*) of each technology, as well as at *Gnd*, depending on the device type (*n* or *p*). Observing Fig. 4 (a) it is possible to see that the saturation currents of the pFET and the nFET are of 46 μA and 52 μA, respectively. Fig. 4 (b) depicts the saturation currents of the pMOS and nMOS transistors, being of 16 μA and 29 μA, respectively. The magnitude of the drain current for nMOS is about twice the pMOS. This happens because the same W was adopted for both transistors' types. For FinFETs, the drain currents are similar, the pFET has a similar behavior to the nFET, with reverse bias. Despite the similar dimensions adopted for designing the CMOS and FinFET SRAM cells, the *Id* of the nFET is 79% larger than the one associated to the nMOS transistor. Considering the pFET and pMOS, this difference is still more significant, pFET being about 180% larger.

A. *Impact of Temperature on Critical Resistances*

Before performing the experiments aiming the evaluation of the power supply voltage impact on the behavior of defective SRAM cells, a set of simulations has been performed in order to identify the critical resistance considering three different operating temperatures. Table I and Table II present the critical resistances obtained by performing simulations considering three different temperatures and the associated faulty behavior for each kind of defect. Resistances from 0 Ω to 30 MΩ have been injected in the SRAM blocks according to Fig. 3. It is important to point out that the temperatures adopted for the CMOS- and for the FinFET-based SRAMs are different because the CMOS-based SRAM was not able to properly operate considering the corner temperatures (−40 °C, 27 °C and 125 °C). Basically, the CMOS-based SRAM cells have been designed based on the FinFET design parameters, generating an SRAM cell that is not robust enough to operate at a temperature higher than 62 °C.

Table I CMOS-based SRAM – Critical Resistances

Defect	Temperature		
	−39 °C	**27 °C**	**62 °C**
DFO1	49.60 kΩ (TF)	169.4 kΩ (TF)	21.80 kΩ (IRF)
DFO2	25.40MΩ (TF)	5.252MΩ (dRDF)	23.54MΩ (dRDF)
DFO3	490.8 kΩ (IRF)	23.40 kΩ (IRF)	1.550 kΩ (IRF)
DFO4	–	6.349MΩ (TF)	158.78 kΩ (TF)
DFO5	3.174MΩ (TF)	1.295MΩ (IRF)	157.2 kΩ (IRF)
DFO6	3.174MΩ (TF)	1.607MΩ (TF)	524.0 kΩ (dRDF)
DFB1	117.1 kΩ (NSF)	253.7 kΩ (WRF)	2.091MΩ (IRF)
DFB2	15.48 kΩ (TF)	45.16 kΩ (dDRDF)	180.7MΩ (IRF)
DFB3	113.2 kΩ (RDF)	363.5 kΩ (DRDF)	1.486MΩ (IRF)
DFB4	18.52 kΩ (TF)	53.81 kΩ (SAF0)	79.01 kΩ (IRF)
DFB5	2.569 kΩ (dRDF)	9.237 kΩ (TF)	28.29 kΩ (TF)

Table II FinFET-based SRAM – Critical Resistances

Defect	Temperature		
	−40 °C	**27 °C**	**125 °C**
DFO1	16.9 kΩ (TF)	15.3 kΩ (TF)	15.3 kΩ (TF)
DFO2	297 kΩ (dDRDF)	144 kΩ (dDRDF)	73.0 kΩ (dRDF)
DFO3	137 kΩ (dDRDF)	71.5 kΩ (dDRDF)	37.2 kΩ (dRDF)
DFO4	–	–	6.6MΩ (dRDF)
DFO5	1.40MΩ (TF)	1.47MΩ (TF)	1.60MΩ (TF)
DFO6	2.58MΩ (TF)	2.46MΩ (TF)	2.23MΩ (TF)
DFB1	54.4 kΩ (WRF)	41.6 kΩ (WRF)	30.8 kΩ (WRF)
DFB2	13.9 kΩ (dRDF)	13.8 kΩ (dRDF)	14.8 kΩ (dRDF)
DFB3	54.6 kΩ (dRDF)	46.4 kΩ (dRDF)	37.8 kΩ (dRDF)
DFB4	14.1 kΩ (dIRF)	14.1 kΩ (dIRF)	12.8 kΩ (dRDF)
DFB5	1.74 kΩ (TF)	2.13 kΩ (IRF)	3.53 kΩ (IRF)
	57.5 kΩ (dCFir)	49.5 kΩ (dCFir)	38.2 kΩ (dCFir)
DFB6	11.61 kΩ (SAF)	10.92 kΩ (SAF)	10.52 kΩ (SAF)
	52.6 kΩ (dCFir)	44.0 kΩ (dCFir)	32.0 kΩ (dCFir)

Observing Table I it is possible to see that for DFO1 decreasing of the temperature, from 27 °C to −39 °C, makes the cell less robust with respect to the occurrence of TFs. When considering DFO2, it is possible to observe the occurrence of dynamic faults at 27 °C as well as at 62 °C. For DFO3, DFO4, DFO5 and DFO6, the temperature increasing makes the SRAM cells less robust, since the critical resistance value is smaller when operating at 62 °C than at 27 °C. Considering the resistive-bridge defects, the increasing of the temperature affects the robustness of the cell in the presence of the defects. In other words, a fault is easier sensitized at logic level when the temperature increases.

Table II shows that no dynamic behavior was observed when injecting DFO4 into a cell that operates at −40 °C and 27 °C. However, when comparing to the CMOS-based SRAM cell, the injection of DFO4 did not cause dynamic faults, just TFs when operating at 27 °C and 125 °C. It is important to highlight that, for resistive-open defects, the resistance able to cause a fault at 27 °C is much bigger in CMOS- than in FinFET-based SRAM cells. In other words, the FinFET-

based SRAM cell is less robust than the CMOS one, since a smaller defect is able to propagate a fault at logic level. The opposite behavior is observed when considering resistive-bridge defects.

Observing the results summarize in Table I and Table II it is possible to see that temperature plays an important role with respect to fault propagation at logic level. For DFO4, it is possible to observe that no fault is propagated at logic level unless the test procedure is performed with an operating temperature of 125 °C. In more detail, this means that for the temperature of −40 °C and 27 °C the defective SRAM cell does not propagate any fault and the circuit could be considered fault free. In addition, it is possible to see that for some cases the kind of fault associated to the critical resistance can change according to the operating temperature. This situation is observed for DFB5, for example.

B. *Impact of Power Supply Voltage on the Fault Occurrence*

In order to understand the impact of power supply voltage on the functional behavior of CMOS- and FinFET-based SRAM cells in the presence of resistive defects, electrical simulations have been performed considering the following parameters:

- *FinFET-based SRAM*: power supply voltage varying from 0.7 V to 1.1 V, adopting steps of 0.05 V;
- *CMOS-based SRAM*: power supply voltage varying from 0.9 V to 1.15 V, adopting steps of 0.05 V. It is important to mention that a further reduction of the power supply voltage was not possible because the CMOS-based SRAM lost synchronism, as the circuit becomes slower.

Note that the nominal power supply voltage for CMOS- and FinFET-based SRAMs are of 0.95 V and 0.9 V, respectively.

In the next figures, the faulty behavior associated to resistive-open defects will be analyzed while varying the power supply voltage. Fig. 5 depicts the behavior of the CMOS- and FinFET-based SRAM cell in the presence of DFO1. Observing Fig. 5 it is possible to observe the occurrence of TFs for both circuits. However, when comparing the CMOS- with the FinFET-based SRAM cell it is possible to observe that increasing the power supply voltage makes the FinFET-based SRAM cell less robust in the presence of weak resistive-open defects. In other words, a TF is already observed for a really small DFO1 when increasing the power supply voltage. Thus, comparing a CMOS- and a FinFET-based SRAM cell adopting a power supply voltage bigger than 1.0 V, it can be stated that CMOS-based SRAMs are more robust, since a bigger resistive-open defect needs to be considered in order to propagate a TF at logic level. Moreover, considering a power supply voltage of 0.9 V it is possible to see that it is necessary to inject a bigger defect in the FinFET-based SRAM cell than in the CMOS-based one for propagating a faulty behavior. A resistance value smaller than 1Ohm is sufficient to propagate a TF in the CMOS cell. However, a defect bigger than 1.5Ohm is needed to cause a TF at FinFET-based cell. Other important consideration is related to the fact that in order to detect weak defects it becomes necessary to adopt a power supply voltage smaller than the nominal one for the CMOS-based cell while a bigger than the nominal is needed when dealing with FinFET- Faulty behavior associated to DFO1: (a) CMOS- and (b) FinFET-based SRAM cell.

Fig. 6 depicts the results related to DFO2. The observed faulty behavior, when varying the power supply voltage and increasing the defect size, is similar to the one observed when injecting a DFO1. The difference is that instead of observing a TF only, it is also possible to observe a dRDF at the CMOS-based SRAM cell. For the FinFET-based SRAM cell, dDRDF, dRDF and DRDF are observed. Moreover, the faulty behavior of the two considered versions of SRAM cells is completely different when applying the same power supply voltage of 0.9 V. Observing the graphs presented in Fig. 6, it is possible to see that a smaller defect is able to propagate a fault at logic level when considering the CMOS-based cell. Another important point here is that considering the minimal power supply voltage of both SRAM cells, the defect size necessary to

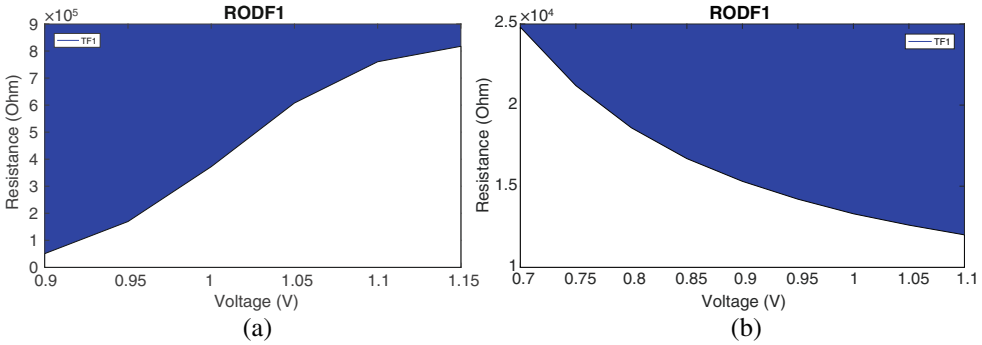

Figure. 5. Faulty behavior associated to DFO2: (a) CMOS- and (b) FinFET-based SRAM cell.

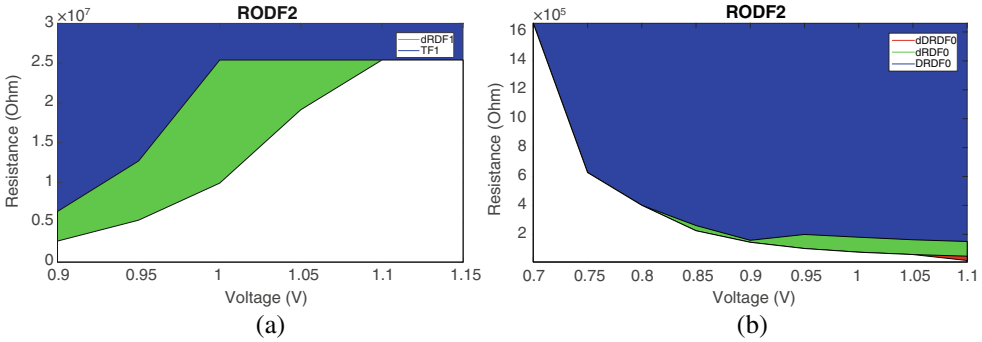

Figure 6. Faulty behavior associated to DFO5: (a) CMOS- and (b) FinFET-based SRAM cell.

propagate a fault is bigger when considering the FinFET-based cell than in the CMOS one. Note that the faulty behavior observed when injecting a DFO3 is similar to the one observed when considering a DFO2.

The injection of a DFO4 causes faults only when considering a CMOS-based SRAM cell. In other words, no faults are propagated at logic level when analyzing the FinFET-based cell. Thus, the results obtained when simulating the CMOS-based SRAM cell in the presence of DFO4 show that it is necessary to have a bigger defect, which means a bigger resistance value, for propagating a TF when increasing the power supply voltage.

Fig. 7 depicts the faulty behavior observed when injecting DFO5. The graphs show a similar behavior when varying the power supply voltage. Basically, the increase of the power supply voltage makes the cells more robust, since it is necessary to inject a slightly bigger resistance to propagate a fault at logic level. Despite the very similar behavior, the defective CMOS-based SRAM cell also causes an IRF, a fault never observed at the FinFET cell. Regarding the minimum power supply voltage adopted during the experiments, it is possible to see that it is necessary to inject a bigger defect in the FinFET-based cell to observe a TF when compared to the CMOS-based cell. For both technologies, the results depicted in the graphs of Fig. 7 indicates that it is easier to propagate faults adopting the minimum power supply voltage during the teste procedure, since it is necessary to have a bigger defect when considering the nominal power supply voltage for guaranteeing the fault propagation.

The faulty behavior is completely different when injecting DFO6. While the other defects cause different scales of the same faulty behavior, DFO6 causes CMOS and FinFET to react contrarily. Fig. 8 shows that DFO6 causes dynamic faults at the FinFET-based SRAM cell. On one hand, it is possible to observe that the increase of power supply voltage makes the CMOS-based SRAM cell more robust, since it is necessary to inject a stronger resistive-open defect to propagate a faulty behavior at logic level. On the other hand, the impact of increasing the power supply voltage on the defective FinFET-based SRAM cell is negative, since a weaker defect is able to cause TFs. In addition, it is possible to see that by applying a power supply voltage of around 0.9 V one is able to propagate faults caused by defects with around 1Ohm when considering the CMOS-based SRAM and around 2.4Ohm at the FinFET-based SRAM. Note that depending on the defect size we can have static or dynamic faults. When considering the impact of defect size, it can be stated that dynamic faults are associated to weak defects that are related to small defect sizes. In the case of DFO6, it is possible to see that a weaker defect, of around 2.4Ohm, causes a dynamic fault when applying a power supply voltage of 0.7 V and a static fault when applying a voltage of 0.9 V. Because the detection of static faults is considered easier than the detection of the dynamic ones, in the case of the FinFET-based SRAM the test should be performed using the nominal power supply voltage.

Before presenting the results related to resistive-bridge defects it is important to mention that a smaller resistance value means a stronger defect. In other words, a weak defect is

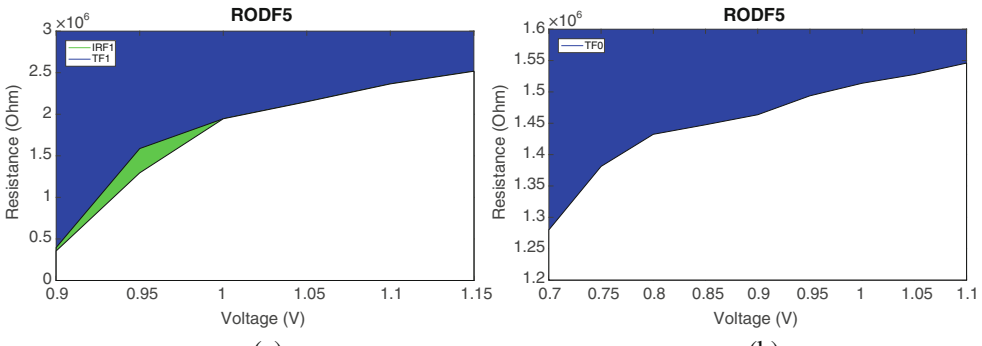

Figure 7. Faulty behavior associated to DFO6: (a) CMOS- and (b) FinFET-based SRAM cell.

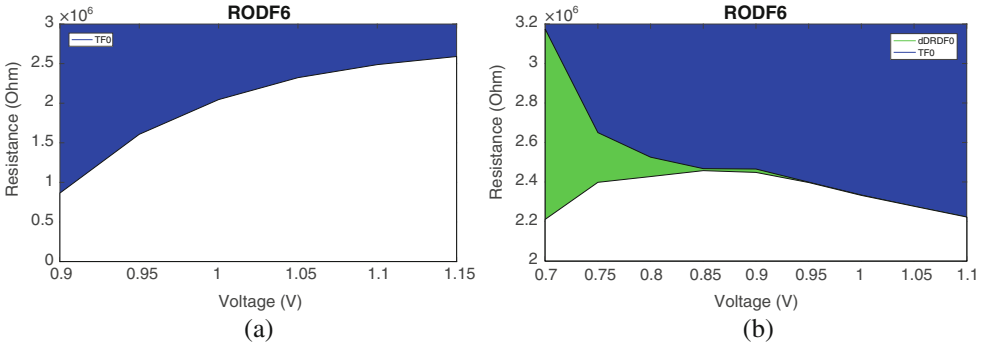

Figure 8. Faulty behavior associated to DFB1: (a) CMOS- and (b) FinFET-based SRAM cell.

modelled using a big resistance, which means that resistive-bridge defects have the invers behavior of resistive-opens. Fig. 9 summarizes the faulty behavior observed when injecting a resistive-bridge defect at position 1 (DFB1). Observing these graphs, it is possible to conclude that the impact of power supply voltage variation is similar for both memory cells. Basically, when increasing the power supply voltage, the defect size necessary to propagate a faulty behavior is bigger. Note that for DFO1, the defective CMOS-based SRAM cell propagates also an IRF, a situation that was not observed when considering the FinFET-based cell. Considering the same power supply voltage of 0.9 V for both technologies, it is possible to see that a fault can propagate to logic level injecting a weaker defect in the CMOS-based SRAM than in the FinFET-based SRAM. In other words, considering the same power supply voltage of 0.9 V, the defective FinFET-based SRAM will propagate a faulty behavior in the presence of a stronger defect, which means a resistance value of at least around 0.8Ohm. In addition, when injecting a defect of 2Ohm in both memories, a fault classified as NSF is observed at the CMOS-based SRAM when applying a 0.9 V of power supply voltage and a WRF is observed at the FinFET-based SRAM when applying a 0.7 V of power supply voltage.

The injection of DFB2 causes three different faulty behaviors. The defective CMOS-based SRAM cell propagates a SAF1, TF and dDRDF. For the FinFET-based SRAM cell we observe RDFs instead of TFs. Another important aspect to be considered is that the type of faults did not change when varying the power supply voltage. It seems that the defect size plays a more important role on the observed faulty behavior.

The injection of DFB3 causes dynamic faults at the FinFET-based SRAM only. Observing the respective graphs, it is possible to see that the defect magnitude necessary to propagate a faulty behavior at logic level changes when increasing the power supply voltage. Basically, a stronger defect is needed in order to propagate the fault at logic level.

A similar behavior is observed when considering a DFB4. However, the impact of increasing power supply voltage when considering the CMOS-based SRAM cell is very expressive, since it is necessary to inject a stronger defect to cause a SAF or a TF, as it is possible to see in Fig. 11 (a). Comparing the behavior between the CMOS- and the FinFET-based SRAM cell, it is possible to see that impact of power supply voltage is less expressive in FinFET-based memories.

A completely different behavior is observed when injecting a DFB5. Fig. 12 (b) shows a faulty behavior overlap with the increasing of power supply voltage. The FinFET-based SRAM cell has a different faulty behavior depending on the value stored in the cell. In more detail, when a cell is storing "0" the defect causes a DRDF and when the cell is storing "1" an IRF is caused. Note that this situation is not observed when applying a power supply voltage smaller than 0.76 V. The increasing of the power supply voltage accelerates the cell output signal and causes a synchrony loss of the flip-flop. However, the region related to the occurrence of TFs decreases with increasing power supply voltages, which means

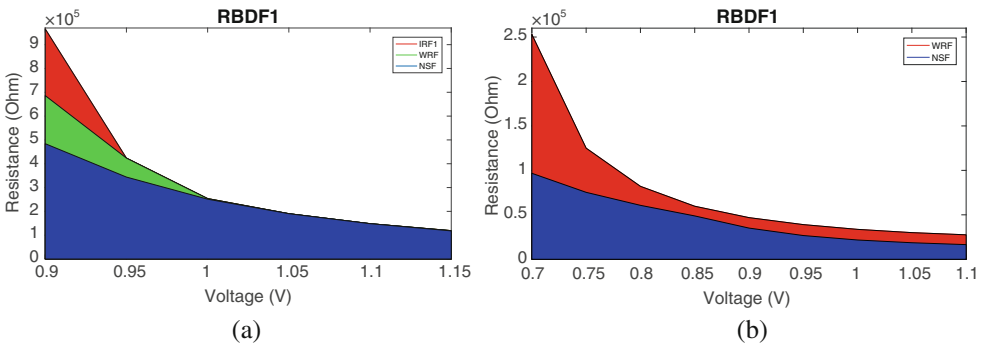

Figure 9. Faulty behavior associated to DFB3: (a) CMOS- and (b) FinFET-based SRAM cell.

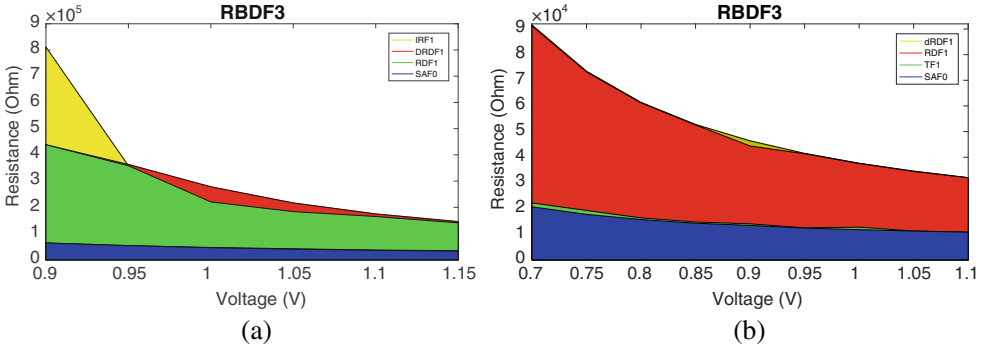

Figure 10. Faulty behavior associated to DFB4: (a) CMOS- and (b) FinFET-based SRAM cell.

that a TF is propagated with stronger defects or in other words with small resistance values.

Finally, Fig. 13 depicts the results observed when varying the power supply voltage for a FinFET-based SRAM cell in the presence of a DFB6. Note that this defect exclusive occurs for this kind of memory cell. It is possible to observe the same tendency observed for the other resistive-bridge defects, except for the DFB5.

I. Final Considerations

The faulty behavior associated to resistive defects in CMOS- and FinFET-based SRAM cells has been analyzed when considering a range of power supply voltages around the nominal one, adopting a variation step of 0.05 V. In more detail, the paper presented an analysis of the impact of varying the power supply voltage on the faulty behavior of defective memory cells. The range of power supply voltages and defects considered was vast and included very weak resistive defects. Critical resistances were individually evaluated for three distinct operating temperatures in order to draw a preliminary conclusion regarding the relation between temperature and defect strength. Further, an analysis regarding the impact of power supply voltage on the faulty behavior of CMOS- and FinFET-based SRAM cells in the presence of resistive defects was performed. The obtained results demonstrate that the power supply voltage plays an important role in the faulty behavior of defective SRAM cells, being more expressive for FinFET-based ones. As observed in [27], the results show a more prominent occurrence of dynamic faults induced by resistive defects in the FinFET-based memories than in the CMOS-based SRAMs. In more detail, the detection of weak resistive-bridge defects in CMS-based SRAM cells can be guaranteed by applying higher operating temperatures. When dealing with FinFET-based SRAMs, the increase of temperature assures the detection of weak resistive-open defects. Considering weak resistive-bridge defects, the opposite behavior is observed. The results regarding the analysis of the power supply voltage impact on the behavior of defective cells aggregates relevant insight regarding the behavior of FinFET-based memory cells affected by manufacturing resistive defects. In general terms, the detection of weak defects can be facilitate adopting a power supply voltage below the nominal one when considering CMOS-based SRAMs. The opposite behavior is observed when dealing with FinFET-based SRAMs. A particular situation is observed when injecting DFO6 in the FinFET-based SRAM cell where the detection of weak defects can be guaranteed when applying the two extreme power supply voltages. Comparing the CMOS- and the FinFET-based SRAM it is possible to conclude that equal defect sizes are propagated to logic level using two different power supply voltages - 1.05 V for the CMOS and 0.9 for the FinFET version. When analyzing the results related to the resistive-bridge defects it is possible to observe a tendency where for detecting weak defects a power supply voltage smaller than the nominal one is required. Finally, this work introduces an analysis of the power supply voltage impact, showing how test manufacturing procedures for FinFET memories can benefit from properly adjusting the operating power supply voltage to detect resistive defects and avoid test escapes.

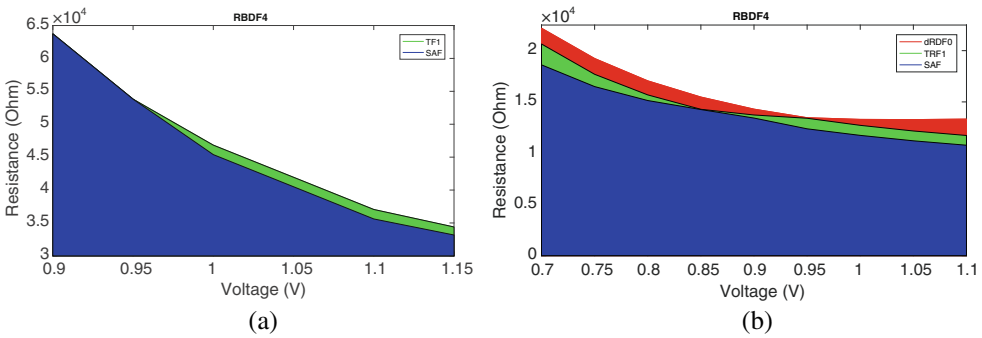

Figure 11. Faulty behavior associated to DFB5: (a) CMOS- and (b) FinFET-based SRAM cell.

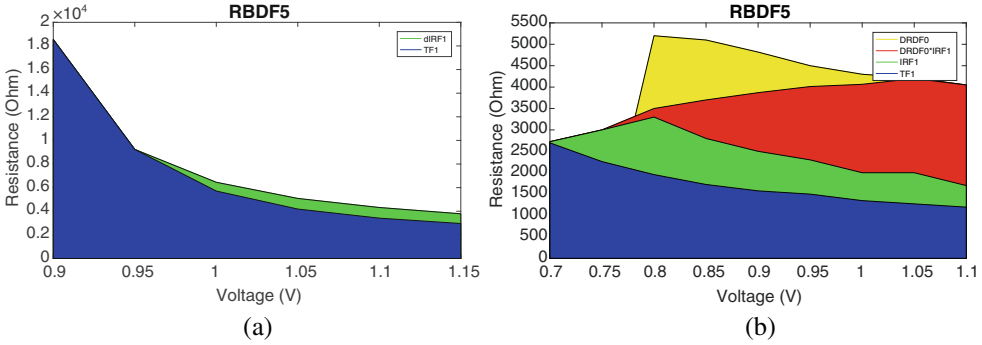

Figure 12. Faulty behavior associated to DFB6: FinFET-based SRAM cell.

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