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IEEE Photonics Journal

DOI:
10.1109/JPHOT.2021.3121168

E-pub ahead of print: 01/12/2021

Peer reviewed version

Timing Jitter Analysis and Mitigation in Hybrid OFDM-DFMA PONs

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***Abstract*—Hybrid orthogonal frequency division multiplexing-digital filter multiple access passive optical networks (OFDM-DFMA PONs) offer a cost-effective solution to the challenging requirements of next-generation optical access networks and 5G and beyond radio access networks. It is crucial to consider the impact of timing jitter in any ADC/DAC-based system, therefore this paper presents an in-depth investigation into the impacts of DAC/ADC timing jitter on the hybrid OFDM-DFMA PON's performance. We introduce improved accuracy white and coloured, DAC and ADC timing jitter models, applicable to any DSP-based transmission system. We prove that DAC and ADC timing jitter effects are virtually identical and investigate the effects of white/coloured timing jitter on upstream performance in hybrid OFDM-DFMA PONs and determine the associated jitter-induced optical power penalties. To mitigate against the timing jitter-induced performance degradations, a simple, but highly effective DSP-based technique is implemented which increases robustness against the timing jitter effects and significantly reduces timing jitter-induced optical power penalties. This consequently relaxes DAC/ADC sampling clock jitter requirements and so reduces implementation costs. White (coloured) timing jitter effects are shown to be independent of (dependent on) ONU operating frequency band and a trade-off between DAC and ADC jitter levels can be exploited to reduce ONU costs.**

***Index Terms*— 5G, analogue-digital conversion, digital-analogue conversion, digital filter multiple access, digital signal processing (DSP), orthogonal frequency division multiplexing (OFDM), passive optical networks (PONs), timing jitter.**

I. Introduction

To satisfy the rigorous requirements imposed by future 5G networks such as ultra-reliable low latency connections, massive device connectivity and the ever-increasing demands for higher capacity, all delivered in a cost and energy-efficient manner [1], [2], it is essential to offer elastic, flexible, dynamic and high-performance optical networks which seamlessly converge the traditional mobile and fixed networks into cloud access networks (CANs) [3]. These converged networks can thus offer greater network bandwidth utilisation efficiency and flexibility via features such as shared, on-demand bandwidth provision [4], [5]. Moreover, there is a pressing need to redevelop the currently existing inflexible vendor locked-in network infrastructure to support a centralized abstraction and virtualization of the network infrastructure using the software-defined networking (SDN) platform. The SDN architecture with its network control being extended into the physical layer provides excellent operational agility and optimum resource utilization as multiple services share a common multi-vendor dynamic architecture with a flexible multi-layer controllability. Therefore, to be compatible with the SDN paradigm future optical access networks are also required that support the corresponding SDN functionality across all layers.

To address the aforementioned technical challenges, a digital filter multiple access passive optical network (DFMA PON) based on intensity modulation and direct detection (IMDD) has been proposed [6], [7] which offers significantly increased flexibility with the use of SDN-controllable, software-reconfigurable digital shaping filters at the transmitter side and their corresponding matching filters at the receiver side to realize dynamic multiplexing of multiple independent user channels within the available PON bandwidth. However, the number of digital signal processing (DSP)-based matching filter processes required at the optical line terminal (OLT) is proportional to optical network unit (ONU) count, therefore, accommodating more ONUs results in an increased OLT DSP complexity.

To overcome this challenge, very recently, a hybrid orthogonal frequency division multiplexing (OFDM)-DFMA PON based on IMDD has been proposed [8], [9], where for upstream transmissions, ONUs utilize software-reconfigurable digital shaping filters to locate their OFDM signals at different sub-wavelength (SW) spectral regions, whereas a single fast Fourier transform (FFT) operation, followed by simple parallel data recovery processes, is now employed to achieve a matching filter-free OLT architecture. The hybrid OFDM-DFMA PON maintains all salient features of DFMA PONs whilst achieving both reduced OLT receiver DSP complexity and greatly enhanced upstream performance compared to DFMA PONs. However, as the hybrid OFDM-DFMA PON is based on high-speed DSP combined with multi-Giga-samples/s (multi-GS/s) digital-to-analogue converters (DACs), and analogue-to-digital converters (ADCs), and as low jitter GHz speed clock sources are expensive, it is crucial to explore the random sample timing jitter (referred to as timing jitter throughout the paper) performance degradation mechanisms

This work was supported by the DSP Centre of Excellence funded by the European Regional Development Fund (ERDF) through the Welsh Government *(Corresponding author: R. P. Giddings).*

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and identify effective approaches to mitigate their impacts on hybrid OFDM-DFMA PON performance.

In any DSP-based system including DACs/ADCs, timing jitter is mainly caused by the thermal noise and thermal vibrations of the semiconductor crystal structure of sampling clocks used to drive the DACs and ADCs which lead to random fluctuations of their clock signal edges from their ideal positions [10]–[12]. Also, internally induced aperture jitter is prevalent in practical ADCs, this is caused by the uncertainty of the aperture time during disconnecting the hold capacitor from the input buffer amplifier inside the sample-and-hold circuit when switching from the sample mode to the hold mode [13], [14]. Depending on the implementation of the sampling clock source and the specific architecture of the DAC/ADC, timing jitter is classified as white when timing jitter values at different samples are independent, whereas coloured timing jitter values are interdependent.

Timing jitter can potentially be a significant performance-limiting factor, especially at multi-GS/s sampling speeds [15], [16]. Thus, an understanding of the trade-off between timing jitter and system performance such as receiver optical power penalty is essential for transceiver design, as it will help determine the specifications of components such as clock sources, DACs, and ADCs. Moreover, for practical systems operating at multi-10GS/s, the practical levels of ADC timing jitter can be of the order of only ~1% unit interval root-mean-square (UI_{rms}) [17]–[20], also attractive low cost, low power CMOS digital phase-locked loop (DPLL)-based oscillators, can have timing jitters of around 1 – 4.5% UI_{rms} [21]–[24]. It is therefore important to investigate the hybrid OFDM-DFMA PONs jitter-induced optical power penalty at these practically realisable jitter levels. Thus, to limit jitter-induced optical power penalty the maximum allowed DAC/ADC jitter specification can then be determined.

The work in [25]–[27] presented a DAC timing jitter model which calculates a sample-error sequence, by multiplying the derivatives of the signal by the timing jitter values, however, this timing jitter model is only accurate for low frequencies much smaller than the sampling frequency [27], [28]. The work in [29] introduced a white ADC timing jitter model that is specifically applicable only to OFDM-based systems and requires an increase to the OFDM inverse FFT (IFFT) size to perform oversampling. Several pieces of research have analysed the effects of DAC and ADC timing jitters on OFDM-based point-to-point systems [15], [16], [29]–[33], the work in [32] theoretically analysed the relation between the error vector magnitude (EVM) of the received subcarriers and the DAC's white sampling clock jitter in an OFDM transmitter but did not consider coloured DAC timing jitter. In [15], the authors introduced a white ADC timing jitter matrix and numerically investigated timing jitter-induced inter-carrier interference (ICI), phase rotational effects, and the bit error ratio (BER) degradation due to white ADC timing jitter. Whereas, the work in [16] analysed the ICI caused by white and coloured ADC timing jitters on OFDM-based ultra-wideband (UWB) systems. Moreover, the work in [16], [33] shows that white ADC timing jitter-induced ICI in OFDM-based systems can be reduced by oversampling the signal at the receiver's ADC, however, this requires an ADC with a higher sampling rate which leads to increased costs. In addition, oversampling in the ADC is seen to have limited effectiveness when ADC timing jitter is coloured, as increasing the sampling rate causes the timing jitter at adjacent samples to become more and more correlated [16], moreover it is completely ineffective against white/coloured DAC timing jitter. Furthermore, all the aforementioned research considered OFDM-based systems with only either DAC or ADC timing jitters. Whereas in reality, both DAC and ADC timing jitters exist together in any practical system, thus the total system timing jitter can be a mixture of white/coloured DAC and ADC timing jitters. Therefore, in this work, the effects of different combinations of white/coloured DAC and ADC timing jitters are investigated and compared. Also, none of the aforementioned research considered the existence of an optical transmission channel, which is crucial to fully understand the impact of timing jitter in optical systems, therefore this work investigates the impact of DAC/ADC timing jitter on optical power penalty.

In this paper, we introduce both DAC and ADC timing jitter models based on the DAC timing jitter models in [25]–[27] and ADC timing jitter model in [29], but with improved accuracy. The improved models can be serially combined as standalone algorithms to simulate the jitter effect in any DSP-based transmission system without the need to change any transmission system parameters. The improved DAC and ADC jitter models are independent of each other and can be either individually deployed or used together to offer different combinations and mixtures of white/coloured DAC and ADC timing jitters as needed. Similar to [25]–[27], our DAC timing jitter model is based on the conversion of timing error into an amplitude error that can be added to the ideal output signal, but in addition, oversampling is employed in our model to increase its accuracy. Our ADC timing jitter model, based on first-order Lagrange fractional delay filters, also employs oversampling for increased accuracy. Both models are very effective for analysing phase rotation and ICI effects caused by timing jitters. In addition, both models support any modulation format and any sampling rate.

In this paper, we fully describe and validate our improved timing jitter models where the accuracy of our models is examined by comparing our model's results with the theoretical results in [15], [16], [32], [34], where numerical analysis is applied to show the theoretical analysis is highly accurate. The models are then used to extensively investigate the effect of white/coloured DAC and ADC timing jitters on the upstream transmission performance of a four-ONU hybrid OFDM-DFMA PON where it is shown that the effects of DAC and ADC timing jitters are virtually identical. It is also shown that, to achieve BERs below the adopted forward error correction (FEC) limit of 1×10^{-3}, the maximum tolerable white DAC/ADC timing jitter is 8% UI_{rms} (in total) when one sideband is chosen for processing at the OLT, however applying a simple DSP-based Joint Sideband Processing (JSP) technique, can mitigate the timing jitter effect and increases the jitter robustness up to 12.5% UI_{rms}. When an optical transmission link is considered, there is an associated jitter-induced optical power penalty when compared with the received optical power (ROP) of a jitter-free

system. We show that JSP greatly reduces the timing jitter-induced optical power penalty, for example, at a fixed EVM of -17dB with white DAC, ADC or total timing jitter of 8% UI_{rms}, the optical power penalty is reduced by 4.8dB, whereas for the case of coloured timing jitter even higher optical power penalty reductions are achieved, with some ONUs failing to achieve EVMs below -17dB at certain jitter levels unless JSP is applied. Moreover, the results reveal that white DAC and ADC timing jitter with a combined total level of approximately >5% (8%) UI_{rms} start to rapidly dominate over other PON induced noise and distortions when processing one (both) sideband(s) and all ONUs are equally impacted regardless of their operational frequency band. The impact of coloured timing jitter is however dependent on an ONU's operational frequency band as ONUs operating in lower (higher) frequency bands, see the jitter start to dominate the performance at higher (lower) jitter values. In addition, we also show the important result of trading-off the effects of highly jittered DAC clock sources by using a low jittered ADC clock source, this result has a significant impact for practical PONs as it permits the use of lower-cost clock sources at the cost-sensitive ONUs. The effects of combined white DAC and coloured ADC timing jitters are also investigated, the dominating jitter is shown to be ONU operating frequency band-dependent due to the frequency-dependent characteristics of coloured timing jitter-induced ICI.

II. DAC AND ADC TIMING JITTER MODELS

A. DAC and ADC timing jitters

Timing jitter is generally modelled as a wide sense stationary (WSS) Gaussian process with a zero mean and characterized by its normalized standard deviation relative to the sampling unit interval T_s which is also called the normalized RMS value. White timing jitter values are uncorrelated, while we assume a Gaussian correlation relationship between coloured timing jitter values, the correlation coefficient between timing jitters at the b^{th} and l^{th} samples is as follows [16]:

$$\rho_{b-l} = e^{-\alpha^2(b-l)^2} \tag{1}$$

where α is the correlation factor, thus a smaller α corresponds to a higher level of correlation. $\alpha = 0$ indicates that all timing jitter values are 100% correlated and the effect of the timing jitter becomes identical to the effect of sample timing offset (STO). As α increases, the correlation relationship between successive timing jitter values decrease which whitens the observed timing jitter.

It is worth noting that clock timing jitter is commonly observed in the frequency domain as oscillator phase noise. Depending on the internal circuitry of the oscillator, the oscillator timing jitter can either be white or coloured. It is very common to observe different regions in a free-running oscillator phase noise spectrum. A phase noise power spectral density (PSD) proportional to f^{-2} which corresponds to a constant slope of -20dB/decade [35], [36] is often caused by white frequency noise resulting in white timing jitter, whereas a phase noise PSD with a more complex dependency on frequency is usually due to coloured noise such as flicker noise and causes coloured timing jitter. The characteristics of phase locked loop (PLL)-based clocks for example, always results in coloured timing jitter. For the coloured timing jitter adopted here with a Gaussian correlation relationship, the level of correlation has an influence on the phase noise PSD.

The ideal output signal of a zero-order hold (ZOH) non-return-to-zero (NRZ) DAC [37] (referred to as DAC throughout the paper) consists of a sequence of rectangular pulses with a constant width equal to the sampling interval T_s. Timing jitter causes a random change in the width of the pulses denoted as $(T_s + \tau_{dac}(n))$ where $\tau_{dac}(n)$ represents the DAC timing jitter, and n is the digital sample index. The timing error due to DAC timing jitter is modelled as time-domain slivers added to the ideal output DAC pulses, the error slivers have a random width of $\tau_{dac}(n)$ and a height of $[r_{in}(n) - r_{in}(n-1)]$, where $r_{in}(n)$ is the DAC input digital signal [27]. However, this requires a fine time step, i.e., an increased sampling rate, to model DAC timing jitter in time-based numerical simulations. Therefore, to maintain the original sampling rate and thus simplify numerical simulations, the timing error is usually converted into an amplitude error sequence $e_{dac}(n)$ that can be directly added to the ideal output samples. This method is used in [25]–[27], [34], [38], [39] and similarly, the same conversion method is adopted in our analysis. The amplitude error sequence is generally approximated as follows [27], [34], [40], [41]:

$$e_{dac}(n) = \frac{\tau_{dac}(n)}{T_s}[r_{in}(n) - r_{in}(n-1)] \tag{2}$$

ADC timing jitter causes the ADC to sample the signal at the wrong time instants during the analogue-to-digital conversion, which is equivalent to introducing a small random positive or negative delay that is different from sample-to-sample. Therefore, a jittered sample can be obtained by calculating the difference in the amplitude (amplitude error) between the ideal and the jittered samples and adding it to the ideal sample. The amplitude error $e_{adc}(n)$ is approximately proportional to the first derivative of the input signal [27], [29], [42]–[44]:

$$e_{adc}(n) = (\tau_{adc}(n)/T_s)\left.\frac{dy_{in}(t)}{dt}\right|_{t=nT_s} \tag{3}$$

where $y_{in}(t)$ is the input analogue signal at the ADC, and $\tau_{adc}(n)$ denotes ADC timing jitter.

To numerically simulate the ADC timing jitter, we simply filter the ideal signal using first-order Lagrange fractional delay filters [45], [46] with the following general form for filter coefficients:

$$h_n(q) = \prod_{\substack{k=0 \\ k\neq q}}^{N} \frac{(\tau_{adc}(n)/T_s) - k}{q - k}$$
$$q = 0,1,2,\dots N, \qquad n = 0,1,2,\dots, L-1 \tag{4}$$

where q is the index of the filter coefficients, L is the number of samples, and if $N = 1$ this signifies first-order fractional delay filters. Eq. (4) denotes that L fractional delay filters are required to jitter a signal of L samples as a different filter is needed for each sample. According to Eq. (4), the filter

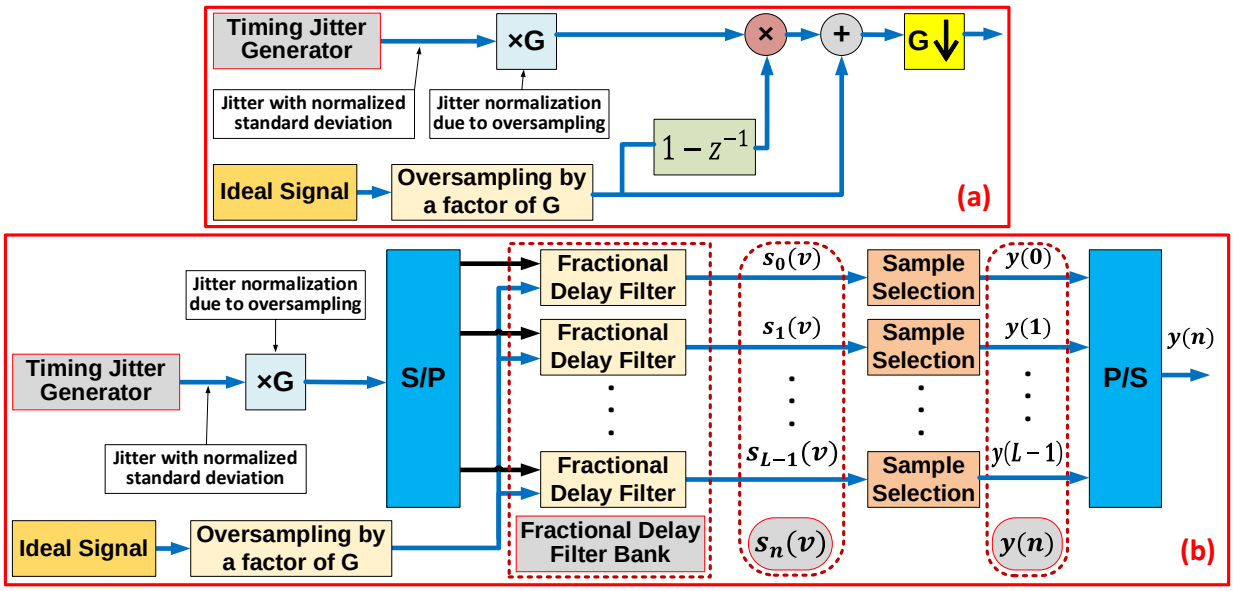

Fig. 1. (a) DAC timing jitter model, (b) ADC timing jitter model.

coefficients of a first-order fractional delay filter for the n[th] sample are:

$$h_n(0) = 1 - (\tau_{adc}(n)/T_s),\ \ h_n(1) = (\tau_{adc}(n)/T_s) \qquad (5)$$

A general form of the output jittered signal after filtering can be written as:

$$\begin{aligned} y_j(n) &= h_n(0).y_{out}(n) + h_n(1).y_{out}(n-1) \\ &= y_{out}(n).\left[1 - \left(\frac{\tau_{adc}(n)}{T_s}\right)\right] + y_{out}(n-1).\left[\frac{\tau_{adc}(n)}{T_s}\right] \\ &= y_{out}(n) + \frac{\tau_{adc}(n)}{T_s}[y_{out}(n-1) - y_{out}(n)] \end{aligned} \qquad (6)$$

where $y_j(n)$ and $y_{out}(n)$ represent the jittered output samples and the ideal output samples respectively. Since the standard deviation σ of random variables is not affected by changing the sign of all random variables:

$$\sigma(\tau_{adc}(n)) = \sigma(-\tau_{adc}(n)) \qquad (7)$$

Then Eq. (6) can be re-written as follows:

$$y_j(n) = y_{out}(n) + e_{adc}(n) \qquad (8)$$

$$e_{adc}(n) = \frac{\tau_{adc}(n)}{T_s}[y_{out}(n) - y_{out}(n-1)] \qquad (9)$$

where $e_{adc}(n)$ represents an ADC jitter error sequence added to the ideal output samples. Eq. (2) and Eq. (9) thus suggest that the effects of DAC and ADC timing jitters are virtually identical.

B. DAC timing jitter model

Similar to the DAC timing jitter model in [25]–[27], our DAC timing jitter model, shown in Fig. 1(a), is based on converting the timing error into an amplitude error sequence as defined in Eq. (2). However, the accuracy of this conversion method is frequency-dependent [27], [28]. Therefore, the ideal signal of L samples is first oversampled by a factor of G by padding zeros in the frequency domain, then the amplitude difference sequence $[r_{in}(n) - r_{in}(n-1)]$ is obtained by filtering the oversampled signal using a digital finite impulse response (FIR) filter with a transfer function of:

$$H(z) = 1 - z^{-1} \qquad (10)$$

The timing jitter generator shown in Fig. 1(a) produces $G \times L$ white or coloured timing jitters with the desired normalized standard deviation (σ_{dac}/T_s), a simple MATLAB function is used to produce white timing jitters, whereas coloured timing jitters with the desired level of correlation are generated according to Eq. (1) using the Cholesky decomposition method [47]. The normalized timing jitters are multiplied by the same oversampling factor G to compensate the effect of oversampling and so to maintain the required normalized level of the DAC timing jitter. The oversampled filtered signal with a length of $G \times L$ is then multiplied by normalized timing jitters $G \times (\tau_{dac}(n)/T_s)$, and then added to the ideal oversampled signal before being down-sampled by the same oversampling factor.

C. ADC timing jitter model

Unlike our DAC timing jitter model where an error sequence is calculated and added to the ideal signal, the ADC timing jitter model in Fig. 1(b) can directly obtain the jittered samples.

To intentionally jitter an ideal signal of L samples, L timing jitters with the desired normalized standard deviation (σ_{adc}/T_s) are generated in a similar manner as in the DAC timing jitter model, where the timing jitters represent fractional delays for the fractional delay filter bank, the latter is composed of L parallel first-order Lagrange fractional delay filters which have limited distortion-free bandwidth as their magnitude response starts to deviate from the ideal characteristic near the Nyquist frequency. To overcome this effect, the ideal signal is oversampled by a factor of G before filtering, thus reducing the relative signal bandwidth, and so restricting it to the undistorted spectral region of the Lagrange filters. Accordingly, the timing jitters are multiplied by the same oversampling factor.

The oversampled signal, with a length of $G \times L$, is filtered L times with the filter bank in a parallel pipelined approach

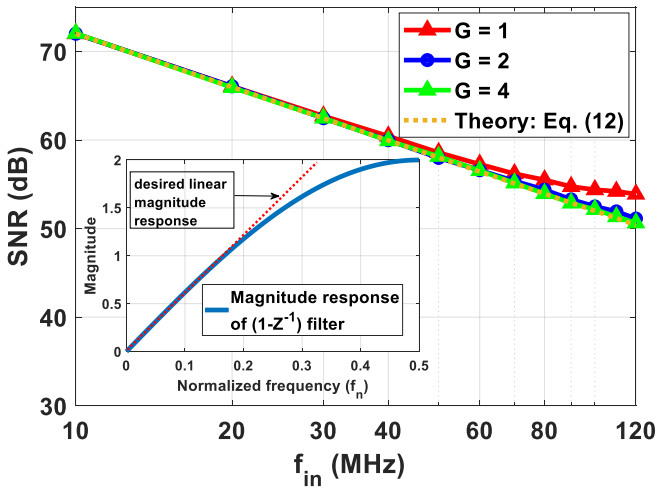

Fig. 2. Verification of simulated DAC timing jitter model. SNR for a sinusoidal signal with $f_{in} = 10MHz$ to $120MHz$, $f_s = 250MS/s$, and $\sigma_{dac} = 4ps$, when using the simulated DAC timing jitter model. The inset shows the magnitude response of the diffrentiator filter $(1 - Z^{-1})$. G: oversampling factor employed in the DAC timing jitter model.

generating L parallel sequences denoted as $s_n(v)$ in Fig. 1(b). Then, only one sample is extracted from each sequence according to the following equation:

$$y(n) = s_n(G \times n) \tag{11}$$

The signal is thus effectively down-sampled by a factor of G and the resultant L samples are then serialised to produce the jittered signal.

D. Verification of the DAC timing jitter model

To verify the accuracy of our proposed DAC timing jitter model and to validate the improvement attained by oversampling the signal prior to jitter addition, similar to [34], a sinusoidal signal affected by white NRZ DAC timing jitter is considered where the theoretical signal-to-noise ratio (SNR) is [34]:

$$SNR_{NRZ} = \frac{1}{4\sigma_{dac}^2 \pi^2 f_{in}^2} \tag{12}$$

where f_{in} is the frequency of the sinusoidal signal, and σ_{dac} is the RMS value of DAC timing jitter. Fig. 2 shows the numerical results when the frequency of the signal is swept between 10MHz and 120MHz, where the sampling rate is $f_s = 250MS/s$ and $\sigma_{dac} = 4ps$. Without considering oversampling of the signal, as in the jitter model in [25], the resultant SNRs at high frequencies near the Nyquist frequency do not match the theoretical values due to the non-linear magnitude response of the employed differentiator filter near the Nyquist frequency as shown in the inset of Fig. 2. In addition, adopting an oversampling by a factor of 2 restricts the signal within normalized frequencies $(f_n' \leq 0.25)$, this enhances the accuracy of the model but the highest frequency components of the oversampled signal are still within the non-linear region of the differentiator filter. An oversampling by a factor of 4 restricts the oversampled signal to be within the linear operating region of the differentiator filter $(f_n'' \leq 0.125)$, and therefore, the resultant SNR simulation result almost perfectly matches the theoretical result. Accordingly, oversampling by a factor of $G = 4$ is chosen for our DAC timing jitter model in Fig. 1(b).

Considering an ideal electrical point-to-point (PTP) OFDM system of 128 subcarriers with only white DAC timing jitter implemented with the DAC jitter model described in Section II.B, the relationship between the subcarrier EVM (dB) and the normalized RMS value of the white DAC timing jitter is shown in Fig. 3(a). The result obtained with our model when the $G = 4$ coincides well with the theoretical analysis developed in [32]:

$$\text{EVM (dB)} \cong 10Log_{10}\left(\frac{\pi^2 \, (\sigma_{dac}/T_s)^2}{3}\right) \tag{13}$$

Due to the mathematical approximation method adopted in [32], there is a small deviation when compared to the EVM results of our DAC timing jitter model (when $G = 4$) when the timing jitter exceeds ~20% UI_{rms}, as shown in Fig. 3(a).

E. Verification of the ADC timing jitter model

To verify our ADC timing jitter model, we consider the same ideal 128 subcarrier OFDM system. Assuming white ADC timing jitter, the resultant ICI power to signal power ratio (P_{ICI}/σ_s^2), where σ_s^2 is the signal power, is found to be independent of the subcarrier index. Fig. 3(b) shows the simulation result of our model when $G = 4$ for subcarrier 0, the result coincides well with the result in [15] and are within the bounds derived in [16]:

$$\frac{\pi^2 \, (\sigma_{adc}/T_s)^2}{3}\left[1 - \frac{3\pi^2 \, (\sigma_{adc}/T_s)^2}{10}\right] \leq \frac{P_{ICI}}{\sigma_s^2} \leq \frac{\pi^2 \, (\sigma_{adc}/T_s)^2}{3} \tag{14}$$

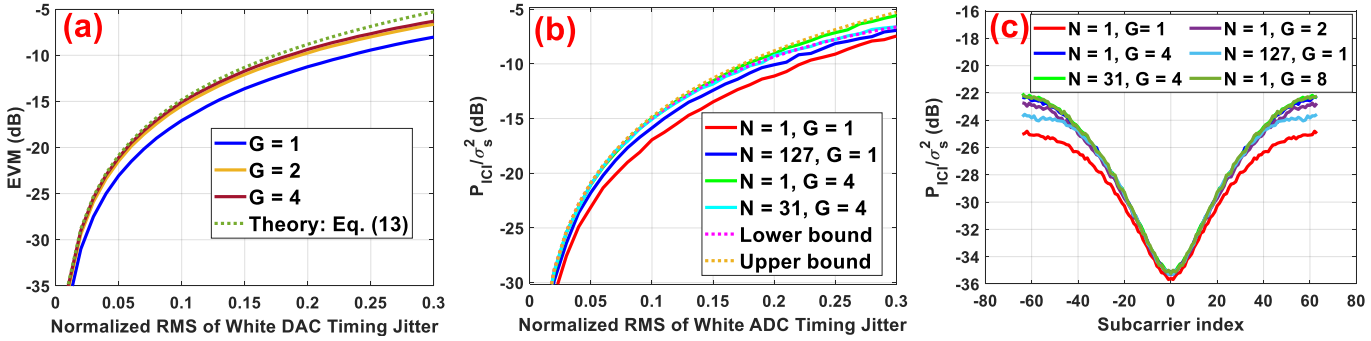

Fig. 3. Verification of DAC and ADC timing jitter models in OFDM-based systems: (a) EVM (dB) of subcarrier 0 vs. normalized RMS value of white DAC timing jitter, (b) ICI power to signal power ratio at subcarrier 0 vs. normalized RMS value of white ADC timing jitter, (c) ICI power to signal power ratio (dB) vs. subcarrier index for an OFDM system with coloured $(\alpha = 0.4)$ ADC timing jitter $(\sigma_{adc}/T_s) = 3\%$ UI_{rms}. G: oversampling factor employed in the DAC/ADC timing jitter model, N: order of fractional delay filters employed in the ADC timing jitter model.

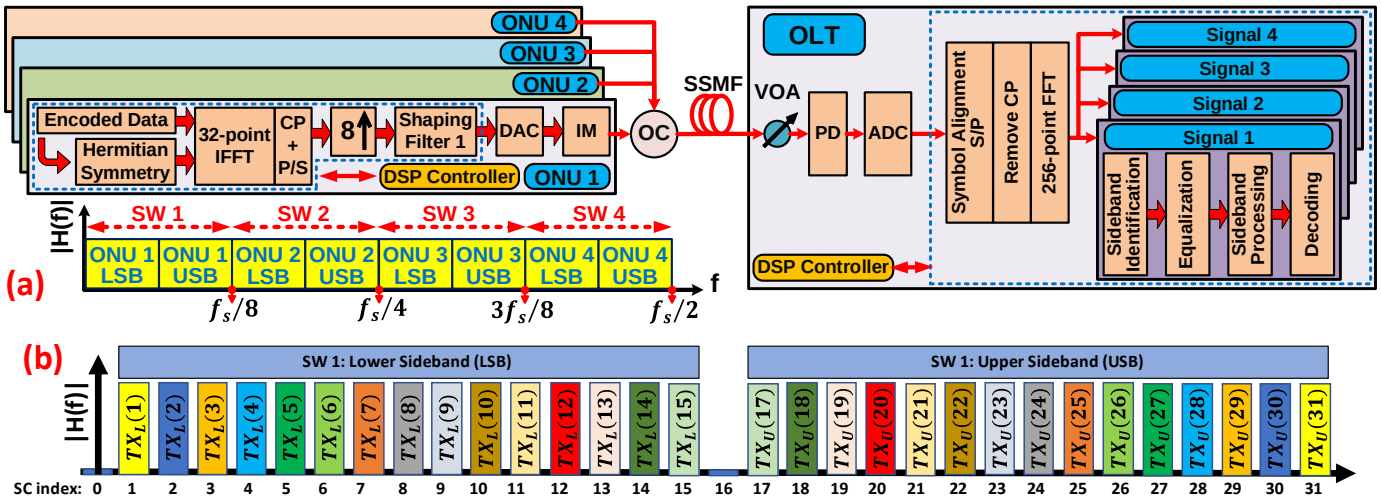

Fig. 4. (a) System setup for four-ONU hybrid OFDM-DFMA PON. (b) conjugate symmetry property of lower and upper sidebands in SW 1. DAC: digital-to-analogue converter, ADC: analogue-to-digital converter, CP: cyclic prefix, S/P: serial-to-parallel conversion, P/S: parallel-to-serial conversion, LSB: lower sideband, USB: upper sideband, IM: intensity modulator, OC: optical coupler, SSMF: standard single mode fibre, PD: photodetector, VOA: variable optical attenuator, f_s: DAC/ADC sampling frequency, SW: sub-wavelength. $TX_L(p)$: transmitted QAM symbols on LSB, $TX_U(p)$: transmitted QAM symbols on USB.

Next, when the ADC timing jitter is coloured with a normalized RMS value of $(\sigma_{adc}/T_s) = 3\%$ UI_{rms}, the ICI becomes subcarrier dependent as shown in Fig. 3(c) where our model results, when $G = 4$, show excellent similarity with the results in [16].

In addition, when an oversampling factor of 4 is employed in our model, the results in Figs. 3(b) and 3(c) confirm that adopting higher-order Lagrange fractional delay filters (31st order) becomes unnecessary and a linear relationship can be assumed between adjacent oversampled samples. Moreover, employing an oversampling factor of 2 slightly reduces the accuracy of the model as illustrated in Fig. 3(c), whereas an oversampling by a factor of 4 is found to be an optimum choice considering both model accuracy and complexity. Also, Figs. 3(b) and 3(c) show that increasing the length of fractional delay filters to 128 taps without oversampling results in less accurate ICI estimations. Therefore, it is essential to oversample the signal before fractional delay filtering. Thus, an oversampling factor of $G = 4$ and first-order Lagrange fractional delay filters are considered optimum for the employed ADC timing jitter model.

III. Numerically Simulated Hybrid OFDM-DFMA PON Architecture

Fig. 4(a) shows the architecture of the numerically simulated four-ONU hybrid OFDM-DFMA PON where signal generation and detection are simulated using MATLAB and the optical fibre transmission is simulated using VPI Transmission Maker. The detailed operating principle of the considered PON, without timing jitter, has been presented in [8], [9]. The key system parameters employed here are listed in Table I, where all applicable system parameters, e.g., DAC/ADC resolution and clipping ratios, are carefully optimised to minimise their impact on system performance and so minimising their impact on timing jitter effect observations.

In each ONU, a real-valued OFDM signal containing 15 data-bearing subcarriers is produced at the output of an IFFT by adopting Hermitian symmetry. To allow comparison with [6], [8], a similar cyclic prefix (CP) length of 25% is adopted. $M\uparrow$ up-sampling operation and Hilbert pair-based reconfigurable in-phase digital shaping filters are then employed to flexibly locate the ONU's signal at the desired SW spectral region where ONU N occupies the Nth SW spectral region as illustrated in Fig. 4(a). Each ONU's signal is then individually clipped, quantized and converted into an analogue signal. Similar to the treatment in [8], [48] after digital-to-analogue conversion, each ONU employs an ideal optical intensity modulator (IM) for the E/O conversion. The utilization of a fixed and common wavelength and the adopted method of coupling different

TABLE I
LIST OF PARAMETERS

Parameter	Value
DAC/ADC Sample Rate	12.5 GS/s
OFDM IFFT/FFT Size	32/256
Data-carrying subcarriers (per ONU)	15
Modulation format	16QAM
Cyclic Prefix	25%
Up-sampling factor (M)	8
DAC/ADC effective number of bits	8 bits
Clipping Ratio	13 dB
Digital Filter Length	64
Excess of the Bandwidth	0
Net bitrate per ONU	2.344 Gb/s
Raw bitrate per ONU	2.93 Gb/s
ONU Optical Launch Power	0 dBm
Optical Wavelength	1552.524 nm
Transmission Distance	30 km
Fibre Dispersion	16 ps/nm/km
Fibre Kerr Coefficient	2.6e-20 m^2/W
Fibre Dispersion Slope	0.08 $ps/nm^2/km$
Fibre Loss	0.2 dB/km
PIN Detector Bandwidth	12.5 GHz
PIN Detector Quantum Efficiencies	0.8
PIN Detector Thermal Noise	18.8e-12 $A/\sqrt{Hz}$
PIN Detector Shot Noise (at ROP = 0 dBm)	17.8e-12 $A/\sqrt{Hz}$

ONUs' signals in the optical domain can completely eliminate the optical beating interference (OBI) effect [8], [48]. However, upstream OBI effects can be efficiently minimized in practical IMDD PON systems if suitably spaced wavelengths are employed for different ONUs [49].

After E/O conversion, the passively coupled signals from the different ONUs' are transmitted through the fibre transmission link where the system frequency response can be considered flat. In the OLT side, a variable optical attenuator (VOA) is employed to adjust the total ROP level prior to optical detection by the PIN photodetector. After the ADC, a single FFT operation, followed by four parallel processing-based data recovery processes of sideband identification, subcarrier equalization, sideband processing and 16QAM decoding are then employed for data recovery. The sideband processing operation is used to select a single subcarrier from either of the sidebands or to perform JSP.

Linear, low chirp IMs are always preferable for practical PON applications, and many optical IMs with low chirp and a linear operating region are widely available for practical application in OFDM-PONs [50]. In addition, practical PONs are typically highly linear systems where linear E/O and O/E optical intensity conversions can be achieved when the associated devices are operated in their linear regions, therefore we have assumed ideal optical IMs to clearly observe the targeted timing jitter effects by effectively minimizing other effects. However, it should be noted that although ideal optical intensity modulators are considered for the E/O conversion, the non-linear mapping between electrical and optical domains and the fibre non-linear effects are still present in our system. In addition, all system components in Fig. 4(a) can be considered to have bandwidths >6.25GHz i.e., the signal bandwidth to avoid bandwidth limitation effects. Also, in IMDD-based OFDM-PONs laser phase noise has a very minimal impact on performance when the transmission distance is relatively short [51]–[53]. Therefore, the effects of laser phase noise are not included.

It should be highlighted that the timing jitter-induced optical power penalty is measured by calculating the difference in the minimum required ROP for a given EVM, with and without timing jitter, therefore any system impairments should not have a significant impact on the observed optical power penalty.

To allow observations of jitter timing effects in isolation, an electrical back-to-back (EBTB) configuration is implemented by summing the outputs of all ONU-based DACs and feeding the combined signal directly to the ADC input at the OLT.

IV. Operating Principle of Joint Sideband Processing

As shown in Fig. 4(b), two conjugate symmetric sidebands carrying the same data in their lower sideband (LSB) subcarriers $TX_L(p)$ and upper sideband (USB) subcarriers $TX_U(p)$, where p is the subcarrier index of positive frequencies at the output of the FFT and $1 \le p \le (MN_{ifft}/2) - 1$ with N_{ifft} denoting the IFFT size, are employed in each SW spectral region and have the relationship:

$$TX_L\big(k + N_{ifft}(m-1)\big) = TX_U^*\big(mN_{ifft} - k\big) \tag{15}$$

where $[.]^*$ denotes the complex conjugate operation, m is the SW index (1,2,3…), and k is the corresponding subcarrier index before upsampling in the transmitter, thus for data-carrying subcarriers $1 \le k \le (N_{ifft}/2) - 1$.

At the OLT, without JSP, where a single subcarrier in one sideband is chosen, the resultant SNR is:

$$SNR_{k,m,w} = \frac{\sigma^2_{X_{k,m,w}}}{\sigma^2_{N_{k,m,w}}} = \frac{E\{|X_{k,m,w}|^2\}}{E\{|N_{k,m,w}|^2\}} \tag{16}$$

where $E\{.\}$ is the expectation operator, $|.|$ denotes the absolute value, w denotes the chosen sideband, i.e., LSB or USB. $\sigma^2_{X_{k,m,w}}$ and $\sigma^2_{N_{k,m,w}}$ are the signal and noise powers at the corresponding subcarrier in the chosen w sideband in the m^{th} SW respectively. Similarly, as the recovered signal is a complex value (phasor) $X_{k,m,w}$ and $N_{k,m,w}$ denote amplitude of the received signal and the noise at the corresponding subcarrier respectively.

With JSP, corresponding subcarrier pairs from upper and lower sidebands undergo a simple sideband coherent sum operation after conjugating the upper sideband subcarrier. Therefore, ignoring the noise, and assuming perfect channel estimation and equalization, then, as can be concluded from Eq. (15), the resultant signal component of each two corresponding subcarriers carrying the same data are related by:

$$X_{k,m,L} = X^*_{k,m,U} \tag{17}$$

where L and U denote lower and upper sidebands respectively.

For every corresponding subcarrier pair, the total signal after JSP is defined as:

$$JSP_{k,m} = (X_{k,m,L} + N_{k,m,L}) + (X_{k,m,U} + N_{k,m,U})^* \tag{18}$$

The total useful signal in Eq. (18) is:

$$X_{JSP_{k,m}} = X_{k,m,L} + X^*_{k,m,U} \tag{19}$$

whereas, the total noise is:

$$N_{JSP_{k,m}} = N_{k,m,L} + N^*_{k,m,U} \tag{20}$$

Using Eqs. (17) and (19), the resultant signal power after JSP is:

$$\begin{aligned}\sigma^2_{X_{JSP_{k,m}}} &= E\left\{\left|X_{JSP_{k,m}}\right|^2\right\} = E\left\{\left|X_{k,m,L} + X^*_{k,m,U}\right|^2\right\} \\ &= E\left\{\left|2.X_{k,m,w}\right|^2\right\} \\ &= 4\sigma^2_{X_{k,m,w}}\end{aligned} \tag{21}$$

Therefore, JSP increases the signal power by a factor of 4. From Eq. (20), the total noise power after JSP is:

$$\begin{aligned}\sigma^2_{N_{JSP_{k,m}}} &= E\left\{\left|N_{JSP_{k,m}}\right|^2\right\} = E\left\{\left|N_{k,m,L} + N^*_{k,m,U}\right|^2\right\} \\ &= \sigma^2_{N_{k,m,L}} + \sigma^2_{N^*_{k,m,U}} + 2\sigma_{N_{k,m,L}N^*_{k,m,U}}\end{aligned} \tag{22}$$

where the term $\sigma_{N_{k,m,L}N^*_{k,m,U}}$ is the covariance between different noise $N_{k,m,L}$ and $N^*_{k,m,U}$. The exact values of covariance and noise variances at every corresponding subcarrier pair highly depend on the degree of correlation of DAC/ADC timing jitter and the frequency of the subcarrier pair. For white DAC/ADC timing jitter, the noise at different subcarriers is always uncorrelated, thus the covariance term in Eq. (22) is always 0.

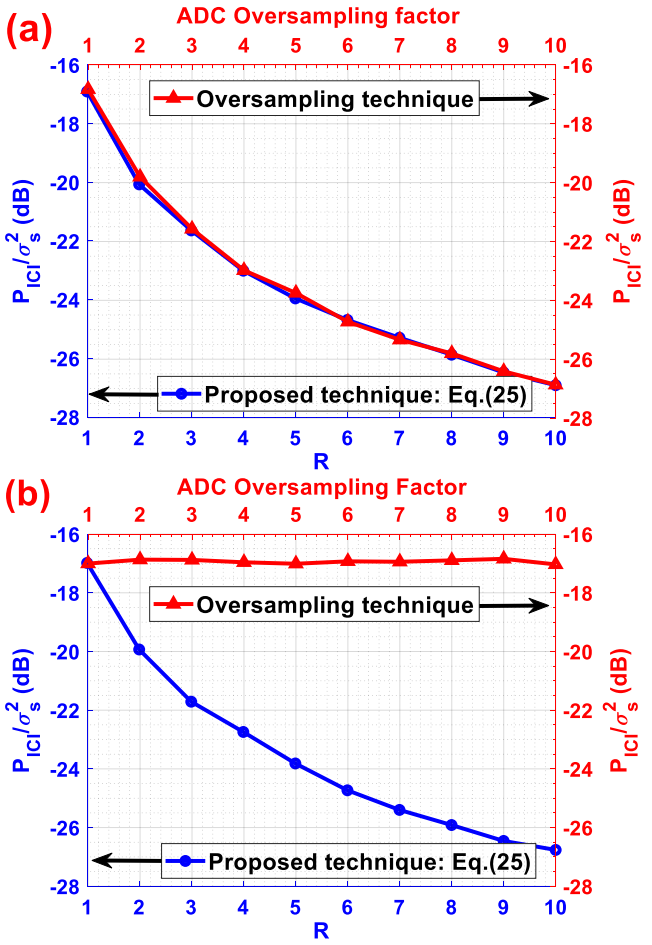

Fig. 5. Proposed technique vs. ADC oversampling: ICI power to signal power ratio (dB) for 16QAM 256 subcarrier OFDM system with (a) white ADC timing jitter of 8% UI_{rms}, (b) white DAC timing jitter of 8% UI_{rms}.

Moreover, the noise variance is fixed and frequency-independent, therefore, Eq. (22) becomes:

$$\sigma^2_{N_{JSP_{k,m}}} = 2\sigma^2_{N_{k,m,w}} \tag{23}$$

Therefore, after JSP, the total white DAC/ADC timing jitter-induced noise power increases by a factor of 2. Now, using the results from Eq. (21) and Eq. (23), the resultant SNR after JSP is:

$$SNR_{JSP_{k,m}} = \frac{\sigma^2_{X_{JSP_{k,m}}}}{\sigma^2_{N_{JSP_{k,m}}}} = \frac{4\sigma^2_{X_{k,m,w}}}{2\sigma^2_{N_{k,m,w}}} = 2\,SNR_{k,m,w} \tag{24}$$

Eq. (24) suggests that, for hybrid OFDM-DFMA PONs with white DAC/ADC timing jitter, the JSP technique improves the overall SNR and increases the signal power to ICI power ratio by a factor of 2 i.e. 3dB. It should be noted, however, that for coloured DAC/ADC timing jitter, the maximum achievable SNR increase may be less than 3dB, as $\sigma^2_{N_{k,m,L}}$ and $\sigma^2_{N_{k,m,U}}$ are dependent on frequency and the value of α.

To confirm our mathematical analysis, an ideal OFDM transmission link with a white DAC or ADC timing jitter is considered. In general, if the same data are transmitted on R different subcarriers, then by joint subcarrier coherent addition at the receiver, the timing jitter-induced ICI power increases by a factor of R, whereas the resultant subcarrier power increases by a factor of R^2, thus the signal power to ICI power ratio (σ_s^2/P_{ICI}) increases by a factor of R or $10Log_{10}(R)$ (dB) as follows [15]:

$$\frac{\sigma_s^2}{P_{ICI}} = \frac{3R}{\pi^2\left(\sigma_j/T_s\right)^2} \tag{25}$$

where σ_j denotes the RMS value of white DAC or ADC timing jitter. Compared with oversampling the signal at the receiver's ADC [16], [33], this technique demonstrates the same ability in reducing white ADC timing jitter-induced ICI as shown in Fig. 5(a). In addition, this technique outperforms the ADC oversampling technique, as the latter is seen to be completely ineffective against DAC timing jitter as evidenced in Fig. 5(b).

V. Numerical Results

A. Performance robustness against white timing jitters and joint sideband processing to mitigate timing jitter effect

Fig. 6 shows the performance robustness against individual white DAC or ADC timing jitter where the EBTB configuration, defined in Section III, is considered to effectively observe the effect of timing jitter in isolation, it is assumed that all four DACs always have the same level of timing jitter. The results confirm our theoretical analysis in Section II.A that both DAC and ADC timing jitters have virtually identical effects. Moreover, white timing jitter-induced ICI has a flat PSD; therefore, regardless of operating SW, all ONUs and their sidebands show identical BER performances where all ONUs have BER performance lower than the adopted FEC limit up to 8% UI_{rms}, whereas jointly processing both sidebands increase the robustness against white DAC or ADC timing jitters to 12.5% UI_{rms}, as shown in Fig. 6(c).

Fig. 7(a) shows the overall EVM (dB) of the received subcarriers versus the ROP and timing jitter for upstream hybrid OFDM-DFMA PON transmissions with white DAC timing jitter where JSP is adopted at the OLT and all four DACs always have the same level of timing jitter. As all ONUs demonstrate similar performance due to the white nature of the timing jitter, only the result of ONU 2 (2nd SW) is presented. Similarly, Fig. 7(b) shows the EVM performance for the same ONU in the considered PON with a white ADC timing jitter only.

The results in Figs. 7(a) and 7(b) confirm that the effects of DAC and ADC timing jitters are virtually identical even when considering an optical transmission channel. Moreover, the results demonstrate the considered PON's ability to still tolerate up to 12.5% UI_{rms} white DAC or ADC timing jitter. However, within this timing jitter range, the higher the level of the DAC/ADC timing jitter, the higher the required minimum ROP to achieve the desired BER of 1×10^{-3} or its equivalent 16QAM EVM of -17dB. Thus, for any fixed EVM level, there is a jitter-induced optical power penalty, when compared to the corresponding ROP of -11.6dBm for a jitter-free system. Moreover, as the timing jitter is white, the resultant optical power penalty is also frequency-independent.

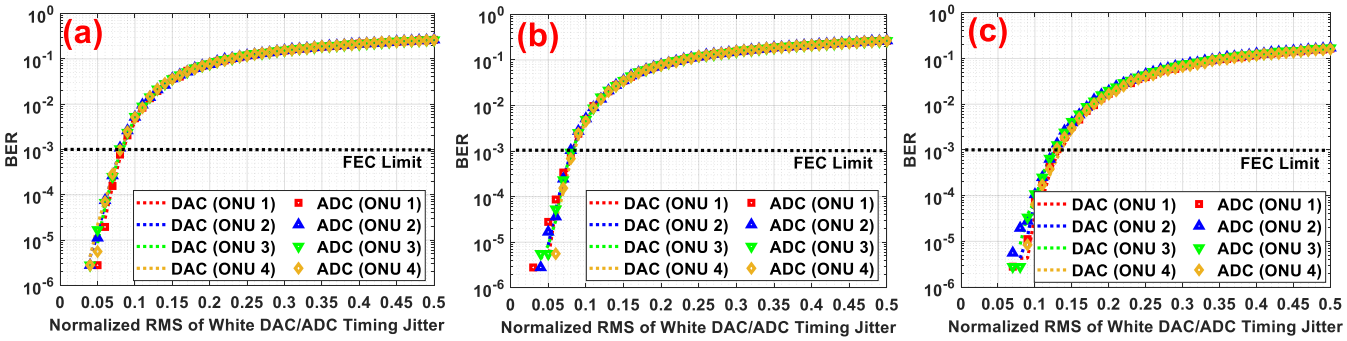

Fig. 6. BER vs. normalized RMS value of white DAC or ADC timing jitter for (a) LSB, (b) USB, (c) JSP.

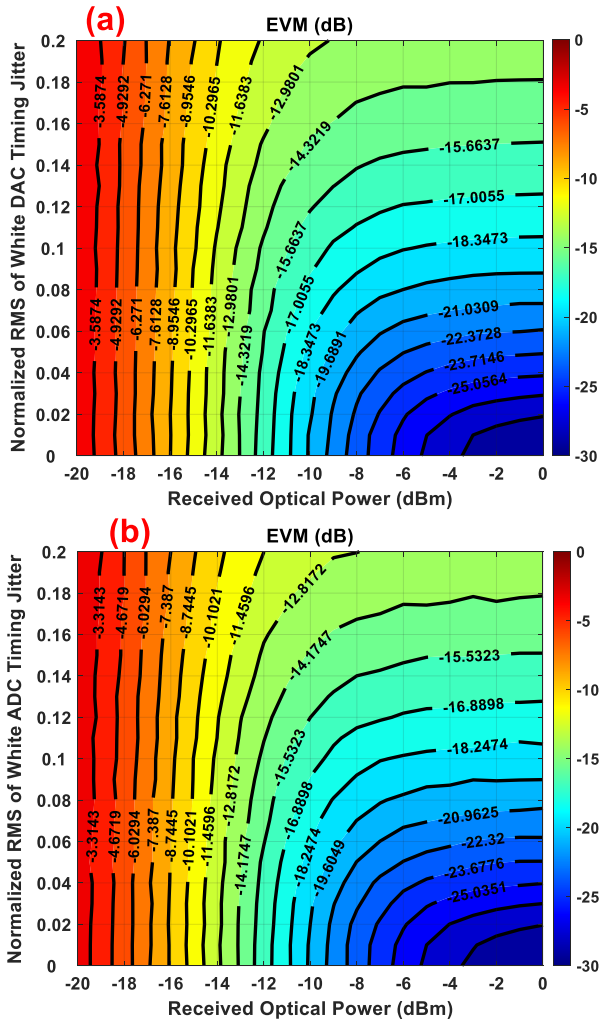

Fig. 7. EVM (dB) of ONU 2 in hybrid OFDM-DFMA PON with JSP and: (a) white DAC timing jitter, (b) white ADC timing jitter.

The ROP penalty at a fixed EVM of -17dB for ONU 2 is illustrated in Fig. 8 for both DAC and ADC white timing jitter, showing that DAC and ADC white timing jitters, both result in a similar ROP penalty. In addition, the results in Fig. 8 also illustrate the excellent effectiveness of JSP in significantly reducing the timing jitter-induced ROP penalty compared to the cases of LSB or USB processing only. The technique increases overall effective SNR thus achieving the same BER performance at a lower ROP, hence reducing the ROP penalty. For example, at a fixed white DAC or ADC (or combined) timing jitter level of 8% UI_{rms}, the technique results in a 4.8dB

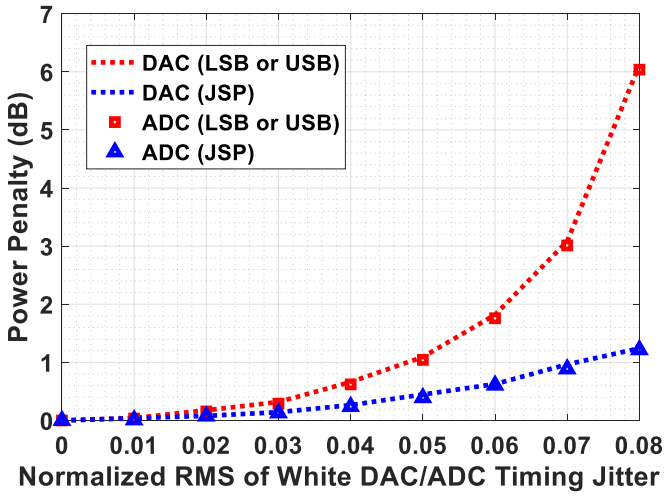

Fig. 8. Optical power penalty (dB) due to white DAC/ADC timing jitter at a fixed EVM of -17dB.

reduction in the ROP penalty as shown in Fig. 8. Furthermore, when only one sideband is processed at the receiver, white DAC/ADC timing jitter levels of approximately >5% UI_{rms} (in total) start to rapidly dominate over other system induced noise and distortions as evidenced by the rapid increase in the ROP penalty, whereas when JSP is adopted, the timing jitter starts to dominate only when the jitter level is beyond ~8% UI_{rms}.

B. Performance robustness against coloured timing jitters and joint sideband processing to mitigate timing jitter effect

Fig. 9 shows the numerical results for EBTB hybrid OFDM-DFMA PON with either highly correlated ($\alpha = 0.3$) DAC or ADC timing jitter, the results coincide with our theoretical analysis where both DAC and ADC timing jitters are expected to have virtually identical effects. Furthermore, unlike oversampling which has a limited efficiency when ADC timing jitter is coloured [16], JSP is seen to be an effective technique to enhance the jitter tolerance characteristics against both DAC and ADC timing jitters as shown in Fig. 9(c).

The result in Fig. 9 illustrates that coloured timing jitter is frequency-dependent as the total ICI is non-uniformly distributed over the entire bandwidth causing different ONUs to experience different ICI power as shown in Fig. 3(c). The non-uniform characteristics of the ICI distribution result from two facts; firstly, high-frequency subcarriers cause higher ICI than low-frequency subcarriers, secondly, subcarriers cause higher ICI to their adjacent subcarriers than distant subcarriers

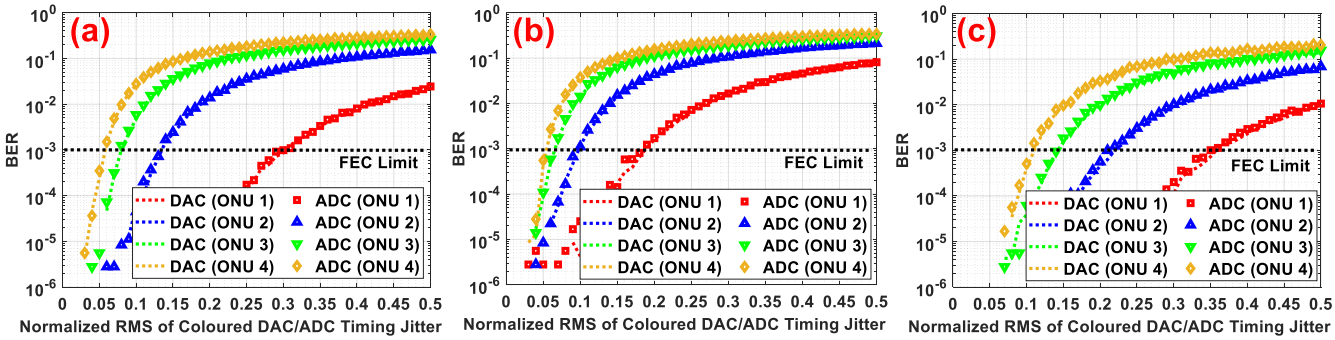

Fig. 9. BER vs. normalized RMS value of coloured DAC or ADC timing jitter (α = 0.3) for (a) LSB, (b) USB, (c) JSP.

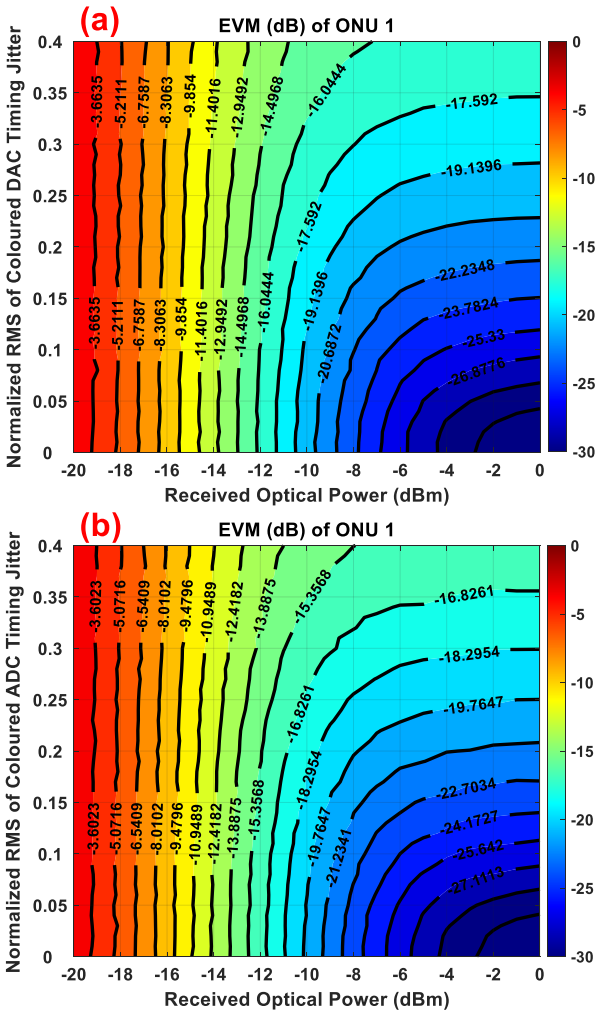

Fig. 10. EVM (dB) of ONU 1 in hybrid OFDM-DFMA PON with JSP and: (a) coloured (α = 0.3) DAC timing jitter, (b) coloured (α = 0.3) ADC timing jitter.

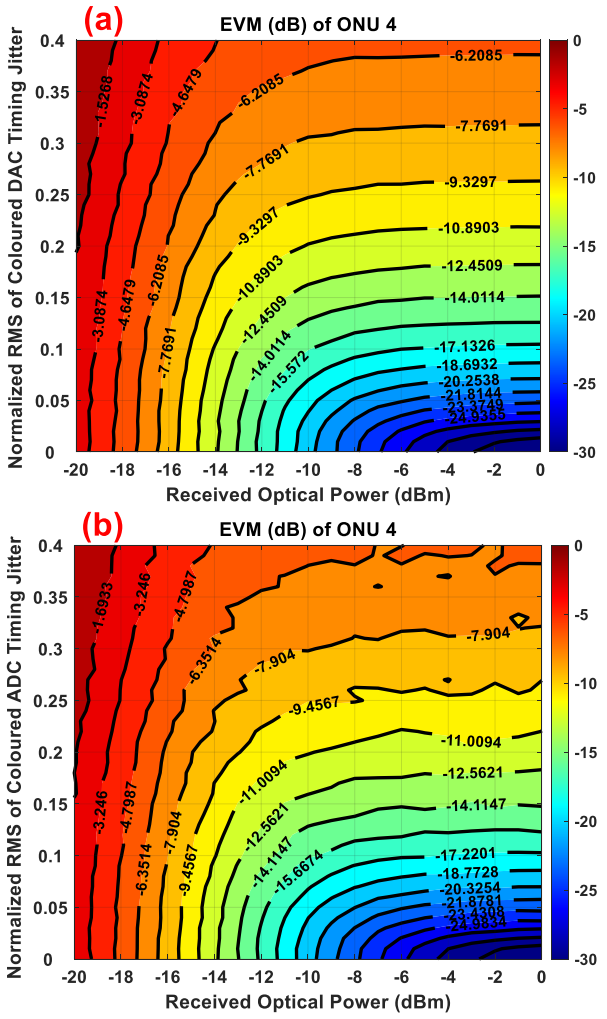

Fig. 11. EVM (dB) of ONU 4 in hybrid OFDM-DFMA PON with JSP and: (a) coloured (α = 0.3) DAC timing jitter, (b) coloured (α = 0.3) ADC timing jitter.

[15]. As a result, ONUs using low-frequency channels experience less ICI and so tolerate more timing jitter compared with the ONUs using high-frequency channels. Moreover, LSBs experience less ICI than USBs and thus show more robustness against coloured timing jitter.

Figs. 10 and 11 demonstrate the EVM (dB) of the received subcarriers versus ROP and timing jitter of ONU 1 (lowest SW) and ONU 4 (highest SW) respectively in the considered upstream transmissions of the hybrid OFDM-DFMA PON with a highly correlated coloured ($\alpha = 0.3$) DAC or ADC timing jitter where JSP is employed at the OLT, and all DACs always have the same level of the timing jitter. The numerical results confirm the frequency-dependent nature of coloured DAC/ADC timing jitter as ONU 1 shows better jitter robustness than ONU 4.

Figs. 12(a) – 12(c) demonstrate the corresponding ROP penalty for each ONU at a fixed EVM of -17dB for the cases of processing LSB, USB and using JSP, respectively. For the same level of coloured timing jitter, lower-frequency channel ONUs always show lower optical power penalties, thus, in contrast to white timing jitter, coloured timing jitter results in a frequency-dependent ROP penalty. In addition, for a fixed level of

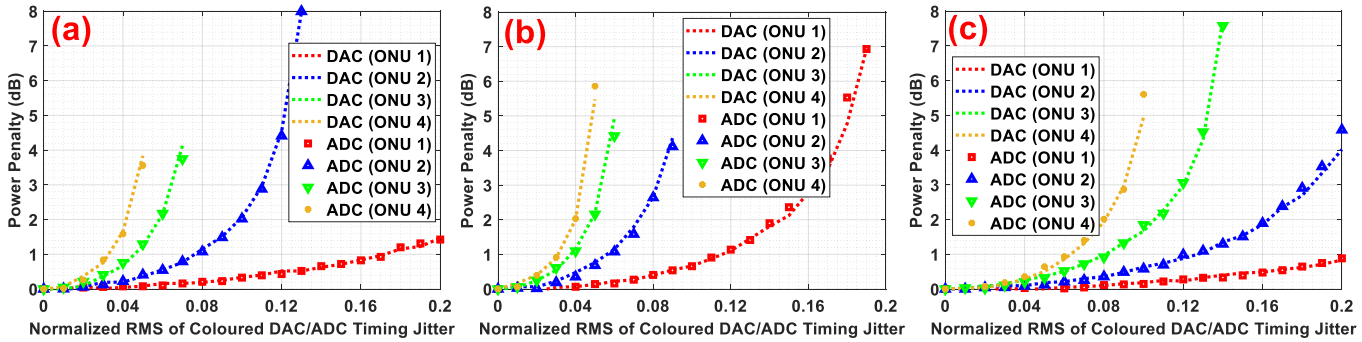

Fig. 12. Optical power penalty (dB) due to coloured (α = 0.3) DAC/ADC timing jitter at a fixed EVM of -17dB for (a) LSB, (b) USB, (c) JSP.

coloured timing jitter, LSB processing achieves a lower ROP penalty than USB processing, whereas JSP achieves the lowest ROP penalty, as shown in Fig. 12(c), with significant improvements compared to LSB/USB processing, especially at the lower frequency channel ONUs. It should also be highlighted that, in some cases, at reasonably low levels of timing jitter, some ONUs fail to achieve a BER below the FEC limit unless the JSP technique is applied.

For the hybrid OFDM-DFMA PON with JSP, for a fixed optical power penalty of ≤1.2dB, and assuming a jitter-free ADC at the OLT, each ONU can utilize a lower-quality DAC sampling clock with white timing jitter levels up to 8% UI_{rms} as illustrated in Fig. 8. However, when the jitter is highly correlated ($\alpha = 0.3$), the maximum allowed jitter for ONU 4 is then limited to ~6.5% UI_{rms} as can be concluded from Fig. 12(c), while a sampling clock with poor jitter levels up to 20% UI_{rms} can be deployed at ONU 1 as shown in Fig. 12(c). Overall, this indicates that, for a fixed ROP penalty, when compared with low-frequency channel ONUs with white-jitter sampling clocks, the same ONUs are able to achieve the same performance using lower quality (higher jitter level) coloured-jitter sampling clocks. In contrast, high-frequency channel ONUs require higher quality coloured-jitter sampling clocks to meet the same performance compared to using white-jittered sampling clocks. In addition, the result in Fig. 10 shows that for ONU 1 (lowest SW), other system induced noise and distortions dominate the ONU's performance until the jitter level is ≥~20% UI_{rms}. However, lower coloured jitter levels of ≥~6% UI_{rms} dominate over other system induced noise and distortions in affecting the performance of ONU 4 (highest SW) as evidenced by the more rapid increase in the ROP penalty in Fig. 12(c).

C. Performance robustness against combined DAC and ADC timing jitters and practical trade-off relationship between DAC and ADC sampling clocks

Fig. 13(a) shows the jitter tolerance characteristics of EBTB hybrid OFDM-DFMA PON with JSP to different mixtures of white DAC and white ADC timing jitters, since all ONUs show identical performance, only the result for ONU 2 is presented. The result confirms that for a fixed value of EVM, the variance of the total timing jitter is a summation of DAC and ADC timing jitter variances as follows:

$$(\sigma_{total}/T_s)^2 = (\sigma_{dac}/T_s)^2 + (\sigma_{adc}/T_s)^2 \qquad (26)$$

Eq. (26) thus reveals a practical trade-off relationship between the quality of the sampling clocks used to drive the

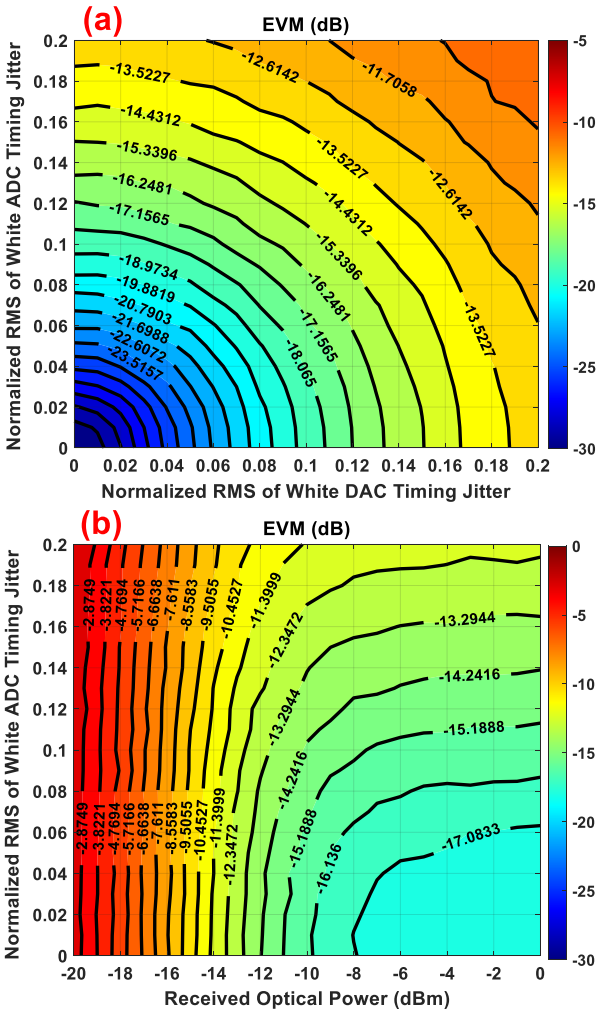

Fig. 13. Effect of combined white DAC and ADC timing jitters on the hybrid OFDM-DFMA PON with JSP: (a) EVM (dB) of ONU 2 in EBTB hybrid OFDM-DFMA PON with both white DAC and ADC timing jitters, (b) EVM (dB) of ONU 2 in upstream transmissions of hybrid OFDM-DFMA PON with both white DAC and ADC timing jitters (DAC jitter is 11% UI_{rms}).

DACs and ADCs. The hybrid OFDM-DFMA PON is efficiently able to tolerate up to 12.5% UI_{rms} of either individual or combined white DAC and ADC timing jitters, therefore, low-quality sampling clocks with up to $(\sigma_{dac}/T_s) = 11\%$ UI_{rms} jitter, for example, can be used at the ONU side as long as a higher-quality sampling clock with $(\sigma_{adc}/T_s) \leq 6\%$ UI_{rms} jitter is used to drive the OLT's ADC as can be confirmed in Fig. 13(a). Moreover, in a system with identical levels of white DAC and white ADC timing jitters, Fig. 13(a) and Eq. (26) suggest

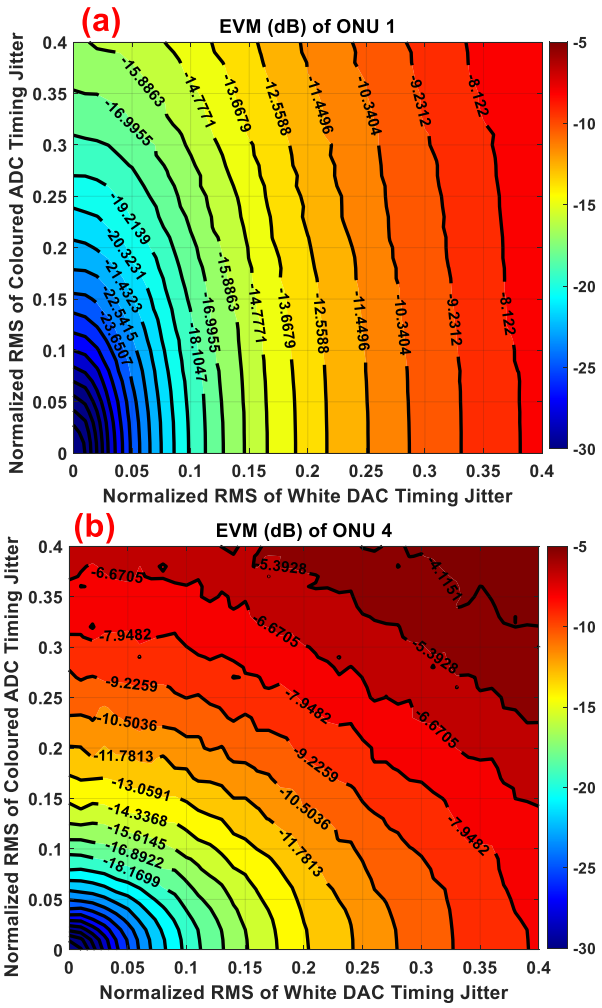

Fig. 14. Effect of combined white DAC and coloured (α = 0.3) ADC timing jitters on EBTB hybrid OFDM-DFMA PON with JSP: (a) EVM (dB) of ONU 1, (b) EVM (dB) of ONU 4.

that the maximum value of DAC and ADC timing jitters is 8.8% UI_{rms} each. If DAC timing jitter exceeds this value, an ADC with a lower timing jitter is then required to trade-off the effect of higher DAC timing jitter. Furthermore, based on Eq. (26) and Fig. 8, to limit the ROP penalty to ≤1.2dB the individual DAC/ADC timing jitters must be ≤5.6% UI_{rms} (≤8% total), which is well-aligned to practically realizable jitter levels.

Fig. 13(b) verifies that the DAC/ADC jitter trade-off effect is still valid for upstream transmissions when an optical system is considered and emphasises the possibility of trading-off the effect of low-quality DAC clock sources with a white timing jitter of 11% UI_{rms} by using a higher quality ADC clock source with white timing jitter ≤6% UI_{rms}, thus maintaining a total timing jitter of ≤12.5% UI_{rms}.

Fig. 14 investigates the effects of combinations of white DAC timing jitter and highly correlated ($\alpha = 0.3$) coloured ADC timing jitters on EBTB hybrid OFDM-DFMA PON with JSP. Fig. 14(a) shows that white DAC timing jitter is more dominant than the coloured ADC timing jitter in affecting the EVM (dB) of the low-frequency channel ONUs. In contrast, Fig. 14(b) emphasizes that high-frequency channel ONUs show more robustness against white timing jitters than coloured timing jitters as the EVM (dB) performance of ONU 4 is slightly dominated by coloured ADC timing jitter. The same result is obtained for a combination of coloured DAC timing jitter and white ADC timing jitter.

VI. Conclusions

In this paper, we introduce and verify improved DAC/ADC timing jitter models based on DAC/ADC timing jitter models in [25]–[27], [29], different combinations of white/coloured DAC and/or ADC timing jitters are then applied to investigate the timing jitter robustness characteristics of the recently proposed hybrid OFDM-DFMA PON. A DSP-based JSP technique is also demonstrated to mitigate white and coloured timing jitter effects and to significantly reduce the timing jitter-induced optical power penalties.

The work investigates the effect of DAC and ADC timing jitters on the upstream performance of a four-ONU hybrid OFDM-DFMA PON where JSP is employed at the receiver, we show that white DAC and ADC timing jitter levels up to 8% UI_{rms} (in total) affect the performance of all ONUs equally and result in a low ONU-independent optical power penalty of ≤1.2dB. However, coloured (α = 0.3) timing jitter results in a frequency-dependent ROP penalty, as for a fixed power penalty of ≤1.2dB, the maximum jitter value for ONU 1 (lowest SW) and ONU 4 (highest SW) is ≤20% and ≤6.5% UI_{rms} respectively. The work also highlights the possibility of trading-off the DAC and ADC jitter effects, hence lower quality DAC sampling clocks can be used at the cost-sensitive ONUs by using a higher quality ADC sampling clock at the OLT.

Overall, this work gives deep insights into the DAC/ADC timing jitter tolerance characteristics of the recently proposed hybrid OFDM-DFMA PON and the associated timing jitter induced optical power penalties, thus aiding the specification and selection of the required timing jitter inducing components.

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