Review of PMU Algorithms Suitable for Real-Time Operation With Digital Sampled Value Data

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***Abstract*—Phasor Measurement Unit (PMU) instruments are continuously evolving to reflect the needs of electrical grids for enhanced and more accurate monitoring of the AC signal parameters, and to contribute towards optimization of real-time control tasks. In turn, enhanced monitoring can contribute to a more stable and reliable power supply. PMU standards are also being updated to reflect the latest performance requirements PMUs and new technological developments. As described in standard IEC/IEEE 60255-118-1, a PMU may receive streams of timestamped digital samples using the IEC 61850-9-2 Sample Values (SV) protocol, instead of traditional analog signals. This means that the signal conditioning and sampling parts can be located at a different location from the computational unit. This approach requires remote processing, so additional time delay is introduced that affects the reporting latency of the PMU. Therefore, not all the PMU algorithms presented in the literature will be valid candidates to operate with SV data and at the same time comply with reporting latency requirements. To address this issue, the paper presents a literature review of PMU algorithms, to identify algorithms which are suitable for real-time operation with the SV data protocol. Among many proposed PMU algorithms, only a few of them can estimate synchrophasor, frequency, and rate of change of frequency (ROCOF) on a sample per sample basis. Recommendations on selecting PMU algorithms for hardware implementation that complies with SV data has been also provided.**

***Index Terms*—Algorithms, frequency, phasor measurement unit, real-time operation, ROCOF, sample value data, synchrophasor.**

I. Introduction

Phasor Measurement Units (PMUs) are widely deployed in electricity grids of transmission systems [1] because of their capability to provide accurate, reliable, fast, and comparable measurements of synchrophasors, frequency, and rate of change of frequency (ROCOF). These advanced features have enabled PMUs to be utilised in measurement-based control and protection schemes [2]; to support state estimation [1], [3]; and to monitor network disturbances such as harmonics, voltage stability indicators, inter-area oscillations, and power system dynamic phenomena of the transmission system through wide-area measurement systems (WAMS) [1], [3].

PMU instruments also are installed in distribution electric grids for voltage, current, and power flows [4] monitoring; to estimate the line parameters [5], and for protection such as loss of main and load shedding [6]. They are expected to have a larger utilisation to enhance the monitoring and real-time control capability of these grids, considering the increasing connections of renewable energy generation.

Due to the growing demand for these instruments, many conventional PMUs (that access the AC signals of the grid through instrument transformers) are developed and are available on the market. Fig. 1 presents a typical block diagram of a conventional PMU. All its building blocks (except the time source), such as signal conditioning, analog to digital converter (ADC), and the processing unit are located within the PMU instrument. Manufacturers are free to choose and implement any of the proposed parameter estimation algorithms presented in the literature, as long as they meet the requirements of the standard IEC/IEEE 60255-118-1.

However, another approach for PMU design involves using input signals in the form of streams of timestamped digital samples. Typically, this would be implemented using the IEC 61850-9-2 [7] Sample Values (SV) protocol along with the requirements for sample rates and other factors in IEC 61869-9, and the new technique for compressing SV data in real-time [8]. This approach is expected to operate on a continuous data stream of a relatively small number of data samples per SV message, rather than buffering and transferring large batches of samples (such as a window containing a full cycle of data). It provides greater flexibility and allows PMUs to be deployed efficiently where an existing IEC 61850 substation process bus already provides voltage and current data in IEC 61850-9-2 format. A typical block diagram of a PMU interfacing power system signals through electronic instrument transformer (EIT), and provided with SV data is presented in Fig. 2. In this case, the EIT block is located in the field, whereas the computational and communications unit may be located in a remote location. This approach normally requires appropriate algorithms which are suitable for real-time operation with SV data protocol, to comply with the reporting latencies declared in [9].

This paper presents a literature review of PMU algorithms used to estimate synchrophasors, frequency, and ROCOF with a special focus on identifying those algorithms that can estimate these parameters after each acquired sample, using IEC 61850-9-2 SV data as the input. Due to extra delay introduced by the merging unit (MU) within an EIT resulting from time-tagging the samples and communicating the SV data to the computational unit, algorithms not designed to operate

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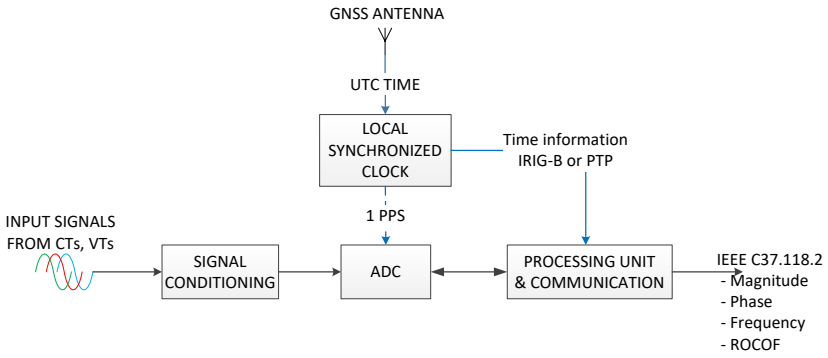

Fig. 1. Block diagram of a conventional PMU

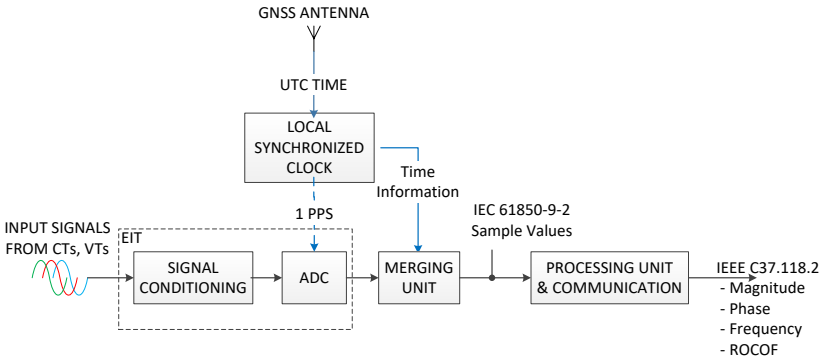

Fig. 2. Block diagram of a PMU with SV data as input, according to IEC/IEEE 60255-118-1:2018, Annex E

on sample by sample basic may exceed the reporting latency recommended by the IEC/IEEE 60255-118-1 standard [9].

PMU reporting latency and the factors that influence synchrophasor errors are also considered, focusing on the differences arising when splitting the PMU front-end from the computational part. In such a context, this paper aims to provide recommendations on selecting appropriate PMU algorithms for hardware implementation to comply with the SV data protocol.

The paper is structured as follows: Section II presents a review of the existing synchrophasor estimation methods. In Section III the PMU reporting latency issues are discussed, and possible error sources of synchrophasors are considered in Section IV. Conclusions are summarised in Section V.

II. Synchrophasor Estimation Methods

In this section, the synchrophasor estimation methods are reviewed. Proposed methods that are capable to estimate synchrophasor, frequency, and ROCOF parameters on a sample by sample basis are identified and discussed.

A. Discrete Fourier Transform

Discrete Fourier Transform (DFT) based algorithms are optimised to work in stationary conditions and when the measurement interval matches an integer number of cycles. An ideal situation like this reflects a zero error of the phasor magnitude and phase [10].

A more realistic situation reflecting the off-nominal frequency conditions and possibly other disturbing phenomena is encountered in real electric grids, where the spectral leakage and scalloping loss effect compromise the accuracy of the estimated phasor. To make the estimated parameters more accurate, one approach is to increase the length of the measurement window. However, this will have a direct impact on the calculation time, and it is well known that DFT based algorithms are computationally intensive. This is an obvious limitation for the DFT based algorithms to update the synchrophasor estimation after each acquired sample.

Another approach to improve the algorithm performance under limited off-nominal frequency conditions, and therefore improving the accuracy of the estimated parameters, is to exploit the different frequency responses of the window functions [11], [12], or to use the Interpolated DFT approach (IpDFT) [13] to cope with a large frequency deviation from nominal. As the algorithm has to interpolate the highest bins of the frequency spectrum (to eliminate the scalloping loss), an extra step in the calculation process is added, and this fact

makes the IpDFT algorithm more computationally intensive than the basic DFT approach. The computational drawback can be addressed by using an FPGA for real-time processing, but this requires additional cost.

Other proposed DFT based algorithms that aim to improve the accuracy of the synchrophasor estimated parameters, such as the Enhanced Interpolated DFT algorithm (E-IpDFT) [14], which considers the effect of the spectral interference coming from the negative image of the fundamental tone, or the Iterative-interpolated DFT (i-IpDFT) [15], that considers the effect of the spectral interference generated by harmonics and interharmonics, both use post-processing techniques needed to compensate for these effects. The algorithm presented in [15] calculates the phasor over a 3-cycle measurement window and slides the window every cycle to produce a reporting rate of 50 reports per second (for a 50 Hz power system). It is clear that this algorithm is not intended to update the synchrophasor parameters after each sample is acquired. A DFT based algorithm developed for a relatively high reporting rate of 5 kHz is proposed in [16] as an Enhanced interpolated-modulated sliding DFT (E-IpMSDFT). The algorithm is implemented by using the sliding DFT technique over a 3-cycle measurement interval and shows reduced reporting latency. High reporting rates up to 5 kHz are achieved by updating only a small number of DFT bins around the fundamental component. This algorithm is intended to update the synchrophasor estimation in real-time after each sample is acquired.

B. Time Domain Signal Analysis

Reference [17] presents a synchrophasor estimation technique based on time-domain signal analysis. The signal parameters such as the amplitude, phase, and the DC offset (the frequency is considered known or estimated by other methods) are determined by using “three parameters sine-fit algorithm” [18]. The parameters are estimated by solving the system of linear equations and using the least-squares approach. A more computationally intensive method for the determination of the signal parameters including the unknown frequency is the “four parameters sine-fit algorithm” calculated through an iterative process.

Synchrophasor estimation accuracy by considering three and four parameters sine-fit algorithms, evaluated on one-cycle and half-cycle measurement intervals, together with their respective computational time was considered in [17]. It was shown that the four parameters sine-fit algorithm is 4.4 times more computationally intensive than the three parameters sine-fit algorithm. It is clear that processing times makes these algorithms not appropriate for sample-based synchrophasor estimation.

Another synchrophasor, frequency, and ROCOF estimation algorithm based on time-domain signal analysis has been presented in reference [19]. Parameters are estimated by using the space vector transformation combined with digital filters. The algorithm complexity is low, however, its ability to operate on a sample per sample basis needs verification.

C. Demodulation and Filtering

A method of estimating synchrophasors based on the demodulation and filtering technique is proposed in standard [9], and is named as the reference algorithm. In [20], the standardised algorithm for P class PMUs is further improved by adjusting in real-time the oscillator frequency and by using adaptive cascaded finite impulse response (FIR) filters to completely attenuate the harmonic interference. This was achieved by using the measured frequency of the signal.

In [21], the improvement proposed in [20] for the P class PMUs is extended to M class PMUs, and both referred to as P and M class alternative algorithms. The performance of the P and M class alternative PMU algorithms has been analysed in [21]. Reduced ROCOF errors by a factor of 40 for P class and 100 for M class have been achieved in off-nominal frequency conditions, with respect to the reference algorithms proposed in [9]. These algorithms are tested at a sampling rate of 10 kHz and were able to produce continuous reports at these conditions. Therefore, these alternative algorithms are appropriate for sampled based synchrophasor estimation.

D. Hilbert Transform

In [22], a synchrophasor estimation algorithm based on the Hilbert transform has been proposed for P-class PMUs. The algorithm exploits the low computational burden of the Hilbert transform to achieve the fast response required by P-class PMUs. The requirements of the static and dynamic conditions set in IEEE C37.118.1 standard are fulfilled by the algorithm. However, the reporting rate of the estimated parameters was limited to 60 reports per second, and no indication of parameter estimation based on sample value was found. However, by considering that the Hilbert transform is a natural extractor of instantaneous magnitude, instantaneous phase, frequency, and ROCOF, it is assumed that with an alternative implementation this algorithm may be adapted to work on a sample-by-sample basis. Care is required to ensure full compliance with the IEEE synchrophasor standard requirements.

E. Dynamic Phasor Model Evaluated by Taylor Polynomial Series

Reference [23] presents an algorithm for the definition of the dynamic phasor using the second-order Taylor polynomial approximation. Experimentally, the amplitude and phase estimation together with their respective derivatives, are performed every 2 signal cycles. This algorithm has been modified in [24] and optimised for real-time operation. Calculations are performed over a 3-cycle and 5-cycle measurement windows for P class and M class PMUs, so not on a sample per sample basis. However, the low computation times estimated on a real-time PC-based platform indicate their potential to work on a sample-by-sample basis.

Reference [25] presents a synchrophasor estimation algorithm for M-class PMUs based on the dynamic phasor model approximated by the second-order Taylor expansion within

the considered measurement window. The synchrophasor algorithm was implemented and tested at a reporting rate of 50 Hz.

F. Phase Locked Loop

In [26] a new method for phasor estimation parameters (magnitude and phase, together with frequency and ROCOF) for single-phase and three-phase signals was proposed based on a modified phase-locked loop technique. The modification consists of a better elimination of the double frequency ripple in the loop by an improved low pass filter design.

As explained by the authors, the estimated output signal parameters (magnitude, phase, and frequency) are internally adjusted to minimize the difference (error) with their respective (parameters) of the input signal. This mechanism requires at least 20 ms for the parameters to settle or achieve a steady state. This is a limitation of the algorithm, which is not able to estimate the signal parameters on a sample per sample basis.

G. Prony's Method

In [27] a method for estimating dynamic phasor parameters based on Prony's method has been proposed, aiming to improve the synchrophasor estimation accuracy during power system oscillations. In terms of implementation, the shortest possible window required to calculate the synchrophasor parameters is one cycle.

The synchrophasor estimation methods discussed in this section are presented in Table 1. Based on the way these algorithms are implemented, only some methods can directly estimate the required parameters on a sample-by-sample basis, rather than operating on a group of samples. Note that this is based on a qualitative assessment of the algorithm operation. A full implementation and quantification of the real-time algorithm performance is required to fully assess the presented methods, to determine if they comply with the standard requirements, but this is beyond the scope of the paper.

TABLE I
SYNCHROPHASOR ESTIMATION METHODS

Synchrophasor estimation methods based on	***Appropriate for operation with SV data***
Discrete Fourier Transform (DFT)	no
Interpolated DFT (IpDFT)	no
Enhanced Interpolated DFT (E-IpDFT)	no
Iterative-interpolated DFT (i-IpDFT)	no
Enhanced interpolated-modulated sliding DFT (E-IpMSDFT)	yes
Three parameter sine-fit algorithm	no
Four parameter sine-fit algorithm	no
Demodulation and Filtering (reference algorithm)	yes
Demodulation and Filtering (alternative algorithm)	yes
Hilbert transform	no
Taylor Polynomial Series	no
Taylor-Fourier (modified)	yes
Phase Locked Loop	no
Prony's Method	no

III. CONSIDERATIONS ON PMU REPORTING LATENCY

Latency sources that influence the total reporting latency of both conventional PMUs and PMUs with SV data inputs are discussed in this section.

When the sampling stage of a PMU is located inside a device together with the computational unit and the communication interface, as in normal conventionally developed PMUs, the time difference between the evaluation of the synchrophasor parameters and the time the measurement is made available at the output communications port of the PMU [9] is known as the "reporting latency". It consists of known latency sources.

Discussion on the impact of digital PMUs on reporting latency is given in IEC/IEEE 60255-118-1 standard [9], Annex E. Factors that influence the PMU reporting latency are: the measurement window length; delays introduced by the analog and digital filters; ADC conversion delay which decreases proportionally with the increasing sampling rate and can be significantly shorter in SAR architecture compared to Sigma-Delta ADCs; algorithm processing time; and communications interface delays. The total delay is evaluated by the proposed and very accurate method in [28] for two different algorithm implementations for P and M class PMUs, and has been applied to characterise the reporting latency of a complete platform for validating wide-area monitoring, protection, and control systems in real-time based on PMU data [29].

As the sampling stage is separated from the computational unit [9], an additional delay is introduced by the merging unit (MU) in the preparation of SV data (processing delay time) [30], and another delay is introduced by the addition of the communications link needed to transmit the SV to the processing unit. In total, for one particular implementation, these additional latencies have been measured and estimated to contribute to the total reporting latency by approximately 800 µs [28]. However, the total reporting latency of a PMU cannot be considered as a fixed quantity because some of the contributing latency sources are not constant. If we denote the constant latency sources by the letter T and the variable latency sources by t, the total reporting latency of a PMU (with SV data input) can be expressed as:

$$PMU_{\text{Latency}} = EIT_{\text{Latency}} + \boldsymbol{CU}_{\text{Latency}} \tag{1}$$

$$PMU_{\text{Latency}} = T_{\text{analog filter}} + T_{\text{ADC}} + t_{\text{MU}} + t_{\text{network}} + \boldsymbol{T}_{\text{window}} + \boldsymbol{T}_{\text{algorithm}} + \boldsymbol{t}_{\text{communication}} \tag{2}$$

where:

- $\boldsymbol{CU}_{\text{Latency}}$ is the computational unit latency
- $T_{\text{analog filter}}$ is the contribution from the group delay of the analog antialiasing filter
- T_{ADC} – is time delay required by the SAR algorithm to convert an analog sample into a digital representation
- t_{MU} processing delay time of the MU in preparation of SV data
- t_{network} amount of time needed by a packet to transfer from MU to computational unit

- $\boldsymbol{T}_{\text{window}}$ delay introduced by a fixed measurement window length
- $\boldsymbol{T}_{\text{algorithm}}$ algorithm processing time
- $\boldsymbol{t}_{\text{communication}}$ network propagation delay for a PMU report to transfer from the output port of the PMU to the application or a phasor data concentrator.

As can be seen, t_{MU}, t_{network} and $t_{\text{communication}}$ are variable latency sources can affect the PMU reporting latency. For the latency source t_{MU}, one should also consider the fact that various system clocks of each physical unit within a MU (e.g. for the analog sampling and the local processor) are subject to drift over time unless they are all synchronized by, for example, a 1 PPS signal. This factor can have a negative impact on increasing the overall PMU reporting latency over time. Furthermore, if the algorithm or computational part of the PMU is not executed on a real-time platform (e.g. to reduce costs), then it is unlikely to meet the reporting latency requirements [29].

In reference [31], the latency introduced by the communications network at a power substation level has been evaluated by simulations, together with jitter (variation in the latency of packets). A total of 250 streamed packets have been considered for the test. Each packet contains 6 data samples provided by a MU. The estimated packet latencies introduced by the network were within 0.6 ms to 0.7 ms time range for most of the evaluated packets, with few packets showing a longer arrival time of 1.5 ms to 2 ms. This appears to include both the SV encoding delay and the network delay (which would be similar to the 800 μs value in [28].

IV. Consideration of Synchrophasor Measurement Errors

Errors that affect the synchrophasor estimated parameters from the PMU point of view, where the ratio and phase displacement errors introduced by voltage and current transformers are excluded [9], are caused mainly by:

1) signal conditioning circuitry (scaling errors, non-ideal magnitude and phase response of the analogue filter)
2) ADC quantization error
3) time synchronization errors
4) algorithm limitations.

In conventional PMUs with analogue input signals, voltage and current transformers serve as external sensors for the PMUs, whereas elements 1 to 4 form the PMU instrument itself. In cases where a PMU is fed with SV data rather than analogue signals, items 1) and 2) are combined inside an EIT. The most common elements [32], that can form items 1) and 2) are presented in the block diagram of Fig. 3. Because items 1) and 2) will be the same either for a PMU fed with analog signals or a PMU provided with digital samples, the error contributions have no reasons to differ, and hence splitting the signal conditioning and the ADC part from the computation part has no reason to have negative effects [9].

In [33], a performance comparison between a PMU with an analog input signal and a PMU with SV input has been performed, and it was shown that better performance was achieved by the digital PMU (lower TVE, FE, RFE errors) in some steady-state tests. However, the observed differences were due to the test setup variations, where for the case of a PMU test setup with an analogue interface, an additional amplifier is employed in the scheme so, influencing the results.

V. Conclusions

This paper has presented a review of PMU algorithms compliant to IEC/IEEE 60255-118-1 standard requirements, used to estimate synchrophasors, frequency, and ROCOF, focusing on those algorithms that are appropriate to estimate these parameters on a sample per sample basis. Algorithms based on steady-state and dynamic phasor models, exploiting both the time domain and the frequency domain techniques, have been considered.

It has been shown that, in general, DFT based algorithms are computationally intensive and not appropriate for fast reporting rates that match the sampling frequency. However, a DFT based algorithm, named Enhanced interpolated-modulated sliding DFT (E-IpMSDFT), has shown relatively low processing requirements making it appropriate for reporting rates up to 5 kHz. Also, algorithms based on demodulation and filtering techniques have been shown to be capable of high reporting rates and therefore are appropriate for sampled-based synchrophasor parameter estimation. Synchrophasor parameter algorithms estimated by other methods based on either the steady-state phasor model or the dynamic phasor model were shown to be more computationally intensive and not appropriate to estimate the parameters on a sample-by-sample basis.

PMU reporting latency and the factors that influence the total reporting time of both types of PMUs (whether with analog or digital inputs) have been considered. All possible latency sources are listed and are categorised as either constant or variable in nature. It is considered that the constant latency sources, although larger in nature, cannot affect the variability of the total reporting time of a PMU, whereas variable latency sources, while much smaller than the constant sources, can have a negative impact by increasing the overall PMU reporting latency over time.

The errors introduced by the analogue front-end are considered to have a large impact on the PMU accuracy. However, by considering that the same elements can potentially be employed either at a PMU provided with analog signals or at a PMU provided with digital signals, it was concluded that splitting the signal conditioning and the ADC part from the computation part has no reason to have a negative effect on the PMU accuracy.

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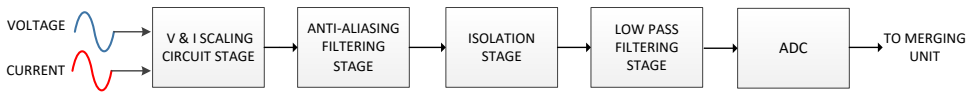

Fig. 3. Typical block diagram representing the signal conditioning circuitry blocks and the ADC block for a PMU

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