Technical Review of Dual Inverter Topologies for More Electric Aircraft Applications

Zhen Huang, Tao Yang, *Senior Member, IEEE*, Paolo Giangrande, *Senior Member, IEEE*, Michael Galea, *Senior Member, IEEE*, and Patrick Wheeler, *Fellow, IEEE*

Abstract—Electric drives are an essential part of more electric aircraft (MEA) applications with ever-growing demands for high power density, high performance, and high fault-tolerant capability. High-speed motor drives can fulfil those needs, but their speeds are subject to the relatively low DC-link voltage adopted by MEA. The power inverters are thus expected to efficiently and effectively manage that limited voltage. A recently popular topology is represented by the dual inverters. They are featured by inherited fault tolerance, a high DC-link voltage utilization and an excellent output power profile. This paper aims to present a comprehensive review of different structures based on the dual inverter. To meet the stringent requirements of MEA applications, three performance aspects, including the voltage utilization, the inverter output quality and the fault-tolerant capability, are selected. Based on the chosen performance metrics, the key features of adopting dual inverter topologies against other converter selections are explicitly demonstrated. Finally, a practical guideline for choosing suitable dual inverters for different MEA applications is provided.

Index Terms—Dual inverter, floating bridge, multilevel inverters, space vector modulation, voltage regulation

I. BACKGROUND

In civilian aircraft, the gas turbines provide the power primarily for the propulsion thrust and the secondary power required for all the onboard systems [1]–[3]. To enhance the secondary power system controllability and overall performance, more electric aircraft (MEA) initiative has been developed, progressively replacing the pneumatic, hydraulic and mechanical sources with their electric counterparts [4], [5].

Electrical drives enable the adoption of MEA concept facilitating cost-effective and efficient renewable energy generation and conversion [2], [6]. For a representative MEA onboard system shown in Fig. 1 [7], electrical drives can be found in the energy generation system, including starter-generators (SG)/generators [1], [8]–[10], and energy consumption loads covering wing ice protection system (WIPS), flight control

Z. Huang, T. Yao, P. W. Wheeler, M. Galea and P. Giangrande are with the Power Electronics Machines and Control Group, Department of Electrical and Electronics Engineering, University of Nottingham, Nottingham, NG7 2RD, UK. (e-mails: zhen.huang@nottingham.ac.uk, tao.yang@nottingham.ac.uk, pat.wheeler@nottingham.ac.uk, michael.galea@nottingham.ac.uk, paolo.giangrande@nottingham.ac.uk).

M. Galea is also with the University of Nottingham Ningbo China, Ningbo 315100, China.
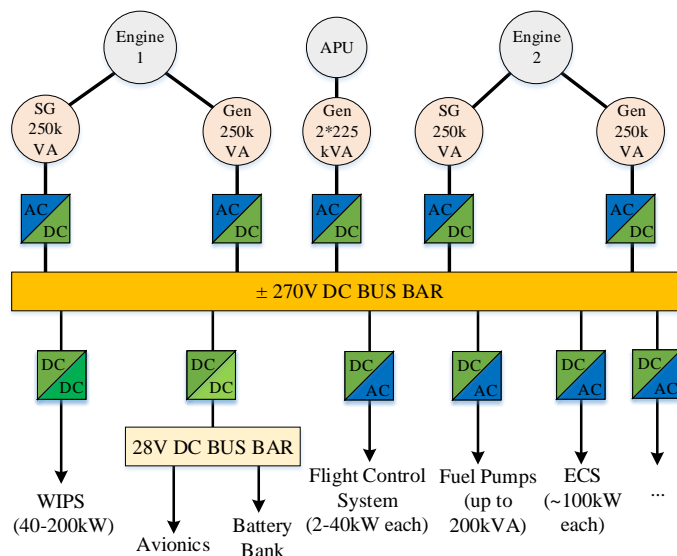

Fig. 1: Onboard electrical system architecture in MEA. (APU: auxiliary power unit)

system, fuel pumps, environmental control system (ECS), etc. [3], [10]. The estimated power levels of those electric systems for a medium/large MEA are indicated in Fig. 1. Compared to using non-electric systems, the ones with electric power can achieve gains in the overall efficiency, weight/cost saving while maintaining reliability [10]–[13].

However, today there is an ever-growing need for higher performance and more efficient systems. Especially from a transport industry perspective, today the industry is facing immense challenges related to emissions and efficiency. Higher power densities, coupled with excellent efficiency are fast becoming the standard requirement for applications in the MEA. A common approach to meet the requirement of high power density is by looking at higher speed drives [14], [15].

For a motor drive, its wide-speed operation is subject to the supply voltage from the power converters [16]. Entering the field-weakening region is not favourable as it may result in potentially higher losses [17]. As the motor's back electromotive force (EMF) grows linearly with speed, a sufficiently high output voltage from inverters is essential [14], [18]. However, the reality is that for MEA applications, the most common DC-link feeding the power inverters value is 270V or 540V as seen in Fig. 1. A DC-DC boost converter is typically adopted, but extra power electronics simply lower the system reliability [19]–[21]. Another concept was to adopt a variable

voltage DC bus where WIPS has been taken as the case study in [22]. However, regardless of different DC-link voltages, greater utilization of the power inverters is highly expected [23]. A larger speed without field weakening could allow the machine to minimize its weight and volume considerably, which can be beneficial for MEA applications [24], [25].

On the other side, it is very important to note that for aerospace applications, simply having better power densities is not enough. Regardless of how pushed the design is in terms of power density, the electrical drive still needs to respect the fault-tolerant capabilities that are set for such safety-critical applications [6] [26]. Driven by the motivations of enhancing DC-link voltage utilization, the power quality as well as the fault-tolerant capability, new inverter topologies as well as adapting advanced modulation schemes are being intensively investigated [27].

Multilevel inverters are being recognized as one of the most promising solutions for MEA applications. Their reduced dv/dt, better power quality and higher efficiency are perceived to give a significant advantage over traditional two-level inverters [28]. Cascaded H-bridge inverters (CHI), flying-capacitor inverters (FCI) and diode-clamped inverters (DCI) are the three most recognized multilevel inverters [13].

A recent very popular configuration is represented by the dual inverter topology. It employs two standard two-/multilevel converters connecting to either side of an open-end winding (OeW) machine [29], [30]. This configuration offers excellent redundancy [8] and fault-tolerant ability [21] using a reduced device count [31] in comparison to other multilevel inverters configurations. For a given amount of switching devices, the number of isolated supplies, capacitors with voltage regulation needs, and diodes needed by a dual inverter are less than the number required by a CHI, FCI, and DCI, respectively [24], [31]. From the above, it can be concluded that the dual inverter has great control flexibility from its abundant switching states within a relatively simple structure. Therefore, this topology now is very attractive for aerospace applications.

Compared to other multilevel inverters, dual inverters are featured by three design freedom that may further enhance the converter performance. The first one is for the power supplies arrangements. There are three choices, namely the dual inverter with two isolated voltage sources, with a common DC-link and with a floating capacitor (FC) [32].

Secondly, two modulation schemes, namely the coupled method and the decoupled modulation, can be alternatively applied for dual inverters. The previous one modulates the reference vector for a whole dual inverter, while the latter resolvers the reference vector into two vectors, each representing one inverter [33]. Substantially, the coupled modulation perceives the dual inverter as a whole converter for modulation, whereas the decouple one considers it as two separate systems.

The last design freedom of a dual inverter is the assignment of the voltage ratio between two inverters. It is reported the dual inverters can enhance their performance by identifying appropriate voltage ratios. The improvement consists of improving the converter output quality by increasing the number of output voltage levels [25], [31], [33]–[38] and boosting the
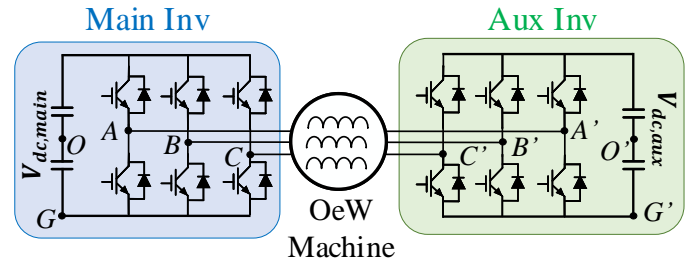

Fig. 2: Schematic of the motor drive with a dual inverter.

DC-link voltage utilization [16], [25], [39]–[42].

However, similar to a CHI, an FCI, or a DCI, the capacitors' voltages of the dual inverters also have to be properly controlled. Otherwise, the voltage steps that are clamped by capacitor voltages would be altered, and then undesirable harmonic distortion will be induced in the inverter output, deteriorating its quality. To fully exploit the potentials of dual inverters with exclusive design freedom, the capacitor voltage regulation is the main challenge [25].

In this paper, the operation principle of dual inverters will be briefly introduced in Section II. This is followed by reviewing three exclusive design freedom featured by dual inverters, the configurations in Section III, modulation schemes in Section IV, and voltage ratio assignments in Section V that may optimize their performance. With those design potentials, Section VI summarizes the addressed voltage regulation schemes in literature. The performance evaluation of dual inverter topologies is comprehensively assessed in Section VII. Based on that, Section VIII provides recommendations of suitable dual inverter configurations for MEA applications, and the conclusions are drawn in Section IX.

II. DUAL INVERTER OPERATION PRINCIPLE

Considering the motor drive in Fig. 2, one can observe the dual inverter configuration, where the left inverter in blue colour is called the Main-Inv and the right-hand side one in green colour is denoted as the Aux-Inv. The OeW machine is connected between the AC outputs of the Main-Inv (main inverter) and Aux-Inv (auxiliary inverter), as shown in Fig. 2. Fig. 2 shows the supplied voltages of the Main-Inv and Aux-Inv are assigned to $V_{dc,main}$ and $V_{dc,aux}$, respectively.

Considering the loops AA'O'O, BB'O'O, CC'O'O in Fig. 2, the three-phase voltages $V_{AA'}$, $V_{BB'}$ and $V_{CC'}$ can be expressed by (1) according to Kirchhoffs Voltage Law (KVL),

$$\begin{cases} V_{AA'} = V_{AO} - V_{A'O'} + V_{OO'} \\ V_{BB'} = V_{BO} - V_{B'O'} + V_{OO'} \\ V_{CC'} = V_{CO} - V_{C'O'} + V_{OO'} \end{cases} \quad (1)$$

where V_{AO}, V_{BO}, V_{CO} and $V_{A'O'}$, $V_{B'O'}$, $V_{C'O'}$ are the three-phase pole voltages for the Main-Inv and Aux-Inv, respectively.

Assuming the three-phase loads are symmetrical, then as stated in (2), the sum of load phase voltages should be zero. Thus, $V_{OO'}$ can be derived by adding three equations in (1), as shown in (3).
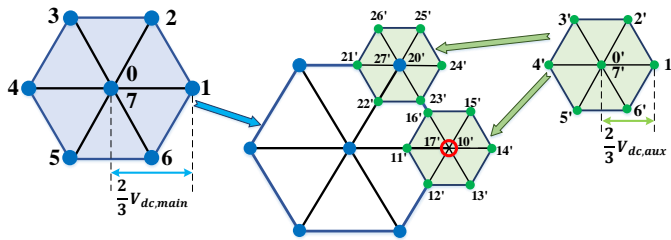
Fig. 3: Space vector diagram by a dual inverter.

$$V_{AA'} + V_{BB'} + V_{CC'} = 0 \quad (2)$$

$$V_{OO'} = \frac{V_{A'O'} + V_{B'O'} + V_{C'O'}}{3} - \frac{V_{AO} + V_{BO} + V_{CO}}{3} \quad (3)$$

Substituting (3) into (1), then the phase voltage expression can be updated to (4),

$$\begin{cases} V_{AA'} = (\frac{2}{3}V_{AO} - \frac{1}{3}V_{BO} - \frac{1}{3}V_{CO}) - (\frac{2}{3}V_{A'O'} - \frac{1}{3}V_{B'O'} - \frac{1}{3}V_{C'O'}) \\ V_{BB'} = (\frac{2}{3}V_{BO} - \frac{1}{3}V_{CO} - \frac{1}{3}V_{AO}) - (\frac{2}{3}V_{B'O'} - \frac{1}{3}V_{C'O'} - \frac{1}{3}V_{A'O'}) \\ V_{CC'} = (\frac{2}{3}V_{CO} - \frac{1}{3}V_{AO} - \frac{1}{3}V_{BO}) - (\frac{2}{3}V_{C'O'} - \frac{1}{3}V_{A'O'} - \frac{1}{3}V_{B'O'}) \end{cases} \quad (4)$$

From (4), it can be found that the phase voltage applied from a dual inverter on the OeW machine in Fig. 2 is the phase voltage difference produced by the two inverters (i.e. the Main-Inv and the Aux-Inv). Based on that, the resultant space vector diagram of a dual inverter can be showed in Fig. 3, where the set of space vector hexagons due to the Aux-Inv 'orbiting' the space vector hexagon of the Main-Inv.

Generally, the voltage applied to the machine is represented by the switching states of both inverters. For instance, the switching state 15' indicates 1 (100) for the Main-Inv and 5' (001) for the Aux-Inv. The three numbers within the bracket, such as (100) and (001), indicate the states of the top switches for each leg in Fig. 2. In Fig. 3, each dot represents one switching vector, and it can be expressed by several switching states. These are known as redundant states. For example, the vector denoted in red circle in Fig. 3 can be represented by either 10' or 17'. For a standard two-level three-phase converter, there are eight switching states to form seven vectors in the plane. Since a dual inverter employs two two-level inverters, it possesses $8^2 = 64$ switching states.

In Fig. 3, the area of space vector diagrams for the Main-Inv and Aux-Inv is defined by their supplied voltages $V_{dc,main}$ and $V_{dc,aux}$, respectively. From Fig. 3, it can be observed that the space vector diagram of a dual inverter is dependent on the voltage ratio between $V_{dc,main}$ and $V_{dc,aux}$. A comprehensive study on this ratio will be reviewed in Section V.

III. DUAL INVERTER DESIGN FREEDOM ①: CONFIGURATIONS

A. Type I

As shown in Fig. 4, there are three different arrangements for power sources in a dual inverter. They can be either two
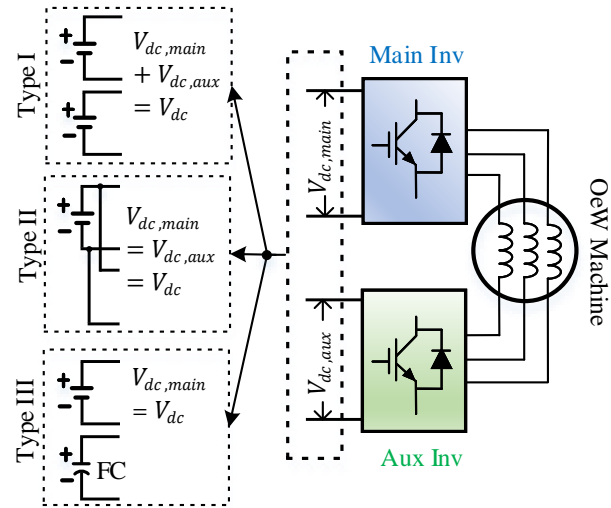

Fig. 4: Three configurations of dual inverter topology.

TABLE I: Three dual inverter configurations and their applications

	Dual Inverter Configurations		
	Type I	Type II	Type III
DC-link Voltage Utilization k	≤1 [43], [44]	1-2 [45]	>1 [24]
Number of Output Levels	≥3 [31]	2 [46]	≥3 [31]
MEA Applications		Starter-generator (100kW) [8], [9], [47], [48]	Starter-generator (100kW) [8], [9], and EMA (40kW) [24]

isolated DC-links (type I), a common DC-link (type II), or a DC-link with a FC (type III). Table I preliminarily compares the performance of three dual inverter types seen in Fig. 4 and their applications in MEA. It can be seen from Fig. 4 only the dual inverter type I needs a bulky transformer to achieve isolation [31], [49]. This would increase the volume and weight of system significantly, which are not desired in MEA applications.

In this work, the indicator k shown in Table I is employed to compare the voltage utilizations of the dual inverters. It is calculated by dividing the maximum output voltages from a dual inverter $V_{ref,max}$ over the voltage from its DC-link voltage $V_{dc}/\sqrt{3}$ within the linear modulation region, as expressed in (5) [25].

$$k = \sqrt{3} * V_{ref,max}/V_{dc} \quad (5)$$

The dual inverter type I uses two isolated DC-links where their voltages' sum is equivalent to V_{dc}, as shown in Fig. 4. Table I indicates that voltage utilization of the dual inverter type I could be less than one [43], [44]. This is due to the overcharge concerns, which will be elaborated in Section VI-A.

It can be seen from Table I that the output levels of dual inverter type I/III can be more than three [31], which is obviously an appealing feature. A higher number of output levels

are conceivable for asymmetric supplies ($V_{dc,main} \neq V_{dc,aux}$), and this study will be presented in Section V.

B. Type II

The dual inverter type II has the highest degree of fault tolerance and the double voltage utilization, as shown in Table I. References [47], [48] have taken those advantages by using the dual inverter type II for starter-generators. However, this configuration is suffered from the zero-sequence current (ZSC) circulating [50]. For a dual inverter, the ZSC is determined by the differential common-mode voltage (D-CMV) [45], [51], [52]. The expression of D-CMV is given in (6) [53].

$$D-CMV = \frac{V_{AO} + V_{BO} + V_{CO}}{3} - \frac{V_{A'O'} + V_{B'O'} + V_{C'O'}}{3} \tag{6}$$

Equations (3) and (6) indicate that D-CMV is identical to the voltage difference between the medium points of the voltage supplies on the two inverters, i.e. OO' in Fig. 2. To suppress this D-CMV, the dual inverter type II may degrade from multilevel to two-level operation [46], as shown in Table I. At the same time, the DC-link voltage utilization may also be affected [45]. A common methodology to virtually remove all ZSC is to implement the dual inverter type I or III [49].

C. Type III

Table I shows that the dual inverter type III has the advantages of the other two configurations in terms of multilevel output capability due to avoiding ZSC circulation and no need for any isolation circuitry since one bridge is floating. In particular, an attractive feature brought by type III is that its voltage utilization can be more than one thanks to the existence of the FC [24]. Researchers in [24] have applied the dual inverter with a FC for driving electromechanical actuators (EMAs) in the secondary flight control surface.

IV. DUAL INVERTER DESIGN FREEDOM ②: MODULATION SCHEMES

A summary of the previously addressed modulation techniques for three types of dual inverters is reported in Table II. As stated in the introduction, the coupled modulation technique's primary benefit is that the multilevel output voltage can be guaranteed at all time. On the other hand, the resultant voltage on load for the decoupled method is unpredictable due to the decoupled modulation of the two inverters [91]. In this case, undesirable voltage steps in the inverter output can occur. The decoupled modulation scheme does however offer the main advantages of flexibility, fault tolerance and greater adaptability in terms of the various control objective functions for the drive. In the following, these two schemes are introduced using related previous works and publications.

A. Coupled Modulation

For coupled modulation, a dual inverter can be treated as a single multilevel converter. To reduce the switching actions, an alternate-sub-hexagonal centre (SHC) modulation scheme
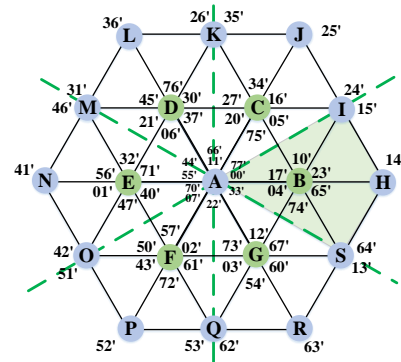

Fig. 5: Principle of the alternate-SHC modulation scheme for a symmetric dual inverter.

can be used to switch one inverter while clamping the other inverter to one state during a switching period [54], [55], [58]. Fig. 5 shows the mechanism of the alternate-SHC modulation scheme. In Fig. 5, the whole space vector diagram is divided into six sections, where the SHCs are marked by the circles B, C, D, E, F and G in green. As for each SHC, one inverter is switching whereas the other one is clamped, then the role is alternated for the next SHC. For instance, point B is the SHC of the quadrangle ASHI painted in light green in Fig. 5. Within this quadrangle, the applied switching states would be either 10', 11', 12', 13', 14', 15', 16', 17' (clamping the Main-Inv at 1 and switching the Aux-Inv) or 04', 14', 24', 34', 44', 54', 64', 74' (clamping the Aux-Inv at 4' and switching the Main-Inv). In particular, [55] conducts a thermal losses analysis of using the alternate-SHC modulation scheme, and [58] proves this technique is featured by equalizing losses between two inverters.

A power-sharing scheme between two inverters is established along with the relationship between the unbalanced sharing and the modulation index (M.I.) in [56]. In addition, researchers in [60]–[68] and [24], [31], [33]–[36], [38], [49], [84], [85] cope with the capacitor voltage regulation for the dual inverter type I and type III, respectively.

B. Decoupled Modulation

As mentioned before, the output voltage of a dual inverter is the difference between the voltages generated by two inverters. When the decoupled modulation is applied, the voltage reference V_{ref} is synthesized into $V_{ref,main}$ and $V_{ref,aux}$ feeding into two inverters separately. This process can be expressed by (7),

$$V_{ref}e^{j\theta} = V_{ref,main}e^{j\theta_{main}} - V_{ref,aux}e^{j\theta_{aux}} \tag{7}$$

where θ_{main} and θ_{aux} are the angles of reference vectors $V_{ref,main}$ and $V_{ref,aux}$, respectively.

The schematic of reference vector synthesis is shown in Fig. 6. From (7) and Fig. 6, it can be observed that there are four user-defined variables. This allows for great control flexibility, which can then be taken advantage of. For example, [70] adjust the θ_{main} and θ_{aux}, improving the output voltage profile for dual inverters. To reduce the output current ripple,

TABLE II: Summary of modulation techniques for dual inverters in literature

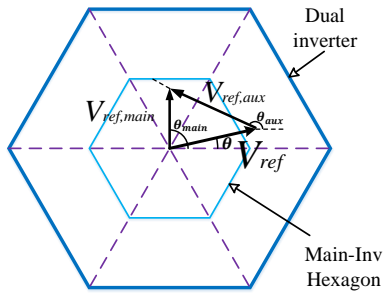| Dual Inverter Design Freedom		②Modulation strategy	
		Coupled (modulate as one whole inverter)	Decoupled (modulate as two separate inverters)
①Configuration	Type I	[54]–[68]	[44], [69]–[75]
	Type II	[45], [46], [76]–[81]	[82], [83]
	Type III	[24], [31], [33]–[35], [35], [36], [38], [49], [84], [85]	[33], [40], [42], [64], [86]–[90]

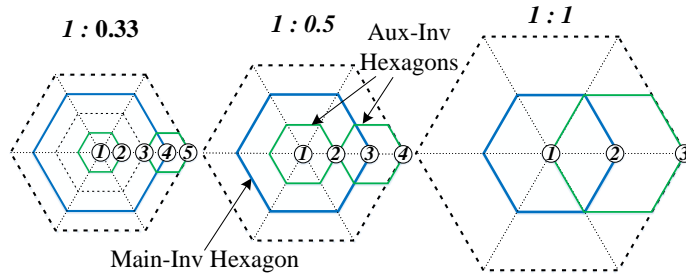Fig. 6: Principle of decoupled modulation for a dual inverter.

Fig. 7: Space vector diagram of the dual inverters with different voltage ratios.

[69] conducts an analytical study and then proposes a strategy based on the decoupled modulation.

Researchers in [44], [71]–[73] and [24], [31], [33]–[36], [38], [49], [85] deals with the capacitor voltage regulation for the dual inverter type I and type III, respectively.

Even though the decoupled modulation can bring excellent control flexibility, the undesirable voltage steps would inevitably be seen in the inverter output [24]. In consequence, the converter output performance is affected significantly.

V. DUAL INVERTER DESIGN FREEDOM ③: VOLTAGE RATIO ASSIGNMENTS

As revealed in Fig. 3, the output voltage from a dual inverter is the output voltage difference between the Main-Inv and the Aux-Inv. Therefore, the voltage ratio essentially alter the resulting space vectors' distribution of a dual inverter. In addition to that, the area of space vector diagram and the inverter output levels are both affected by the ratio choice. Fig. 7 shows the space vector diagram of the dual inverters with different voltage ratios. It can be observed that three, four, and five levels are achievable with ratios 1:1, 1:0.5, and 1:1, respectively.

It is worth of mentioning that the last design freedom is only applicable to the dual inverter type I and type III, while type

II has a common DC-link such that the ratio is fixed to one. In this section, the ratios considerations for the dual inverter type I and type III will be reviewed in order.

A. Type I

Initially, the dual inverter was mostly comprised of identical supply voltage for two inverters. This is known as the symmetrical voltage ratio (1:1). H.Stemmler demonstrated that dual two-level inverters with symmetric supplies had the equivalent performance of a three-level inverter in 1993 [92]. The advantages of asymmetric voltage supplies were first investigated in 1999 when a voltage ratio of 1:0.5 was primarily introduced to achieve a four-level operation in [60], [61]. However, this asymmetric ratio will raise the overcharge issue, which will be reviewed in Section VI-A.

B. Type III

One attractive freedom of the dual inverter type III is that the FC voltage can be flexibly controlled during the motor operation. If suitable voltage ratios are chosen, an increased number of output voltage levels [31], [33], [34], [38] or a boosted DC-link voltage utilization of dual inverters can be achieved [16], [40]–[42]. It has been revealed in [25] that the voltage ratio would define the 1) distribution of switching states; 2) area of space vector diagram; and 3) number of output levels. After selecting the ratios, the main issue is to properly regulate the FC voltage at that ratio.

In terms of utilizing the voltage ratios to increase the voltage levels, the ratio 1:0.5 is applied to provide three-level operation in [31], [38]. The researchers in [31], [38], [93] all adopted the coupled modulation. Despite guaranteeing the multilevel output waveform of dual inverters, their maximum output voltages are within the DC-link voltage due to limited regulation capabilities [31], [33], [36]–[38]. As a result, the FC voltages, which can be substantially beneficial for motor drives, are highly under-utilized [24].

Alternatively, the voltages ratios can be assigned to have a relatively large FC voltage, and thus the DC-link voltage utilization can be potentially high. However, the FC voltage could not be assigned extremely high as it has to below the capability of applied regulation methods. For example, a ratio of 1:2.5 is chosen to boost the voltage utilization in [40]. However, the six-step modulation technique is adopted, which naturally lowers the inverter output quality. Reference [42] has studied using the ratio 1:2, but its approach is perceived as a very complex control scheme with several non-linear regulators tuning [90]. Besides, the utilization improvement of 35% and 100% can be achieved using a voltage ratio of
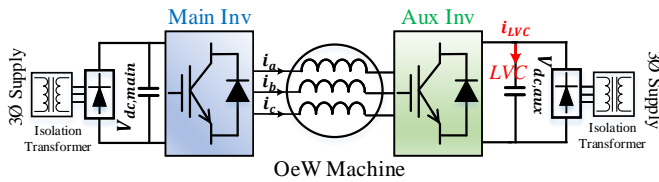
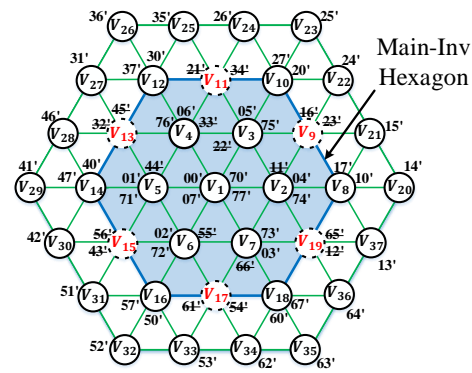Fig. 8: Dual inverter type I (with isolated DC supplies).

Fig. 9: The dual inverter type I with ratio 1:0.5 using the passive regulation method [62].

Fig. 10: Current flow schematics of using the overcharging states [44].

1:1 [94] and [41], respectively. A varied voltage ratio was investigated in [16], which can enhance the DC-link voltage utilization by up to 60%. All the FC regulation methods in [16], [40]–[42], [90], [94] apply the decoupled modulation strategy that separately allocates the reference voltages for two inverters, but this strategy causes undesired voltage steps at the inverter output resulting in distortions [24], [95]. In this case, the DC-link voltage utilization of dual inverters can be increased, but their output quality is significantly compromised.

The above shows that even selecting a suitable voltage ratio can potentially enhance the dual inverter performance, but this is significantly affected by the applied FC regulation method. The researchers firstly applied an advanced regulation method [24] on the dual inverter type III with 1:0.5, boosting the DC-link voltage utilization by 50% along with four-level output [24]. Based on that, four more ratio candidates (1:2, 1:1, 1:0.5, and 1:0.33) were considered in [25], while a strategy of integrating ratios 1:0.5 and 1:1 was addressed. Using this ratios strategy will allow the dual inverter to double voltage utilization while maintaining good power quality [25].

VI. VOLTAGE REGULATION FOR DUAL INVERTERS

As summarized in the previous sections, voltage regulation is crucial to the converter performance improvement. For instance, in the dual inverter with a FC, the main challenge is to regulate the FC's voltage to the desired value. Similarly, in the dual inverter with isolated asymmetric supplies, the capacitor at the lower-voltage side is at risk of being overcharged by the higher-voltage side. And for the one with a common DC-link, its challenge is to control the D-CMV properly. In this section, voltage regulation issues in dual inverters are explained, and the previously reported solutions are reviewed.

A. Type I

While an asymmetric dual inverter configuration enables the possibility to improve output quality (four-level operation), it however entails the risk of overcharging the low-voltage capacitor (LVC) on the Aux-Inv shown in Fig. 8. Such a situation will eliminate the voltage ratio and may cause safety issues of LVC on account of the charge accumulation [65], [73]. The overcharging issue at 1:0.5 ratio is reported initially in [62], and it is studied thoroughly in [44]. During the modulation process, the phase current flows into the LVC, and the overcharged capacitor will result in that the voltage ratio of 1:0.5 is not maintained. Under this condition, the phase voltage is distorted, rendering extra harmonic distortion into motors [44], [62]. Reference [73] proposed implementing
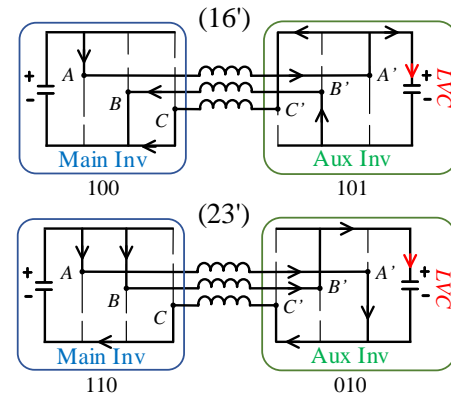
a fully controllable supply with bidirectional power flow as the DC-link on the Aux-Inv. This however comes at the cost of more complexity of hardware and of course an increased component count.

To remove the need for a bidirectional supply and also to solve the overcharging problem, there are generally two approaches found in literature, namely 1) through adjusting the modulation schemes [44], [62], [66], [68], [71], [73], and 2) by employing additional hardware [59], [63], [67], [72]. The first option is based on a selection of the switching states from analyzing the current flow associated with switching states to identify the states that may cause overcharging. Those states are then avoided for modulation process. This type of voltage regulation methods that assume the load current direction are denoted as the passive regulation method [24]. An illustration is given in Fig. 9. The states, such as 16' and 23' in Sector I marked with strikethroughs in Fig. 9, are regarded as the overcharging states and are therefore not considered. The current flows of using that two states are shown in Fig. 10, where the potential of overcharging the LVC can be observed [44]. The main drawback of such methods is that by reducing the number of vectors that can be used for modulation, such as V_9 in the red colour in Fig. 9. Under this case, the nearest three vectors (NTV) principle sometimes could not follow, which in turn lowers the output voltage quality.

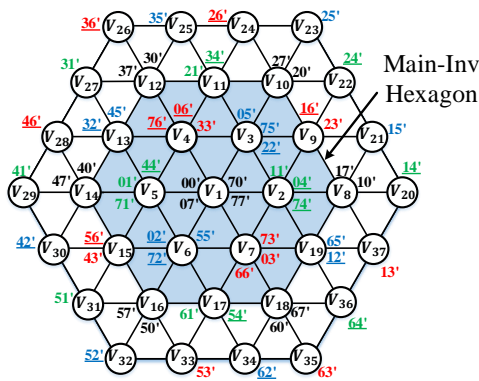A strategy to switch the Main-Inv while clamping the

Fig. 11: The dual inverter type I with ratio 1:0.5 using the active regulation method [43].
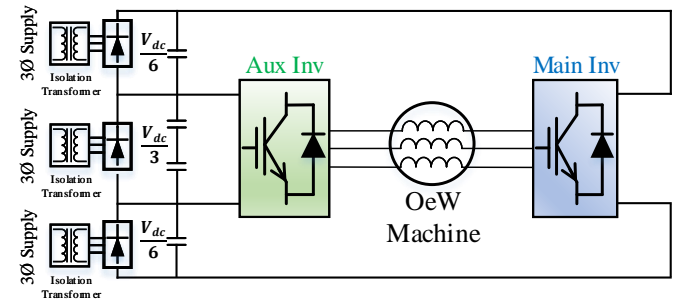

Fig. 12: Dual inverter with a nested rectifier-inverter reported in [63].

Fig. 13: Motor phases connection for state 11' in the dual inverter with a nested rectifier-inverter.

Aux-Inv is presented in [66]. However, this method entails a larger modulation area, which implies that the harmonic distortion in the inverter output may be worsened. To improve power quality, a coupled discontinuous carrier-based pulse width modulation (PWM) technique is established in [68]. However, the modulating signal in this method intersects with all the carrier signals throughout the whole M.I. region. It implies that the switching actions could be considerably high, thus increasing the switching losses. In particular, the major problem of passive regulation is that their analysis in [44], [62], [68], [71] takes the assumption of current direction, which is actually affected by the load power factor (PF) [24].

An enhanced version of passive regulation, namely the active regulation, was addressed in [43]. This scheme will actively choose the suitable states according to the regulation need with the help of the measured phase current values. The active regulation method starts with characterizing all the switching states by their resulting currents into the LVC. An example of the dual inverter with ratio 1:0.5 using active regulation method is shown in Fig. 11. Defining the current flowing into the Aux-Inv as the positive direction, the switching states causing the negative current flow is underlined in Fig. 11. In addition to that, the line colour highlights the flow path of different phase currents. The green colour represents the flow path of current i_a, the red colour indicates the path of current i_b, and blue shows the path of current i_c. With an appropriate switching states' selection, a suitable current flow can be determined to avoid overcharging the LVC. For instance, assuming the vector V_9 is chosen for modulation, there are two switching states 23' and 16' in Fig. 11 that can be used for modulation and one of those two will not cause the overcharging depending on the current direction. Compared to the passive regulation approach shown in Fig. 9, the vector V_9 associated states 16' and 23' are regarded as the overcharging states that are forbidden to use for modulation purposes. In contrast, when active regulation scheme is adopted, vector V_9 can be applied, such that the NTV algorithm can be followed and the inverter output quality would not be affected.

Reference [73] proposes a modulation technique, unequal reference sharing algorithm based on carrier-based PWM that naturally regulates the LVC voltage. The mean value sign of the current i_{LVC}, i.e. the current acting on the LVC showed in
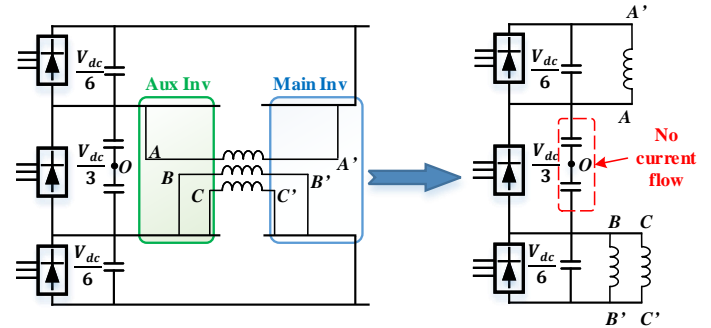
Fig. 8, is analyzed through a numerical iteration. It is observed that i_{LVC} would have a negative mean value when the method in [73] implements. However, this method attributes to the decoupled modulation so undesirable voltage steps can be witnessed, resulting in a deteriorated output voltage waveform.

For the hardware solution, a structure of nested rectifier-inverter is proposed in [63] (see Fig. 12), and it is further revised in [59]. In this structure, the Aux-Inv with lower-voltage DC-link is nested within higher-voltage DC-link that feeds the Main-Inv. Subsequently, based on this structure, more advanced modulation schemes are addressed to achieve a boosted voltage utilization for the $6n$-pole OeW motor in [72], or suppress the ZSC in an average sense in [67]. The feasibility of the structure in Fig. 12 is explained through Fig. 13. In Fig. 13, a particular instance of using the state 11' is shown. Fig. 13 shows the connection of motor phases to the LVC for the state 11'. It is evident that the configuration of a nested rectifier-inverter successfully achieves the prevention of overcharging problem. However, the main drawback of this solution is that it needs one more isolated DC supply when compares to the scheme of Fig. 12 with Fig. 8. Naturally, employing a more complicated structure with an increased component count would considerably increase the volume and the cost of the motor drive system [66], [68].

B. Type II

Fig. 14 shows that the dual inverter type II share one common DC-link. The primary concern of this topology is the ZSC current, i_{ZSC} in Fig. 14, may circulate the system. It would increase the value of the phase current without any
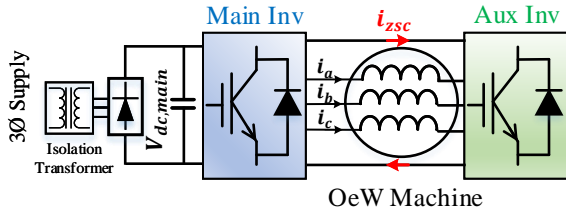
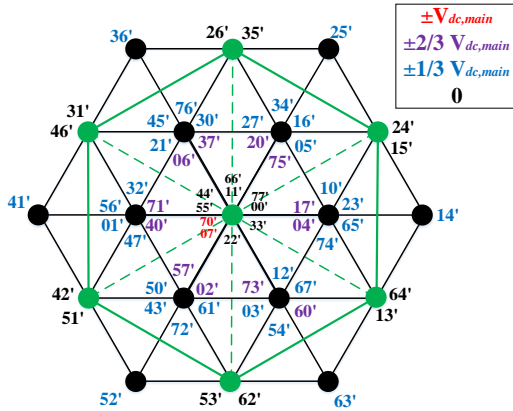Fig. 14: Dual inverter type II (with a common DC-link).

Fig. 16: Dual inverter type III (with a FC).

Fig. 15: D-CMV by the dual inverter type II.
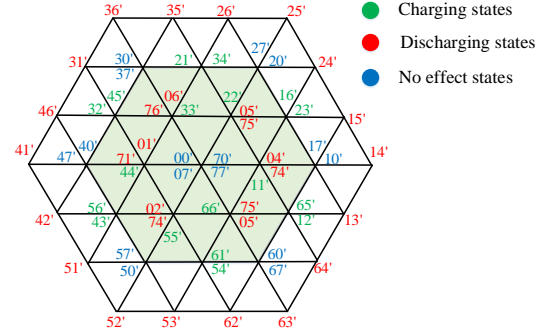
Fig. 17: Dual inverter type III with 1:0.5 using the passive regulation [31].

contribution to the real power [96]. Thus, significant effort has been made to eliminate or reduce D-CMV [45], [46], [48], [48], [77]–[81].

In Fig. 15, the D-CMV generated by the dual inverter type II is shown. This figure can be obtained by using Equation (6). Since the two inverters share one voltage source, this implies that $V_{dc,main} = V_{dc,aux}$. Fig. 15 shows that switching states can lead to seven different levels of D-CMV, i.e. 0, $\pm\frac{1}{3}V_{dc,main}$, $\pm\frac{2}{3}V_{dc,main}$ and $\pm V_{dc,main}$. In [45], [47], [51], [52], [79]–[81], only the switching states that results in zero D-CMV are utilized for modulation purposes, and these are shown with the green points in Fig. 15. An alternate-SHC scheme is presented in [79]–[81], aiming to distribute the losses evenly between two inverters. The zero states are redistributed to suppress D-CMV [46], [77]. Reference [77] claims that if the angle difference of θ_{main} and θ_{aux} is 120° (see Fig. 6), D-CMV can be virtually eliminated.

However, similar to the CMV reduction in a two-level inverter, all the D-CMV elimination methods for a dual inverter would inevitably sacrifice the output quality. As shown in Fig. 15, the output level is degraded from three-level to two-level, fulfilling the zero D-CMV. More importantly, the vertices of the space vector diagram (14', 25', 36', 41', 52', and 63') in Fig. 15 cannot be used for modulation, thus reducing the voltage utilization by 13.4% [45], [47], [52].

C. Type III

Compared to the dual inverter type I and II, type III integrates the advantage of virtually no ZSC circulation or any need for isolation circuitry. However, the major challenge with this configuration is to maintain the FC voltage due to
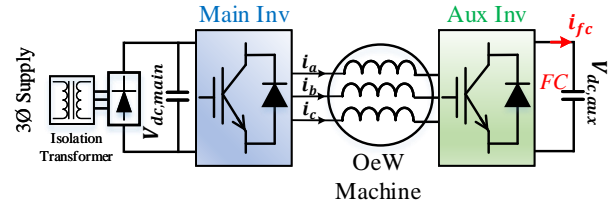
its floating nature [24]. References [31], [38] claim that if achieving the FC voltage regulation and multilevel operation at the same time, the performance of the dual inverter with a FC has to be compromised.

In [31], [33], [35], [36], [38], [85], the coupled modulation method is selected where from a modulation perspective, the dual inverter is considered as a whole inverter. The effect of switching states on the capacitor voltage is analyzed in steady-state operation [31], [36], [85]. The method proposed in [31] is shown in Fig. 17, where all the switching states are divided into three groups: the charging states in green, the discharging states in red and the no effect states in blue. In [31], there are no charging states at the outermost space vector diagram, and thus it can be said that the voltage utilization is constrained within the DC-link voltage of the Main-Inv, i.e. the green hexagon in Fig. 17. Under this condition, the capacitor voltage, which can be substantially beneficial for motor drive applications, is under-utilized [24], [91]. On the other side, the voltage output level is reduced from four to three. The analysis in [31], [36], [85] assumes the current direction, but the instantaneous current that flows into the capacitor is practically defined by the motor PF angle [33], [38]. Essentially, these methods [31], [36], [85] are attributed to passive regulation without the need for load current information.

In [38], a regulation scheme that involves the feedback of the motor PF angle is developed. Besides, a redundant state selection table that requires current feedback based on the level-shifted PWM technique is investigated in [33], [35]. A particular M.I. zone is identified for the reference vector of a dual inverter in [34]. To operate within that zone and supply the required voltage at the same time, a variable DC source is necessary. This would increase the complexity of the system and may raise instability problems.

Similar to the active regulation method developed for the

dual inverter type I (see Section VI-A), it has been extended for type III in [24]. Compared to avoiding the overcharge issues by selecting the states associated with negative currents, FC voltage regulation schemes appear to be more complicated. This is because the associated current needs to be carefully controlled such that the FC voltage can be maintained at the desired level. In [24], the capacitor charge variations by using all switching states are analytically derived. Depending on the difference between the measured FC voltage and its reference value, the dwell time among redundant states will be allocated. Compared to using the passive regulation, the advantages of proposed active schemes include a boosted voltage utilization and improved output quality [24], [25].

The FC voltage regulation also can be achieved using decoupled modulation. In [29], [33], [40], [42], [87], [90], the FC is treated as a reactive power compensator such that it accommodates all the reactive power where the active power into FC should be zero at the steady state. Under this consideration, the FC voltage regulation could be readily accomplished by controlling the active power flowing into FC via a proportional-integral controller. In [88], the M.I. of reference vector for the Aux-Inv is maintained at the maximum, and then the M.I. of reference vector for the Main-Inv is employed for the FC voltage regulation. In addition, one particular control freedom of the decoupled modulation is to vary the angle between two reference vectors, which is taken advantage of regulating FC voltage in [16]. However, as emphasized in Section IV-B, the decoupled modulation would lead to undesirable voltage steps, which deteriorate the output performance [91].

In [86], a modulation strategy that the Main-Inv utilizes the staircase modulation to switch at the fundamental frequency whereas the Aux-Inv operates at high-frequency PWM is reported. The FC voltage is regulated by adjusting the firing angle of the fundamental voltage reference for the Main-Inv. This scheme could considerably reduce the switching losses of the system since the Main-Inv is operated at the fundamental frequency. However, it is not suitable for some operation regions, and also it is perceived as a relatively complex implementation [85].

VII. PERFORMANCE EVALUATION ON DUAL INVERTERS

In this section, the performance of dual inverter topologies in terms of the fault-tolerant capability, the inverter output power quality and the DC-link voltage utilization is assessed. This is followed a final recommendation of the most suitable topologies for MEA applications.

A. Fault-Tolerant Capability

The fault-tolerant capability is of great interest for safety-critical aerospace applications. As seen in previous discussions, the DC-link voltage utilization and the inverter output power quality may be affected by all three design freedom of dual inverters. However, the fault-tolerant capabilities of dual inverters only depend on their configurations.

Among three types of dual inverters, type II has the highest degree of fault tolerance as it is symmetrical [98], [99].
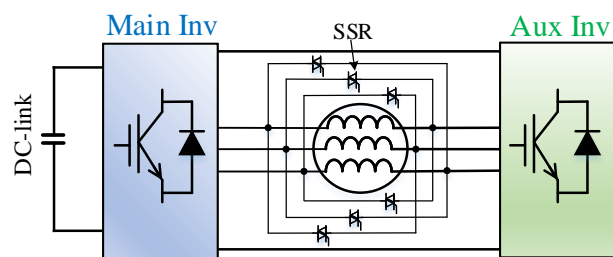

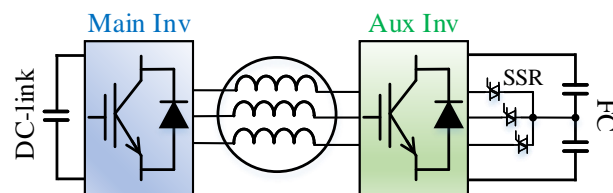Fig. 18: Reported dual inverter type II structure with the enhanced fault tolerance in [97].

Fig. 19: Reported dual inverter type III structure with the enhanced fault tolerance in [19]–[21].

Researchers in [100] proposed a predictive control that can well compensate the ZSC under the case of single-phase open-fault. It was proven that this particular configuration could accommodate up to six diode/switch open-circuit faults using the proposed post-fault zero-sequence current injection in [98]. To enhance the fault-tolerant capability of dual inverter type II, six additional bidirectional solid-state relays (SSRs) are added in [97], as shown in Fig. 18. For this structure, the fault-tolerant operation can be realized by winding reconnection for open-circuit fault in up to three legs, without lowering the output capacity [97].

Dual inverter type I exhibits a slightly lower fault tolerance capability to type II. Once one inverter, Main-Inv or Aux-Inv, is failed, its three bridges can be shorted, forming a neutral point [101], [102]. In comparison, type III exhibits relatively limited fault tolerance, where the faults can be resolved only for the switches on the Aux-Inv [25], [37]. When the switches on the Aux-Inv are failed; its three bridges can then be shorted, forming a neutral point [31]. The fault-tolerant capability of the dual inverter type III can be enhancing by including three SSRs, as shown in Fig. 19, where the Aux-Inv can be reconfigured to a four-switch inverter with one-phase fault [19]–[21].

B. Voltage Utilization and Power Quality

After studying fault tolerance, this part will focus on the rest two performance aspects. Table III summarizes all the state-of-the-art research on dual inverters in literature. With three exclusive design freedom featured by dual inverters and different voltage regulation methods, the converter performance in terms of the power quality through the number of output levels and the voltage utilization can be varied, as shown in Table III.

According to Table III, the dual inverter type II contributes to the highest voltage utilization of $1.73V_{dc}$, but with relatively

TABLE III: Summary of all the studied dual inverters in literature

Dual Inverter Design Freedom			Voltage Regulation Method	Performance		Paper
①Configuration	②Modulation strategy	③Voltage ratios		DC-link Voltage Utilization k	Output Quality (level number)	
Type I	Coupled	1:1	N.A.	1	High (3)	[57]–[59]
		1:0.5	Passive regulation		High ($<$4)	[44], [68], [71]
			Active regulation		**Very high (4)**	[43]
	Decoupled	1:1	N.A.	1	Low	[69], [70]
		1:0.5	Unequal reference voltages sharing			[73]
Type II	Decoupled	1:1	Apart θ_{main} and θ_{aux} by 120°	$<$2	Low	[77]
	Coupled		Utilize states with zero D-CMV	**1.73**	**Medium (2)**	[51], [52], [81]
Type III	Decoupled	1:2.5	Reactive power control	$>$1	Low	[40]
		1:1		Up to $\sim$1.3		[42]
		1:1		1-1.35		[94]
		Varied		1-1.6		[16], [90]
		1:2		Up to 2		[41]
	Coupled	1:0.5	Passive regulation	1	High (3)	[31], [38], [93]
			Active regulation	1.1-1.5	Very high (4)	[24]
		1:0.5+1.1	Active regulation	**1.1-2**	**Very high (3-4)**	[25]

Fig. 20: Overall assessment of inverter topologies with 12 switches for MEA applications.

C. Final Assessment

Fig. 20 selects three dual inverter candidates after the overall assessment in the above discussion. The chosen inverters are dual inverter type I with the voltage ratio 1:0.5 in the blue triangle, dual inverter type II in the red triangle and dual inverter type III with the voltage ratio 1:0.5 and 1:1 in the green triangle, as shown in Fig. 20. Besides, the DCI in the yellow colour, a representative of multilevel inverters, is also included in Fig. 20 as the benchmark.

It can be seen from Fig. 20 that the dual inverter type III with 1:0.5 and 1:1 performs the best in terms of the output power quality and the DC-link voltage utilization. As for fault-tolerant capabilities, the dual inverter type II is the strongest, following by type I, type III, while the DCI is the lowest, as shown in Fig. 20.

A DCI is supposed to generating a three-level output voltage, but it suffers from the neutral point fluctuation. To balance the DC-link capacitors while retaining the full DC-link voltage utilization, the DCI has to lower the output quality [13], [15], as shown in Fig. 20. It was reported that DCI has a very limited fault tolerance where only one short-circuit fault can be accommodated [103].

It is undoubted that from the point of view of finding a suitable motor drive, dual inverter type III with 1:0.5 and 1:1 is the best choice. A considerably high-voltage utilization together with maintaining good power quality are achievable at the same time. This topology can be particularly beneficial for MEA applications, adopted with relatively low dc-link voltages. Higher speed motor drives are an obvious choice fulfilling the stringent requirement of MEA applications in terms of high power density coupled with higher efficiency, but their wide-speed operation is essentially subject to the DC bus voltage onboard. By fully exploiting the FC voltage, the machines' constant-torque region can be boosted, allowing

low output quality (two-level operation) on account of avoiding the ZSC [51], [52], [81]. Alternatively, the dual inverter type III with the ratios 1:1 and 1:0.5 using coupled modulation and active regulation could achieve a comparable utilization [43], as shown in Table III. Considering the power quality aspect in Table III, the dual inverter type I with 1:0.5 and type III with the ratio ratios 1:1 and 1:0.5 comprise the best results with a perfect four-level operation [25].

motors to minimize their weight and volume considerably [24], [25]. Besides, the machines' constant-power region also can be extended as the FC can be regarded as a reactive power compensator [104]–[106].

On the other side, the standard two-level converter still dominates in MEA, while applying the three-level converter such as DCI with better power quality have been intensively discussed [5], [6], [13], [15], [107]. It is apparent from Fig. 20 that the dual inverter type III with 1:0.5 and 1:1 can provide superior output quality compared to using a DCI. This excellent harmonic profile can potentially reduce machines losses [108]. Above all, the dual inverter type III with 1:0.5 and 1:1 is the optimal topology driving the high-performance machines.

However, if fault tolerance is the most vital consideration, dual inverter type II will be the best choice. And when taking the output power quality into account, the dual inverter type I with 1:0.5 may stand out. However, it is worth mentioning that this particular configuration needs isolation between two power supplies. This means that the dual inverter type I is more suitable for the system powering by the batteries with natural isolation.

VIII. IMPLEMENTATIONS OF DUAL INVERTERS IN MEA

A. Suitable Applications

The reliability of power electronics has been identified as one of the most crucial challenges for their promotion in MEA applications [109]. The key areas for safety-critical consideration are generators, primary flight surface control, landing system, and fuel pumps [10]. Therefore, dual inverter type II is recommended due to its extremely strong fault tolerance. For the electric systems with lower reliability requirement, such as the secondary actuators, the dual inverter type III can be selected. This topology may be broadly used once enhancing its fault-tolerant capability by involving three more SSRs, as seen in [19]–[21]. However, the weight increase and power consumption of those three SSRs need to be further investigated.

B. Switching Device Choice

In the last two decades, the commercial application of silicon carbide (SiC) devices are prone to have profound implications on the development of MEA applications [1], [5], [107]. Compared to silicon (Si) -based devices, the ones using SiC can operate at greater voltage, higher temperature, faster switching frequency [107]. Researchers in [8], [9] studied the performance of dual inverter type II with a full SiC and with hybrid SiC and Si solutions for starter-generator applications in MEA. For the hybrid one, the Main-Inv is built by Si-IGBT switching at the fundamental frequency, while the Aux-Inv is constituted by SiC-MOSFET switching at higher frequencies [47], [48]. This hybridization can reduce the converter loss compared to the full SiC solution but with a compromised output quality [110]. However, considering the whole drive system, a full SiC solution is still recommended due to their faster switching frequencies such that higher speed machines are feasible [6], [12], [111].

C. Future Trends

Compared to a standard machine, there is no additional manufacture, cost challenge or extra magnetic modifications raised by the OeW machines [110], [112]. In fact, the OeW machines fed by dual inverters have been extensively used in commercial hybrid-/all- electric vehicles with similar DC-link voltage constraints as seen in MEA [113]. In many cases, the aircraft are utilizing inverter topologies from automotive applications [1]. Therefore, the OeW motor drives penetration can be identified as a promising trend for MEA applications in the near future.

IX. SUMMARY

In this paper, a comprehensive technical review of dual inverter topologies for motor drives in MEA applications was conducted. The operation principle, modulation schemes, capacitor voltage regulation, and the voltage ratio considerations of dual inverters were elaborated in sequence. To identify an optimal power inverter configuration, the dual inverters in three types with all applicable voltage ratios were considered. Their performance covering the DC-link voltage utilization, the output quality and the fault-tolerant capability were assessed. After a holistic comparison, the dual inverter type III with 1:0.5 and 1:1 was recommended due to its high voltage utilization coupled with maintaining good power quality. And the dual inverter type II was preferred in case the fault tolerance is the essential requirement. It has been proven that those two dual inverter topologies have emerged as significantly competitive choices against other multilevel inverter topologies for MEA applications.

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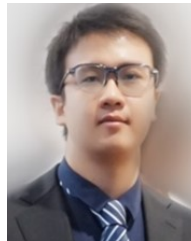
Zhen Huang received the B.Eng. (hons.) degree in electrical and electronics engineering in 2015, and the Ph.D. in electrical engineering in 2019, both from the University of Nottingham, Nottingham, UK.

Since January 2020, he has been a Research Fellow with the Power Electronics, Machines and Control Group, the University of Nottingham. His research interests include high-speed machine drives, multilevel converters, and on-board electrical power system protection for hybrid/all-electric vehicles and more/all-electric aircraft applications.

Tao Yang (Senior Member, IEEE) received the M.Eng Degree from Shanghai Jiao Tong University, China in 2008 and the Ph.D. degree in electrical engineering from the University of Nottingham, UK in 2013. His PhD research within EU Clean Sky on 'Modelling electrical power system for more-electric aircraft applications' has resulted in him winning the inaugural Clean Sky Best PhD Award in 2016.

Since 2013, he has been a Researcher with Power Electronics, Machines and Control Group, University of Nottingham, where he became an Assistant Professor in 2016, and an Associate Professor in 2019. His research interests include high-speed electric motor drive control, power electronic conversion, electrical system design and optimization for more electric/hybrid/all-electric aircraft applications.

Dr. Yang is an Associate Editor for the IEEE TRANSACTIONS ON TRANSPORTATION ELECTRIFICATION and *Chinese Journal of Aeronautics*.

Paolo Giangrande (Senior Member, IEEE) received the bachelor's (hons.), master's (hons.), and Ph.D. degrees in electrical engineering from the Politecnico of Bari, Bari, Italy, in 2005, 2008, and 2011, respectively.

Since 2012, he has been a Research Fellow with the Power Electronics, Machines, and Control Group at the University of Nottingham, U.K. In 2018, he was appointed as a Senior Research Fellow and he is currently the Head of the Accelerated Lifetime Testing Laboratory at the Institute of Aerospace Technology, Nottingham. His main research interests include sensorless control of ac electric drives, design and testing of electromechanical actuators for aerospace, thermal management of high-performance electric drives, and lifetime modeling of electrical machines.

Pat Wheeler (Fellow, IEEE) received his B.Eng. (hons.) in electrical engineering in 1990 and his Ph.D. degree for his work on matrix converters in 1994, both from the University of Bristol, Bristol, U.K.

In 1993, he moved to the University of Nottingham, Nottingham, U.K., and worked as a Research Assistant with the Department of Electrical and Electronic Engineering. In 1996, he became a Lecturer with the Power Electronics, Machines and Control Group, University of Nottingham, where he has been a Full Professor since January 2008. From 2015 to 2018, he was the Head of the Department of Electrical and Electronic Engineering, University of Nottingham. He has authored/co-authored over 700 academic publications in leading international conferences and journals.

Prof. Wheeler is currently the Head of the Power Electronics, Machines and Control Research Group, Global Director of the University of Nottingham's Institute of Aerospace Technology and was the Li Dak Sum Chair Professor in Electrical and Aerospace Engineering (2016 to 2020). He is a member of the IEEE PELS AdCom and was an IEEE PELS Distinguished Lecturer from 2013 to 2017.

Michael Galea (Senior Member, IEEE) received the Ph.D. degree in electrical machines design from the University of Nottingham, Nottingham, U.K., in 2013.

He was appointed as Lecturer, as Associate Professor, and as Professor in electrical machines and drives with the University of Nottingham, in 2014, 2018, and 2019, respectively. He currently lectures in electrical machines and drives and in aerospace systems integration and manages a number of diverse projects and programmes related to the more/all electric aircraft, electrified propulsion, and associated fields. His main research interests include design and development of electrical machines and drives (classical and unconventional), reliability and lifetime degradation of electrical machines and the more electric aircraft.

Dr. Michael is a fellow of the Royal Aeronautical Society. He also serves an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and for the IET ELECTRICAL SYSTEMS IN TRANSPORTATION.