Solid-State Electronics 186 (2021) 108173

Contents lists available at ScienceDirect

Solid State Electronics

journal homepage: www.elsevier.com/locate/sse

Performance and reliability in back-gated CVD-grown MoS_2 devices

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ARTICLE INFO

Handling Editor: Bogdan Cretu

Keywords:
Transition metal dichalcogenide
Molybdenum disulfide
MoS_2
Two-dimensional materials
More than Moore
Reliability
Low-frequency noise

ABSTRACT

In this work, the electrical performance and reliability of as-synthesized CVD-grown MoS_2 transistors directly grown on SiO_2/Si substrate without any transfer process have been evaluated. Transfer and output characteristics, current hysteresis, capacitance-voltage and low-frequency noise signatures have been characterized revealing the huge influence of surface and oxide defects and the disturbance due to the fluctuations of the carrier number on the back-gated transistor response.

1. Introduction

Since the discovery and isolation of graphene has been awarded with The Nobel Prize in Physics [1,2], two-dimensional (2D) materials have received an outstanding attention from various fields, especially in electronic, optics and photonic applications [3–5]. These 2D materials have demonstrated an optimal electrostatic control of the channel thanks to their reduced thickness with potentially better immunity to short channel effects than the planar silicon counterparts [6]. However, despite the exceptional properties of graphene [7], the absence of a band gap limits its application in digital electronics. As alternative, the transition metal dichalcogenides (TMDs) have taken advantage of the reduced thickness with a non zero-bandgap to preserve interesting properties in electronic applications [8]. Advantages in terms of higher ON/OFF ratios, reduced power consumption, lower current leakage and shorter switching delay are expected according to the International Roadmap for Devices and Systems (IRDS) guideline [9]. Inside the TMDs family, molybdenum disulfide (MoS_2) has emerged as a prominent candidate to advance in the progressive scaling of the semiconductor industry. MoS_2 presents indirect to direct bandgap transition as the film thickness is reduced from multilayer to monolayer due to quantum confinement. Moreover, a band gap in the range of 1.2–1.8 eV [10], makes it suitable for near-infrared absorption and emission applications in optoelectronics. However, in general terms, the fabrication and processing of these materials to be integrated in ultimate electronic devices is still a bottleneck. Costly fabrication methods and non-optimized integration with industrially standardized insulators and materials result in device performances which rarely accomplish the promising theoretical properties. On the one hand, the advance on the synthesis method is crucial. Despite fundamental physics and devices on 2D TMDs have relied on the exfoliation method [11,12], wafer-scale deposition of films with well-controlled properties is mandatory in semiconductor industry. In this regard, vapor deposition techniques (CVD) [13,14], metal–organic CVD (MOCVD) [10] or plasma enhanced chemical vapor deposition (PECVD) [15,16] are being extensively explored due to their potential for high scalability. Withal, precise film deposition with well-controlled properties and thicknesses is still a challenge. On the other hand, despite the advances on the device reliability when using these materials [17–19], defects and impurities (grain boundaries, corrugation, sulfur vacancies, oxygen or moisture incorporation and oxide ions) still play an important role on the actual drop in performance of the fabricated transistors (Schottky barriers and current hysteresis). To advance in this aspect, in our previous work, we addressed the scalable fabrication of back-gated MoS_2 devices following a chemical vapor deposition (CVD) synthesis, without any film transfer, and a standard CMOS photolitography and etching processing [20]. The transient

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https://doi.org/10.1016/j.sse.2021.108173
Received 7 December 2020; Received in revised form 11 June 2021; Accepted 16 June 2021
Available online 19 August 2021

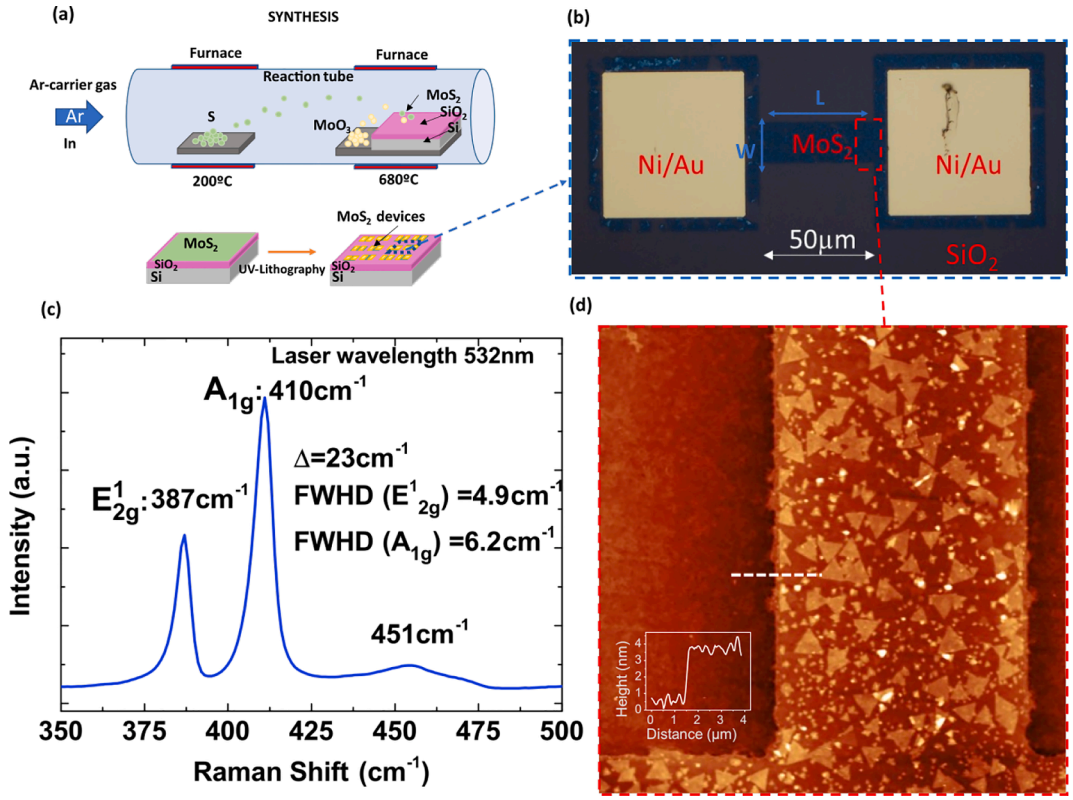

Fig. 1. a) Scheme of the synthesis (top) and lithography (bottom) processes. b) Optical image of a fabricated 50 μm-length device. MoS_2 appears as a blue layer. c) Raman characterization of the synthesized MoS_2 layer carried out using 532 nm-wavelength laser. d) Atomic force microscopy a MoS_2 device. Inset: topography profile corresponding to the dashed line.

response of the conformed Schottky barrier devices were analyzed. In this work, we extended this study to evaluate the performance and the reliability implications of these fabricated transistors. Importantly, these devices have not been passivated or encapsulated in order to address the investigation on the inherit properties of the interfaces and the as-synthesized material. Moreover, this kind of study is mandatory to determine the potential of these devices as sensors or detectors, where direct interaction of the target with the surface of the bare material could be required. Regrettably, the absence of encapsulation, passivation layers or the characterization under ambient conditions make that variability due to disturbing mechanisms (defect, adsorbates, oxide traps …) could be comparable with the effect of dimension scaling (L or W) in the electrical parameters. This is the reason why despite having devices with different footprints, this study is more focused on determining the possible origin and implications of these disturbing mechanisms than on the optimization of the devices in terms of channel length or width.

2. Experimental and measurement setup

The direct synthesis of large-area MoS_2 films on an n-type silicon substrate (1×10^{15} cm^{-3}) covered by a 100 nm-thick SiO_2 layer was accomplished via CVD through sulfurization of molybdenum trioxide (MoO_3) at a maximum temperature of 680 °C [20]. This process was carried out in a two-temperature-zone furnace as Fig. 1.a (top) indicates. Later, optical photolithography was employed to define the source and drain patterns, a scheme is shown in Fig. 1.a (bottom) summarizing the process: electron beam evaporation was used to deposit the Ni/Au electrodes. The thicknesses of Ni and Au were 20 nm and 200 nm, respectively. A lift-off process was carried out to complete contact fabrication of the back-gated MoS_2 FET. Then, a dry etching of the MoS_2 material outside the channel between S/D contacts was performed. The hard mask employed during the photolithography process allowed the fabrication of devices with a range of different channel lengths and widths as the optical microscope characterization shows (Fig. 1.b). The observed pads correspond to drain and source contacts. To improve the conductivity and reduce the contact resistance, the metal pads (Ni/Au) are deposited directly on the MoS_2, i.e, there is a MoS_2 layer underneath the deposited contacts increasing the contact area. Regarding the layer thickness, the structural analysis was carried out by Raman spectroscopy (Jasco NRS-5100) and atomic force microscopy (NTMDT NTEGRA). The static DC characteristics were acquired using a Keithley SCS 4200 and an Agilent B1500 systems. The low-frequency noise characterization was carried out using a low-noise-current amplifier connected to a software-based spectrum analyzer [21].

3. Results and discussion

3.1. Structural characterization

Fig. 1.c shows the Raman characterization of the MoS_2 film exhibiting the two Raman characteristic bands at 387 (E^1_{2g}) and 410 cm^{-1} (A^1_g) with a shift between peaks (Δ) around 23 cm^{-1}. These results are consistent with the presence of thin MoS_2 layers [22]. The additional peak observed at 451 cm^{-1} is usually attributed to disorders or partial oxidation on the MoS_2 sample [23]. This fact could suggest the presence of dislocation or impurities on the MoS_2 layer. In this case, due to the absence of any passivation on the samples, these disorders may be caused by the interaction with the ambient, with the SiO_2 interface or be intrinsic to the material growth. Fig. 1.d shows the result of the atomic force microscopy characterization. Channel conformed by coalescence of triangle flakes of MoS_2 can be inferred. As the topography profile shows in the inset of Fig. 1.d, this device presents a 4 nm-thick MoS_2 channel approximately. Under similar synthesis conditions, samples

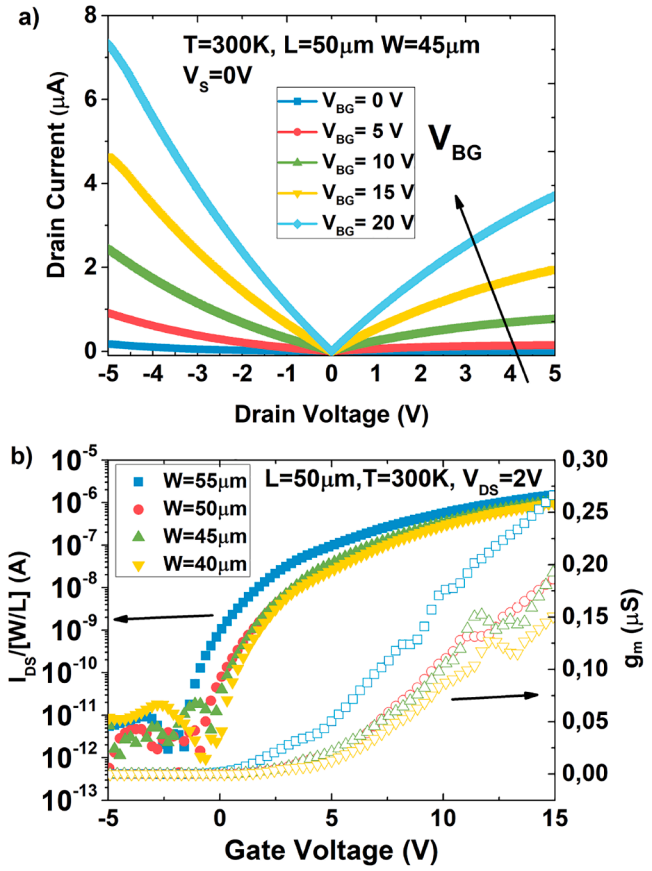

Fig. 2. a) Output characteristic for different back-gate biases. b) Normalized transfer characteristic for different device widths and the correspondent transconductace. Asymmetrical behavior in a) and absence of hole current in b) are attributed to back-to-back Schottky barriers. The Schottky barriers are modulated with the back-gate bias.

with down to 1.5 nm-thick MoS_2 channels have been achieved [20].

3.2. Electrical performance

The output characteristic (I_D-V_D) of a 50 μm-length and 45 μm-width device is depicted in Fig. 2.a. Different back-gate biases (V_{BG}) reveal the modulation of the channel resistance with the applied voltage. The non-symmetrical and non-linear nature of these curves indicates the formation of back-to-back Schottky diodes in the metal–semiconductor interfaces [17,20].

Fig. 2.b shows the normalized transfer characteristic (I_D-V_{BG}), in logarithmic scale, for devices with different channel width. Despite the work function of the selected metals (Ni/Au) would facilitate the ambipolar behavior (both electron and hole currents), the curve presents only electron current characteristic. This absence of hole current demonstrates the Schottky barrier formation which blocks these carriers. This Schottky barrier is usually attributed to Fermi level pinning at the metal–semiconductor interface [24]. An extensive study of the Schottky barrier formation and how the current is modeled by the thermo-ionic emission in these devices can be found in [20]. The ON/OFF current ratio for these devices is around 10^6. The transconductance is depicted in the right axis in Fig. 2.b. The curves present a monotonic increasing behaviour with a lack of saturation in the drain current. This result could be explained considering that the source-drain current is not only modelled by the carrier density in the channel but also by the Schottky diodes (metal–semiconductor junctions) whose barrier height depends on the applied gate bias as demonstrated in [20]. Due to the singular behavior of our devices with this monotonic increase in the

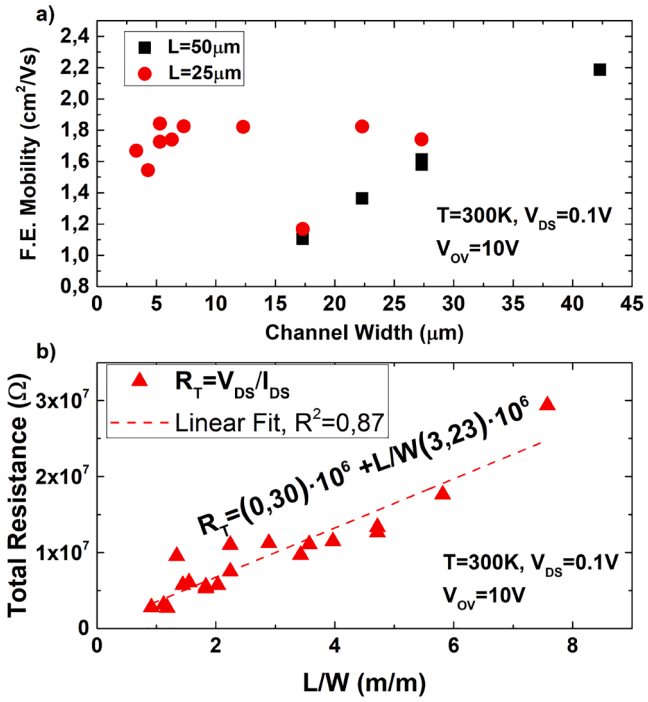

Fig. 3. a) Field effect mobility for two different gate lengths as a function of the channel width. b) Total resistance as a function of the channel dimension ratio (L/W). In dashed line the regression curve for the extraction of the sheet and contact resistances. Gate overdrive voltage, V_{OV} = 10 V and low lateral voltage V_D = 0.1 V.

transconductance, the mobility will present an increase with the gate voltage where field effect mobility (μ_{FE}) can be calculated following the expression:

$$\mu_{FE} = \frac{1}{C_{ox}} \frac{L}{W} \frac{dI_{DS}}{dV_{GS}} \frac{1}{V_{DS}} \quad (1)$$

where $C_{ox} = \epsilon_{ox}/t_{ox}$ is the capacitance per unit area of the SiO_2 gate oxide dielectric, L and W are the channel length and width, respectively. Fig. 3.a shows the case for a gate overdrive voltage (V_{OV}=V_G-V_T), V_{OV} = 10 V, and devices of two channel lengths and different channel widths. A smooth decrease in the mobility is presumable reducing the device dimensions, probably due to the higher influence of border effects and traps in smaller channels. The highest mobility observed in our characterized devices corresponds to $\mu = 2.2\ cm^2V^{-1}s^{-1}$. This mobility results are around one order of magnitude lower than the reported in other studies after annealing or passivisation processes [25,26]. This effect could indicate that mobility is also limited by process residuals, surface roughness and other defects specially presented in these non-passivated devices.

Regarding the semiconductor conductance and contact resistance, Fig. 3.b depicts the total resistance measured as a function of the physical dimension ratio (L/W) of the devices. Through these results the sheet resistance, conductance and contact resistance can be extracted. Considering the total resistance should follow the expression: $R = (L/W)\rho_S + 2R_C$ where $\rho_S = \rho/t$ being ρ the material resistivity, t the thickness and Rc the corresponding contact resistance. Please note that this evaluation method could underestimate the value of mobility, contact and channel resistances. However this extraction could present a reasonable approach in absence of TLM structures [27] or when more accurate methods such as Y-function based method [28] cannot be applied due to the contact resistance dependence with gate voltage. From the experimental extrapolation (dashed curve in Fig. 3.b) the results are $\rho \approx 1.3\ \Omega.cm$ and the contact resistance $R_C \approx 0.15\ M\Omega$ ($t \approx 4$ nm V_{OV} = 10 V and V_{DS} = 0.1 V).

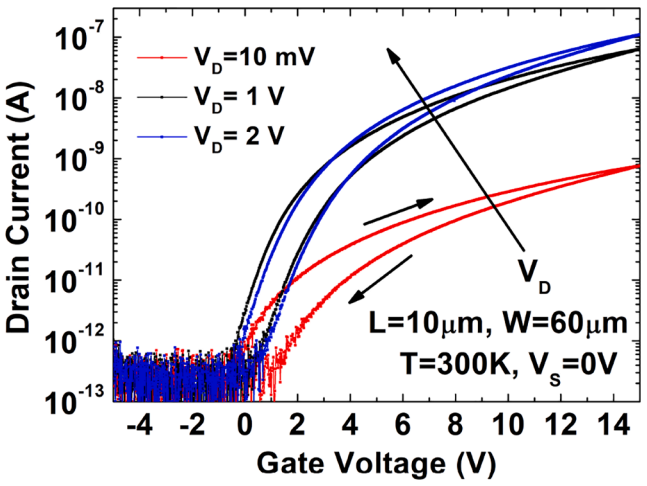

Fig. 4. Transfer characteristic of a back-gated transistor for different drain voltages in a double voltage sweep. L = 50 μm, W = 45 μm.

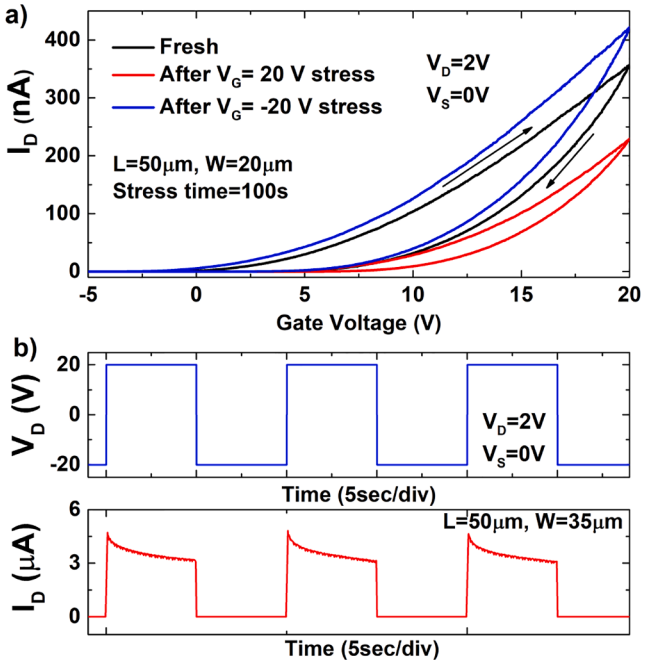

Fig. 5. a) Transfer characteristic for a device at fresh conditions (blue), after a gate pulse of 20 V for 100 s (red) and after a gate pulse of −20 V for 100 s (blue). Drain current response of a device (bottom) to successive positive (stress) and reverse (recover) back gate pulses (top). L = 50μm, W = 35μ. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

The relative low mobility and the high contact resistance, together with the Fermi-level pinning causing the Schottky barriers at the contact-MoS_2 junction, may have their origin in defects, traps and impurities but not exclusively in these phenomena. To further analyze these issues and the implications of defects in the reliability of the devices, Fig. 4 depicts the transfer characteristic of a 10 μm-length and 60 μm-width device in a double gate voltage sweep characterization for different drain biases.

The current hysteresis for different drain voltages shown in Fig. 4 suggests the presence of traps at the MoS_2/SiO_2 interface, surface or in the oxide. Although in our previous work we demonstrated that an anti-clockwise behavior (for thicker devices) may suggest initial transient response of the device which needs an initial time to form the inversion

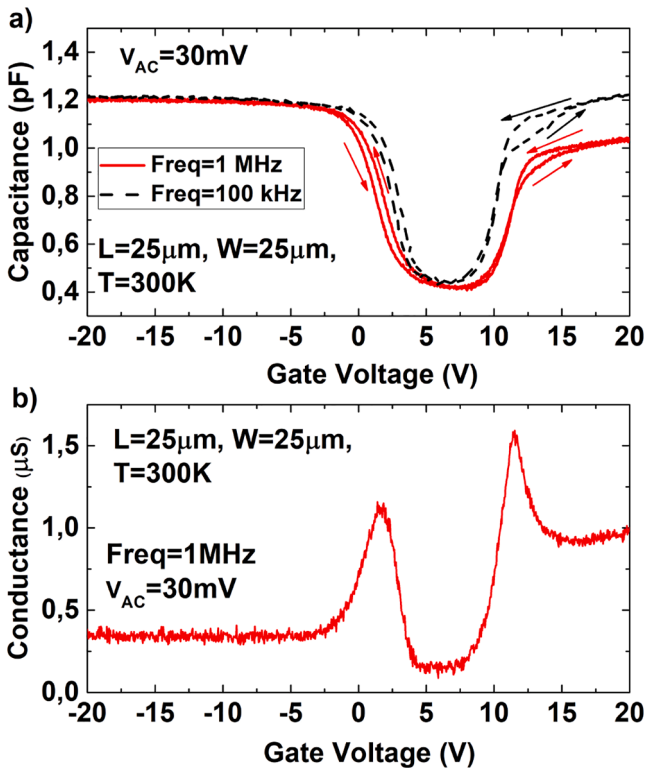

Fig. 6. a) Capacitance–voltage (C-V) characteristics for two frequencies and b) Conductance-voltage (G-V) characteristic. Room temperature for a L = 25 μm and W = 25 μm back-gated device.

layer [20], in this case the clockwise behavior (marked with the arrows) points to trapping and detrapping carrier phenomena and mobile ions in the oxide or at interface as main mechanism [29,18,30,31]. A charge density change during the characterization induces a shift (increase) in the threshold voltage, therefore the channel resistance is higher (lower current level) in the backward voltage swept. When a forward gate bias is applied, the traps whose energy levels are below the Fermi level are filled by electrons with different characteristic times. The trapped electrons and the shift of mobile ions contribute to the increase of negative charge and therefore, increase the threshold voltage. To determine if this threshold voltage shift is permanent, the transfer characteristic of a device is characterized before and after applying positive and negative back gate pulses, Fig. 5.a. As Fig. 5.a shows, this threshold voltage shift can be totally inverted with a recovery pulse. A more complete perspective of these effects can be acquired measuring the device response while the stress/recovery gate voltage pulses are applied, Fig. 5.b. Please note that the on-operation of the device happens only for the positive gate bias. In this on-the-fly characterization both previous effects are observed: i) there is a current decay as a function of the time while a positive voltage pulse is applied, which induces the hysteresis at double sweep characterizations (Figs. 4 and 5.a); and ii) the initial current level is recovered after the negative pulse (V_G=-20 V), repeating the same response in successive stress periods. The origin of defects and ions which induce these characteristic response on the devices could be associated with both extrinsic (diffused water molecules and the chemisorption of oxygen and intrinsic defect at the interface due to oxygen and sulfur vacancies [32,18,29], or even defects due to a non-passivated surface bonds of the MoS_2 [33].

More information regarding the type of defects can be determined through capacitance–voltage (C-V) characterization. The measurement is carried out directly on the fabricated MOSFET devices ($Si/SiO_2/MoS_2$), where the force and low biases are applied at the Si substrate and at the drain contact, respectively. Fig. 6.a shows the C-V characteristic of

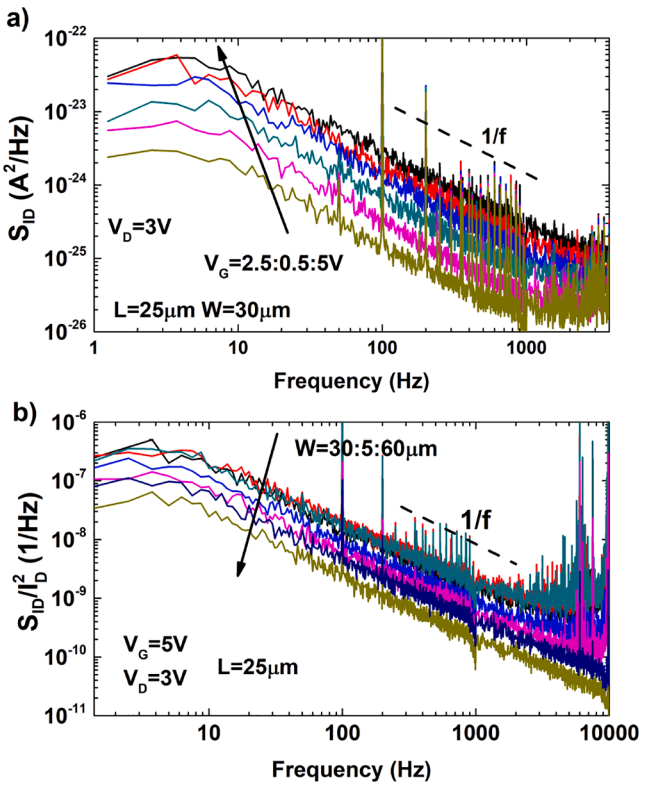

Fig. 7. a) Spectral density of the noise for a L = 25 μm and W = 30 μm device for different gate biases. V_G from 2.5 V to 5 V with 0.5 V step. b) Normalized spectral noise density of the current as a function of the frequency for different device dimensions. W from 30 μm to 60 μm with 5 μm step. V_S = 0 V, T = 300 K.

a 25 μm-length and 25 μm-width device. Two frequencies (f = 100 kHz and f = 1 MHz) are recorded both for double voltage sweep measurements. The structure presents a clear accumulation channel, a depletion region and a inversion channel corresponding to the electron carriers (positive voltages at the back gate). Note that the measured maximum capacitance (C_{ox} = 1.24 pF) agrees with the theoretical oxide capacitance value (C_{ox}) for a 100 nm-thick SiO_2 oxide and the area of the contact. Regarding the influence of traps in the device behavior, this device presents frequency dispersion in the inversion region, usually attributed to border traps [34]. A shift in the flat-band and threshold voltage is also inferred from the C-V characteristic. This shift depending on the signal frequency is attributed to the interface traps [34,19]. In accordance with this suggestion is the presence of conductance (G_p) peaks shown in Fig. 6.b, which marks the activity of mid-gap traps representing the losses due to the exchange of carriers with the interface traps [35,36,34].

Additionally to C-V and I-V characteristics, low-frequency noise characterization may shed light on the traps and defect origin. Fig. 7.a depicts the spectrum of the current noise for different gate biases. The spectral signature presents an unambiguous 1-decade/1-decade characteristic associated with the flicker ($1/f$) noise contribution [37–39]. Flicker noise is usually caused by imperfections of the fabrication process and material defects appearing mostly at low frequencies. In transistors, the trend was described by McWhorther [37], who attributed the source of 1/f noise to slow oxide traps, ruled by the carrier tunneling between the inversion channel and slow oxide traps located at the Si-SiO_2 interface. The result is a carrier number fluctuation during the device operation. As previous C-V and Raman characterizations indicate, in our devices, the carrier trapping phenomena could take place both at the semiconductor surface due to the non-passivated characteristic and in the oxide traps located close to the MoS_2/SiO_2 interface.

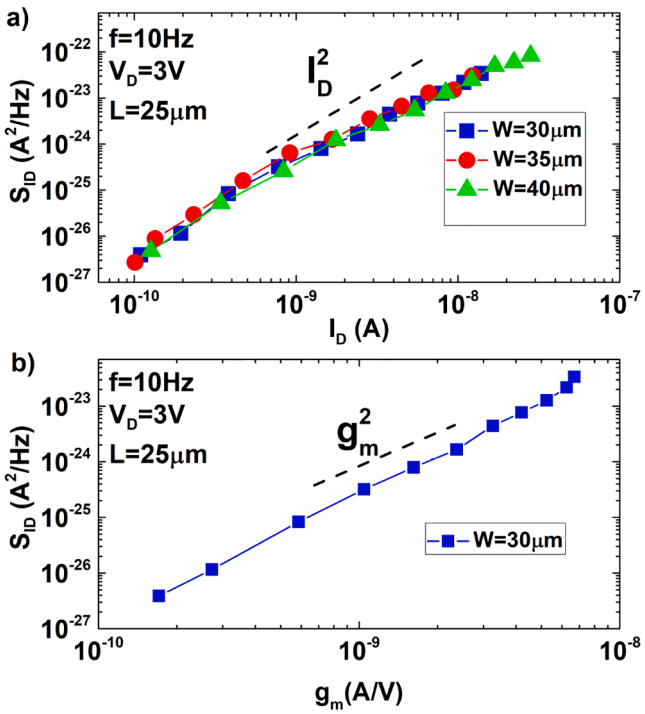

Fig. 8. Current noise spectral densities as a function of a) drain current and b) transconductance for different front-gate biases at f = 10Hz. Different channel widths are characterized in a) for devices with 25 μm channel length. V_S = 0 V, T = 300 K.

For the sake of comparison, normalized spectral noise density is shown in Fig. 7.b for devices with different physical dimensions. Narrower devices present higher noise levels in normalized spectrum representation. This increase is expected with device scaling (voltage flat band noise level scales with the factor 1/WL) and the possible contribution of high series and contact resistances to the total noise spectrum [40,41,39].

Additionally, Fig. 8.a shows the noise power spectral density as a function of the drain current. Curves follow a quadratic trend with the drain current, $S_{ID}(f) \propto I_D^2$. Fig. 8.b shows how the noise power spectral density also follows a quadratic trend with the transconductance (g_m) corroborating that the low frequency noise is a trap-related (carrier number fluctuations) and not a mobility related ($S_{ID} \propto I_D$) effect [42].

4. Conclusion

In this work, the performance and reliability of MoS_2 transistors have been studied. Back-gated transistors fabricated following a scalable chemical vapor deposition synthesis have demonstrated high current ratios and considerable contact resistance. The electrical characterization reveals the Schottky barrier formation suppressing the hole current due to Fermi level pinning. This pinning is probably caused by imperfections and defects. The reliability study demonstrates that defects also produce current hysteresis. Capacitance–voltage characterization shows frequency dispersion indicating the presence of both interface and border traps in the devices. Finally, the devices present a flicker noise characteristic which points to trapping/de-trapping phenomena influenced by the back-gate bias. These trapping phenomena induces a carrier number fluctuation which has more impact in narrower devices.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence

the work reported in this paper.

Acknowledgment

This project has received funding from the European Union's Horizon 2020 research and innovation programme under the Marie Skłodowska-Curie grant agreement No 895322, from the Spanish Government under Juan de la Cierva Formacion Grant No. FJC2018-038264-I. The Spanish Program (TEC2017-89800-R), ASCENT (EU Horizon 2020 GRANT 654384) and Science Foundation Ireland: INVEST (SFI-15/IA/3131) and AMBER (12/RC/2278-P2) are also thanked for financial support. Funding for open access charge: Universidad de Granada / CBUA.

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