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Review

On the Practical Evaluation of the Switching Loss in the Secondary Side Rectifiers of LLC Converters

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Abstract: The switching loss of the secondary side rectifiers in LLC resonant converters can have a noticeable impact on the overall efficiency of the complete power supply and constrain the upper limit of the optimum switching frequencies of the converter. Two are the main contributions to the switching loss in the secondary side rectifiers: on the one hand, the reverse recovery loss (Q_{rr}), most noticeably while operating above the series resonant frequency; and on the other hand, the output capacitance (C_{oss}) hysteresis loss, not previously reported elsewhere, but present in all the operating modes of the converter (under and above the series resonant frequency). In this paper, a new technique is proposed for the measurement of the switching losses in the rectifiers of the LLC and other isolated converters. Moreover, two new circuits are introduced for the isolation and measurement of the C_{oss} hysteresis loss, which can be applied to both high-voltage and low-voltage semiconductor devices. Finally, the analysis is experimentally demonstrated, characterizing the switching loss of the rectifiers in a 3 kW LLC converter (410 V input to 50 V output). Furthermore, the C_{oss} hysteresis loss of several high-voltage and low-voltage devices is experimentally verified in the newly proposed measurement circuits.

Keywords: C_{oss} hysteresis; isolated converters; LLC; switching loss; soft switching

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1. Introduction

A high-power off-line Power Supply Unit (PSU) normally comprises at least two stages: a front-end Power Factor Correction (PFC) and a back-end DCDC converter that provides isolation and a tight regulated output [1,2]. The total efficiency of the complete PSU is the result of multiplying the efficiency of each of the separate stages. Therefore, the total efficiency is always necessarily lower than the lowest of the individual efficiencies. This imposes very challenging requirements for the design of converters for the increasingly rising efficiency standards.

The main contributions to losses in the DCDC converter include the conduction, the auxiliary, the switching, the driving, and the core loss [3,4]. Most of these contributions to losses are, in some manner, frequency dependent, i.e., while the driving and the switching losses increase proportionally to the frequency, the core losses decrease proportionally to it (within the usable range of the specific material and considering a fixed geometry and number of turns, and therefore a decreasing magnitude of the magnetic field). The analysis of the conduction losses can be more complicated (depending on the construction of the conductors and the magnetics), but in all cases have a tendency to increase at the higher frequencies. Therefore, for every converter design there is an optimum switching frequency at which the overall sum of losses is at its minimum and the maximum efficiency is achieved.

Resonant and quasi-resonant converters aim to diminish or completely get rid of the switching loss contribution, i.e., soft-switching the power semiconductor devices. This can be accomplished by turning on at zero volts the so-called Zero Voltage Switching (ZVS) and turning off at zero current the so-called Zero Current Switching (ZCS) [5]. Among the resonant and quasi-resonant converters, the LLC has become very popular because of its simple circuitry (Figure 1) and the very high efficiencies it can achieve [6,7]. In the LLC the primary side devices are switched on in ZVS and can be switched off in ZCS, while the secondary side devices are switched on and off in ZVS, although they commutate with the transformer.

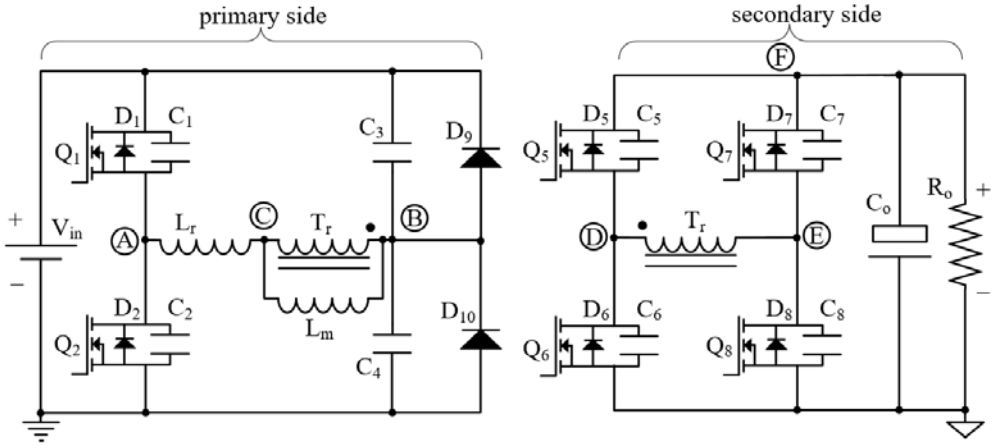

Figure 1. Half-bridge LLC DCDC converter with full-bridge rectification.

However, it has been reported that in the LLC (and other resonant converters), although the high-voltage (HV) primary side devices are soft-switched, their switching loss does not completely disappear [8]. The phenomenon can be interpreted as an equivalent series resistance (R_{oss}) appearing in series to the output capacitance of the devices (C_{oss}) during the resonant transitions [9–16]. However, there are no similar reports about the soft-switching loss contribution of the secondary side low-voltage (LV) rectifiers, even though the most mature technology for the LV secondary side rectifiers is the Silicon (Si) Trench MOSFET with shield-plate [17–21], and it is known that in their construction a series resistance appears with the output capacitance [22–24].

For the construction of a complete PSU targeting 97.5% peak efficiency, an LLC DCDC converter with the specifications in Table 1 was designed and built [25]. However, it was observed that the efficiency was unexpectedly decreasing while the series resonant frequency of the design was increasing (Figure 2). The origin of the unexpected contribution to losses was found to be the secondary side rectifiers, which was experimentally demonstrated with a new proposed technique for the characterization of the switching loss in the rectifiers of isolated converters. Moreover, the principle of the measurement technique was applied to a new testing circuit for the isolation and measurement of the C_{oss} hysteresis loss (excluding Q_{rr} contribution), which can be used for both HV and LV devices.

Table 1. Key specifications of the prototype.

Parameter	Value
Nominal input voltage	410 V
Input voltage range	320–430 V
Nominal output voltage	50 V
Maximum output power	3000 W
Target peak efficiency	98.5%
Switching frequency	70–150 kHz
Magnetizing inductance (L_m)	65 µH
Resonant capacitor (C_r)	480 nF
Turn ratio of the transformer	16:4

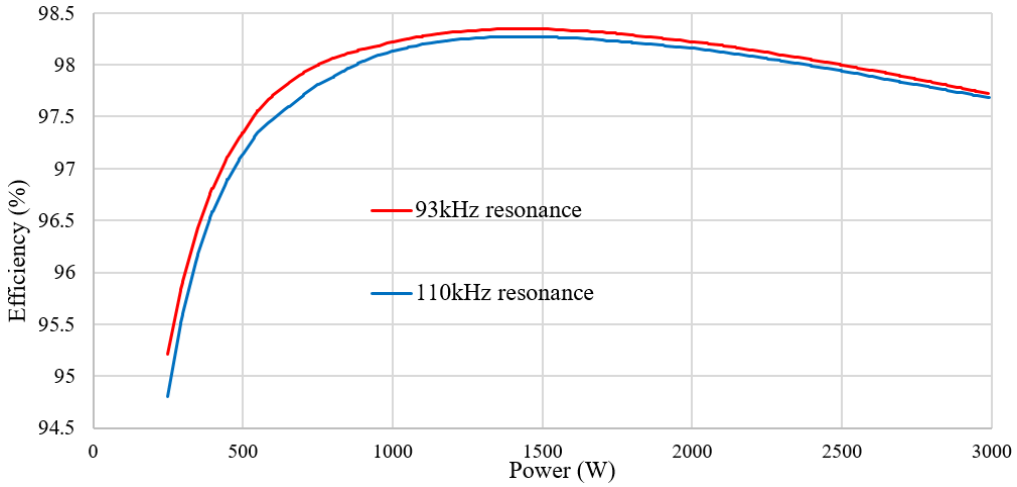

Figure 2. Measured efficiency of the 3 kW half-bridge LLC at the nominal input and output voltages and with two different resonant tank configurations: L_r = 6.1 µH (93 kHz) and L_r = 4.36 µH (110 kHz).

The rest of this document is organized as follows. In Section 2, the commutation of the secondary side rectifiers in LLC converters is analyzed and a new technique for the characterization of the switching loss (Q_{rr} plus C_{oss} hysteresis) within the application is proposed. In Section 3, two new circuits for the isolation of the C_{oss} hysteresis loss are introduced and analyzed. The study is corroborated by the experimental results in Section 4 where the measurement techniques are applied to LV and to HV semiconductor devices. Finally, Section 5 presents a summary of conclusions of this work.

2. Analysis of the Commutation of the Rectifiers

The rectifiers in the LLC resonant converter can be switched on and off in ZVS. However, they are commutated by the transformer, with the *di/dt* being only limited by the series resonant inductor (L_r), the leakage of the transformer (L_{lkg}) and other stray inductances. In this section, the commutation process is analyzed and a new technique is proposed for measuring Q_{oss}, Q_{rr} and the related switching loss.

2.1. Charge and Discharge of C_{oss}

Figure 3 shows the main driving signals and waveforms in the LLC resonant converter during the commutation of the secondary side rectifiers. In this example, the converter is operating above the series resonant frequency, sometimes referred to as continuous conduction mode (CCM). Before the analysis, some assumptions are made: (1) all diodes and switches are ideal; (2) all switches are MOSFETs with intrinsic anti-parallel body diodes; (3) all capacitors and inductors are ideal; (4) $C_1 = C_2$, $C_5 = C_6 = C_7 = C_8$; (5) $(C_3 + C_4) >> (C_1 + C_2)$; (6) L_{lkg} = zero. In the following paragraphs, we analyze the

operation principles of the rectifier's commutation. It should be noted that the analyzed modes do not necessarily align with the rising of falling edges of the gate driving signals.

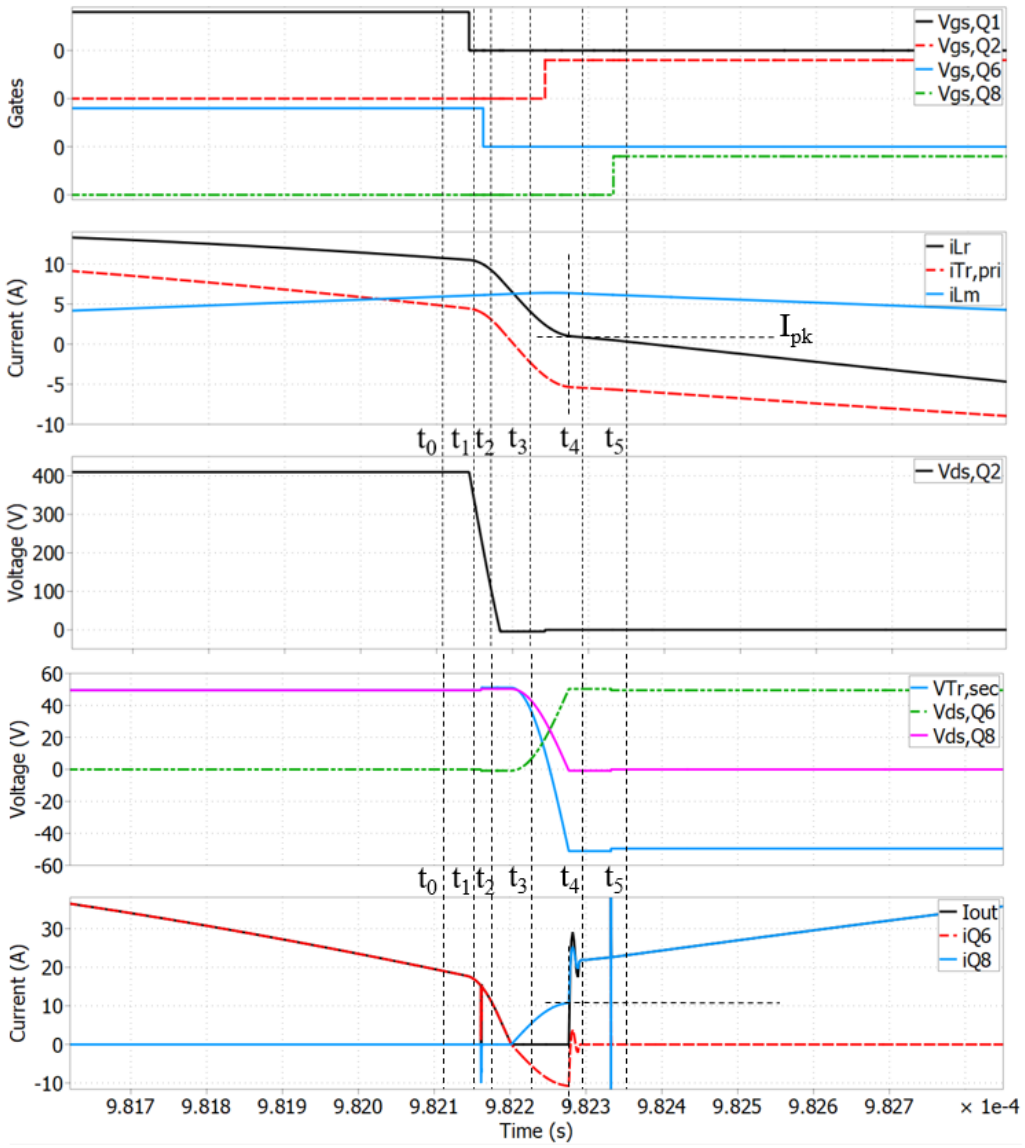

Figure 3. Main waveforms in the half-bridge LLC during the commutation of the secondary side rectifiers.

1. Mode 1[t_0] (Figure 4a)

The primary high-side device Q_1 is on and its channel is conducting. The current through L_r (iL_r) flows towards the resonant capacitor C_r (C_3 plus C_4), which is therefore partially charged and discharged every period. The current iL_r comprises the transformer-reflected load current ($iT_{r,pri}$) and the magnetizing current (iL_m), which both flow in the same direction at this point. Because of that, at higher loads and/or at lower frequencies the voltage excursion in C_r increases (also depending on the capacitor size).

In the secondary side of the converter, Q_6 and Q_7 are on and their channel is conducting the transformer secondary current ($iT_{r,sec}$) that equals the output current (I_{out}) at this point.

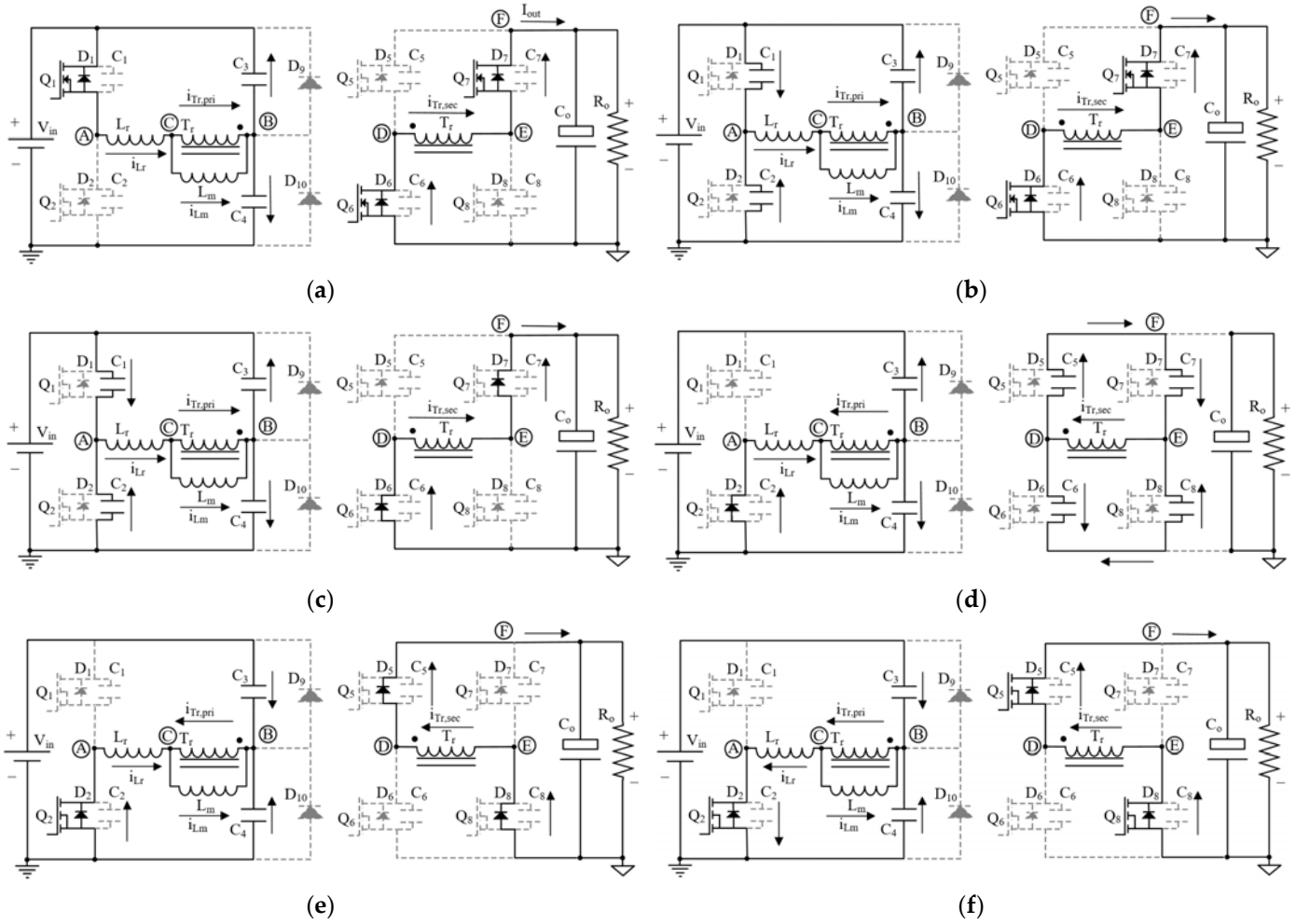

Figure 4. Main operation modes of the half-bridge LLC converter during the commutation of the rectifiers: (**a**) [t_0]; (**b**) [t_1]; (**c**) [t_2]; (**d**) [t_3]; (**e**) [t_4]; (**f**) [t_5].

2. Mode 2[t_1] (Figure 4b)

Both primary side devices are off and their capacitances C_1 and C_2 are being respectively charged and discharged by iL_r, which continues to flow towards C_r, but starts to decrease with a slope that depends on the size of the capacitors C_1 and C_2 (natural resonance with L_r), and the voltage of C_r and T_r (i.e., the voltage effectively applied over L_r). Therefore, at higher loads, the current slope increases.

3. Mode 3[t_2] (Figure 4c)

Q_6 and Q_7 are turned off, and their intrinsic body diodes continue to conduct the secondary side current ($iT_{r,sec}$). A transient drop in the current of iQ_6 can be observed in Figure 3 due to the charge of C_6 to $-V_f$ and C_8 to V_{out} plus V_f, corresponding to the forward voltage of their intrinsic antiparallel diode. It should be noted that in this example, the full transition of C_1 and C_2 from the upper voltage rail (V_{in}) to the lower voltage rail (GND) happens before the secondary side starts to commutate because C_1 and C_2 are relatively small size capacitors, and the turn-off current is relatively high. However, in other cases, the voltage transition of C_1 and C_2 can also overlap the commutation of the secondary side rectifiers [26].

4. Mode 4[t_3] (Figure 4d)

The voltage transition of C_1 and C_2 reaches under the GND rail and the intrinsic body D_2 continues conducting the resonant current (iL_r). The secondary side devices are all off.

The output capacitances of Q_6 and Q_7 are being charged while the output capacitances of Q_5 and Q_8 are being discharged. It should be noted that during the charge of C_6 and C_7 and the discharge of C_5 and C_8, no current is being delivered to the output.

5. Mode 5[t_4] (Figure 4e)

The primary low-side device Q_2 is on and the resonant current iL_r flows mostly through its channel (although some current can be shared with its antiparallel diode). The diodes of the secondary side devices D_5 and D_8 conduct the secondary side current $iT_{r,sec}$ which is again equal to the output current I_{out}.

The peak current of the charge-discharge (I_{pk}) depends on the size of the capacitances C_5–C_8, the size of the series resonant inductor L_r (natural resonance), and the voltage excursion of the primary side resonant capacitor C_r (i.e., effectively higher voltage applied to L_r). Therefore, at higher loads I_{pk} and the *dv/dt* of the secondary side rectifiers increases.

6. Mode 6[t_5] (Figure 4f)

Q_5 and Q_8 are on and their channels are conducting the transformer secondary side current ($iT_{r,sec}$). The primary reflected load current ($iT_{r,pri}$) is larger than the magnetizing current (iL_m) and of the opposite direction. Therefore, iL_r flows at this point towards Q_2.

It follows from the previous analysis that due to the charge and discharge of the secondary side rectifiers' capacitance, the output current does not start at zero but at I_{pk}. This has several consequences:

- The natural resonance of L_r and C_r does not start at zero degrees, but it is shifted by an angle which depends on the ratio of I_{pk} with regard to the amplitude of the series resonance current (AI_{out}) (1). However, AI_{out} decreases in turn because of the I_{pk} shift, therefore effectively reducing the *rms* currents through the converter. Therefore, discontinuous conduction mode (DCM) operation can be observed above the series resonant frequency (Figure 5).

$$\varnothing = \arcsin\left(\frac{I_{pk}}{AI_{out}}\right) \quad (1)$$

- During the charge and discharge of the rectifiers' capacitance no current is being delivered to the output (so-called dead time), effectively increasing the output *rms* current. This effect is further described in [27].
- The two effects above combine at a different level depending of the converter's design. Therefore, extending the analysis in [27], which does not include the first effect above, within a certain range of sizes of the rectifier's capacitance the *rms* currents through the converter can decrease and the overall efficiency can actually improve.
- Finally, due to the charge-discharge current, the converter may deliver more energy than necessary at very light loads, effectively increasing its large signal gain and limiting the regulation range [28,29].

Figures 5 and 6 show two scope captures of the LLC converter built with the specifications in Table 1 and with a series resonant frequency approximately equal to 93 kHz. The shift in the resonance phase can be better appreciated in Figure 5 where, although the converter is operating above resonance, the secondary side current becomes zero before the end of the half of the period (iL_r crosses iL_m). On the other hand, the improvement in the *rms* currents can be better appreciated in Figure 6 where the current waveforms are closer to a trapezoid than to a pure sinusoidal.

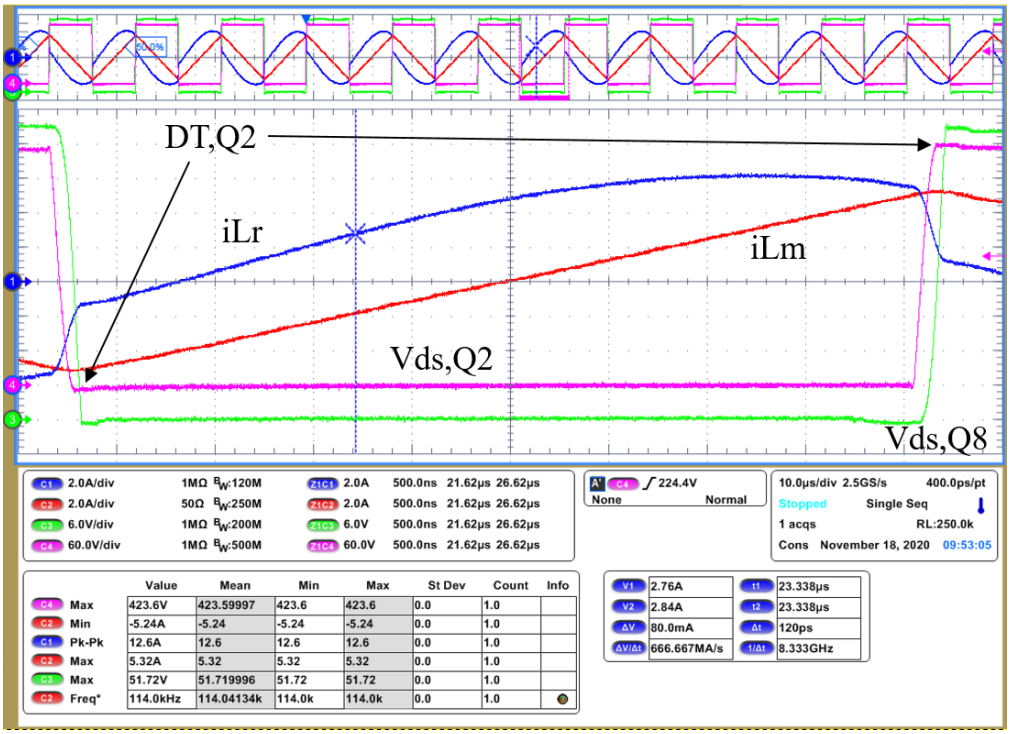

Figure 5. Main waveforms of the 3 kW half-bridge LLC at 10 A of load. SRs dead time (DT).

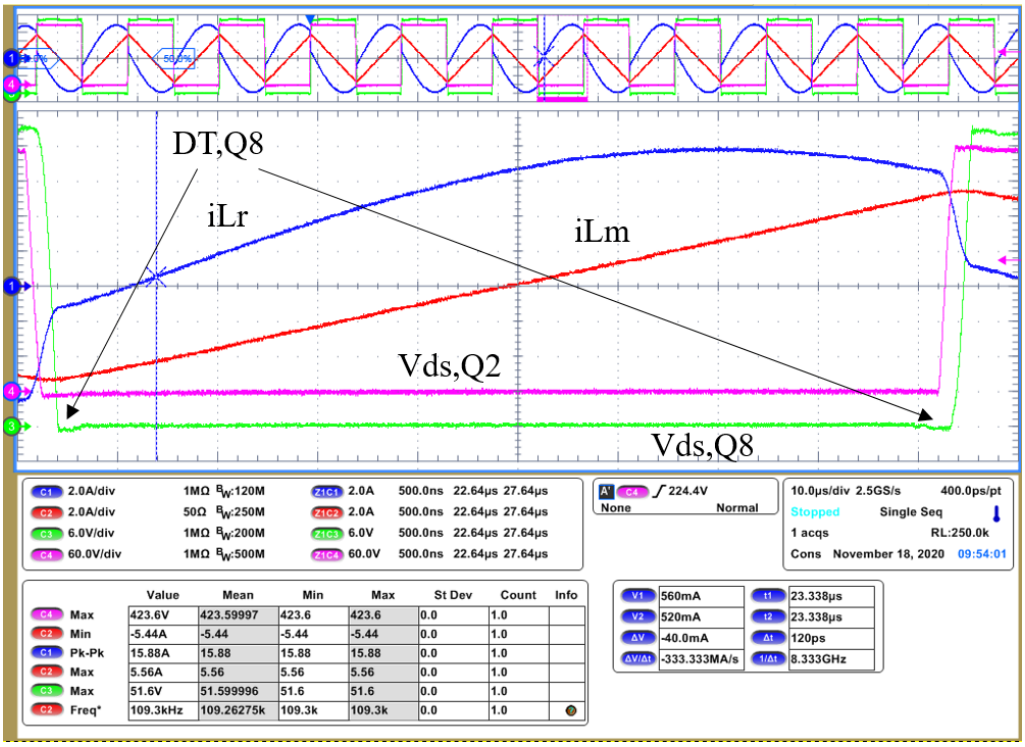

Figure 6. Main waveforms of the 3 kW half-bridge LLC at 20 A of load.

2.2. Measurement of Q_{oss}, Q_{rr}, and Switching Loss

During the commutation of the secondary side rectifiers, it is possible to measure, directly in the application, the stored charge (Q_{oss}), the reverse recovery charge (Q_{rr}), the stored energy (E_{oss}), and the total switching loss (E_{loss}) of the devices.

If the magnetizing inductance is realized with a discrete external inductor (L_m) and the main transformer is near ideal (its magnetizing inductance is much bigger than the

external L_m) the total transferred charge, which includes Q_{oss} and Q_{rr}, can be calculated from the measurement of iL_m and iL_r by means of (2). The integral of the current shall be computed from the start of the commutation (t_a) until the point where the antiparallel body diodes start to conduct (t_c). The start of the commutation corresponds to the cross of iL_r with iL_m (Figure 7), whereas the end of the commutation can be estimated at the point where $vT_{r,sec}$ reaches the output voltage plus the diode forward drop (3).

$$Q_{oss} + Q_{rr} = \Delta Q = \int_{t_a}^{t_c} (iL_m - iL_r) dt \tag{2}$$

$$\begin{cases} iL_m(t_a) - iL_r(t_a) = 0 \\ vT_{r,sec}(t_a) = (v_{out} + v_f) \\ vT_{r,sec}(t_c) = -(v_{out} + v_f) \end{cases} \tag{3}$$

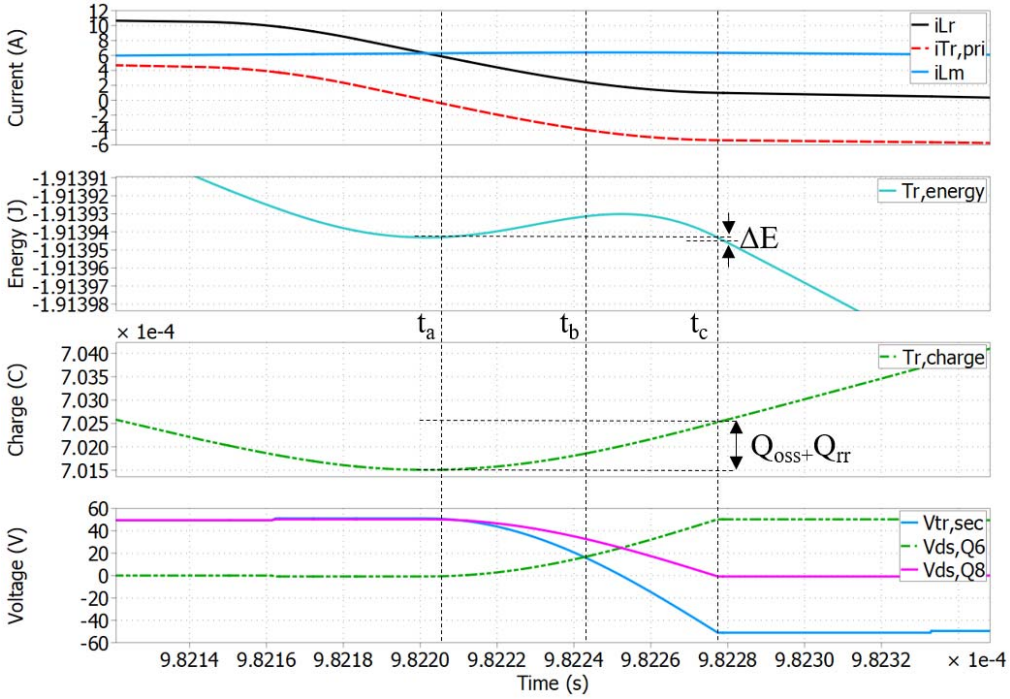

Figure 7. Main waveforms in the half-bridge LLC during the commutation of the rectifiers. Measured charge and energy during the commutation.

The switching loss can be calculated by computing the balance of energy that flows through the transformer during the commutation. From the point of view of the transformer, from t_a to t_b energy is recovered during the charge and discharge of C_5–C_8. Inversely, from t_b to t_c energy is delivered (Figure 7). The point t_b corresponds to the zero crossing of $vT_{r,sec}$ (4), where all the capacitors C_5 to C_8 have an equal voltage.

Notice that because no energy is being delivered to the output during the commutation of the rectifiers, if there were no losses, the total energy at the start and at the end of the transition shall be equal. However, if there is a difference between the measured energies at the start and at the end, it necessarily corresponds to losses, which can be attributed to the switching loss contribution of the rectifiers, and calculated with (5) and (6).

$$vT_{r,sec}(t_b) = 0 \tag{4}$$

$$\text{if } Q_{rr} = 0 \xrightarrow{\text{yields}} \begin{cases} \Delta E_1 = \left| \int_{t_a}^{t_b} (iL_m - iL_r) \cdot vT_{r,sec} dt \right| \\ \Delta E_2 = \left| \int_{t_b}^{t_c} (iL_m - iL_r) \cdot vT_{r,sec} dt \right| \\ \Delta E_2 \geq \Delta E_1 \end{cases} \tag{5}$$

$$E_{loss,1} = \Delta E_2 - \Delta E_1 = \Delta E \tag{6}$$

However, due to the effect of the reverse recovery charges (Q_{rr}) the apparent energy balance could be smaller than the actual losses, even zero or negative (7). Therefore, the correct estimation of the total loss, including the Q_{rr} contribution, requires a measurement that can exclude its effect, even more for semiconductor devices where the Q_{rr} can be relatively large [30] (e.g., HV SJ Si MOSFETs [31] or LV Si shield-plate FETs [22]). For this purpose, a novel measurement setup is introduced in the next sections of this manuscript. Thereafter the C_{oss} hysteresis loss ($E_{loss,1}$) can be substituted in (8) and (9) to subsequently obtain the Q_{rr} component.

$$\text{if } Q_{rr} \neq 0 \xrightarrow{\text{yields}} \begin{cases} \Delta E_3 = \left| \int_{t_a}^{t_b} (iL_m - iL_r) \cdot vT_{r,sec} dt \right| \\ \Delta E_4 = \left| \int_{t_b}^{t_c} (iL_m - iL_r) \cdot vT_{r,sec} dt \right| \\ \Delta E_3 > \Delta E_1 \;\&\; \Delta E_4 \geq \Delta E_2 \end{cases} \tag{7}$$

$$E_{loss,2} = (\Delta E_3 - \Delta E_1) + (\Delta E_4 - \Delta E_2) + (\Delta E_2 - \Delta E_1) = \Delta E_3 + \Delta E_4 - 2\Delta E_1 \tag{8}$$

$$(E_{loss,2} > E_{loss,1}) \;\&\; (E_{loss,2} > \Delta E) \tag{9}$$

3. Testing Setup for the Isolation of C_{oss} Loss

The principles of operation during the commutation of the rectifying devices in the LLC converter are utilized in two novel measurement circuits that isolate the loss due to the charge and discharge of the C_{oss} and exclude other contributions, i.e., Q_{rr} and conduction losses. These two circuits are introduced and analyzed in this section.

3.1. Back-To-Back Devices under Test

The first proposed circuit is represented in Figure 8, with its main differences to the original half-bridge LLC circuit in Figure 1 being that the output capacitance and the load of the converter have been removed, and the full-bridge rectification has been replaced by a back-to-back configuration of the Devices Under Test (DUTs).

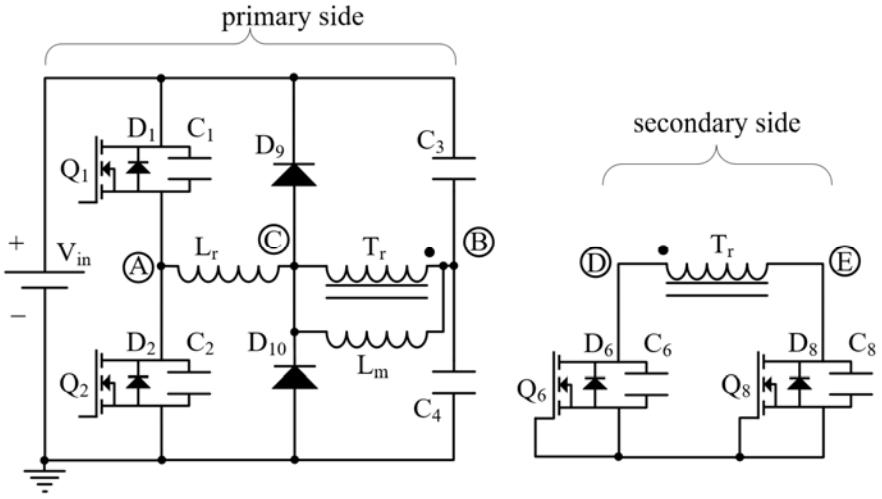

Figure 8. Proposed circuit configuration for the measurement of the C_{oss} hysteresis loss.

Placing the DUTs in a back-to-back configuration ensures that their intrinsic body diodes or their channels do not conduct. As a result, we can exclude the Q_{rr} in the computation of the switching loss which could mask the soft-switching losses, as was analyzed in the previous section. More importantly, the proposed circuit can be used for testing devices of very distinct voltages by only adapting the transformer turn ratio and/or the input voltage V_{in}. Whereas the same purpose could be achieved with the full-bridge

configuration in Figure 1, it is convenient to reduce the number of required DUTs for the test.

Figure 9 shows the main driving signals and waveforms of the proposed circuit. Before the analysis some assumptions are made: (1) all diodes and switches are ideal; (2) all switches are MOSFETs with intrinsic antiparallel body diodes; (3) all capacitors and inductors are ideal; (4) $C_1 = C_2$, $C_5 = C_6 = C_7 = C_8$; (5) $(C_3 + C_4) >> (C_1 + C_2)$; (6) $L_m = \infty$; (7) the switching frequency (F_{sw}) is greater than the series resonant frequency ($F_r = \frac{1}{2\pi\sqrt{L_r(C_3+C_4)}}$); (8) the duty cycle is 50%. In the following paragraphs, we analyze its operation principles.

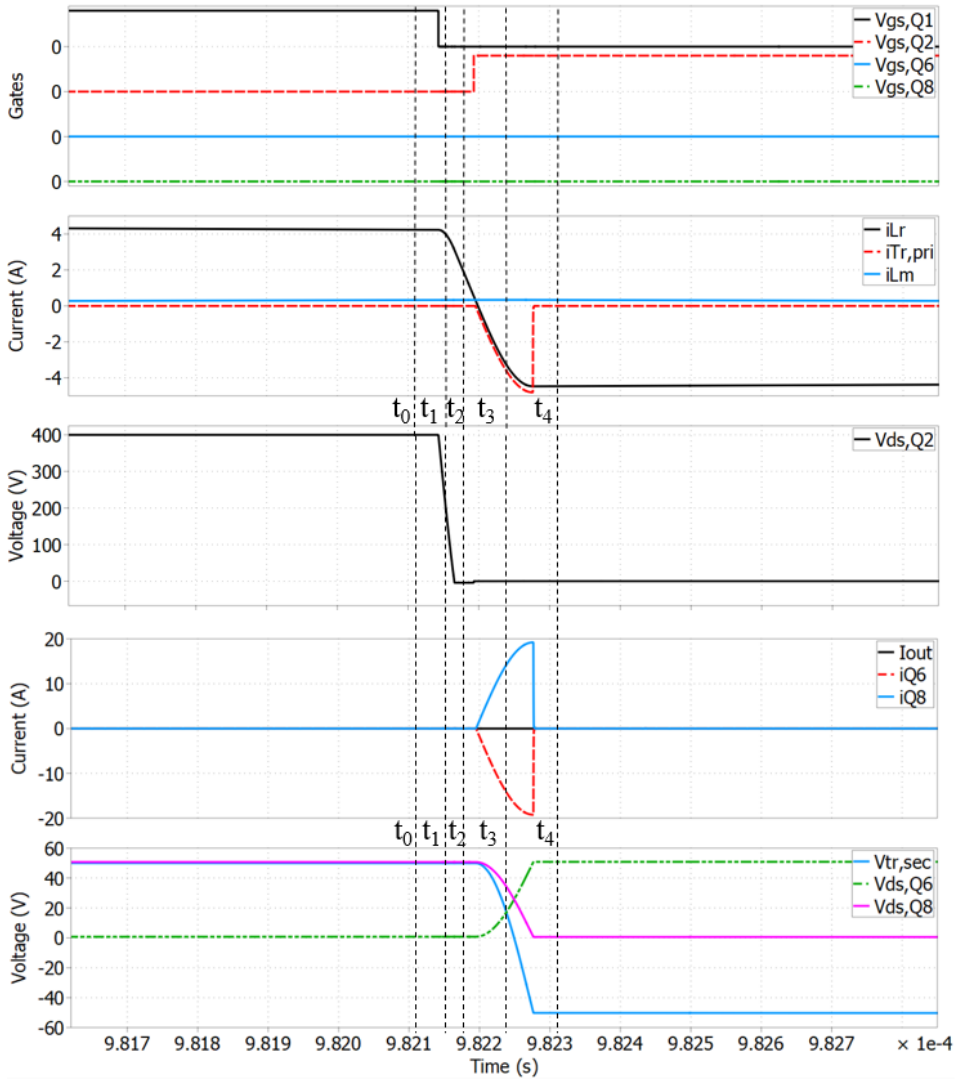

Figure 9. Main waveforms of the proposed circuit for the measurement of the C_{oss} hysteresis loss.

1. Mode 1[t_0] (Figure 10a)

The primary high side device Q_1 is on and its channel is conducting. The current through L_r (iL_r) freewheels through one of the clamping diodes (D_9). Since there is no current through the transformer ($iT_{r,pri}$ = zero), only the magnetizing current iL_m flows towards C_r (C_3 plus C_4). We can consider L_m to be large enough that we can neglect its contribution.

In the secondary side of the converter, the voltage of the transformer $VT_{r,sec}$ is clamped thanks to the primary side diodes (D_9 and D_{10}), which holds true as far as the primary

current continues to freewheel through one of them. The switching frequency of the circuit is adjusted to ensure that.

2. Mode 2[t_1] (Figure 10b)

Both primary side devices are off and their capacitances, C_1 and C_2, are being respectively charged and discharged by iL_r, which continues to freewheel through D_9.

3. Mode 3[t_2] (Figure 10c)

The voltage transition of the primary side devices ends and the intrinsic body diode D_2 continues to conduct the freewheeling current. Notice that depending on the size of the capacitances, the transition of the primary side devices and the transition of the secondary side devices can overlap. Notice also that it might be possible that the primary side devices do not reach full ZVS turn-on. However, none of those phenomena have an impact on the proposed measurement technique of the secondary side switching losses.

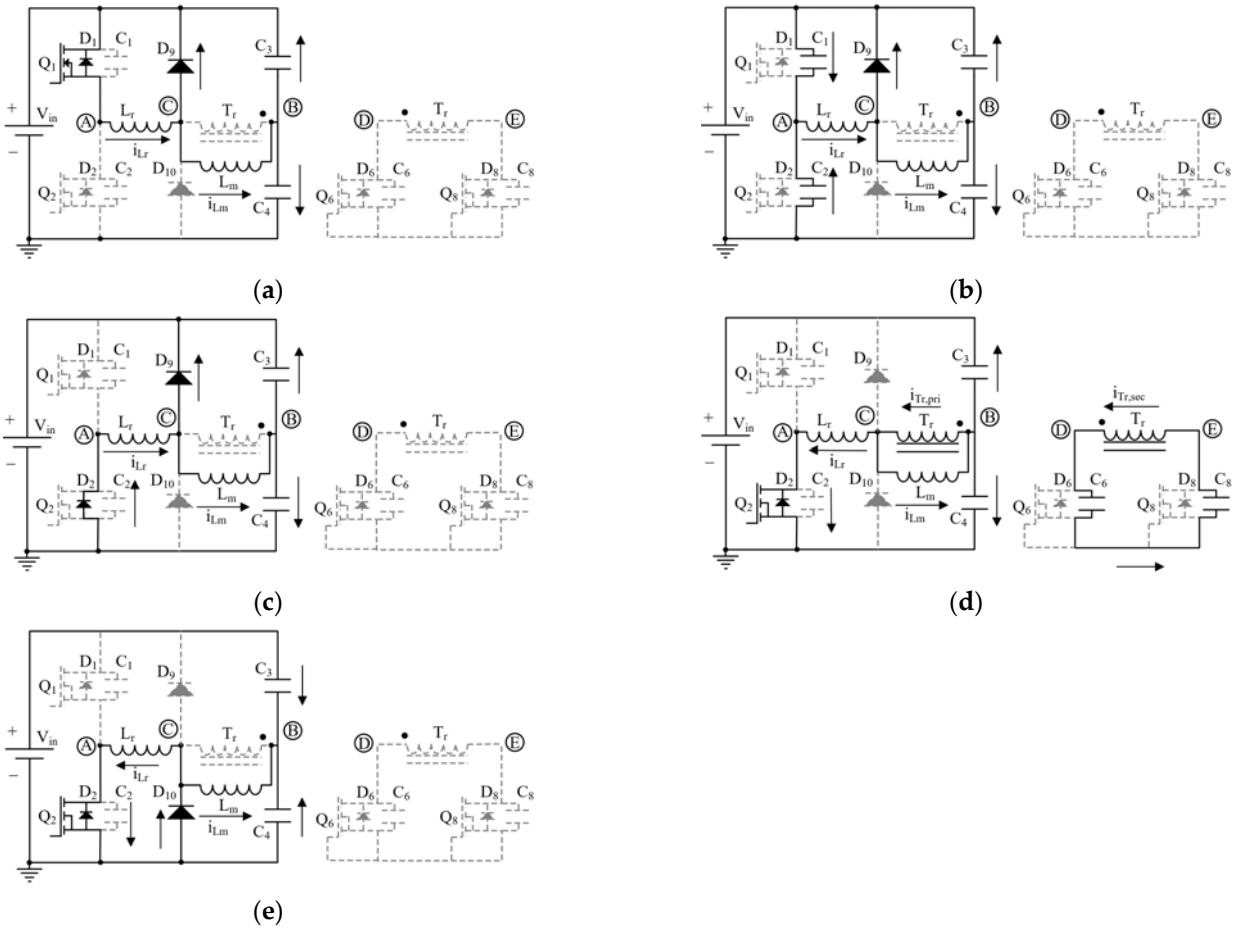

Figure 10. Main operation modes for the proposed circuit for the measurement of the C_{oss} hysteresis: (**a**) [t0]; (**b**) [t1]; (**c**) [t2]; (**d**) [t3]; (**e**) [t4].

4. Mode 4[t_3] (Figure 10d)

Q_2 is on and its channel is conducting $iT_{r,pri}$ minus iL_m. At the same time, the capacitance of Q_8 is being discharged while the capacitance of Q_6 is being charged. We can observe that Q_6 and Q_8 form a closed loop and the charge and energy is transferred back and forth from one to the other. Therefore, the proposed circuit works best when both devices are equal ($C_6 = C_8$) so all of their charge can be moved during the transition.

5. Mode 5[t_4] (Figure 10e)

Ideally, at this point no current should circulate through the transformer or the capacitances of the DUTs. However, due to non-idealities of the circuit, after the charge of C_6 and the discharge of C_8, the leakage of the transformer and other stray inductances cause a resonance and a subsequent overshoot in the secondary side devices (Figure 11).

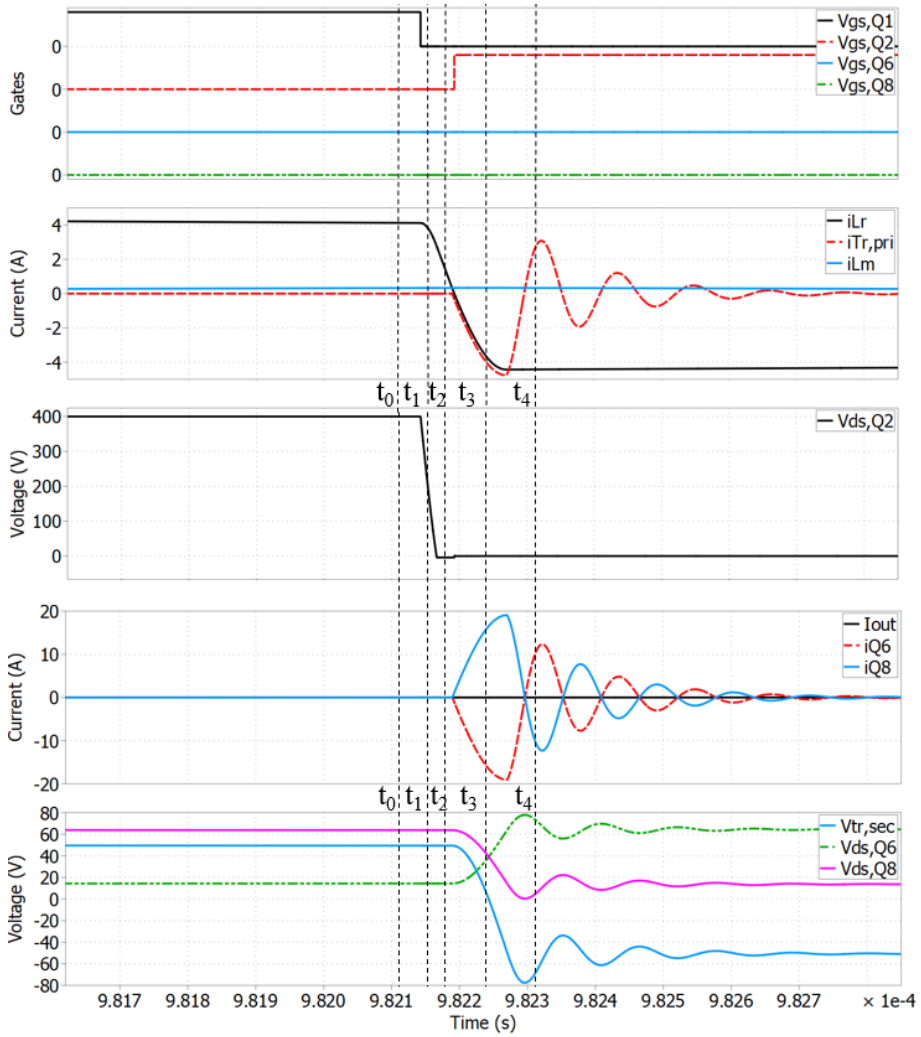

Figure 11. Main waveforms in the proposed circuit for the measurement of the C_{oss} hysteresis loss including the effect of L_{lkg} and stray inductances.

It should be noted that the unwanted resonance and overshoot does not interfere with the proposed measurement technique. As was previously analyzed, Q_{oss} and the energy have to be computed only between t_a and t_c. However, the overshoot may limit the measurement range when the peak voltage comes closer to the breakdown limit of the DUTs, e.g., in the capture in Figure 12, the overshoot reaches a peak of 372 V while measuring a charge-discharge of 200 V (i.e., 172 V of overshoot). Therefore, it is desirable to further improve the circuit and to reduce the effect of the stray inductances to a minimum.

The main sources of error are the inaccuracy and uncertainty of the voltage and current measurements and their relative shift (skew). It is essential to evaluate the influence of such parameters on the results. The sensitivity of the results for several of the DUTs to the variation of the gain in the voltage measurement (ΔV), the gain in the current measurement (ΔI), and the skew (Δskew) is shown in Figure 13, which indicates that the most sensitive parameter is the ΔV (unless for DUT_3 in the graph). On the other hand, the current gain and the skew between the signals presented relatively minor sensitivity values.

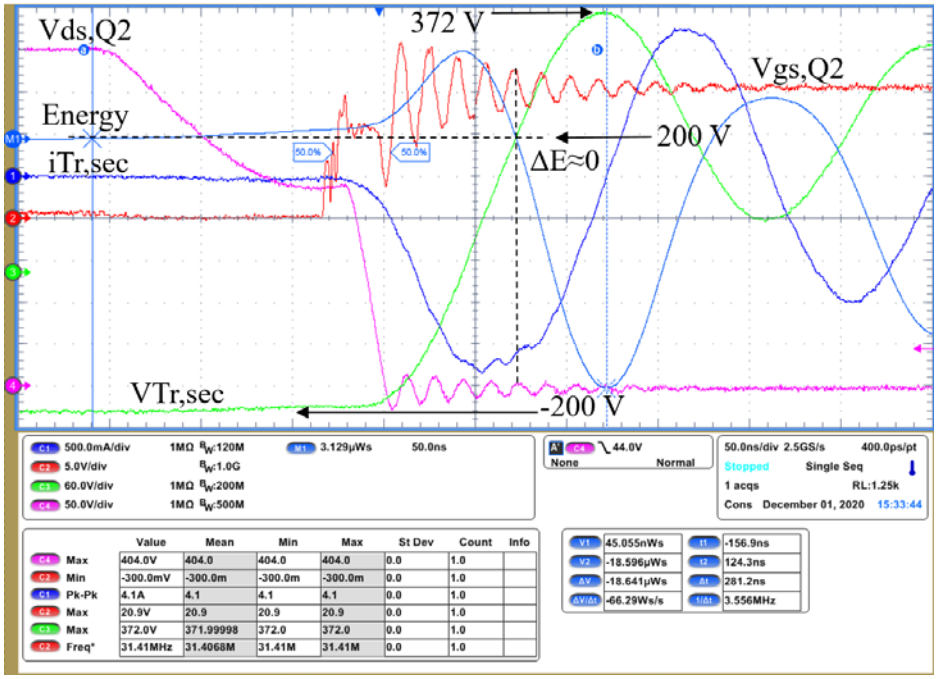

Figure 12. Measurement of the hysteresis loss of a high-quality 330 pF ceramic capacitor. Near zero energy is lost during the charge and discharge.

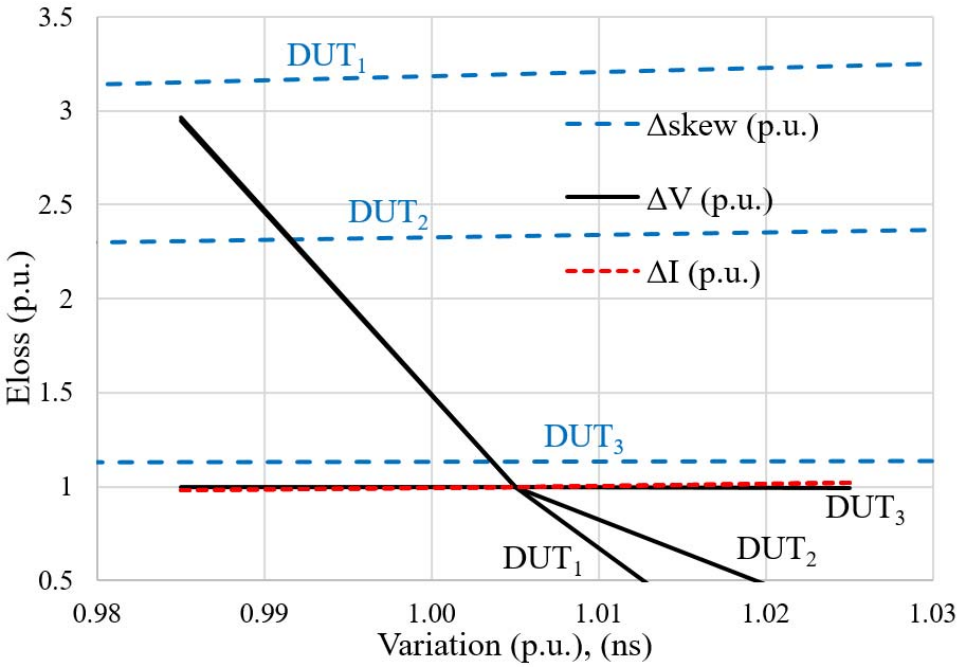

Figure 13. Sensitivity analysis of the C_{oss} hysteresis loss (E_{loss}) with respect to the varying parameters: skew (Δskew), voltage measurement gain (ΔV), and current measurement gain (ΔI).

It is worth highlighting that the LC resonance between the stray inductances and the capacitance of the DUTs at the end of the charge transition, e.g., in the measurement of a ceramic capacitor in Figure 12, can be used to adjust the skew between the current and voltage signals (i.e., the zero crossing of the current should match the peak amplitude of the voltage oscillation), therefore improving the accuracy of the proposed method. On the other hand, a possible offset in the measurement can be corrected in the post-processing of the data.

3.2. Improved Back-To-Back Configuration

The proposed measurement circuit in Figure 8 is further improved by moving the clamping diodes to the secondary side of the transformer (Figure 14). In this new configuration, the transformer ratio needs to be 1/2 (e.g., 8:16), for the clamping diodes to freewheel the current and clamp the DUTs voltage at the input supply rails. Thanks to this configuration, the current through the leakage of the transformer is also freewheeled through the clamping diodes. Moreover, other stray inductances can be reduced, placing the diodes as close as possible to the DUTs.

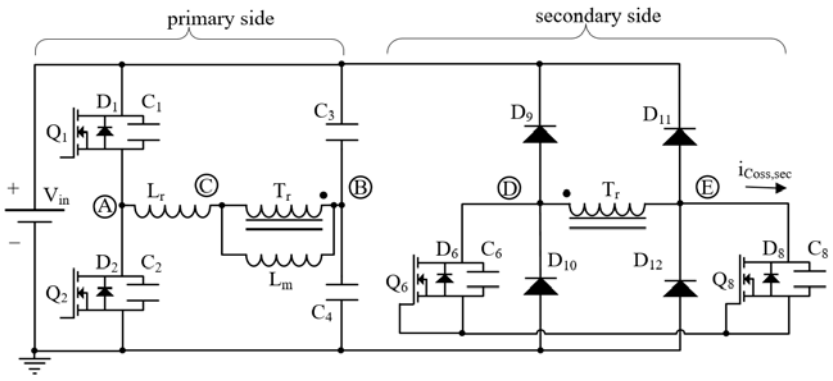

Figure 14. Alternative, improved circuit for the measurement of the hysteresis loss in C_{oss}.

The working principles of the circuit in Figure 14 are equal to the working principles of the circuit in Figure 8. It is only required that the transformer current measurement is done between one of the DUTs and its clamping diodes ($iC_{oss,sec}$), to exclude from the measurement in this manner the freewheeling current and the clamping diode capacitances.

In Figure 15, a 650 V SiC MOSFET is measured in the improved circuit configuration, charging and discharging 400 V while the peak of the overshoot only reaches 466 V (i.e., 66 V overshoot).

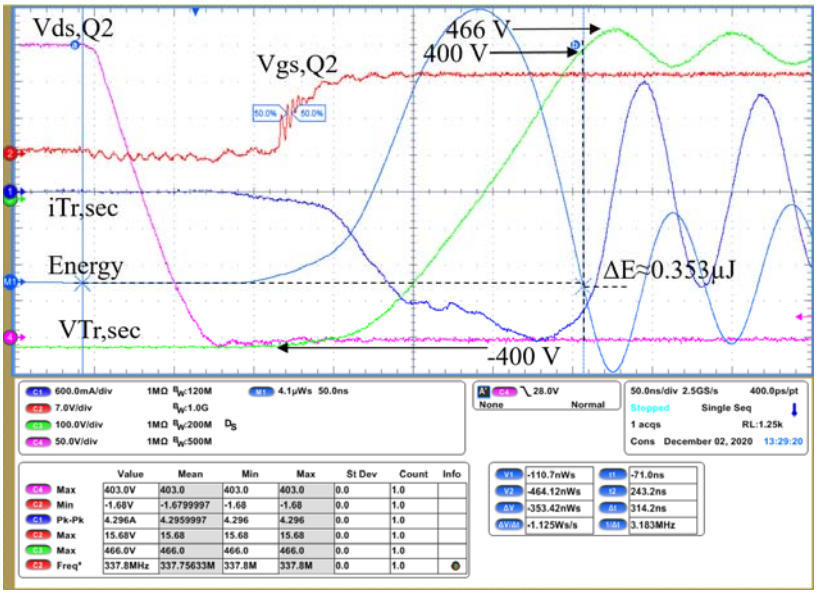

Figure 15. Measurement of the hysteresis loss of IMW65R027M1H. Approximately 0.35 µJ are lost during the discharge and charge from 400 V to zero V and from zero V to 400 V.

4. Experimental

The 3300 W LLC DCDC converter in [32], whose main specifications are listed Table 1, was modified to demonstrate the measurement techniques proposed in this work. The SRs

in place during the experiments were a total of twenty-four NTMFS08N003C, six devices in parallel per position in the secondary side full-bridge. The main experimental results are summarized in this section.

4.1. Low Voltage Rectifiers C_{oss} Loss

The secondary side voltage $vT_{r,sec}$ and the primary side currents iL_r and iL_m were measured at different points of load, from 10 A to 40 A, and in two different operation modes: under resonance (400 V input and 50 V output) and above resonance (410 V input and 50 V output). The measurements of the voltage, the current, the integral of the charge and the integral of the energy are plotted in Figures 16 and 17 for the operation under resonance, and Figures 18 and 19 for the operation above resonance.

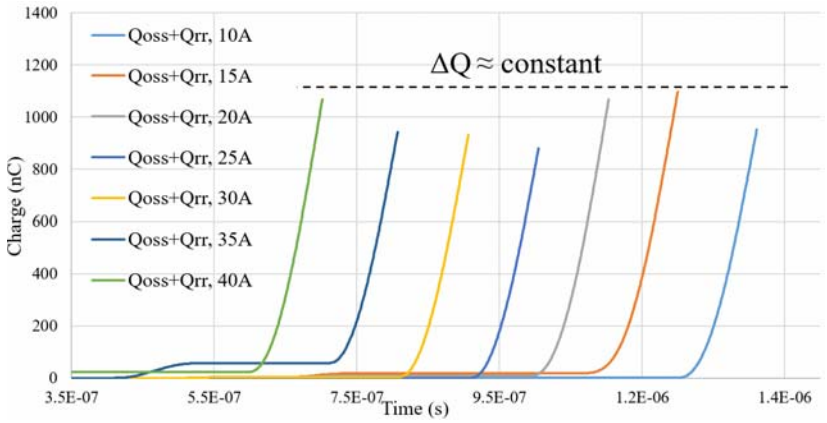

Figure 16. Measured transferred charge in the secondary side of the 3 kW half-bridge LLC converter during the commutation of the rectifiers. DCM operation.

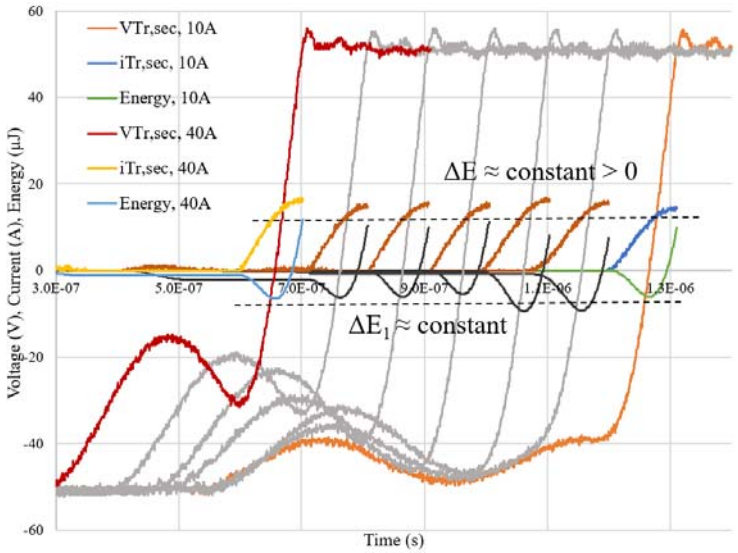

Figure 17. Measured transformer voltage and current in the secondary side of the 3 kW half-bridge LLC converter and the calculated accumulated energy during the commutation of the rectifiers. A positive offset in the energy indicates a loss. DCM operation.

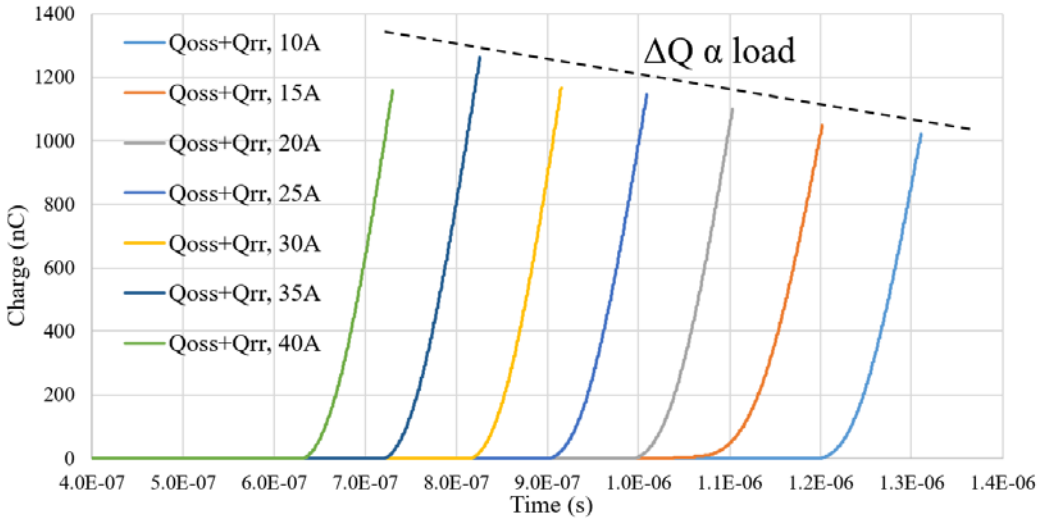

Figure 18. Measured transferred charge in the secondary side of the 3 kW half-bridge LLC converter during the commutation of the rectifiers. CCM operation.

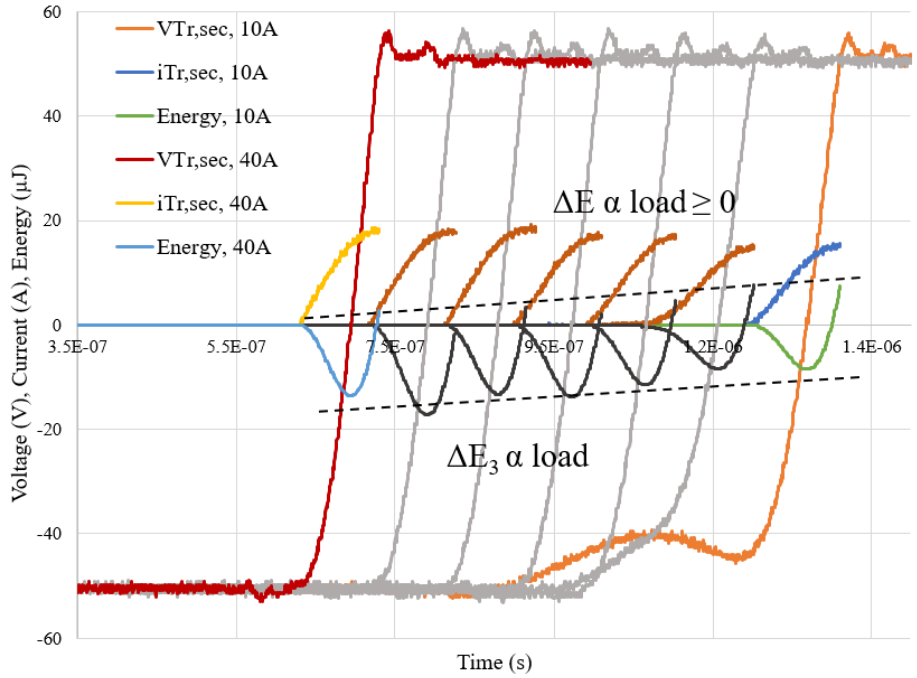

Figure 19. Measured transformer voltage and current in the secondary side of the 3 kW half-bridge LLC converter and the calculated accumulated energy during the commutation of the rectifiers. A positive offset indicates a loss. CCM operation.

In the operation under resonance, sometimes referred to as DCM, a consistent ΔE around 8 μJ (Figure 17) and a consistent Q_{oss} around 950 nC (Figure 16) can be observed. However, in the operation above resonance (where the rectifiers are commutated by the transformer), a noticeable increase in ΔE_3 and an apparent decrease in ΔE (Figure 19) can be observed. Nevertheless, as was previously analyzed, this should not be interpreted as lossless transitions but as an effect of the additional Q_{rr}. This is further corroborated by the noticeably load-dependent increase in the measured charge (Q_{oss} plus Q_{rr}) in Figure 18.

Two samples of the NTMFS08N003C were subsequently tested in the improved back-to-back proposed circuit to isolate the loss due to the charge-discharge of their output capacitance. The result is captured in Figure 20, where a hysteresis loss of approximately 61 nJ can be observed. To account for the total losses in the application, the 61 nJ is

multiplied by the total number of devices (twenty-four), resulting in approximately 1.5 µJ. The discrepancy between this result and the previously estimated 8 µJ can be attributed to the different *dv/dt*, and therefore the relatively smaller currents passing through the lumped equivalent series resistance (R_{oss}).

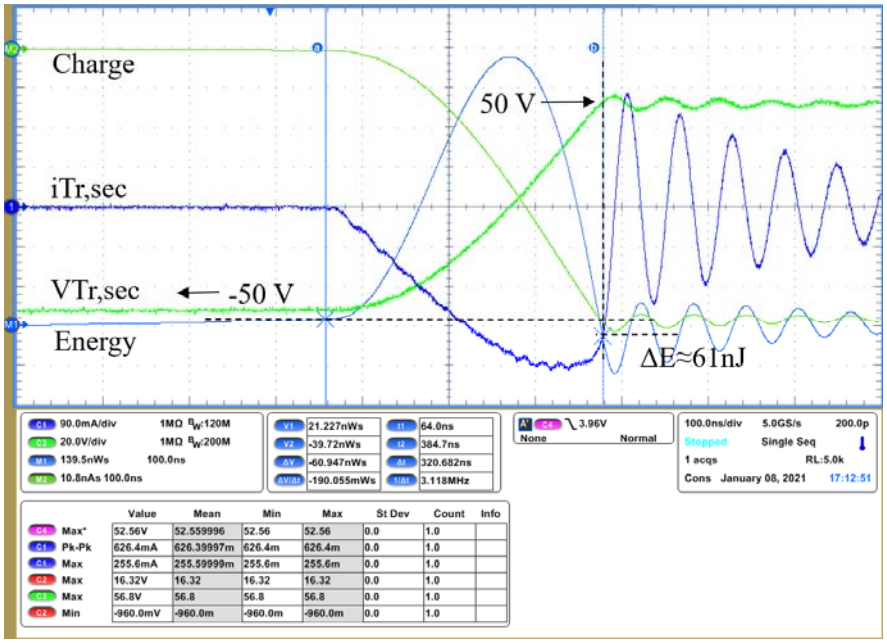

Figure 20. Measured hysteretic loss of NTMFS08N003C. Approximately 61 nJ.

In addition, two early samples of a new LV MOSFET technology from Infineon (ISC033N08NM6) were also tested in the proposed back-to-back circuit. The result is captured in Figure 21, where a comparatively lower hysteresis loss of approximately 57 nJ can be observed.

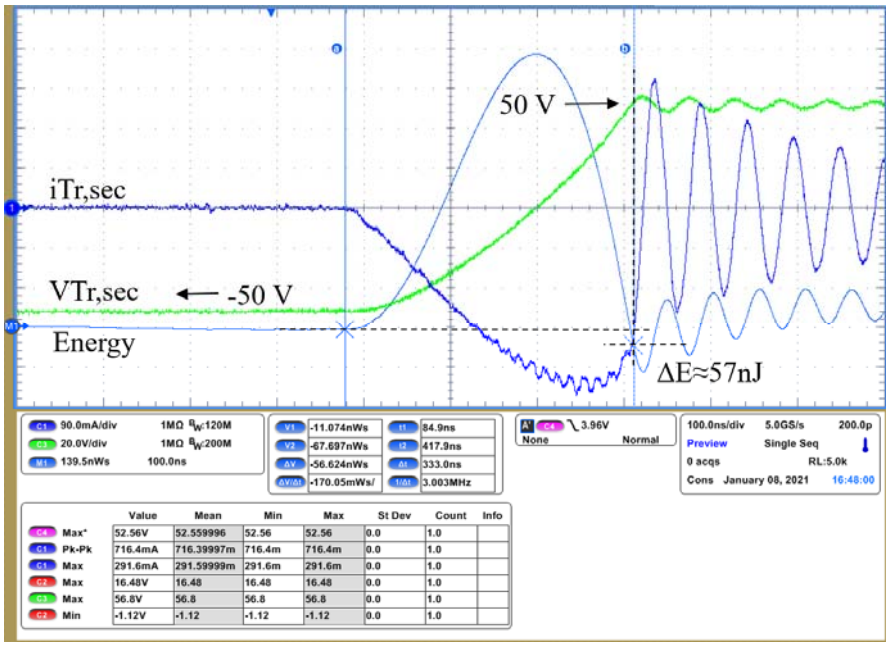

Figure 21. Measured hysteretic loss of ISC033N08NM6. Approximately 57 nJ.

4.2. High Voltage MOSFETs C_{oss} Loss

The LLC DCDC converter in [32] was further modified into the proposed improved measurement circuit in Figure 14 and applied to the measurement of the C_{oss} hysteresis loss in HV MOSFETs. As a result, it is also possible to evaluate, with the same setup, the ZVS switching losses of the primary side devices in the LLC converter. Figure 22 is a top-view of the newly developed measurement platform, including the selectable series inductor to achieve variable *dv/dt* conditions.

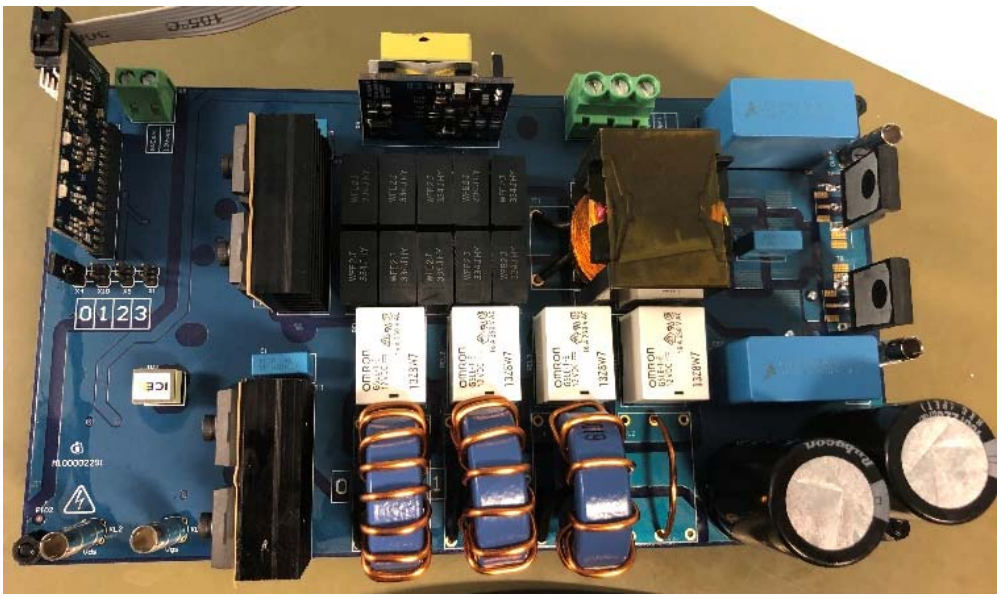

Figure 22. C_{oss} hysteresis loss measurement platform. The DUTs can be soldered to the multi-package pads on the top-right side of the image (e.g., the two standing TO-247 without a heatsink in this image).

Several examples of distinct HV MOSFETs technologies were measured while being charged-discharged at 400 V, which is a typical nominal input voltage in back-end DCDC converters as part of a complete PSU. In the experimental results, we compared a relatively old 650 V Silicon Super-Junction (SJ) technology (IPP65R065C7 in Figure 23), with a more modern 600 V Si SJ MOSFET of similar $R_{ds,on}$ (IPP60R070CFD7in Figure 24), and with a 650 V SiC MOSFET (IMW65R027M1H in Figure 15 and SCTW35N65G2VAG in Figure 25), and finally with a high-ohmic 700 V Si SJ MOSFET (IPAN70R900P7S in Figure 26). A summary of their results is presented in Table 2 together with the LV devices that were tested inside the LLC converter application in the previous section (NTMFS08N003C and ISC033N08NM6). This example highlights the convenience of the proposed method while underlining the superiority of the more recent technologies.

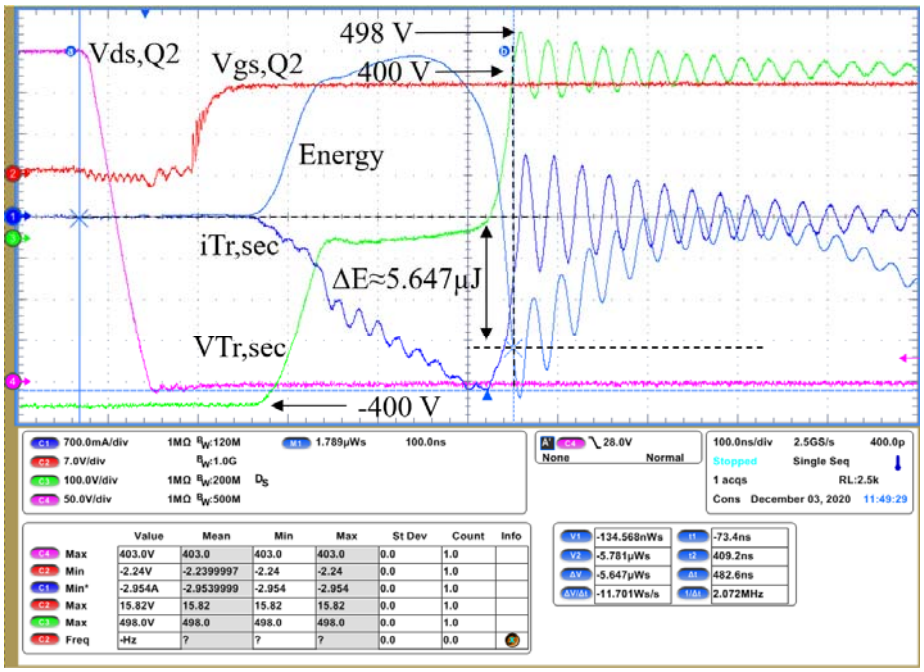

Figure 23. Measured hysteretic loss of IPP65R065C7. Approximately 5.65 μJ.

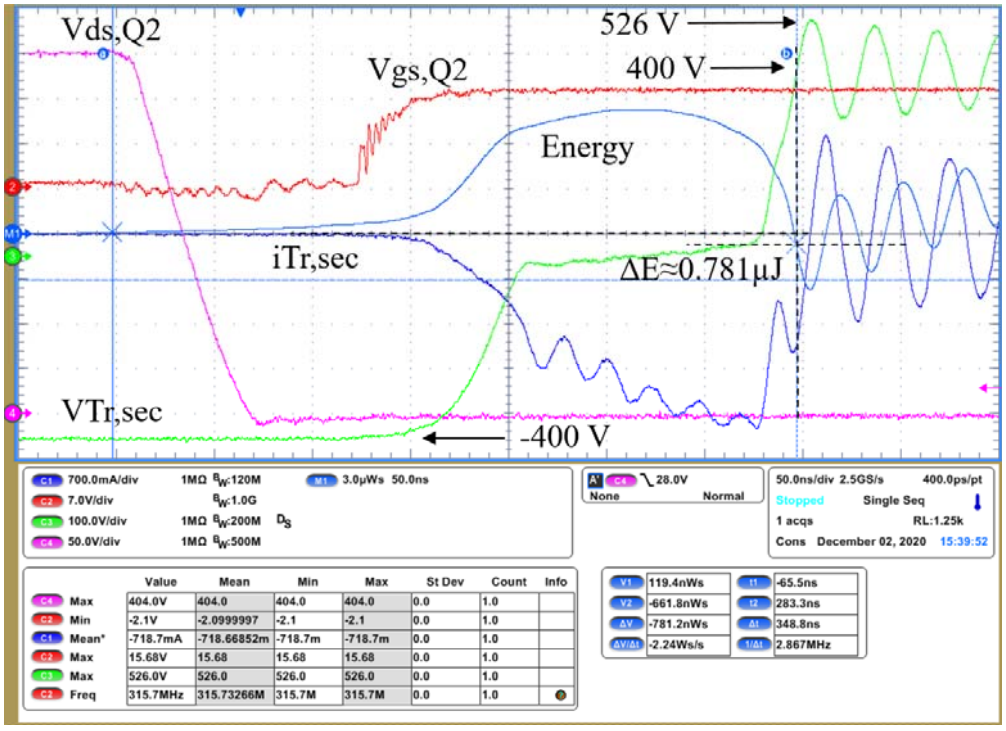

Figure 24. Measured hysteretic loss of IPP60R070CFD7. Approximately 0.78 μJ.

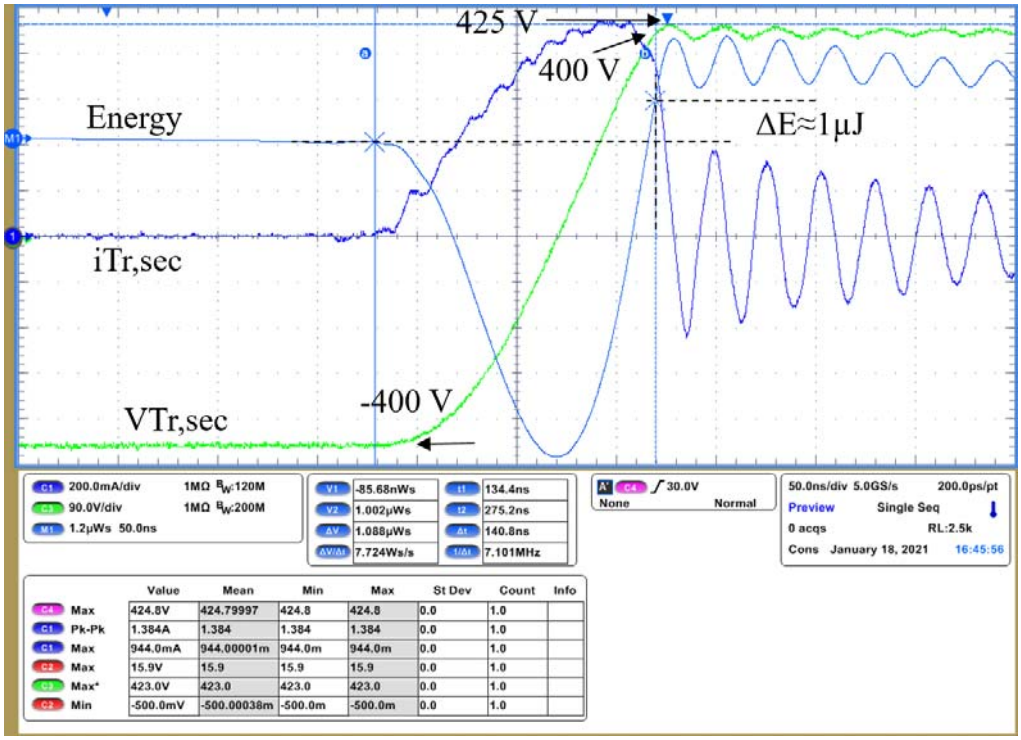

Figure 25. Measured hysteretic loss of SCTW35N65G2VAG. Approximately 1 μJ.

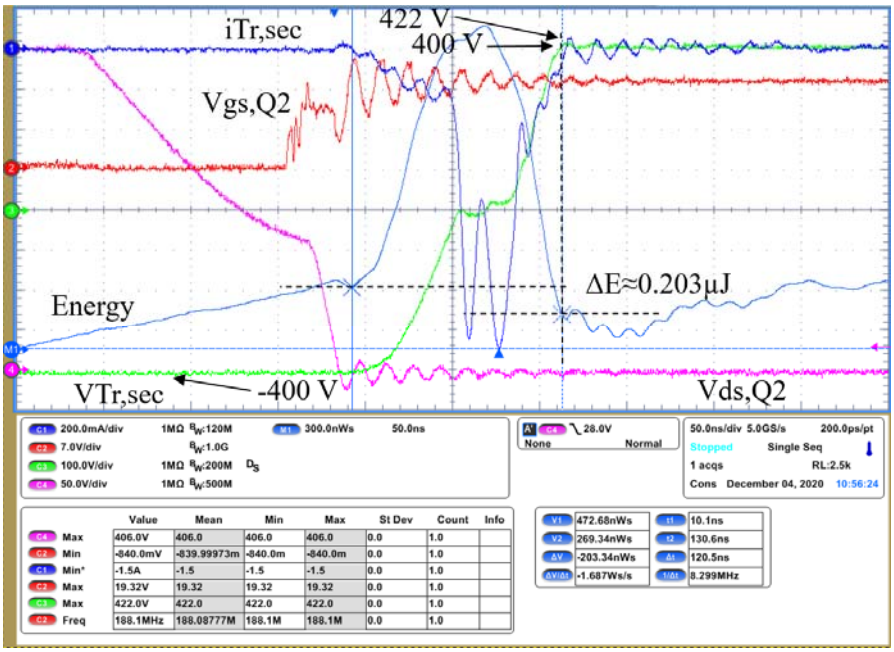

Figure 26. Measured hysteretic loss of IPAN70R900P7S. Approximately 0.203 μJ.

Table 2. Summary of device characteristics.

	$V_{DS,MAX}$ (V) @ 25 °C	$R_{DS,ON}$ @ 25 °C	E_{LOSS} (µJ)
IPP65R065C7	650	65 mΩ	5.65 @ 400 V
SCTW35N65G2VAG	650	67 mΩ	1 @ 400 V
IPP60R070CFD7	600	70 mΩ	0.78 @ 400 V
IMW65R027M1H	650	34 mΩ	0.35 @ 400 V
IPAN70R900P7S	700	900 mΩ	0.203 @ 400 V
NTMFS08N003C	80	3.1 mΩ	0.061 @50 V
ISC033N08NM6	80	3.3 mΩ	0.057 @50 V

5. Conclusions

In this paper, it has been experimentally demonstrated that the contribution of the switching loss of the secondary side rectifiers in LLC resonant converters can have a noticeable impact on the overall losses in all the operation modes of the converter, therefore decreasing the final efficiency of the complete power supply unit [25].

The analysis of the commutation process of the secondary side rectifiers together with the measurement techniques proposed in this paper enable the accurate estimation of the switching loss contribution. The experimental results demonstrate that the switching loss of the rectifiers comprises two sources: the reverse recovery charges Q_{rr}, especially (but not only) while operating the LLC above resonance; and the output capacitance C_{oss} hysteresis loss, not reported elsewhere in low-voltage MOSFETs previously, and present in all the operation modes of the LLC.

The principles of operation of the proposed characterization techniques for the switching loss in the secondary side rectifiers in isolated converters were utilized in two novel circuits designed for the separation and the measurement of the C_{oss} hysteresis loss of low-voltage and high-voltage semiconductor devices.

Finally, the C_{oss} hysteresis loss of several high-voltage and low-voltage MOSFETs was experimentally verified in the proposed testing circuits.

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