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Development of an Engineering Model for ESTCube-2 Power Distribution Electronics

Bachelor's Thesis (12 ECTS)

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Abstract:

Development of an engineering model for the ESTCube-2 power distribution electronics.
The power distribution is a crucial function of the satellite electrical power system (EPS)
responsible for the voltage conversion, power-related measurements, and power distribution to
various satellite systems. EPS of the satellite also includes energy harvesting and energy storage;
due to these functions, the electrical power system is one of the most essential systems of a
satellite. It must have a redundant, rigid design that can withstand some system or component
failures, the temperature, radiation, and other conditions presented by the low Earth orbit
environment. The different functions of EPS are performed in various locations in the ESTCube-
2 satellite - 3U CubeSat developed by the Estonian Student Satellite Foundation. It is critical
to carry out thorough tests for each electrical power system element to ensure that the power
requirements of each satellite system will be met. This bachelor's thesis aims to develop an
engineering model for the power distribution electronics that are located on a single board within
the ESTCube-2 nanosatellite - the EPS mainboard.

Lühikokkuvõte: ESTCube-2 toitealamsüsteemi insenerimudeli väljatöötamine Toitejaotus
ja signaalitöötlus on satelliidi toitealamsüsteemi (inglise k electrical power system, lühend EPS)
ülioluline element, hõlmates pinge muundamist, võimsusega seotud mõõtmiste läbiviimist ja
toite jaotamist erinevatele satelliitsüsteemidele. Satelliidi EPS tegeleb ka energia kogumise
ja salvestamisega; nende funktsioonide tõttu võib väita toitealamsüsteem üks satelliidi kõige
olulisemaid süsteeme. See peab olema robustse disainiga, mis taludes mõne süsteemi ja/või kom-
ponendi riket, temperatuuri muutusi, kosmilist kiirgust ja muid tingimusi madalal Maa orbiidil.
Väga tähtis on põhjalikult katsetada elektrisüsteemi igat elementi, et täita kõik satelliitsüsteemide
esitatavad võimsusnõuded. ESTCube-2, 3U kuupsatelliit Eesti Tudengisatelliidi Sihtasutuse
poolt, EPS'i funktsioonid asuvad välja töötatud satelliidi eri kohtades. Selle bakalaureusetöö
eesmärk on aga välja töötada energia jaotuse ja signaalitöötlemise elektroonika insenerimudel,
mis seondub ESTCube-2 nanosatelliidi EPS põhiplaadiga.

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Acronyms and Abbreviations

AC	Alternating Current
ADC	Analog to Digital Converter
AOCS	Attitude and Orbit Control Subsystem
BUS	Function and command block of the satellite, which has all of the required subsystems
CGP	Cold Gas Propulsion Payload
CMOS	Complementary Metal Oxide Semiconductor
COM	Communications Subsystem
COTS	Commercial-off-the-shelf
CRE	Corrosion Resistance Experiment Payload
DC	Direct Current
EC1	ESTCube-1
EC2	ESTCube-2
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EOP	Earth Observation Payload
EPS	Electric Power System
ESR	Equivalent Series Resistance
FRAM	Ferroelectric Random Access Memory
GND	Electrical ground
HSCOM	High-Speed Communications Payload
IC	Integrated Circuit
LDO	Low-Dropout Regulator
LEO	Low Earth Orbit
Li-ion	Lithium-ion
MCU	Microcontroller Unit
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
MPB	Main Power Bus. Voltage range for this bus is from 6.6V to 8.4V
MPPT	Maximum Power Point Tracker
OBC	On-Board Computer Subsystem
PCB	Printed Circuit Board
RTC	Real Time Clock
RW	Reaction Wheel
SP	Side Panel Subsystem

Introduction

ESTCube-2 is a three-unit CubeSat developed by the Estonian Student Satellite Foundation, and it is planned to be launched in 2022. It is the successor to the ESTCube-1 mission launched in 2013, and it is a prototype for the ESTCube-3 mission that is planned to be sent further from Earth to test the electric sail in a natural solar wind environment. CubeSat is a class of nanosatellites built from units of standard dimensions of 10x10x10 centimeters, and one unit typically does not weigh more than 1.33 kilograms. CubeSats can be made up of more than one unit in different combinations resulting in different dimensions. [3] Design choices have to be made accordingly so that the available space is used as efficiently as possible. In the case of ESTCube-2, the dimensions of the satellite will be 10x10x30 centimeters.

Currently, approximately 6000 satellites are orbiting the Earth, 60% of these satellites are not functional, and by the year 2028, this number could reach 15 000 satellites.[4] As the number of satellites increases, the possibility that they will collide increases as well. As the Kessler syndrome indicates, this could lead to a self-sustaining chain of collisions between other satellites and the debris of previous clashes. [5] This can deem further space exploration very difficult. The main goal of ESTCube-2 is to deploy a conductive, 300-meter long tether that will take advantage of the Coulomb drag phenomenon and lower the satellite's orbit from 700 kilometers to 500 kilometers in one and a half years. It will also provide scientific data for using the electric sail as means for future spacecraft propulsion. The satellite will also conduct various other experiments throughout its lifetime. [6]

ESTCube-2 consists of different subsystems and payloads that ensure the proper operation of the satellite, gathering of scientific data, and the completion of its scientific goals. One of these subsystems is the electrical power system (EPS). It is responsible for various power-related functions of the satellite and consists of three different elements - energy harvesting, energy storage, and the power distribution network. The latter element has the main focus in the thesis, and it involves voltage conversion, power distribution, power-related measurements, and other critical functions.

This bachelor's thesis aims to develop an engineering model for the EPS power distribution electronics located on a single board within the satellite - the EPS mainboard. An engineering model closely resembles the flight model placed on the satellite and can be connected with other subsystems. The thesis covers an overview of the electrical power system of spacecrafts, overview for the design of physical circuits, types of different voltage regulators, previous research, and papers closely related to the EPS of ESTCube-2 and the estimated power requirements of the ESTCube-2 nanosatellite. New devices have been implemented within the EPS mainboard to maintain consistency across different subsystems, and a description of various parameters has been included. Schematics and printed circuit board design of the power distribution electronics have been developed, and initial tests have been performed to determine the functionality of different devices present on the engineering model.

1   Literature Review

1.1   Electrical Power System of Spacecrafts

An electrical power system (EPS) is responsible for different functions regarding power management within a spacecraft. Thus it is considered one of the most critical systems. It has to ensure that all the power requirements of other systems are met so that the spacecraft can function correctly. It has to be reliable and robust against failures, such as short circuits, within the system or the supplied units. Many of the early satellites failed due to the loss of EPS. [7] [8]

Main functions of an EPS are power harvesting, power distribution, voltage conversion, monitoring the data related to power consumption, and communicating with other subsystems. EPS typically consists of three elements: [8]

- Primary source of energy that is responsible for supplying electrical power throughout the lifetime of the mission

- Secondary source of energy that is responsible for supplying electrical power when the consumption of power exceeds the power capabilities of the primary energy source or when the primary source is not available

- Power distribution network that manages the electrical power path between the sources and the loads

The primary source of energy for a spacecraft usually depends on combining the required power output of the source and the duration of the mission. Most typical power sources for spacecraft are solar arrays, fuel cells, batteries, radioisotope thermoelectric generators, and other less commonly used sources such as nuclear fission or solar heat systems. For missions that extend over few weeks, solar arrays are a common choice for the primary power source. Batteries are the common choice for the secondary power source, and the type of the battery cells depends on the discharge rates and depths required by the mission. The characteristics of the power sources will change throughout their lifetime; thus it is important to establish power regulation and control within the system so that the current and voltage requirements of the satellite are satisfied throughout the whole mission period. A common combination of power sources in satellites is solar arrays as the primary source and battery cells as the secondary source. [8] Li-ion cells gain popularity in space missions, and also Li-ion cells were used as the secondary power source in the ESTCube-1 mission.[9] Li-ion battery cells will be used in the ESTCube-2 mission as well.

The underlying architecture of spacecraft EPS design remains somewhat consistent across different satellite missions. However, there is no single, correct configuration. Each satellite mission tries to maintain systems reliability and efficiency and tries to satisfy the specific requirements introduced by exotic payloads, subsystems, environments, or other factors related to the given mission. A single power bus controlled by a single EPS is usually an acceptable solution, as in the ESTCube-1 mission, where the primary/secondary source is connected to a single power bus that is controlled and distributed through a single power distribution network. There have also been attempts to increase the reliability of the spacecraft by implementing multiple power systems that operate in parallel, each managing its power sources. Also, architectures of isolated and redundant spacecraft systems that allow the spacecraft to operate if one system fails. [10][11][12][13][14]

A typical spacecraft power system can be seen in figure 1., which consists of solar arrays, batteries, and power distribution/regulation elements. There are two basic types of energy transfer for solar arrays - direct energy transfer and series bus transfer, which usually is the maximum power point tracking (MPPT). ESTCube-1 and ESTCube-2 use MPPT for energy harvesting, which allows the utilization of the solar cells at their maximum power point and follows the maximum power point in cases where the power characteristics of the solar cell change (different illumination or temperature). The drawback of MPPT is its relatively low power transfer efficiency since the MPPT system is connected in series with the solar arrays and the power bus. [15]

Commercial power systems may also be used for the satellite rather than building one "in-house." Commercial power systems may provide a reliable solution for power management. However, they may also add additional spatial restrictions that may not be suitable to the satellite design. They may not be compatible with the power requirements of other satellite systems and add to the overall costs of the satellite. [16]
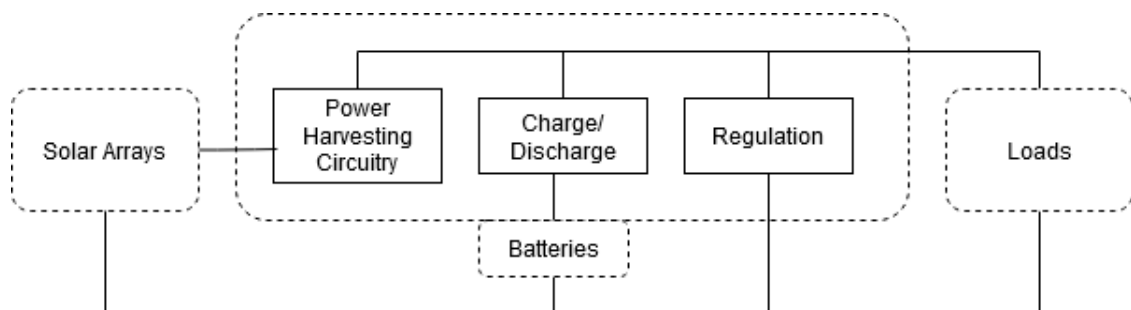

Figure 1. Block diagram of typical spacecraft power system elements

1.2 Design of Physical Circuits

Electromagnetic interference (EMI) and electromagnetic compatibility (EMC) have been a significant concern since the 1970s when digital circuits gained popularity in commercial electronics. However, military, space agencies, and other government institutions had been aware of this issue for many years before. [17] Even if the proposed logic and schematics of the circuit are correct, it does not necessarily mean that the actual circuit will operate as expected. Thus, it is essential to keep the EMC of the circuit in mind when designing the physical circuit to avoid EMI-related issues further in the development process and avoid redesigning the circuit.

The node size of the current semiconductor devices already reaches into the 10nm range, which allows the development of small, powerful devices.[18] The internal planes, interconnections, bond wires, and other parts of the semiconductor devices have electrical characteristics that may lead to unexpected results in a real-life environment. For example, "ground bounce" as well as "VDD drop" is a concern of complementary metal-oxide-semiconductor (CMOS) devices - if the state of the internal transistor changes, sudden movement of charge will be present that will develop a voltage drop across parasitic inductances within the device, causing a voltage difference between the die and the circuit reference point. The voltage difference may be significant enough that the device observes a completely different logic state and cause false triggering. Additionally, the power source may not provide sudden, instantaneous current flow, which will cause a drop in voltage supply and reduce the voltage difference between the power and the ground pins. It is typically not an option to affect the device's internal design, so the physical circuit design must be developed so that there is no addition to these unwanted characteristics. For example, reduce the pin load capacitance, proper use of decoupling capacitors at the power pins, and stable reference planes. [19][20]

The energy within the circuit will flow through the path with the least impedance. Impedance depends on three different elements - inductive reactance, capacitive reactance, and resistance. Reactances are dependent on the frequency, so in direct current (DC) circuits impedance is dominated by resistance, and the current will flow through the path of least resistance. However, when the frequency of the signal increases, reactive elements start to take over, and the path of energy is not necessarily a continuous conductive material anymore. Another important thing to note is that the signal travels in a closed circuit and will return to the signal source, meaning that it will have both the signal and the return paths. Different elements of the printed circuit board (PCB) may have specific electrical characteristics and may form additional propagation paths. For example, two parallel traces could be observed as a capacitor with some finite capacitance and thus capacitive reactance. [21] As the alternating current (AC) signal travels through the signal path, in some cases, the signal can directly couple into the return path and may not even reach the receiver. Also, if the AC signal travels through the signal path, it may encounter a change in the instantaneous impedance that will result in some of the signal being reflected back to the source. As this occurs, the propagating signal and the reflected signal may interfere with each other resulting in higher and lower signal amplitudes that may damage the device or result in faulty triggering. [22]

1.2.1 Noise in Electric Circuits

Noise in circuits can become a serious issue if energy path within the circuit is not considered. There are three types of noise - inherent circuit noise, quantization noise, and the coupling noise. The inherent circuit noise arises from the natural movement of electrons and always will appear in measurements to some extent. The quantization noise arises from the digitization of analog signals as a certain amount of information is lost during this process. Coupling noise arises from the unexpected transfer of energy from one part of a circuit to another and is of particular interest to PCB designers. There are four types of coupling mechanisms, through which interference can occur: [23]

- Conductive coupling - a type of coupling that results from two signals sharing a common impedance, and some energy from one signal can be transmitted to the other signal

- Magnetic coupling - a type of coupling that occurs when the magnetic flux of a current loop passes a receptor loop, inducing a voltage potential. A major suggestion for PCB designers is to maintain these current loops as small as possible, as they will be less susceptible to receiving noise, and they will be less capable of transmitting noise.

- Electric field coupling (Capacitive coupling) - a type of coupling that occurs when the electric field flux of one circuit terminates on the conductor of another circuit.

- Electromagnetic coupling - Coupling occurs as a simultaneous electric and magnetic field coupling into another circuit. At close distances, usually, either of the fields dominates and can be observed as an electric dipole. These are known as near-field emissions. But as the distance from the source increases, the intensity of dominating field lowers and generates a proportional counterpart of other field type. The field strength decreases until both electric and magnetic fields have only the characteristic wave impedance of 377 Ω

1.2.2 Power Loss

Resistors are one of the most common devices in circuits. It is important to consider that different objects within the circuit - traces, wires, integrated circuits (IC), and others, have different electrical characteristics, including resistance. This will result in power loss that is proportional to the current flowing through this element and its resistance. In power traces, where typically large currents are involved, power losses can become quite remarkable if trace widths and lengths are not designed properly. Power loss within a trace can be calculated with equation 1., where X is the width, Z is the height, Y is the length, and ρ is the resistivity of the material. [24]

$$R = \frac{\rho \cdot Z}{X \cdot Y} \qquad \text{(Eq. 1)}$$

1.3 Linear and Switching Voltage Conversion

Linear and Switching regulators are a common choice for achieving the necessary voltage in DC circuits. They typically consist of three elements - feedback signal, pass element, and control circuitry that manages the pass element. Suppose the regulator operates with the active region of the pass element. In that case, it is considered the linear voltage regulator. If it operates in the component's saturation regions, it is regarded as a switching regulator. Both types have specific advantages and disadvantages, and the choice can depend on different design factors. These factors can include available space, load current, efficiency requirements, and others. These devices also serve an important role in the ESTCube-2 (EC2) EPS power distribution electronics. The following sections cover the design requirements for each of the devices.

1.3.1 Linear Voltage Regulators

Linear voltage regulators can range from a relatively simple circuit consisting of only a zener diode, transistor, and a resistor to more complex designs involving current limiting, feedback control, and others. These devices are not considered very efficient as a considerably large amount of power is being dissipated as heat and are only able to regulate the voltage to lower values. However, the voltage changes are linear, and no fast switching is involved, thus the devices are much less noisy and generally do not need additional attention to the layout. There are two types of linear voltage regulators - shunt regulator, connected in parallel with the load, and series regulator, which is in series with the load. [25]

Typically, the output of the series voltage regulator is sensed by an error amplifier through a resistive divider. The output of the error amplifier controls the resistance of the pass element. The input current and the output current of the regulator are almost the same. The amount of power being dissipated in the series regulator is proportional to the load current and the difference between input and output voltage. Typically the result from equation 2. provides a good estimate of power loss within the series regulator. [25]

$$P = (V_I - V_o) \cdot I_L \qquad \qquad \textit{(Eq. 2)}$$

Shunt regulators have an additional resistor in series with the load. The regulator tries to maintain a certain voltage drop across the resistor by directing some of the current to the electrical ground. Shunt linear regulator functions as a simple resistive divider, where the resistors are the pass element of the regulator connected to the electrical ground and an actual resistor, which is in series with the supply.

1.3.2 Switching Regulators

Switching regulators are more efficient devices than the previously described linear regulators. However, they have drawbacks and factors to consider to obtain this advantage. Switching regulators involve high-frequency switching and relatively large currents, thus it has the potential for severe EMI issues. There are many switching regulator topologies, some more and some less complex. This section will focus on the step-down (buck) converter topology used in EC2 EPS.

1.3.3 Basic Operation of a Step-Down Converter

Key elements and logic of typical buck converter can be seen in figure 2. The pass element is periodically turned off and on, and the duty cycle of the pulses depends on the feedback signal. The frequencies of the switching can range from hundred kilohertz to several megahertz. With higher frequencies, smaller value inductors and capacitors can be used, which leads to more space on the board, however, with increasing frequencies, the EMI issues and guidelines become more prevalent. [26]

When the device is operating, high switching currents are involved. When the switch goes from open to closed, the current will flow as indicated with the blue loop in figure 2., and there will be some voltage difference across the inductor, so the current will gradually increase. When the switch opens, the magnetic field stored in the inductor will collapse and produce a voltage drop across the inductor opposite the current direction allowing the current to flow in the same direction. This step is represented with the red loop in figure 2. These loops can be a serious source of EMI if not designed properly because the loop path can cross potentially susceptible signals or devices. [27] The switch state and transitions depend on the resistive divider on the output that provides the feedback signal for the converter. [28]

The efficiencies of these devices depend on the components present and their characteristics. The highest power losses occur in the pass element and the free-wheeling diode. Considering that there are AC switching losses present, the exact power loss in the regulator is harder to estimate. [27]
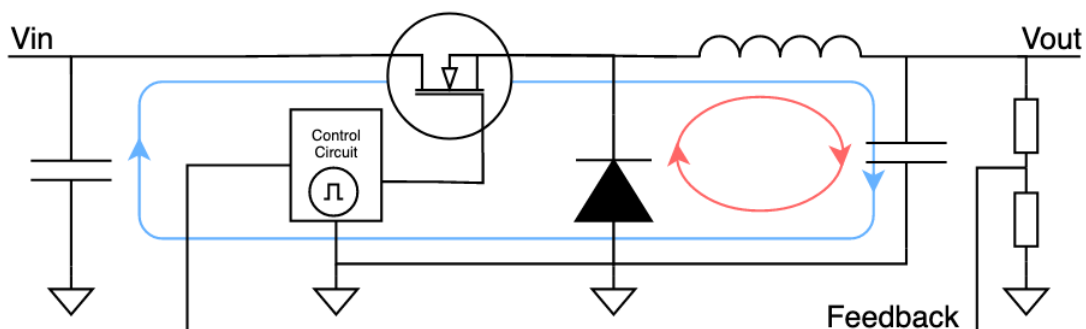

Figure 2. Diagram of a basic step-down converter topology

1.3.4 Inductor

The inductor is an essential component in switching regulators as it provides energy in the off states of the pass element and delays the current on the output when the switch is closed. Larger inductance inductors also reduce the ripple current amplitude, decreasing the power dissipation in the capacitors and increasing their lifetime. As the magnetic field can couple into other parts of the circuit and induce a voltage, the inductor can operate as a transmitting loop antenna, so the choice of the inductor and its placement must be approached with care. Inductors can be classified as un-shielded, semi-shielded, and shielded. Shielded inductors are particularly of interest in power circuits. However, this comes to the cost of lower inductor saturation currents and considerably larger package sizes. Shielded inductors also have leads that are not covered and can potentially radiate energy. [29]

1.3.5 Capacitors

Capacitors are an important part of the switching regulator circuits as they provide a low impedance path for the switching currents. The placement of the capacitors is important, and the low equivalent-series-resistance (ESR) capacitors have to be placed as close as possible to the switching elements because with the distance, the impedance of the path increases due to parasitic resistances and inductances present in the physical circuit. The frequency characteristics of capacitors must also be considered. They must meet the frequency requirements because, with increased frequencies, stray inductance within the capacitor can noticeably increase the impedance. [30] [31]

Input capacitors are used to supply the ripple currents for the converter and the low impedance path for the switching currents. Small ESR capacitors have to be used for input capacitors as large values do not reduce ripple and may cause excessive power dissipation in the capacitor. Input capacitors are also necessary to avoid switching currents to be sourced from the power supply that would cause EMI issues. Suppose large transient load currents are frequent in the design. In this case, additional bulk capacitors may be needed because the power supply cannot provide current instantaneously, meaning that the voltage on the input would drop. [30] [31]

Output capacitors play an important role in the switching current return path. For output capacitors also low ESR capacitors have to be used. If placed far away, the switching current will also travel a larger distance causing a larger loop. They also provide a fast transient response - when a transient event occurs, initially, the current has to be supplied from the capacitors until the current in the inductor has risen to this level. [30] [31]

2   ESTCube-2 Electrical Power System Overview

Different power system elements of EC2 EPS have been located in various locations of the satellite. The power harvesting circuitry is located on the satellite's side panels. The battery management circuitry is located on the battery management board. The power distribution, conditioning, and the primary EPS control logic electronics are located on the EPS mainboard. The MPPT of the satellite is independent of the EPS mainboard, so this element is not discussed in this thesis. However, the EPS mainboard has to control and communicate with devices present on the battery management board, and additional connections must be made between the two boards. It is also important to discuss and study the prior work closely related to the ESTCube-2 EPS power distribution logic so that direct continuation of the previous work can be done without any misinterpretation. Several theses are written related to the ESTCube-2 EPS, each covering a specific aspect of the system and includes the lessons learned from the successful ESTCube-1 mission. This information and a general overview of EC2 EPS are covered in this chapter.

2.1   Electric Power System Architecture

ESTCube-1 EPS was designed to be efficient, fault-tolerant, and made from commercial-off-the-shelf (COTS) components. The general architecture consisted of a single main power bus (MPB) powered by solar arrays through maximum power point tracking (MPPT), acting as the primary power source. Two Li-ion cylindrical battery cells served as the secondary power source. The MPB supplied varying voltage in the range from 3.7V to 4.2V to the energy distribution block that used switching regulators to convert this voltage to three different voltages - 3.3V, 5V, and 12V, and then distributed them to other systems of the satellite. [32]

ESTCube-2 implements a similar approach and uses a single power bus with a varying voltage from 6.6V to 8.4V (MPB), which is a crucial difference compared to the ESTCube-1 power architecture. The primary power source in EC2 is solar arrays located and managed on the satellite's side panel subsystem (SP). The maximum power point tracking (MPPT) of the solar arrays are also executed on the side panels of the satellite. The secondary power source consists of two battery packs, each containing two prismatic Li-ion battery cells in series. Both of the power sources are connected to the MPB. The MPB voltage will be either directly distributed to the loads, or it will be converted to 3.3V and only then distributed further by the EPS mainboard. Additional voltage conversion steps are taken if there are particular voltage requirements by specific subsystems or payloads. The control over the power distribution and voltage conversion is achieved with a microcontroller unit (MCU) located on the EPS mainboard. [1] The described EC2 EPS architecture can be seen in figure 3., which shows all of the EPS elements that will be present in the EC2 satellite.
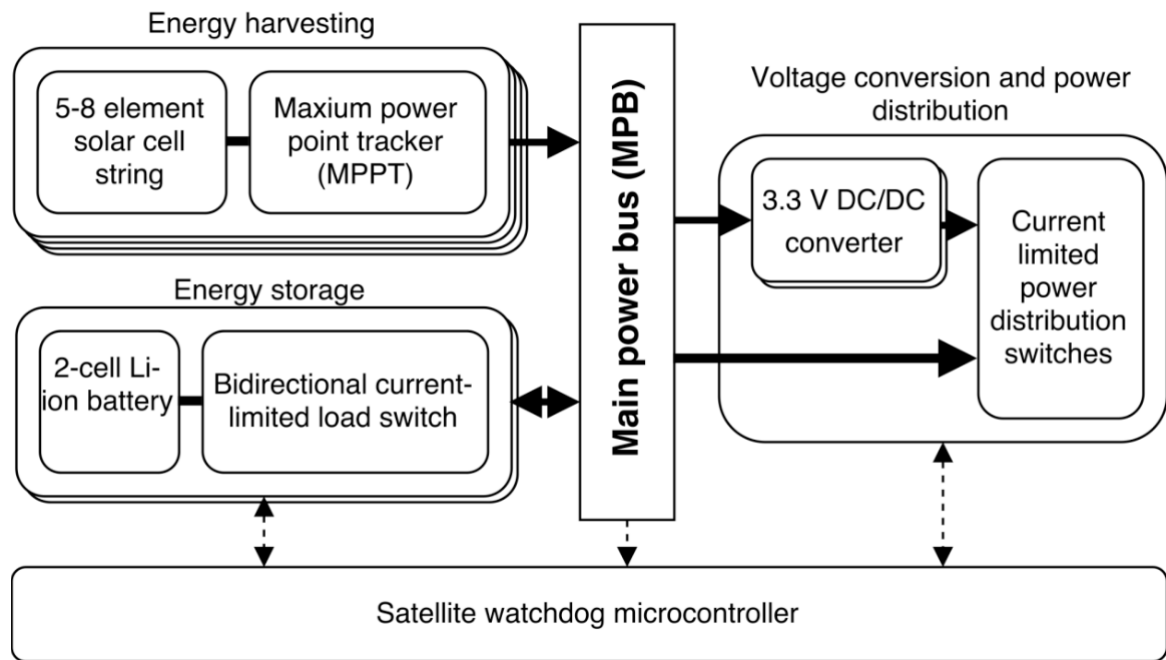
Figure 3. Blcok diagram of ESTCube-2 electrical power system architecture, proposed by Erik Ilbis in 2015. Bold arrows represent current flow and dashed lines illustrate control and measurement interfaces. [1]

2.2 Voltage Conversion

As discussed in the previous section, the MPB is converted to a 3.3V which is further distributed to other satellite subsystems. The choice for the voltage regulators was narrowed down to a step-down converter due to its relatively large current capabilities and high efficiency. However, these devices are more complex and require more care in layout on the circuit board. Six devices were evaluated, and the final choice was narrowed down to the LTC3603 synchronous step-down converter. The output current rating of this device is 2.5A. The selection of this specific device was based on the high efficiency compared to the other devices. It had a good transient response, low ripple, and low near-field magnetic field emission in the 430MHz band, the predicted communication frequency. [1] [33] [34] The suggested layout for the step-down converters was to place the LTC3603 IC directly underneath the inductor and not place the convertor circuitry near any critical signals or devices. The proposed design for the 3.3 voltage regulation step was an FPF2700 load switch in a series with an LTC3603 regulator and a combination of a MOSFET and an LTC4412 low-loss power path controller IC that would act as a near-ideal diode configuration. For redundancy and load sharing purposes, two of these voltage regulation circuits should be connected in a hot-redundant parallel connection, meaning they both will operate simultaneously. [1]

2.3 Power Distribution

The power distribution circuitry aims to protect the supplied systems, power sources, and the EPS mainboard from excessive current consumption and switch individual loads off when their operation is not required. Every subsystem and payload on ESTCube-2 has a dedicated load switch located and controlled on the EPS mainboard. An exception is the communications subsystem (COM), which does not have load switches located on the EPS mainboard. For the consumers that use MPB, two different solutions have been proposed and tested for the power path control - a combination of ADM1170 hot-swap controller[1], sense resistor, and a MOSFET or an FPF2700 load switch. Both of the proposed solutions have specific advantages over the other. In the ADM1170 solution, the current capabilities are determined by the chosen MOSFET, which can be noticeably higher than the FPF2700 2A current rating. Another noticeable difference is the power that will be dissipated as heat when the current will flow through. In the case of FPF2700, the typical ON-resistance is 95mOhms. As the MOSFET determines the power dissipation in the ADM1170, it can be considerably lower than the 95mOhms of the FPF2700 device. As current measurements will be performed in both described solutions, the sense resistor is also necessary for the FPF2700 load switch, which adds to the overall losses. A significant difference between these two solutions is the radiation tolerance data that is very appealing to space technology. ADM1170 has no radiation tolerance information available. On the other hand, FPF2700 has been shown to function under radiation levels similar to those observed in the low Earth orbit (LEO) environment. [35] For devices that operate under 1.5A, the FPF2700 solution is suggested, and for devices that require higher currents, the ADM1170 solution is suggested. Both solutions are also suitable for 3.3V consumers. Another suggested possibility for the 3.3V distribution is to use TPS2551 (TPS2553 improved version of TPS2551) or TPS2557 load switches which were successfully used in the ESTCube-1 mission. [1]

2.4 Control Logic

The voltage for ESTCube-1 (EC1) control circuitry was 5V, and it also required additional level converters for separate devices that operated at 3.3V. This was not optimal as it reduced the overall robustness of the system. Suppose a fault occurs within these level converter devices, the whole system's functionality could be significantly affected. This was a major factor that led to a single 3.3V voltage for the EC2 control circuitry. Initially, the control logic of EC2 EPS was based on two identical MCUs (MSP430FR5969) - one as the main MCU and the other for diagnostic purposes. The main MCU was able to take over the functions of the diagnostics MCU through a bus switch, which provided additional robustness of the system in case of failures. However, in further development, a new, more capable device of the same device family with a higher pin-count became available. Due to these reasons, the two MCUs were switched to one MSP430FR6989. An input voltage fault detector was implemented to detect the loss of input voltage. When this state is detected, additional capacitor banks that store electrical energy

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[1]Devices used to control sudden inrush currents, when a system is connected

allow the MCU to perform emergency operations or writes to the memory before it shuts down completely. On ESTCube-1, MAX1230 by MaximIntegrated analog-to-digital converter (ADC) was used. However, this device does not operate at 3.3V, leading to a decision to switch to MAX1231 ADC, which MaximIntegrated also develops. [1] [2] General functionality of the EPS control electronics prototype can be seen in Table 1.

Device	Part Number	Function
MCU	MSP430FR5969	Subsystem control
MCU	MSP430FR5969	Diagnostics
ADC(2x)	MAX1231	Analog signal measurements
FRAM(3x)	FM25V20	External memory
RS485 Transeiver (2x)	LTC2850	Communications with other satellite subsystems
External watcdog timer	MAX6369	Additional external timer tht is tied to the reset pin
Real time clock	DS3234	Keeping track of time
Operational Amplifier	LMR10515	Power failure detection

Table 1. EPS control electronics prototype functionality. [2]

3   ESTCube-2 System Requirements

Different subsystems and payloads of the EC2 ensure successful satellite operation and completion of scientific experiments. Each system has specific power requirements which have to be satisfied for proper, predictable operation. All subsystems - EPS, COM, on-board computer (OBC), star tracker (ST), except the side panel (SP) subsystem, are located in a single stack of printed circuit boards, which is visualized in figure 4. The same PCB stack also contains the battery management board responsible for the battery cell management and protection and an additional bottom plate adapter meant for connections with other satellite systems. These boards and their locations are also visualized in figure 4. Side panels are located on each plane of the satellite. There are also additional payloads that are not developed by the students of the University of Tartu. Their physical location in the satellite is either above or below the PCB stack. However, they can't be visible in figure 4. An exception is the corrosion resistance experiment (CRE) payload, which is located on the SP subsystem. Connections between the COM, ST, OBC, and EPS subsystems are made through connectors that run through the whole PCB stack. Connections to the side panels are made through four right-angle connectors on each of the four EPS and COM board sides and the connectors located on the battery management board and the bottom plate adapter. Based on location in the satellite, connections to the payloads are made through the bottom plate adapter or the battery management board.

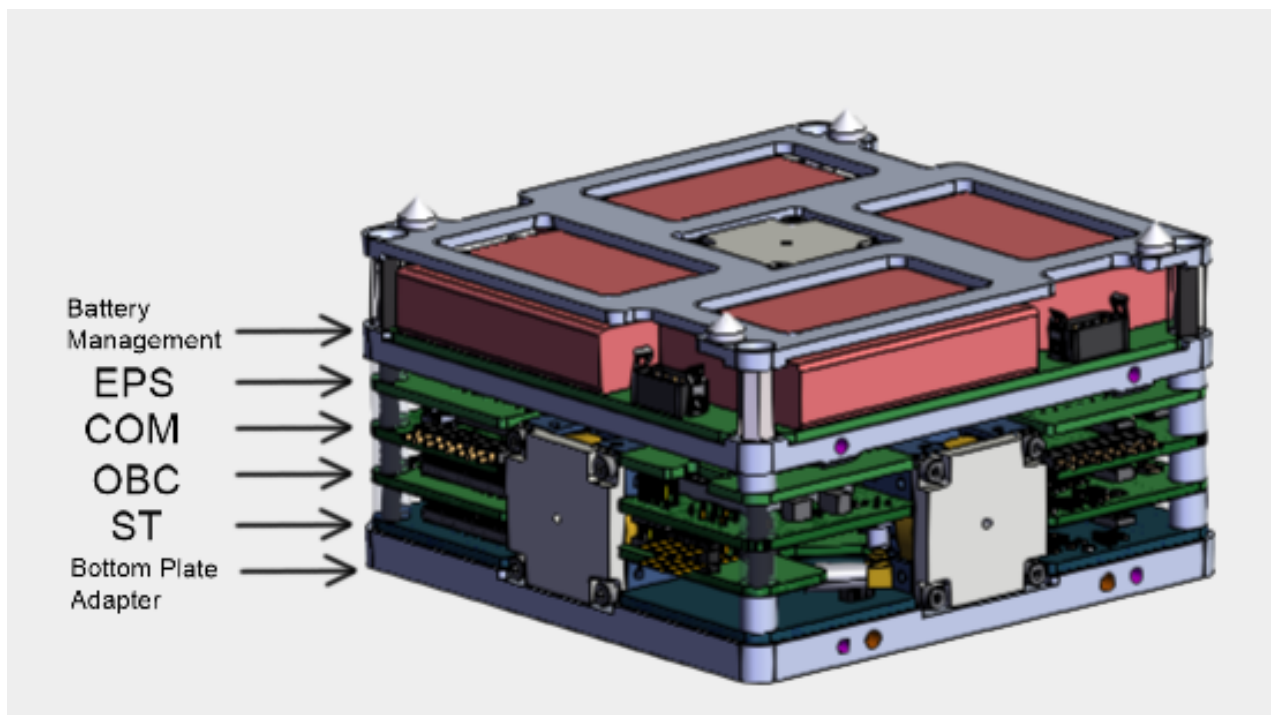**Figure 4.** 3 dimensional rendering of EC2 BUS consisting of EPS, COM, OBC, ST subsystems, batteries, structural elements, and other

Both the payloads and the subsystems have different modes of operation, including various power consumption for different periods. There are also single events that may involve specific power consumption, after which this mode will never occur again, for example, the burning

of wire for side panel deployment or E-Sail deployment, which involves numerous different steps. Responsibilities of the EPS mainboard in the ESTCube-2 include the assurance of the appropriate power supply to the specific system when it is operating, the possibility to turn off a particular system if its operation is not necessary and limit the current that is supplied to this system in case of faults. The most recent state of the power distribution network of the ESTCube-2 satellite can be seen in figure 5. In the block diagram, the EPS block represents both the EPS mainboard and the battery management board as their operation is closely related. There are three different voltage levels present in the ESTCube-2 satellite - 3.3V, 5V, and the MPB, which has a floating voltage from 6.6V to 8.4V. The current at MPB voltage level can flow bidirectionally between the battery management board, EPS mainboard, and the side panels. In all other cases, the current only leaves the EPS mainboard.
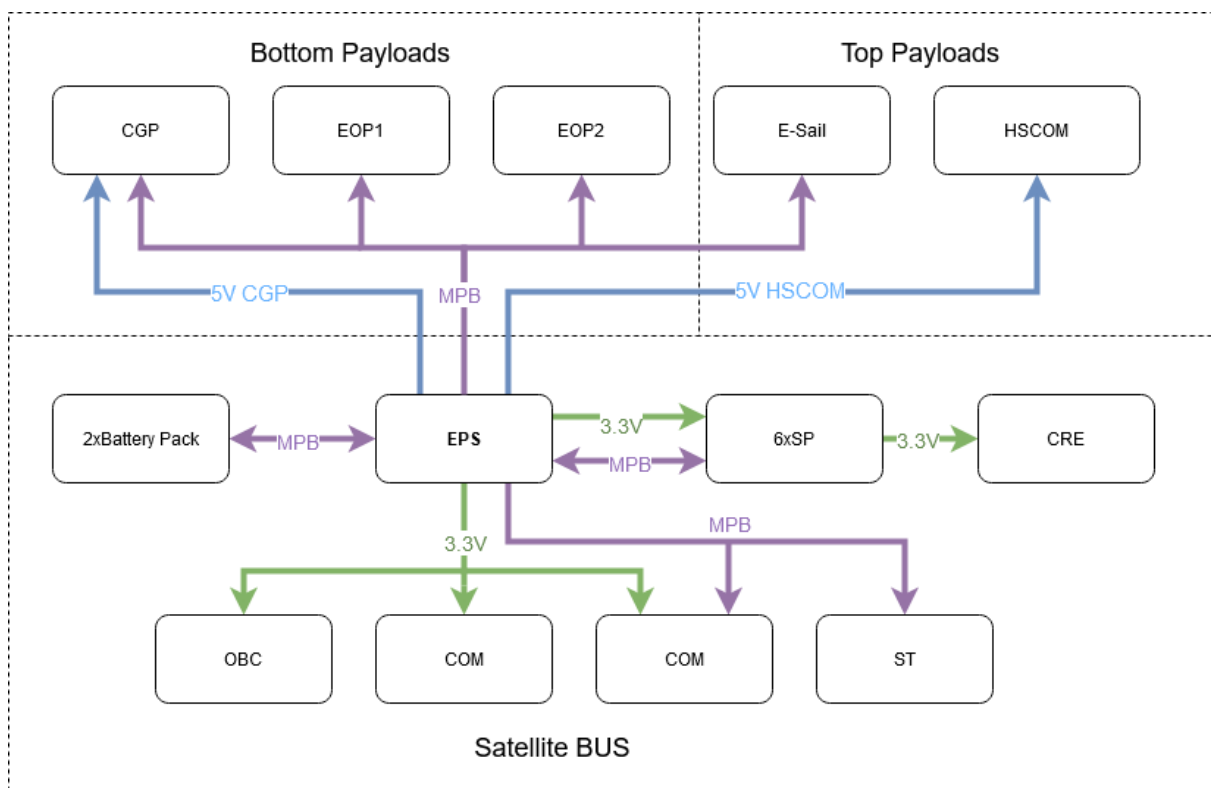
Figure 5. Block diagram of the ESTCube-2 power distribution network. Arrows indicate current flow and its direction

There are six side panels present on EC2, and they, as a whole, are considered the side panel subsystem (SP). Side panels are responsible for solar energy harvesting. The MPPT step is located on the side panels as well, and its output is connected to the MPB, allowing it to power the satellite and charge the Li-ion battery cells. The EPS supplies side panels with 3.3V. The configuration of each side panel is slightly different and may consist of different devices, but the primary 3.3V consumers of a single side panel remain consistent - main MCU, sun sensor, and dedicated sun sensor MCU. Four of the side panels also have burning transistors used to deploy solar arrays, but the EPS mainboard has no control over this. SP subsystem generally is always active, but the EPS can turn off the 3.3V supply for power cycling purposes.

Another critical subsystem of the satellite is the communications subsystem (COM), which gives us the possibility to communicate with the satellite, receive data, and provide software updates for the satellite. EPS provides COM with 3.3V as well as the MPB. There are no dedicated load switches present on the EPS mainboard for this subsystem. The load switches are located on the COM subsystem itself, controllable by the EPS mainboard MCU. The leading consumer of the COM is the power amplifier, which is a part of the transmit chain that amplifies the signal. However, it consumes large amounts of power only for brief periods when the subsystem is transmitting.

The on-board computer (OBC) subsystem is the central processing unit on the satellite, and it is responsible for the processing of telecommands, monitoring of the satellite health, processing algorithms for the attitude determination/control system, and compression and storage of mission data for most of the payloads [36]. OBC is supplied with 3.3V, which is provided by the EPS mainboard.

Star tracker (ST) is a subsystem that takes photos of stars and compares them to the database of known stars, and from this information, it is possible to determine the satellite's attitude. It is a powerful attitude determination tool but also consumes a lot of power. It is supplied with the MPB of the satellite through a load switch located on the EPS mainboard. ST converts MPB voltage to 3.3V. The power-related information of the ST was obtained from the developed prototype board, and the conversion efficiencies of various voltage conversion steps present. [37]

RW210 reaction wheels by Hyperion Technologies are a part of the attitude and orbit control system (AOCS) of the satellite. There are three reaction wheels present on the EC2 satellite, and they can operate at voltage levels from 3.25V to 3.5V. [38] The product flyer references a different model of this device, which has slightly different power characteristics than the model used on EC2. The author was not able to find published data of the model used on EC2.

Various estimated power requirements of EC2 subsystems and their modes can be seen in Table 2. The data was obtained mainly by studying different papers, available system designs, and available test results. At the moment, the parameters of the EPS engineering model have been based on this data. However, this data is only an estimate, and more precise parameters have to be set when satellite subsystems are assembled and operational. Only the consumption of systems is included that is related to the operation of the EPS mainboard.

Similarly, also the power requirements and modes for payloads can be seen in Table 3. The data was primarily obtained from unpublished sources. Datasheets for commercial payloads - high-speed communications (HSCOM) payload and cold gas propulsion (CGP) payload, were studied to determine the power consumption levels. However, due to non-disclosure agreements, this data is not referenced or explained. Generally, the payloads are supplied from the MPB, with few exceptions. CRE payload requires 3.3V, the HSCOM and CGP payloads require an additional 5V power supply. In HSCOM, the 5V is obtained on the battery management board with an additional switching regulator. The CGP payload also requires 5V, but the voltage difference from MPB is not that large, and the consumption is relatively low. Thus this voltage can be obtained with a linear voltage regulator that will not cause significant power losses.

Subsystem	Voltage, V	Estimated Consumption, mW	Mode
COM	3.3	400	Transmit
	MPB	3000	
	3.3	130	Receive
	MPB	650	
OBC	3.3	560	MCU operation with peripherals
		75	Sensors
ST	MPB	4370	Image Acquisition
		2822	Image Processing
SP	3.3	40	1x SP active
		102	1x SP active + sun sensor
		250	1x ICP transmit
		10	1x SP idle
AOCS	3.3	1000	1x Reaction wheel maximum consumption

Table 2. Power requirements of EC2 subsystems

Subsystem	Voltage, V	Estimated Consumption, mW	Mode
CGP	5	200	-
	MPB	6000	-
HSCOM	5	5000	-
CRE	3.3	<300	Active
EOP1	MPB	420	Idle
		1425	Image Acquisition
EOP2	MPB	420	Idle
		1425	Image Acquisition
E-Sail	MPB	5500	Wire burning (One time occurance)
		160	Plasma brake mode
		800	E-sail mode

Table 3. Power requirements of EC2 payloads

3.1 Requirements for the ESTCube-2 Power Distribution Engineering Model

Different system and design requirements were introduced for the engineering model of ESTCube-2 power distribution electronics. Also, the previous recommendations will be considered, and previous designs will be conserved in cases where new requirements have not been introduced. All the proposed requirements can be seen in the following list:

- STM32L4 will be used as the main control unit of the EPS mainboard

- It will be possible to power-cycle[2] the EPS mainboard MCU

- CY15B104Q and CY15B104QSN will be used as the memory storage devices of the EPS mainboard

- Power requirements of different subsystems and payloads will be met

- EPS mainboard engineering model will convert MPB voltage level to 3.3V

- The path loss for the 3.3V supplied to other subsystems in general should not exceed 100mV at maximum estimated consumption

- EPS mainboard will supply CGP payload with 5V

- Current limiting will occur within the device characteristic values

- Current and voltage measurements will occur within the expected margins based on used component tolerances

- EPS mainboard will be able to control battery management circuitry

- EPS will be able to communicate with other subsystems

- It will be safe to integrate the EPS main board along other systems of the satellite (figure 4.)

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[2]Process where a device is turned off and then by cutting off the power

4 EPS Devices and Parameters

4.1 Current State of the EPS Mainboard

Detailed visualization of the EPS engineering model electronics, including most recent devices and connections, can be seen in figure 6. Control electronics of the EPS engineering model consist of an MCU (STM32L496), two transceivers (LTC2850), two analog-to-digital converters (MAX1231BETI+), two ferroelectric random access memory (FRAM) devices (CY15B104Q and CY15B104QSN), and a real-time clock (RV3049-C3). Additionally, another ADC is also located on the battery management board that has connections with the EPS mainboard MCU. Control circuitry operates at 3.3V, which is mainly supplied by two LT3045 LDO devices in parallel. The 3.3V supplied by these devices are separated from the other satellite subsystems with a diode, as shown in the upper part of figure 6. Additionally, the EPS mainboard contains the signals for battery management circuitry, however, these signals are not included in the figure 6. Also, in the lower part of the same figure, the voltage regulation and power distribution steps can be seen. Voltage regulation for the HSCOM payload occurs on the battery management board.
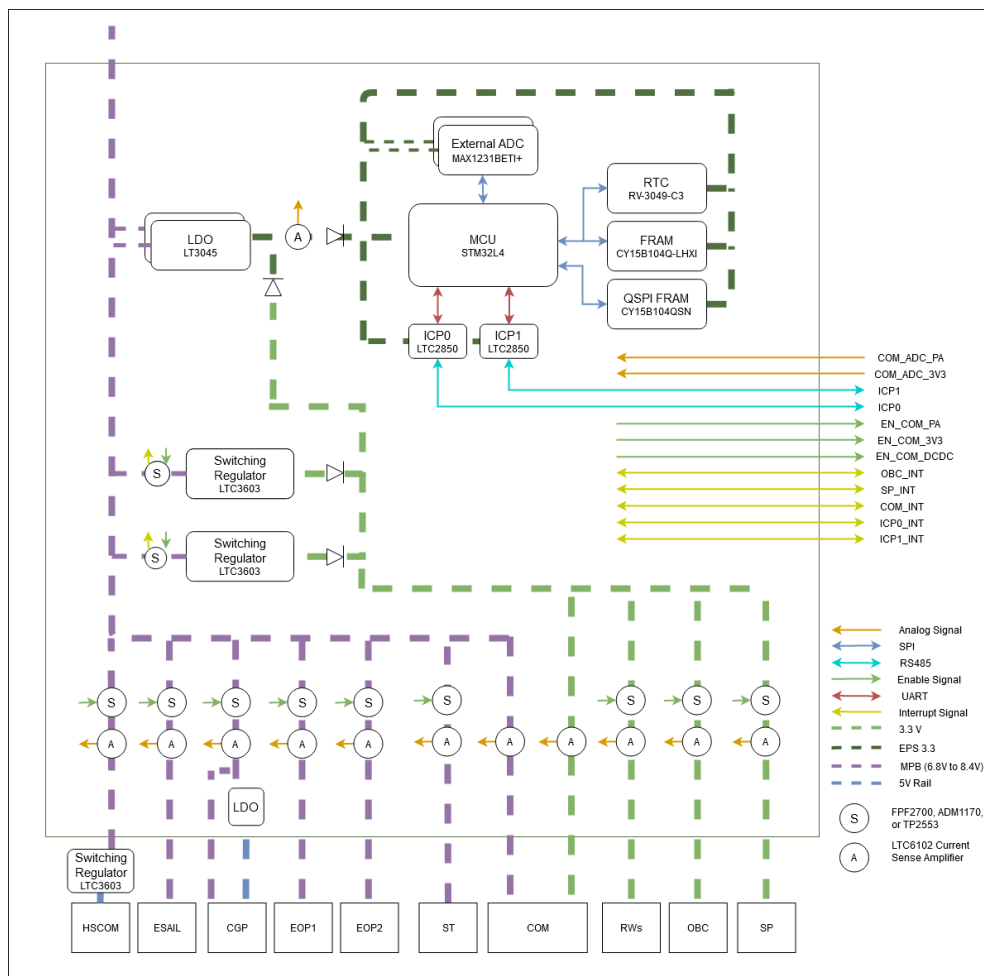

Figure 6. Block diagram of the current state of the EPS mainboard. Solid arrows represent signals and their direction. Dashed lines represent power connections

4.2 New Devices

In the development process of the engineering model for the ESTCube-2 power distribution electronics, a new MCU has been integrated within the system. The previously used MSP430FR6989 MCU device was changed to STM32L496 MCU by STMicroelectronics. This decision was based on maintaining consistency of devices across different satellite subsystems because this specific device is also used on COM and SP subsystems. COTS ARM®32-bit Cortex®-M4 architecture has also been successfully tested for radiation equivalent to the one present in the LEO. [39] ESTCube-2 should experience similar radiation levels. This is a positive note, however, it does not indicate the reliability of the STM32L4 microcontroller family in the space environment. The author was not able to find any information of the device's radiation tolerance. The new device is a low-power device that features an ARM®32-bit Cortex®-M4 central processing unit that can support frequencies up to 80 MHz. The device has 1 mega-byte flash memory, which is almost eight times more than in the previously used MSP430FR6989(128 kilo-bytes), and 320 kilo-byte static random access memory. The 100 pin, low profile quad flat package STM32L496 is being used for the EPS engineering model, where 2 SPI, 1 QSPI, and 2 UART interfaces are being utilized. [40]

Additionally, two new FRAM devices have been implemented. The two FM25V20 FRAM devices were swapped to CY15B104Q and CY15B104QSN, both with 512 kilo-byte storage space. This decision was also based on maintaining the consistency of devices between different subsystems on EC2. FRAMs are non-volatile memory devices based on the ferroelectric material as the information storage medium, which in general are resilient against radiation and magnetic field upsets. [41]

Two new MAX15006BATT+ low-dropout regulators (LDO) devices by Maxim Integrated were also implemented to supply CGP payload control electronics with 5V and up to 40mA. The guaranteed output current for this device is 50mA. Component de-rating for space applications was considered when choosing the device, where the maximum output current experienced is below 80% of the device's rated value. [42] This device does not have any particular radiation tolerance data available. However, it is meant for automotive purposes, which indicates its reliability. For additional robustness, two of these devices have been connected in parallel so that the EPS mainboard can continue supplying CGP with 5V if one device fails.

A configuration of a capacitor, a resistor, and a MOSFET was added so that the MCU could control the enable signal of the LT3045 LDO devices that supply the EPS logic circuitry with 3.3V. The goal of this configuration was to perform self-induced power cycling by the MCU. This also allows to turn off the LDO and source the 3.3V from the more efficient step-down converters and avoid the large ground currents of the LT3405 devices. The schematic of this circuit can be seen in figure 7., where the "POW_CYC_EN" is the signal from the MCU, and the "LDO_EN" is the signal tied to the enable pins of both LT3045 devices. When MCU pulls the "LDO_EN" high, the capacitor and the MOSFET gate will start to charge, and when the gate-source threshold voltage of 1.6V (typical) is reached, the MOSFET source-drain will close, allowing the current to pass through. This will lead to voltage potential to drop on the enable pins

of the LT3045 devices, effectively turning them off. When this occurs, the MCU will continue the operation for a brief period of time as the current can be sourced from the capacitor banks[3]. When the supply voltage falls below a certain voltage threshold, 1.71 V, the MCU is expected to turn off based on the characteristics of this particular device. [40] When the device is turned off, the general-purpose pins of the MCU enter the high impedance mode, which will cause the capacitor in the schematic visible in figure 7. to discharge through the $100k\Omega$ resistor.

When the voltage on the gate pin of the MOSFET falls below the gate-source threshold of 1.6V (typical), the drain-source of the MOSFET will open, allowing the LT3045 devices to turn on and start supplying 3.3V to the MCU. Equation 3. can be used to obtain the time to discharge a capacitor to a specific voltage, where v is the target voltage, V is the initial voltage, t is time, R, is the resistance, and C is the capacitance. [43]

$$v = V \cdot e^{\frac{-t}{RC}} \implies t = ln\frac{v}{V} \cdot (-RC) \qquad (Eq.\ 3)$$

The used values for the resistor connected to the electrical ground (GND) and the capacitor are $100k\Omega$ and $1\mu F$, respectively. To achieve the 1.6V to open the MOSFET, it would take approximately 72 ms, meaning that LT3045 would be turned off during this period. However, the actual result is expected to be slightly different considering the tolerances of the components and the devices and the fact that the supply voltage will be lower than 3.3V due to the path losses.
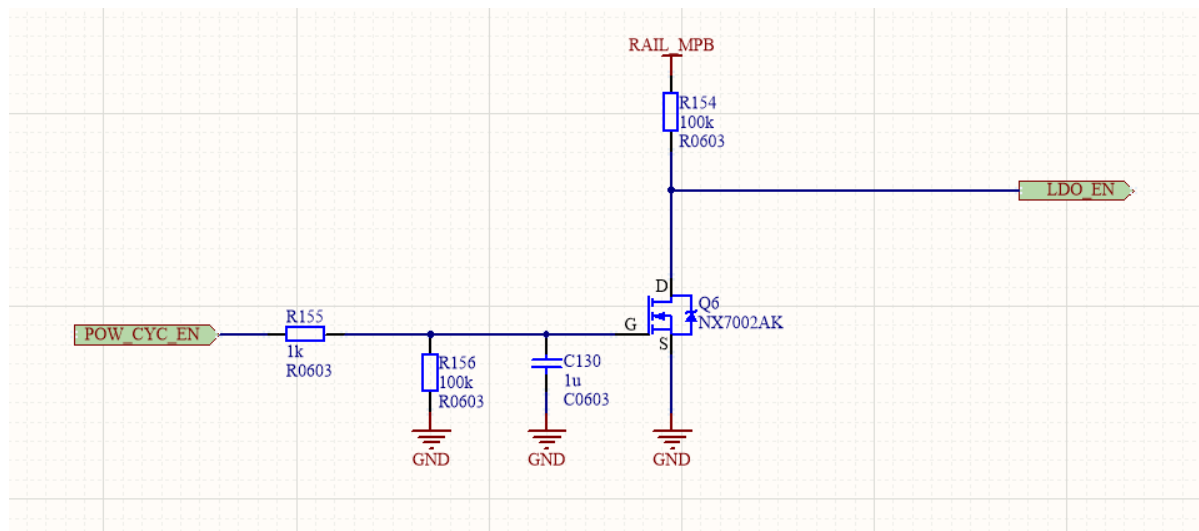

Figure 7. Schematic of power cycling logic for the main MCU

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[3]Capacitor bank are capacitor or capacitors connected in parallel or series with a purpose to store electrical energy

4.3   Load Switches

Several different load switch devices are used to cut off power for specific systems on the EPS mainboard. Previously recommended and tested devices were implemented within the engineering model - FPF2700, ADM1170, TPS2553. All of these devices also include current limiting abilities. The current limit for a specific system was chosen based on the maximum estimated consumption of the system with 20% margin and the lowest value at which the current limiting could be enabled, depending on the device's characteristic tolerance.

Following information in this paragraph is taken from the FPF2700 datasheet. [44] Only one parameter can be set in the FPF2700 load switch - the current limit programmed by a resistor. The device's current limit tolerance is 20%, which was taken into account when choosing the current limit so that the device wouldn't open the switch when still in the expected power consumption range. Nominal current limit can be set with the equation 4.

$$I_{lim}(A) = \frac{277.5}{R_{set}(k\Omega)} \qquad\qquad (Eq.\ 4)$$

Following information in this paragraph is taken from the ADM1170 datasheet. [45]. In the ADM1170 solution, the circuit breaking functionality is achieved by combining a sense resistor, the ADM1170 device, and a MOSFET. If the voltage potential on the "ON" pin of the ADM1170 is over 1.3V (typical), the device closes the MOSFET switch and the current can pass through. If ADM1170 senses voltage drop across a shunt resistor that exceeds 50mV (typical), it starts to charge a timer capacitor with a constant current. Once a specific voltage potential is reached on the capacitor, the ADM1170 opens the MOSFET switch, stopping the current flow. It also has the soft-start functionality to avoid large inrush currents, which is achieved by charging a another capacitor. In this case, the current limit is proportional to the voltage across the capacitor. For systems where the ADM1170 solution was used, the soft-start and the timer was set to 2.2ms as no system start-up information was available. An exception is HSCOM, where the soft-start was set to 10ms. Three different parameters can be set for the ADM1170 device:

- Current limit, I_{lim}, for the system can be set by choosing the resistance of the sense resistor, R_{sense}, as shown in equation 5.
$$I_{lim} = \frac{50mV}{R_{sense}} \qquad\qquad (Eq.\ 5)$$

- The time period, t_{ss}, between detecting current extending over the limit and opening the MOSFET can be set with equation 6.

$$t_{timer} = 1.3 \cdot \frac{C_{timer}}{60\mu A} \qquad\qquad (Eq.\ 6)$$

- Duration of the soft-start, t_{ss}, can be controlled by choosing another capacitor, C_{ss}, as indicated in the equation 7.

$$t_{ss} = \frac{C_{ss}}{10\mu A} \qquad\qquad (Eq.\ 7)$$

TPS2553 load switch device was used on two occasions - for turning on and off the OBC subsystem and the reaction wheels, which operate at 3.3V. Current limiting ability of this device is established with a resistor. The minimal current limiting value can be calculated with equation 8. [46]

$$I_{lim}(min)(mA) = \frac{22980}{R_{lim}^{0.94}(k\Omega)} \qquad (Eq.\ 8)$$

4.4 Current Measurements

Current measurements on the EPS mainboard are done by LTC6102 current-sense amplifier, which is a device that measures a small voltage drop across a resistor and outputs a voltage that is proportional to the gain, that is established by the user. The output voltage is measured by an ADC with a positive reference voltage of 3V, and a negative reference as the GND. The parameters were chosen so that output voltage would be ~2.9V at the highest expected load conditions. All the following information in this section is taken from the LTC6102 datasheet. [47] Parameters for the desired operation of the device can be obtained with equation 9., where the V_{out} is the output voltage of the device, V_{sense} is the voltage drop across the sense resistor, R_{in} is the input resistance, and R_{out} is the output resistance.

$$V_{out} = V_{sense} \cdot Gain = V_{sense} \cdot \frac{R_{out}}{R_{in}} \qquad (Eq.\ 9)$$

The maximum allowed output current for the LTC6102 devices is 1mA, and the output voltage can go as high as the supply voltage. In the engineering model, the devices are powered from the MPB, so the output voltage could reach 8.4V. Based on this information, the output resistors with resistance values over $8.4k\Omega$ were considered to avoid output currents exceeding 1mA, although this condition is not expected.

The LTC6102 device has a typical input offset value of 0.003mV, which is the voltage that is sensed when there is no potential difference between the inputs. This offset should be consistent, but it does vary with temperature, and the maximum stated value of this offset is 0.035mV. This offset is amplified along with the voltage drop across the sense resistor and will affect the output voltage of the LTC6102 device. The output voltage is eventually measured by the ADC (MAX1231BETI+). To maintain the accuracy of the ADC measurement without additional calibration, the gain values of LTC6102 devices were chosen to be below 122.4, which would give an offset amplification <0.357mV, or half the least significant bit measurement of the ADC device. Furthermore, the resistor's resistance was chosen as small as possible to reduce power losses while still satisfying the previously described conditions. 1% tolerance resistors were chosen to program the LTC6102 devices. Additionally, a low pass filter consisting of a resistor and capacitor was added to start filtering out frequencies over ~ 159 Hz for each analog signal.

4.5   Parameters for Step-Down Converters

There are two LTC3603 step-down converters present on the EPS mainboard engineering model. They operate in a hot-redundant configuration, meaning that they are connected to the same output and operate simultaneously. Thus, they can share the load, and one can continue to operate if the other regulator fails. A proper inductor and capacitors have to be chosen to obtain a stable output voltage with a small ripple. The highest output current of these converters was set as 2A, based on current rating of the LTC3603 device and the de-rating of the plastic encapsulated ICs. [42]

Input capacitance of both of the regulators was chosen to reduce the input ripple voltage. equation 10. was used to determine the minimum ceramic capacitor capacitance. [30] The efficiency, η, was assumed to be $\sim 90\%$, considering the results from the previous papers describing the efficiency of LTC3603 converters. [33][1]

$$C_{min} = \frac{I_{LOAD} \cdot D \cdot (1-D)}{f_{SW} \cdot V_{P(max)}}$$

(*Eq. 10*)

$$D = \frac{V_{OUT}}{V_{IN} \cdot \eta}$$

Frequency is another critical factor in the switching regulator design. Frequency can affect the impedance of the capacitors that lead to larger ripple voltages and EMI. Switching regulator devices also have a specific minimum on time, meaning that the duration of the MOSFET pulses should be larger than this value. Otherwise, the output voltage regulation can be negatively affected and become unpredictable. In LTC3603 devices, this time can be as high as 115ns. The frequency is directly related to the on-time of the pulses, and the maximum usable switching frequency, f_{SW}, can be calculated with equation 11. [48]

$$f_{SW} \leqslant \frac{V_{out}}{t_{ON}(min) \cdot V_{in}(max)}$$

(*Eq. 11*)

An important value, which should be reduced as much as possible, is the ripple current so that the power dissipation in tantalum capacitors would be as low as possible, which in turn will increase their lifetime. Maximum allowed ripple current for tantalum capacitors changes based on the package size, capacitance, and the rated voltage. Ripple current can be calculated with equation 12. [34].

$$\Delta i = \left(\frac{V_{OUT}}{fL} \right) \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

(*Eq. 12*)

Following information and equations in this section is taken from the datasheet of the LTC3603 device and are device-specific. [34] Output voltage of the LTC3603 step-down converters can be programmed with a resistive divider consisting of two resistors. The two resistors are connected between the GND and the output voltage. The voltage level between these resistors is taken as the feedback signal for the converter. The output voltage can be obtained with equation 13., where the R_2 is the resistor between the feedback point and the output voltage and the R_1 is the resistor between the feedback point and the GND.

$$V_{out} = 0.6 \cdot \left(1 + \frac{R_2}{R_1} \right)$$
(*Eq. 13*)

The usable frequency range for LTC3603 step-down converter is from 300kHz to 3MHz. The frequency is programmed by choosing an appropriate resistor value, R_{osc}, and equation 14.

$$R_{osc} = \frac{1.15 \cdot 10^{11}}{f(Hz)} - 10 \cdot 10^3$$
(*Eq. 14*)

5 Engineering Model Design

There are specific spatial restrictions in the EPS mainboard engineering model. Firstly, the board outline is restricted by the general satellite dimensions, which results in a 94x94 mm square shape. The location of the ST camera and the two reaction wheels (RW) results in cutouts leading to the final board outline visualized in figure 8. There is also component height clearance, which is 4mm for both top and bottom layers arising from a distance between other boards present in the PCB stack.

The red areas in figure 8. represent allocated space for different functional blocks of the EPS mainboard. Each functional block contains specific devices that have specific functions within the system. The goal of the proposed placement of each block was to use the space as efficiently as possible, separate analog signals from digital signals as much as possible, place the switching regulators as far as possible from other devices, keep the power distribution circuitry close to the connectors.
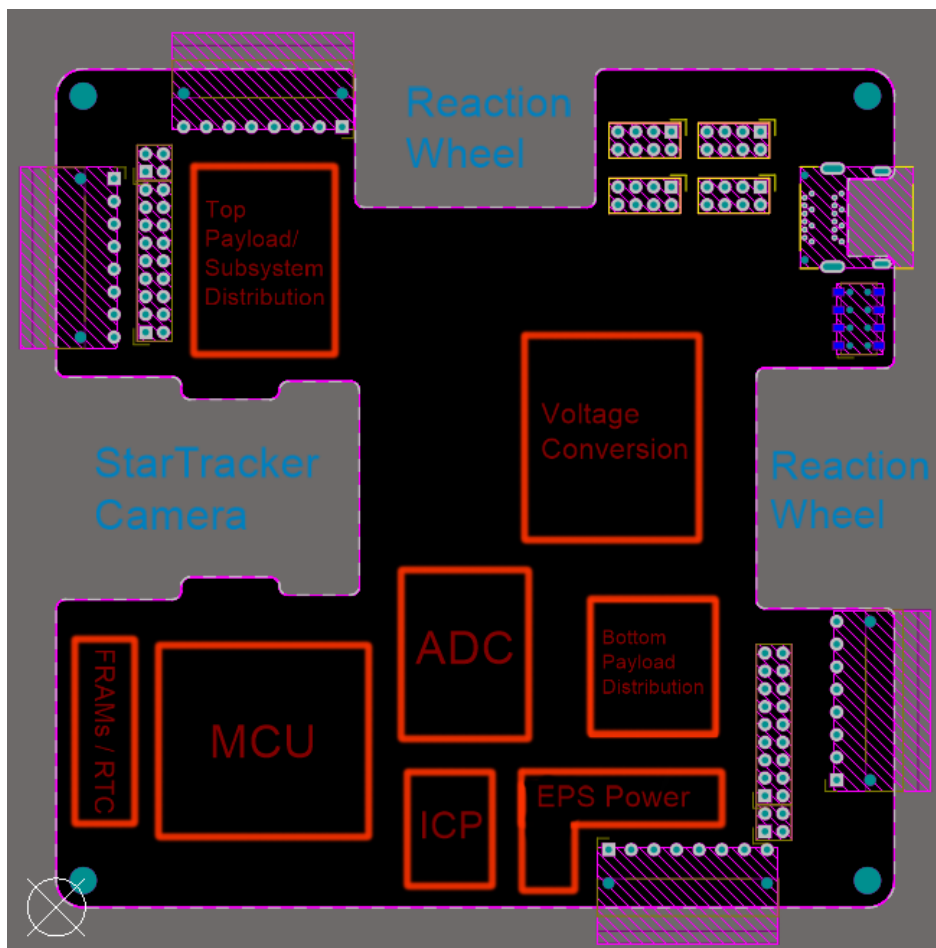

Figure 8. EPS mainboard engineering model outline, connectors and space allocation

5.1 Connectors

There are two connectors for the BUS, four connectors to connect with the side panels, and four connectors connected with the battery management board. Additional connectors are meant for debugging and software upload purposes, battery charging, and enabling different satellite modes. Connectors and their locations are fixed as any changes would lead to misalignments between other boards, and it would not be possible to assemble the boards correctly. Connector signal allocations are also fixed because changing these signals results in changes in other subsystems. Frequent changes of signal allocations increase the probability of inconsistencies between different subsystems. However, when the changes were unavoidable in rare cases, it was done by communicating with other subsystem engineers. Exceptions are the access port connector, battery management connectors, and debugging connectors, for which some amount of freedom can be taken when allocating signals.

5.2 Layer Assignment

EPS mainboard PCB has six layers in which signals can be routed. Each layer was assigned a general function, which was considered during the designing process. PCB layers can be seen in the Appendix 1. Following list provides a description for each layer:

- Layer 1 was meant for the placement of components and also routing for short connections. Also, some of the higher frequency signals were routed on this layer so they can directly couple into layer 2.

- Layer 2 consists only of a GND polygon and serves as a low impedance path for the return currents.

- Layer 3 was meant for routing of analog signals. Additionally, it served as a layer for higher frequency signals because of its proximity to the low impedance layer. These signals were routed as far away as possible from the analog signals.

- Layer 4 consists of digital signals between different components and the MCU. These signals are mostly either fault or enable signals that do not involve high frequencies.

- Layer 5 consists of power traces that supplied power to different components on the board or provides power to the connectors.

- Layer 6 was meant for placement of components as well as routing short connections.

5.3 PCB Design Considerations

Several different design practices were considered when developing the PCB design of the engineering model to reduce the extent of EMI, maintain signal integrity, and also maintain the predictability and functionality of the system.

One very straightforward solution is to use as many GND vias[4] as possible. These vias provide a path for return currents to travel through the low impedance layer. Additionally, a separate via should be used for each GND pad present because this allows avoiding different signals sharing the same return path, which could cause cross-talk and common-impedance coupling. Additionally, GND vias were placed along the border of the PCB so that the external signals entering the cross-section of the board would couple into the electrical ground and avoid any signals leaving the board that could cause EMI for other systems of the satellite.

Another good design practice is to use the Kelvin connection for analog signal measurements, which can be seen in figure 9a. Traces, pads, and component leads have some finite resistance, and as current flows through the specific part, a voltage drop will occur. Kelvin connection avoids these losses by sampling the voltage as close as possible to the resistor. [49] For example, in the figure 9b. the sampled voltage would be slightly different because as the current runs through the pad and trace, there will be additional voltage drops.
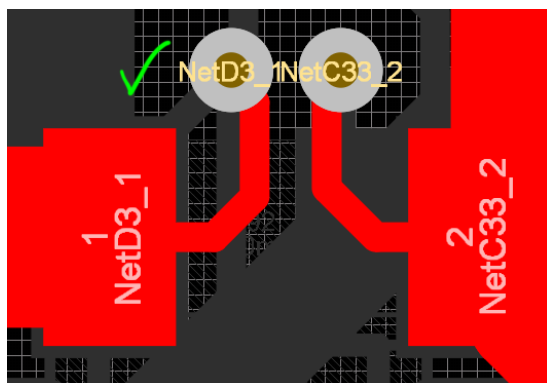
(a) Example of a Kelvin connection, where the traces for signal measurements are as close as possible to the shunt resistor leads
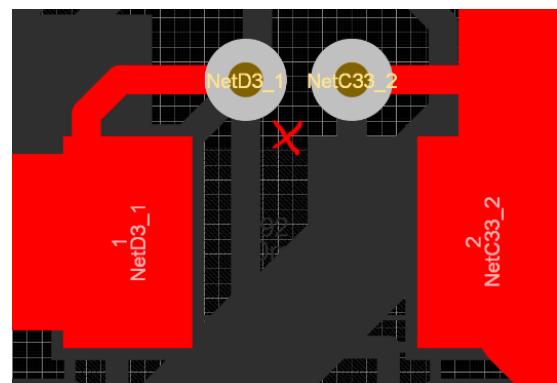
(b) Connection, where the traces for measurements are located further away from the shunt resistor

Figure 9. Examples of a Kelvin connection and an incorrect connection that could reduce signal quality

Decoupling capacitors are another common component that can be seen in digital circuits. Decoupling capacitors serves two purposes. One is to supply near-instantaneous current when there is a sudden change in the device's current consumption. The power supply is not able to provide this instantaneous current due to the parasitic inductances between the device and the source. The other reason is to shunt any high-frequency noise to the electrical ground. Other circuits or devices could cause this noise. It is important to place these capacitors as close as possible to the device; otherwise, as the distance between the device and the capacitor increases, so do the parasitic inductances.

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[4]Plated hole that connects different layers of the PCB

Ground vias are also placed on the thermal relief pads of different devices, allowing heat to be transferred away from the devices through heat conduction. Heat convection is negligible in the space environment due to the absence of the atmosphere. Also, the solder mask has been removed on the other side of the PCB, allowing trapped gasses to escape. Otherwise, as temperature increases, so does the pressure caused by gasses trying to escape to the vacuum environment. This can cause mechanical stress on the device connected to the board.

EPS engineering model involves larger current as power is supplied to other subsystems. Considering that traces that carry the current have some finite resistance, a voltage drop will be induced. So implementing wider and shorter traces was an important aspect when designing the engineering model. Also, as the power traces involve larger magnetic fields due to the movement of charges, they were separated from more susceptible signals, such as analog signals.

Also, the step-down converter layout and connections were approached with care. Suppose the components that support the device's function - capacitors, inductors, feedback resistors, and others, are placed without any considerations. In that case, it could cause serious EMI-related issues and degrade the overall efficiency and reliability of the device. The switching current loops have to be maintained as small as possible as described in Chapter 1.3.2. The design approach for maintaining the current loops in the step-down converter circuitry can be seen in figures 10. and 11. The drawn current loops in the figures only present a general idea when laying out different components on the PCB. It is not possible to prove if these are the current paths present in the real circuit, and only the performance of the device can indicate if the proposed design is appropriate. Switching regulators themselves have signals that are susceptible to interference, for example, the feedback signals. It is essential to separate these signals and their return paths from the power-related currents. Another suggestion for the connection of step-down converters was to take the feedback point after the near-ideal diode configuration that involves a MOSFET as the pass element. [33] This should compensate for the voltage drop across the MOSFET. Two options were implemented in the engineering model - feedback point at the output of the step-down converter circuit or feedback point after the near-ideal diode configuration. Another recommendation was to place the inductor directly below the switching regulator IC [1]. However, his recommendation was not followed to avoid switching currents going through the vias, which has some parasitic inductance and would radiate varying magnetic fields. Also, the bottom layer is relatively close to the COM subsystem and could cause EMI. Instead, the inductor was placed on the top layer as close as possible to the converter IC. There are two step-down converters present on the EPS mainboard engineering model. The layout and connections of both converters are almost identical, so the author expected a similar performance.
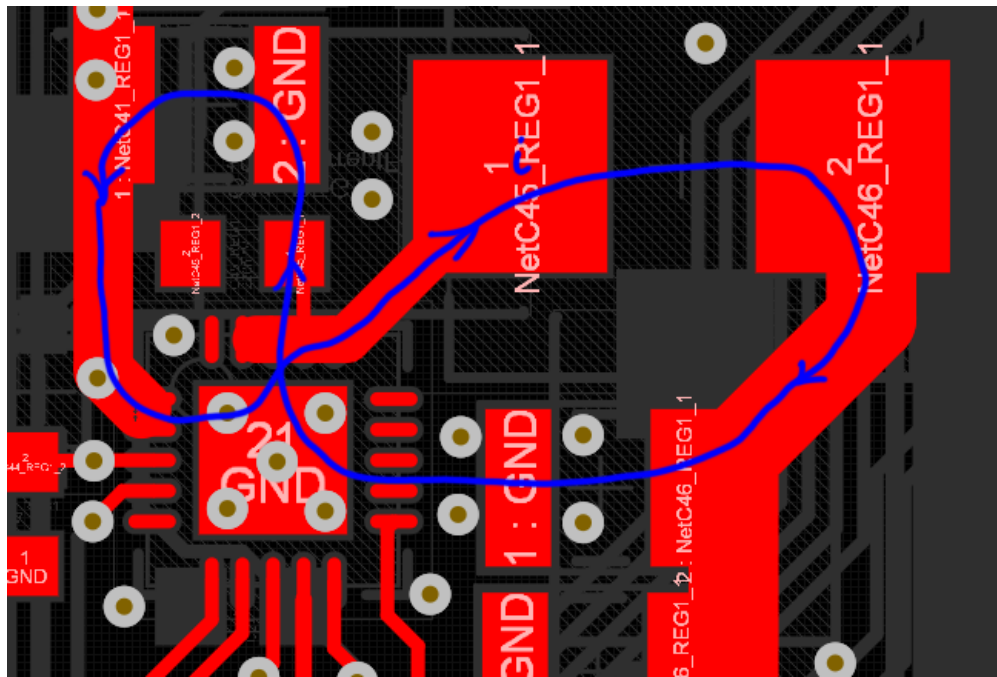
Figure 10. Current loop of step-down converter in the EPS mainboard engineering model, which is represented as the blue loop in figure 2. schematic
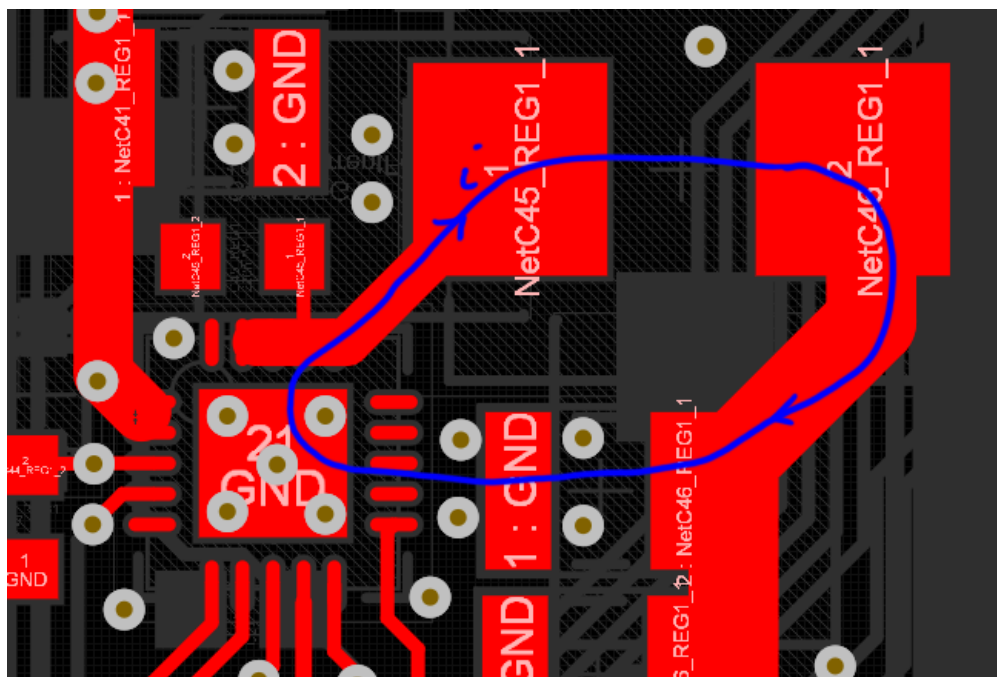

Figure 11. Current loop of step-down converter in the EPS mainboard engineering model, which is represented as the red loop in figure 2. schematic

6 Methodology

Initially, the schematics of the engineering model were developed based on the previous papers and prototypes related to the EPS power distribution electronics. EC2 power requirements and different devices present in the design were studied to set parameters in schematics accordingly. The printed circuit board was developed considering all the spatial restrictions and connections to other satellite systems. Both schematics and the printed circuit board design were developed with the "Altium Designer 18" software.

Efficiency of step-down converters was determined by varying the load current and measuring the input current, input voltage, output current, and output voltage. The input voltage was adjusted after each load current step to avoid losses within the wires. Three different input voltages were taken - 6.6V, 7.4V, and 8.4V. Currents were measured with two BM257 digital multimeters with a reading accuracy of $\pm$ (0.5% + 3mA). FLUKE 116 digital multimeter was used to measure the output voltage with a reading accuracy of $\pm$ (0.5% + 2mV). The DL24-PCB electronic load was used to achieve various load conditions. Load current was manually varied from 0 to 2A with 0.05A intervals. Final efficiency was obtained with the equation 15. Additional 20-21mA were consumed by other devices present on the board. This consumption was constant over the used input voltage range, and it was subtracted from the input current, I_{in}, used in the equation 15. The input voltage measurements did not consider losses in the load switch that is located before each step-down converter.

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} \cdot I_{out}}{V_{in} \cdot I_{in}} \qquad\qquad (Eq.\ 15)$$

The functionality of different load switches and current-sense amplifiers were determined by connecting the DL24-PCB electronic load in series with the particular power distribution step. The voltage across the load, the output voltage of the current-sense amplifier, and the current at which current limiting occurs were measured for each system power distribution step. Voltages were measured with the Fluke 116 digital multimeter, and the current measurement was performed with the BM257 digital multimeter. Also, it was determined if the MCU can turn off and on each load switch.

Initial software for the MCU was developed with ARM Keil µVision® integrated development environment, which also allows the control of the MCU registers while the device is operating. The software was uploaded to the device with the ST-LINK/V2 programmer by STMicroelectronics.

7   Results

The following section covers results from testing different devices present on the EPS mainboard engineering model. It has to be mentioned that these are only preliminary tests, which implies the general functionality of different devices, and if they operate within the expected margins. Further testing has to be implemented to determine a more accurate operation of the engineering model. The design of the engineering model has been finished, and the board has been manufactured and partially soldered. Some of the elements that are less crucial for the initial tests have been left unsoldered, for example, connectors to other subsystems. Also, the MAX15006BATT+ LDO devices remains unsoldered as they were not ordered at the time of the soldering. The current state of the EPS mainboard engineering model can be seen in figures 12. and 13. Some problems were noticed during the testing and soldering process, which are described in the following sections. They were fixed or they have to be fixed in the following revision.
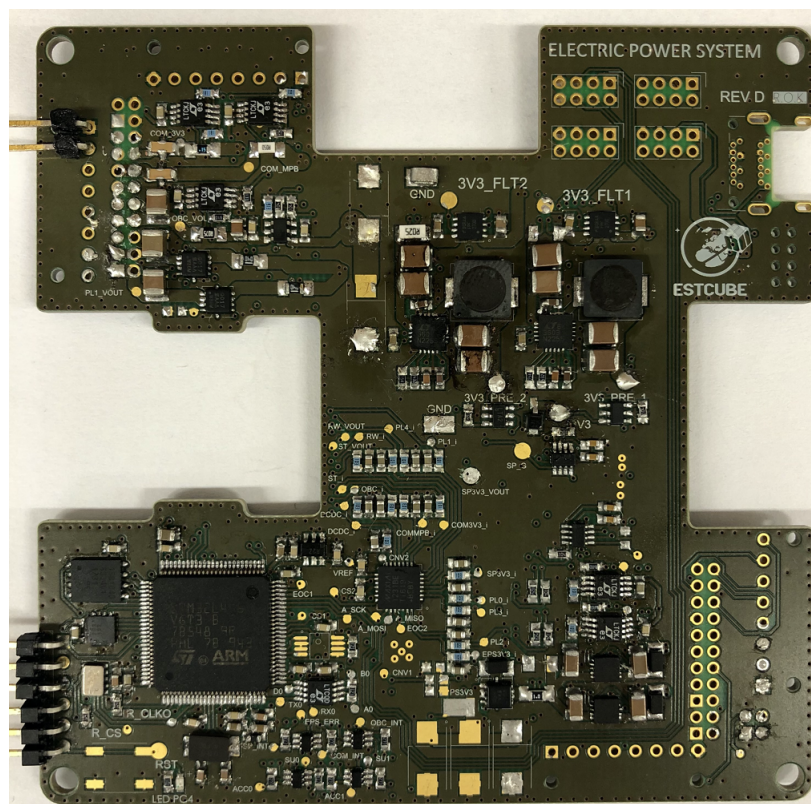

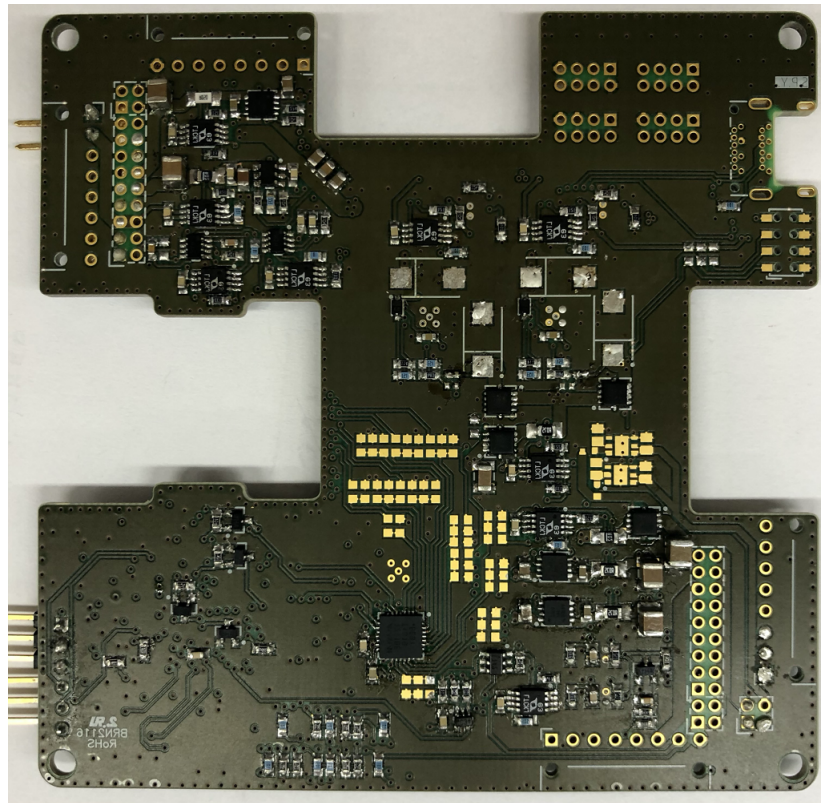**Figure 12.** Top side of the manufactured and soldered engineering model

Figure 13. Bottom side of the manufactured and soldered engineering model

7.1 Control Electronics

The primary device of the control electronics is the MCU, which has been flashed successfully and operates as expected. The software drivers for various control logic devices were not developed during the thesis. Thus it is not possible to determine if these devices are functioning as intended. Initially, the overall consumption of control logic devices was 42mA, extending over the expected consumption based on the available device characteristics. The LTC2850 has two modes, transmit or receive, and the mode is chosen by setting the appropriate logic level provided by the MCU. As the general outputs of the MCU by default are in the high impedance state, it was enough to make the LTC2850 transceiver enter the transmit mode and consume relatively large currents. The overall current consumption of the control logic was reduced to 22mA when the receive mode of the LTC2850 was enabled. This consumption can be further decreased by implementing low power and sleep mode for the various devices present. The consumption of the two LT3045 LDO devices that supply the control electronics with 3.3V consumes ∼10mA. This is quite large; however, it is within the characteristics of the device. [50] As this consumption was expected, a solution was proposed in the design to turn these devices off. However, these devices failed to turn off in the testing process and continued to consume power when the voltage level on the "EN" pin was below 1.24V - the typical voltage level to turn off the LT3045 devices. (voltage level was equal to 11mV). This result also indicates that the power cycling functionality cannot be tested as turning off the LT3045 devices is inherent to the proposed power cycling mechanism.

7.2 Step-Down Converter Tests

Both LTC3603 step-down converters were soldered, and their performance was determined under different load conditions. The used frequency for the step-down converters was ~719kHz. In the soldering process, the author noticed a mistake in the PCB design. The "BOOST" pin of the LTC3603 was not connected. This particular pin is responsible for increasing the voltage of the internal MOSFET gate to achieve a greater gate-to-source voltage difference and sufficiently close the switch. [34] Beacause this particular pin was not connnected, the device could not properly turn on, and there was no voltage present on the output. The author resolved this issue by soldering a small wire, connecting all the necessary components.

7.2.1 Efficiency Measurements

Efficiencies were obtained for both step-down converters operating simultaneously. Efficiency graphs under different input voltage and load conditions is visualised in figure 14. Throughout the applied load conditions, the efficiency remained fairly consistent, but it did slightly decrease as the difference between output and input voltages increased. The efficiency ranged from 89% to 92% at 6.6V input, 88% to 92% at 7.4V, and 84% to 91% at 8.4V input. The efficiency could be further increased if the voltage drop across the near-ideal diode configuration can be reduced or compensated. The obtained efficiencies remain consistent with the previous tests and are similar to the performance figures available in the LTC3603 datasheet. [1][33][34]
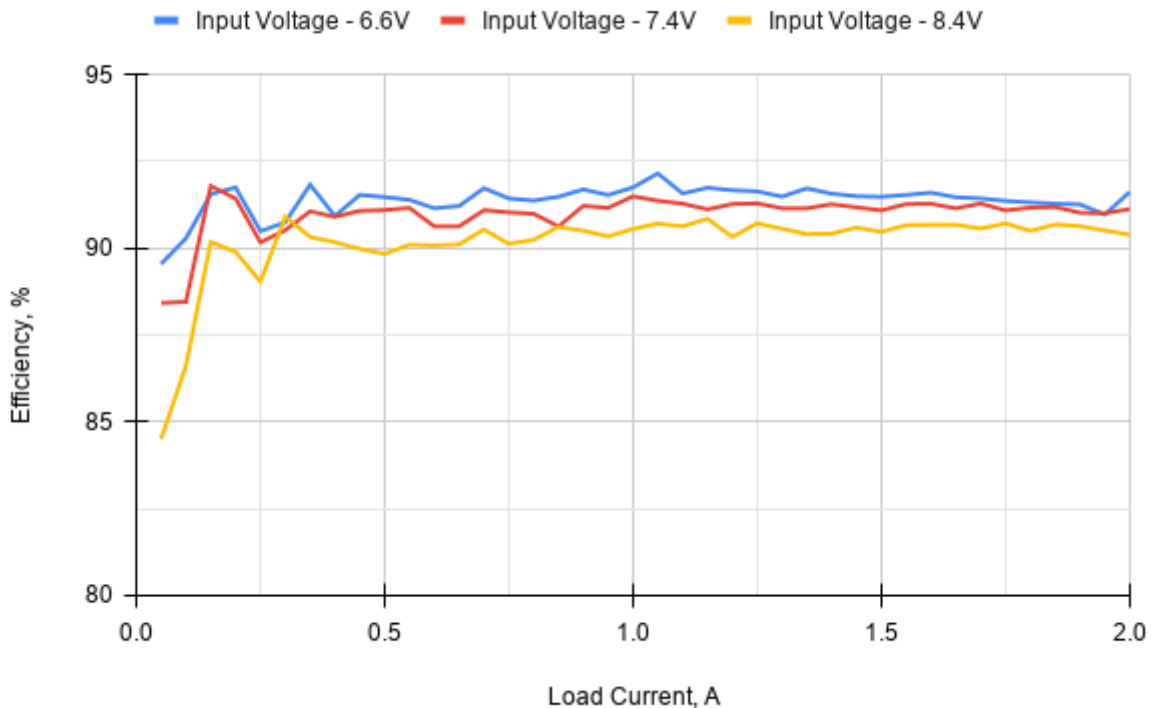

Figure 14. Efficiency measurements of both LTC3603 step-down converters operating simultaneously

7.2.2 Output Voltage Measurements

The output voltage of individual step-down converters and voltage after the near-ideal diode configurations were measured over different load conditions. The results are visualized in figure 15. The yellow line indicates the voltage response for the converter which had a design flaw (converter Nr1.), the Orange line indicates the voltage response for the converter that had no design flaws (converter Nr2.), and the blue line indicates the final output voltage after near-ideal diode configurations, where both converter outputs are connected. The expected nominal output voltage of both converters was 3.320V. The open-circuit voltage of converter 1. and converter 2. were 3.328V and 3.293V, respectively. The deviation from the nominal voltage and the difference between the output voltages most possibly is a result of the used 1% tolerance feedback resistors. Initially, all voltages decrease, but as the individual converter voltages converge to a specific value, the final voltage decreases linearly. This is due to the finite resistance of the MOSFET in the near-ideal diode configuration. The final voltage drops to 3.23V, which is quite severe. This voltage drop could be reduced by using a lower ON-resistance MOSFET. Another solution already present in the engineering model is to use the converter feedback point after the near-ideal diode, compensating for this severe voltage drop. However, when tested, one of the regulators ceased to function. A solution for this problem is yet to be found, but it has a great potential to avoid large voltage drops and increase the overall efficiency of the voltage conversion step.

Ripple voltage measurements were not included in the results as proper measurements and comparison could not be established due to late arrival of the boards and the fact that one of the converters had a design flaw that could affect its performance; however the author did manage to look at the output voltage waveform, were the ripple peak-to-peak voltage ranged from $\sim 30mV$ to $\sim 115mV$.
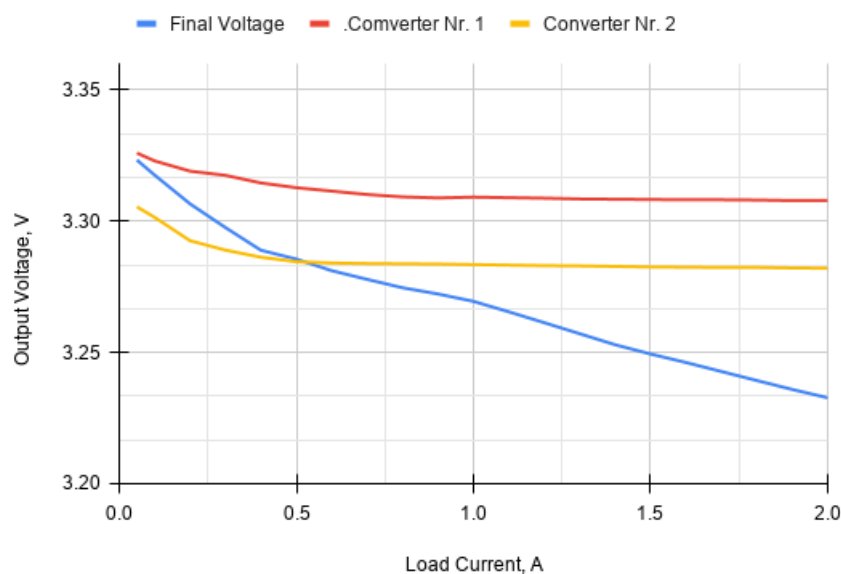

Figure 15. Different voltage measurements of the LTC3603 step-down converters

7.3 Power Distribution Tests

Each system's power distribution step has been tested, each step involving a load switch and a current-sense amplifier. An exception is the COM subsystem, which does not have particular load switches present on the EPS mainboard. The Table 4. contains the results of the performed tests. For systems that operate at MPB voltage levels, 6.6V were used as the supply voltage. For the systems that operate at 3.3V, the voltage obtained from the step-down converter was used (Output voltage of the converter under various loads can be seen in figure 15). The voltage across the load at maximum expected current consumption, current-sense amplifier output voltage, and the current, at which the current limiting would enable, was measured. The "Device" in the Table 4. represents the device with which the circuit breaking functionality is achieved, and the "Output voltage, V," represents the output voltage of the LTC6102 current-sense amplifier.

System	Device	Voltage at maximum load,V	Maximum load, A	Observed current limit, A	Output voltage,V
COM (MPB)	-	6.548	0.55	-	2.755
COM (3.3V)	-	3.214	0.31	-	0.026
OBC	TPS2553	3.233	0.25	0.28	0.000
ST	FPF2700	6.479	0.8	0.94	2.962
RWs	TPS2553	3.125	1.09	1.16	0.001
SP	ADM1170	3.236	0.55	0.58	0.000
CGP	ADM1170	6.451	2.21	2.36	2.956
EOP1	FPF2700	6.544	0.26	0.33	2.885
EOP2	FPF2700	6.546	0.26	0.33	2.874
HSCOM	ADM1170	6.529	1.01	1.15	2.941
E-Sail	ADM1170	6.528	1.00	1.15	2.960

Table 4. Power distribution results of the EPS mainboard engineering model

The MCU was able to control the circuit breaking for all the systems that had the circuit breaking functionality. In all cases, the current limiting was enabled in the expected range, which depends on the characteristic tolerances of the used devices. Similarly, the output voltage of the current-sense amplifier provided results within the predicted range for devices that operated at 6.6V, considering the used 1% tolerance resistors.

There are also several issues in the power distribution circuitry. The output voltage for reaction wheels (RWs) dropped to 3.091 due to the relatively large currents these devices could consume. The minimum voltage for the operation of RW210 by Hyperion Technologies is 3.25V.[38] The maximum load current was taken assuming that all the reaction wheels would be braking at the same time, which is a highly unlikely scenario, so in real life, these losses would be potentially smaller. Considering the blue line in figure 15. the output voltage at load $\sim 1A$ would already be approximately 3.268V, which is above the minimum operating conditions for the reaction wheels; however, this voltage is already very close to the minimum operating voltage of the RW210 reaction wheels.

TPS2553 and FPF2700 devices had voltage levels on the output even if the devices were turned off (the switch is open), and these voltages were able to withstand small currents. There was no output voltage for LTC6102 current-sense amplifiers for the systems supplied by the 3.3V level. The same issue was observed in the same LTC6102 device used to determine the current consumption for the EPS mainboard's control electronics that also operate at 3.3V level. Further investigation is required to determine the underlying fault.

8 Summary

This bachelor's thesis aimed to develop an engineering model for the ESTCube-2 power distribution electronics. This is an essential element of the electrical power system of the ESTCube-2 nanosatellite that is responsible for voltage conversion, power-related measurements, and managing the power path between the power sources and systems of the satellite.

Following tasks were completed:

- Continuation of previous work related to the ESTCube-2 power distribution electronics

- Implementation of new devices within the system

- Development of schematics based on previous prototypes and recommendations

- Printed circuit board has been developed, manufactured, and soldered

- Initial tests have been performed to determine the functionality of the proposed design

Several issues were already discovered during the testing and soldering process. Description and possible causes were given for some of the issues. These issues were either resolved or have to be resolved in the following revision.

Additionally, the thesis contains information, which can be helpful in further development of the ESTCube-2 power distribution electronics. It can be taken as a reference for tuning different parameters within a developed engineering model as more precise data related to the power requirements of the ESTCube-2 nanosatellite becomes available. Suggestions for further development have also been proposed based on the results of the initial tests. Additional testing, software development, and integration, among other subsystems, have to be performed to determine the overall functionality of the developed engineering model for the ESTCube-2 power distribution electronics.

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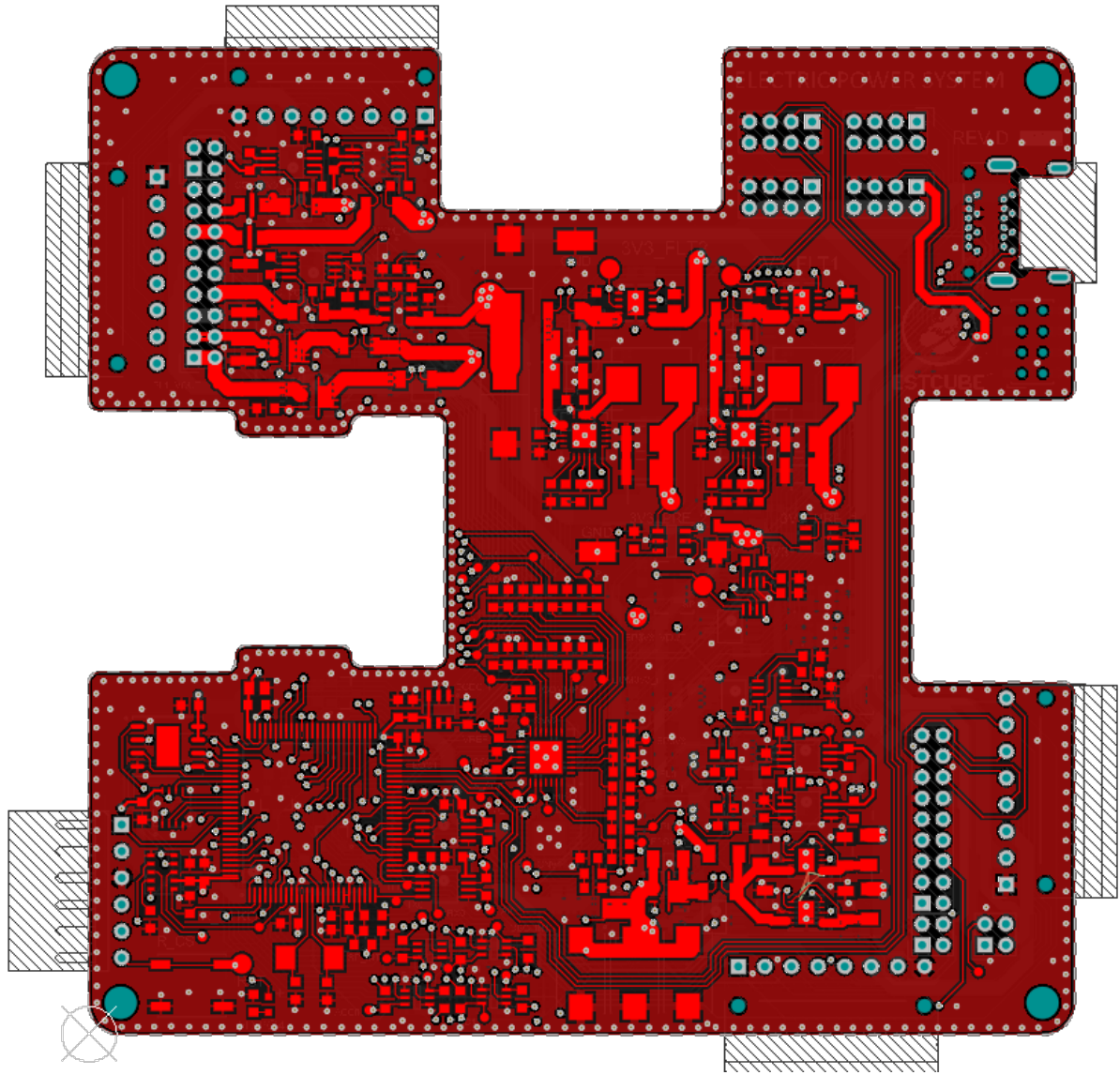# Appendix

I. Printed Circuit Board Layers
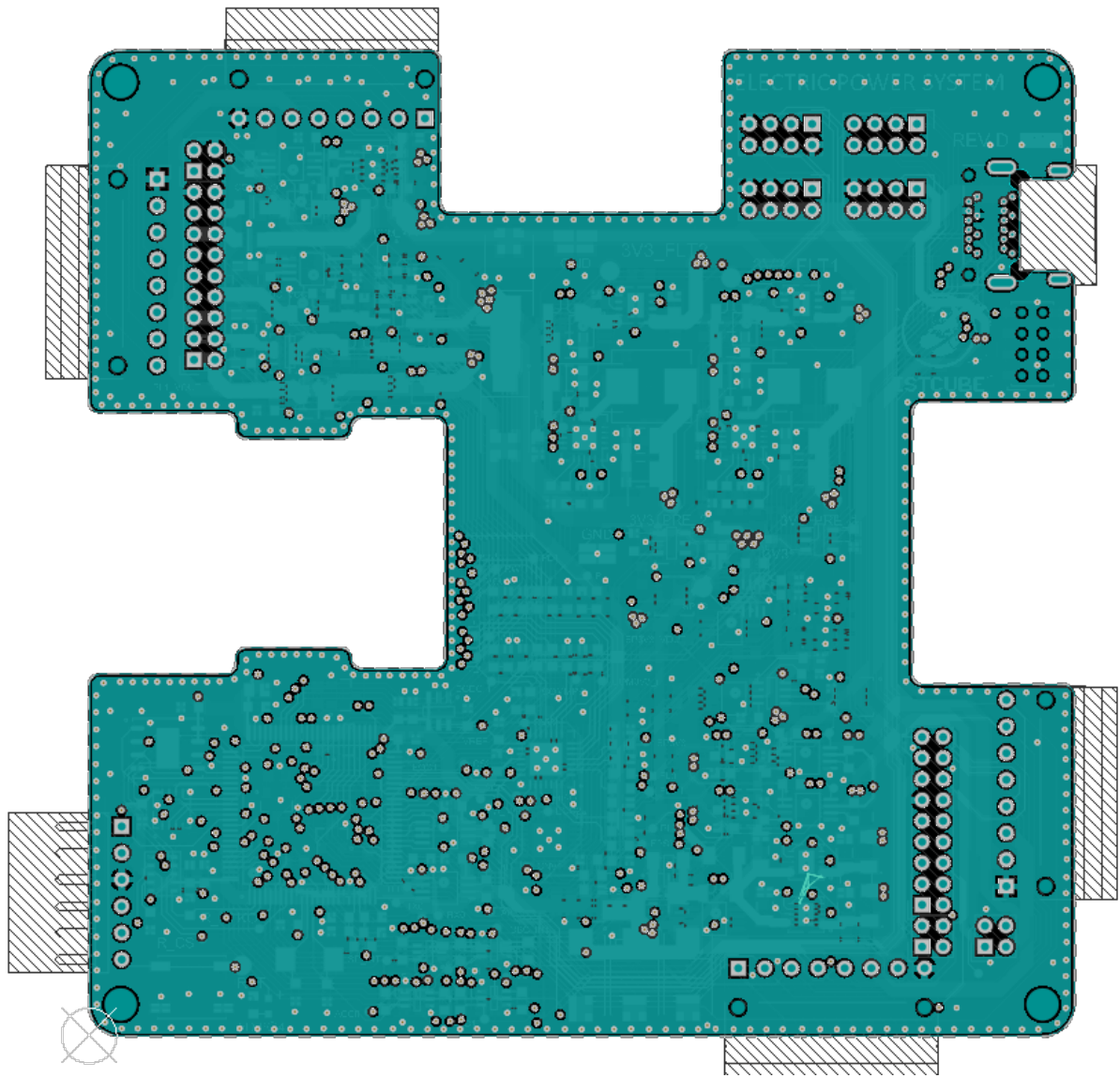

Figure 16. PCB Top Layer
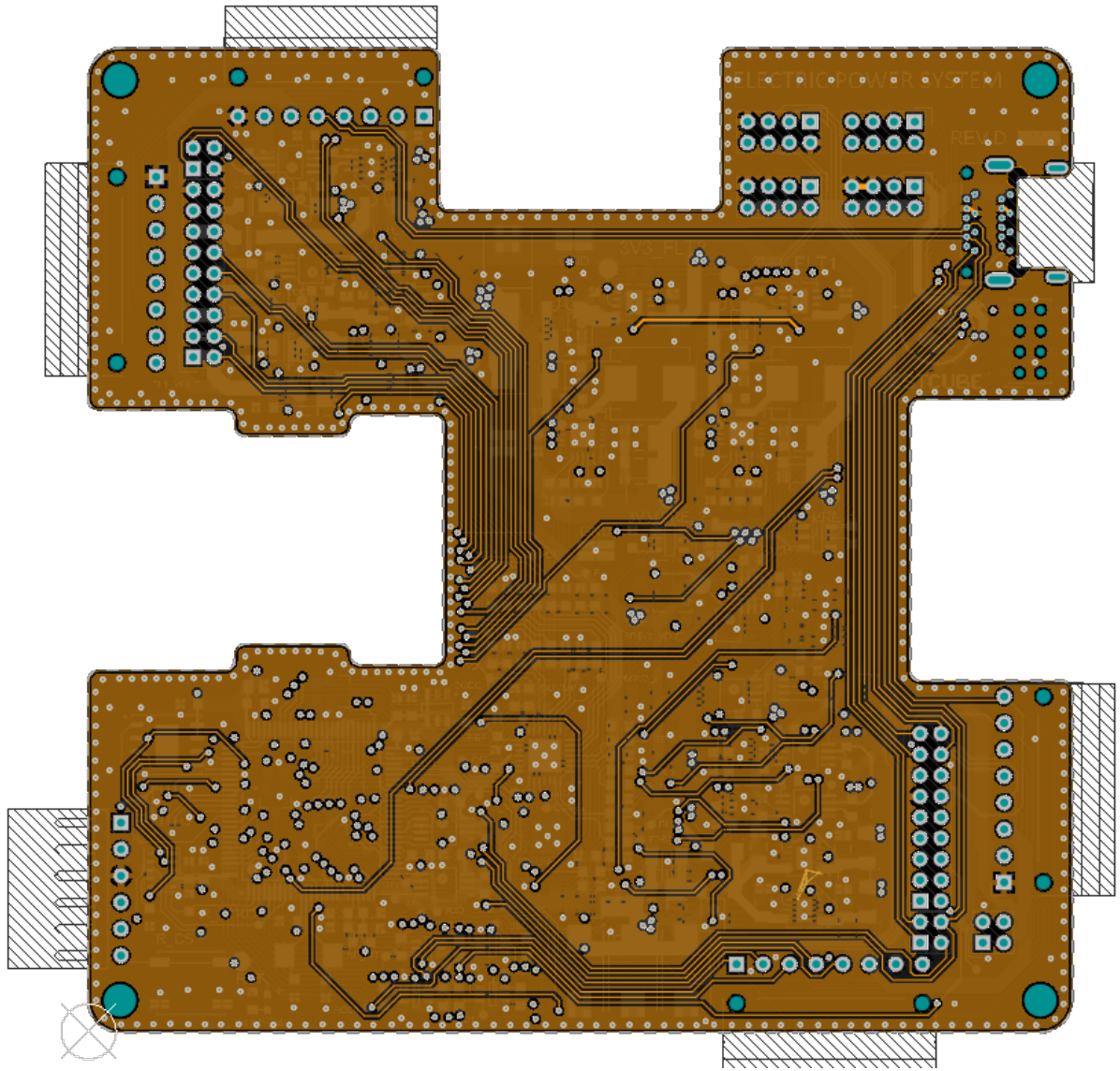
Figure 17. PCB Low Impedance Layer

Figure 18. PCB Analog Signal Layer
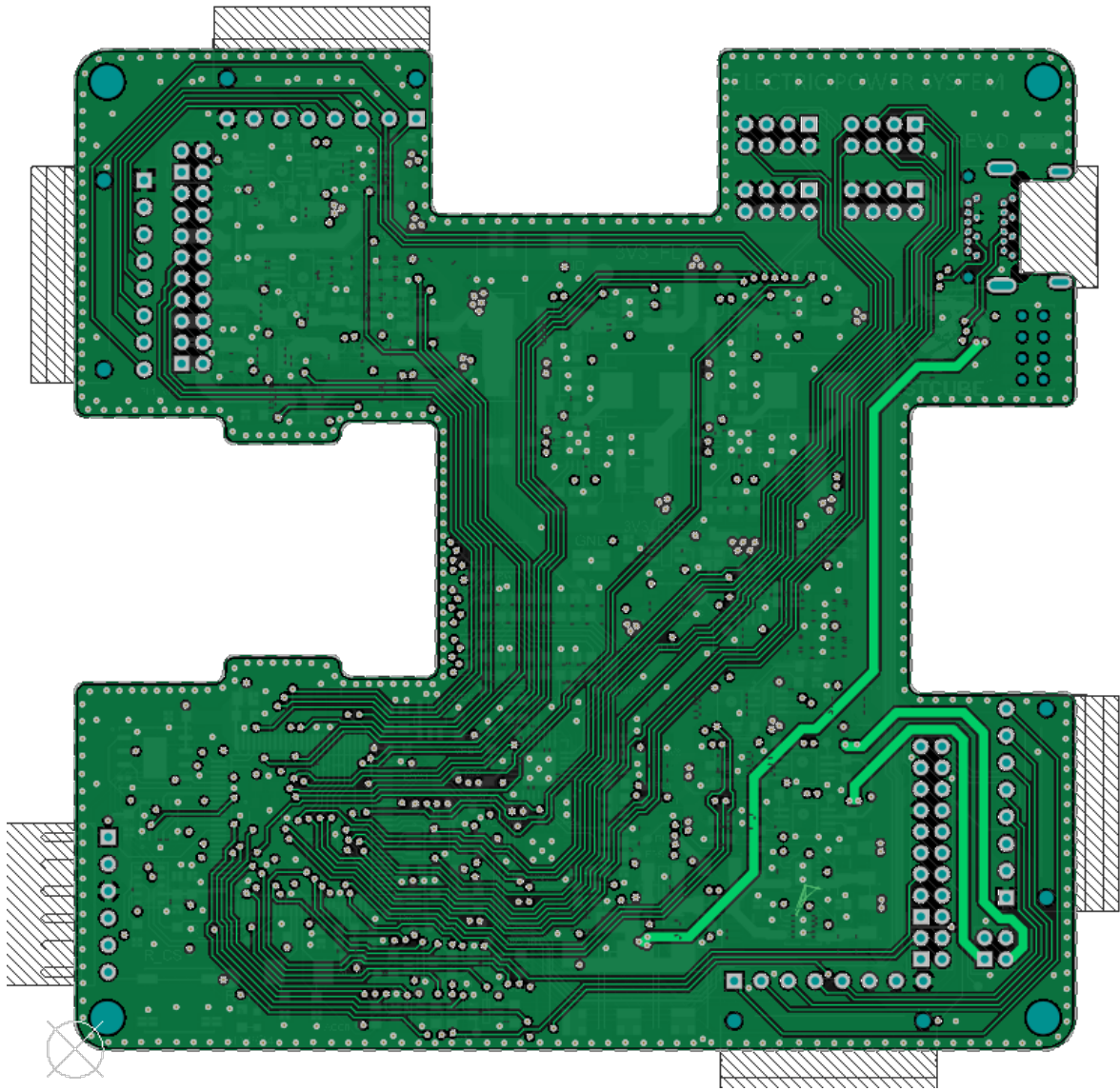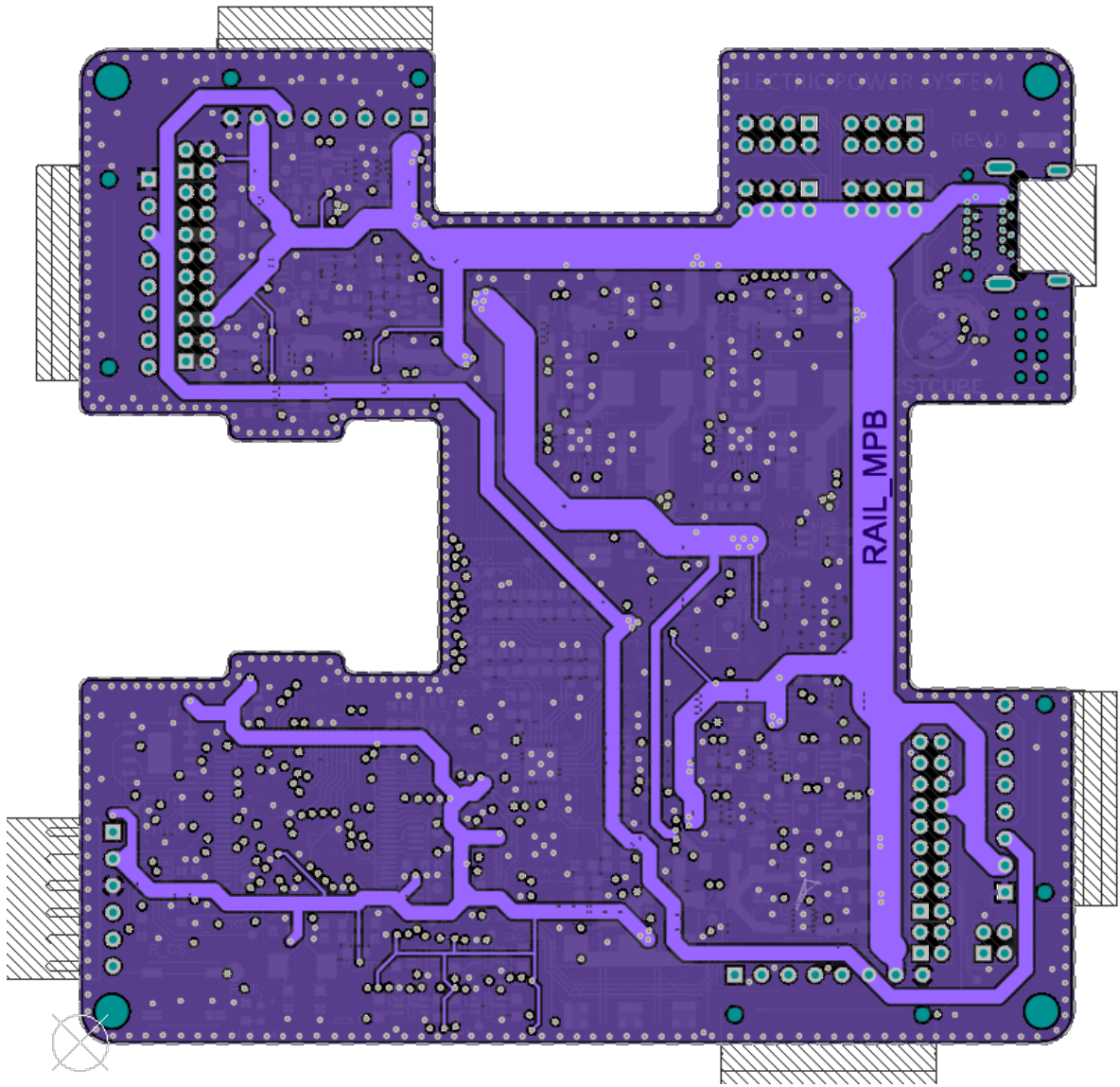
Figure 19. PCB Digital Signal Layer
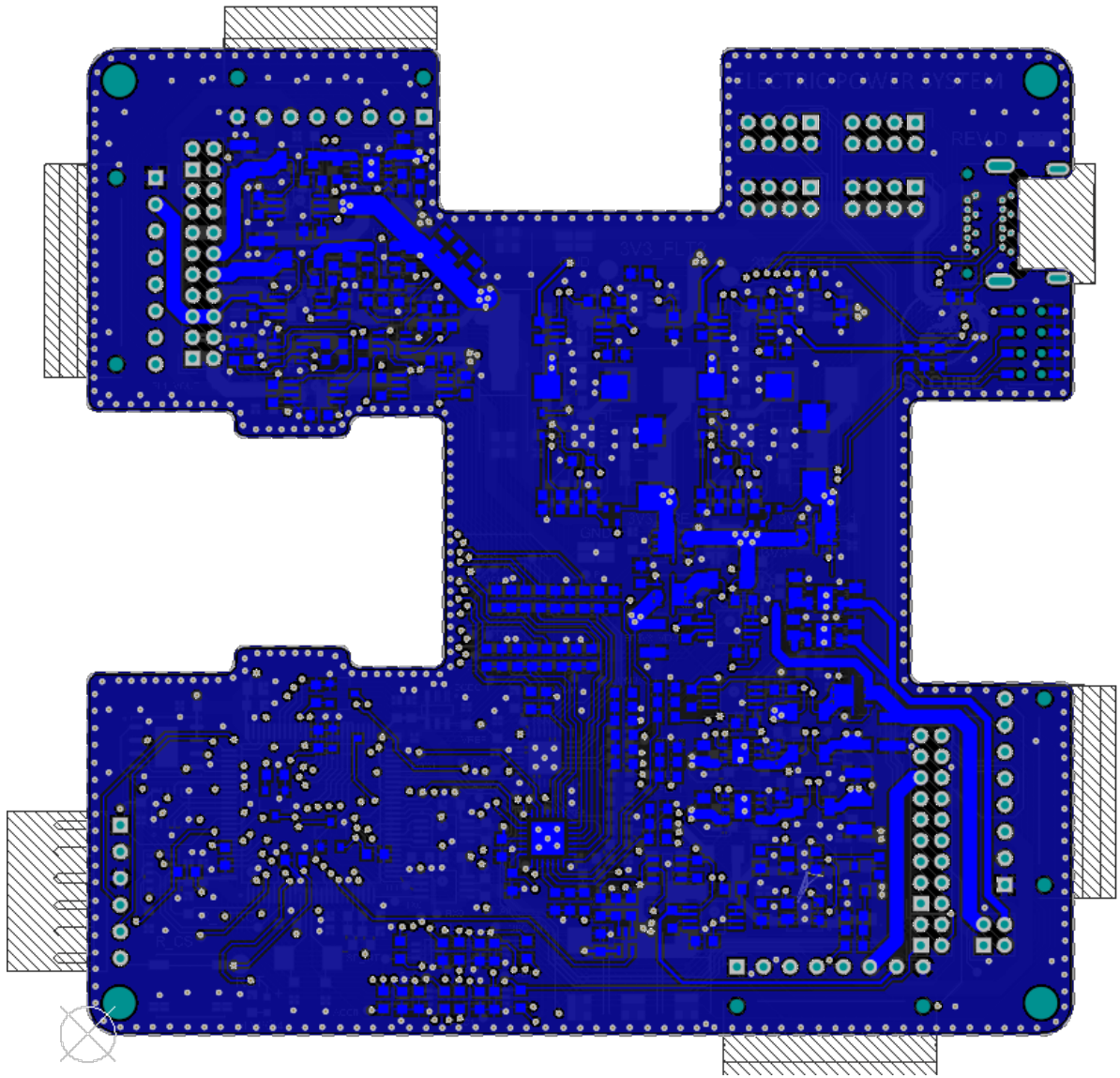
Figure 20. PCB Power Layer

Figure 21. PCB Bottom Layer

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Roberts Oskars Komarovskis
20/05/2021