Low power multicarrier- code division multiple access receiver on field programmable gate array

ABSTRACT

This paper presents a low power multi-carrier code division multiple access (MC-CDMA) receiver on field-programable gate array (FPGA). Most of the wireless application nowadays such as wireless sensor networks, portable computation and many more require a low power design. Time-division multiple access (TDMA) is used in most wireless receivers are not very efficient since they adopt scheduling technique. The first objective of this paper is to design and verify a low power MC-CDMA receiver and the second objective is to implement the MC-CDMA receiver on FPGA. MC-CDMA act as a processor with the ability to process transmit or receive data simultaneously over a single communication channel. The MC-CDMA design in this paper consists of pipelined FFT and combiner. The primary purpose of pipelined FFT plus combiner module in this research is to execute the instruction on communication (data send and receive) and self-organization. Besides these two modules, there is a memory for temporarily storing the data and an internal clock, among other things. To accomplish these, the designs have been carried out using Verilog coding in Modelsim software, and the design verifications are done through Matlab. The design implementation is via Quartus and on DE2-115 Altera FPGA board. The functionality analyses have been carried out on simulation, and the hardware implementation of the MC-CDMA receiver is tested. Both simulation and hardware execution are successful where the receiver received and displayed the output accordingly. MC-CDMA achieves 39.13mW total power consumption.

Keyword: Combiner; FPGA; MC-CDMA; Pipelined FFT; Receiver