Energy Consumption Evaluation of Flip-Flops for Dynamic Voltage Scaling Systems and Circulating-Temperature Applications

by

Minghe Shao

Submitted to the Graduate Faculty of the

Swanson School of Engineering in partial fulfillment

of the requirements for the degree of

Master of Science

University of Pittsburgh

2021

UNIVERSITY OF PITTSBURGH

SWANSON SCHOOL OF ENGINEERING

This thesis was presented

by

Minghe Shao

It was defended on

March 5, 2021

and approved by

In Hee Lee, PhD, Assistant Professor, Department of Electrical and Computer Engineering

Samuel Dickerson, PhD, Assistant Professor, Department of Electrical and Computer Engineering

Rajkumar Kubendran, PhD, Assistant Professor, Department of Electrical and Computer Engineering

Thesis Advisor: In Hee Lee, PhD, Assistant Professor, Department of Electrical and Computer Engineering

Energy Consumption Evaluation of Flip-Flops for Dynamic Voltage Scaling Systems and Circulating-Temperature Applications

Minghe Shao, M.S.

University of Pittsburgh, 2021

CMOS circuit technology has developed with a help of transistor scaling. In past decades, previous studies found that operating environment of digital system affects circuit performance significantly. For example, extensive research has been performed to learn temperature dependency of CMOS circuits and optimize their performance at given temperature. Adaptive voltage scaling (AVS) is one of the important techniques, responses to operating temperature and dynamically change supply voltage of digital circuits to optimize circuit performance. AVS can enable energy optimization for a system experiencing significant temperature variation, including a space satellite. However, inappropriate AVS results in functional failure in an extreme condition, which can cause substantial problem for a critical mission. This work proposes technique to evaluate recently published flip-flops considering their power-delay product (PDP) and reliability for an AVS system operating under circulating temperature. The 8 flip-flops are evaluated under different temperature and supply voltage. Their PDPs are compared assuming that temperature changes linearly. Functional reliability is quantitatively evaluated using corner and Monte-Carlo simulations, and failure mechanisms of flip-flops are discussed as well.

Table of Contents

List of Tables

List of Figures

Acknowledgement

This thesis would not be possible without the guidance of my thesis advisor Dr. Lee and all the people who helped me on the study of integrated circuit. I am very thankful to Dr. Lee, his patient teaching and instructing made me confident to keep going on my M.S. thesis and future study.

I thank my families who always believe in me. I thank Yan Yu who is always by my side when I was doing this thesis. And I thank all of my friends who encouraged me.

1.0 Introduction

This work evaluates energy performance and functional reliability of flip-flops in a dramatically circulating temperature profile. It investigates how a harsh temperature environment profile affects energy consumption of flip-flops. The tested flip-flops are designed and tested in a 180nm CMOS process.

1.1 Background & Motivation

A flip-flop is one of the most fundamental components in a digital system. It holds state from fast data transition to regulate overall data flow and contributes to a considerable part of energy consumption of the system. Energy consumption is a critical factor for energy-limited applications including a space satellite. Thus, improving energy efficiency of the flip-flops is important for such applications to enable the system to operate on harvested energy from environment.

A satellite experiences significantly varying temperature. For example, a metal plate in low earth orbit (LEO) experiences temperature from –170°C to 123°C. Depending on its direction and exposure time to the sun, a satellite running at LEO experiences temperature difference ranging from -101°C to 93°C, with a help of heating and cooling devices on it [1]. The temperature change affects saturation velocity and mobility and thus the performance of CMOS devices [2]. Therefore, the operating circumstances bring challenges for electronics since electronic devices have to be reliable at the significantly varied temperature.

This work explores the optimal flip-flop design for a target temperature profile from -100°C to 100 °C. As one of the most important digital components, prior research has proposed a variety of flip-flops with different topologies. However, there is still a margin to further optimize performance of the flip-flops, considering a circulating temperature condition. In addition to energy consumption, this work also include reliability evaluation for flip-flop since functional failure of target mission-critical systems can cause critical safety issues and economic losses.

1.2 Related Work

1.2.1 CMOS Circuits under Voltage and Temperature Variations

For CMOS integrated circuits, delay is affected by both supply voltage (V_{DD}) and operating temperature. The relationship among delay, V_{DD}, and threshold voltage (V_{th}) is expressed as:

$$Delay \propto \frac{V_{DD}}{(V_{DD} - V_{th})^{\xi}} \qquad (1.1)$$

where ξ is empirical constant and usually $\xi > 1$. The delay decreases at higher supply voltage [3]. Temperature also influences speed performance of MOS circuit, and the effect is introduced with coefficient μ as T^{μ} as:

$$Delay \propto \frac{V_{DD} \times T^{\mu}}{(V_{DD} - V_{th})^{\xi}} \qquad (1.2)$$

where coefficient μ is empirically chosen to 1.19 [4]. Temperature affects V_{th} as well because of shift in Fermi level and bandgap energy and decreases V_{th} at higher temperature [5].

$$V_{th} = V_{th}(T_{ref}) - k_{vt}(T - T_{ref}) \qquad (1.3)$$

In addition, higher temperature increases subthreshold leakage current, which leads to serious energy dissipation during OFF state in CMOS circuits. It exponentially increases current consumption by decreasing V_{th}. The quantitative relationship between temperature and leakage current (I_{ds}) can be expressed as the following equations,

$$I_{ds} = I_{ds0} \cdot e^{\frac{V_{gs} - V_{th}}{n \cdot v_T}} \left(1 - e^{\frac{-V_{ds}}{v_T}} \right) \tag{1.4}$$

$$I_{ds0} = \beta \cdot v_T{}^2 \cdot e^{1.8} \tag{1.5}$$

$$\beta = \frac{W}{L} \cdot C_{ox} \cdot \mu_n \tag{1.6}$$

where v_T is the thermal voltage, μ_n is the mobility of carriers, W/L is the width to length ratio of the device, and C_{ox} is the oxide thickness [6].

1.2.2 Temperature Dependence in Subthreshold Region

EQ 1.2 shows that propagation delay increases at higher temperature in super-threshold region. However, at low supply voltage (subthreshold), propagation delay decreases at higher temperature. The delay model and drain current in the subthreshold condition can be simply introduced by alpha-power law [7], [8], shown as below:

$$Delay \propto \frac{C_{out} \times V_{DD}}{I_d} \tag{1.7}$$

$$I_d \propto \mu(T) \cdot \left(V_{DD} - V_{th}(T) \right)^{\alpha} \tag{1.8}$$

$$\mu(T) = \mu(T_0) \cdot \left(\frac{T_0}{T} \right)^m \tag{1.9}$$

where C_{out} is the output load, I_d is the drain current, $\mu(T)$ is the mobility, $T_0 = 300$ K, α and m are small positive constants. EQ 1.7 shows that gate delay is reversely proportional to drain current.

EQ 1.8 and EQ 1.9 reveal that lower temperature increases the carrier mobility thus the drain current. On the other hand, EQ 1.3 shows that lower temperature increases threshold voltage thus decreases the drain current. Therefore, the actual dependence of temperature on the gate delay is determined by the dominating factor between mobility and threshold voltage. For super-threshold operation, mobility factor dominates, thus higher temperature brings higher delay. For subthreshold operation, the threshold voltage dominates the drain current, higher temperature makes the device faster [9]. In this work, circuits are operating at subthreshold region.

1.2.3 Adaptive Voltage Scaling Based on Temperature Variation

In an AVS system that optimizes energy consumption, transistors operate in near or subthreshold region. In this condition, propagation delay decreases at higher temperature, and thus supply voltage can be lowered to save further energy consumption for similar delay performance. Ranjith Kumar proposed AVS technique that tunes the supply voltage based on fluctuated die temperature. It saves energy consumption by 21 % for a system with die temperature ranging from 25°C to 125°C [10]. J. Zhu and N. Bai proposed a SRAM with AVS technique that compares its data with one from the original power supply. It saves energy by 60% by reducing supply voltage from 1.2 V to 0.7 V [11]. In 2016, A. Chhabra developed a temperature-based memory subsystem that modulates body bias voltage to reduce SRAM V_{min}, and it improves dynamic power by 18% and timing by 30% [12].

1.2.4 Power-Delay Product

In digital circuit, propagation or gate delay is time used to change state of a signal between a driver and a receiver. The average power consumption for the operation can be expressed as [13]:

$$P_{avg} = \frac{E}{T} = \frac{1}{T} \int_0^T P(t)dt \qquad (1.10)$$

where P_{avg} is the average power during the operation, E is the total energy consumption, T is the time interval of the operation. Hence, multiplication of the delay and average power, called power-delay product (PDP), provides the energy consumed in single operation.

In this work, PDP is adopted as figure-of-merit (FoM) for evaluating the energy performance of flip-flops.

1.3 Contribution of This Work

This work proposes a method evaluating flip-flops in energy consumption for a system using AVS technique and also for circulating-temperature applications. Also, this work explores an optimization technique that maximizes energy efficiency by selecting an optimal flip-flop for a target circulating temperature profile (e.g., space satellite). Various designs of flip-flops are evaluated by comparing PDP for an AVS system working at the temperature environment. The flip-flops, selected from previous research, are sized for fair comparison. This paper also proposes an algorithm that analyzes simulation results considering process, voltage, and temperature (PVT) variations and determines the optimal supply voltage for the minimum PDP. From the result, this work finds that for a given speed requirement, most flip-flops save energy consumption by about

5

30% by using AVS technique and optimizing supply voltage, compared with ones using constant supply voltage, shown in Appendix C. It also finds that supply voltage scaling depends on robustness of flip-flop circuits, which determines the maximum energy saving for a target system. In addition, the PDP evaluation result shows that, among the tested flip-flops, Static Contention-free Differential Flip-Flop (SCDFF) is the optimal circuit for an AVS system and a target temperature profile.

1.4 Organization

In this paper, Chapter 1 introduces the background and motivation of this work and review related previous works.

Chapter 2 discusses different structures of flip-flops used for the simulation, including their operating mechanism and weakness (for a part of the flip-flops), a method of sizing these flip-flops to normalize the simulation result, and testbench circuits and method for their performance evaluation.

Chapter 3 reports functionality test results for the target temperature profile, evaluation results using Figure-of-Merit (FoM), and statistical outcomes.

Chapter 4 concludes this paper and discusses the future potential work.

2.0 Proposed Evaluation Process

2.1 Introduction

Recently Proposed 7 flip-flops are evaluated to find the most energy-efficient circuit for a target temperature profile. In addition, a conventional flip-flop is added to the evaluation to help performance comparison. Since the flip-flops are developed for different purposes, this chapter firstly discuss the pros and cons of the flip-flops. Transistors of flip-flops are resized in the same scale for fair performance comparison by simulating an inverter for balanced pull-up and pull-down strength.

2.2 Evaluated Flip-Flops

2.2.1 Conventional Transmission-Gate Flip-Flop

Figure 2.2-1 shows the transmission-gate-based flip-flop (TGFF), which was mainstream in earlier microprocessors [14]. It has typical master-slave latch topology. TG3 contributes to fully isolation between two latches under the control of clock signal. When CLK is low, TG1 is closed, and TG2 is open. It passes the input (D) to Net1 and then Net2. When CLK is high, TG3 is closed, and TG4 is open. It passes the signal to Net3, Net4 and then output (Q).

At this point, D before the rising CLK edge is latched in the master latch with closed TG2, and D value after the rising CLK edge is isolated. As CLK falls low, the updated Net3 and Net4 at the high CLK is stored in the slave latch with closed TG4. This circuit includes an output inverter to generate a non-inverted output.
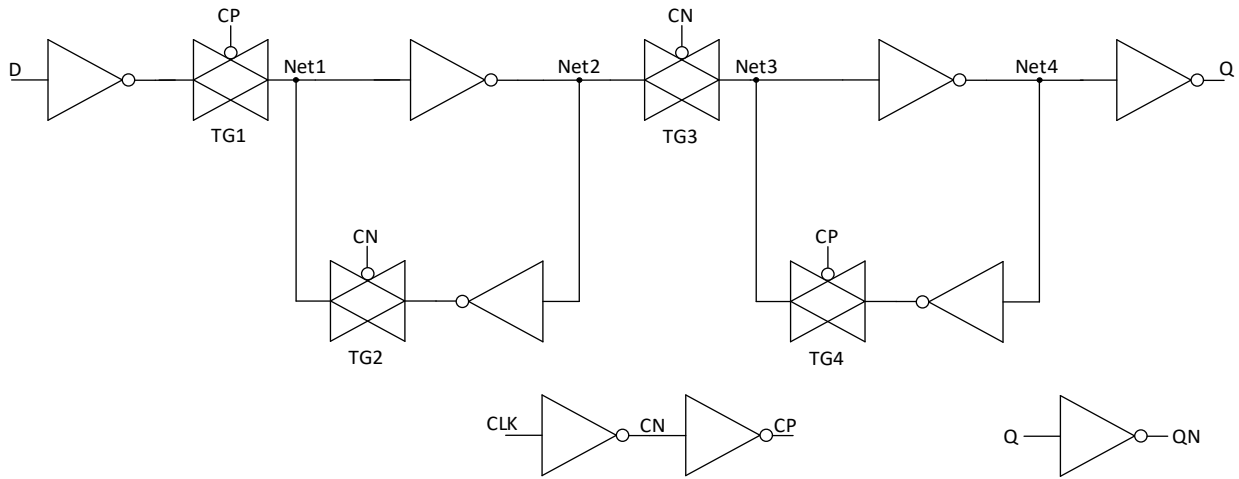
Figure 2.2-1. Schematic of TGFF (Clock inputs of NMOS of the transmission gates are not shown).

TGFF satisfies contention-free and fully static. When the circuit performs a writing operation, TG1 isolates the input for better noise immunity, which makes it suitable for large scale designs with high clock skew [15]. However, it has 8 transistors loaded with clock signals, which contributes to higher energy consumption from internal clock toggling.

2.2.2 Write-Port Master-Slave-Latch Flip-Flop

Figure 2.2-2 shows the write-port master-slave-latch flip-flop (WPMS) that replaces transmission gates with pass transistors to construct the master and slave lathes [16]. It reduces the

number of clock-loaded transistors and thus the total number of transistors in the flip-flop. Therefore, WPMS can reduce cell area and energy consumption compared to TGFF. PMOS transistors are only present in the latches so that, the data path has less clock-delay and parasitic capacitance.
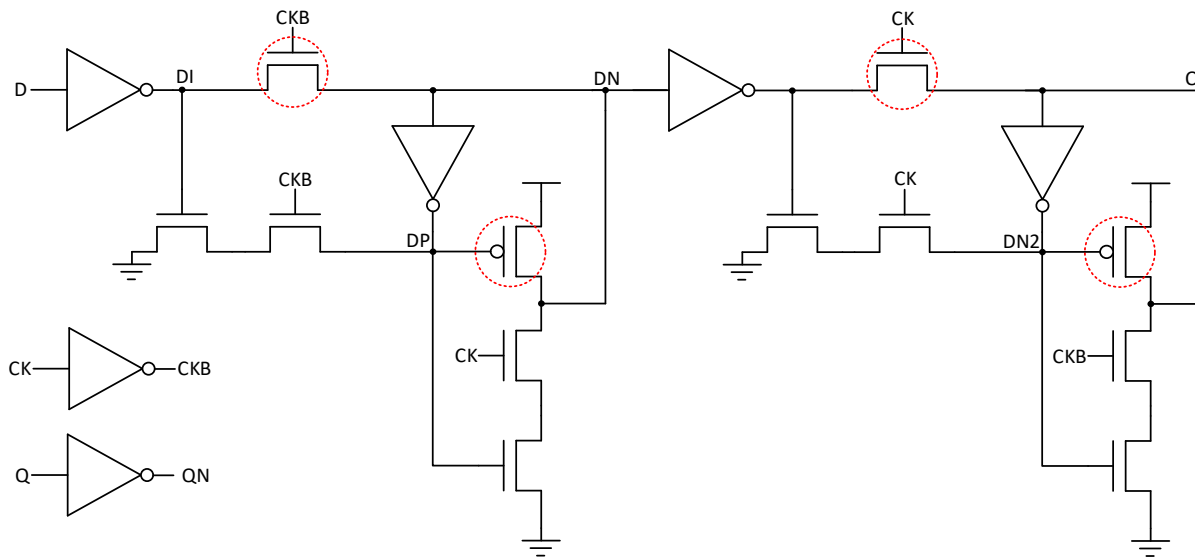
Figure 2.2-2. Schematic of WPMS.

However, WPMS has 6 clock-loaded transistors that brings large redundant energy consumption. The pass transistors are placed in the critical path, weakening the timing characteristic [17]. Furthermore, the width of the critical transistors, circled in the figure, is required to be properly scaled to relieve the experimentally observed imbalance on pull-up and pull-down strength in transition phase. The pass transistors and PMOS transistors require P/N ratio less than 0.65 (3.24 µm for PMOS width, 5 µm for NMOS width) to avoid obvious imbalance and retention failure caused by contention.

2.2.3 18-Transistor Single-Phase-Clocked

Figure 2.2-3 shows the 18-transistor single-phase-clocked flip-flop (TSPC). It is designed with topology of fully static and contention-free with single phase clock. When CLK is high, input D changes the state of L1 of the master latch, and the slave latch is isolated from D. When CLK falls low, D is isolated from master latch, and the data latched in L1 passes to the slave latch and updates the output.
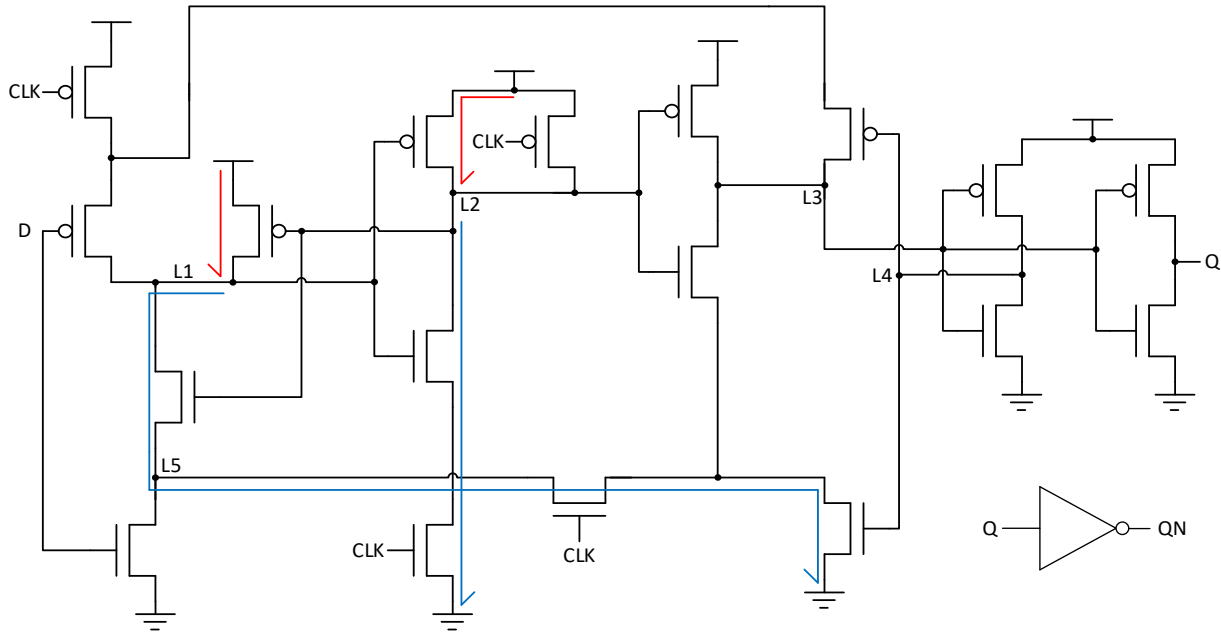
Figure 2.2-3. Schematic of 18TSPC.

Compared with TGFF of 24 transistors, it remarkably saves energy and cell area with less transistors. Also, it is twice efficient than TGFF [18] in energy-delay FoM. Transistor merging helps reduce the number of clocked transistors. However, there is potential contention that can cause the device failure [19]. When current output Q_{prev} is 1 and input D is 0. Thus, when CLK is

0, L1 is 1 and L2 is 1 through the pull-up network. As CLK rises, ideally, L2 is connected to pull-down network controlled by L1 and CLK, then L1 should be pulled up according to L2. However, since $Q_{prev} = 1$, L4 and L2 are both 1 before the rising edge of the CLK. Hence, in this CLK condition, L1 can be pulled down under the control of L2, L4 and CLK, which leads L2 to be pulled up and potentially reversing states of L1 and L2. The contention issue is worse with PVT variation.

2.2.4 Static Single-Phase Contention-Free Flip-Flop

Figure 2.2-4 shows the static single-phase contention-free flip-flop (S^2CFF) [20]. It has fully static operation and completely contention-free characteristic. It uses a single-phase clock and lowers power consumption. Compared with traditional TGFF, it has no additional transistor while limiting redundant transition. It simplifies hold-time path so that the hold time of S^2CFF is less prone to variation compared to TGFF. Also, S^2CFF has the advantage of robustness and energy-efficiency over wide range of operating voltage.

However, it suffers from unnecessary energy consumed by internal clock toggling. Only when the input D stay high, it eliminates the redundant transitions. On the other hand, if input D stays low, Net2 presents inverted CLK, causing internal clock toggling [21]. This can be seen as half-redundant transition with 0.5 coefficient but resulting in considerable additional energy consumption in low activity operation.

11
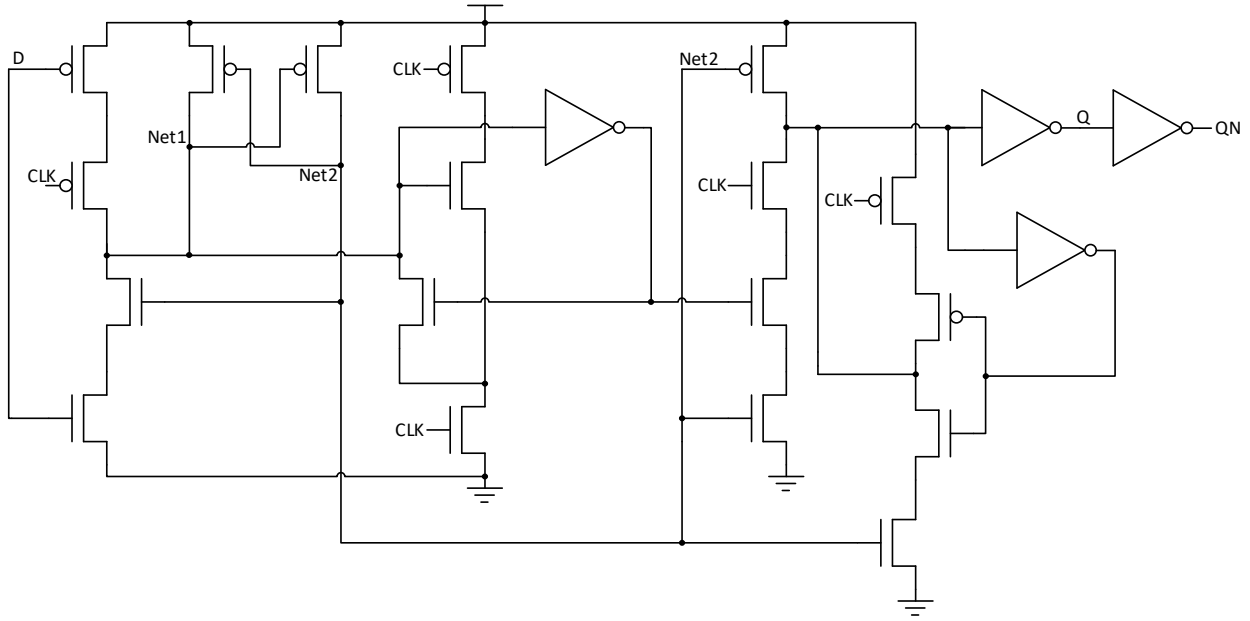
Figure 2.2-4. Schematic of S^{2}CFF.

2.2.5 Adaptive-Coupling Flip-Flop

Figure 2.2-5 shows the adaptive-coupling flip-flop (ACFF) [22]. It has differential master-slave topology that modifies TGFF by removing the clock buffer inverters. It features single phase clock pulse since the clock buffer and pre-charge state is removed. This structure gains large energy saving at idle data state by reducing redundant transition when the input does not change. The adaptive coupling (circled in the figure) is added to weaken state-retention coupling when the input data is not the same as the internal data. This is because the state-retention circuit suffers from weak driving strength of the PMOS pass transistor.
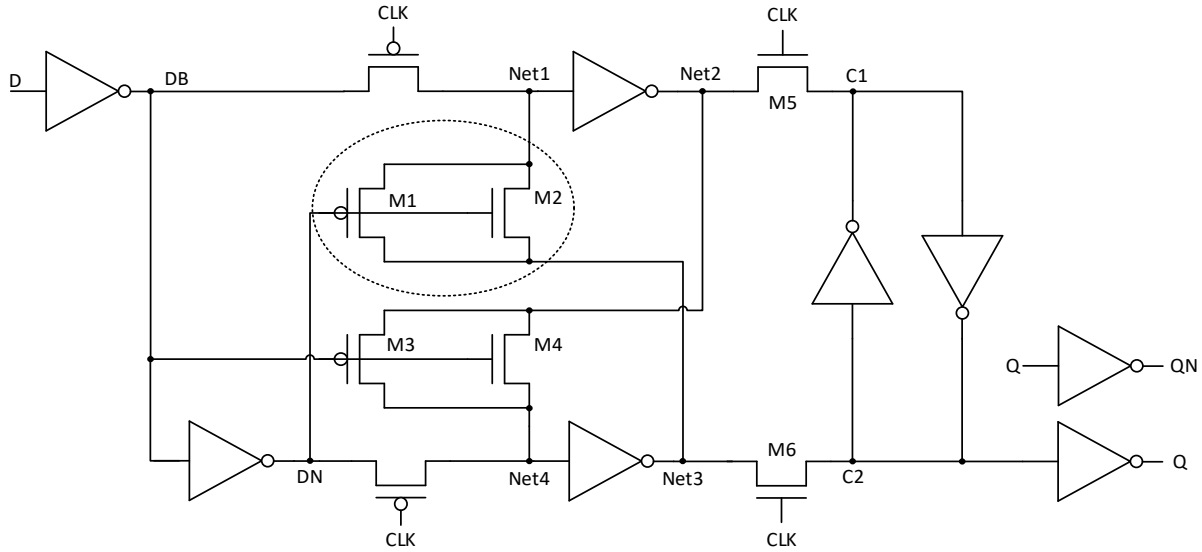
Figure 2.2-5. Schematic of ACFF.

The adaptive-coupling scheme includes PMOS and NMOS transistors, connected in parallel, in the first latch structure. When D is low, the input is written to the first latch. High DB and low DN make M1 and M4 closed so that the path between Net2 and Net4 discharges Net2. However, it is hardly discharged completely due to the PMOS transistor between Net4 and DN. On the other side, M1 provides a strong charging path between Net1 and DN, so Net2 is discharged to 0 completely.

Even though ACFF weakens the state-retention issue, the slave latch suffers from contention, resulting in writing failure [19]. When D = 0, the previous output Q_{prev} = 1, and CLK rises, Net 2 has a good discharging process so that the CLK rising edge puts the new data forward. However, if C2 is 0 previously, it charges to high through M6 of which pull-up strength is weak. Thus, C1 loses robustness and makes the circuit not static, which can cause contention on C1, especially in PVT variation.

This failure phenomenon can be relieved by scaling up the NMOS width of M5, M6 and inverters connected on their left, but it is not a long-term solution and causes extra energy consumption.

2.2.6 Change-Sensing Flip-Flop

Figure 2.2-6 shows the change-sensing flip-flop (CSFF), which Van and Kim proposed to reduce the energy consumption caused by internal redundant transition of flip-flops [21]. It has local change-sensing scheme to lower such transition caused by clocked nodes, shown in a rectangle in the figure. Theoretically, it almost does not consume any dynamic power when the circuit is idle and has a great energy-efficient advantage in low activity mode. In the simulation of this work, the circuit can operate at low functional supply voltage (100 kHz clock frequency, 0.15 V for the best condition, and 0.55 V for the worst condition).

In pre-charge phase, CS is pulled up. After CLK rises, CS can only be discharged when QN = D = 1 or DN = QI = 1 since QN and DN are connected with D and QI in series, respectively. CS acts as a trigger of the master latch, and redundant transition is eliminated if CS = 1.

CSFF extremely lowers dynamic power occurred with unchanged states, and the circuit itself is also contention-free. However, it has a reliability issue with dynamic nodes in some conditions, making it not fully static. Assuming CS = 1 and D = 0, Q, QN and DN should be 0, 1, and 1, respectively, according to the change-sensing mechanism. When CLK rises (marked as red), CS is neither pulled up nor down and becomes floating, which makes QN floating as well. Thus, the floating input node affects the output.
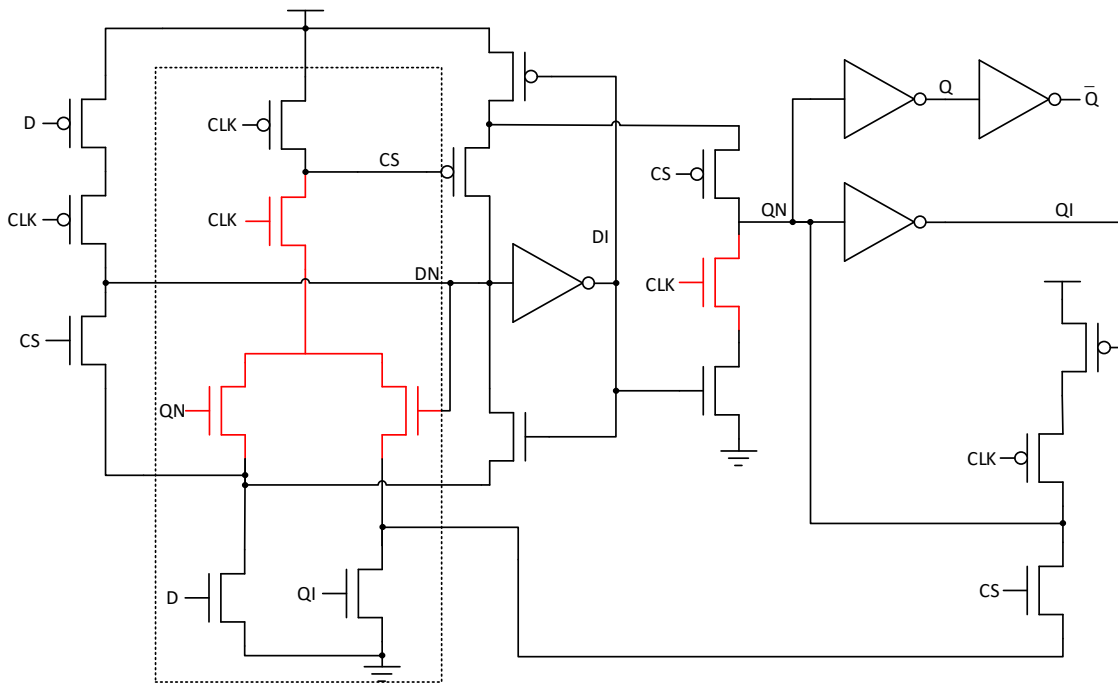
Figure 2.2-6. Schematic of CSFF.

2.2.7 Topologically Compressed Flip-Flop

Figure 2.2-7 shows the topologically compressed flip-flop (TCFF) [23]. Based on unconventional latch structure, TCFF applies topological compression method and merges logically equivalent transistors to reduce the number of transistors. Thus, it maintains its cell area as the same as the conventional TGFF. It achieves similar timing performance but saves dynamic energy consumption by including only 3 clocked transistors without dynamic or pre-charge circuits.

TCFF removes unnecessary internal clock nodes, and the area overhead is well controlled by topological compressing and logical merging. However, the number of shared transistors is too large to maintain good robustness. The degraded robustness of TCFF contributes to contention and failure issue when the circuit experiences large PVT variation, especially at low supply voltage.

15

Low operating voltage reduces voltage swing of VD1 and VD2 of the circled NMOS transistors in the master latch. It causes contention related to NMOS and PMOS networks in the master latch. Also, if CLK and D is 0, VD1 up pulls N1, making N2 to 0 and N3 to 1. With PVT variation, contention happens on N2. If D rise to 1 at this moment, VD2 pulls up N2 (red lines) since the circled NMOS is still closed. On the other hand, N3 is high, and a pull-down network is on at N2 (blue line), which leads to strong contention and thus circuit failure.

Figure 2.2-7. Schematic of TCFF.

2.2.8 Static Contention-Free Differential Flip-Flop

Figure 2.2-8 shows the static contention-free differential flip-flop (SCDFF) [19]. It uses footers & headers and bridges of ground and supply. It features fully static and contention-free while minimizing internal clock toggling and cell area overhead are minimized, achieving good robustness to PVT variation.
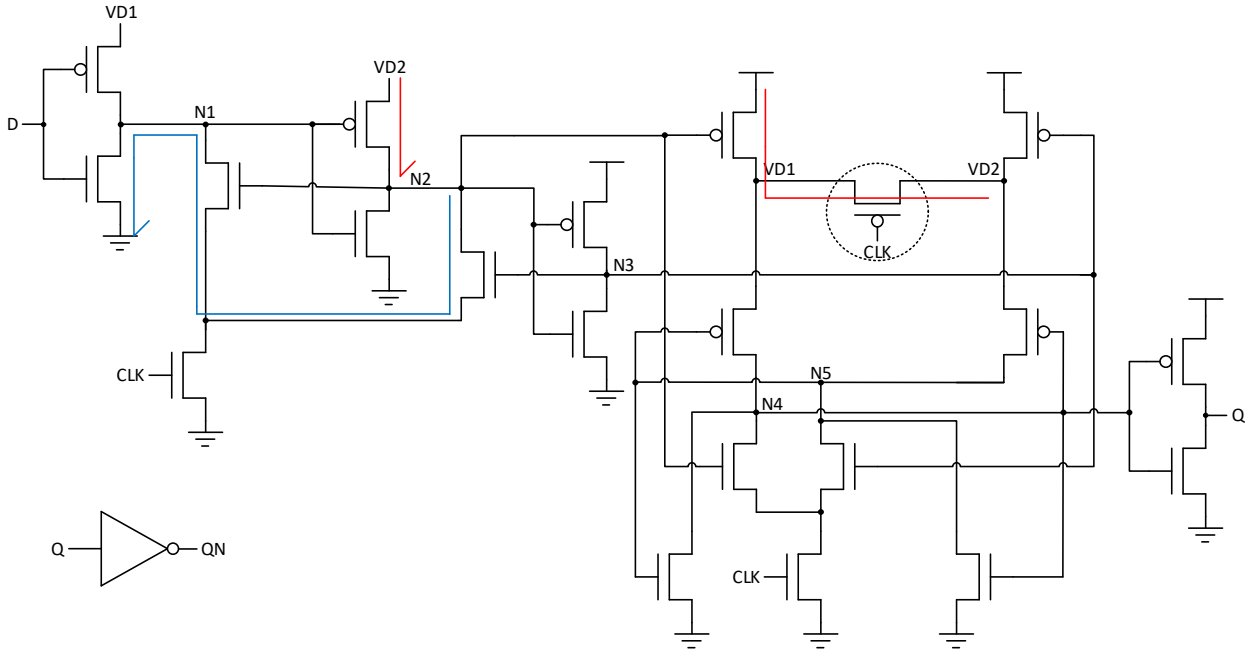
16

It includes master and slave latches that are footed or headed by NMOS or PMOS transistors in the red circles. Suppose the 4 circled transistors are ignored. The master latch includes two parts with DN and DI for each side, controlled by CLK and DB. DB is an inverted the input D. In the slave latch, QN and QI perform similar roles of DN and DI. This causes a contention that the latched data on two parts of the latch put each other into wrong pull-up or pull-down networks. Since QN and QI are the opposite, QI unexpectedly makes QN to be pulled up although QN should be pulled down. To remove this potential contention, 1) QN is headed under the control of DI with the headers in slave latch, 2) the pull-down and pull-up for QN and QI are respectively secured, 3) input data is transferred to the master latch when CLK = 0, 4) the DB footer cuts off the pull-down network to DI, and 5) the D footer cuts off the pull-down network to DN to secure their transitions when the changed data comes from the input.

Such cut-off structure remains active when the circuit is in retention phase, causing floating nodes. The bridge transistors (circled in blue) solve this issue and make this circuit fully static. For example, when CLK = 0, the circuit is in retention phase. The header controlled by DI blocks the pulling up for QN when CLK rises. It acts as a bridge to supply the pull-up path to QN until the rising of CLK.

SCDFF removes internal clock toggling. Also, it is fully static and contention-free, providing robustness at the cost of 2 additional transistors compared to TGFF, increasing energy consumption.
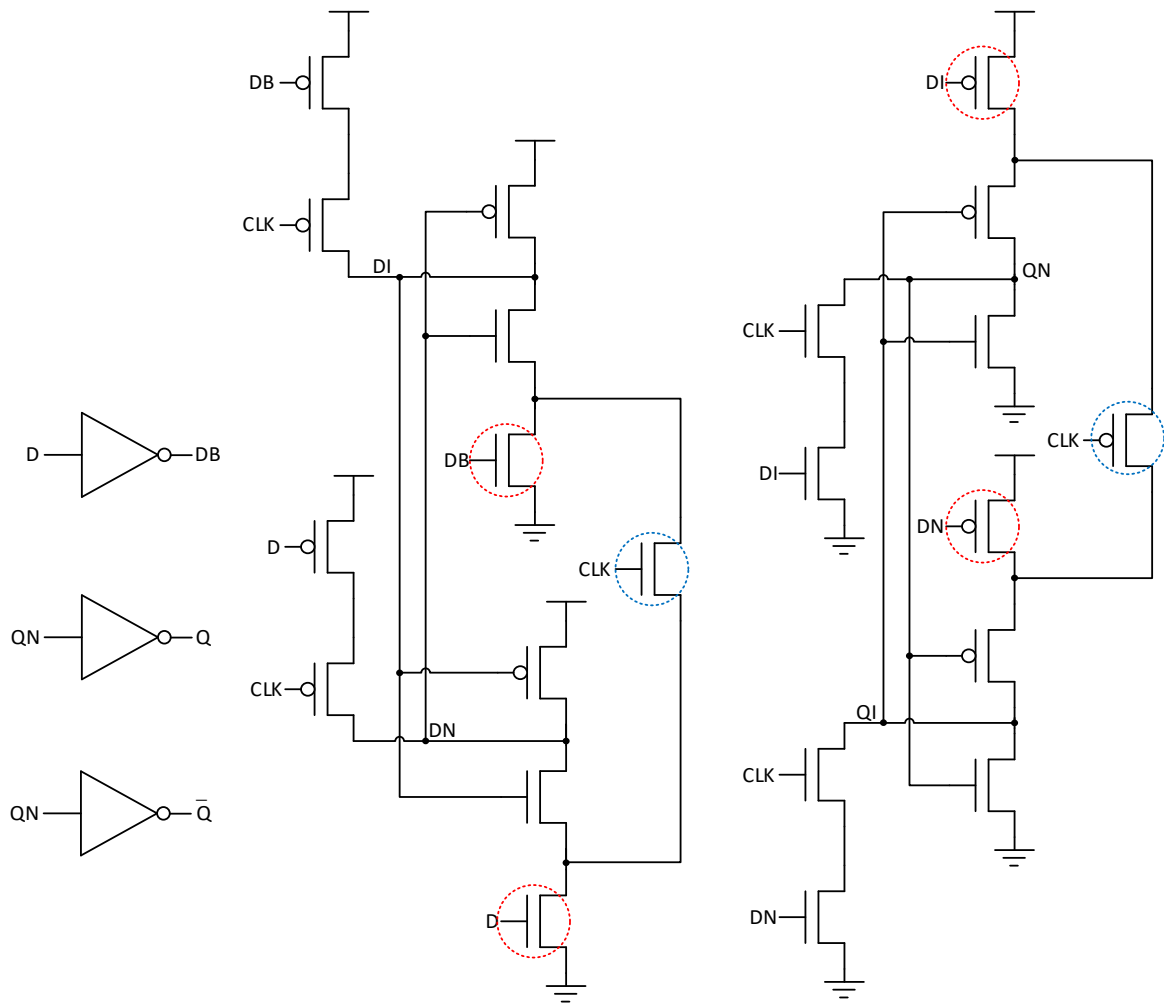
Figure 2.2-8. Schematic of SCDFF.

2.3 Transistor Sizing for Flip-Flops

In this work, the flip-flops, introduced in Section 2.2, are designed with the same P/N ratio to compare them with a unified design approach. To obtain the P/N ratio, an inverter is tested in a 180 nm CMOS process. Initially, corner, V_{DD}, and temperature are set to typical, 1V, and 0°C respectively. Figure 2.3-1 shows the voltage transfer curve of the inverter, which presents unbalance between pull-up and pull-down strength due to the weaker pull-up network.
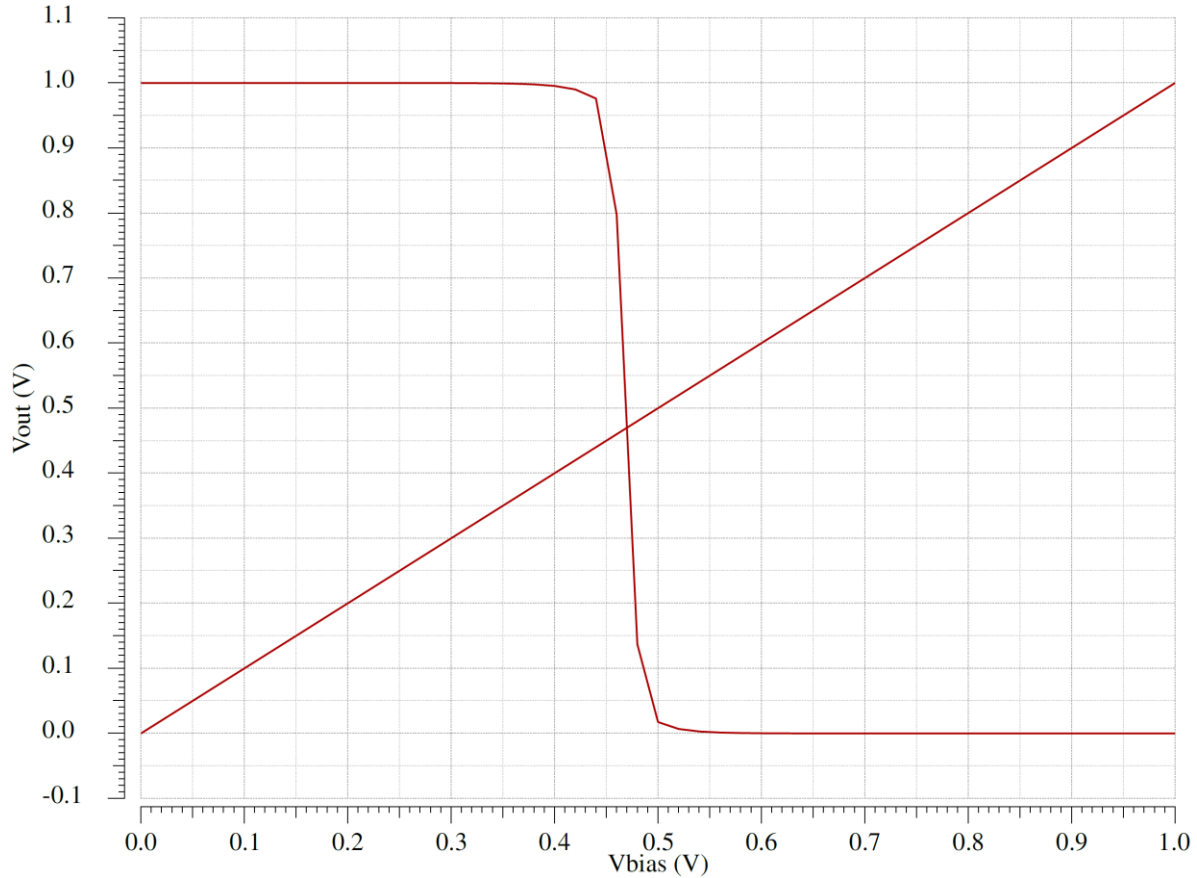
Figure 2.3-1. Result of DC simulation of single inverter.

To balance the pull-up and pull-down networks, bias voltage (Bias) is defined by finding how much the crossing point is apart from a half supply voltage as:

$$Bias = \left| X\left(\frac{V_{DD}}{2}\right) - \frac{V_{DD}}{2} \right| \qquad (2.1)$$

Figure 2.3-2 shows simulated Bias by sweeping the width of NMOS transistor (W_n) from 360 nm to 2 µm and also sweeping the width of PMOS transistor (W_p) from 720 nm to 6 µm. L is the minimum length, 180 nm. Before the minimum point of each curve, Bias is proportional to W_n at a given W_p because pull-up is weaker than pull-down. After the minimum point, the pull-up network becomes stronger than the pull-down network, and Bias becomes smaller with larger W_n. In this work, W_n is set to 360 nm for low power consumption and W_p is set to ~3 µm for the minimum Bias.
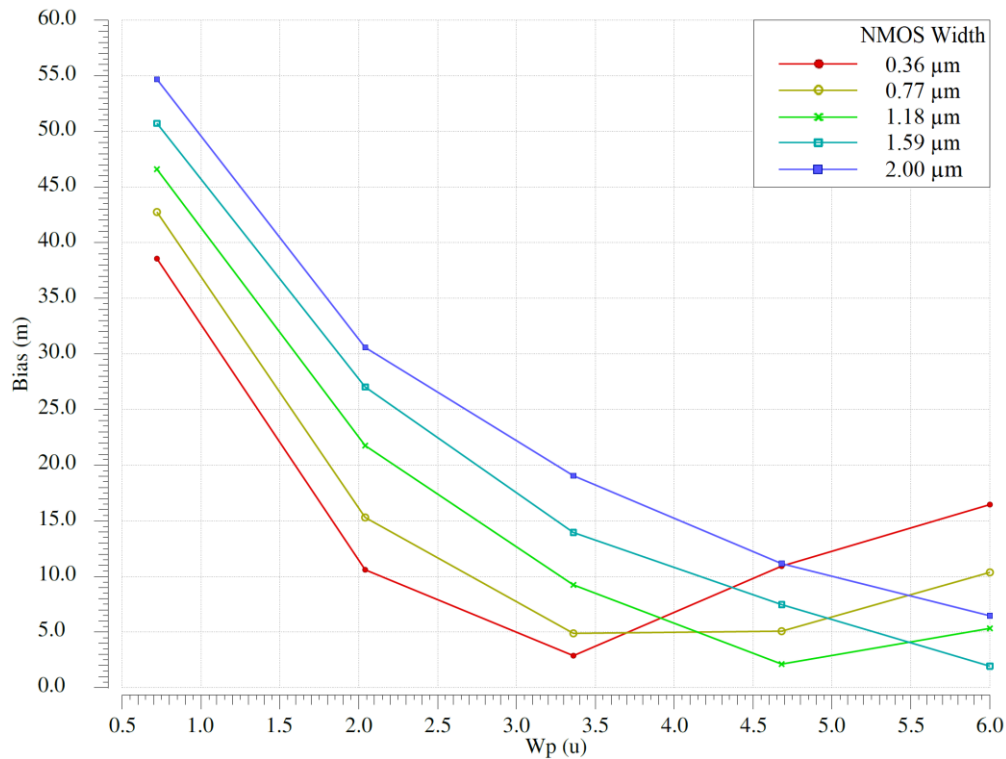
Figure 2.3-2. Simulation result with different NMOS width and PMOS width.

20

This work covers the temperature range from -100 ℃ to 100 ℃, and a target AVS system provides supply voltage from 0.2 V to 1 V. Bias is also evaluated considering this condition, and simulation result is shown in Figure 2.3-3. With a help of Python IDE (Appendix A), it shows the mean and sigma of Bias for W_p from 0.72 µm to 4.32 µm with steps of 0.18 µm, considering supply voltage from 0.2 V to 1 V with steps of 0.05 V and temperature from -100 ℃ to 100 ℃ with steps of 20 ℃. From the results, W_p is set to 3.24 µm (W/L = 18) since the Bias value becomes saturated with larger W_p. The P/N ratio of 9 is applied to the evaluated flip-flops.
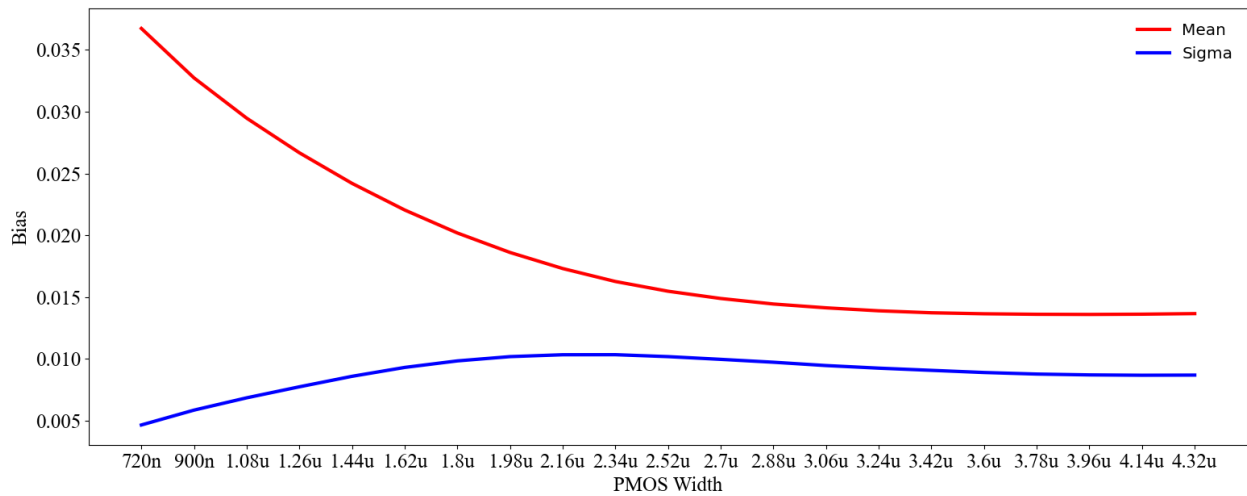
Figure 2.3-3. Simulation result with W_p-temperature-V_{DD} combinations.

2.4 Testbench for Evaluation

Figure 2.4-1 shows the testbench to evaluate flip-flops. The input of the tested flip-flop is driven by an inverter, and the output is loaded by 4 inverters for fan-out of 4. The input and clock signals have rising and failing time of 1 ps. Figure 2.4-2 shows a simulation result as an example. The input and clock signals provide 5 different input-output states, including 0-Floating, 1-0, 1-1,

0-1, 0-0. Functionality of the tested flip-flops is checked by comparing the simulated output (e.g., CSFF, SCDFF, S²CFF, and ACFF) with a desirable signal (Comp). PDP of the flip-flop for rising (falling) output switching is calculated as:

$$Q = \int_{t_{Q_{startRise}}}^{t_{Q_{rise\ to\ 0.5VDD}}} i(t)\, dt \tag{2.2}$$

$$PDP_{rise} = Q \times V_{DD} \tag{2.3}$$

where $i(t)$ is the current flow from the supply to the flip-flop, $t_{Q_{rise\ to\ 0.5VDD}} - t_{Q_{startRise}}$ is the propagation delay for the rising switching of the flip-flop, and Q is the amount of charge consumed. Then, PDP is calculated by multiplying Q and the supply voltage.
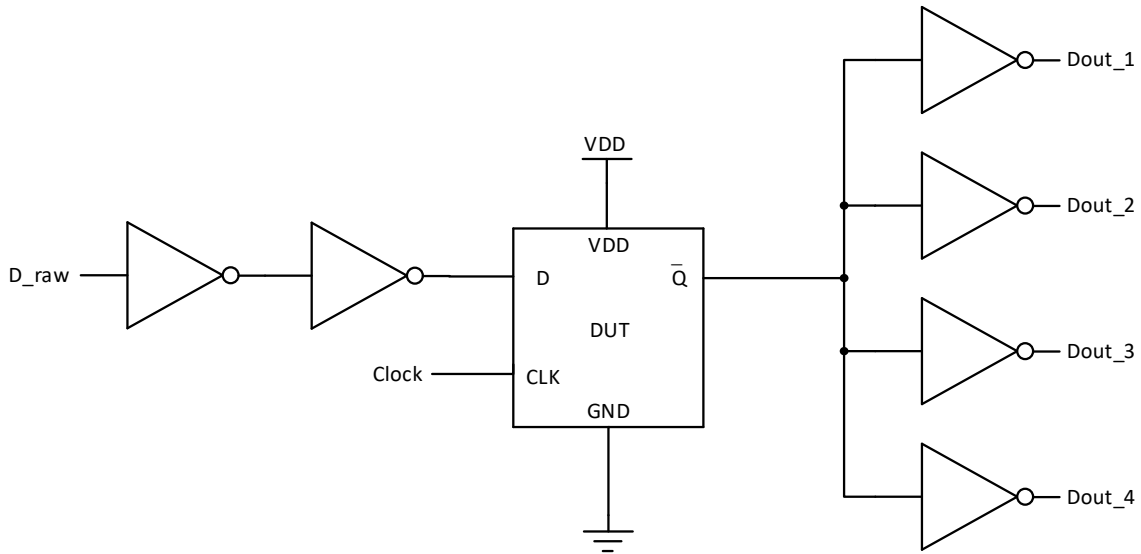
Figure 2.4-1. Test circuit for flip-flops.
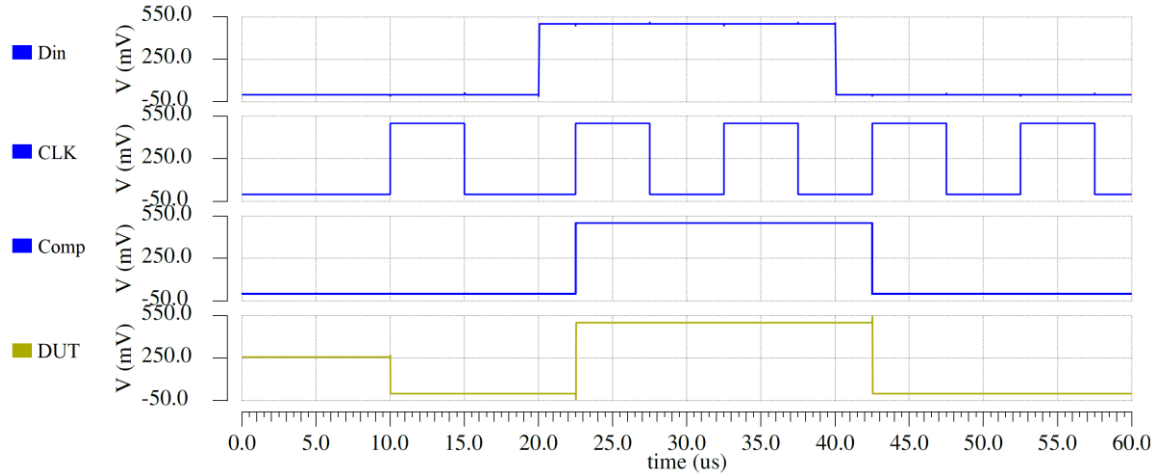
Figure 2.4-2. Simulation waveforms.

2.5 Evaluation Process

Figure 2.5-1 shows the proposed overall procedures to evaluate the FoM of the flip-flops. As the first step, each flip-flop is tested in the extreme cases including worst and best conditions, to check if the flip-flop is suitable for the target temperature range (-100 ℃ – 100 ℃) and frequency (100 kHz or 2 MHz) and obtain a rough voltage range for corner simulations. The worst condition is -100 ℃ and slow-slow corner, and the best condition is 100 ℃ and fast-fast corner, considering the minimum functional supply voltage. For example, in the worse condition, a flip-flop needs higher supply voltage for correct functionality. Based on the obtained voltage range from the extreme case simulations, the flip-flop is tested again with all the 5 corners (typical-typical, slow-fast, fast-slow, slow-slow, and fast-fast) and searches for the minimum supply voltage at each temperature (-100 ℃ to 100 ℃ with 10 ℃ steps). At this supply voltage, the flip-flop should successfully operate across target temperature, from -100 ℃ to 100 ℃ with 10 ℃ steps, and at the target frequency. If the flip-flop operates without an issue at a supply voltage, the

23

test decreases the supply voltage until the flip-flop does not operates properly in any condition, and thus finding the minimum functional supply voltage for each temperature point.

Next, as the second step, the functionality of the flip-flop is tested using process variation and device mismatch using 1,000 Monte-Carlo simulations across the target temperature range. At one temperature condition, if all the 1,000 simulations show successful flip-flop operation, it records 'average + 3 × sigma' of PDP as a representative number for the temperature. Otherwise, it increases the supply voltage until all the Monte-Carlo simulations show desirable flip-flop function. Then, it increases supply voltage again by searching for the supply voltage providing the minimum 'average + 3 × sigma' of PDP.

In this evaluation, the first step coarsely searches for a good candidate of the minimum supply voltage using corners, and then the second step finely finds the minimum 'average + 3 × sigma' of PDP point considering robustness of the flip-flop including device mismatch.
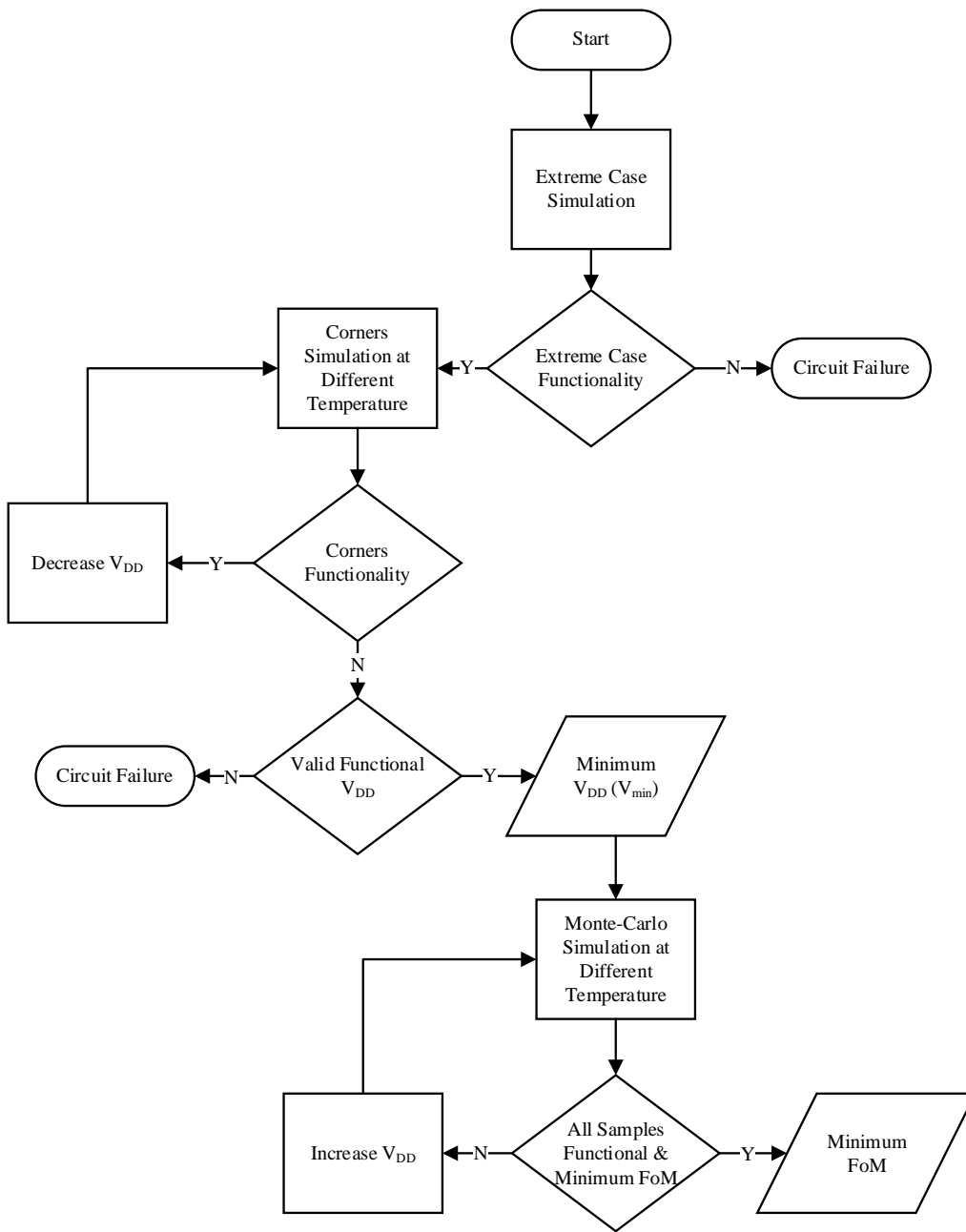
Figure 2.5-1. Flowchart of the evaluation process.

2.6 Conclusion

This chapter discusses the basic operation and advantages or disadvantages of selected flip-flops. The transistors of the flip-flops are sized by the P/N ratio of 9, based on the simulation result of a logic inverter considering target range of temperature and supply voltage. It also discusses the proposed evaluation process including the testbench for PDP evaluation, the first and second step simulation processes, and the flowchart to illustrate the evaluation procedure.

3.0 Evaluation Result and Analysis

3.1 Introduction

This chapter discusses the evaluation result and analysis based on functionality and robustness tests discussed in Chapter 2. For the evaluation, the operation frequency is set to 100 kHz and 2 MHz as examples.

In the corner simulation, WPMS is not reliable at low temperature, and TCFF shows higher minimal supply voltage than other flip-flops. In Monte-Carlo simulation (the second step), FoM evaluation across the temperature profile shows that SCDFF has lower FoM than the others, especially after increasing the frequency from 100 kHz to 2 MHz.

Section 3.4 discusses circuit failures during corners and Monte-Carlo tests and the FoM evaluation result from the second step simulations.

3.2 Evaluation Results of the First Step Using Corner Simulation

Table 1 presents the evaluation results of extreme cases in the first step, discussed in Section 2.5. It finds the minimum supply voltage where a tested flip-flop correctly operates in worst and best conditions. The worst condition is slow-slow corner and -100 °C while the best condition is fast-fast corner and 100 °C. The result shows that WPMS cannot pass all the tests even in the best condition because the pass-transistor in the critical path fails due to the contention with PMOS transistors. WPMS only works at fast-slow corner, which means the P/N ratio needs to be

smaller for reliable functionality. Also, TCFF shows the minimum supply voltage higher than the

others since its reduced robustness causes contention at low supply voltage. Failure and contention

mechanisms are talked in Section 3.4.

Table 1. Extreme cases simulation result.

Device	100 kHz		2 MHz	
	Worst Case (Slow-Slow & -100 ℃)	Best Case (Fast-Fast & 100 ℃)	Worst Case (Slow-Slow & -100 ℃)	Best Case (Fast-Fast & 100 ℃)
ACFF	550 mV	150 mV	650 mV	350 mV
S^{2}CFF	550 mV	150 mV	650 mV	300 mV
SCDFF	550 mV	150 mV	650 mV	300 mV
TCFF	700 mV	150 mV	850 mV	300 mV
TGFF	550 mV	150 mV	650 mV	300 mV
TSPC	550 mV	150 mV	650 mV	300 mV
CSFF	550 mV	150 mV	650 mV	300 mV
WPMS	failure	failure	failure	failure

The working flip-flops from Table 1 are further tested across all the five corners (typical-

typical, fast-fast, fast-slow, slow-fast, and slow-slow) and temperature (-100 ℃ – 100 ℃ with 10

℃ step). The simulation result is processed by a Python-coded program attached in Appendix B.

Table 2 and 3 show the result for target frequencies of 100 kHz and 2 MHz, respectively. For

example, under 100 kHz frequency, at the typical-typical corner, ACFF works at -100 ℃ at the

supply voltage of 0.5 V, which is the minimum supply voltage compared to the other flip-flops.

However, it fails at the slow-fast corner at the supply voltage of 0.55 V. At the supply voltage ≥

0.6 V, ACFF passes tests with all corners. The result shows that the minimum supply voltage of

most flip-flops decreases at higher temperature due to reduced threshold voltage of transistors [5].

Table 2. Minimal supply voltage found from functionality tests for 100 kHz [V].

Temperature (°C)	ACFF	S^{2}CFF	SCDFF	TCFF	TGFF	TSPC	CSFF	WPMS
-100	0.60	0.55	0.55	0.70	0.55	0.55	0.55	0.55*
-90	0.55	0.55	0.55	0.70	0.55	0.55	0.55	0.50*
-80	0.55	0.50	0.55	0.70	0.50	0.50	0.50	0.50*
-70	0.55	0.50	0.50	0.65	0.50	0.50	0.50	0.50*
-60	0.50	0.50	0.50	0.65	0.50	0.50	0.50	0.45*
-50	0.50	0.45	0.50	0.60	0.50	0.45	0.45	0.45*
-40	0.50	0.45	0.45	0.60	0.45	0.45	0.45	0.45*
-30	0.45	0.45	0.45	0.55	0.45	0.45	0.45	0.45*
-20	0.45	0.45	0.45	0.55	0.45	0.45	0.45	0.40*
-10	0.45	0.40	0.45	0.50	0.45	0.40	0.40	0.40*
0	0.45	0.40	0.40	0.45	0.40	0.40	0.40	0.40*
10	0.45	0.40	0.40	0.45	0.40	0.40	0.40	0.35*
20	0.45	0.35	0.40	0.40	0.40	0.35	0.35	0.35*
30	0.45	0.35	0.35	0.40	0.35	0.35	0.35	0.30*
40	0.50	0.35	0.35	0.40	0.35	0.35	0.40	0.30*
50	0.50	0.35	0.35	0.35	0.35	0.30	0.35	0.30*
60	0.50	0.30	0.30	0.35	0.35	0.30	0.30	0.25*
70	0.50	0.30	0.30	0.35	0.30	0.30	0.30	0.25*
80	0.50	0.30	0.30	0.35	0.30	0.30	0.30	0.25*
90	0.50	0.25	0.25	0.35	0.30	0.25	0.25	0.20*
100	0.50	0.25	0.25	0.30	0.25	0.25	0.25	0.20*

* The test fails functionality at a corner at least.

Table 3. Minimal supply voltage found from functionality tests for 2 MHz [V].

Temp(°C)	ACFF	S^{2}CFF	SCDFF	TCFF	TGFF	TSPC	CSFF	WPMS
-100	0.65	0.65	0.65	0.80	0.65	0.65	0.65	0.60*
-90	0.65	0.65	0.65	0.80	0.65	0.65	0.65	0.60*
-80	0.65	0.60	0.65	0.75	0.65	0.60	0.60	0.60*
-70	0.65	0.60	0.60	0.75	0.60	0.60	0.60	0.60*
-60	0.60	0.60	0.60	0.70	0.60	0.60	0.60	0.55*
-50	0.60	0.60	0.60	0.70	0.60	0.60	0.60	0.55*
-40	0.60	0.55	0.60	0.70	0.60	0.55	0.55	0.55*
-30	0.60	0.55	0.55	0.65	0.55	0.55	0.55	0.55*
-20	0.60	0.55	0.55	0.65	0.55	0.55	0.55	0.50*
-10	0.55	0.55	0.55	0.60	0.55	0.55	0.55	0.50*
0	0.55	0.55	0.55	0.60	0.55	0.50	0.50	0.50*
10	0.55	0.50	0.50	0.60	0.50	0.50	0.50	0.50*
20	0.55	0.50	0.50	0.55	0.50	0.50	0.50	0.45*
30	0.55	0.50	0.50	0.55	0.50	0.50	0.50	0.45*
40	0.50	0.50	0.50	0.55	0.50	0.50	0.50	0.45*
50	0.50	0.50	0.50	0.50	0.50	0.45	0.45	0.45*
60	0.50	0.45	0.45	0.50	0.45	0.45	0.45	0.40*
70	0.50	0.45	0.45	0.50	0.45	0.45	0.45	0.40*
80	0.50	0.45	0.45	0.45	0.45	0.45	0.50	0.40*
90	0.50	0.45	0.45	0.45	0.45	0.45	0.45	0.40*
100	0.50	0.45	0.45	0.45	0.45	0.40	0.40	0.40*

* The test fails functionality at a corner at least.

As an example, Figure 3.2-1 shows the minimum supply voltage of S^{2}CFF and SCDFF for operating frequencies of 100 kHz and 2 MHz. The evaluation result for a target frequency of 100 kHz shows the similar temperature dependency with one for 2 MHz. However, the minimum supply voltage is noticeably reduced for 100 kHz, compared with one for 2 MHz. For higher operating frequency, range of the minimum supply voltage across temperature is lower. This is because lower frequency allows more delay for a flip-flop and thus lower supply voltage.
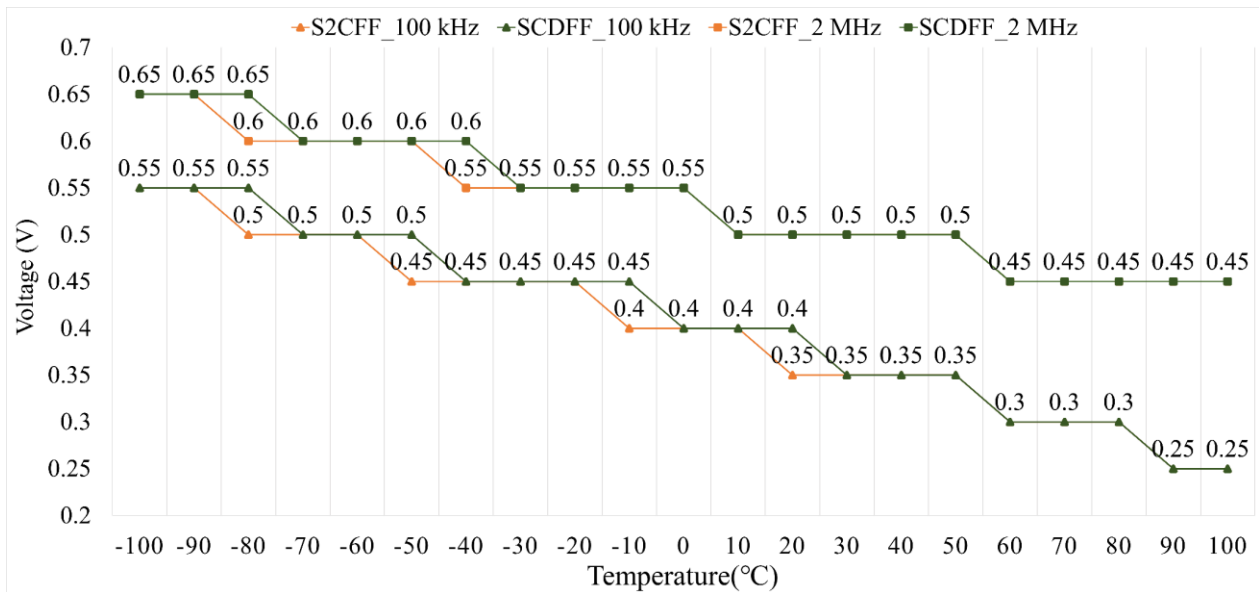
Figure 3.2-1. Minimum functional voltage for operating frequency of 100 kHz and 2 MHz.

3.3 Evaluation Results of the Second Step Using Monte-Carlo Simulations.

As discussed in Section 2.5, the proposed evaluation process performs further tests including device mismatches using Monte-Carlo simulations. It covers temperature from -100 °C to 100 °C with 10 °C step and operating frequency of 100 kHz and 2 MHz. Table 4 shows the

result at -100°C as an example. Note that the minimum V_{DD} from corners is the minimum supply

voltage from the first step (from Section 3.2) while the minimum VDD from MC is one from the

second step. It is the minimum supply voltage passing the functionality at all the 1,000 Monte-

Carlo samples. SCDFF shows the best (or lowest) FoM. In the second step, the supply voltage

increases from 0.55 V to 0.7V for TSPC and CSFF. The increment increases their FoM.

Also, TCFF fails the test even with the supply voltage of 1 V due to contention caused by

device mismatch. Circuit failure is discussed in Section 3.4 in detail.

Considering the effect of temperature dependence discussed in Section 1.2.2, the FoM for

each temperature point is evaluated with the supply voltage range starting from the minimum

supply voltage from the corner simulations at the temperature. The result shows that, at each

temperature, all flip-flops obtain the minimum FoM at the minimum supply voltage from the MC

simulations.

Table 4. 1000-Sample Monte-Carlo simulation result at -100 °C and 100 kHz frequency.

Flip-flop	Minimum V_{DD} from corners (V)	Minimum V_{DD} from MC (V)	Average PDP (μ) (10^{-15} J)	Standard Deviation (σ) (10^{-16})	FoM (= $\mu+3\sigma$) (10^{-15} J)
ACFF	0.60	0.65	17.890	10.590	21.067
S^{2}CFF	0.55	0.55	13.890	1.464	14.329
SCDFF	0.55	0.55	9.672	2.748	10.496
TGFF	0.55	0.55	17.660	1.971	18.251
TSPC	0.55	0.70	25.930	4.005	27.132
CSFF	0.55	0.70	20.230	2.980	21.124

Figure 3.3-1 shows the FoM for the operating frequency of 100 kHz. At temperature below -30 ℃, TSPC shows the worst (highest) FoM since it needs higher supply voltage to overcome the contention caused failure at low temperature. At temperature higher than -30 ℃, ACFF shows the highest FoM. Affected by its potential contention, the supply voltage for ACFF is hardly to be reduced. SCDFF shows the minimum FoM across temperature so that it is evaluated as the most energy-efficient device for 100 kHz operating frequency. CSFF shows the same FoM only with SCDFF only at one temperature point (-10 ℃).
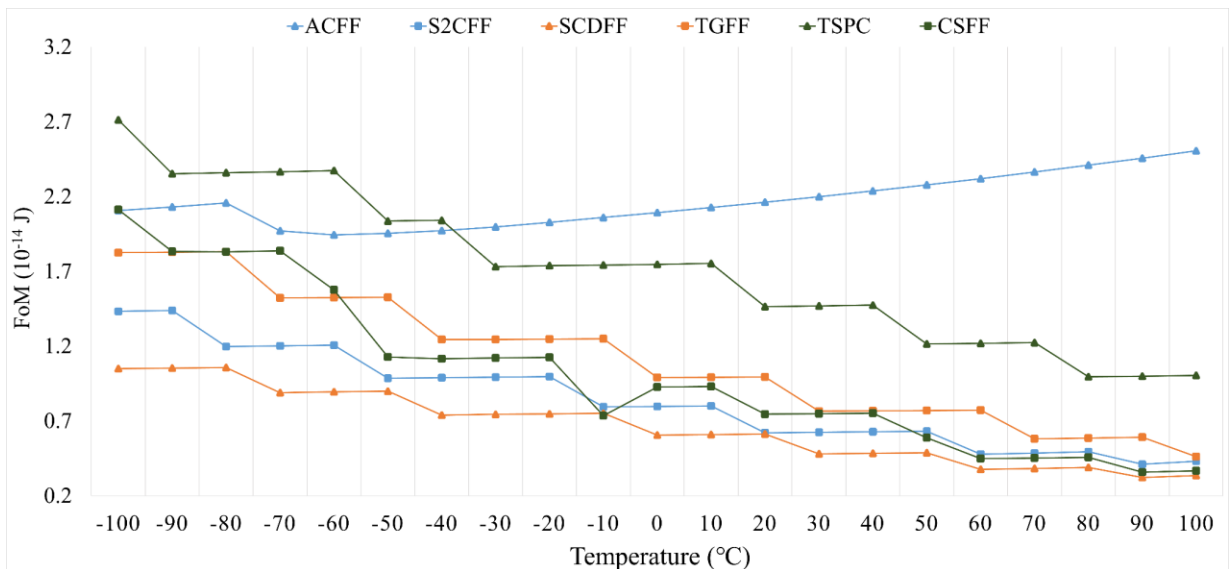

Figure 3.3-1. Evaluation result of the second step across temperature at 100 kHz.

Figure 3.3-2 shows the FoM for the operating frequency of 2 MHz. Compared with one for 100 kHz, it shows higher FoM because the flip-flops require higher supply voltage to obtain shorter delay. The result shows that SCDFF achieves overwhelming FoM than the other flip-flops.

Figure 3.3-3 shows the accumulated FoM, which is valid for a linearly changing temperature profile. It also shows that SCDFF is the best choice for both operating frequencies. If

temperature changes in a different way, weighting factor can be applied to the FoM for each temperature, and this evaluation process can provide an update FoM. However, SCDFF is still the best flip-flop since it shows the lowest FoM at all the temperature.
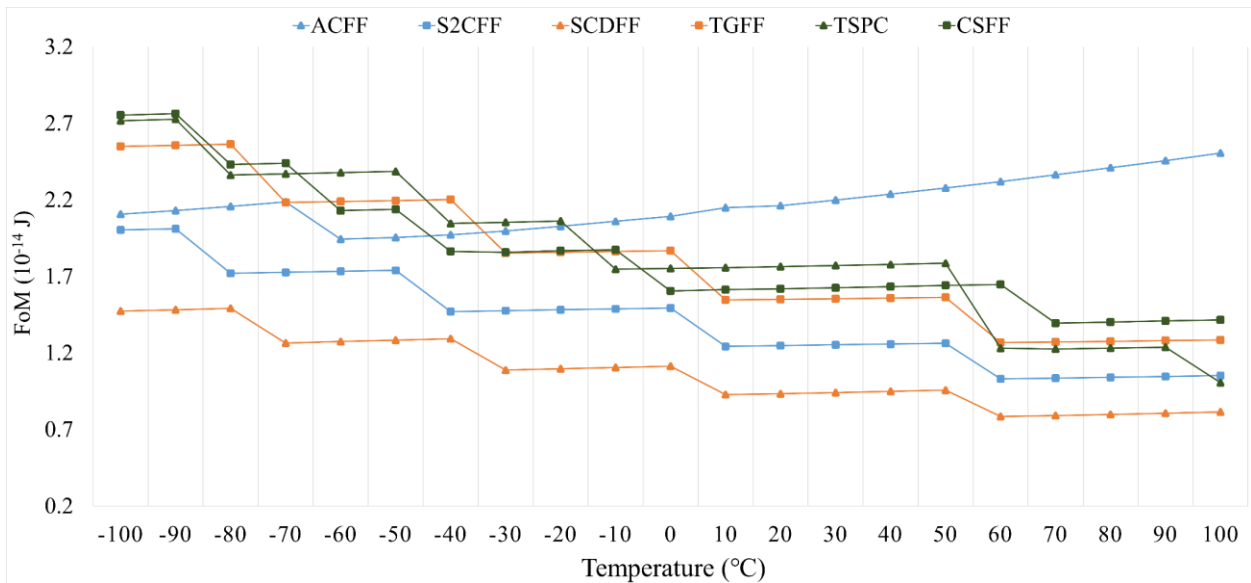

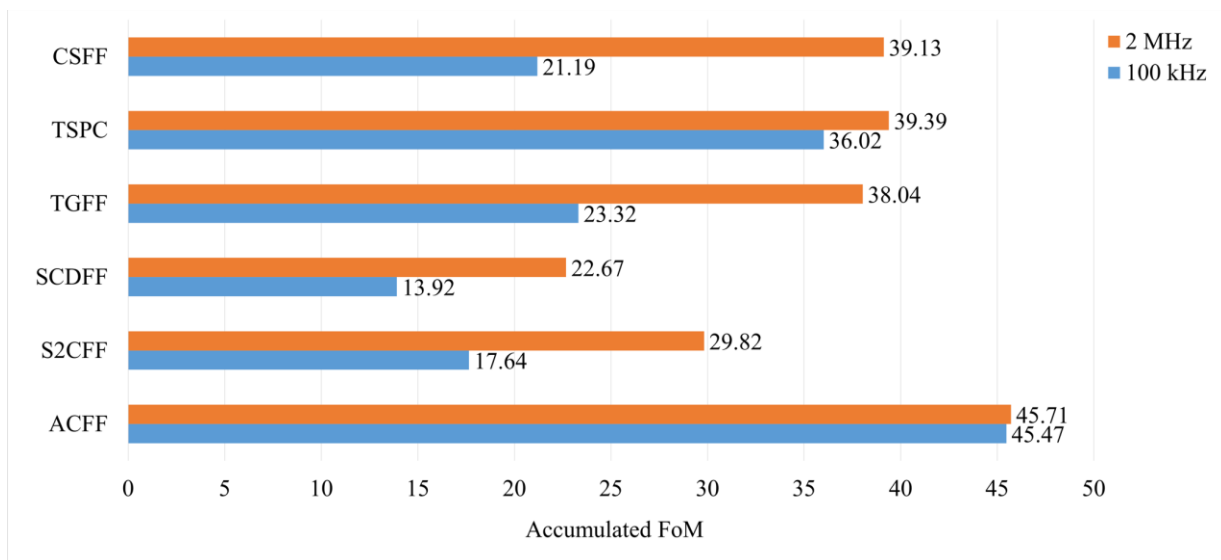**Figure 3.3-2. Evaluation result of the second step across temperature at 2 MHz.**

Figure 3.3-3. Accumulated FoM across temperature assuming a linearly changing temperature profile.

34

3.4 Analysis of Device Failures and Energy Efficiency

3.4.1 WPMS Retention Failure from Pass Transistor

Figure 3.4-1 shows the waveform of internal nodes of WPMS at low temperature and low supply voltage. Figure 3.4-2 shows the schematic for the failure mechanism. If DN = 1, CKB = 0, input D = 1, DI = 0, DP = 0 (denoted as green in the schematic), when CKB rises to high, DN is supposed to be pulled down as DI for a correct logic operation. However, the PMOS pulls DN up thus causing contention at DN. The NMOS pass transistor in the important path weakens the timing characteristic and robustness under irregular PVT condition, resulting in the circuit contention and thus the failure.
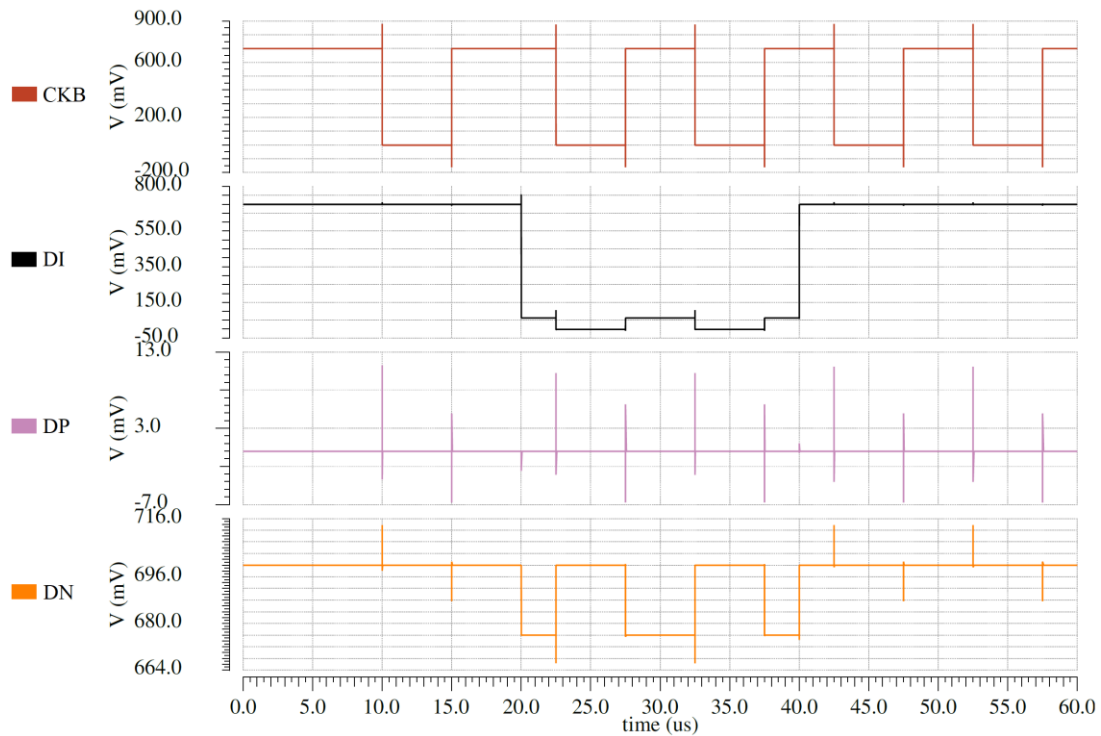

Figure 3.4-1. Contention-caused retention failure of WPMS under PVT variation.
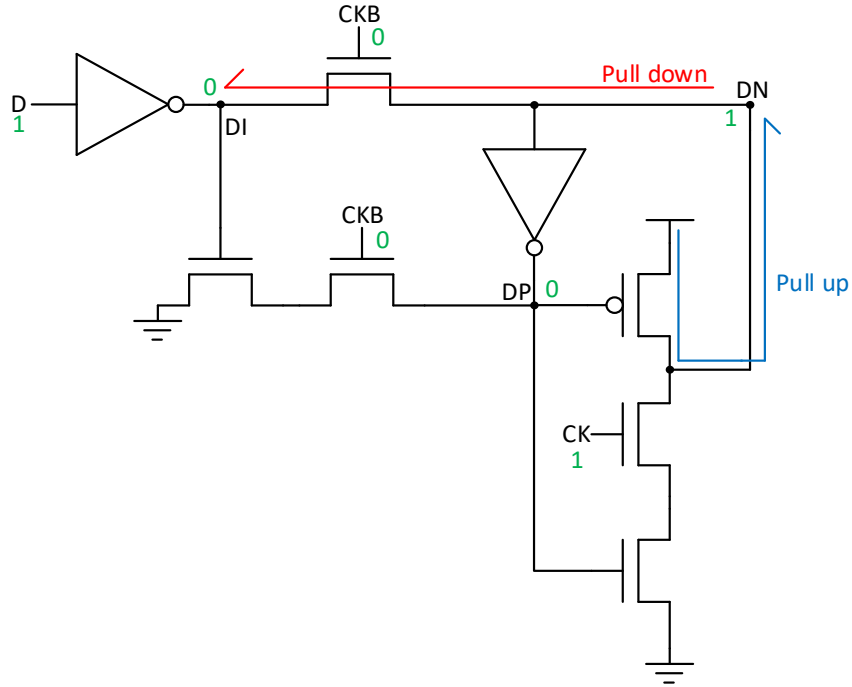
Figure 3.4-2. Schematic of the latch in WPMS with contention on DN.

Such contention is obviously avoided at the fast-slow corner or smaller P/N ratio (≤ 0.65). It proves that the functional failure comes from the pass transistor.

3.4.2 TCFF Failure from Contention

TCFF fails due to contention, which also causes WPMS to fail. Figure 3.4-3 shows the waveform of internal signals of TCFF at 0.7 V and 100 kHz. Figure 3.4-4 shows the schematic with noted contention. In corner simulations in Section 3.2, TCFF shows good performance in the condition, but reliability cannot be fulfilled with Monte-Carlo simulations. The waveforms show that N2 cannot be correctly pulled to high through VD2 due to contention caused by N3 and VD2. N1 has the opposite value to the input D. When CLK and D is 0, N1 is 1, N2 is 0, and N3 is 1. D rises to 1 at 20 µs which connects N2 to both pull-up and pull-down networks at the same time.
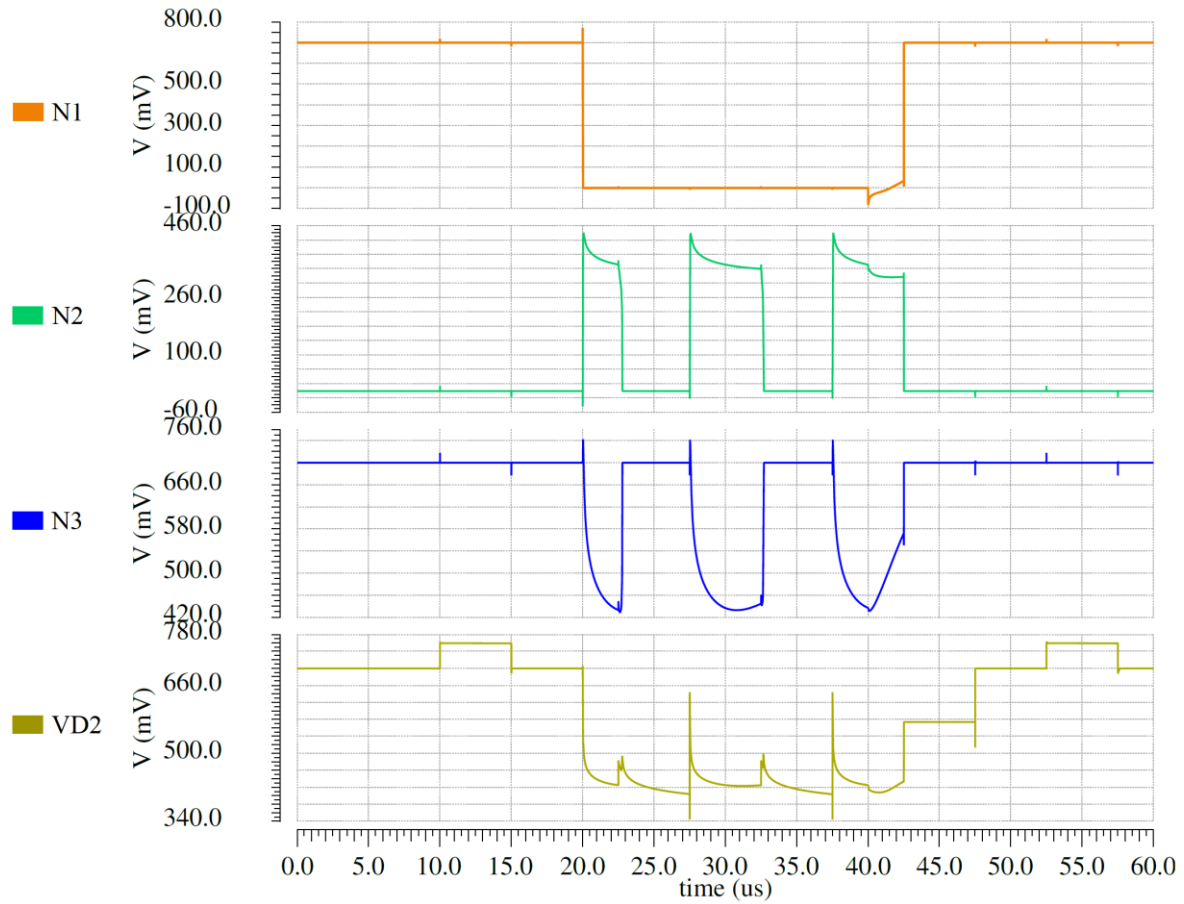
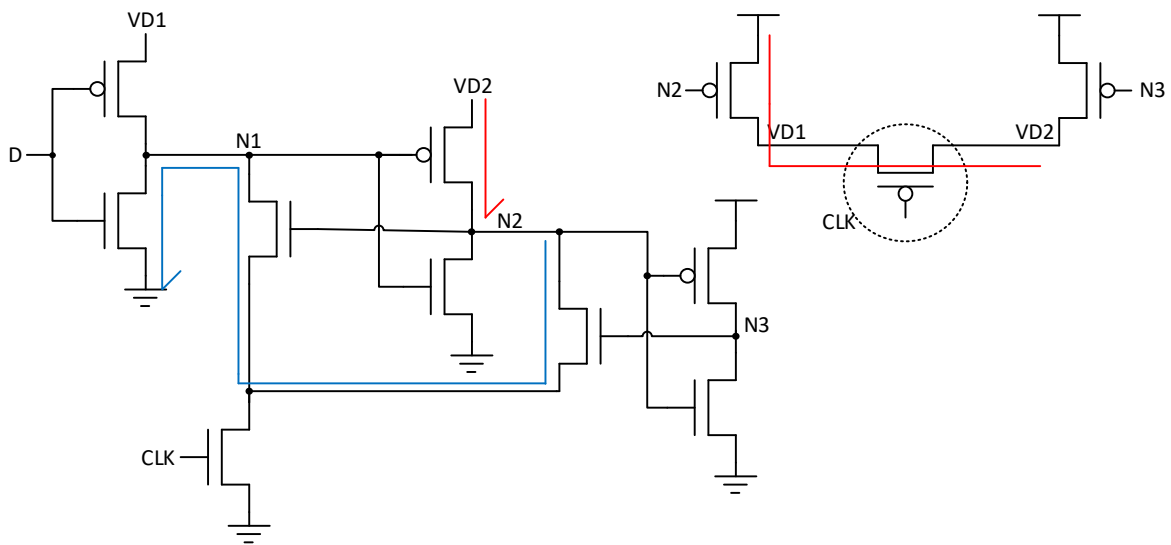**Figure 3.4-3. Waveforms of TCFF with failure.**

Figure 3.4-4. Schematic of TCFF with contention on N2.

37

Figure 3.4-5 shows the waveform of a functional case in the same condition. The red circled trace is similar to the failure case. VD2 has a pull-down phase, but the circuit keep properly operating.
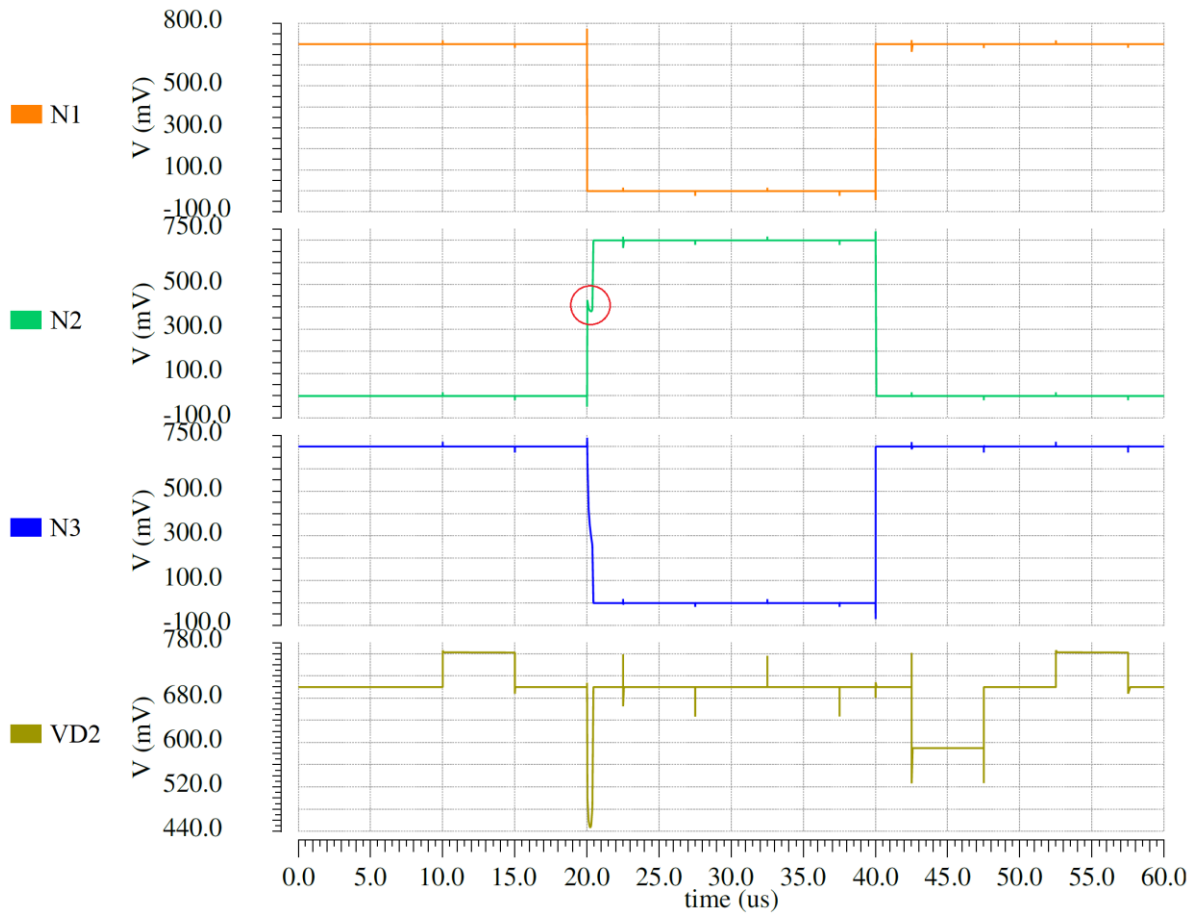
Figure 3.4-5. Waveforms of TCFF with functionality.

3.4.3 Potential Contention in TSPC

Figure 3.4-6 shows the failed operation of TSPC with a Monte-Carlo simulation at -20 °C, supply voltage of 0.5 V, and operating frequency of 2 MHz. 'Q_Failure' shows an obvious logic error compared with 'Q_Functional' and 'Comp' (ideal Q). The failure comes from L2 pulled up persistently. It prevents L3 to be pulled up. As CLK rises, L2 should be pulled down, and thus L1 should be pulled up. However, at the condition, contention occurs, and L1 is pulled down prior to the transition of L2. It pulls up L2, making the following nodes into the opposite value to the desirable ones finally.
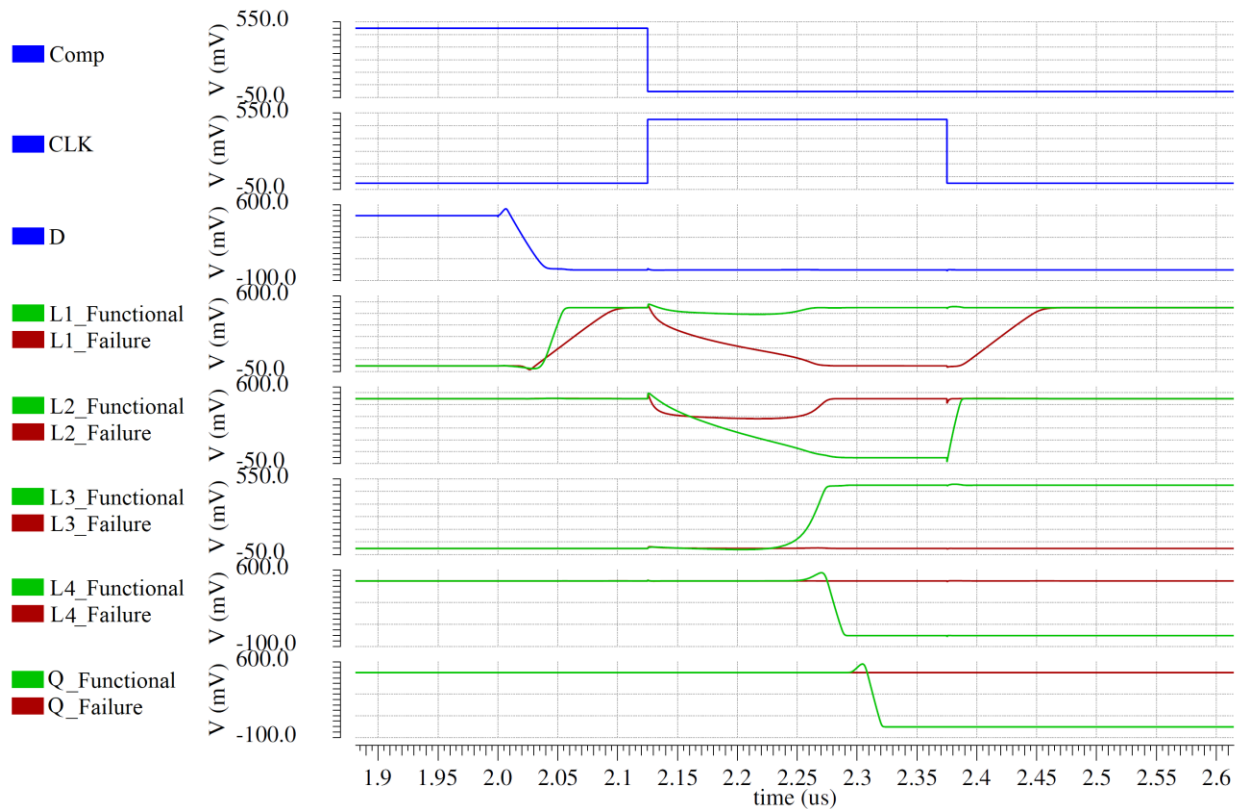
Figure 3.4-6. Waveforms of TSPC with and without failure.

Figure 3.4-7 shows the schematic of TSPC in that condition, the logic value before CLK rising is noted as green in the figure. It shows that as CLK rises, L1 is connected to a discharge path which has contention with the discharge path of L2.
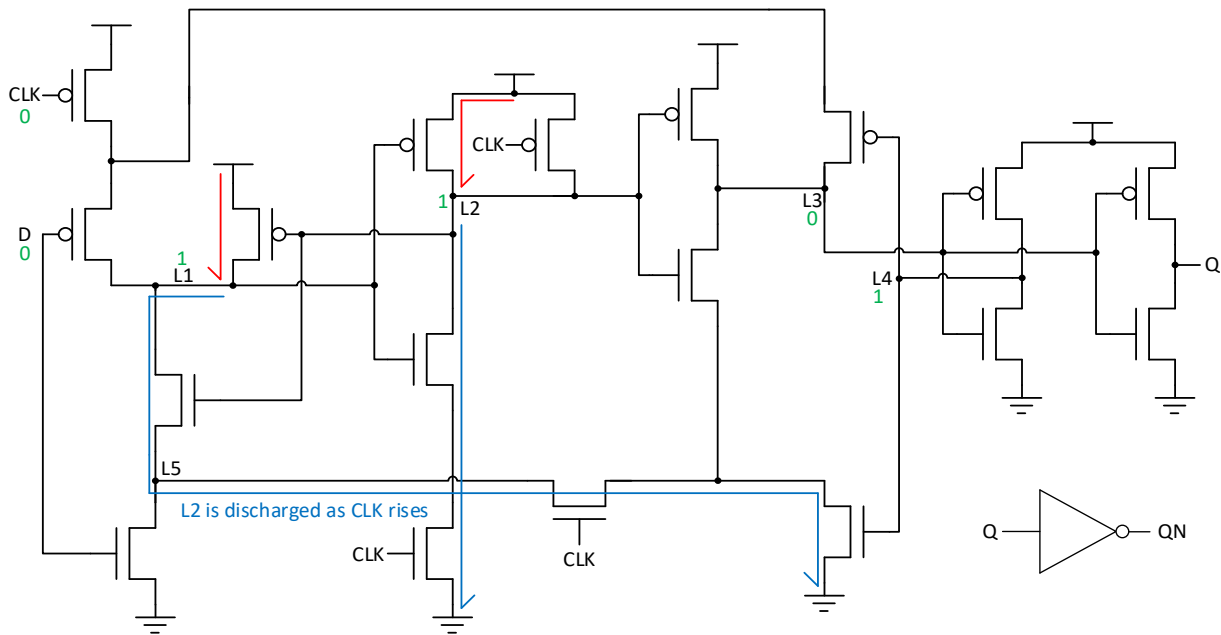
Figure 3.4-7. Schematic of TSPC in failure condition.

3.4.4 Unstable Phase in CSFF from Floating Nodes

Figure 3.4-8 shows a brief schematic of CSFF. It shows that CSFF is pre-charged when CLK is 0 and can only be discharged with sensed difference of previous output Q_{prev} and input D. Also, node CS controls the output QN and Q. The unstable phase can occur when D = 0 as CLK rises. In the condition, CS is neither pulled up nor down (closed transistor is marked as red) and becomes floating, which causes the output unstable.
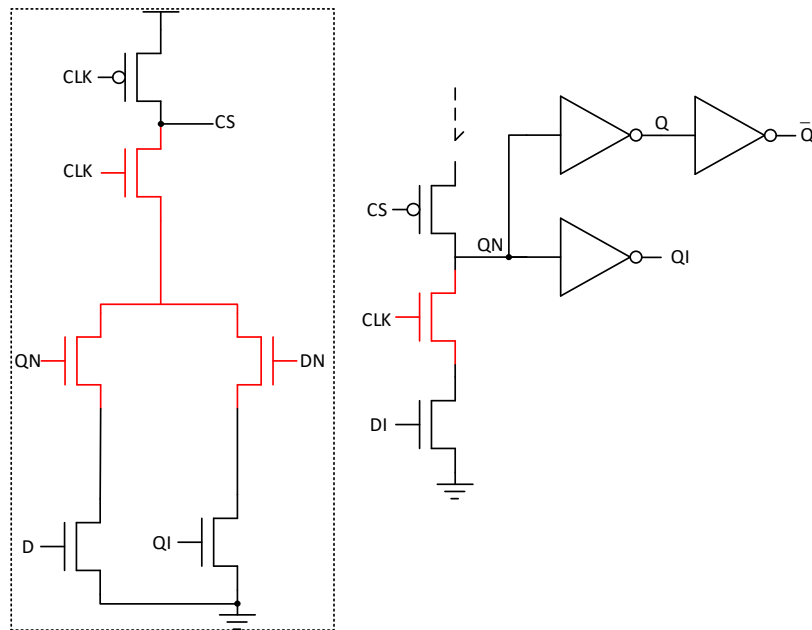
Figure 3.4-8. Brief schematic of CSFF.
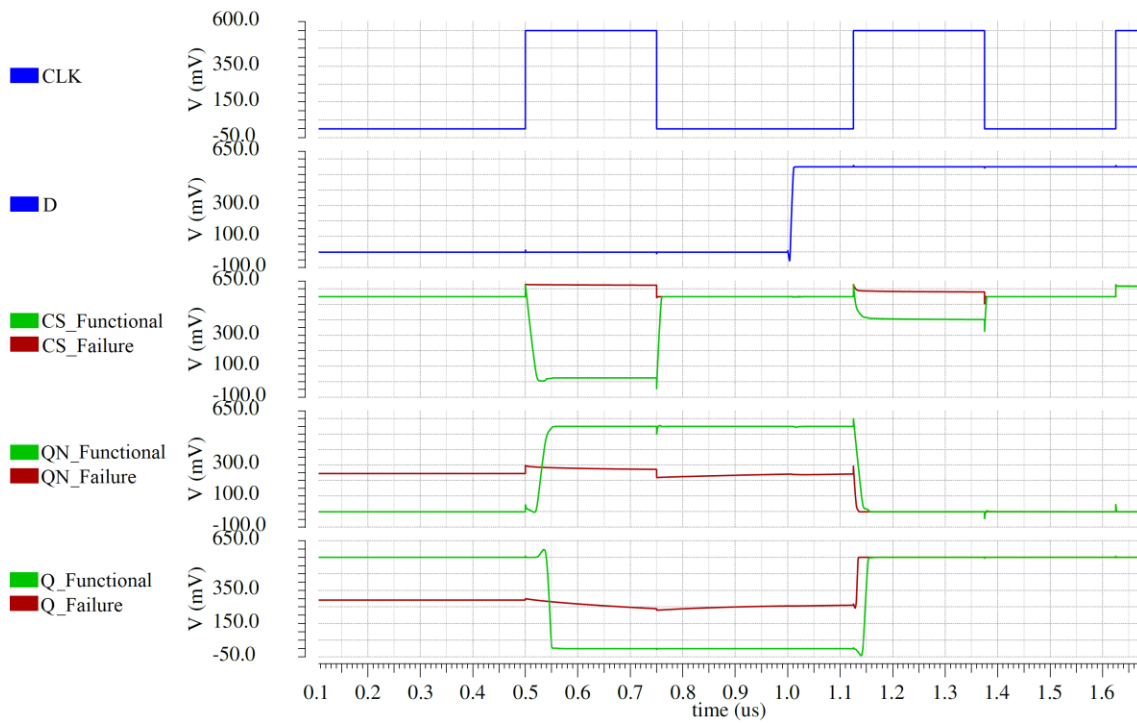
Figure 3.4-9. Waveforms of initialization phase for CSFF.

41

Figure 3.4-9 shows an example of simulated CSFF where the initial floating value of the output Q affects the functionality of the change-sensing structure. When CLK = 0, CS is pulled up. After CLK rises, CS cannot be pulled down through the path controlled by DN and QI since nodes related to Q_{prev} floats.

3.4.5 Write-Failure in ACFF from Weak NMOS Pull-Up

Figure 3.4-10 shows a write-failure case of ACFF at -10 °C, supply voltage of 0.55 V, and operating frequency of 2 MHz. Figure 3.4-11 shows the schematic for that condition. Before CLK rises, $Q_{prev} = 1$ and current $D = 0$. Thus, C1 and C2 are supposed to be 0 and 1 through the retention of the slave latch, respectively. However, weak pull-up strength of NMOS M6 makes C1 stay as high, making Net2 and Net4 charged. Thus, Net3 is unexpectedly pulled down.
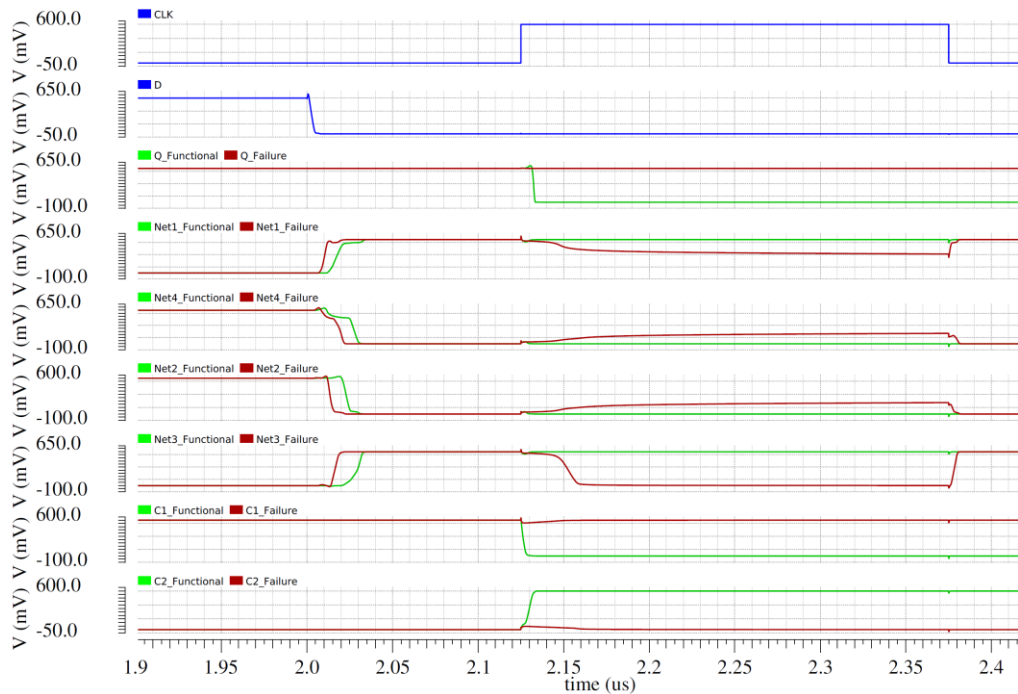
Figure 3.4-10. Observed write-failure of ACFF.
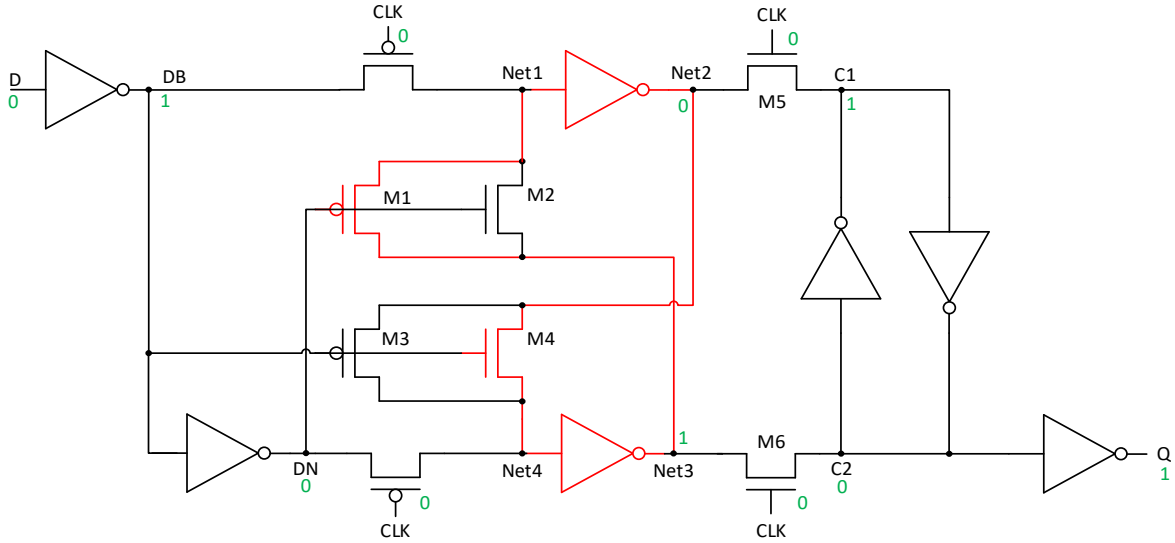
Figure 3.4-11. Schematic of ACFF in failure condtion.

The schematic denotes the logic values before the rising of CLK as green. M1 and M4 are closed to perform the retention of master latch (red path).

3.4.6 Energy Efficiency Analysis

Figure 3.4-12 shows the minimum supply voltage of TGFF across temperature from both corner and Monte-Carlo simulations. It shows no difference between the two simulations, which means TGFF is robust again device mismatch due to its robust circuit and contention-free characteristics. Flip-flops such as SCDFF and S^2CFF, which is fully static and contention-free, shows the similar result since it is not affected by device mismatch. Among TGFF, SCDFF, and S^2CFF, TGFF shows higher energy consumption due to many clocked transistors. SCDFF consumes less energy than S^2CFF since it removes internal clock toggling while S^2CFF has internal clock toggling under some conditions, resulting in half-redundant-free, as discussed in Section 2.2.4.

43
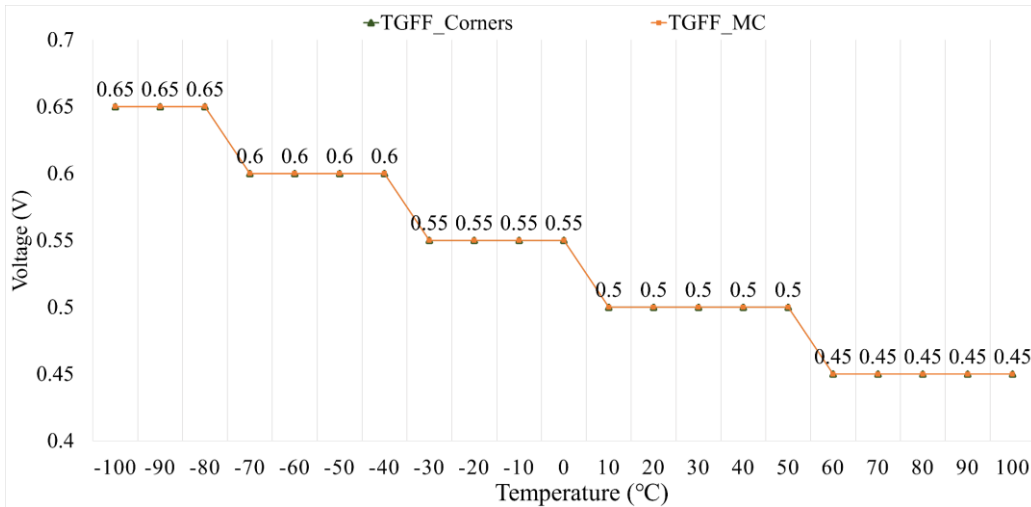
Figure 3.4-12. Minimun supply voltage for TGFF across temperature.

Figure 3.4-13 shows the minimum supply voltage of CSFF from the same simulations. From the Monte-Carlo simulations with device mismatch, the minimum supply voltage is dramatically increased due to functional failure at lower supply voltage. This issue also happens to ACFF and TSPC. The flip-flops, which is not fully static or not contention-free, require higher supply voltage for their reliability when device mismatch is considered.
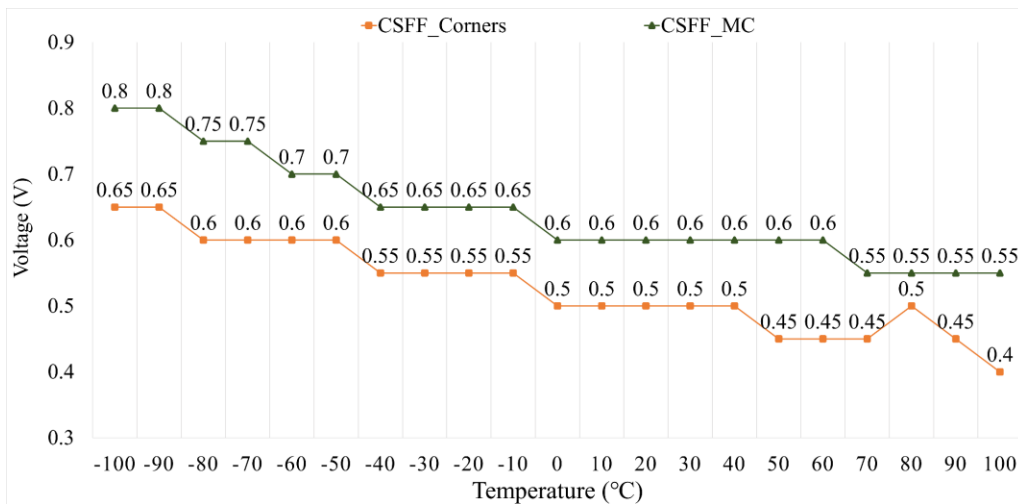
Figure 3.4-13. Minimun supply voltage for CSFF across temperature.

3.5 Conclusion

This chapter discusses the result of the evaluation. In the first step using corner simulations, WPMS fails the worst case due to weak robustness and timing characteristic by the pass transistor in the main path. TCFF requires the highest minimum supply voltage at because of significant contention under low supply voltage, creating more performance degradation in the following second step using Monte-Carlo simulations. Other devices show the similar minimum functional supply voltage.

In the second step, the minimum supply voltage of TSPC and CSFF increase significantly since the contention or potential strength imbalance results in circuit functional failure from device mismatch. SCDFF achieves the minimum (best) FoM for the both target frequencies of 100 kHz and 2 MHz, which means that it is the most energy-efficient flip-flop for a target linearly changing temperature profile.

In addition to the evaluation, performance of flip-flops is analyzed. The failure mechanisms of WPMS and TCFF are discussed in detail. In WPMS, a NMOS pass transistor in the critical path weakens the robustness significantly and causes retention failure. In TCFF, process variation and mismatch create contention and thus reliability issue. CSFF, ACFF and TSPC present degraded FoM since their minimum supply voltage becomes higher by weak robustness or potential contention. S^2CFF and TGFF are fully static and contention-free, but they show worse FoM than SCDFF by internal clock toggling.

4.0 Conclusion and Future Work

This thesis presents an evaluation method for flip-flops in AVS system and circulating temperature. Power-delay product, PDP, is used as the FoM for energy consumption evaluation. Seven recently published flip-flops and conventional TGFF are re-sized for fair comparison and evaluated by transistor-level simulation. The evaluation has 2 steps including corner test and Monte-Carlo simulation. In the corner test, the minimum supply voltage for the flip-flop is coarsely found. Monte-Carlo simulation further validates the minimum supply voltage considering robustness of the circuit and finds the FoM ('average $+ 3 \times$ sigma' of tested PDP values). Also, the failure mechanisms of the flip-flops are analyzed based on simulation result. In this work, it is found that the minimum supply voltage for voltage scaling mainly depends on static or dynamic operation, contention, and robustness of the flip-flop. Flip-flops with contention or loss of robustness fail at higher supply voltage and does not achieve much energy saving by voltage scaling. For flip-flops that are fully static and contention-free, energy performance mainly depends on internal clock toggling. Finally, SCDFF is evaluated as the most energy-efficient flip-flop for the target temperature profile.

In the future work, the performance of the selected flip-flops can be improved for the target temperature by optimizing the size of each transistor, especially for the flip-flops with a robustness issue. A new topology of flip-flop can be also proposed to obtain better FoM. If the FoMs show a different best flip-flop at each temperature, the new FoM should be proposed using weighting factors since the accumulated FoM of this work only works for the application with a linearly changing temperature profile.

Appendix A Program Codes for Transistor Sizing in Voltage-Temperature Variation

```python
import csv
import numpy as np
import matplotlib.pyplot as plt
import matplotlib as mp

class WidthSolution:
    def __init__(self):
        self.data = fed("s.csv")
        self.voltages = list(range(200, 1000 + 50, 50))
        self.widths = width_generator("720n", "4.32u", 180)
        self.temperatures = list(range(-100, 100 + 20, 20))
        for volNum in range(0, len(self.voltages)):
            if self.voltages[volNum] == 1000:
                self.voltages[volNum] = "1"
            elif self.voltages[volNum] > 1000:
                self.voltages[volNum] = self.voltages[volNum] / 1000
            else:
                self.voltages[volNum] = f"{self.voltages[volNum]}m"
        self.score_sheet = []


    def scoring(self):
        for width in self.widths:
            width_score = []
            for temperature in self.temperatures:
                for voltage in self.voltages:
                    for data_row in range(0, len(self.data)):
                        if len(self.data[data_row]) != 0:
                            if self.data[data_row][0] == f"Parameters: Vdd={voltage}, Wp={width}, Temp={temperature}":
                                current_result = self.data[data_row + 1][6]
                                width_score.append(float(current_result))
            width_mean = np.mean(width_score)
            width_sigma = np.std(width_score)
            width_fom = width_mean + 3 * width_sigma
            self.score_sheet.append({"Width": width, "Mean": width_mean, "Sigma": width_sigma, "FoM": width_fom})
        return self.score_sheet
```

Appendix B Program Codes for Flip-flop Functionality Test with PVT Variation

```python
import csv

def indexing(filename, corner, lowest_vdd, highest_vdd, voltage_scaling_step):
    data_file = csv.reader(open(filename, "r"))
    data = []
    for row in data_file:
        data.append(row)
    if corner == 0:
        corner_name = "TT"
    elif corner == 1:
        corner_name = "FF"
    elif corner == 2:
        corner_name = "FS"
    elif corner == 3:
        corner_name = "SF"
    elif corner == 4:
        corner_name = "SS"
    else:
        corner_name = "null"
    # index_head = [corner_name, "-101", "-97.7", "-88", "-72.6", "-52.5", "-29.1", "-4",
    #          "21.1", "44.5", "64.5", "80", "89.7", "93"]
    index_head = [corner_name, "-100", "-90", "-80", "-70", "-60", "-50", "-40",
            "-30", "-20", "-10", "0", "10", "20", "30", "40", "50", "60", "70", "80", "90", "100"]
    inner_index = [index_head]
    number_of_device = 8
    corner_offset = corner
    voltage_lane    =    list(range(lowest_vdd,    highest_vdd    +    voltage_scaling_step,
voltage_scaling_step))
    temp_lane = index_head.copy()
    temp_lane.remove(temp_lane[0])

    for num in range(1, number_of_device + 1):
        current_device = [f"Q{num}"]
        for temp in temp_lane:
            min_vdd = 0
            threshold = 0
            for vdd in voltage_lane:
                if threshold == 0:
                    for i in range(0, len(data)-1):
                        if  len((data[i]))  !=  0  and  data[i][0]  ==  f"Parameters:  Temp={temp},
VDD={vdd}m":
```

48

```python
                    if  data[i+num][8  +  corner_offset]  !=  "eval  err"  and  data[i+num+8][8  +
corner_offset] != \
                        "eval err" and data[i+num+16][8 + corner_offset] != "eval err":
                      if float(data[i+num][8 + corner_offset]) >= 9e-16 and \
                          float(data[i+num+8][8 + corner_offset]) >= 1e-12 and \
                          float(data[i+num+16][8 + corner_offset]) >= 1e-12:
                        threshold = 1
                        min_vdd = vdd
                        break
            else:
                break
        current_device.append(f"{min_vdd}m")
      inner_index.append(current_device)
    return inner_index


  class _CornersLowestVDD:
    def __init__(self, lowest_vdd, highest_vdd, voltage_scaling_step):
      self.indexTT  =  indexing("FoM_simulation_1129.0.csv",  0,  lowest_vdd,  highest_vdd,
voltage_scaling_step)
      self.indexFF  =  indexing("FoM_simulation_1129.0.csv",  1,  lowest_vdd,  highest_vdd,
voltage_scaling_step)
      self.indexFS  =  indexing("FoM_simulation_1129.0.csv",  2,  lowest_vdd,  highest_vdd,
voltage_scaling_step)
      self.indexSF  =  indexing("FoM_simulation_1129.0.csv",  3,  lowest_vdd,  highest_vdd,
voltage_scaling_step)
      self.indexSS  =  indexing("FoM_simulation_1129.0.csv",  4,  lowest_vdd,  highest_vdd,
voltage_scaling_step)
      self.indexAll = [self.indexTT, self.indexFF, self.indexFS, self.indexSF, self.indexSS]
      self.lowest_vdd = lowest_vdd
      self.deviceList = ["Q1", "Q2", "Q3", "Q4", "Q5", "Q6", "Q7", "Q8"]
      self.Corners = ["TT", "FF", "FS", "SF", "SS"]
      self.temperatureSheet = ["-100", "-90", "-80", "-70", "-60", "-50", "-40", "-30", "-20", "-
10",
                     "0", "10", "20", "30", "40", "50", "60", "70", "80", "90", "100"]
      self.tableHead = ["Device"] + self.temperatureSheet
      self.resultTable = [self.tableHead]

    def filter(self):
      local_result = []
      for device in self.deviceList:
        device_result = [device]
        for temp in self.temperatureSheet:
          failure_flag = 0
          min_in_temperature = f"{self.lowest_vdd}m"
          for corner in self.Corners:
            for index in self.indexAll:
```

```python
            if index[0][0] == corner:
                for temperature_num in range(0, len(index[0])):
                    if index[0][temperature_num] == temp:
                        for row_num in range(0, len(index)):
                            if index[row_num][0] == device:
                                current_result = index[row_num][temperature_num]
                                if int(current_result[:-1]) < self.lowest_vdd:
                                    failure_flag = 1
                                elif int(current_result[:-1]) > int(min_in_temperature[:-1]):
                                    min_in_temperature = current_result
        if failure_flag == 0:
            device_result.append(min_in_temperature)
        else:
            device_result.append(f"*{min_in_temperature}")
    local_result.append(device_result)
return local_result
```

Appendix C Energy Performance Gained from AVS

Appendix Figure 1 compares the accumulated FoMs with and without applying AVS technique. Most flip-flops reduce the accumulated FoM by ~30% except for ACFF. ACFF does not show any difference since the supply voltage cannot be reduced further at different temperature due to the robustness issue discussed in Section 2.2.5 and illustrated in Section 3.4.5.
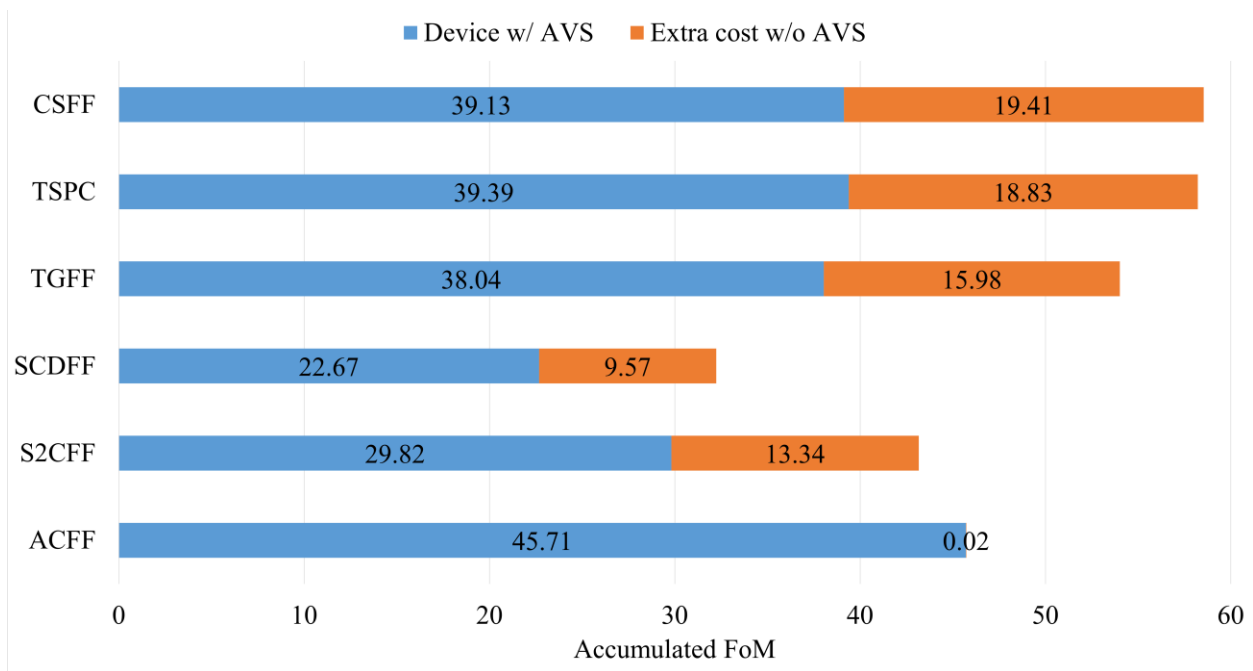
Appendix Figure 1. Comparison of flip-flops with or without AVS at the target operating frequency of 2 MHz.

Bibliography

[1]   Y. Lu, Q. Shao, H. Yue, and F. Yang, "A Review of the Space Environment Effects on Spacecraft in Different Orbits," *IEEE Access*. 2019, doi: 10.1109/ACCESS.2019.2927811.

[2]   W. F. Clark, B. El-Kareh, R. G. Pires, S. L. Titcomb, and R. L. Anderson, "Low Temperature CMOS—A Brief Review," *IEEE Trans. Components, Hybrids, Manuf. Technol.*, 1992, doi: 10.1109/33.148509.

[3]   W. Liao, L. He, and K. M. Lepak, "Temperature and supply voltage aware performance and power modeling at microarchitecture level," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, 2005, doi: 10.1109/TCAD.2005.850860.

[4]   R. S. C. Cobbold, "Temperature effects in m.o.s. transistors," *Electron. Lett.*, 1966, doi: 10.1049/el:19660160.

[5]   S. Kalra, "Effect of temperature dependence on performance of digital CMOS circuit technologies," 2013, doi: 10.1109/ICSPCom.2013.6719819.

[6]   J. Jose, A. Ravindran, and K. K. Nair, "Study of Temperature Dependency on MOSFET Parameter using MATLAB," *Int. Res. J. Eng. Technol.*, 2016.

[7]   T. Sakurai and A. R. Newton, "Alpha-Power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas," *IEEE J. Solid-State Circuits*, 1990, doi: 10.1109/4.52187.

[8]   A. Dasdan and I. Hom, "Handling inverted temperature dependence in static timing analysis," *ACM Trans. Des. Autom. Electron. Syst.*, 2006, doi: 10.1145/1142155.1142158.

[9]   A. Wang and B. H. Calhoun, *Sub-threshold Design for Ultra Low-Power Systems*. 2007.

[10]   R. Kumar and V. Kursun, "Temperature-adaptive body-bias and supply voltage scaling for enhanced energy efficiency in nano-CMOS circuits," 2007, doi: 10.1109/MWSCAS.2007.4488675.

[11]   J. Zhu, N. Bai, and J. Wu, "Process-temperature-frequency adaptive voltage scaled SRAM system for power reduction," in *ICM 2011 Proceeding*, 2011, pp. 1–4, doi: 10.1109/ICM.2011.6177409.

[12]   A. Chhabra *et al.*, "Temperature-based adaptive memory sub-system in 28nm UTBB FDSOI," 2016, doi: 10.1109/ISCAS.2016.7527416.

[13]   N. H. E. Weste and D. M. Harris, *CMOS VLSI Design*. 2013.

[14]   G. Gerosa *et al.*, "A 2.2 W, 80 MHz Superscalar RISC Microprocessor," *IEEE J. Solid-*

State Circuits, 1994, doi: 10.1109/4.340417.

[15] D. Marković, B. Nikolić, and R. W. Brodersen, "Analysis and design of low-energy flip-flops," 2001, doi: 10.1145/383082.383093.

[16] Dejan Markovic, J. W. Tschanz, and V. K. De, "Transmission-gate based flip-flop," US6642765B2, 2003.

[17] K. Singh, S. C. Tiwari, and M. Gupta, "A modified implementation of tristate inverter based static master-slave flip-flop with improved power-delay-area product," *Sci. World J.*, 2014, doi: 10.1155/2014/453675.

[18] Y. Cai, A. Savanth, P. Prabhat, J. Myers, A. S. Weddell, and T. J. Kazmierski, "Ultra-low power 18-transistor fully static contention-free single-phase clocked flip-flop in 65-nm CMOS," *IEEE J. Solid-State Circuits*, 2019, doi: 10.1109/JSSC.2018.2875089.

[19] G. Shin, E. Lee, J. Lee, Y. Lee, and Y. Lee, "A Static Contention-Free Differential Flip-Flop in 28nm for Low-Voltage, Low-Power Applications," 2020, doi: 10.1109/CICC48029.2020.9075922.

[20] Y. Kim *et al.*, "27.8 A static contention-free single-phase-clocked 24T flip-flop in 45nm for low-power applications," 2014, doi: 10.1109/ISSCC.2014.6757516.

[21] V. L. Le, J. Li, A. Chang, and T. T. H. Kim, "A 0.4-V, 0.138-fJ/Cycle Single-Phase-Clocking Redundant-Transition-Free 24T Flip-Flop with Change-Sensing Scheme in 40-nm CMOS," *IEEE J. Solid-State Circuits*, 2018, doi: 10.1109/JSSC.2018.2863946.

[22] C. K. Teh, T. Fujita, H. Hara, and M. Hamada, "A 77% energy-saving 22-transistor single-phase-clocking D-flip-flop with adaptive-coupling configuration in 40nm CMOS," 2011, doi: 10.1109/ISSCC.2011.5746344.

[23] N. Kawai *et al.*, "A fully static topologically-compressed 21-transistor flip-flop with 75% power saving," *IEEE J. Solid-State Circuits*, 2014, doi: 10.1109/JSSC.2014.2332532.